Mixed signal pcb design and Analog Readout Circuitry for a Pixelated Capacitive Sensor E-nose array

BSc Thesis

P. Olyslaegers
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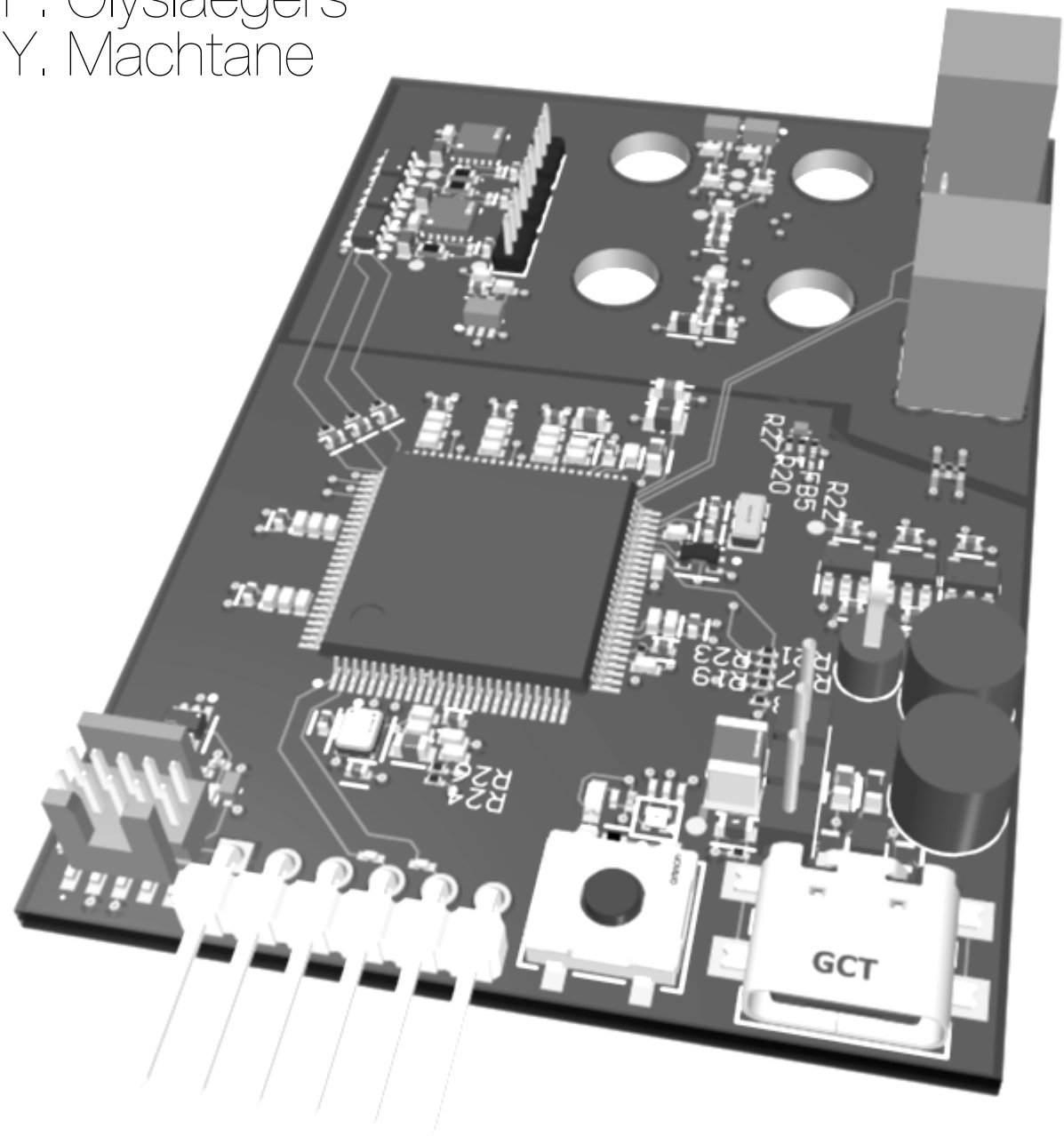

Technische Universiteit Delft

TU Delft

Mixed signal pcb design and Analog Readout Circuitry for a Pixelated Capacitive Sensor E-nose array

BSc Thesis

by

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to obtain the degree of Bachelor of Science
at the Delft University of Technology,

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TU Delft

Abstract

This thesis addresses the development of a supporting electronics platform for a CMOS Pixelated Capacitive Sensor (PCS) array intended for high-sensitivity applications. The work focuses on enabling accurate extraction of capacitance changes at the sensor interface and translating them into signals suitable for digital processing. The design process emphasizes functional integration and signal integrity.

A custom analog front-end was developed, featuring a transimpedance amplifier (TIA) optimized for low input-referred noise and sufficient bandwidth to preserve pixel-level signal integrity. The complete analog signal path supports capacitive measurements with attofarad-level resolution and readout frequencies ranging from 1 MHz to 100 MHz.

The main PCB integrates the readout circuitry with a central microcontroller (MCXN947), DAC-controlled programmable power supplies, and a variety of user interface connectors, all within a compact six-layer mixed-signal stackup. Particular attention was given to minimizing electromagnetic interference (EMI) and power supply noise through careful grounding, power segmentation, and layout strategies. Although the PCB theoretically satisfies most mandatory and trade-off requirements, including spatial and interface constraints, final verification of the noise performance remains pending due to fabrication lead times.

Preface

Every chip requires a reliable interface, and every sensor must be properly read to deliver meaningful data. The goal of this project was to provide the e-nose sensor with the necessary supporting infrastructure and readout circuits, while maintaining an efficient and compact PCB footprint.

We would like to express our sincere gratitude to our daily supervisor, Tao Shen, and our supervisor, Prof. Dr. Ir. Frans Widdershoven, for their invaluable guidance and advice throughout this project. We also warmly thank Dr. Ir. Chris Verhoeven for his insightful discussions and for serving as an inspiring sounding board for our ideas.

Furthermore, we extend our heartfelt thanks to our team members, Chantal Chen, Feifei Lin, Kevin Pang, and Wilson Rong, for their dedication, enthusiasm, and friendship over the past few months.

P. Olyslaegers
Y. Machtane
Delft, June 2025

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Introduction

In large-scale greenhouse cultivation, effective disease control is essential for both crop yield and economic sustainability. For example, in 2020 the average pesticide usage for roses in the Netherlands reached $40.1\ \frac{\text{kg}}{\text{ha}}$ [1]. In a 4-hectare greenhouse, this corresponds to €4,010–€16,040 per treatment, based on current pesticide pricing, excluding labor and application overhead. Reducing unnecessary pesticide use not only minimizes environmental impact but also presents significant cost-saving opportunities.

Electronic nose (e-nose) systems provide a promising route for precision agriculture by enabling early detection and localization of plant diseases. These systems detect Volatile Organic Compounds (VOCs) emitted by infected plants, allowing targeted treatment at the individual plant level. The e-nose architecture employed in this project uses a CMOS Pixelated Capacitive Sensor (PCS) array functionalized with VOC-sensitive inks. These inks exhibit changes in dielectric constant upon exposure to specific gaseous compounds, leading to a corresponding change in capacitance that can be measured electronically.

While the sensing mechanism is conceptually straightforward, its practical implementation involves significant technical challenges. Capacitance variations induced by VOC interactions are extremely small, typically in the attofarad ($10^{-18}F$) range, necessitating low-noise, high-resolution analog front-ends for accurate signal acquisition. In addition, the mixed-signal nature of the system imposes stringent requirements on power distribution, electromagnetic compatibility, and grounding strategies. These constraints become particularly demanding in embedded platforms where size, power, and integration density are limited.

State of the Art

Early e-nose systems were based on large-scale lab instrumentation such as gas chromatography and mass spectrometry, which offered high selectivity and sensitivity but lacked portability and affordability. More recent approaches have leveraged miniaturized sensor arrays, often based on metal-oxide semiconductors, conductive polymers, or capacitive sensing—to provide compact and application-specific alternatives.

Capacitive e-noses based on CMOS technology, such as PCS arrays, offer several advantages: scalability, low power consumption, and compatibility with post-processing steps such as inkjet printing for functionalization. However, their practical deployment depends on the ability to read out the capacitive signals with high fidelity. As sensor dimensions decrease, parasitic effects and noise become dominant, requiring robust circuit design techniques such as differential readout, shielding, and correlated sampling.

An effective analog front-end design requires a careful balance between gain, resolution, and noise to maintain sensitivity while preserving signal integrity. Additionally, the integration of these analog systems with modern microcontrollers, such as the NXP MCXN947, provides a platform for building fully embedded e-nose solutions. However, few existing systems document the challenges and design decisions involved in building such a tightly integrated, high-precision capacitive readout platform.

Thesis Overview

This thesis addresses these challenges through the design of a custom mixed-signal PCB that interfaces a CMOS PCS array with a high-performance microcontroller. The work involves the development of an analog readout chain tailored to small-signal detection, integration of a multi-rail programmable power subsystem, and layout of a compact, interference-resilient board architecture.

The remainder of this thesis is organized as follows:

- Chapter 2 outlines the Program of Requirements for the system and details design constraints.
- Chapter 3 describes the design methodology and analog circuitry, including amplification stages and readout considerations.
- Chapter 4 covers full system implementation, stackup considerations, and mechanical layout.
- Chapter 5 presents performance evaluations and discusses limitations and observations.
- Chapter 6 summarizes the work and provides recommendations for future development.

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Programme of Requirements

In order to evaluate the success and objectives of the project, a **Programme of Requirements** was created. This is divided into two parts for each task. For every task, the structure consists of:

- **Mandatory Requirements (MR):** These must be fulfilled for the project to be considered successful.
- **Trade-Off Requirements (ToR):** These are desirable goals that can be compromised if necessary.

Readout Circuit

Mandatory Requirements (MR.1)

[MR.1.1] The pixel capacitance shall be measured with sufficient resolution to allow detection of changes induced by the presence of VOCs.

[MR.1.2] The measured capacitance values shall be converted into a digital format readable by the MCXN947 microcontroller

[MR.1.3] The analog noise present at the output of the readout circuit shall not exceed the equivalent of four quantization steps of the ADC.

Trade-Off Requirements (ToR.1)

[ToR.1.1] The system should support pixel readout using a variable switching frequency in the range of 1 MHz to 100 MHz.

[ToR.1.2] Only the capacitance variation resulting from interactions with VOCs should be measured, while the intrinsic pixel capacitance should be excluded. This requirement builds upon **[MR.1.1]** to further enhance measurement accuracy.

[ToR.1.3] The analog noise at the output of the readout circuit should not exceed two quantization steps of the ADC when measuring VOC-induced capacitance changes.

Main PCB

Mandatory Requirements (MR.2)

[MR.2.1] The PCB shall support UART for serial communication.

[MR.2.2] The PCB shall support SWD/JTAG for debugging and programming.

[MR.2.3] The PCB shall support USB-C for power and data connectivity.

[MR.2.4] The PCB shall employ the MCXN947 microcontroller as the central unit for control and sensor data processing.

[MR.2.5] The PCB shall have a physical footprint smaller than 84.5 mm × 49 mm, which corresponds to the dimensions of the previous board revision.

[MR.2.6] The PCB shall regulate the 5 V input voltage to 3.3 V and distribute it to all components requiring a 3.3 V supply.

[MR.2.7] The PCB shall be able to deliver the necessary power to all onboard components, taking into account an estimated total current consumption of approximately 100 mA based on the previous board implementation.

[MR.2.8] The PCS array chip shall be supplied with the required power, control and differential clock signals.

[MR.2.9] The PCS chips VDDA and VDDD inputs shall have a variable power source to allow for further testing the optimal voltage level.

[MR.2.10] The output signals from the PCS array chip shall be acquired, processed, and transferred to the MCU for further handling.

[MR.2.11] The noise at the outputs of the chip caused by the combination of crosstalk from the VDDA, VDDE, and VDDD supplies shall not exceed 4 quantization steps of the ADC.

Trade-Off Requirements (ToR.2)

[ToR.2.1] All external connectors and interface ports should be located on a single side of the PCB to simplify cable routing during testing and deployment.

[ToR.2.2] The PCB should provide an option to connect an external lab power supply.

[ToR.2.3] The noise at the outputs of the chip caused by the combination of crosstalk from the VDDA, VDDE, and VDDD supplies should not exceed 2 quantization steps of the ADC.

3

Design Process

3.1. System Overview

The system consists of five main components, as illustrated in Figure 3.1.

- **PCS**: The Pixelated Capacitive Sensor (PCS) array serves as the core sensing element. Each pixel detects changes in capacitance caused by interactions between sensing inks and Volatile Organic Compounds (VOCs).
- **Readout circuit**: This block converts the capacitance variations from the PCS into voltage signals using low-noise analog circuitry, including a transimpedance amplifier and differential gain stages. The processed signal is then digitized for interpretation by the MCU.
- **MCXN947**: The microcontroller coordinates the operation of the system. It receives data from the readout circuit, processes it, and communicates with the user interface. It also controls various peripherals, including programmable DACs.
- **UI**: The user interface (UI) comprises the physical connectors and indicators that enable interaction with the system. This includes SWD/JTAG, UART, and USB-C ports for communication, as well as status LEDs and a reset button for basic user control and feedback.
- **Power**: The power subsystem generates and distributes the required supply rails (e.g., 3.3 V) to all components. It includes low-dropout regulators and decoupling strategies to ensure signal integrity and reduce noise.

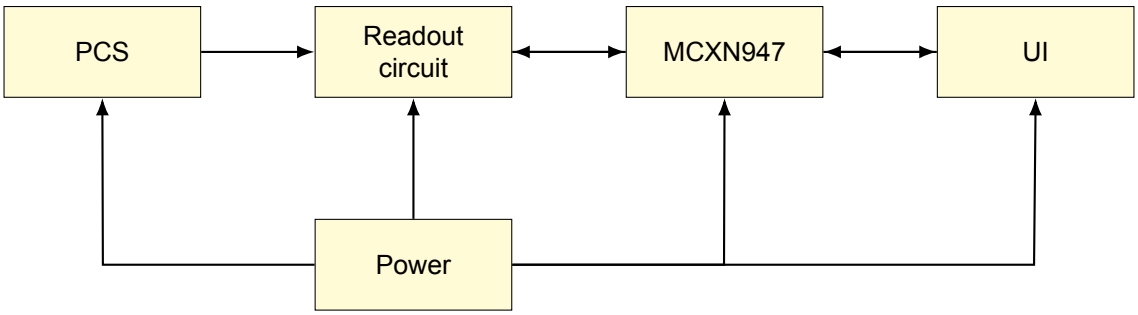


Figure 3.1: Overview of the components in the system

3.2. Background information

As introduced in Chapter 1, the e-nose system developed in this thesis employs a CMOS-based electrode array in which mutual capacitances are formed between adjacent electrodes. Each sense electrode in the array can be individually toggled, while the surrounding electrodes are held at ground potential to create localized capacitance measurements.

As illustrated in Figure 3.2, a sensing ink is deposited between the electrodes onto a self-assembled monolayer (SAM), which serves to improve the fluidic properties of the printed ink droplets prior to the drying or curing process. This structure defines the functional sensing region. The sensing ink, located between the electrode pins, functions as the dielectric medium and thereby determines the relative permittivity during capacitance measurements.

Figure 3.3 depicts the scenario in which Volatile Organic Compounds (VOCs) interact with the sensing ink. The absorption of VOC molecules alters the ink's relative permittivity ϵ_r, which in turn changes the measured capacitance between the electrodes.

A detailed overview of the PCS chip pinout and corresponding functionality of each pin is provided in Appendix D.

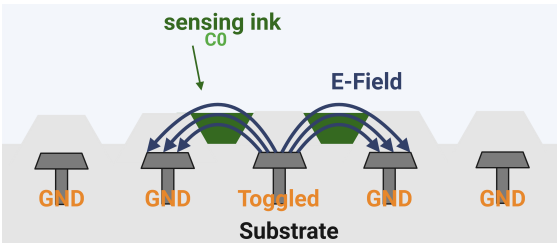


Figure 3.2: The electrodes and sensing ink in the PCS array

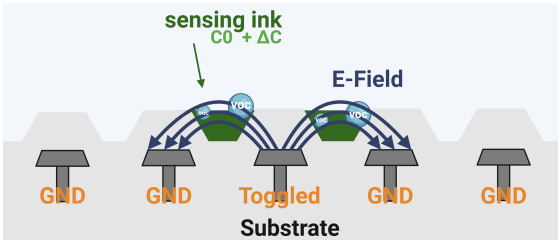


Figure 3.3: The electrodes and sensing ink with VOCs in the PCS array

3.2.1. SLICAP

In this report, circuit noise and transfer function analyses are primarily performed using **SLiCAP**, while circuit verification is conducted with LTspice. SLiCAP is a Python-based symbolic analysis tool that expresses circuit behavior such as transfer functions and noise contributions in terms of symbolic variables, rather than relying solely on fixed numerical values. This symbolic approach offers deeper insight into the circuit's parametric dependencies and relationships, enabling a more comprehensive understanding of its behavior. [2]

3.3. Sensor readout

In this chapter, the expected output characteristics of the PCS array are presented. Various circuit configurations for sensor readout are examined, with an emphasis on accurately detecting the dielectric changes in the sensing ink of the PCS array. Furthermore, the quantization requirements are discussed to ensure that these changes are captured with sufficient fidelity

3.3.1. PCS output

To understand the design of the readout circuit, it is important to first clarify what type of signal is expected from the PCS array. This section outlines the assumptions made regarding the sensor's behavior and the resulting electrical characteristics of its output. These include the nature of the capacitive changes in the sensing ink of the PCS array and how these changes appear as measurable current at the readout interface.

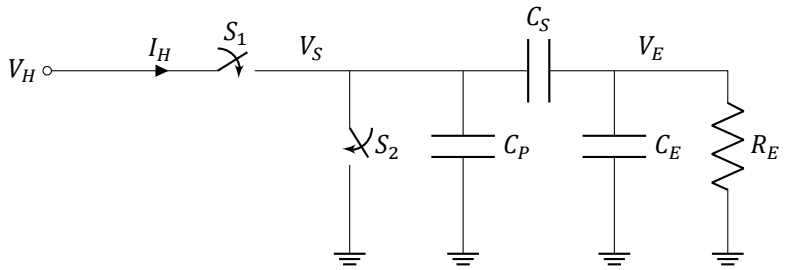


Figure 3.4: Equivalent circuit of a capacitive sensor pixel.

From previous research [3], it is known that a single pixel can be modeled by the equivalent circuit shown in Figure 3.4. Here, C_P is the parasitic capacitance, and C_S is the surface capacitance of a self-assembled monolayer (SAM) on the microectrode surface. The elements C_E and R_E represent the material in the passivation layer valleys, which can be either sensing ink or air. In the case of air, $R_E = \infty$. [4]

The value of C_E is influenced by the presence of specific VOCs , as absorption of these compounds changes the relative permittivity ε_r of the sensing ink, thus altering C_E.[5]

The switches S_1 and S_2 alternately toggle the sensing node voltage V_S between the input voltage V_H and ground, operating at a switching frequency f_s. When S_1 is closed, the pixel connects to V_H, causing a charge build up and when S_2 is closed, the pixel is grounded, and the accumulated charge is discharged.

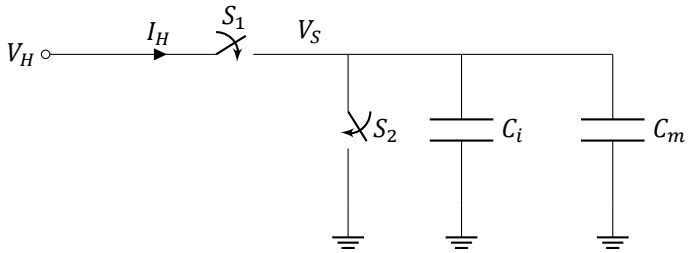


Figure 3.5: Simplified equivalent circuit of a capacitive sensor pixel.

For $f_s \gg \frac{1}{2C_E R_E}$, the current through R_E becomes negligible [4]. Under this condition, C_S and C_E can be considered effectively in series and approximated by a single equivalent capacitance.

From this point onward, the baseline (VOC-independent) of the equivalent capacitance is grouped with the parasitic capacitance C_P and denoted as C_i, representing the intrinsic capacitance of the pixel. The VOC-dependent component is referred to as the measurement capacitance C_m. The total capacitance C_{pixel} at the sensing node is then defined as the sum of these two contributions. This simplified representation, as illustrated in Figure 3.5, will be used in the subsequent analysis of the pixel's electrical behavior.

Although a sensor pixel model has been established, many elements of the surrounding circuitry remain unspecified. At first glance, this may appear to be a significant limitation. However, upon closer analysis, it becomes evident that much of this complexity can be abstracted away under some assumptions.

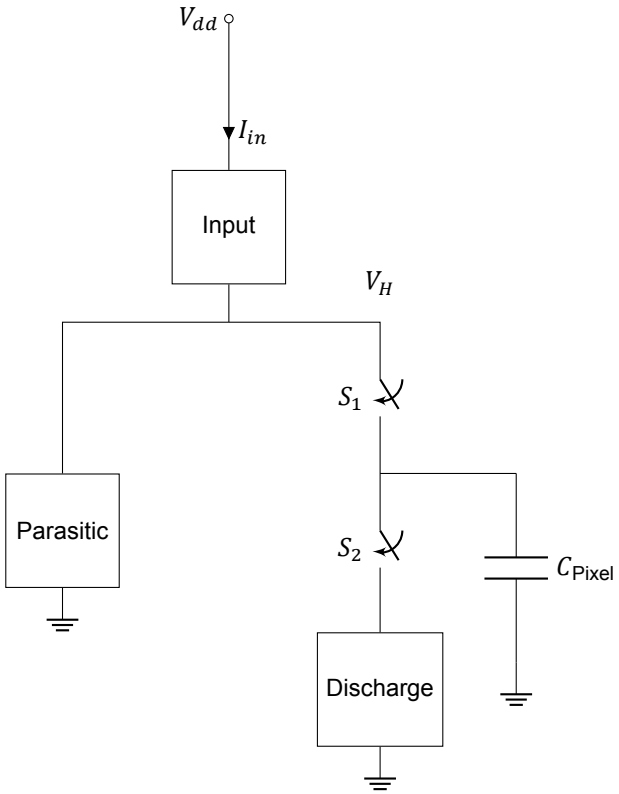


Figure 3.6: Capacitive sensor pixel with surrounding abstracted blocks for input, discharge, and parasitic network.

Assuming the pixel behaves purely as a capacitive load C_{Pixel}, and that the surrounding network can be abstracted by three simplified functional blocks: an input, a discharge, and a parasitic network, as illustrated in Figure 3.6. Despite these element blocks not being known at the circuit level, their influence on the behavior can be inferred by analyzing the charge balance of the system.

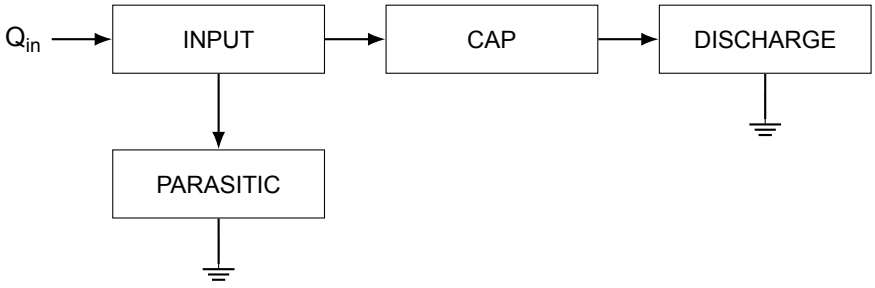


Figure 3.7: Charge flow representation .

From a charge flow perspective, the system can be represented as shown in Figure 3.7. All incoming charge must pass through the input network. Subsequently, part of this charge is dissipated through the parasitic path, while the remainder flows into the capacitor and discharge network.

Assuming that charge loss through the parasitic network is negligible, nearly all of the transferred charge is eventually accumulated in the capacitor C_{Pixel}. In this idealized case, the system behaves like a sequential pipeline, all charge stored in the capacitor must have passed through the input network and will subsequently pass through the discharge network. This unidirectional flow implies that analyzing any one stage provides insight into the charge behavior across the entire system within the same cycle.

If the capacitor is completely discharged during the discharge phase, then the total transferred charge is given by:

$$Q = C \cdot V_{\text{discharge}} \tag{3.1}$$

Where $V_{\text{discharge}}$ corresponds to the capacitor C_{Pixel} voltage V_S immediately before switch S_2 is toggled.

Since the charge flow of the capacitor is effectively in series with the rest of the functional blocks, this same amount of charge must pass through the preceding input network during that cycle. Resulting in that,under steady-state operation at a switching frequency f_s, the average input current can be expressed as:

$$I_{\text{avg}} = C_{\text{pixel}} \cdot V_{\text{discharge}} \cdot f_s \tag{3.2}$$

The input network includes an additional current mirror that amplifies this current, producing an output current with a gain factor $G_{\text{current mirror}}$. Therefore, for an enabled PCS array operating in steady state under a fixed differential clock, the average output current is assumed to be:

$$I_{\text{output}} = G_{\text{current mirror}} \cdot C_{\text{pixel}} \cdot V_{\text{discharge}} \cdot f_s \tag{3.3}$$

This relationship establishes the expected output characteristics of the pixilated capacitive sensor array and forms the basis for the design of the sensor readout circuitry.

For the PCS array used, the current mirror has a gain factor $G_{\text{current mirror}}$ of 100, the discharge voltage $V_{\text{discharge}}$ is approximately 0.9 V, and the intrinsic pixel capacitance is $C_i = 3.8$ fF [5]. The added measurement capacitance C_m varies in the range of 3.2 aF to 64 aF [5]. To ensure robustness in the readout design, a margin is applied, extending the effective upper bound of C_m to 75 aF.

Applying the derived equation 3.3 with these parameter values, the expected output current can be estimated for the intrinsic, minimal and maximum measurement current based on the frequency used. Table 3.1 summarizes the resulting output currents for the operating frequencies f_s: 40 MHz (matching the preceding board), 1 MHz, and 100 MHz.

Table 3.1: Estimated output current across frequency and capacitance ranges

Frequency (MHz)	Pixel capacitance	Output Current (A)
40	$C_i = 3.8$ fF	13.67×10^{-6}
40	$C_i + 3.2$ aF	13.69×10^{-6}
40	$C_i + 75$ aF	13.95×10^{-6}
1	C_i	3.42×10^{-7}
1	$C_i + 3.2$ aF	3.42288×10^{-7}
1	$C_i + 75$ aF	3.4875×10^{-7}
100	C_i	3.42×10^{-5}
100	$C_i + 3.2$ aF	3.42288×10^{-5}
100	$C_i + 75$ aF	3.4875×10^{-5}

3.3.2. Sensor readout considerations

Building on the expected sensor output previously defined, this section examines the design considerations for the readout circuitry. This involves proper signal conversion and amplification before the sampling stage.

A critical consideration is that the ADC selection range for voltage signals is significantly wider than for current, therefore it is advantageous to convert current into voltage prior to sampling. This conversion can be described using the transformation matrix T1 notation [6], with two practical implementations:

A Current Integrator:

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{s}{G_{\text{integrator}}} & 0 \end{bmatrix} \cdot \begin{bmatrix} V_o \\ I_o \end{bmatrix} \tag{3.4}$$

Configuration A corresponds to an integrator that accumulates input current over each sampling period and is then reset at the end of the cycle. The integration period is not limited to a clock cycle; it can span multiple clock cycles. This due to the fact that each pixel will be enabled for more than one clock cycle to reach a steady-state current [5]. Once the integrated charge is obtained, the microcontroller (MCU) can divide it by the integration period to determine the average current during that period.

B Transimpedance Amplifier:

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{1}{G_{\text{TIA}}} & 0 \end{bmatrix} \cdot \begin{bmatrix} V_o \\ I_o \end{bmatrix} \tag{3.5}$$

While the integrator facilitates the measurement of total accumulated charge, configuration B - based on a standard transimpedance amplifier (TIA) , may be sufficient when the input current remains relatively constant during the sampling interval. Furthermore, implementing an integrator presents certain practical challenges. Specifically, below its cutoff frequency, the integrator begins to behave as a high-gain TIA due to the large value of the feedback resistor. As a result, for low-frequency input signals, the integrator output will quickly clip.

It is observed that the output signal operates closer to a near-DC signal [5], which makes Configuration B, the simple transimpedance amplifier, the more suitable choice. The transimpedance gain G_{TIA} is selected to convert the expected input current range into a voltage that maximally utilizes the allowable output swing of the readout circuit, thereby maximizing the usable input range for the ADC.

Since the array sequentially switches between pixels during readout, each pixel remains active for a fixed duration before advancing to the next one. During this interval, the signal output is effectively constant, producing a piecewise-constant waveform that exhibits jumps at fixed time intervals. Although each segment exhibits near-DC behavior while a pixel is active, the transitions between pixels introduce higher-frequency components into the overall waveform.

To preserve the integrity of each pixel's response, the transimpedance amplifier (TIA) must have sufficient bandwidth to accurately reproduce this stepwise behavior. Specifically, the TIA bandwidth is chosen to be:

$$f_{\text{BW}} = \frac{N}{T_{\text{pixel}}} \tag{3.6}$$

Where T_{pixel} is the duration each pixel is active, and N is the number of harmonics to retain. In this case $N = 5$, which is sufficient to preserve the first 3 harmonics of the signal, assuming a square wave. This choice strikes a balance between capturing sharp transitions and limiting noise amplification.

The pixel activation duration $T_{\text{pixel}} = 150\,\mu\text{s}$ is inherited from the preceding board design and is assumed fixed throughout the analysis. Based on this timing and the harmonic requirement, the corresponding minimum bandwidth requirement for the TIA is determined. Table 3.2 summarizes these design considerations, which form the basis for the specification of the read out circuit.

Table 3.2: Readout Circuit considerations

	Description	
Readout Circuit	Final readout architecture selected based on signal behavior	TIA
T_{pixel}	Pixel activation duration (sampling period)	$150\ \mu$s
N	Number of harmonics retained	5
f_{BW}	Minimum required bandwidth for TIA	33.33 kHz

3.3.3. Quantization and noise budget

While it may initially appear premature to address quantization before completing the sensor readout circuitry, this section focuses on defining the quantization specifications. These specifications will also establish the corresponding noise budget, which will subsequently be back-propagated to inform the design of the readout circuit.

Quantization

To define the ADC requirements for the system, two measurement strategies are evaluated: one that considers the full pixel capacitance, and another that isolates the dynamic component. These approaches determine both the minimum number of bits required for quantization and the associated noise constraints imposed on the sensor readout circuit.

The two strategies are defined as follows:

- **Full-range measurement**: accounts for the total capacitance observed at the pixel, comprising the intrinsic pixel capacitance C_i and the variable measurement capacitance C_m.
- **Differential measurement**: isolates only the variable component C_m, assuming the intrinsic part C_i can be suppressed through techniques such as biasing or subtraction. Signal amplification may be applied afterward to restore usable dynamic range.

What makes the differential approach particularly compelling in this context is that the intrinsic capacitance causes a current three orders of magnitude larger than that caused by the measurement variation. As a result, when measuring the full range, a significant portion of the ADC resolution is consumed in representing a known quantity, effectively reducing the sensitivity to changes in C_m. For both strategies the target resolution is set to 1 aF, corresponding to the change in C_i being in the aF range.

To determine the number of ADC bits required to achieve this resolution, the same methodological procedure is applied to both measurement strategies. The voltage range of the ADC is translated into an equivalent measurable capacitance range, from which the bit depth needed to meet the resolution criterion can be calculated.

The measurable voltage range is first derived from the available ADC input range. Both the readout circuit and the ADC are supplied by a 3.3 V source. However, due to practical limitations, the output of the readout circuit and the ADC input range is limited by the supply voltage. In particular, the readout output voltage is expected to clip below the ADC's maximum input, resulting in a region of unused ADC range.

This unexploited headroom is expressed as:

$$V_{\text{unused}} = V_{\text{ADC,max}} - V_{\text{readout,max}} \tag{3.7}$$

This unused margin reduces the effective signal swing at the ADC input. To express this in terms of measurable capacitance, an equivalent capacitance C_{headroom} is computed based on the inverse of the expected output current of the PCS array 3.3 and the overall gain of the TIA:

$$C_{\text{headroom}} = \frac{V_{\text{unused}}}{G_{\text{TIA}} \cdot G_{\text{mirror}} \cdot V_{\text{discharge}} \cdot f_s} \tag{3.8}$$

Accordingly, the measurable capacitance range for each strategy is defined as:

$$C_{\text{full}} = C_i + C_{m,\text{max}} + C_{\text{headroom}}$$
$$C_{\text{diff}} = C_{m,\text{max}} + C_{\text{headroom}}$$

The number of ADC bits required to meet the resolution target of 1 aF is then calculated as:

$$\text{Bits}_{\text{ADC}} = \left\lceil \log_2 \left(\frac{C_{\text{range}}}{1\ \text{aF}} \right) \right\rceil \tag{3.9}$$

Noise budget

Once the quantization resolution has been determined, it indirectly translates this into a noise budget for the sensor readout circuit. Additional noise introduced by the ADC itself is not included but would further tighten the noise budget in a practical implementation. The guiding principle for defining the noise budget is that the signal-to-noise ratio (SNR) must exceed the quantization noise floor; otherwise, the additional resolution provided by the ADC is effectively lost. Consequently, a minimum SNR must be maintained at the output of the readout circuit that exceeds the SNR caused by quantization.

The corresponding signal-to-noise ratio (SNR) resulting from quantization is then determined by:

$$\mathrm{SNR}_{\mathrm{quant}} = 6.02 \cdot \mathrm{Bits}_{\mathrm{ADC}} \tag{3.10}$$

To ensure a sufficient noise margin, an additional 3 dB is added:

$$\mathrm{SNR}_{\mathrm{in}} = \mathrm{SNR}_{\mathrm{quant}} + 3\ \mathrm{dB} \tag{3.11}$$

Since SNR is a dimensionless ratio, it must be expressed as a physical RMS voltage in order to define a more concrete noise constraints for the readout circuit. This requires establishing the expected signal power at the output. As the output signal is originally defined as a DC current, it is converted to a voltage through a transimpedance gain G_{TIA}. Based on the signal voltage and the required input SNR, the corresponding maximum permissible RMS noise voltage at the readout output is:

$$V_{\mathrm{noise,rms}} = \frac{G_{\mathrm{TIA}} \cdot I_{\mathrm{signal}}}{10^{\mathrm{SNR_{in}}/20}} \tag{3.12}$$

Assuming that the ADC input range extends close to its supply voltage of 3.3 V, and that the sensor readout circuit clips approximately 0.3 V below this limit, and the resulting headroom. Using the previously established current level at 40 MHz, the corresponding noise budget results are calculated and summarized in table 3.3 .

Table 3.3: ADC noise and resolution specifications

	Description	**Value**
$Resolution_C$	Desired resolution	1 aF
$Bits_{diff\_C}$	Required ADC resolution if only the differential C is measured	9 bits
$Bits_{full\_C}$	Required ADC resolution if full range of C is measured	13 bits
SNR_{Quant_diff}	Quantization SNR for differential C	54.18 dB
SNR_{Quant_full}	Quantization SNR for full C	78.25 dB
SNR_{In_diff}	Required input SNR for differential C	57.18 dB
SNR_{In_full}	Required input SNR for full C	81.25 dB
V_{rms_diff}	Max RMS noise voltage at output for differential C	$1 \cdot 10^{-2}$ V
V_{rms_full}	Max RMS noise voltage at output for full C	$630.5 \cdot 10^{-6}$ V

Having defined the current ranges, bandwidth requirements and established noise constraints, the design of the transimpedance amplifier can now proceed based on these specifications and design budgets. To ensure that the resulting design meets all performance targets, validation will be performed primarily using SLiCAP [2].

3.3.4. Basic Tia

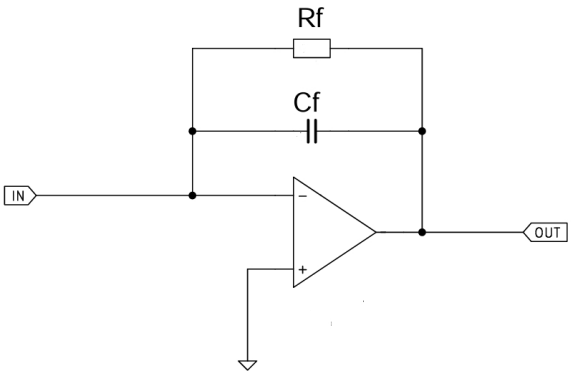


Figure 3.8: Basic Tia schematic

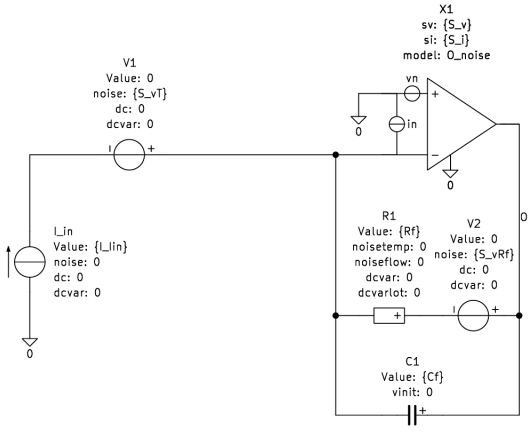


Figure 3.9: Basic Tia noise model

When implementing a basic transimpedance amplifier (TIA), as illustrated in Figure 3.8, the feedback network consists of a resistor R_f in parallel with a capacitor C_f. The transfer function describing the conversion from input current to output voltage is given by:

$$H(f) = \frac{-R_f}{1 + j\omega R_f C_f} \tag{3.13}$$

Given the target transimpedance gain G_{TIA}, the feedback resistor R_f is selected to match this gain. The feedback capacitor C_f is then chosen such that the -3 dB point of the transfer function aligns with the defined bandwidth :

$$C_f = \frac{1}{2\pi R_f f_{\text{bw}}} \tag{3.14}$$

Since the TIA provides a negative gain and the readout circuit operates from a single 3.3 V supply without a negative rail, the operational amplifier must be properly biased. Given that only positive input currents are expected and full-range utilization is desired, the amplifier is biased near the upper rail. Letting V_{bias} denote the non-inverting input bias voltage, chosen with sufficient headroom below the supply voltage to prevent clipping, the amplifier is biased accordingly. For input currents within the bandwidth of the TIA, the corresponding output voltage is given by:

$$V_{\text{out}} = V_{\text{bias}} - R_f \cdot I_{\text{in}} \tag{3.15}$$

To evaluate the noise performance of this configuration, a symbolic noise model as shown in Figure 3.9 is constructed and analyzed. The model captures the individual contributions of each circuit component to the total output noise voltage. Using the calculated values for R_f and C_f, the total output-referred noise is expressed as:

$$V_{\text{oNoise}} = 3.132 \cdot 10^{7} \left(S_i + 3.399 \cdot 10^{-11} S_v + 2.669 \cdot 10^{-11} S_{vR_f} + S_{vT} \right)^{0.5} \tag{3.16}$$

By selectively enabling individual noise sources within the model, their isolated contributions to the total output noise can be independently evaluated. Comparing each of these with the specified noise constraint $V_{\text{rms\_full}}$ allows the determination of upper limits for each source. The bounds represent the threshold at which a single noise contributor alone would cause the output noise to exceed the permissible limit.

For the input-referred noise at the output, the equivalent noise bandwidth B_{eq} of the TIA is computed:

$$B_{\text{eq}} = \frac{\int_0^\infty |H(f)|^2 \, df}{|H(0)|^2} \tag{3.17}$$

Based on the voltage noise constraint $V_{\text{rms\_full}}$, the input noise limit is calculated as:

$$S_{i,\text{max}} = \frac{V_{\text{rms\_full}^2}}{B_{\text{eq}}} \tag{3.18}$$

To select a suitable operational amplifier, noise specifications alone are insufficient, specifications such as the minimum slew rate and gain-bandwidth product (GBW) are considered. For the slew rate, the maximum expected voltage change at the TIA output corresponds to the difference between the peak input current and the intrinsic baseline current, scaled by the transimpedance gain.

The voltage transition resulting from a measurement must settle quickly enough to ensure accurate readout. However, since the TIA acts as a low-pass filter, its response is inherently delayed. It is therefore not meaningful to require a transition faster than the circuit's natural response. A practical settling time is approximated as 5τ, where $\tau = R_f \cdot C_f$. Within this time frame, the output should transition from maximum to minimum voltage. Accordingly, the minimum required slew rate SR_{min} is defined as:

$$\text{SR}_{\text{min}} > \frac{G_{\text{TIA}} \cdot (I_{\text{max}} - I_{\text{intrinsic}})}{5 \cdot R_f \cdot C_f} \tag{3.19}$$

To estimate the minimum required gain-bandwidth product (GBW) for the transimpedance amplifier, the following expression is used [7]:

$$\text{GBW} > \frac{C_i + C_f}{2\pi \cdot R_1 \cdot C_f^2} \tag{3.20}$$

where $C_i = C_S + C_d + C_{cm}$, with:

- C_S: Input source capacitance
- C_d: Differential input capacitance of the op-amp
- C_{cm}: Common-mode input capacitance of the inverting input

Since the op-amp has not yet been selected, and the input source capacitance is unspecified, the exact value of C_i cannot be determined at this stage. To ensure sufficient design margin, a **conservative** estimate of $C_i = 100\,\text{pF}$ is assumed.

Given that the measurement currents in the TIA are in the microampere range, the input bias current of the operational amplifier is a critical design consideration. Excessive bias current can significantly distort the measured signal, making accurate readout infeasible. To ensure measurement accuracy, the input bias current is chosen to be at least three orders of magnitude smaller than the input current, i.e., less than $10^{-3} \cdot I_{\text{in}}$.

Using the previously defined specifications, the necessary component values and corresponding noise limits have been derived. These results provide a basis for further implementation and validation. A summary of the selected parameters and their permissible noise contributions for $fs = 40Mhz$ is presented in Table 3.4

Table 3.4: Final TIA Design Specifications

Symbol	Description	Value	Units
C_f	Feedback capacitor	$24.66 \cdot 10^{-12}$	F
R_f	Feedback resistor	$193.5 \cdot 10^{3}$	Ω
$f_{-3\text{dB}}$	TIA bandwidth (-3 dB point)	$33.33 \cdot 10^{3}$	Hz
SR_{min}	Minimal slew rate of the op-amp	$2.253 \cdot 10^{-3}$	$V/\mu s$
GBW	Minimal GBW rate of the op-amp	168.6	kHz
I_{Bias}	Minimal bias current of the op-amp	13.67×10^{-9}	A
$S_{i\text{max}}$	Maximum current noise opamp input	$7.593 \cdot 10^{-12}$	A^2/Hz
$S_{vT\text{max}}$	Maximum voltage noise opamp input	$18.91 \cdot 10^{-9}$	V^2/Hz
$S_{iT\text{max}}$	Maximum input current noise	$12.04 \cdot 10^{-9}$	A^2/Hz
$S_{vR_f\text{max}}$	Maximum feedback resistor voltage noise	$24.08 \cdot 10^{-9}$	V^2/Hz
$S_{v\text{max}}$	Maximum input voltage noise	$642.9 \cdot 10^{-21}$	V^2/Hz

3.3.5. T-network

The feedback network of a transimpedance amplifier is not limited to the conventional parallel resistor-capacitor configuration discussed previously in section 3.3.4. An alternative implementation, based on a T-network topology, has been extensively considered and is recommended in application literature by Texas Instruments [8]. This topology is suggested to offer improved noise performance. Given that noise minimization is a critical design criterion for the TIA, the potential benefits of the T-network approach merit detailed consideration.

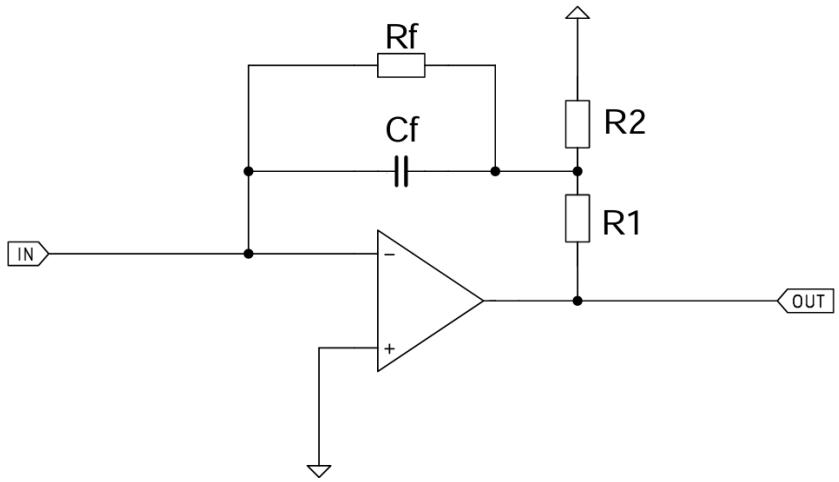


Figure 3.10: Tia implemented with a T-network circuit schematic

The premise of the T-network is that the amplifier's output is attenuated through a voltage divider before being applied to the original feedback path of a basic TIA, as can be seen in Figure 3.10. This configuration is intended to achieve the same gain using smaller resistors values, thereby reducing thermal noise. However, during evaluation, this premise didn't hold in practice. As a result, the T-network configuration was not selected for the final design. Thus only a brief overview is presented here, while a more detailed analysis, including a possible reason for this lack of improvement is provided in Appendix B.

3.3.6. Differential

Focusing exclusively on measuring the change in capacitance induced by the presence of VOCs, presents multiple advantages for PCS array readout, which are discussed in detail in Section 3.3.3. Most notably, it eliminates the need to digitize the intrinsic, known baseline capacitance, thereby reducing the required resolution of the output ADC and increasing the permissible noise margin at its input. To realize this measurement approach, a differential stage is required, as illustrated in Figure 3.11.

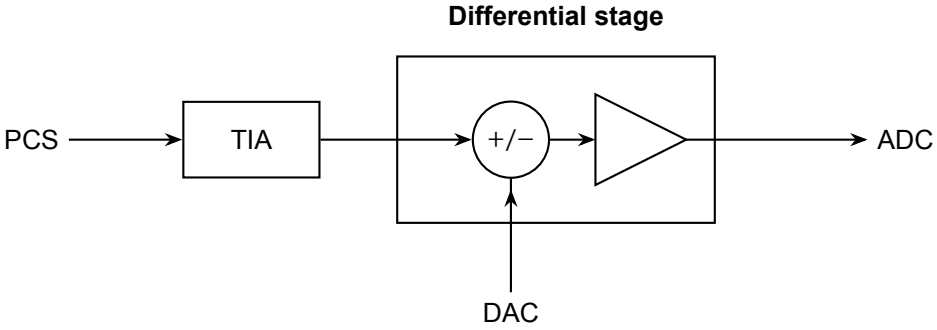


Figure 3.11: Block diagram of differential stage implementation

The TIA stage remains unchanged; however, it's important to recall that it has a negative gain and is positively biased. As a result, the output voltage corresponding to the intrinsic current is higher than the voltage produced by a VOC-induced change. To isolate only the variation caused by VOCs, the TIA output is **subtracted** from a baseline voltage. This baseline is simply the output voltage of the TIA at intrinsic current conditions and is generated by a DAC to allow for fine-tuning. Approximately, the baseline voltage should be equal to:

$$V_{\text{DAC}} = -G_{\text{TIA}} \cdot (I_{\text{intrinsic}} - I_{\text{max}}) \tag{3.21}$$

However, this subtraction step alone does not improve the signal resolution. It merely inverts the signal around the baseline, without expanding the voltage range. Since the differential stage operates on a single supply, it cannot represent negative values. Current inputs below the intrinsic level create a TIA output voltage that is higher than the baseline voltage, therefore the differential output is clipped to zero. Conversely, when the current rises above the intrinsic level, the differential output increases, but will not exceed the original baseline voltage of the TIA. As a result, the measurable current variation remains constrained to the same limited portion of the ADC's range. Therefore, to enhance resolution, the output of the differential stage must be amplified so that the VOC-induced current variation spans a broader portion of the ADC's input range.

To implement the differential stage, a simple differential amplifier is added at the output of the TIA, as shown in Figure 3.12.

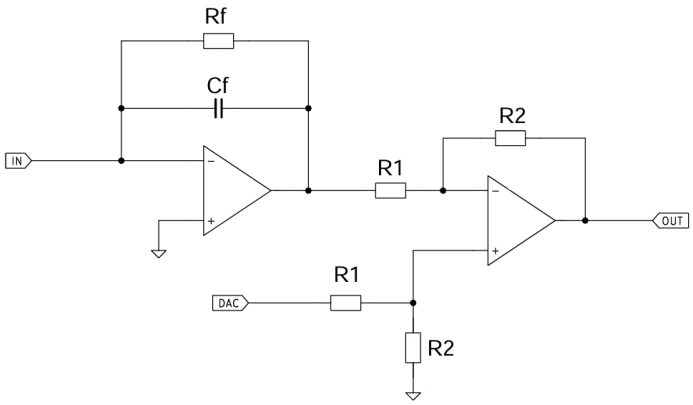


Figure 3.12: Basic TIA with differential stage schematic

With the inclusion of the differential stage, the output voltage is expressed as:

$$V_{\text{out}} = \frac{R_2}{R_1}\left(V_{\text{DAC}} - V_{\text{TIA}}\right) \tag{3.22}$$

Here, the ratio $\frac{R_2}{R_1}$ defines the gain of the differential amplifier. To ensure that the full range of VOC-induced current variation is observed at the ADC, the differential stage required gain, g_{diff}, is determined as the ratio of the unused voltage range to the baseline voltage. This is expressed as

$$g_{\text{diff}} = \frac{V_{\text{readout,max}} - V_{\text{DAC}}}{V_{\text{DAC}}} \tag{3.23}$$

The selection of resistor values R_1 and R_2 requires careful consideration to balance loading effects and noise performance. If the resistance is too low, it may excessively load the amplifiers and the DAC. Conversely, excessively high resistance increases thermal noise .

The current drawn from the DAC can be approximated as $I_{\text{DAC}} = V_{\text{DAC}}/(R_1 + R_2)$. For the amplifiers, the worst-case loading scenario occurs when the TIA output is near 0 V. In this condition, the differential amplifier must source at least :

$$I_{\text{differential}} = \frac{V_{\text{DAC}} \cdot R2}{(R1 + R2)} \cdot \frac{1}{R1} \tag{3.24}$$

This arises because R_1 and R_2 form a voltage divider with V_{DAC} applied to the non-inverting terminal of the amplifier. Since the op-amp maintains equal voltages at both terminals, its similar at the inverting terminal, which is connected to the near 0 V output of the TIA through R_1. For the op-amp in the TIA, it must sink this current in addition to the measurement current.

To minimize loading and limit thermal noise contributions, resistor values in the kilo-ohm range were selected. These values reflect practical trade-offs rather than detailed optimization. Specifically, R_1 was chosen to be $5\ \text{k}\Omega$, and R_2 was set to $250\ \text{k}\Omega$, which achieves the required gain for the differential stage.

The op-amp specifications for the TIA stage remain unchanged in this context. However, for the differential amplifier stage, the op-amp must be reconsidered. Since the voltage difference will now span the full output range, the minimum required slew rate is given by:

$$\text{SR}_{\text{min}} > \frac{V_{\text{readout,max}}}{5 \cdot R_f \cdot C_f} \tag{3.25}$$

To ensure stable operation across the intended bandwidth, the minimum required GBW of the op-amp in the differential stage is estimated by using the desired gain g_{diff} and the bandwidth f_{BW}:

$$\text{GBW} > g_{\text{diff}} \cdot f_{\text{BW}} \tag{3.26}$$

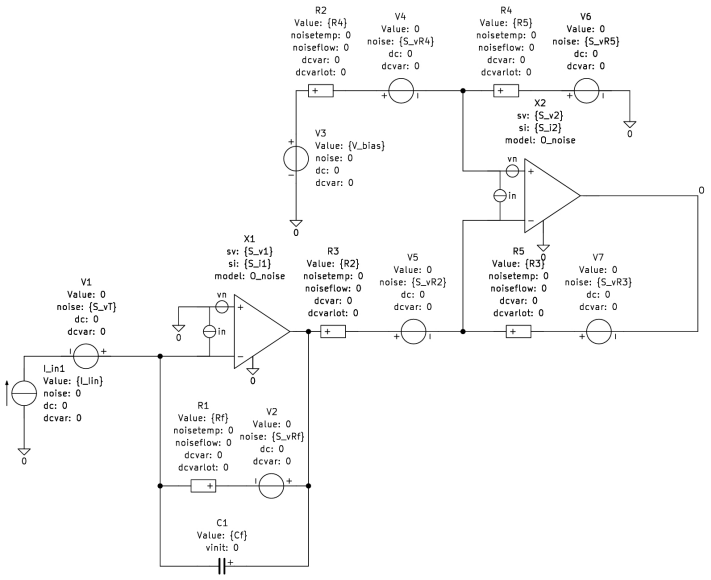


Figure 3.13: Basic TIA with differential stage schematic noise model

Following the same methodology outlined in Subsection 3.3.4, a corresponding noise model is made, as shown in Figure 3.13. In this case, the noise constraint is based on $V_{\text{rms\_diff}}$ rather than $V_{\text{rms\_full}}$ The resulting noise limits for each contributing source and parameters are summarized in table 3.5.

Table 3.5: TIA with differential stages specifications

Symbol	Description	Value	Units
C_f	Feedback capacitor	$24.66 \cdot 10^{-12}$	F
R_f	Feedback resistor	$193.5 \cdot 10^{3}$	Ω
R_1	R1	$5 \cdot 10^{3}$	Ω
R_2	R2	$258.3 \cdot 10^{3}$	Ω
R_3	R3	$5 \cdot 10^{3}$	Ω
R_4	R4	$258.3 \cdot 10^{3}$	Ω
SR_{diff}	Minimal slew rate of the op-amp (differential)	0.12	$\text{V}/\mu\text{s}$
GBW_{diff}	Minimal GBW rate of the op-amp (differential)	1.70	MHz
SR_{TIA}	Minimal slew rate of the op-amp (TIA)	$2.253 \cdot 10^{-3}$	$\text{V}/\mu\text{s}$
GBW_{TIA}	Minimal GBW rate of the op-amp (TIA)	168.6	kHz
I_{Bias}	Minimal bias current of the op-amp (TIA)	13.67×10^{-9}	A
$S_{i1\text{max}}$	Maximum current noise opamp 1	$107.7 \cdot 10^{-21}$	A^2/Hz
$S_{i2\text{max}}$	Maximum current noise opamp 2	$44.04 \cdot 10^{-21}$	A^2/Hz
$S_{v1\text{max}}$	Maximum voltage noise opamp 1	$3.171 \cdot 10^{-9}$	V^2/Hz
$S_{v2\text{max}}$	Maximum voltage noise opamp 2	$1.100 \cdot 10^{-12}$	V^2/Hz
$S_{vR2\text{max}}$	Maximum noise of R2	$3.171 \cdot 10^{-9}$	V^2/Hz
$S_{vR3\text{max}}$	Maximum noise of R3	$8.465 \cdot 10^{-6}$	V^2/Hz
$S_{vR4\text{max}}$	Maximum noise of R4	$1.143 \cdot 10^{-12}$	V^2/Hz
$S_{vR5\text{max}}$	Maximum noise of R5	$3.051 \cdot 10^{-9}$	V^2/Hz
$S_{vR_f\text{max}}$	Maximum feedback resistor noise	$4.037 \cdot 10^{-9}$	V^2/Hz

3.3.7. Variable gain

As outlined in requirement **[ToR.1.1]**, it is desirable to develop a readout circuit capable of operating across a range of clock frequencies, specifically from 1 MHz to 100 MHz, rather than being limited to a fixed frequency. To accommodate this variability, a configurable gain is required. As shown in section 3.3, the average output current is linearly dependent on the clock frequency. Consequently, operating across this frequency span implies a change in output current by a factor of up to 100.

To address this, the proposed architecture consists of a TIA followed by a variable-gain amplification stage which is controlled by the MCU, as illustrated in Figure 3.14.

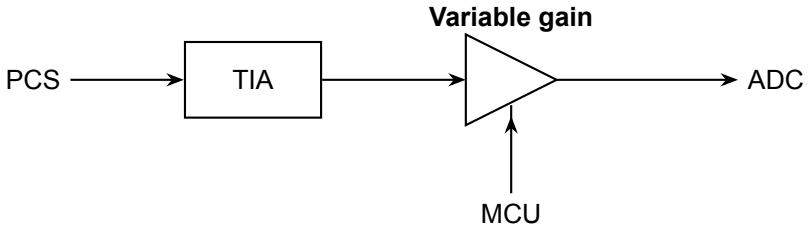


Figure 3.14: Block diagram of variable gain implementation

The implemented circuit consists of a TIA , with R_f and C_f selected to an input current corresponding to a f_s of 100 MHz, following the same design methodology outlined in Section 3.3.4. The output of the TIA is connected to a non-inverting amplifier stage, where the gain is set by a feedback network incorporating a potentiometer, as shown in Figure 3.15. To enable gain control by the MCU, a digital potentiometer is employed instead of a conventional one.

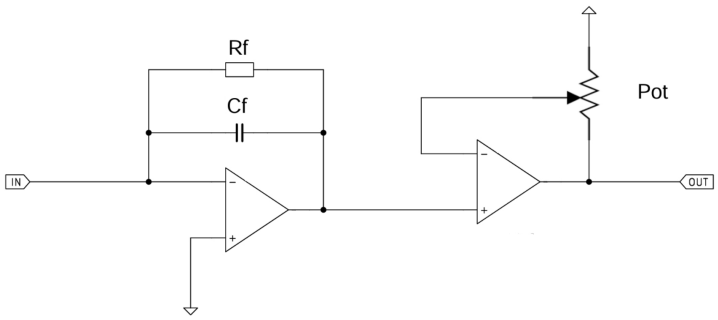


Figure 3.15: Basic TIA with variable stage schematic

Because a digital potentiometer is more complex than a simple resistor pair with a center tap, modeling it in this way would be an oversimplification. As a result, simulation was deemed impractical, and the selection focused instead on digital pots whose datasheet specifies low output noise voltage and adequate bandwidth.

3.4. Power

To enable full-system functionality, a consistent power distribution approach was implemented for the Main PCB. Unlike the previous revision, which employed multiple supply rails, this design uses a single voltage level of $3.3\,\mathrm{V}$ across the entire board. This decision was made to simplify the design and layout, and because the MCXN947 microcontroller **[MR.2.4]** operates natively at $3.3\,\mathrm{V}$. Consequently, all other components were selected to be compatible with this voltage.

The following subsections detail the power requirements for each major circuit block, beginning with the MCU, and followed by the PCS chip and the readout circuit. The user interface (UI) components are excluded from this discussion, as they operate directly from the $3.3\,\mathrm{V}$ rail without any special requirements.

To ensure stable and noise-free power delivery, each component is equipped with dedicated decoupling capacitors. These capacitors serve to suppress electromagnetic interference (EMI) from the surrounding environment and to buffer against transient voltage drops caused by dynamic load changes. For the components discussed in the sections below, the specific values and placement strategies of their associated decoupling capacitors will also be addressed. In addition to the use of decoupling capacitors, ferrite beads were employed to suppress high-frequency noise above $25\,\mathrm{kHz}$. Without such filtering, this noise could propagate through the power distribution network and potentially interfere with sensitive components, such as the reference sources of ADCs, thereby degrading their performance [9].

The value of decoupling capacitors was, where feasible, estimated using the guideline provided in [10, Ch. 6.1, p. 244]:

$$C = I_{\text{peak}} \cdot \frac{t}{V_{\text{droop\_max}}} \tag{3.27}$$

where I_{peak} is the estimated peak current, t is the duration of the transient, and $V_{\text{droop\_max}}$ is the maximum allowable voltage droop. However, as noted in [10, Ch. 6.1], this formula serves only as a rough approximation, since the involved parameters are often imprecisely known and rather vague the capacitor value is therefore not highly critical.

3.4.1. MCU PWR

The microcontroller unit (MCU) is a digitally intensive component that features multiple independent voltage domains, including a system domain (V_{dd_SYS}), a core domain (V_{dd_CORE}), and per-port I/O domains ($V_{dd}, V_{dd\_P2} - V_{dd\_P4}$, corresponding to Port 1, Port 2 - Port 4). To simplify the power distribution the the port domains while maintaining flexibility, the design uses a single regulated $3.3\,\mathrm{V}$ rail that is split into the required voltage domains through removable $0\,\Omega$ resistors as can be seen in Fig.3.16. This approach allows for easy rerouting or isolation of power domains during testing or debugging. On the current version of the PCB, most GPIO pins have been routed to the Port 3 domain. Therefore (this will be discussed later in 3.7), V_{dd_P3} must be powered.

Per the datasheet [11], the V_{dd_SYS} domain must always be supplied as it powers essential subsystems such as internal regulators and the power-on-reset circuitry. V_{dd_CORE} is typically powered via an on-chip LDO or DCDC converter derived from V_{dd_SYS}. Additionally, there are V_{bat} and V_{dd_ANA} pins, which have been connected to the power rail according to the datasheet [11].

To ensure signal integrity and suppress transient noise on the digital power domains, each supply pin is locally decoupled with ceramic capacitors. Proper placement of these decoupling capacitors is critical to minimize power distribution network (PDN). As discussed in [12], the effectiveness of decoupling relies not only on the capacitor value but also on the via placement and the return current path in multilayer PCBs. The implemented layout adheres to these guidelines by placing capacitors as close as possible to the supply pins and using short traces to ground. The decoupling capacitor are also added to the Power distribution network of the MCU in Fig.3.16. Please note that C_{eq} represents multiple capacitors. In the final design, three $0.1\,\mu\mathrm{F}$ and a single $1\,\mu\mathrm{F}$ caps were used as per the schematic of the FRDM-MCXN947 development board [13].

3.4.2. PCS chip PWR

The PCS chip features three distinct power supply inputs: `VDDE`, `VDDD`, and `VDDA`. The analog domains `VDDD` and `VDDA` operate nominally at $1.1\,\mathrm{V}$. To enable crosstalk characterization, `VDDA` and `VDDD` are

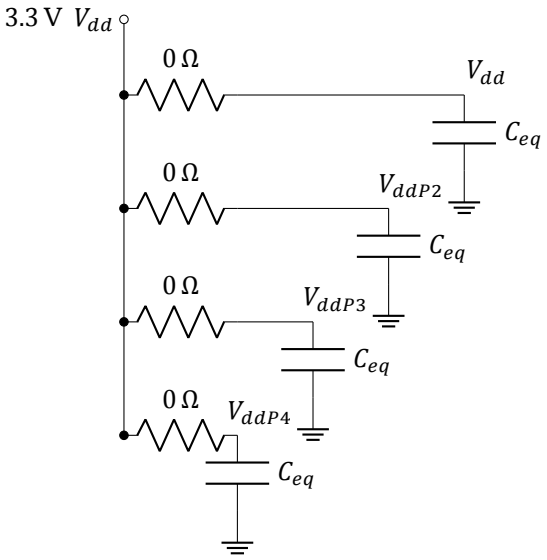


Figure 3.16: Power distribution MCU

supplied by adjustable power sources, permitting fine voltage adjustments (e.g., $\pm 25\,\mathrm{mV}$) around the nominal $1.1\,\mathrm{V}$ level. This allows for the evaluation of crosstalk effects from `VDDA` to the output current, as well as for tuning `VDDD` to mitigate timing issues, albeit at the expense of accelerated degradation. In contrast, `VDDE` operates at a nominal voltage of $3.3\,\mathrm{V}$ and is directly powered by a low-noise Linear Dropout Regulator (LDO) with additional decoupling capacitors.

As previously discussed, the PCS chip is a highly sensitive analog component and particularly susceptible to power supply noise. As noted by F. Widdershoven, "variations on VDDA are expected to transfer almost 1:1 to the sensor's cell voltage and, therefore, to the sense current" (F. Widdershoven, personal communication, June 3, 2025). According to Requirement **[MR.2.11]**, the noise originating from the readout circuit must not exceed four quantization steps of the ADC. Since the noise is limited to 4 bits, dithering techniques can be applied to recover the signal.

Using Python in combination with SLICAP (Symbolic Linear Circuit Analysis Program), the noise corresponding to these four quantization steps was back-propagated to the output of the PCS chip. This analysis yielded a maximum total noise power spectral density of $7.104 \times 10^{-19}\ \mathrm{V^2\,Hz^{-1}}$ at the output of the current mirror. Taking the square root of this value results in a noise voltage spectral density of $0.843\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. Since the intrinsic noise contribution of the chip itself is unknown, the voltage variations at the input should remain well below this threshold. It should be noted, however, that this analysis does not include possible `1/f` noise contributions of the PCS chip or surrounding circuitry. Given the potentially significant impact of low-frequency noise on high-resolution measurements, incorporating 1/f noise into the noise budget analysis would be a valuable extension for future work.

To support software-controlled regulation of the `VDDA` and `VDDD` supplies, Digital-to-Analog Converters (DACs) are employed. However, identifying DACs with sufficiently low noise proved challenging. In scenarios where cost and board area are less restrictive, the AD5791, a 20-bit DAC, offers a promising (but not complete) solution, with a noise spectral density of $7.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ [14]. However, given that this project serves as a prototyping platform for academic research and must remain low-cost to allow for free distribution to external collaborators, the use of such a high-end DAC is not feasible.

More affordable DACs typically exhibit noise spectral densities in the range of 100–$200\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. To minimize design risk and ensure consistency, the DAC previously used in the board designed by T. Shen was reused. This DAC has a typical noise spectral density of approximately $120\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ [15], exceeding the calculated noise budget by a factor of roughly 150.

To mitigate this, several noise-reduction techniques can be applied:

- **Low-frequency and 1/f noise:** On the software side, correlated double sampling can be used.

This technique leverages the slowly varying nature of low-frequency noise. By acquiring two measurements, one from the target pixel and one from a reference pixel, and subtracting them in post-processing, the common-mode noise component is effectively canceled, preserving only the differential signal.

- **High-frequency noise:** A dedicated RC low-pass filter is included in the final PCB design to suppress high-frequency noise components in hardware. The exact cutoff frequency of this filter is still to be determined but can be chosen relatively low, as crosstalk measurements between VDDA and the sense current will not be conducted at high frequencies.

For the VDDE supply, where little is known about the propagation of noise into the readout circuit, an LDO was selected as a precautionary measure. Although LDOs are generally less energy efficient than switching regulators, they offer superior noise performance [16].

For instance, while typical peak-to-peak noise levels for buck converters can reach $20\,\mathrm{mV}$ [17], the ADPL4050 LDO selected for the final PCB exhibits an output noise of only $20\,\mu\mathrm{V_{rms}}$. This corresponds to approximately $132\,\mu\mathrm{V}$ peak-to-peak at a 99.9% confidence level, based on the statistical scaling of Gaussian noise described in Chapter 7 of [18]. To further reduce noise, additional decoupling capacitors are included at the input of the PCS chip.

3.4.3. Readout circuit PWR

The readout circuit is designed such that the operational amplifiers operate at $3.3\,\mathrm{V}$ and do not require rail-to-rail voltage. This design choice significantly simplifies the power supply architecture. In addition to the amplifiers, the only other active components in the analog signal path are the three ADCs corresponding to the three sensor arrays.

Given that these components operate on sensitive analog signals, a clean and stable reference or supply voltage is critical. As noted in [19], ”any noise greater than 1/2 Least Significant Bit (LSB) in amplitude has some effect upon the converter noise performance. This effect is proportional to the input voltage level.” Since $1\,\mathrm{LSB} = 403\,\mu\mathrm{V}$, the maximum permissible RMS noise on the ADC power supply is $201.5\,\mu\mathrm{V}$.

Consequently, switch-mode power supplies are unsuitable due to their typically higher noise levels [16]. A low dropout regulator (LDO) is therefore required. The ADPL40502 was selected for this purpose, as it provides an RMS output noise of only $20\,\mu\mathrm{V}$ [20], well below the specified limit.

A separate DAC of the same type as that used for the PCS power rails is employed to generate the bias voltage for the operational amplifiers.

To further reduce potential interference between analog subsystems, the final design employs two separate LDOs: one dedicated to the ADCs and DACs, and another exclusively for the operational amplifiers.

3.4.4. Complete system

As specified in Requirement **[ToR.2.2]**, a second power input was added alongside a USB-C connector. The user can select the active $5\,\mathrm{V}$ power source by configuring a header jumper.

The secondary power connector is intended to be a commonly used type with a minimal footprint to conserve board space. Currently, a Keystone 476-2 connector has been selected. However, alternative connectors with smaller footprints are under consideration to further optimize the layout.

A complete overview of the power delivery system is provided in Fig. 3.17. It should be noted that the symbols C_{eq} represent the combined decoupling capacitor network at each supply node.

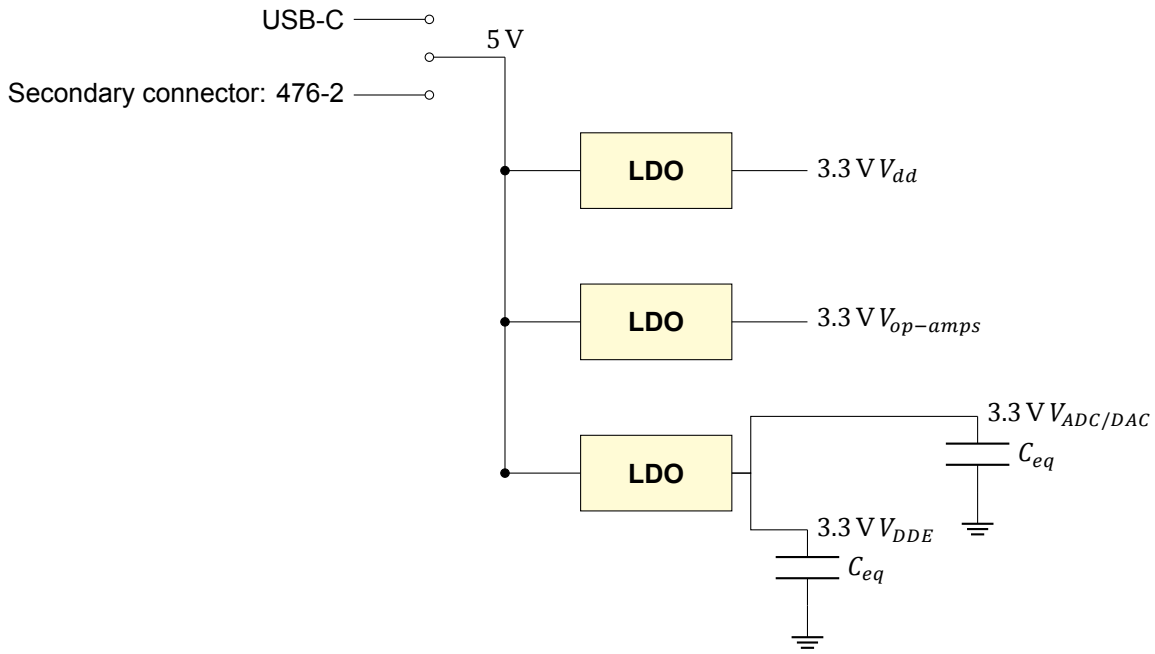


Figure 3.17: Power system overview

3.5. Grounding

With all components now powered, it is essential to establish well-defined return current paths. Following the recommendation by Park [21], the grounding system is divided into two distinct domains: Analog Ground (AGND) and Digital Ground (DGND). This separation helps to isolate digital switching noise from sensitive analog circuitry, thereby enhancing overall signal integrity. Components are assigned to one of the two domains based on guidance provided in their respective datasheets.

For components that feature both AGND and DGND pins (e.g., the PCS chip), Zumbahlen [18], in Chapter 12, recommends connecting these pins externally and routing both to the analog ground (AGND) plane. This approach minimizes the risk of ground loops and supports the maintenance of a low-noise environment.

The practical implementation of these ground planes is described in more detail in Subsection 4.1.1.

3.6. Connectors & UI

This section will focus on Mandatory Requirements **[MR.2.1]**, **[MR.2.2]** and **[MR.2.3]**. The section first covers the design choices for the connectors as well as a quick view on possible future improvements, lastly, it will cover the reset circuitry and status LED. All schematics can be found in more detail in appendix C.

3.6.1. SWD/JTAG

The SWD/JTAG port serves as an interface for programming and debugging microcontrollers. It connects directly to a PC or external debugger via dedicated cables. The pinout of the SWD/JTAG interface is as shown in Fig.3.18.

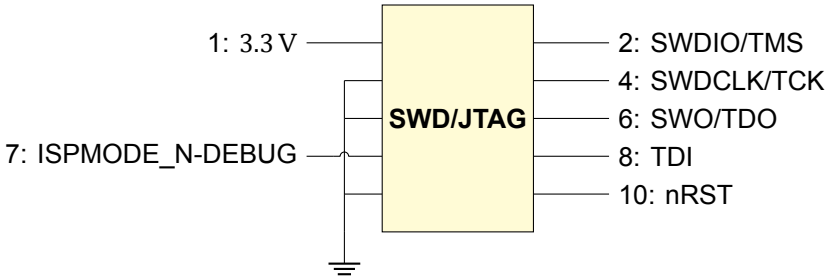


Figure 3.18: SWD/JTAG connector

The cables mentioned above are susceptible to Electrostatic Discharge (ESD) events during connection and disconnection of the debugger. These discharges can pose a risk to the MCU and other connected components. To mitigate this risk, the PESD3V3L5UY was added. This component is a five-channel Transient Voltage Suppression (TVS) diode array and is connected to pins 2, 4, 6, 8, and 10 of the connector. For pin 7, which is not covered by the array, a separate TVS diode (ESD5Z3.3T1G) was used.

3.6.2. UART

The UART port facilitates serial communication with the PC and utilizes a six-pin connector. In this design, only three of the pins are active: `TX`, `RX`, and `GND` as shown in Fig.3.19. The remaining pins are left unconnected.

Although the UART port is fully exposed making it theoretically susceptible to ESD events, dedicated TVS diodes were not included. Instead, according to the FRDM-MCXN947 schematic [13], two $330\,\Omega$ resistors are placed in series between the connector and the microcontroller on the `TX` and `RX` lines. These resistors serve to limit surge currents in the event of accidental misconnections and provide partial attenuation of ESD transients, while preserving signal integrity.

In contrast, the SWD/JTAG interface, which connects directly to critical debug circuitry within the MCU, employs dedicated TVS diodes to ensure robust ESD protection.

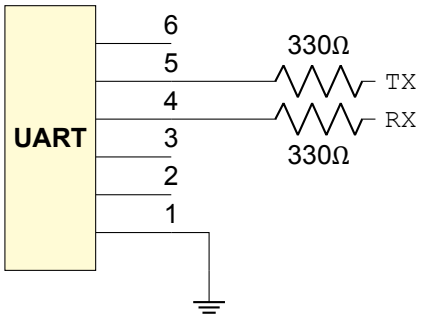


Figure 3.19: UART circuit

3.6.3. USB-C

To comply with modern interface standards, the Micro-USB connector used in the previous version of the board has been replaced by a more versatile USB Type-C port. This connector serves two primary functions: delivering power to the system and enabling data communication between the microcontroller and a host PC.

According to the USB Type-C specification [22], USB 2.0 devices are limited to a default current of $500\,\mathrm{mA}$, although additional circuitry can allow for negotiated currents up to $3\,\mathrm{A}$. In this design, such negotiation is unnecessary. As stated in requirement **[MR.2.7]**, the previous board consumed approximately $100\,\mathrm{mA}$. Given the removal of the power-intensive dual supply operational amplifiers in the new design, the total current draw is expected to remain at or below this value. Thus, the default USB 2.0 configuration provides sufficient power for the board.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND			VBUS	CC1	D+	D-	VBUS	SBU1			GND
GND			VBUS	SBU2	D-	D+	VBUS	CC2			GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 3.20: USB Type-C receptacle pinout.

Power is delivered through the multiple `VBUS` pins, which are duplicated in the connector to support cable reversibility, as shown in Fig. 3.20. These pins are shorted together on the PCB and filtered using a ferrite bead and decoupling capacitor to generate a stable $5\,\mathrm{V}$ supply for the Main PCB.

Similarly, data communication is handled through the `D+` and `D−` lines, which are also duplicated for orientation independence. These lines are shorted accordingly to form a single differential pair. To protect the data interface from ESD and transient events, the RCLAMP0854P-TCT TVS diode is employed. This component is specifically designed to safeguard high-speed differential data lines while maintaining signal integrity.

The `CC1` and `CC2` pins serve to indicate the orientation of the USB-C cable and to establish the role of the connected device. Three roles are defined by the USB-C specification: Upstream Facing Port (UFP), which corresponds to a peripheral or ”slave” device; Downstream Facing Port (DFP), which acts as a host or ”master” device; and Dual-Role Power (DRP), which can dynamically alternate between UFP and DFP functionalities. As specified in [22], for a UFP configuration, the `CC1` and `CC2` pins must be pulled down to ground through $5.1\,\mathrm{k\Omega}$ resistors.

The `SBU1` and `SBU2` pins are designated for low-speed signaling and alternate modes not inherent to the standard USB-C protocol. Since these functionalities are not relevant to the Main PCB, the SBU lines are left unconnected (floating).

3.6.4. UART and SWD/JTAG over USB-C

One of the advantages of USB-C is its support for a dedicated debug mode known as Debug Accessory Mode (DAM). Several developers, including J. Whittington [23], have demonstrated systems that utilize the USB-C DAM protocol to integrate SWD/JTAG and UART functionality into a single USB-C port, alongside the standard USB features. This approach has the potential to significantly reduce PCB footprint by eliminating the need for separate, bulky connectors for UART and SWD/JTAG. However, due to time constraints, the implementation of the additional circuitry required for DAM support could not be completed within the scope of this project.

3.6.5. Reset circuitry & Status LED

A simple reset button and status LED were added to the schematics. To address the issue of contact bounce in mechanical switches, a debounce circuit was implemented, as recommended in [24]. This circuit consists of a $0.1\,\mathrm{\mu F}$ capacitor in combination with a $100\,\mathrm{k\Omega}$ resistor, resulting in a time constant of $10\,\mathrm{ms}$. This duration is sufficient to filter out the $5\,\mathrm{ms}$ bounce time specified for the switch in [25], thereby preventing false triggers during operation.

Two LEDs were included in the design. One is directly connected between the 3.3 V power rail and ground, serving as a power indicator for correct board operation. The second is an RGB LED connected to the microcontroller, which can be configured for status indication or user-defined signaling.

3.6.6. External Clock ports

During the project, several issues and uncertainties arose on the software side related to generating a reliable differential clock. To mitigate the risk of failing to provide a clean clock signal to the PCS chip, two RF connectors were added to allow connection to an external high-quality clock generator. To maintain flexibility and enable testing of the MCU-generated clock, two jumper wires were included, allowing the user to switch between the internal and external clock sources.

3.7. MCU Integration

With all major subsystems defined in the preceding chapters, they must now be interconnected to form a coherent and functional system. This involves routing data lines from the debugger, USB-C interface, UART, and ADC outputs to their corresponding pins on the microcontroller (MCU). In addition, the ADCs, DACs, and the chip itself require dedicated control signals originating from the MCU.

Accordingly, the following subsections are organized into two categories: data lines and control signals.

3.7.1. Data Pins

This subsection addresses all signal lines responsible for transferring data to and from the MCU.

The MCU has designated pins for SWD/JTAG signals, UART `RX/TX`, and USB `D+` and `D-`, which have been connected in accordance with the manufacturer's datasheet.

As described in Subsection 3.4.1, the MCU's I/O structure is organized into four primary ports, each associated with a distinct GPIO speed class: Port 1 provides medium-speed GPIOs, Ports 2 and 3 support fast GPIOs, and Port 4 consists of slow GPIOs.

- **ADC outputs:** For the ADC output signals, signal integrity is of critical importance. To optimize performance, layout support was added for optional RC impedance matching circuits at each output. Although these components will not be populated by default, their corresponding pads have been included to allow for post-assembly modification if necessary.

  The ADC outputs from the readout circuit are not assigned to fixed microcontroller pins. Since a large number of Fast GPIO pins are available, the design aimed to route all ADC outputs to either Port 2 or 3 to ensure redundancy and enable robust signal acquisition. Consequently, the signals were mapped to Fast GPIO pins that provided the most efficient routing paths during the PCB layout phase.

- **Differential clock:** The differential clock for the PCS chip operates at high frequency and thus also requires Fast GPIO support. To accommodate this, two adjacent pins in either Port 2 or 3 were reserved for the `CLK+` and `CLK-` signals. This approach mirrors the rationale used for the ADC outputs, namely to mitigate risk and ensure timing-critical signals are handled appropriately.

- **RGB LED:** Due to the simplicity of the RGB LED, there were no specific requirements regarding port speed, nor was it necessary to assign it to a Fast GPIO. During the layout phase, the pins were selected based on routing convenience and ease of implementation.

3.7.2. Control Signals

This subsection addresses all control lines responsible for operating the ADCs, DACs, the sensor chip, and the MCU itself.

As with the SWD/JTAG signals, UART `RX/TX`, and USB `D+` and `D-`, the MCU datasheet [11] also specifies a dedicated pin for the external reset button.

- **ADCs:** Each ADC at the output of the readout circuit includes a `ADC_SCLK` and `ADC_CS` pin. To simplify the overall design, these signals were shared across all three ADCs by shorting the respective pins, resulting in a single global `ADC_SCLK` and `ADC_CS` line. The connection of these

shared signals to the MCU followed the same routing and port selection considerations as described for the differential clock and ADC output signals.

- **DACs:** The DACs, which are used to generate the bias voltage (V_{bias}) for the readout circuit and to supply `VDDA` and `VDDD` to the PCS sensor, are controlled via a set of SPI signals. Specifically, each DAC includes a `SPI1_MOSI` and `SPI1_SCK` input. To simplify the design, these SPI lines were shared across all DACs by shorting the corresponding pins, resulting in a single global `SPI1_MOSI` and `SPI1_SCK` connection.

  The MCU provides several configurable `FLEXSPI` lines [11] that can be assigned to the `SPI1_SCK` and `SPI1_MOSI` functions. The specific pinout was selected based on routing convenience and layout constraints.

  In addition to the shared SPI lines, each DAC requires a dedicated `CS`/`SYNC` input to enable independent configuration of output voltage levels. To preserve this configurability, one of the key motivations for incorporating DACs, these control lines were routed individually to the MCU. Their layout adhered to the same signal integrity and routing principles applied to the ADC and clock control paths.

- **PCS DMA:** The `DMA_CSS_MOSI` and `DMA_CSS_SCK` signals also serve as SPI lines and follow the same design rationale as the SPI connections used for the DACs. However, unlike the shared SPI lines, these signals are connected to dedicated MCU pins and are not shared with any other peripherals.

- **Additional:** To provide maximum flexibility for the Software Group and future developers, two external oscillators, one operating at $24\,\mathrm{MHz}$ and another at $32.768\,\mathrm{kHz}$, were included, following the reference design of the FRDM-MCXN947 development board [13].

4

System Implementation

4.1. Full PCB

In the preceding chapters, all key schematics were defined and interconnected at the system level. The next phase of the project involves translating these theoretical schematics into a physical printed circuit board (PCB). This process consists of two main stages: first, the design and layout of the PCB using Altium Designer; and second, the fabrication of the board followed by the soldering of all components.

The subsequent chapters will detail the design decisions and layout considerations that guided the implementation of the final PCB.

4.1.1. Stackup

The stackup of a printed circuit board (PCB) defines the arrangement of its layers, including the number of layers and their respective functions. Based on the recommendation of T. Shen, the layout process was initiated using a six-layer PCB.

Eurocircuits, the PCB manufacturer selected for this project, offers a predefined six-layer stackup configuration that specifies the number and thickness of dielectric layers, as well as the weight and thickness of the copper layers.

The functional assignment of each layer depends on the board's application. For mixed-signal PCBs with high component density and the need for three signal layers, the stackup configuration shown below is recommended [26]:

1. Signal
2. GND
3. PWR
4. Signal
5. GND
6. Signal

If, during the design phase, it is determined that a third signal layer is unnecessary, the stackup may be modified to a GND/Signal/GND configuration for the bottom three layers. This alternative improves power-ground coupling and electromagnetic compatibility (EMC). Both configurations can be rather costly due to the need for additional drilling to access internal signal layers [26]:

1. Signal
2. GND
3. PWR

4. GND
5. Signal
6. GND

4.1.2. Electrical Considerations

Crosstalk is a critical factor in high-speed digital and mixed-signal PCB design. As a general rule of thumb, maintaining a spacing of at least $1\,\mathrm{mm}$ between signal traces can reduce crosstalk to below 10% of the signal voltage [10, Ch. 2.2, p. 57]. Additionally, placing grounded conductors between adjacent signal lines further suppresses crosstalk by acting as an electrostatic and electromagnetic shield.

At high frequencies, return currents follow the path of least inductance rather than least resistance. Fig. 4.1 illustrates the difference between low-frequency and high-frequency return paths. The challenge posed by high-frequency currents is that the return path becomes concentrated along a narrow region directly beneath the signal trace, rather than spreading across the entire ground plane. This concentration can result in a non-negligible voltage drop across the ground plane. Therefore, care must be taken to ensure that no other components use this region as a reference point, as they may no longer share a common zero-volt reference.

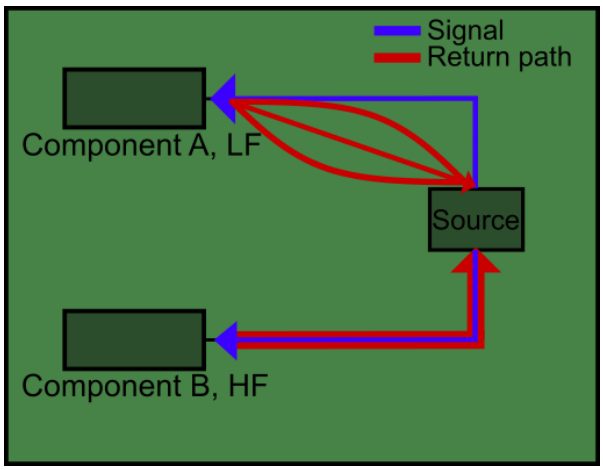


Figure 4.1: Current return path: low vs. high frequency

4.1.3. Mechanical Considerations

Most mechanical design constraints are dictated by the PCB manufacturer's specifications. In this project, the design rules provided by Eurocircuits are used and automatically verified by the Altium Designer software. Furthermore, it is recommended to avoid right-angle and acute-angle trace geometries, as these can act as etchant traps and increase susceptibility to corrosion[1] [10, Ch. 2.2, p. 60]. Wilson also advises that designers should strive for balanced copper coverage across all layers to minimize the risk of PCB warping during manufacturing or in operation [10, Ch. 2.2, p. 60].

4.1.4. Sensor readout

The readout architecture was derived in Section 3.3, resulting in multiple possible topologies. To ensure functional reliability, only the basic TIA will be included on the final PCB. The alternative configurations will first be evaluated separately using a test board, as further discussed in Section 4.2.2.

The selected TIA implementation is detailed in Table 3.4, which lists the final component specifications. The maximum expected resistor noise remains within acceptable thermal noise limits for 25C ; however, 1/f noise is also a concern, especially for near-DC measurements. Since 1/f noise is highly dependent

[1] Etchant traps are typically sharp internal corners (e.g., right or acute angles) where etching chemicals can accumulate, leading to uneven material removal, undercutting, or long-term corrosion issues.

on resistor type, with metal film resistors exhibiting significantly lower excess noise [27], high-precision metal film resistors have been chosen. Additionally, to minimize dielectric distortion in the feedback path, C0G-rated ceramic capacitors were selected.

The operational amplifier selected for the design is the LTC6268 [28], due to its exceptional suitability for high-performance, low-noise applications. From a noise perspective, the LTC6268 meets and exceeds the design requirements: it features a current noise density of $5.5\ \mathrm{fA}/\sqrt{\mathrm{Hz}}$ and a voltage noise density of $4.3\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, both of which are well below the established design constraints.

One of the most significant advantages of the LTC6268 is its extremely low input bias current of $\pm 3\ \mathrm{fA}$ (typical), which is several orders of magnitude lower than the maximum permissible input bias current of $13.67\ \mathrm{nA}$. Furthermore, the amplifier offers a generous gain-bandwidth product (GBW) of $500\ \mathrm{MHz}$, vastly exceeding the minimum required GBW of $168.6\ \mathrm{kHz}$. This ensures a substantial stability margin and reliable operation over the entire target frequency range.

The LTC6268 also provides a high slew rate of $400\ \mathrm{V}/\mu\mathrm{s}$, which is significantly above the minimum required $3.612\ \mathrm{mV}/\mu\mathrm{s}$, thereby supporting fast transient response and preserving signal integrity at high-speed switching between the pixels. To confirm its functional suitability within the overall circuit, the implementation of the LTC6268 was validated through simulations in LTspice. The results of these simulations are presented in Appendix A.

The same ADCs [19] used in the previous board were retained for this design to simplify integration for the software development team [29]. Although the resolution of these ADCs is limited to 12 bits, slightly below the minimum required 13-bit resolution calculated for C_{full} in 3.3.3. This trade-off was considered given the practical benefits of software consistency to reduce development overhead.

4.1.5. Layout

As discussed in Section 3.5, the ground planes are separated into `AGND` and `DGND`, requiring all components to be classified as either analog or digital. The analog domain includes the readout circuitry, external clock ports, analog power supply circuits, and the PCS chip itself. All remaining components are assigned to the digital ground domain.

Throughout the PCB, particularly along the power distribution network, test points were added to facilitate the measurement of voltage levels, signal integrity, and noise performance. These measurements can later be used to validate compliance with the specified requirements.

AGND

The PCB layout begins by organizing the analog components into as compact a footprint as possible. Special attention is given to matching the lengths of the `clk+` and `clk-` traces. This helps keep the clock jitter similar for both signals, preserving the differential nature. To achieve this, layout symmetry and repeated routing patterns are employed wherever possible. The resulting layout is shown in Fig. 4.2. In this figure, the green block represents the readout circuitry, the red blocks denote the DACs and associated decoupling/filtering circuits, the yellow block corresponds to the external clock ports, and the purple block indicates the PCS chip.

Since the PCS chip is not a commercially available component, a custom Altium footprint was developed based on the QFN MLPX5-24-OP01 package and the mounting frame specifications provided by C.R. Chen and F. Lin [30]. The footprint includes both the signal pads and the mechanical mounting holes, labeled MH1 through MH4 in Fig. 4.2.

It is worth noting that a portion of the red block overlaps with the PCS chip. This arrangement is intentional, as the PCS chip is mounted on the backside of the PCB. As recommended in [31], power circuits should be placed as close as possible to the load to minimize parasitic effects. Positioning the power components directly on the opposite side of the PCS chip allows for minimal trace lengths and a single via connection, thereby reducing noise and improving power integrity.

Furthermore, some components are placed either within or outside the yellow outline that surrounds the PCS chip. This distinction is based on mechanical constraints: the components located outside the outline are Through-Hole components with protruding parts on the back side of the PCB, which would interfere with the mechanical chamber and mounting structure of the PCS chip [30].

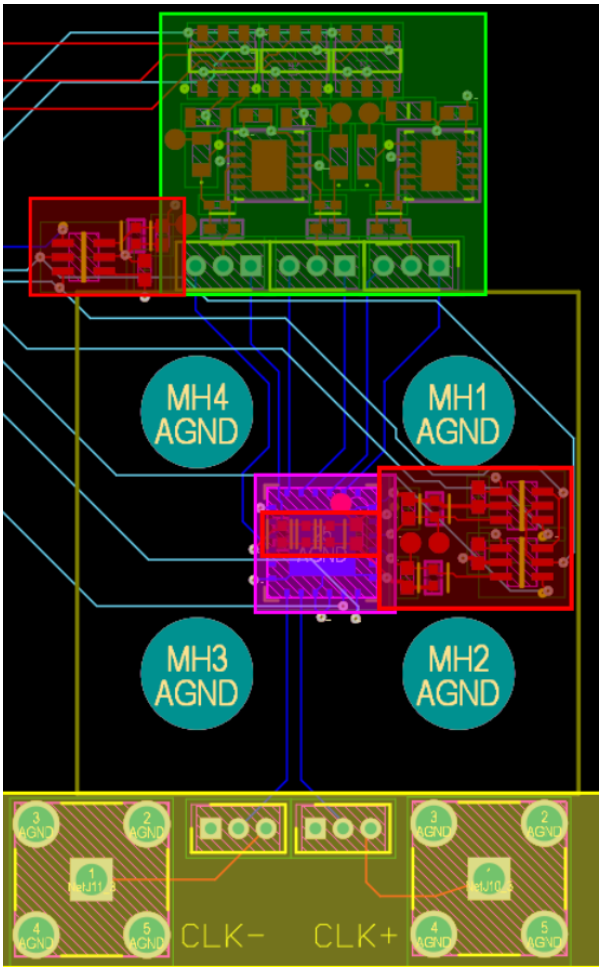


Figure 4.2: Analog section of the PCB layout

DGND

A similar design approach was applied to the digital section of the PCB. Considering the dimensions of the analog portion, all connectors were placed on a single side, in accordance with the requirement specified in **[ToR.2.1]**. Their corresponding support circuits were positioned nearby, with an emphasis on layout density.

Subsequently, a trial-and-error process was employed to determine the optimal placement of the MCU, its associated power infrastructure, and the routing of the I/O signals defined in 3.7. Figure 4.3 illustrates this layout: the connectors are shown in yellow, the MCU and its support circuits in magenta, the power components in red, and the impedance matching circuit from the readout section in green.

Complete PCB

Figure 4.4 provides an overview of the complete PCB layout, highlighting the separation between the analog and digital ground planes. In the lower central region, three zero-ohm resistors are placed to bridge the two ground domains at a controlled location.

The final PCB measures 45.4 mm × 66 mm, which corresponds to less than 75% of the area of the previous version designed by T. Shen.

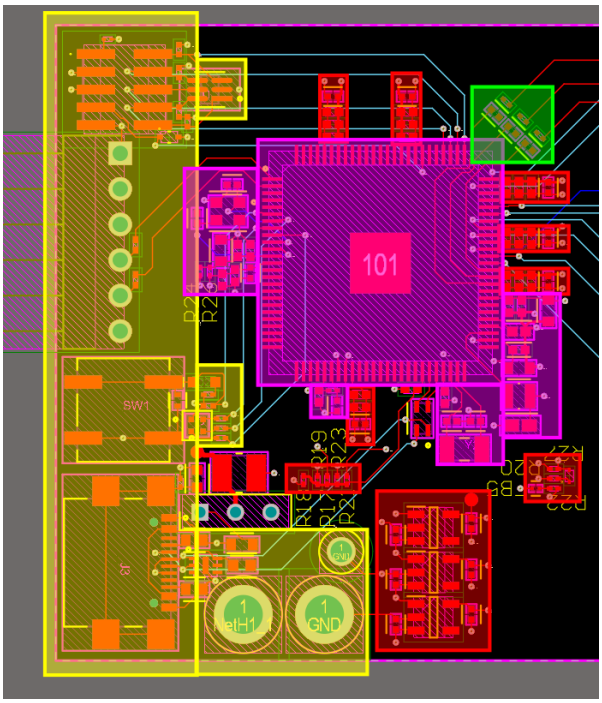


Figure 4.3: Digital section of the PCB layout

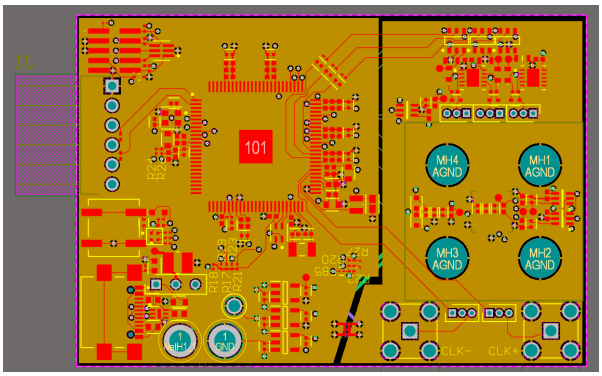


Figure 4.4: Top-level PCB layout showing the division between analog and digital ground planes, with three zero-ohm resistors bridging the two domains

4.2. Test board

To evaluate the variable gain and differential TIA configurations, a dedicated test board was developed. This board is designed as a shield compatible with the FRDM-MCXN947 [13] development board, utilizing the same MCU as the final integrated PCB to ensure firmware consistency and hardware compatibility.

The test board follows the same PCB design considerations as the main system, including layout constraints, grounding strategies, and component selection. Furthermore, the placement of male headers was designed to align precisely with the FRDM-MCXN947 development board, enabling a secure connection, while female headers were positioned to interface correctly with the adapter PCB of the measurement group [32].

4.2.1. Additional components

The TIA stages on the test board mirror those used in the 40 MHz configuration of the final PCB. For the variable gain path, the TIA employs feedback components (R_f and C_f) which are calculated for I_{in} at $f_s = 100\,\text{MHz}$, however share the same electrical rating as those used in the original design. The same equivalence applies to the resistor network in the differential amplifier stage. The differential amplifier continues to utilize the LTC6268 [28] op-amp, which remains suitable for this application by exceeding all performance metrics.

For variable gain control, the AD8400 [33] digital potentiometer was selected. Although no stringent performance constraints were defined for this component, the AD8400 offers several favorable characteristics. Unlike many digital potentiometers that are optimized for low-bandwidth reference-setting applications, the AD8400 supports a bandwidth of 600 kHz, which is more than sufficient for the system requirements. In addition, it exhibits a voltage noise density of 9 nV/$\sqrt{\text{Hz}}$, which is relatively low and acceptable given its placement directly at the output where the max rms noise voltage is $1 \cdot 10^{-2}$ V.

4.2.2. Layout

The PCB layout is partitioned into distinct analog and digital sections to minimize noise coupling and ensure signal integrity. The outer layers are designated for digital components and routing, while the inner layers accommodate the measurement PCB and experimental readout circuitry, as can be seen in Figure 4.5. Accordingly, the power and ground planes are also segmented to reflect this separation, reducing interference between the two domains.

Additionally, test points are placed at nodes throughout the readout circuitry to facilitate debugging and performance verification, as can be seen in the 3D schematic in Figure 4.6 . A dedicated ground connector is included to provide direct access to the analog ground plane for accurate reference during measurements.

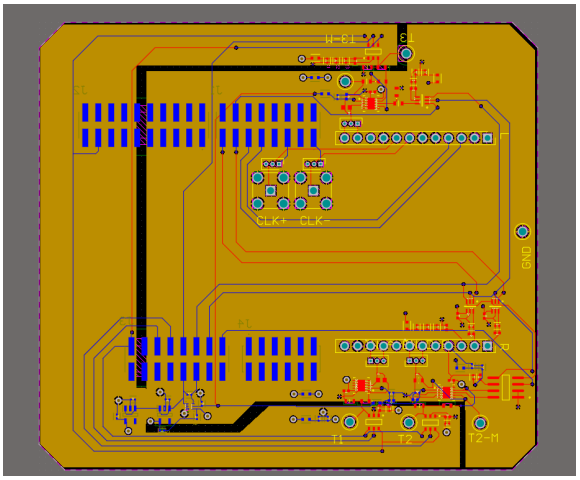


Figure 4.5: 2D testboard schematic

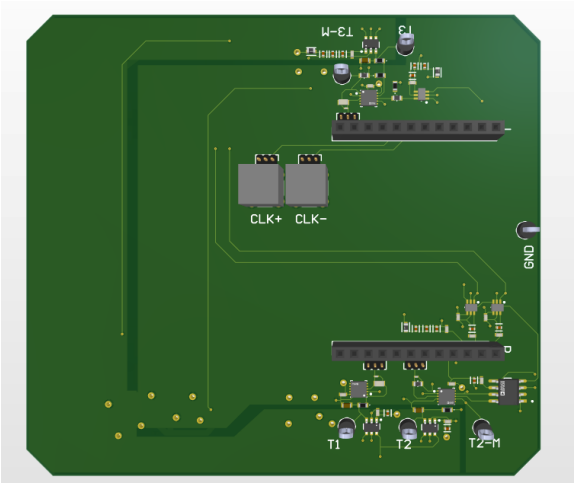


Figure 4.6: 3D testboard schematic

5

Discussion

5.1. Full PCB

Based on the techniques and methodologies described in the previous chapters, a complete PCB was designed using Altium Designer, as shown in Figure 5.1.

Due to time constraints, the PCB has not yet been fabricated. As a result, no measurements or validation tests have been performed, and several requirements cannot yet be verified. The requirements related to the final PCB size **[MR.2.5]** and the placement of connectors on a single side **[ToR.2.1]** have been fulfilled. Progress has also been made toward meeting the other requirements. However, their functionality still needs to be experimentally validated.

The requirement concerning input-referred noise at the PCS outputs **[MR.2.11]** presents a particular challenge. No currently available component is capable of achieving the required noise spectral density, and the effectiveness of the implemented noise mitigation techniques remains to be evaluated.

Nevertheless, the project and testing of the PCB in particular is expected to continue after this thesis.

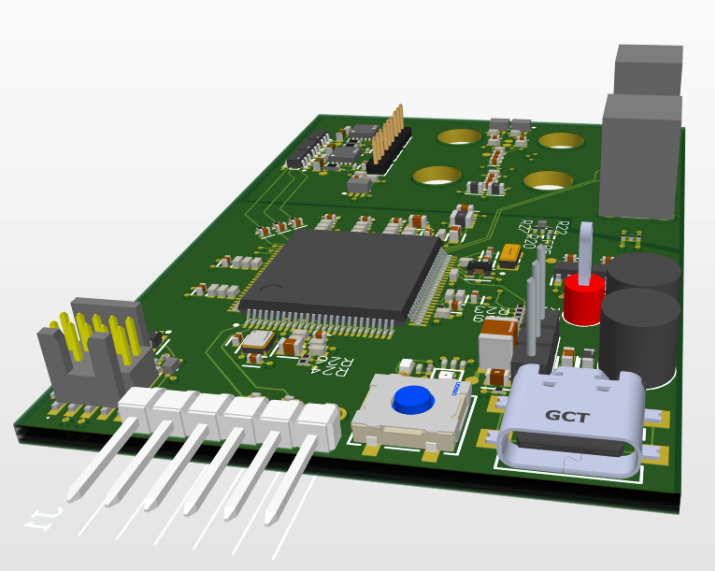


Figure 5.1: Rendered image of the complete PCB in Altium Designer

5.2. Test Board & Readout Circuit

While a readout circuit has been fully designed and implemented on the main PCB, and the experimental architectures have been realized on a dedicated test PCB, the validation thus far has primarily relied on simulation results. Although simulations suggest that these designs effectively address the key challenges, real-world conditions often diverge from idealized models. Therefore, conclusive performance evaluation will only be possible through empirical measurements.

One critical concern is the influence of the analog supply voltage (VDDA) noise. If the noise from VDDA directly translates to output voltage noise without adequate suppression, then noise-reduction strategies applied elsewhere in the signal chain, may prove ineffective. In such a scenario, VDDA noise could become the dominant contributor, potentially overshadowing all other carefully mitigated noise sources.

6

Conclusion

This thesis presents the design and validation of a mixed-signal PCB and analog readout circuitry for a CMOS Pixelated Capacitive Sensor (PCS) array, forming the core of an electronic nose (e-nose) system. The primary objective was to facilitate reliable detection of attofarad changes in pixel capacitance induced by the interaction of sensing inks with volatile organic compounds (VOCs), while meeting stringent constraints on noise, size, and integration.

A comprehensive analog front-end was developed, centered around a transimpedance amplifier (TIA) designed for low input-referred noise and sufficient bandwidth to accurately capture pixel-level signals. To extend the system's dynamic range and enable differential readout of VOC-induced variations, additional stages including a differential amplifier and programmable variable-gain stage were evaluated and implemented on a extra test board.

The main PCB integrates the analog readout chain with an NXP MCXN947 microcontroller, programmable power rails, and standard communication interfaces, all within a compact six-layer layout optimized for mixed-signal performance. Grounding and power distribution strategies were carefully designed to mitigate electromagnetic interference (EMI) and minimize noise coupling between analog and digital domains.

Although time constraints prevented fabrication and noise measurements on the assembled board, extensive simulations and component-level verification confirm that the design in theory satisfies almost all mandatory requirements and meets most trade-off targets outlined in the Programme of Requirements. The proposed test board further provides a platform for exploring alternative readout architectures and for refining the signal chain under controlled experimental conditions.

In conclusion, the system developed in this work lays a robust foundation for high-resolution capacitive sensing in integrated VOC detection platforms and contributes to the broader effort of reducing pesticide usage through early disease detection in greenhouse environments.

Future Work

While this project has resulted in a fully routed PCB design and analog readout circuit, several steps remain to fully characterize system performance and ensure long-term reliability. This section outlines the proposed future work for both the main board and the test board.

Main PCB

After completing the final design checks, the PCB will be fabricated by Eurocircuits. Once manufactured and assembled, the following validation steps are proposed:

- **Power Verification:** Measure all voltages using the designated test pads. Verify that supply voltages are stable and within tolerance. **1/f Noise Characterization:** Conduct a detailed characterization of 1/f noise behavior and its propagation through the readout chain.
- **MCU Communication:** Confirm correct programming and debugging functionality through the SWD interface, and verify UART or USB-C data transmission.
- **PCS Chip Integration:** With an unused PCS chip that has not been exposed to ESD events, attach the sensor to the board. Measure the ADC input noise under quiescent conditions and compare these with similar measurements on the previous board.
- **Readout Functionality:** Evaluate the analog signal chain by applying known current and noise input values and verifying the end-to-end digital performance.

Test Board

After fabrication and component assembly, the following steps are planned:

- **Development Board Integration:** Interface the analog circuits with the NXP FRDM-MCXN947 development board to test digitization quality and validate MCU-side data acquisition routines.
- **Alternative Architectures:** Compare the basic TIA with variable gain and differential designs under controlled signal conditions to evaluate potential improvements in sensitivity and noise margin.

These steps will provide additional insight into the analog front-end's limitations and inform the design of future PCS-based e-nose systems. If successful, these approaches could serve as a standard readout implementation for future works.

A

Simulation results

To validate that the designed TIA meets the specified performance criteria, a series of simulations were conducted in LTspice.

DC Current Sweep
The first simulation involved a DC current sweep to verify the linearity of the TIA's output response. As shown in Figure A.7, the TIA exhibits a linear output over the expected input current range. For clarity, a zoomed-in view of the measurement current range is provided in Figure A.2, demonstrating that the output remains linear even for small signal variations around the baseline.

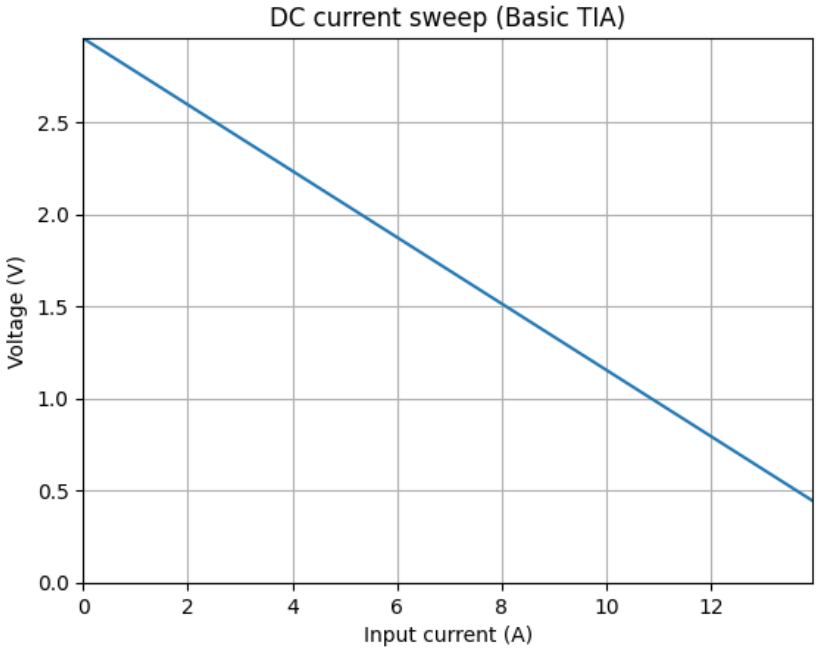


Figure A.1: DC sweep of input current showing full linear range

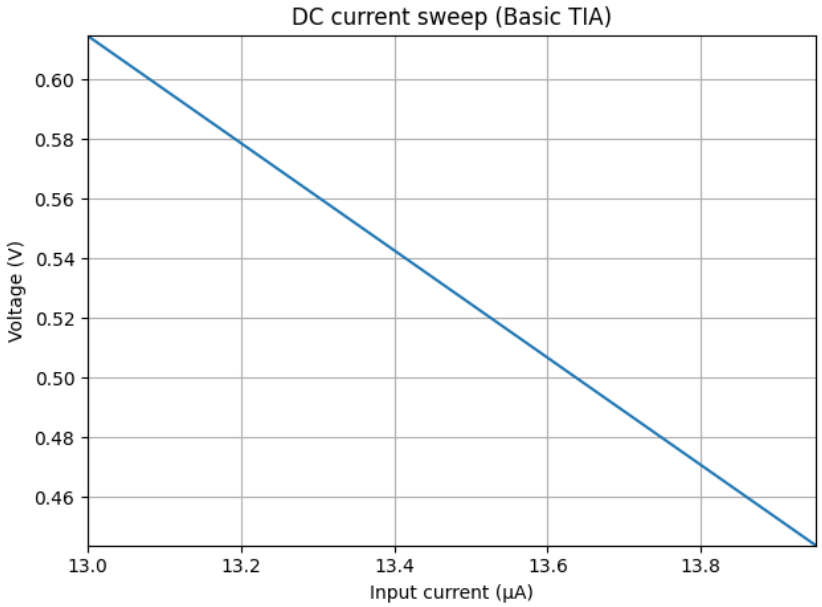


Figure A.2: Zoomed-in view of DC sweep around intrinsic current

Frequency Response and Time-Domain Validation

The AC frequency response of the TIA, shown in Figure A.3, confirms that the circuit behaves as a first-order low-pass filter. The gain matches the expected transimpedance value of 180K,with a -6 dB cut off at 33kHz.

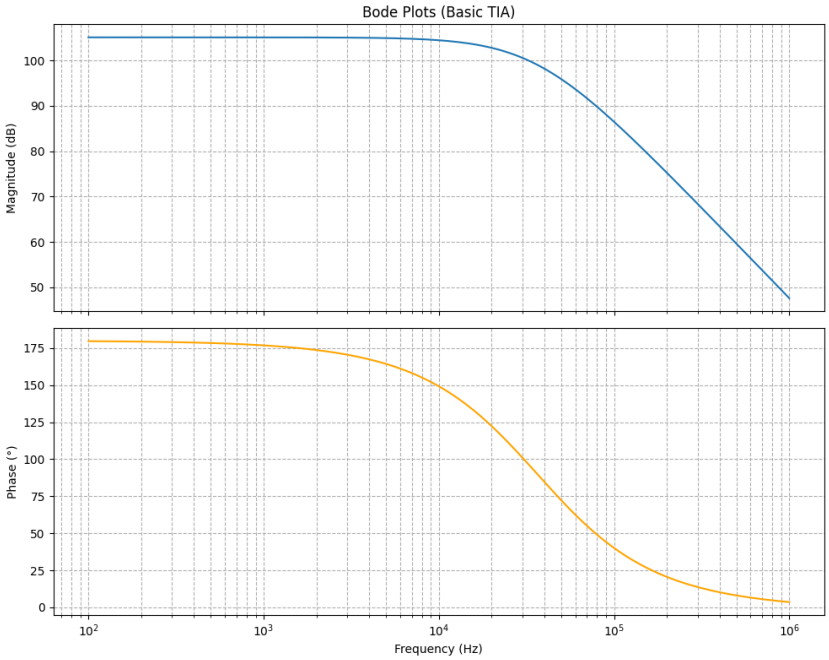


Figure A.3: Bode plot of the TIA

Additionally, the transient response was examined using a step input simulating a current transition from the maximum value to the intrinsic level and back. As shown in Figure A.4, the rising and falling edge times were found to be approximately $27.18\ \mu\text{s}$ and $31.65\ \mu\text{s}$, respectively. Although not within 10% of the ideal settling time derived from the earlier slew rate calculation, these results are consistent with the expected behavior of a low-pass system. Given a time constant of $4.82\ \mu\text{s}$, a much slower response than $24.1\ \mu\text{s}$ isn't to be expected due to the filtering characteristics.

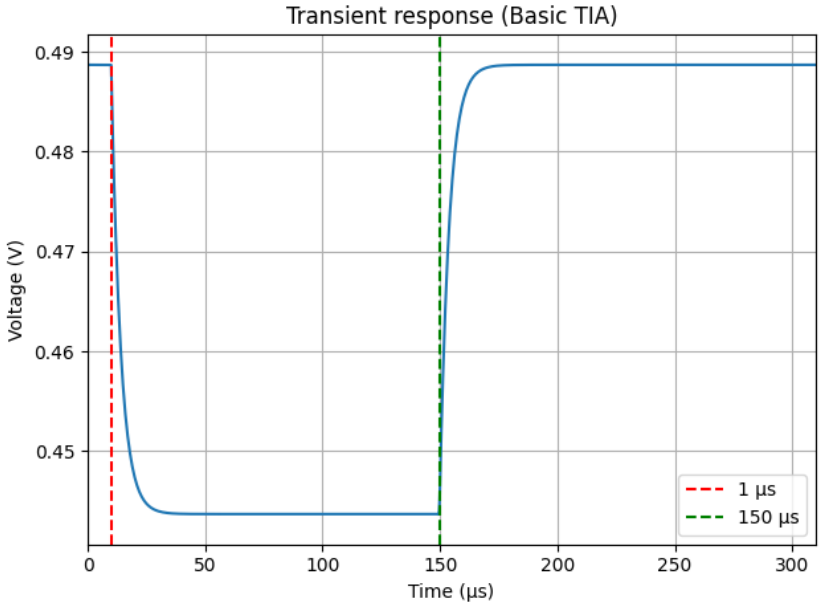


Figure A.4: Impulse response of the TIA showing rising and falling edge times

Noise Analysis

Finally, the most critical evaluation involved the TIA's noise performance. Frequency-domain noise plots and component-wise noise contributions are shown in Figures A.5 and A.6, respectively. The total output-referred noise RMS was measured at $1.9531\ \mu\text{V}$, which is significantly lower than the maximum allowed value of $630.5\ \mu\text{V}$. The analysis shows that the noise is primarily dominated by the op-amp's internal contributions, with the resistors contributing minimally.

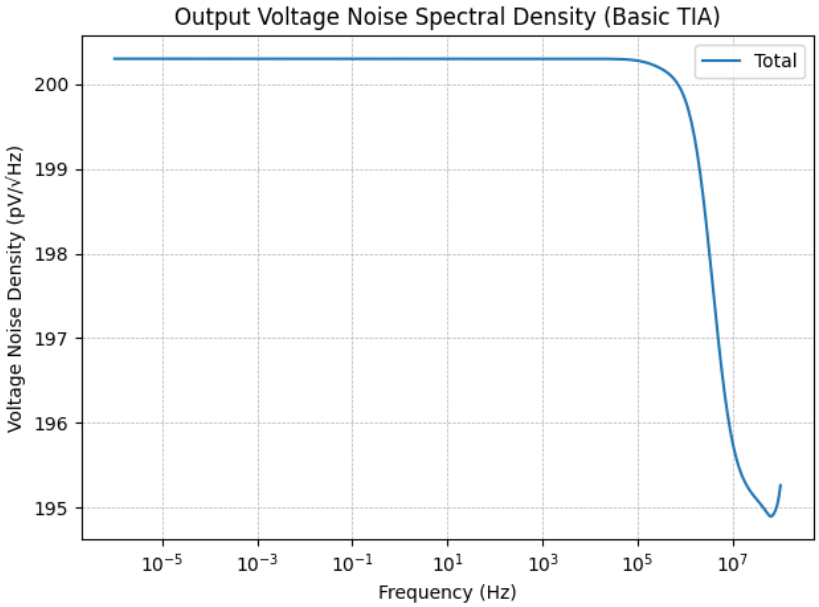


Figure A.5: Frequency-domain noise spectrum of the TIA

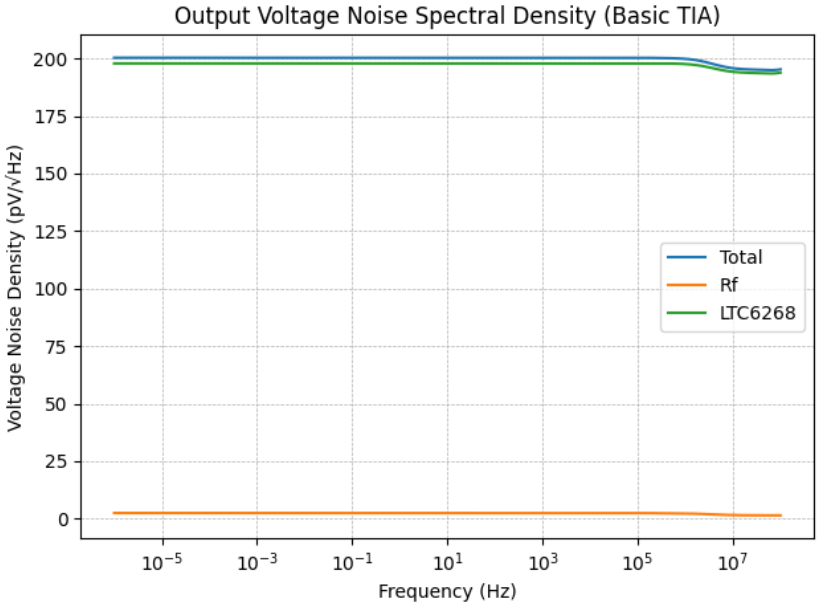


Figure A.6: Breakdown of noise contributions by component

It is important to note that the simulated noise results do not include input noise from the source, which could further impact the total system noise. Nonetheless, these simulations confirm that the TIA, as designed, provides robust performance well within the required specifications.

A.0.1. Differential

The most relevant simulations for comparing the TIA with added differential stage architecture with the original design are the DC sweep and the noise performance analyses.

As shown in Figure A.7, the TIA with a differential stage exhibits a sharp voltage rise beginning before $13.67\ \mu$A. A zoomed-in view of the relevant measurement current range is provided in Figure A.2, clearly demonstrating an improved voltage resolution per unit of current.

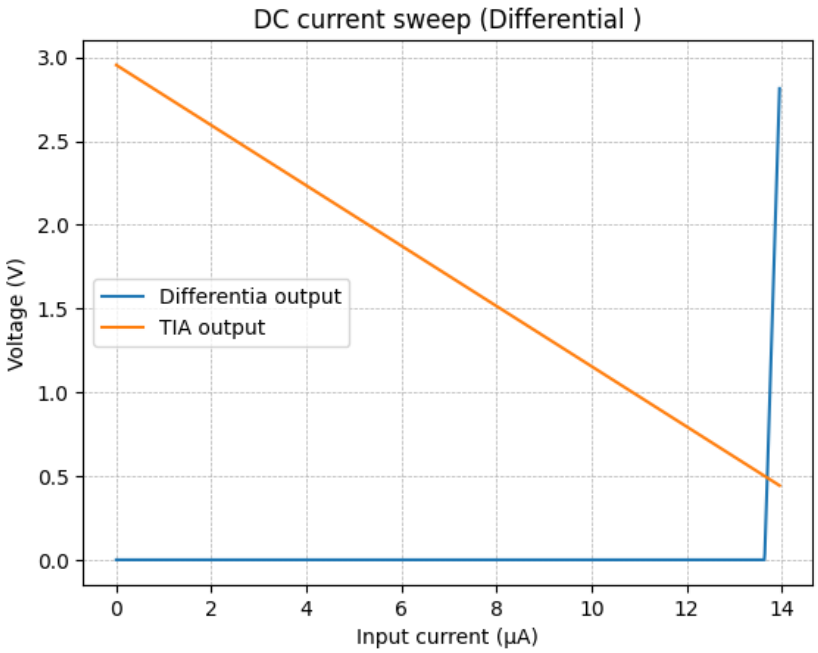


Figure A.7: DC sweep of differential TIA

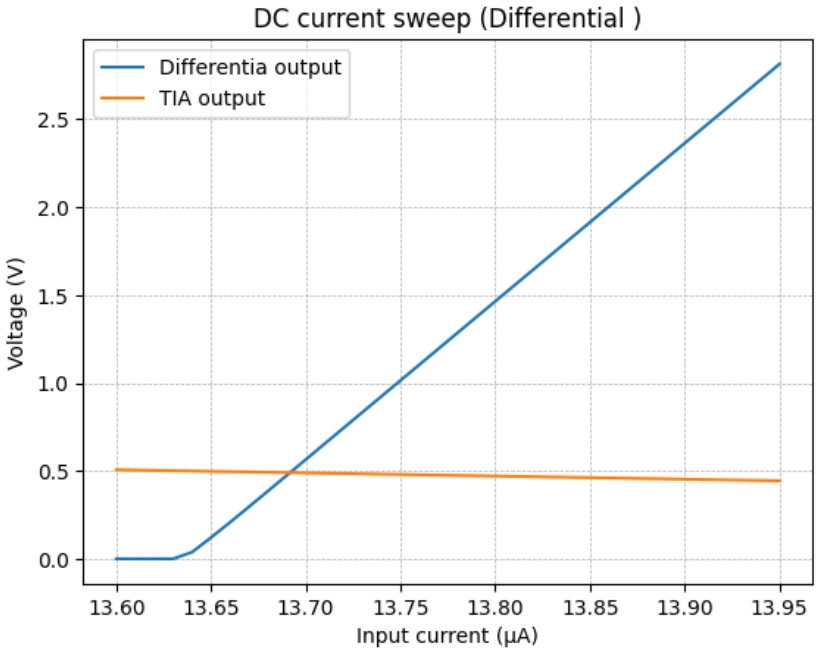


Figure A.8: Zoomed-in DC sweep around the measurement current range

In terms of noise performance as can be seen in figure A.9, the total RMS noise is slightly higher at $1.2774\ \mu$V, yet it remains well below the acceptable limit. However, the simulation reveals that the $1/f$ noise of the operational amplifiers degrades performance more in this differential configuration than in the basic TIA alone. The thermal noise contribution from resistors remains negligible A.10.

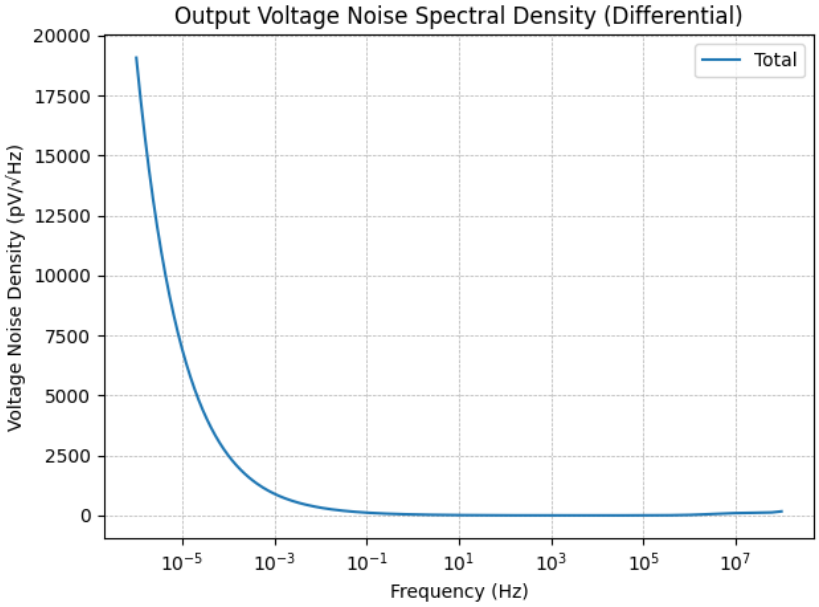


Figure A.9: Total output noise of the differential TIA

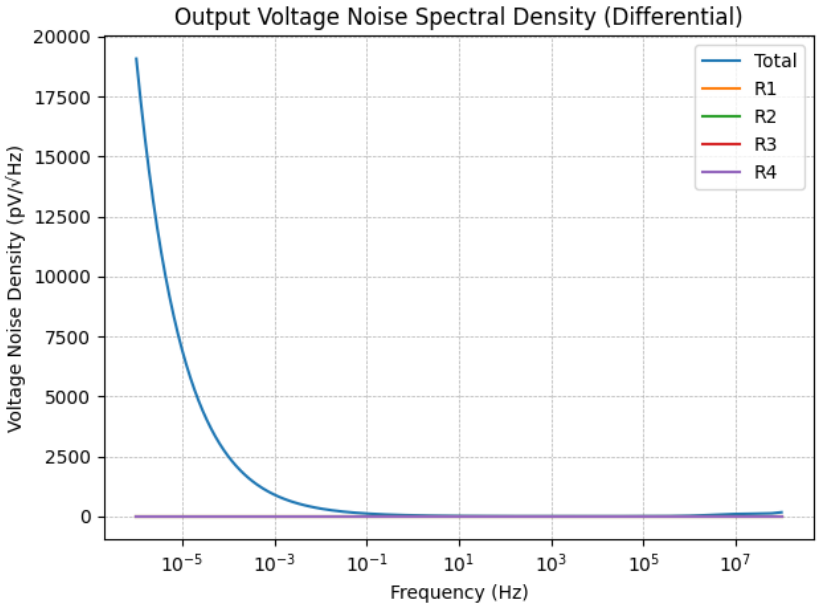


Figure A.10: Noise contributions by circuit components

B

TIA T network

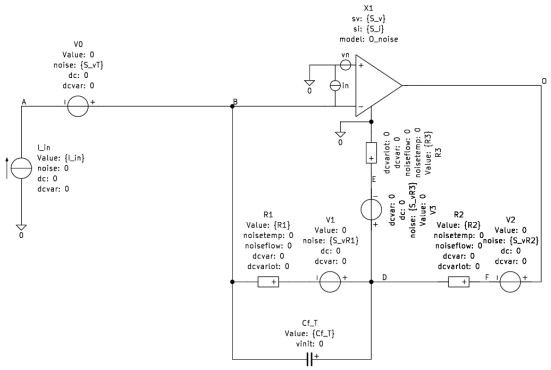


Figure B.1: Noise model T-network

As previously discussed in Section 3.3.5, the T-network configuration attenuates the amplifier's output via a voltage divider before feedback is applied. This results in a modified transimpedance transfer function:

$$\frac{V_{\text{out}}}{I_{\text{in}}} = \frac{\left(\frac{C_f R_1 R_2 R_3 s}{R_1 R_2 + R_1 R_3 + R_2 R_3} + 1\right)\left(-\frac{R_1 R_2}{R_3} - R_1 - R_2\right)}{C_f R_1 s + 1} \tag{B.1}$$

The characteristics of this transfer function are:

- **Zero:**

$$s = \frac{R_1 R_2 + R_1 R_3 + R_2 R_3}{C_f R_1 R_2 R_3} = \frac{1}{C_f R_1} + \frac{1}{C_f R_2} + \frac{1}{C_f R_3}$$

- **Pole:**

$$s = \frac{1}{C_f R_1}$$

- **DC Gain:**

$$\left(-\frac{R_1 R_2}{R_3} - R_1 - R_2\right)$$

Assuming the pole is located at a much higher frequency than the zero (i.e., $|s_{\text{pole}}| \gg |s_{\text{zero}}|$), the T network can be approximated as having a flat frequency response in the low-frequency region up to its $-3\,\text{dB}$ cutoff. Under this assumption, the transfer function reduces to its DC gain with a single-pole roll-off defined by:

The DC gain, determined by the resistive network as:

$$\text{Gain} = -\left(\frac{R_1 R_2}{R_3} + R_1 + R_2\right)$$

The cutoff frequency is set by the pole:

$$\omega_c = \frac{1}{C_f R_1}$$

Hence, the gain is defined by R_1, R_2, and R_3, while the cutoff frequency is controlled by R_1 and C_f.

Since transimpedance gain is defined by a combination of multiple resistors, higher gain values can be achieved using resistor components smaller than those required in a conventional single-resistor TIA. Consequently, a reduction in thermal noise would be expected due to the use of lower resistance values.

However, this behavior is somewhat counterintuitive. Across all tested configurations, no resistor combination within the T-network yielded a lower total output RMS noise voltage than that of a standard TIA employing a single feedback resistor.

The underlying cause lies in how the transfer function shapes the contribution of each noise source to the output.

$$V_{\text{out}} = V_{nR1} \cdot \frac{R_2 + R_3}{R_3(C_f R_1 s + 1)} \qquad V_{\text{out}} = V_{nR2} \cdot 1 \qquad V_{\text{out}} = V_{nR3} \cdot \left(-\frac{R_2}{R_3}\right)$$

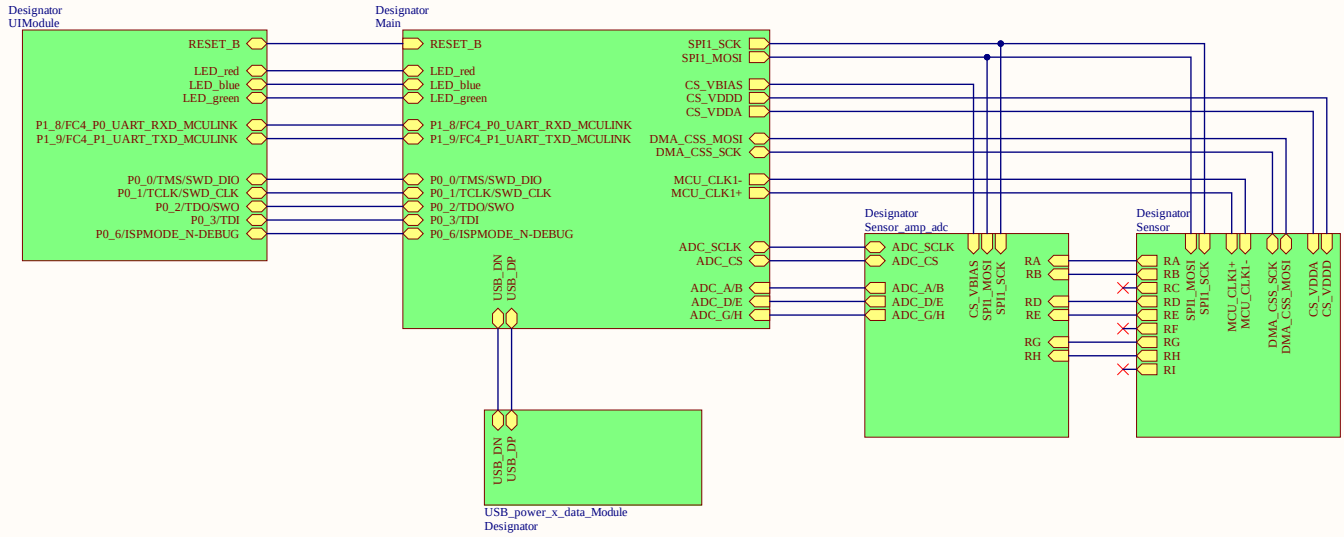
For V_{nR2}, decreasing the resistance lowers not only its own RMS noise contribution but also that of V_{nR1} and V_{nR3}. Therefore, R_2 should be made as small as possible.

For V_{nR3}, increasing the resistance reduces its own RMS contribution, because votlage the noise increase with root (R3) but is divided by R3. In addition decreases the effect of V_{nR1}. Since it has no impact on V_{nR2}, R_3 should be made as large as possible.

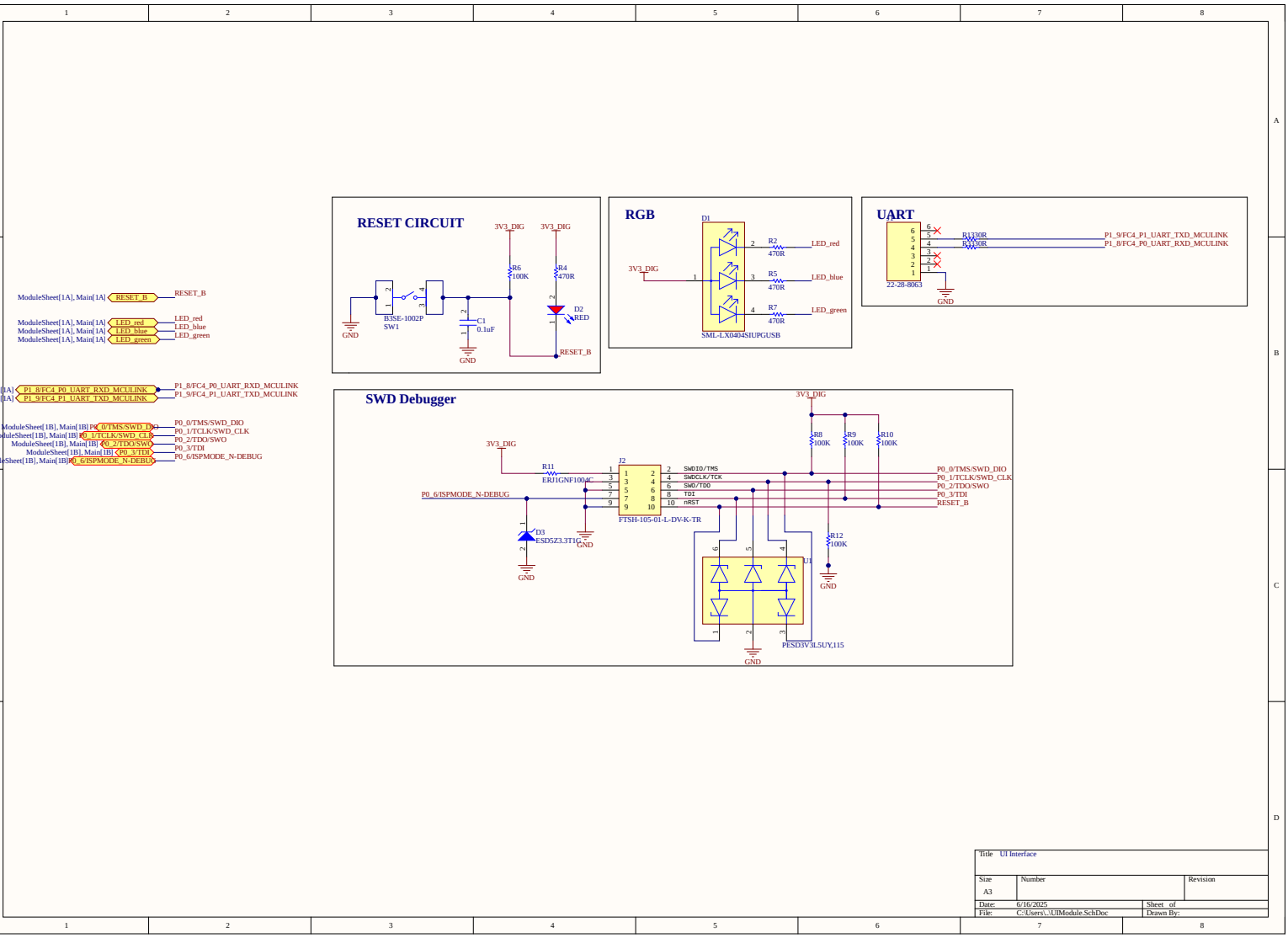
Hence, the optimal configuration is to set R_3 as an open circuit and R_2 as a short circuit, effectively reducing the circuit to the basic TIA topology.

C

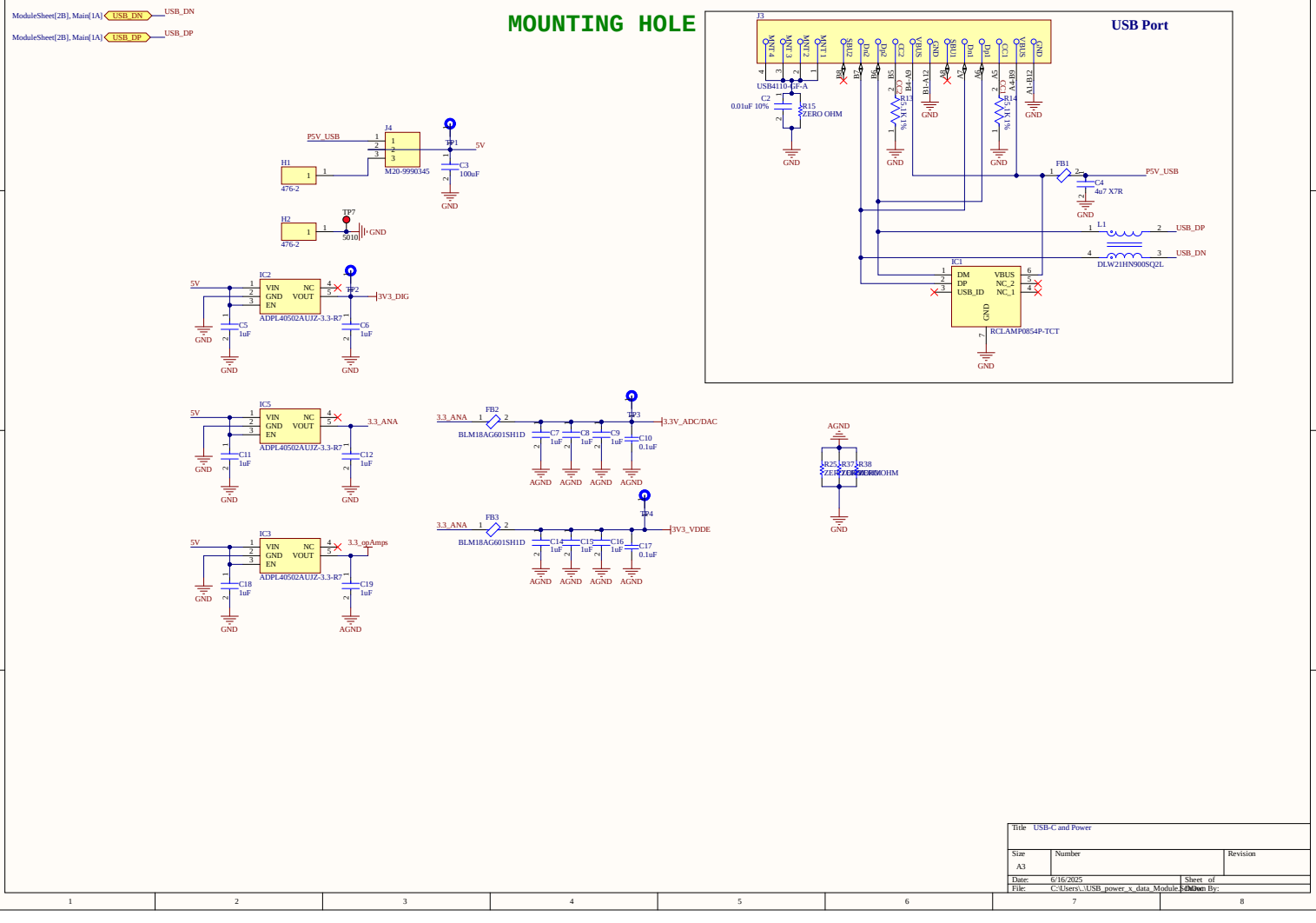
Schematics

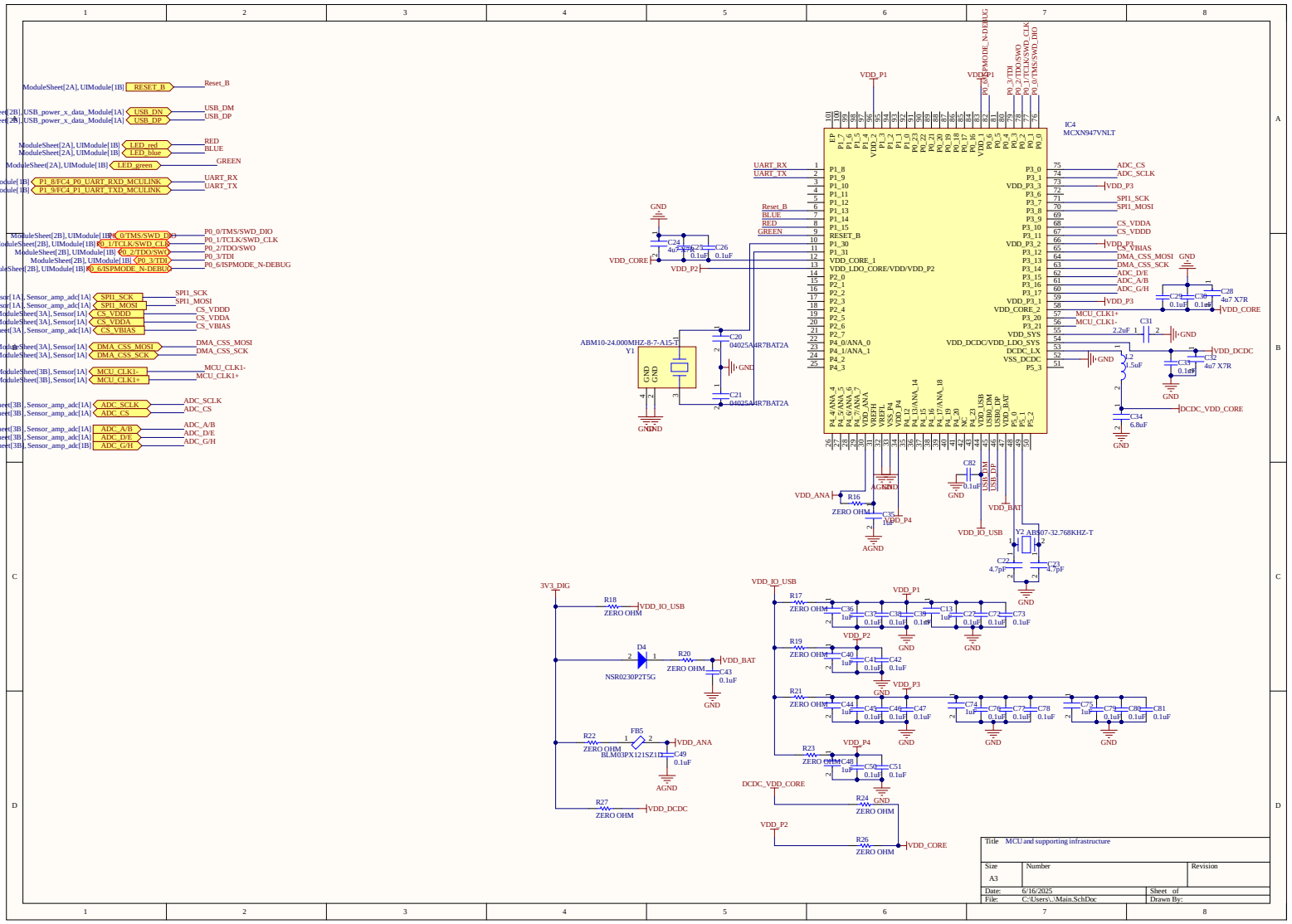


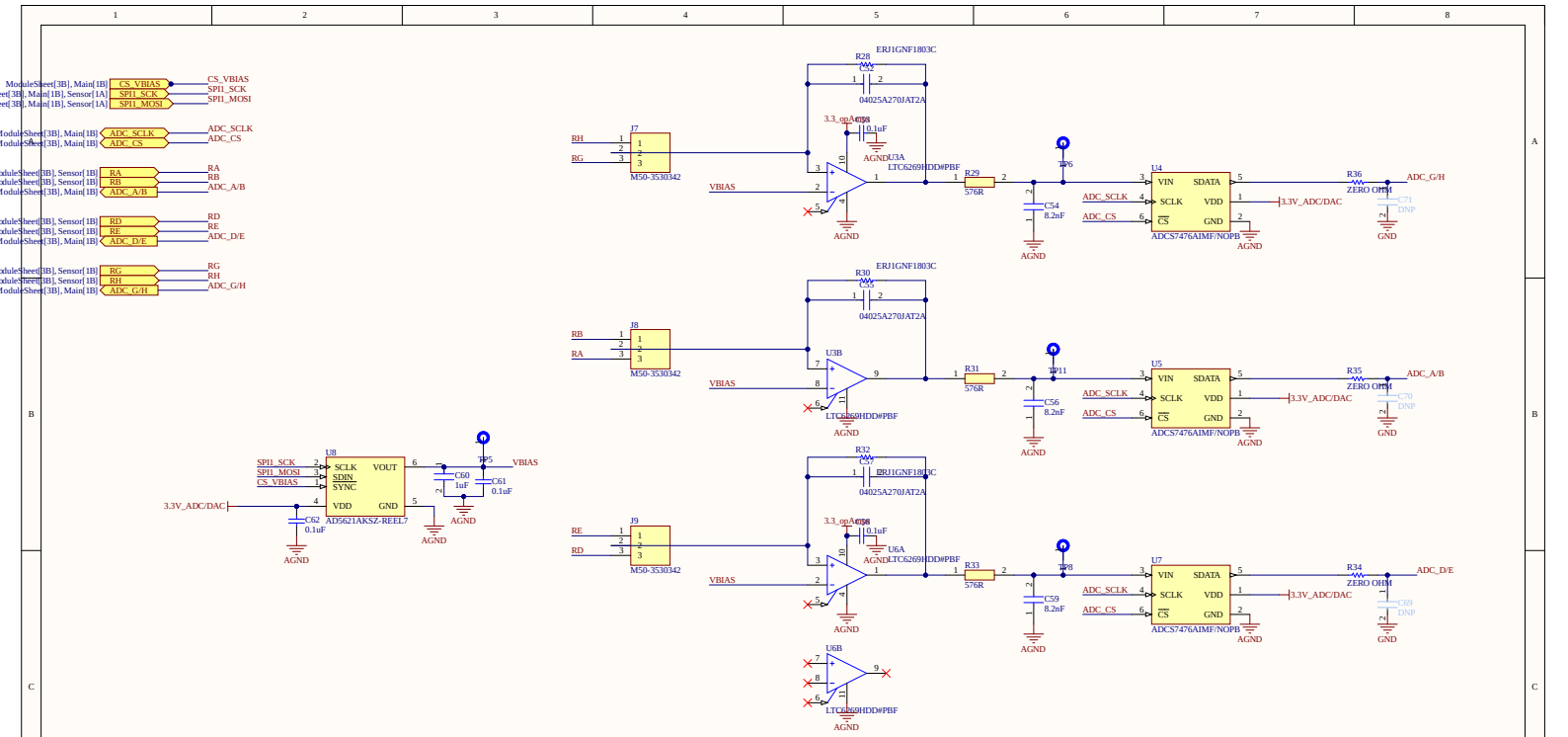
Title			
Size	Number		Revision
A4			
Date:	6/16/2025	Sheet of	
File:	C:\Users\..\ModuleSheet.SchDoc	Drawn By:	



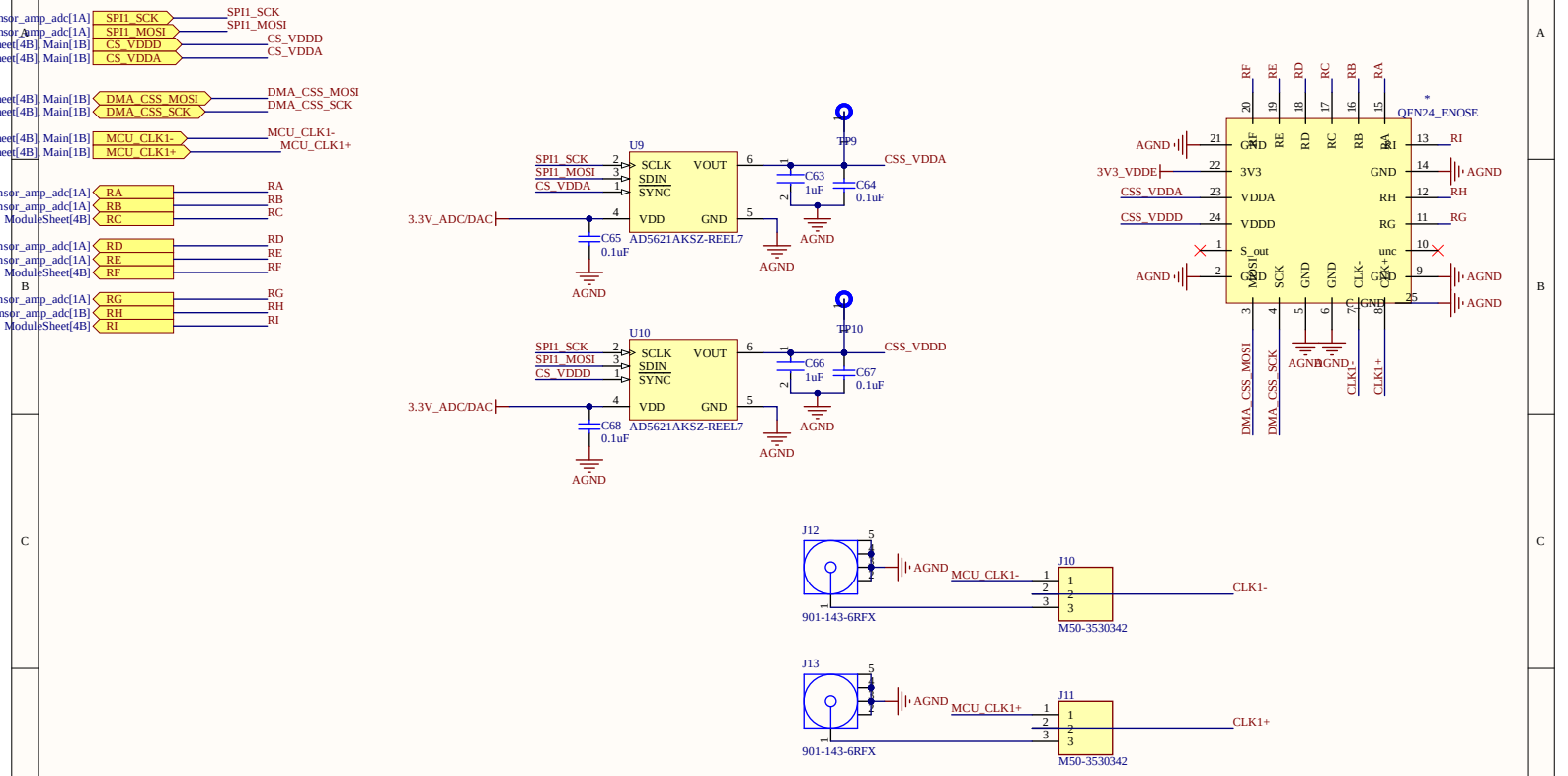
Title	UI Interface		
Size	Number		Revision
A3			
Date:	6/16/2025	Sheet	of
File:	C:\Users\..\UIModule.SchDoc	Drawn By:	


MOUNTING HOLE
USB Port
ModuleSheet[2B], Main[1A]
USB_DN
USB_DP
J3
USB4110-GF-A
C2
0.01uF 10%
R15
ZERO OHM
R14
5.1k 1%
R13
5.1k 1%
FB1
C4
4u7 X7R
P5V_USB
L1
DLW21HN900SQ2L
IC1
RCLAMP0854P-TCT
J4
M20-9990345
H1
H2
476-2
TP1
C3
100uF
5V
TP7
GND
IC2
ADPL40502AUJZ-3.3-R7
TP2
3V3_DIG
C5
1uF
C6
1uF
IC5
3.3_ANA
C11
1uF
C12
1uF
IC3
3.3_opAmps
C18
1uF
C19
1uF
AGND
FB2
BLM18AG601SH1D
C7
1uF
C8
1uF
C9
1uF
C10
0.1uF
TP3
3.3V_ADC/DAC
FB3
C14
1uF
C15
1uF
C16
1uF
C17
0.1uF
TP4
3V3_VDDE
R25
R37
R38
ZERO OHM
Title USB-C and Power
Size A3
Number
Revision
Date: 6/16/2025
Sheet of
File: C:\Users\..\USB_power_x_data_Module.SchDoc
Drawn By:


IC4
MCXN947VNLT
ABM10-24.000MHZ-8-7-A15-T
Y1
V2 ABS07-32.768KHZ-T
NSR0230P2T5G
BLM03PX121SZ1D
Title MCU and supporting infrastructure
Size A3
Number
Revision
Date: 6/16/2025
Sheet of
File: C:\Users\..\Main.SchDoc
Drawn By:



Title	Readout circuit		
Size	Number		Revision
A3			
Date:	6/16/2025	Sheet	of
File:	C:\Users\..\Sensor_amp_adc.SchDoc	Drawn By:	



Title	Sensor and Sensor infrastructure	
Size: A4	Number	Revision
Date: 6/16/2025		Sheet of
File: C:\Users\..\Sensor.SchDoc		Drawn By:

D

PCS Chip Pinout and Functionality

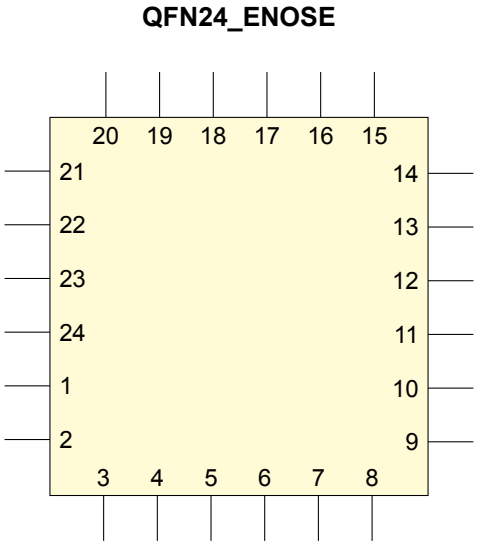


Figure D.1: PCS chip schematic representation

Below is a summary of the pin functionality as implemented on the main PCB. The PCS chip consists of three separate arrays, each with two redundant readout lines and one test line. The test lines are not connected on the main PCB to save space, but could be routed to test points if needed.

1. **S_out:** Unused.
2. **AGND:** Connected to the analog ground plane.
3. **DMA_CSS_MOSI:** SPI data input; connected to an SPI-capable pin on the MCU.
4. **DMA_CSS_SCK:** SPI clock input for synchronization.
5. **AGND:** Connected to the analog ground plane.
6. **AGND:** Connected to the analog ground plane.
7. **CLK−:** Negative differential clock input; routed close to CLK for field cancellation.
8. **CLK:** Positive differential clock input; routed close to CLK−.
9. **AGND:** Connected to the analog ground plane.
10. **Unconnected.**

11. **RG:** Readout line 1 of Array 3.
12. **RH:** Readout line 2 of Array 3.
13. **AGND:** Connected to the analog ground plane.
14. **RI:** Test line of Array 3; unused on the main PCB.
15. **RA:** Readout line 1 of Array 1.
16. **RB:** Readout line 2 of Array 1.
17. **RC:** Test line of Array 1; unused on the main PCB.
18. **RD:** Readout line 1 of Array 2.
19. **RE:** Readout line 2 of Array 2.
20. **RF:** Test line of Array 2; unused on the main PCB.
21. **AGND:** Connected to the analog ground plane.
22. **VDDE (3.3 V):** Main power supply input.
23. **VDDA:** Variable supply, sourced from a DAC.
24. **VDDD:** Variable supply, sourced from a DAC.

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