Development of in-situ doped poly-SiO_x passivating contacts for high-efficiency solar cells

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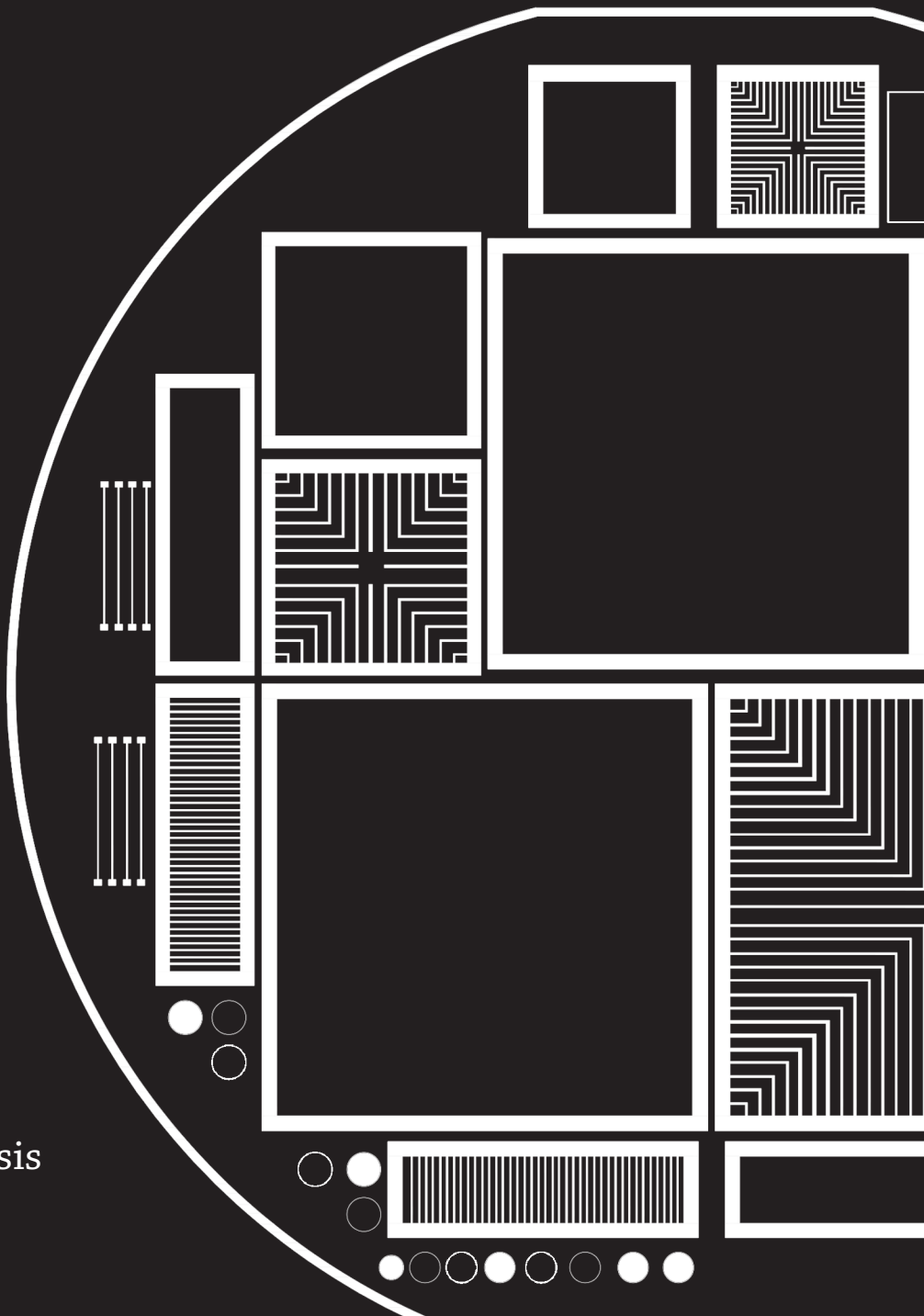

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Development of in-situ doped poly-SiO_x passivating contacts for high-efficiency solar cells

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Abstract

Carrier-selective passivating contacts (CSPCs) is now a popular contact structure that effectively passivates the crystalline silicon (c-Si) surface as well as selectively extracts the specific type of charge carrier (electrons or holes). In this thesis work, we developed the CSPCs based on oxygen-alloyed polycrystalline silicon (poly-SiO_x) passivating contacts, which shows less parasitic absorption especially in the terms of free carrier absorption (FCA) compared with the polycrystalline silicon (poly-Si) passivating contacts.

In order to deploy poly-SiO_x CSPCs in c-Si solar cells, we optimized the oxygen content, doping level, high-temperature annealing as well as the hydrogen passivation process. As a result, the excellent passivation for n-type poly-SiO_x passivating contact on both flat surface (implied-V_{OC} of 727 mV and J_0 of 2.4 fA/cm^2) and textured surface (implied-V_{OC} of 723 mV and J_0 of 6.9 fA/cm^2) and for p-type poly-SiO_x passivating contact on flat surface (implied-V_{OC} of 709 mV and J_0 of 13.9 fA/cm^2) are obtained.

With the optimized poly-SiO_x passivating contacts, the front and back contacted (FBC) solar cells were fabricated in this thesis. An excellent fill factor of 83.5% was obtained in the solar cell with front and rear poly-SiO_x passivating contacts, indicating an efficient carrier transport and collection. An active area efficiency of 21.5% featuring $J_{SC,active}$ of 40.8 mA/cm^2 was measured on a front side textured FBC solar cell with the optimized poly-SiO_x passivating contacts. It indicates the potential for achieving a conversion efficiency of above 23.0 % with the same cell configuration in the short term.

Keywords: Carrier selective passivating contacts, oxygen-alloyed polycrystalline silicon, tunneling oxide, plasma enhanced chemical vapor deposition, high-temperature annealing, hydrogen passivation

Contents

Nomenclature

τ	Effective lifetime
ρ	Contact resistivity
ALD	Atomic layer deposition
a-Si	Amorphous silicon
a-Si:H	Hydrogenated amorphous silicon
c-Si	Crystalline silicon
CTLM	Circular transfer length method
CSPCs	Carrier-selective passivating contacts
DI water	Deionized water
DSP	Double side polished
EQE	External Quantum Efficiency
FBC	Front and back contacted
FF	Fill factor
FGA	Forming gas annealing
FST	Front side textured
FZ	Float Zone
HNO_3	Nitric acid
IBC	Interdigitated back contact
iV_{OC}	Implied open-circuit voltage
ITO	Indium Tin Oxide
J_0	Saturation current density
J_{SC}	Short circuit current density
LPCVD	Low pressure chemical vapor deposition
NAOS	Nitric acid oxidation of silicon
PECVD	Plasma enhanced chemical vapor deposition
pFF	Pseudo fill factor
Poly-Si	Polycrystalline silicon
Poly-SiO_x	Polycrystalline silicon oxide

QSSPC	Quasi-steady-state photo conductance
R_{sheet}	Sheet resistance
SiO_x	Silicon oxide
T_{anneal}	Annealing temperature
TCO	Transparent conductive oxide
TOPCon	Tunnel oxide passivating contacts
V_{OC}	Open-circuit voltage

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Introduction

1.1 Motivation

With the increasing population and the evolution of industries, energy demand is growing faster than ever before, which place human beings under the threat of energy crisis [1]. Problems also arise as the conventional energy sources like coal, oil and natural gas are being depleted because they cannot be refilled by nature itself. This situation addresses the importance of the transition of the energy consumption from fossil fuel based mode to a more renewable mode. Solar energy especially photovoltaic (PV) solar energy is now playing a more and more important role in the balance between energy supply and consumption. This is because photovoltaics based renewable energy has a huge source of solar irradiance which can theoretically provide energy of more than 10,000 times compared to the current energy demand [2]. More facts about the contributions of photovoltaics are shown in table 1.1, among which c-Si wafer based technologies are now having the largest market share (94%) and an outstanding lab cell efficiency of up to 26.7% [3]. The efficiency of the commercial wafer based silicon modules has increased from 12% to 17% for the last decade.

Table **1.1**: Summary of the development in photovoltaics. Table templated based on [4].

Parameter	Value	Status	References
PV market	77.3 GW	2016	IHS
Cumulative installation	320 GW	End of 2016	IHS
c-Si share of production	93%	2016	IHS
Record efficiency: mono-Si/multi-Si	26.7%/21.9%	July 2017	Green et al.

The photovoltaics market is very energetic and fast growing. The government policies, capital injection and the research progress contribute to a Compound Annual Growth Rate (CAGR) of 40% in PV installation between 2010 and 2016. With these support, the learning rate of the PV technologies is reported to be 24% according to data for the last 36 years [4].

However, to further promote the installation of PV modules, the lower price is preferred to attract more investment as well as to compete against the conventional energy, which can be achieved by further improving the conversion efficiency of the solar cells. Efforts can be made by reducing the bulk material cost or the semiconductor/metal interface recombination. According to the status of the photovoltaics reported in [4], the bulk silicon material cost is significantly reduced by either improving the production process or cutting down the wafer thickness to enable low-defect silicon wafers.

Hence, promising research topics can be focused on the technology of advanced passivated contacts to further cut down the surface recombination. One of the most successful passivation technique is the tunnel oxide passivated contact (TOPCon) technology. Fraunhofer ISE successfully fabricated front and back contacted (FBC) cells based on TOPCon structure on a n-type FZ wafer with a record efficiency of 25.8%, and the outstanding open circuit voltage of 724 mV shows high-quality surface passivation [5]. Institute for Solar Cell Research (ISFH) successfully fabricated IBC solar cells based on TOPCon structure on a p-type FZ wafer with a record efficiency of 26.1%, the very high fill factor of 84.2% shows very efficient carrier collection [6]. These research progress shows TOPCon structure is a strong candidate for high efficiency solar cells and it's worth of further investigation.

In this project, the polycrystalline silicon (poly-Si) layer is replaced by an oxygen alloyed polycrystalline (poly-SiO_x) layer in order to further improve the performance of the TOPCon structure. This addition oxygen alloy widens the bandgap of the contacts and consequently provides a larger band bending, which enables higher passivation on the c-Si surface. Besides, it improves the transparency of the passivating layer, and helps decrease the absorption losses. It is also proved to obtain higher thermal stability and still enable efficient charge carriers transport [7]. Therefore, the optimization of both the TOPCon structure and the experiment process will be beneficial for a higher-efficiency solar cell, which enables lower price of commercial PV modules as well as

speeding up of the transition of energy consumption mode.

1.2 Objective

The main objective of this master thesis is to fabricate front and back contacted high-efficiency solar cells with poly-SiO_x passivating contacts. This can be achieved by the optimization of the poly-SiO_x passivating contacts. The interaction among the material properties (oxygen content, doping level), the thermal budget and the hydrogen passivation process will be investigated. By setting the balance among these parameters, the optimized poly-SiO_x passivating contacts can be obtained, which can enable the fabrication of high-efficiency solar cells. The main research questions in this thesis are:

1. What is the influence of the PECVD deposition parameters on the passivation of poly-SiO_x CSPCs?
2. What is the influence of the high-temperature annealing on the passivation of poly-SiO_x CSPCs?
3. How can the hydrogenation process benefit the passivation of poly-SiO_x CSPCs?
4. what is the advantage of passivating contacts with poly-SiO_x films over the poly-Si films?

1.3 Outline

This thesis consists of 7 chapters, with a focus on the optimization of the passivating contacts and the fabrication of the solar cells. It is structured as follows:

In Chapter 2, basic knowledges about PV and the literature review focusing on the passivating contacts will be treated. This chapter aims to introduce the relevant fundamental physics theories as well as the development of the passivating contacts, which give the basic understanding of the research topic.

Detailed experiment processes are described in Chapter 3, which aims to clarify the basics flow of the experiment performed in this thesis work. Both the working principles and the supporting equipment are introduced.

Chapter 4 presents the characterization techniques that are used to determine the electrical and optical properties of the samples. The equipment or systems used in this work are introduced, and the working principle of each measurement is also treated.

Based on the study of basic theories and the experiment process, experiments can be conducted and the results can be analyzed correctly. Therefore, in Chapter 5 and 6 the experiment results will be presented and discussed in detail. Chapter 5 focus on the optimization of poly-SiO_x passivating contacts, and the influence of each deposition parameters on its passivation properties are. In Chapter 6 the poly-SiO_x passivating contacts will be applied into solar cells, and the device level discussions will be presented. Front and back contacted solar cells, double side flat or front side textured, are fabricated with the optimized poly-SiO_x passivating contacts presented in Chapter 5. Furthermore, in order to investigate the best way of applying this poly-SiO_x passivating contact, solar cells with different configurations are fabricated and compared.

After the detailed theory and experiment investigation, the conclusions of this thesis will be carried out in Chapter 7, which gives a summary of the work and the progress made so far. Besides, this chapter also shows an outlook on possible ways to improve solar cell performance in PVMD Group, which will be further investigated during the next research period.

2

Fundamental theory

In order to have a better understanding of the research topic, the fundamental theories are studied and present in this chapter. Firstly, the basics of the semiconductor will be introduced according to the books by A. Smets et al. [2] and Neamen [8]. Secondly, the mechanism of generation and recombination and the working principle of solar cells will be discussed. Then the concept of carrier-selective passivating contacts (CSPCs) is introduced, with the focus on the development of poly-Si (poly-SiO_x) passivating contacts. Finally, the tunneling and pinhole theory as well as the contact resistivity are explained.

2.1 Semiconductor physics

In this thesis, the basic semiconductor material is crystalline silicon (c-Si), with an atomic number of 14. Considering no impurity atoms contained in silicon lattice, the density of atoms is $5\times10^{22}\ cm^{-3}$, and such kind of silicon can be referred to an intrinsic semiconductor. Meanwhile, with different purpose, c-Si can also be doped into p-type and n-type materials with boron (B) and phosphorus (P), respectively.

The operation of a semiconductor device depends on the transport characteristic of the charge carrier transport, which cause the flow of electrons in certain direction and consequently produce electrical currents. One can determine the charge carrier concentration by the density of energy states function $g(E)$ and the occupation function named Fermi-Dirac distribution function $f(E)$. These two functions describe the number of allowed states per unit volume and the possibilities of these allowed states to be filled with an electron at given energy E, respectively. For a semiconductor,

there are discontinuous allowed energy states for electrons named energy bands, and the allowed energy states for valence electrons is called valence band. At T = 0 K, the valence band is fully filled with valence electrons, and the maximum energy state of it is noted as E_V. For T > 0 K, some charged electrons breaks away from its covalent bonding position and "jump" into the so-called conduction band. The minimum allowed energy state for these free electrons is noted as E_C. The valence band and the conduction band is separated by a forbidden energy band, and the energy difference between E_V and E_C is called the bandgap energy E_G. Based on the above-mentioned concept, $g_C(E)$ and $g_V(E)$ can be given by:

$$g_C(E) = 4\pi \left(\frac{2m_n^*}{h^2}\right)^{\frac{3}{2}} \sqrt{E - E_C} \tag{2.1a}$$

$$g_V(E) = 4\pi \left(\frac{2m_p^*}{h^2}\right)^{\frac{3}{2}} \sqrt{E - E_V} \tag{2.1b}$$

The Fermi-Dirac distribution function is defined as:

$$f(E) = \frac{1}{1+\exp\left(\frac{(E-E_F)}{k_B T}\right)} \tag{2.2}$$

The effective charge transport depends on the charge carrier concentration of the electrons in the conduction band and the holes in the valence band, which can be calculated with the following equations:

$$n(E) = g_C(E) f(E) \tag{2.3a}$$

$$p(E) = g_V(E)[1 - f(E)] \tag{2.3b}$$

There are two important transport mechanisms in a semiconductor device called drift and diffusion, which is driven by electrical and chemical potential, respectively. By simplifying the three-dimension transport into one-dimension analysis, one can calculate the drift current density with the following equations:

$$J_{n,drift} = q\mu_n nE \tag{2.4a}$$

$$J_{p,drift} = q\mu_p pE \tag{2.4b}$$

where μ is the charge carrier mobility, E is the electric field.

On the other hand, the diffusion current density can be determined by:

$$J_{n,diff} = qD_n \frac{dn}{dx} \tag{2.5a}$$

$$J_{n,diff} = -qD_p \frac{dp}{dx} \tag{2.5b}$$

where D is the diffusion coefficient.

Finally, the sum of the drift and diffusion current densities result in the total current

densities:

$$J = J_{drift} + J_{diff} = q(p\mu_p + n\mu_n)E + q(D_n \frac{dn}{dx} - D_p \frac{dp}{dx}) \quad (2.6)$$

The electric field is created by the different distribution and density of positive and negative charge carriers, which can be described by Poisson's equation if again one-dimension analysis is applied:

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\epsilon_s} = -\frac{dE(x)}{dx} \quad (2.7)$$

2.2 Generation and recombination – operation of solar cells

The normal operation of a solar cell requires the following three basic principles [9]:

1. An absorber made with semiconductor material to absorb incident photons and generate electron-hole pairs.
2. Selective regions which allow one type of charge carrier to pass through while suppress the transport of the other carrier.
3. Conductive contacts in the device terminals to collect generated electrons and holes separately as the electricity supply to the external load.

The first principle deals with the generation process. If a solar cell is illuminated by a light source which provide photons with energy equal or larger than bandgap energy, the electrons in the valence band can be excited to the conduction band. Meanwhile the vacancies are created in the valence band, which is called holes. If an electron is exited beyond the edge of the conduction band, it will release its excess energy in the forms of lattice vibration. Then the so-called thermal relaxation process happens which converts the energy into heat and consequently this electron falls down to the edge of the conduction band. This electron will then remain in this energy level for a certain time before it recombines with a hole.

The second principle addresses the importance of the carrier selective regions. In a c-Si solar cell these regions are achieved by introducing an emitter and a surface field, which form a p-n junction and a high-low junction with the absorber, respectively.

The last principle tells that two different terminals are needed as the electrons and holes collector, which can continuously transfer these charge carriers to create external

electrical current. In c-Si, metal such as aluminum (Al), sliver (Ag), copper (Cu) can be applied as the carrier collectors.

To further explain the operation of solar cells, one can consider a n-type c-Si wafer as the substrate, usually a heavily doped p-type region is deposited on the front side as its front emitter, while for the rear side a heavily doped n-type region is applied as its back-surface field (BSF). As a result, the photon-generated electrons are collected at BSF while holes at emitter. A photo-generated current (I_L) is formed during this kind of drift flow, while on the other hand, a diffusion current named dark current (I_{Dark}) in opposite direction is also flowing. These two currents result in the current characteristic of a c-Si solar cell under illumination:

$$I(V) = I_{Dark} - I_L = I_0 \left(e^{\frac{qV}{nkT}} - 1\right) - I_L \tag{2.8}$$

where I_0 is the saturation current, n is the ideality factor, k is the Boltzmann constant, T is the temperature. For the characterization of solar cells, a positive current density characteristic is preferred:

$$J(V) = J_L - J_0 \left(e^{\frac{qV}{nkT}} - 1\right) \tag{2.9}$$

Important external parameters can be derived based on equation (2.9), which will be addressed in chapter 4.

However, the inevitable recombination of electrons and holes can undermine the performance of solar cells. For different semiconductor materials, the recombination mechanism can be different, which can be divided into two main mechanisms: bulk recombination and surface recombination. The bulk recombination consists of radiative recombination, Auger recombination and Shockley-Read-Hall (SRH) recombination.

- ***Direct recombination***

For the direct bandgap materials like gallium arsenide (GaAs), the radiative recombination dominants. During this recombination process, an electron directly falls down to the valence band and recombines with a hole, resulting in the transfer of energy and the emission of a photon.

- ***Auger recombination***

For the indirect bandgap materials like crystalline silicon (c-Si), the Auger recombination dominants. Auger recombination is a third particle process, which indicates that except the recombining electron-hole pairs, another electron or hole is

present during this mechanism. Therefore, the Auger recombination includes electron-hole-hole (ehh) and electron-electron-hole (eeh) process, and it is strongly dependent on the charge carrier density. It should be noted that Auger recombination limits the maximum theoretical efficiency of c-Si solar cells to 29.43% [10].

- ***Shockley-Read-Hall (SRH) recombination***

The SRH recombination becomes significant when there are defects or material impurity in the semiconductor. During this recombination process, an extra energy level in the c-Si bandgap is created due to the defects in the material. This energy level stays closer to middle of the bandgap, and it acts like a stepping stone to help electron falls down into the valence band.

- ***Surface recombination***

With the progress made by the silicon manufacturers, the bulk recombination is suppressed under a low level, making surface recombination become the dominant recombination mechanism for most of the current c-Si solar cells. As is shown in figured 2.1, dangling bonds exist on the material surface and increase the defect density, which induces the SRH recombination. The recombination rate can be expressed using the following equation:

$$R_s \approx v_{th}\sigma_p N_{sT}(p_s - p_0) \tag{2.1}$$

Where,

v_{th} is the thermal velocity, [cm/s].

σ_p is the capture cross section, [cm^2].

N_{sT} is the trap density at the surface, [cm^{-2}].

p_s, p_0 are hole concentration at the surface and at equilibrium, respectively.

Here, surface recombination velocity is defined as:

$$S_r = v_{th}\sigma N_{sT} \tag{2.2}$$

Based on the above equations, there are several paths to further minimize the surface recombination: The first option is to cut down the surface recombination velocity. This can be achieved by passivating the dangling bonds with for example hydrogen to reduce the trap density. On the other hand, the excess minority carrier density can be reduced by increasing the doping concentration near the material surface, which in a way creates a barrier to suppress the transport of minority carriers to the surface.

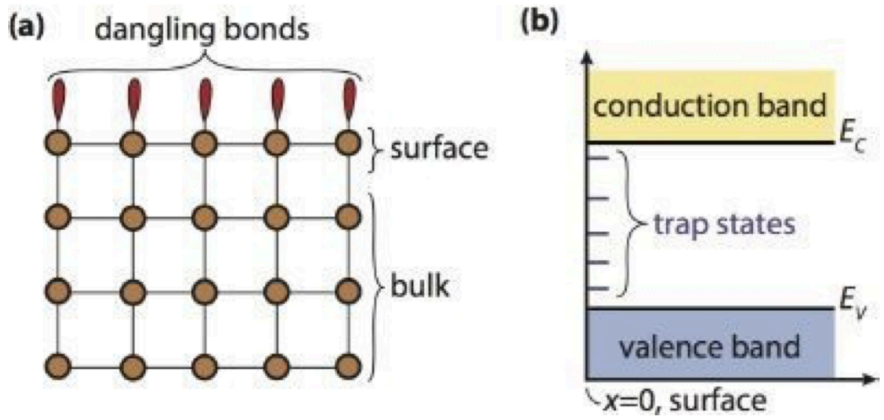


Figure **2.1**: Illustration of the surface recombination: (a) Dangling bonds present on the material surface. (b) trap states within the bandgap created by dangling bonds. Picture adapted from [2].

2.3 Passivating and carrier selective contacts

For classical homo-junction solar cells, field effect passivation is usually applied to suppress the recombination mechanism, where a dielectric with charge or a highly doped layer is applied on top of the bulk silicon material [11]. This layer acts as a very high barrier at the surface of the silicon against the minority charge carrier. As a result, the minority charge carrier is blocked while the majority carrier is attracted. This effect is enhanced when a higher doping concentration is applied. However, the passivation quality will also be undermined if the doping concentration reach a too high level ($N_{D,n^+} \geq 10^{18}\ cm^{-3}$), where the bandgap narrowing is significant and the Auger recombination becomes dominant [12]. Homo-junction also comes across an efficiency loss due to the recombination at the interface of semiconductor and metal. To overcome these limitations, the semiconductor and metal interface is passivated, and the passivated emitter and rear cell (PERC) concept and the light management technology have driven the homo-junction cells to attain higher efficiency [13-15]. However, these also makes the fabrication much more complicated.

Hence, in order to overcome the limitations of homo-junction solar cells, several concepts and technologies are implemented to fabricate high-efficiency solar cells. One competitive alternative is the so-called heterojunction with intrinsic thin layer technology (HIT), which introduces the intrinsic and doped hydrogenated amorphous silicon layer (a-Si:H) as the passivated contact to form a heterojunction with the bulk

c-Si layer [16]. This very thin intrinsic a-Si:H layer significantly reduces the interface defect, which benefits solar cells fabrication with an excellent passivation and consequently high efficiency [17]. However, this thin (typically 10 nm) amorphous layer is responsible for inferior blue spectrum response of SHJ solar cells, it is reported that the transparent conductive oxide (TCO)/a-Si:H contact suffers from the parasitic absorption [18]. Furthermore, it is measured that the short-circuit current density loss can be as high as 1.0-1.5 mA/cm^2 per 10 nm a-Si:H [19]. To overcome such significant parasitic absorption, IBC configuration is combined with HIT technology. Kaneka company successfully fabricated silicon heterojunction-interdigitated back contact (SHJ-IBC) solar cell with a record efficiency of 26.7% [5]. However, the fabrication of such cell seems too complex to be applied into industry. Another drawback of this passivation technology is that the i-Si:H layer is sensitive to high temperature processes (maximum ~250℃), which limits the back-end processes like TCO deposition and the metallization afterwards [20].

Therefore, to overcome these restrictions on high-efficiency solar cells, current research is also focus on the polycrystalline silicon (poly-Si) passivated contacts, which show several advantages compared with HIT technology. For example, solar cells based on poly-Si contacts can have lower parasitic absorption as well as higher stability during high temperature process. High thermal stability is preferred in solar cell fabrication because the standard back-end process such as TCO deposition and the metallization for homo-junction solar cells is well-designed at relatively high temperature. Hence passivating contacts are thought to be a promising technology to improve the solar cell performance. The first successful passivating contacts that significantly improved the solar cell efficiency is called tunnel oxide passivated contact (TOPCon), which is introduced by Feldman et al [21]. A drawing of such configuration is shown in figure 2.2, which consists of an ultra-thin tunnel oxide layer and a highly doped polycrystalline silicon (poly-Si) layer on top. After the poly-Si layer deposition, this configuration receives a high temperature anneal at around 800 to 1000 ℃ for the crystallization as well as the dopant drive-in process [22]. This concept has shown excellent passivation with implied V_{OC} of 733 mV, J_0 of 4.5 fA/cm^2 [23] and V_{OC} of 716 mV, J_0 of 11 fA/cm^2 [24] for n-type and p-type TOPCon, respectively. In the next section, development of this novel configuration will be treated in detail.

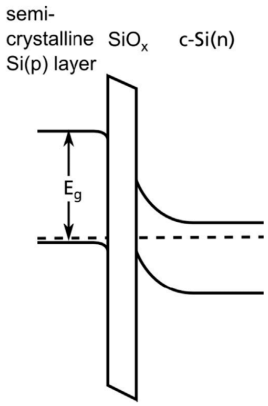


Figure **2.2**: Band diagram of the tunnel oxide passivating contact. Adapted from [25].

2.4 Development of poly-Si/poly-SiO_x passivating contacts

Research of passivating contacts based on TOPCon have been done by many groups, which made great contributions to the development of this novel concept. In this section, a brief summary is given focusing on the excellent results obtained so far in this field.

Eli Yablonovitch et al. successfully fabricated the n^+ - semi-insulating polysilicon (SIPOS):p-Si heterojunction emitters with a saturation current of 10 fA/cm^2 [26]. They further investigated this promising configuration in solar cell level, and calimed good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells, which gave an excellent open-circuit voltage of 720 mV [27].

Udo Römer et al. [28] from ISFH studied the influence of the tunnel oxide on the electrical characteristics of the poly-Si and c-Si junctions. Both thermally and chemically grown oxide are investigated and a low recombination current densities <20 fA/cm^2 was achieved together with a low specific contact resistance $<0.1\Omega \cdot cm^2$.

Yuguo Tao et al. optimized the PECVD grown poly-Si passivating contact, and successfully obtained an implied V_{OC} of 730 mV and a saturation current of 4.3 fA/cm^2 [29].

Excellent solar cells based on n-TOPCon structure on the rear side are successfully fabricated by Fraunhofer ISE, which obtains a record efficiency of 25.8% for double side contacted solar cells [30]. A schematic of the solar cell configuration is shown in figure 2.2.

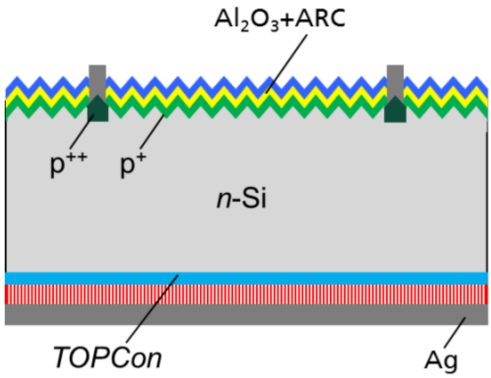


Figure **2.3**: Schematic of solar cell with tunnel oxide passivated emitter and BSF. Picture adapted from [31].

With this TOPCon configuration based on poly-Si as the rear contact, excellent passivation is enabled for the rear side, and the front contact becomes the efficiency-limited element. Hence, in order to further increase the efficiency, passivating contact is also applied on the front side. Frank Feldmann et al. [23] investigated solar cells with poly-Si passivating contacts on top and rear sides on a p-type wafer. Based on the optimization of the TOPCon thickness, the ion-implantation dose and the doping level, a very low saturation current density of 4.5 fA/cm^2 for n-poly contacts and 22.5 fA/cm^2 for p-poly contacts are obtained. These optimized layers enable double side polished solar cells with V_{OC} up to 709 mV and FF higher than 81% [32].

To further improve the efficiency of the solar cells, an option is to implement the IBC configuration. Photovoltaic Material and Devices (PVMD) group from Delft University of Technology applied the poly-Si passivated contacts to the interdigitated back contact concept, an IBC solar cell on a n-type wafer with efficiency of 23.0% and a V_{OC} of 701 mV was successfully fabricated [33]. While for a p-type c-Si material, ISFH successfully fabricated a record IBC solar cell with an efficiency of 26.1%. This cell uses poly-Si passivating contact for both n^+ and p^+ contacts, which results in a very high V_{OC} of 726.6 mV, an excellent fill factor of 84.28% [34].

On the other hand, for a front and back contact cell with top and rear passivating contacts, while ensuring the passivation behavior and the electrical transport, one needs to make the front layer more transparent to prevent or cut down the losses from parasitic absorption. One option is to deposit a thinner and fully crystallized poly-Si layer with a longer annealing process [35]. However, this can cause detrimental damage to the tunneling oxide layer, which significantly undermines the passivation behavior [36, 37].

As an alternative, thicker tunnel oxide layer can be used. However, this thicker layer needs higher thermal budget (above 1050 ℃) [23] for the tunnel oxide break up process [28], which can cause over diffusion of the dopant into the bulk Si material, and consequently degrade the passivation quality. It is also claimed that for a phosphorous doped poly-Si layer, the absorption losses is about 0.5 mA/cm^2 with every 10 nm thick poly-Si stack deposited [23], and the so-called free carrier absorption becomes significant for a poly-Si layer at the wavelength above 1200 nm [38].

To overcome the above-mentioned problem, Josua Stuckelberger et al. used a moderate thermal annealing process (700-900℃) for solar cell fabrication, and still enable an almost fully crystallized layer [7]. In order to decrease the optical losses, they also introduced an additional SiO_x phase into the poly-Si passivating contacts, which can further decrease the optical losses by tuning the refractive index [39]. This novel passivating contact presented is based on the early research on semi-insulating polycrystalline silicon (SIPOS) by Y. H. Kwark et al. [40], P. Brüesch et al. [41] and Y. Pan et al. [42]. They studied the structure and electrical properties as well as electrical conductivity with different oxygen content, which shows the possibility to apply SiO_x films into solar cell fabrication. The mixed-phase passivating contact presents a low saturation current of 8.1 fA/cm^2 after thermal annealing and hydrogenation. With the mixed-phase passivating front surface field (FSF), the proof of concept solar cells fabricated (Figure 2.3) shows an FF of 79.4%, a J_{SC} of 33.9 mA/cm^2) and a V_{OC} of 691 mV [43].

The excellent results gained so far prove that TOPCon configuration can achieve not only very good and reproducible passivation, but also a very efficient carrier transport. As a result, high-efficiency solar cells can be obtained.

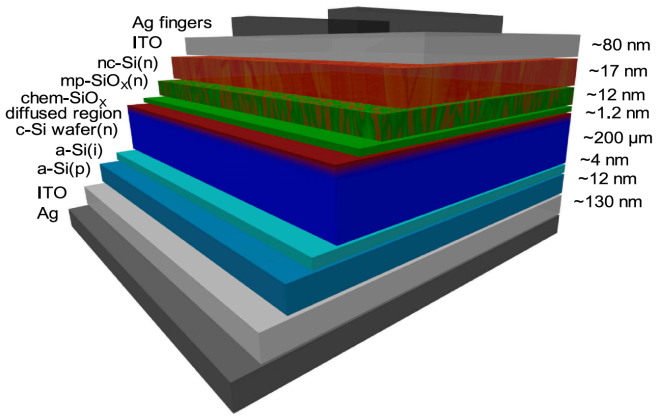


Figure **2.4**: Schematic of the proof of concept cell. Adapted from [43].

2.5 Oxide tunneling

To have better understanding of the working principles of the tunnel oxide passivating contacts, the oxide tunneling theory is introduced in this section. According to the investigation by ISFH [44], although the heavily doped poly-Si layers provide field effect passivation on the c-Si surface, a very high saturation current density J_0 was found without the presence of the untra-thin silicon oxide layer. Hence, this silicon oxide layer also contributes to the extremely low J_0 by preventing the minority charge carrier from being extracted into the poly-Si layer, while the majority charge carrier can tunnel through the ultra-thin oxide layer. As is shown in figure 2.2, there is a band-offset difference between c-Si bulk and the oxide layer (3.2 eV for conduction band, 4.7 eV for valence band), which is known from internal photoemission spectroscopy [45]. The difference in band offset in conduction band and valence band explains the difference in J_0 as the effectiveness of allowing the tunneling of majority charge carriers while hindering the tunneling of minority charge carriers are different. By assuming tunneling phenomenon as the dominant current transport mechanism, the relation of the tunneling probability between electrons and holes can be extracted based on the study of Neamen [8] and Peibst [44], which is shown in equation (2.12):

$$\frac{T_e}{T_h} \propto \frac{exp\left(-d_{ox}\sqrt{\frac{2m_{t,e}}{\hbar^2}\phi_e}\right)}{exp\left(-d_{ox}\sqrt{\frac{2m_{t,h}}{\hbar^2}\phi_h}\right)} \tag{2.12}$$

where, d_{ox} denotes the thickness of the oxide layer, $m_{t,e}$ ($m_{t,h}$) and ϕ_e (ϕ_h) denote the effective tunneling mass and barrier height for electrons (holes), respectively.

2.6 Contact resistance

It is important to characterize the contacts of semiconductor devices like solar cell, and the contact resistance is one of the important parameters that tells whether the metal and the semiconductor have good contact. The metal-semiconductor contacts are very important in solar devices as it connect the solar cells to the external electric circuit [2], which can be distinguished between rectifying contact and ohmic contact. Rectifying contact is also referred as Schottky contacts, which indicates a large contact barrier

(high contact resistance) between metal and semiconductor. Under this condition, the transport of the majority carriers is dominant in the current transport. This can cause a significant reduce of voltage, which is not preferred for a good semiconductor device. On the other hand, when the contact resistance between metal and semiconductor is negligible compared with the bulk semiconductor resistance, the ohmic contact is formed. Ohmic contact have linear or quasi-linear current-voltage characteristics. This contact is preferred in semiconductor devices as it causes nearly zero voltage drop and enable good device performance [2].

3

Processing techniques

In this chapter, the fundamental process techniques included in the experiment part are introduced. The aim as well as the principle of each process are discussed and analyzed in detail. This chapter is structured in the order of occurrence during the fabrication of the samples in this thesis.

3.1 Basic cleaning

The type of wafer used during this project is the high-quality Float-Zone (FZ) c-Si wafer (thickness: 280 $\pm$ 20 μm , orientation: <100>, resistivity: 1-5 Ω cm) manufactured by SIEGERT. The first step is to clean the wafer following a standard cleaning process in PVMD lab environment.

The wafers are first immersed into a 99% HNO_3 solution for 10 minutes to remove the organic contaminations, and then the wafers are rinsed in deionized water (DI water) for 5 minutes. The inorganic contaminations are removed in a 68% HNO_3 solution at 110℃ for 10 minutes, again followed by a 5 minutes DI water rinse. During the above two processes a native oxide layer is formed on the wafer surface, which can be removed by a 4-minute dip in Hydrofluoric acid (HF) at the concentration of 0.55%. it is important to have a HF dip right before the next process, which diminish the re-contaminations or the re-oxidation of the wafers.

The basic cleaning process described above results in a clean and nearly pure c-Si bulk material, which is crucial for the tunnel oxide growth described in section 3.2.

3.2 Chemical silicon oxide growth

The ultra-thin SiO_2 layer in this thesis is grown with the method of Nitric Acid

Oxidation of Silicon (NAOS) [46], which is called chemical oxide. The clean wafers are immersed into the 69.5% HNO_3 solution at room temperature for 60 min, the thickness of the thin chemical tunnel oxide layer obtained is about 1.5 nm [47, 48]. The advantage of the chemically grown oxide is that it attains much more homogeneous layer structure and lower leakage current. Besides, wet growth oxide requests less thermal budget compared with the thermally grown oxide which is normally grown at the temperature of 600 to 700℃. However, it is of relatively lower thermal stability, which affects the later high-temperature anneal process.

3.3 Intrinsic amorphous silicon layer growth with LPCVD

For the poly-Si layer deposition, the wafers are placed in the tube furnace (temperature of 580℃; SiH_4 gas flow of 45 sccm; pressure of 150 mTorr; deposition rate 2 nm/min) to receive a low pressure chemical vapor deposition (LPCVD) process. A LPCVD process helps to form a uniform and pinhole free layers, which provide good protection of the tunnel oxide against the following treatment [49]. As a result, a hydrogenated amorphous silicon (a-Si:H) layer with specific thickness is deposited on both side of the wafers. After the deposition of the intrinsic amorphous silicon layer, an annealing step at 600℃ for 1 hour is used to release the stress.

It should be noted that after the deposition of this a-Si:H layer, the sample should have a 0.55% HF dip right before it goes into the next step. This is because the native oxide can be formed very quickly on the amorphous silicon surface, which can create defects and damage the interface passivation.

3.4 Intrinsic or doped amorphous silicon oxide layer growth with PECVD

Plasma Enhanced Chemical Vapor Deposition (PECVD) is used for the growth of thin-film silicon materials such as amorphous silicon, nanocrystalline silicon, silicon carbide and silicon oxide. During the process, the thin-film materials are made intrinsic, n-doped or p-doped [2]. Note that PECVD only allows low temperature deposition (below 200℃). With the optimized parameters, the PECVD layers can be formed with high

quality, desirable thickness as well as very good uniformity.

The basic setup of a PECVD machine is shown in figure 3.1. Normally, a mixture of different gases such as silane (SiH_4), carbon dioxide (CO_2), hydrogen (H2), phosphine (PH3) and diborane (B_2H_6) are supplied based on the desired flow rate into an ultrahigh vacuum (UHV) reaction chamber. With the effect of plasma in the chamber, several reactions happen which generates the desired reactive radicals, ions, neutral atoms, molecules and electrons. The substrate is then formed with the thin-film layer with the plasma and generated particles.

Key parameters such as the chamber temperature, chamber pressure as well as the gas flow rate, and the composition of the mixture gases should be optimized to ensure a high quality deposited layer. Hence, PECVD is a very important and sensitive process, which significantly influences the passivation quality.

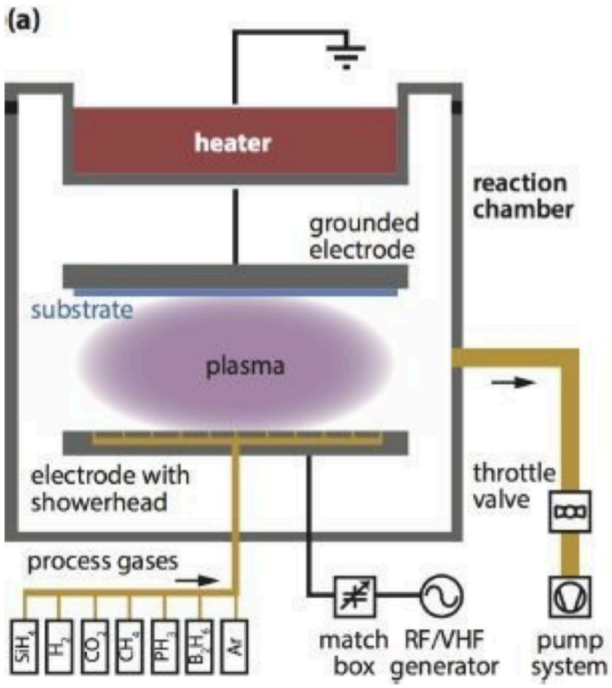


Figure **3.1**: Illustration of plasma enhanced chemical vapor deposition, picture adapted form [19].

3.5 High-temperature annealing

After the deposition of the thin heavily doped hydrogenated amorphous silicon oxide (a-SiO_x:H) layer, the wafers are placed in the Tempress tube furnace to receive a high-temperature annealing at pure N_2 atmosphere at a very high temperature (above 850°C).

During this high-temperature treatment, multiple goals can be achieved: First the top layer which is deposited with a-SiO_x:H is crystallized, resulting in the transformation into a poly-SiO_x layer.

High-temperature annealing also increase the diffusion of the dopants. In most case, it helps activate and drive-in the dopant atoms which are deposited during PECVD process. However, some boron in the doped poly-SiO_x layer will diffuse into the bulk material through the oxide layer, which causes inferior passivation. Hence the annealing parameters should be optimized to have a very good dopant profile at the interface of bulk material and the tunnel oxide, which will result in excellent passivation.

This high-temperature annealing also affects the chemical tunnel oxide layer. The thermal budget may affect the integrity of the tunnel oxide layer and destroy this diffusion barrier, which needs certain attention.

3.6 Hydrogenation

To fabricate high-efficient solar cells, it is of great significance to suppress the surface recombination, and for poly-Si and poly-SiO_x based solar cells, hydrogenation is proved to be an important treatment to passivate the defects [50].

As is shown in section 2.2, the important recombination mechanisms are bulk recombination as well as surface recombination. As is shown in figure 2.1 (a), at a silicon surface, there are many valence electrons on the surface which cannot combine with other atoms to form a covalent bond, resulting in the existence of a defect called dangling bond. These dangling bonds create many trap states within the bandgap of the silicon as is shown in figure 2.1 (b), resulting in a higher recombination and undermine the surface passivation [2].

During the forming gas anneal, three major reactions are identified, namely reflection, Eley-Rideal H_2 abstraction and adsorption. The high adsorption of hydrogen (60%) provides sufficient H atoms for surface passivation, which also closes the voids created by the H_2 abstraction on the silicon surface [51]. Different schemes of hydrogen passivation such as remote plasma hydrogen passivation [37, 52], forming gas anneal [24, 43], and hydrogenation by capping with PECVD deposited silicon nitride (SiN_x) [49] or by atomic layer deposition (ALD) aluminum oxide (Al_2O_3) [53].

3.7 TCO layer (ITO) deposition

The poly-SiO_x layer deposited in this thesis has relatively low conductivity compared with poly-Si, i.e. the charge carriers transport can be inefficient at the poly-SiO_x and metal interface. Hence, a transparent conductive oxide (TCO) layer is introduced, which acts as electric contact for the operation of solar cells. Furthermore, it can also act as the anti-reflection coating (ARC) layer for the better light capping. Hence, this layer should be both highly conductive (high mobility) and highly transparent (suitable refraction index) in the active wavelength range.

Typical TCO layers are made from fluor-doped tin oxide (SnO_2:F), aluminium-doped zinc oxide (ZnO:Al), boron-doped zinc oxide (ZnO:B), hydrogen-doped (hydrogenated) indium oxide (In_2O_3:H) [2]. The TCO material used in this thesis is indium tin oxide (ITO), which consists of 90% indium oxide (In_2O_3) and 10% tin oxide (SnO_2). It is deposited with one of the physical vapor deposition (PVD) method called sputtering, which results in a layer with high carrier mobility and suitable work function to contact the semiconductor layer as well as metal layer without introducing too much damage. It should be noticed that during the deposition of the ITO layer, the as deposited layer can be undermined by the sputtering damage.

The deposition of the ITO layers will result in a target thickness of round 75 nm on the front side and around 120 nm on the rear side, which are suitable for both the carrier transport and the light capping.

3.8 Metallization

For the deposition of the metal layer, well-developed techniques such as metal evaporation with a photolithography are applied, which will be introduced in this section.

Photolithography is also called optical lithography or UV lithography, which is used for growing a layer with certain pattern on top of the wafer. It uses the so-called photoresist to pattern the surface, and the certain type of developer to remove the photoresist. A positive photoresist can become more sensitive to the developer after it is exposed under the UV light, which can become easier to be removed by the developer.

On the other hand, a negative photoresist can become less sensitive to the developer after the exposure of UV light. In the fabrication of the solar cells in this project, the photolithography is used for the deposition of metal layer.

For the deposition of the metal layer, the metal evaporation technique is used. Generally, it applies whether resistive evaporation or electron beam evaporation to heat the source material over its melting point. Then the evaporated material will uniformly fill the deposition chamber, which will consequently condensate on the surface of the substrate [2]. Metal evaporation is a very high-level vacuum process, which means that it can well control the deposition thickness and the oxidation of the material [54]. In PVMD group, the evaporation process is done in the Provac evaporation machine, which is installed with a rotating holder to ensure the uniformity of the deposition layer.

To pattern the metal layer of the solar cells in this thesis, a thick positive photoresist is used to cover the surface of the wafer. this process consists of the spin coating of photoresist and a baking process at the temperature of around 100℃. This process is done for three times on one wafer to ensure a thick and uniform photoresist layer, which makes it possible to deposit a well patterned and thick metal layer. Then the wafer is exposure under the UV light with the coverage of a pattern mask. The exposure time can be different depending on the thickness of the photoresist layer and the type of the photoresist. After that, the sensitive photoresist is removed by the developer and a proper cleaning process is done for the preparation of the following deposition. Then the metal evaporation is done to have a fully deposited metal layer on the surface of the substrate, which is followed by a metal lift-of process with acetone to remove the unwanted metal region grown on the top of the insensitive photoresist layer. Finally, the metal patterning is ended with a proper cleaning in DI-water and drying. For the metallization of the rear side, metal is directly evaporated on top of the substrate with a hard mask, which results in a full area rear contact. This metal patterning process enables high-efficiency solar cells fabrication [24, 47, 55, 56].

4

Characterization techniques

In this chapter, the characterization techniques used for the performance test of the sample are introduced. The working principle as well as the background physics knowledge supporting these measurement methods are discussed and analyzed in detail. Section 4.1 deals with the Quasi-steady-state photo conductance technique for the passivation test. Spectroscopic ellipsometry technique is treated in section 4.2. In section 4.3 the transfer length method is introduced with basic knowledge of contact resistance. Then the measurement of the most important external parameters of solar cells are treated in section 4.4, which is followed by the EQE and the Reflectance/Transmittance measurement in the last two sections.

4.1 Quasi-steady-state photo conductance

Quasi-steady-state photo conductance (QSSPC) technique is a non-destructive and contactless method for measuring the samples and providing important information like effective lifetime, saturation current and implied V_{OC}. As is shown in figure 4.1, the measurement system used in PVMD Group is the Sinton WCT-120 lifetime Tester, which consists of a regular flash lamp (time decay of 2.3 ms and an irradiance up to 1,000 suns) and a coil. With the help of this technique, the samples can be measured during the fabrication to follow up the passivation quality of each process.

To measure the conductivity, the wafer is placed on a coil platform, and the regular flash lamp is installed right above the platform. When the lamp provides a light flash on the wafer, excess charge carriers can be generated and then a photocurrent J_{ph} can be measured as is shown in the following equation:

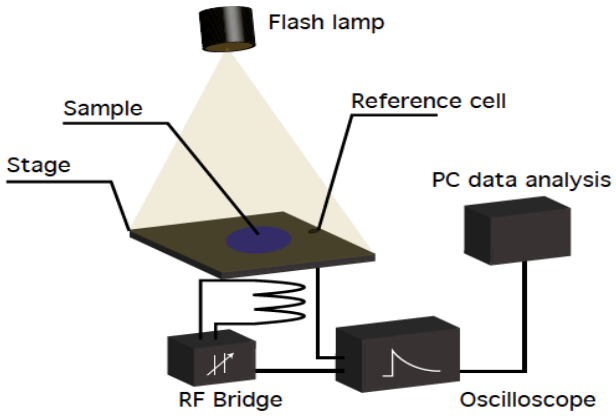


Figure **4.1**: Measurement setup of QSSPC technique. Adapted from [57]

$$J_{ph} = \frac{\Delta n_{av} q W}{\tau_{eff}} \tag{4.1}$$

Where:

Δn_{av} – The average excess minority carrier density;

W – The wafer thickness;

τ_{eff} – The effective minority carrier lifetime.

The excess photo-conductance can be derived as equation (4.2):

$$\sigma_L = q\Delta n_{av}(\mu_n + \mu_p)W \tag{4.2}$$

Where μ_n and μ_p are the mobility of electrons and holes, respectively.

By combining equation (4.1) and (4.2), the effective minority carrier lifetime can be determined by equation (4.3):

$$\tau_{eff} = \frac{\sigma_L}{J_{ph}(\mu_n + \mu_p)} \tag{4.3}$$

Quasi-steady-state(QSS) mode is used for the measurement of the samples with a lifetime less than $100\mu s$. This effective lifetime can be expressed as equation (4.4):

$$\tau_{eff} = \frac{\Delta n_{av}}{G - \frac{\partial \Delta n_{av}}{\partial t}} \tag{4.4}$$

Where, G is the generation rate of the carrier. When the lifetime of the sample is larger than $100\mu s$, steady-state and transient mode are used based on the assumptions that $\frac{\partial \Delta n_{av}}{\partial t} \approx 0$ and $G \approx 0$, respevtively.

For the calculation of the photocurrent, this measurement system uses a calibrated solar cell to measure the incident irradiance, and the software needs information of the sample such as wafer thickness, doping type of the bulk silicon, material

resistivity and the optical constant as the input.

The effective minority carrier lifetime is related to the bulk recombination and the surface recombination, which can be described using equation (4.5):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} = \frac{1}{\tau_{radiative}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{4.5}$$

Based on the effective lifetime measured, the implied open-circuit voltage of a p-type wafer can therefore be determined by equation (4.6)

$$iV_{oc} = \frac{kT}{q} \ln\left(\frac{\Delta n(N_A+\Delta p)}{n_i^2} + 1\right) \tag{4.6}$$

Where N_A is the doping density, Δn and Δp is the electron and hole density generated during the illumination, respectively.

The saturation current can also be determined based on the QSSPC data with the following equation [58]:

$$J_0 = S\frac{qn_{i,eff}^2}{N_A+\Delta n} \tag{4.7}$$

Where S is the effective surface recombination velocity (SRV), and Δp is the injection density. Taking the influence of the injection level on the SRH recombination, this method is further improved and J_0 can be more accurately determined with [59]:

$$J_0 = \frac{qW}{2}\left(\frac{d}{d\Delta n_{av}}\right)\left(\frac{n_{i,eff}^2}{\tau_s - \left(\frac{W}{D\pi^2}\right)}\right) \tag{4.8}$$

4.2 Spectroscopic ellipsometry

Spectroscopic ellipsometry (SE) is used to determine the thickness and the optical properties of the layer deposited on the substrate. The measurement setup in PVMD group is shown in figure 4.2. In this setup, the light source is equally parallel and perpendicular polarized, and then the light passes through the sample (glass or wafer) placed on the stage. According to the material properties of the samples, the polarization will be changed either in phase or intensity, which can be detected and analyzed with the setup.

The parallel and perpendicular polarization can be described by the Fresnel reflection coefficients, which is given with the following equations [60]:

$$r_p = \frac{N_s cos\theta_i - n_a cos\theta_t}{N_s cos\theta_i + n_a cos\theta_t} \tag{4.9}$$

$$r_s = \frac{n_a cos\theta_i - N_s cos\theta_t}{n_a cos\theta_i + N_s cos\theta_t} \tag{4.10}$$

This measurement will give two wavelength dependent parameters, which is the ratio of the reflected and incident field magnitudes ψ, and the phase change value Δ. These two parameters can be related to the Fresnel reflection coefficients with the following equation:

$$tan\,\psi e^{\Delta} = \frac{r_p}{r_s} = \rho \tag{4.11}$$

After the measurement, one should properly select a mathematical model for the analysis of the layer properties, which means $\boldsymbol{\psi}$ and Δ should be fitted very well to attain a accurate value of the layer thickness.

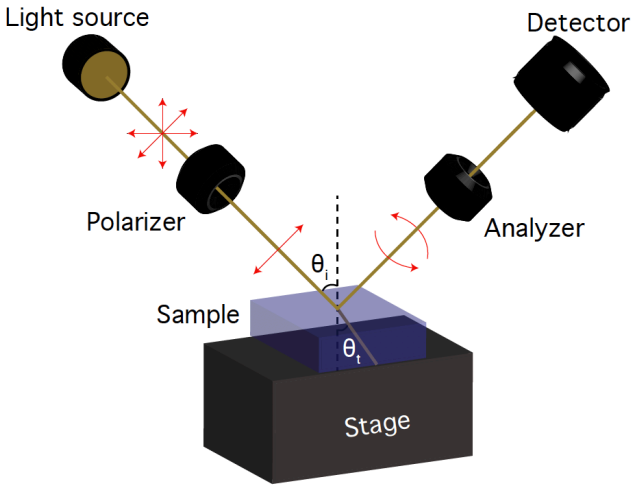


Figure **4.2**: Measurement setup of SE technique. Adapted from [57].

In this thesis, this setup is mainly used for determining the deposition rate of the PECVD a-SiO_x:H layer. A PECVD a-SIO_X:H layer is deposited on a glass substrate for 5min, and the layer thickness is measured with SE. Then the deposition rate of this layer can be calculated, which enable the deposition of a specific layer thickness.

4.3 Transfer length method/Circular transfer length method

The specific contact resistance is a very important parameter that describes the

properties of the metal-semiconductor contact, which is normally obtained by transfer length method (TLM) or circular transfer length method (CTLM) [61, 62].In this thesis, metal is contacted with a highly-doped poly-SiO_x layer, that means quantum-mechanic tunneling of the charge carriers through the barrier is the dominant transport mechanism, and the specific contact resistance is roughly defined using the following expression [63]:

$$R_C \propto \exp\left(\frac{1}{\sqrt{N_D}\hbar}\right) \tag{4.12}$$

It is understood from equation (4.8) that to cut down the specific contact resistance, a highly-doped region close to the metal-semiconductor contact is preferred.

Figure 4.3 shows the schematic diagram indicating the relationship between the contact resistance and the total resistance. As is indicated in the diagram, the total resistance measured consists of metal consistence, contact resistance and the semiconductor resistance, which can be expressed using the following equation:

$$\mathrm{R_T} = 2R_m + 2R_C + R_{Semi} \tag{4.13}$$

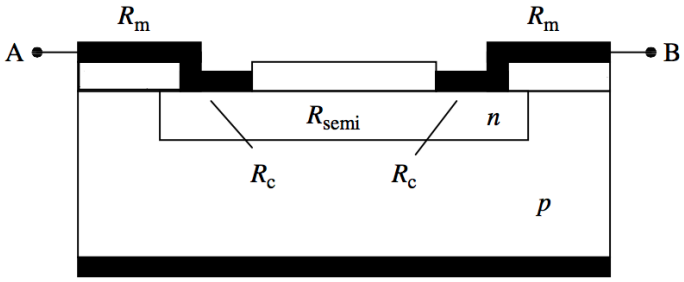


Figure **4.3**: Schematic diagram of the measurement between point A and B of the semiconductor device. Picture adapted from [63].

The resistance of the metal is negligible, which simplifies equation (4.13) into:

$$\mathrm{R_T} = 2R_C + R_{Semi} \tag{4.14}$$

In this project, the circular transfer length method (CTLM) is used for the characterization, and a simple structure designed for the measurement is shown in figure 4.4.

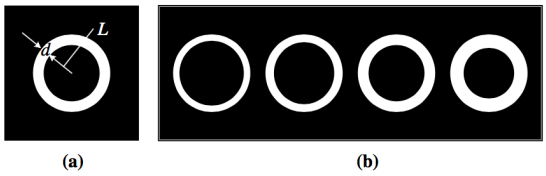


Figure **4.4**: Structure of the CTLM. Picture adapted from [63].

Here the transfer length is defined as the following equation:

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{4.15}$$

Where ρ_c is the contact resistivity with a unit of $\Omega \cdot cm^2$ and R_{sh} is the sheet resistance.

In CTLM, the total resistance measured can be expressed as [63]:

$$\mathrm{R_T} = \frac{R_{sh}}{2\pi L}(d + 2L_T)C \tag{4.16}$$

where C denotes the correction factor:

$$C = \frac{L}{d}\ln\left(1 + \frac{d}{L}\right) \tag{4.17}$$

If d ≪ L, the correction factor can be almost equal to 1, and equation (4.16) can be simplified as:

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T) \tag{4.18}$$

Then the measurement result can be plotted as shown in figure 4.5, which $\mathrm{R_T}$ is plotted as y-axis value, d is for x-axis value. With this plot, the transfer length is determined first, and then the contact resistance is found afterwards.

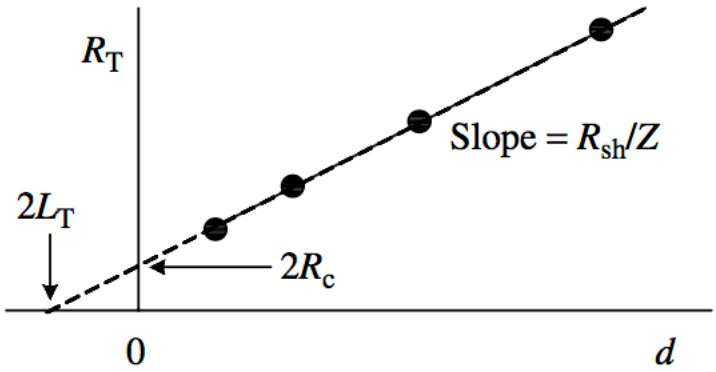


Figure **4.5**: Example of a simplified CTLM plot. Picture adapted from [63].

4.4 Illuminated J-V measurement

The most important external parameters used to characterize the solar cells are the short current density J_{SC}, the open circuit voltage V_{OC}, the fill factor FF and the solar cell efficiency η [2]. These parameters can be obtained using the illuminated current density-voltage (J-V) measurement as is shown in figure 4.6. With this measurement setup, the standard test conditions are simulated with a AAA class Wacom WXS-156S-L2 solar simulator: to accurately simulate the illumination of one sun, a Halogen lamp and a Xenon lamp are combined to present a AM 1.5 spectrum as well as an irradiance equal to 1000 W/m^2; the temperature controller is installed on the test stage where the solar cells are placed, which makes sure that the temperature of the solar cell are kept constant at 25℃.

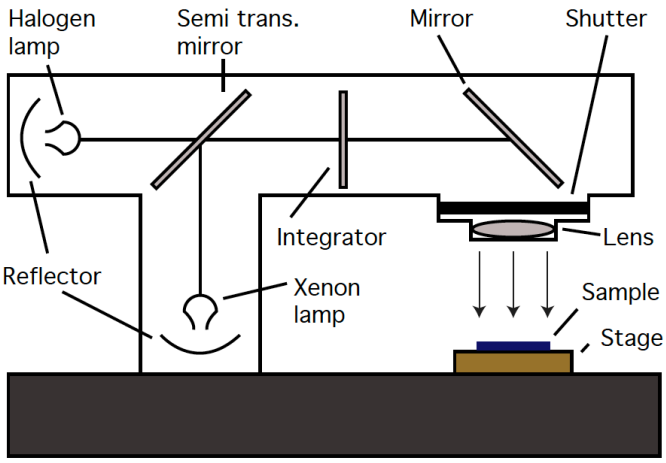


Figure **4.6**: Measurement setup of illuminated J-V measurement. Picture adapted from [57].

- ***Short circuit current density J_{SC}***

The short circuit current I_{SC} is the current obtained by the solar cell under short circuit conditions which is dependent on the area of the solar cell. To have better characterization, the short circuit current density J_{SC} is introduced normally with a unit of mA/cm^2. For crystalline silicon solar cells, the maximum current density that can be delivered under an AM 1.5 spectrum is 46 mA/cm^2.

- ***Open circuit voltage V_{OC}***

The open circuit voltage is the voltage obtained by the solar cell under open circuit

conditions. When the dark current density successfully compensates the photocurrent density, a net zero current is obtained with a forward bias voltage, which is corresponding to the open circuit voltage [2]. V_{OC} can be calculated using the following equation:

$$V_{OC} = \frac{k_B T}{q} \ln\left(\frac{J_{ph}}{J_0} + 1\right) \approx \frac{k_B T}{q} \ln\left(\frac{J_{ph}}{J_0}\right) \quad (J_{ph} \gg J_0) \tag{4.19}$$

- ***Fill factor FF***

The fill factor is defined by the ratio of the maximum power that can be delivered by the solar cell and the product of V_{OC} and J_{SC}:

$$FF = \frac{J_{mpp} V_{mpp}}{J_{SC} V_{OC}} \tag{4.20}$$

The theoretical maximum FF that can be obtained is determined under the assumption that the solar cell can behave like an ideal diode:

$$FF = \frac{v_{OC} - \ln(v_{OC} + 0.72)}{v_{OC} + 1} \tag{4.21}$$

Where v_{OC} is so called normalized voltage, and it is defined as:

$$v_{OC} = V_{OC} \frac{q}{k_B T} \tag{4.22}$$

- ***Conversion efficiency η***

The conversion efficiency is defined by the ratio of the maximum power that can be delivered by the solar cell and the incident power:

$$\eta = \frac{P_{max}}{I_{in}} = \frac{J_{mpp} V_{mpp}}{I_{in}} = \frac{J_{SC} V_{OC} FF}{I_{in}} \tag{4.23}$$

In the system mentioned above, the solar cells are measured under STC condition, which means that the incident power is kept constant at 1000 W/m^2.

4.5 External quantum efficiency measurement

The external quantum efficiency (EQE) is defined as the fraction of the total incident photons on the solar cell which are successfully collected in the absorber in the form of electron-hole pairs. In an ideal solar cell, the EQE is equal to 100%, but in practical, the parasitic absorption, reflection and recombination contribute to the losses of EQE. Equation (4.24) gives a mathematical definition of this parameter as a function of the

wavelength λ:

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \tag{4.24}$$

Where $I_{ph}(\lambda)$ is the photocurrent, which is a measured value dependent on the bias voltage, $\Psi_{ph,\lambda}$ is the spectral photon flux flow. As for crystalline silicon, the pronounced range of the wavelength should be within 300 and 1200 nm.

EQE spectra are measured with a spectral response setup. As is shown in figure 4.7, the setup uses a wavelength selective light source called Monochromator, a calibrated light detector and a current meter.

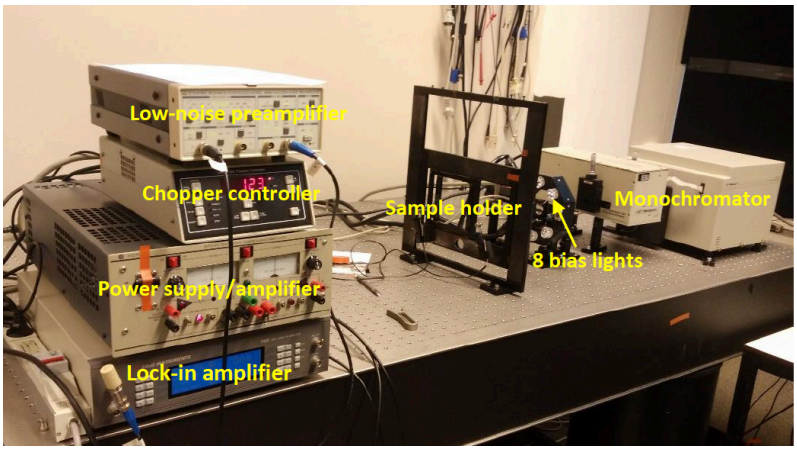


Figure **4.7**: Measurement setup of the EQE in PVMD Group. Picture adapted from [64].

To obtain the EQE of the solar cell, the photocurrent and the photon flux should be determined as indicated in equation (4.24). The photocurrent can be easily obtained by the Ampere meter, while the photon flux should be determined with a reference solar cell installed beneath the sample holder, which is calibrated by Fraunhofer ISE. With the EQE known, the reference cell helps to determine the photon flux based on the following equation:

$$\Psi_{ph,\lambda} = \frac{\mathrm{I}_{ph}^{\mathrm{ref}}(\lambda)}{qEQE^{ref}(\lambda)} \tag{4.25}$$

According to equation (4.24) and (4.25), the EQE of the solar cell can be obtained based on equation (4.26):

$$EQE(\lambda) = EQE^{ref}(\lambda)\frac{I_{ph}(\lambda)}{I_{ph}^{ref}(\lambda)} \tag{4.26}$$

Furthermore, the short circuit current density J_{SC} can be obtained by performing the EQE measurement under short circuit conditions. Although J_{SC} can also be measured by the J-V measurement which was discussed in section 4.3, this EQE measurement can obtain a more accurate J_{SC} as it is independent of the spectral shape of the light source [2]. The measurement of J_{SC} in this project even uses shading cardboards to diminish the influence of the contact area, making the measurement more reliable.
As is described above, the $EQE(\lambda)$ for the defined wavelength region can be obtained (300 to 1200 nm for c-Si solar cells), then the short circuit current density is obtained with the integration of the $EQE(\lambda)$ and spectral photon flux under AM1.5 condition $\Psi_{ph,\lambda}^{AM1.5}$ along the wavelength region:

$$J_{SC} = -q \int_{\lambda_1}^{\lambda_2} EQE(\lambda)\Psi_{ph,\lambda}^{AM1.5} d\lambda \tag{4.27}$$

4.6 Reflectance measurement

For full area back contact solar cells fabricated in this thesis, the absorption analysis with the help of reflectance measurement (1-R), which is obtained by a PerkinElmer Lambda 950 UV/VIS spectrometer. An overview of this measurement setup design is shown in figure 4.8, with the most important component integrating sphere (IS) installed. A highly reflective material named Spectralon is coated on the integrating sphere, and two detectors are installed inside for the measurement of total light intensity and the reflected light intensity, respectively. With this measurement setup, the reflectance can be determined based on equation (4.28) [57]:

$$R = \frac{(R_{meas} - R_{dark})R_{ref}}{R_{ref} - R_{dark}} \tag{4.28}$$

R_{dark} and R_{ref} are the reflectance measured when a Spectralon panel is placed in the reflectance sample holder, with the sample beam off (0% reference) and on (100% reference), respectively. R_{meas} is the reflectance measured when the sample is placed in the reflectance sample holder. This setup can also perform transmittance measurement based on a similar principle, which is not carried out here.

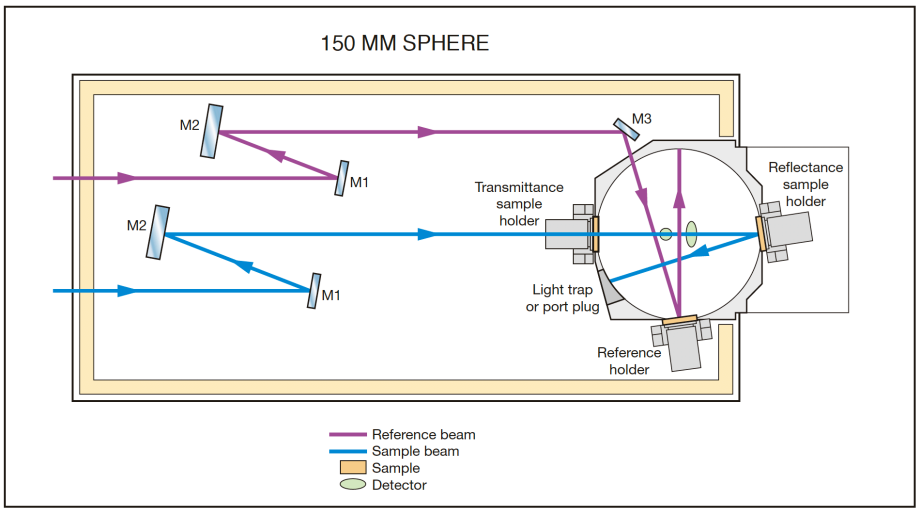


Figure **4.8**: Optical design of 150 mm integrating sphere. Adapted from [65].

5

Passivation optimization of poly-SiO_x passivating contacts

In this chapter, experiments on the optimization of poly-SiO_x passivating contacts are presented in detail. Firstly, in order to set a starting point of the experiment, a rough test is carried out based on the previous work on poly-SiO_x in PVMD group. To apply this novel structure into high-efficiency solar cell, optimizations on the material composition such as layer oxygen content and doping level during the deposition with PECVD were performed. Then the high-temperature annealing parameters are optimized to have highly crystallized structure as well as a nice doping profile of the contact. To minimize the defects, mainly the dangling bonds, at the interface between poly-SiO_x and the bulk c-Si surface, the crucial hydrogenation process is also investigated. Finally, the contact resistance of the poly-SiO_x/metal contacts is measured to make sure a good contact is formed.

5.1 The starting point of this work

In this section, the results obtained on the procedure to prepare the passivation samples with the previously developed process will be shown first. The first experiment is this section is to check whether the previous process flow chart still works. Hence, a rough test run is carried out first, and the measurement results of this section will be treated as the starting point, i.e. for the reference of the further optimization. The symmetric test samples based on poly-SiO_x passivating contacts are prepared as follows, and a schematic of these steps are shown in figure 5.1:

1. For the bulk material, a n-type c-Si wafer (Float-Zone (FZ), <100> orientation,

double side polished) with a thickness of around 280μm is used.

2. For the symmetric textured test samples (n^+ layer in this thesis), the bulk material is first immersed into the Tetramethylammonium Hydroxide (TMAH) solution at the temperature of 80℃ for around 10 mins to randomly texture the c-Si surface.
3. The wafers are processed with a standard cleaning process to remove the organic and inorganic contamination, then the native oxide is removed by a 0.55% HF dip.
4. The samples are immersed in the 69.5% HNO_3 solution at room temperature for 60 mins. This process will result in an ultra-thin tunnel oxide layer of around 1.4 nm [56].
5. The samples are then processed in the RF-PECVD chamber for the deposition of the intrinsic and doped a:SiO_x:H layers. Note that for the deposition of these two layers, the parameters are kept consistent except the doping gas flow ($[PH_3] = 0$ and $[B_2H_6] = 0$ for intrinsic a:SiO_x:H layers).
6. After the PECVD process, a high-temperature annealing at temperature at 850℃ for 30 mins is conducted to crystallize the a:SiO_x:H layers and drive in the dopants, after which a crystallized poly-SiO_x layer can be obtained.
7. Finally, a forming gas anneal at 400℃ for 30 mins is performed to further reduce the surface recombination.

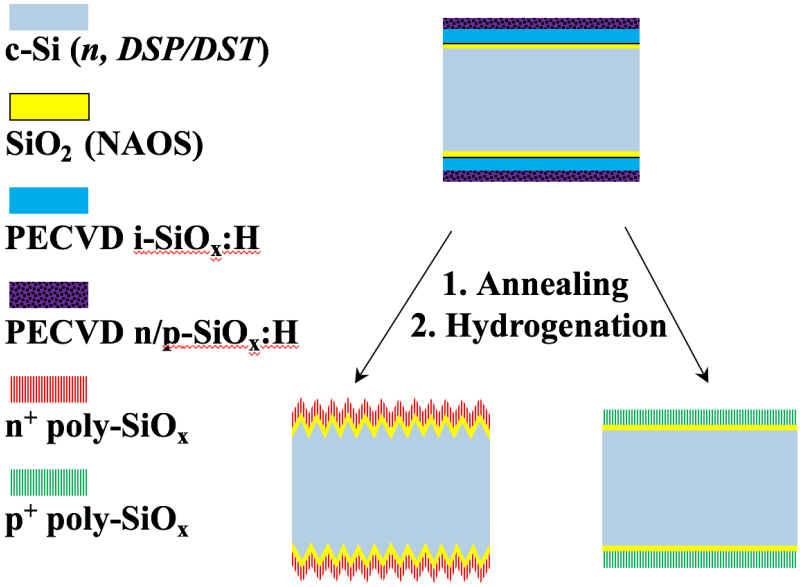


Figure **5.1**: Schematic sketch of the fabrication process of symmetric test samples.

After the high-temperature anneal process, the passivation measurement is performed with the Sinton WC-120 lifetime tester, and the implied V_{OC} as well as the saturation current density are shown in table 5.1.

Table **5.1**: Passivation properties of the poly-SiO_x contact in the test run. The references listed in this table were processed with the same parameters as the n^+/p^+ test samples but before the maintenance of the used setups.

Bulk c-Si	**Sample**	**Lifetime τ (ms)**	**Implied-V_{OC} (mV)**	**Saturation current density J_0 (fA/cm^2)**
n-FZ	n^+ Test	3.0	701	17.8
Textured	n^+ Reference [66]	4.9	710	12.0
n-FZ	p^+ Test	1.1	686	23.9
Flat	p^+ Reference [66]	2.1	692	25.0

5.2 Passivation optimization of poly-SiO_x layer

The aim of this section is to optimize the novel poly-SiO_x passivating contacts, which can be applied into the fabrication of high-efficiency solar cell. The requirements for creating a good poly-SiO_x passivating contact are first demonstrated, which will act as a guide line for the optimization throughout this chapter. Then the optimization is conducted and discussed in detail, including the PECVD process, high-temperature annealing as well as the hydrogenation treatment.

5.2.1 Requirements of the poly-SiO_x passivating contacts

Based on the discussion about the pros and cons of traditional TOPCon structure in chapter 2, the requirement of this poly-SiO_x layer can be summarized as follows:

1. First of all, this contact should have good optical performance, i.e. the deposited contacts should be transparent enough to minimize the light absorption in this layer. This can be controlled by adjusting the *oxygen content* of the layer to tune the band gap of the passivating contacts. It is proved that the absorption coefficient decreases

especially in the long wavelength with increasing oxygen content, which indicates that the material becomes more transparent [24, 38], at least in the long wavelength region. Besides, the thickness of the doped a-SiO_x:H layer should be optimized in a moderate level which provides high enough passivation quality, and avoids introducing additional current losses due to the unwanted absorption of the passivating contacts [23].

2. The passivating contacts should enable high passivation quality. This can be achieved by several ways. By properly controlling the *oxygen content*, the bandgap of this material can be expanded, which enables a larger band bending and thus an effective carrier transport (High open-circuit voltage). Besides, field effect passivation can also be employed to alter the surface concentration, where the *doping level* of the contacts can play an important role. Furthermore, the integrity of the tunnel oxide layer is essential for the chemical passivation of the c-Si surface as is discussed before, which is sensitive to the *high-temperature annealing* process. Last but not least, a defect-free c-Si/SiO_2 interface can further boost the passivation, indicating the importance of optimizing the *hydrogenation* process.

3. Thirdly, this passivating contact should be electrical conductive. Further crystallize the poly-SiO_x layer by properly prolong the *high-temperature anneal* process enables a higher conductivity and minimize current losses, which is preferred in solar cell design.

4. The optimized n^+ and p^+ contacts should be obtained with similar optimum thermal budget for the simplicity and lowering the cost of solar cell fabrication. During the fabrication of the front and back contacts (FBC) and IBC solar cells, both n^+ and p^+ contacts are deposited on the same wafer, and the high-temperature anneal is perform at the same time. With the similar thermal stability, good passivation can be achieved on this kind of asymmetric configurations, thus enabling high-efficiency solar cell fabrications.

Hence, to meet the above-mentioned requirement, the poly-SiO_x layer grown with PECVD should be optimized in both the material and the contacting with other solar cell elements, which will be addressed in the following section.

5.2.2 Material optimization

In this section, the optimization of the PECVD deposited poly-SiO_x layer will be

optimized in three deposition parameters, namely oxygen content, doping gas flow and the layer thickness. First of all, the test samples are prepared similarly as introduced in section 5.1 (see figure 5.1). In order to have better comparison among the results, the test samples are prepared under almost the same conditions except the investigated one. In this thesis, the layer properties are optimized by altering the gas composition during the PECVD process, including Silane (SiH_4), Carbon dioxide (CO_2), Hydrogen (H_2), Phosphine (PH_3) for n^+ contact doping and Diborane (B_2H_6) for p^+ contact doping. Here the oxygen content is defined as the ratio between CO_2 and the total gas flow of SiH_4 and CO_2 (equation 5.1), and the doping gas flow is defined as the ratio between PH_3/B_2H_6 and SiH_4 (equation 5.2). Figure 5.2 shows the schematic of symmetric test samples of both n-type and p-type poly-SiO_x. After the layer growth, high temperature annealing and hydrogenation, all the samples are measured with the Sinton WCT-120 lifetime tester.

$$R_{oxygen} = [CO_2]/([CO_2] + [SiH_4]) \quad (5.1)$$

$$R_{doping,n} = [PH_3]/([PH_3] + [SiH_4]) \quad (5.2a)$$

$$R_{doping,p} = [B_2H_6]/([B_2H_6] + [SiH_4]) \quad (5.2b)$$

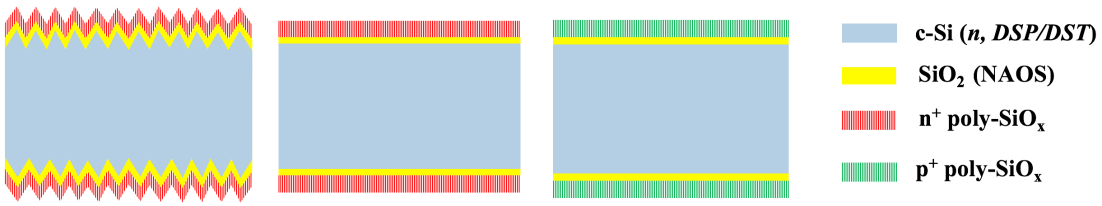


Figure **5.2**: Schematic sketch of the n^+ and p^+ poly-SiO_x passivation test samples.

- ***Influence of the oxygen content on the poly-SiO_x layer properties***

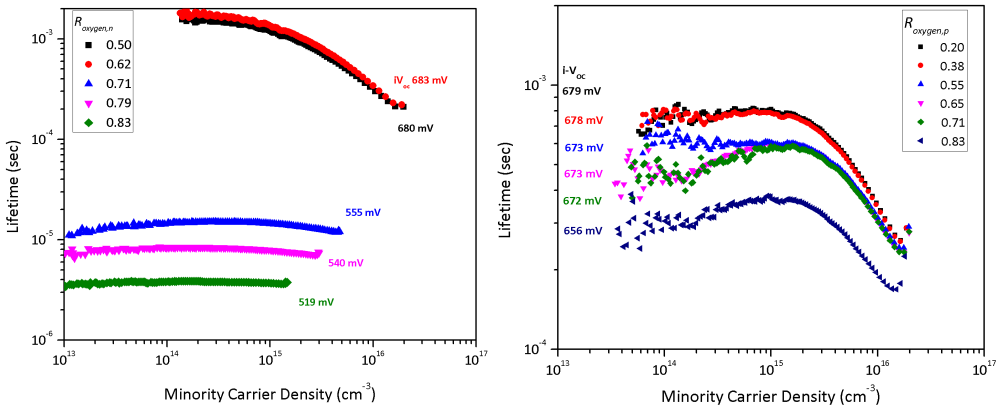
As is discussed before, the oxygen content plays an important role on both the optical and electrical properties of the poly-SiO_x layer. During the optimization of oxygen content, only the gas flow of CO_2 is altered, while the doping gas flows, the layer thickness as well as the high-temperature anneal parameters are kept constant. A summary of the deposition parameters is shown in table 5.2. It should be noted when changing the oxygen content, the deposition rate in PECVD chamber alters as well. Hence before the optimization on c-Si wafers, a test layer deposited on corning glass is first performed with the same receipt to measure the deposition rate with spectroscopic

ellipsometry. And the deposition rate measured should be divided by a factor of 1.7 when it is applied to the deposition on a textured surface.

Table **5.2**: Deposition parameters of test samples with different R_{oxygen}.

		n^+	p^+
PECVD parameters	R_{oxygen}	Variable	Variable
	R_{doping}	0.55	0.38
	Intrinsic layer thickness	10 nm	10 nm
	Doped layer thickness	20 nm	10 nm
High-temperature annealing		850 ℃ 30 mins	
Hydrogenation		No	

The passivation test samples are prepared with the same structure shown in figure 5.2, and the measurement results are shown in figure 5.3. It should be noted that no hydrogenation process is performed during the test.



(a) n^+ poly-SiO_x, textured (b) p^+ poly-SiO_x, flat

Figure **5.3**: Effective lifetime measurement of test samples with various R_{oxygen}.

The main findings from this experiment are summarized as follows:

1. Firstly, for the n^+ poly-SiO_x contacts, the oxygen content R_{oxygen} is increased from 0.5 (black square) to 0.83 (green diamond). For the relatively low oxygen content (R_{oxygen} of 0.50 and 0.62), good passivation can be obtained, with the implied-V_{OC} of 680 and 683 mV, respectively. Similar effective lifetime and saturation current density

values are observed. However, when the oxygen content is further increased (R_{oxygen} above 0.71), almost no passivation improvement is observed, with the implied-V_{OC} lower than 555 mV, the effective lifetime lower than 200 μs and the very high saturation current density above 800 fA/cm^2. The measurement results indicate that for n^+ poly-SiO_x contacts, the R_{oxygen} of 0.50 or 0.62 can be two options for the deposition which provide relatively good passivation.

2. Secondly, the p^+ contacts are also, and the results are shown in figure 5.5(b). Similar to n^+ contacts, the oxygen content R_{oxygen} is increased from 0.20 (black square) to 0.83 (navy blue triangle). A slow decline trend on the effective lifetime is observed, together with a decreasing implied-V_{OC} as a function of increasing R_{oxygen}, which indicates that the passivation quality is undermined when more oxygen is deposited in the layer. Interestingly, for the R_{oxygen} of 0.20 and 0.38, similar implied-V_{OC} of 679 mV and 678 mV and J_0 of around 28.0 fA/cm^2 for both are measured, both of which can be the suitable oxygen content for depositing p^+ poly-SiO_x contacts when considering only the passivation properties.

3. Furthermore, the deterioration of the passivation quality for both n^+ and p^+ passivating contacts under high oxygen content is addressed here. This can be explained by that the field effect passivation may be undermined. The passivating contact is a barrier against the dopant diffusion during the high-temperature annealing. With the increase of oxygen content, this barrier becomes higher, which further hinders the diffusion process. As a result, a not large enough gradient of the doping profile at the c-Si/CO_2 interface, which suppresses the field effect passivation.

4. To further investigate the influence of the oxygen content, quartz glass samples are prepared with the a-SiO_x:H layer directly deposited on top, and again the oxygen content is altered. After a high-temperature annealing at 850 ℃ for 30 mins, the Raman measurement is performed, which results in the Raman spectra shown in figure 5.4. As is indicated by the increase of intensity at the wavenumber of around 480 to 500 cm^{-1} [67], the crystallinity of the poly-SiO_x layer becomes lower with the increase of oxygen content. This can be explained by the increase of the SiO_x amorphous phase [24]. However, the crystallinity of the layer is still at a high level at the oxygen content up to a R_{oxygen} of 0.62.

Based on the above discussion, the optimized oxygen content should have a good balance between the good passivation and the low absorption. Hence, a higher R_{oxygen}

of 0.62 for n^+ passivating contacts and R_{oxygen} of 0.38 for p^+ passivating contacts are preferred, which also show good passivation quality and high crystallinity level.

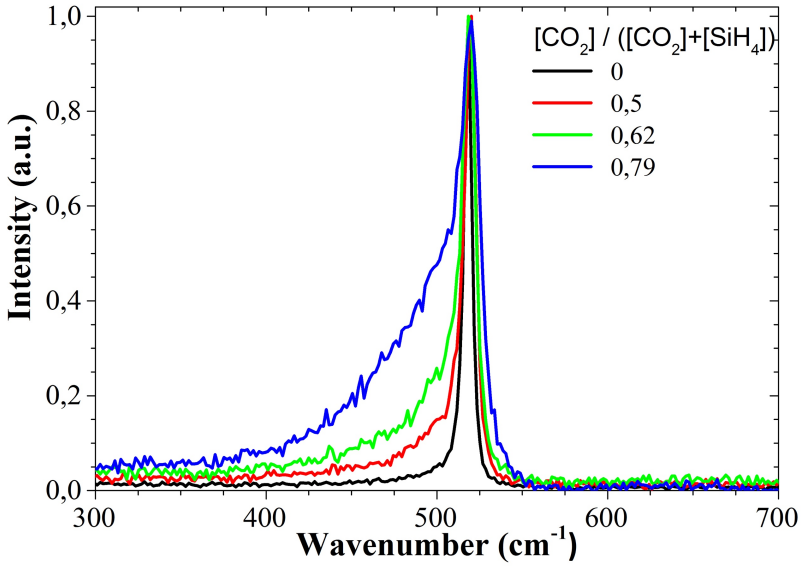


Figure **5.4**: Raman spectra of poly-SiO_x films on quartz glass with different oxygen content after a high-temperature annealing at 850℃ for 30 mins.

Table **5.3**: Deposition parameters of passivation test samples with different R_{doping}.

		n^+	p^+
PECVD parameters	R_{oxygen}	0.62	0.38
	R_{doping}	Variable	Variable
	Intrinsic layer thickness	10 nm	10 nm
	Doped layer thickness	20 nm	10 nm
High-temperature annealing		850 ℃ 30 mins /60 mins	
Hydrogenation		PECVD SiN_x + FGA 30 mins	

- ***The influence of doping gas flow ratio on the passivation quality***

A properly controlled doping concentration of the passivating contacts can benefit the passivation quality by means of field effect passivation. In this thesis, n-type wafers are used as the bulk material, so heavily doped n^+ passivating contact (surface field) is deposited to create a high-low junction. On the other hand, heavily doped p^+ passivating contact (emitter) is deposited to create a p-n junction. In order to investigate the

influence of the doping level on the contact passivation, the doping gas flow ratio is altered. An overview of the deposition parameters is shown in table 5.3. Note that the optimized oxygen content based on previous section are used. The passivation is measured both after annealing and after a hydrogenation process with PECVD SiN_x and FGA for 30 mins.

As is reported in figure 5.5, the best passivation is observed at a moderate $R_{doping,n}$ of 0.55 for n^+ contacts with an implied V_{OC} of 699 mV after annealing and 718mV after hydrogenation. While for p^+ contacts, the best passivation is obtained at a moderate but smaller $R_{doping,p}$ of 0.38, with the implied V_{OC} of 676 mV (as annealed) and 704 mV (after hydrogenation). Furthermore, when the annealing time is prolonged to 60 mins, and still, the best passivation is obtained at $R_{doping,n}$ of 0.55 and $R_{doping,p}$ of 0.38 for n^+ and p^+ contacts, respectively.

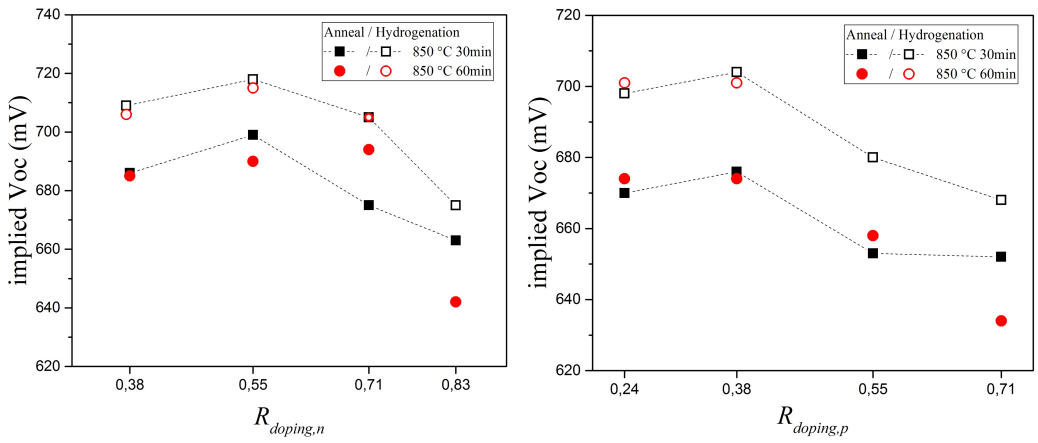


Figure **5.5**: The influence of the doping gas flow on the passivation properties of (a) n^+ and (b) p^+ poly-SiO_x contacts (Dashed lines are only used to guide eyes).

The reason for selecting a moderate deposition doping gas flow is that, if a too low doping gas flow is applied during the deposition, the doping level difference at the interface cannot provide a large enough band bending, thus undermining the field effect passivation. On the other hand, if the doping gas flow goes too high, the dopants can diffuse into the c-Si bulk and cause electrical defects at the c-Si/SiO_2 interface [68], and this over-diffusion causes the lower doping level difference at the interface, where the band bending is not sufficient. As is reported, the Auger recombination become more significant under a higher doping level [12]. Such kind of interaction indicates an

optimum doping concentration of the passivating contact layers can be reached at a moderate level. In conclusion, the optimum doping gas flow ratios are $R_{doping,n}$ of 0.55 and $R_{doping,p}$ of 0.38 for n^+ and p^+ contacts, respectively.

- ***The influence of doped a-SiO_x:H layer thickness on the passivation quality***

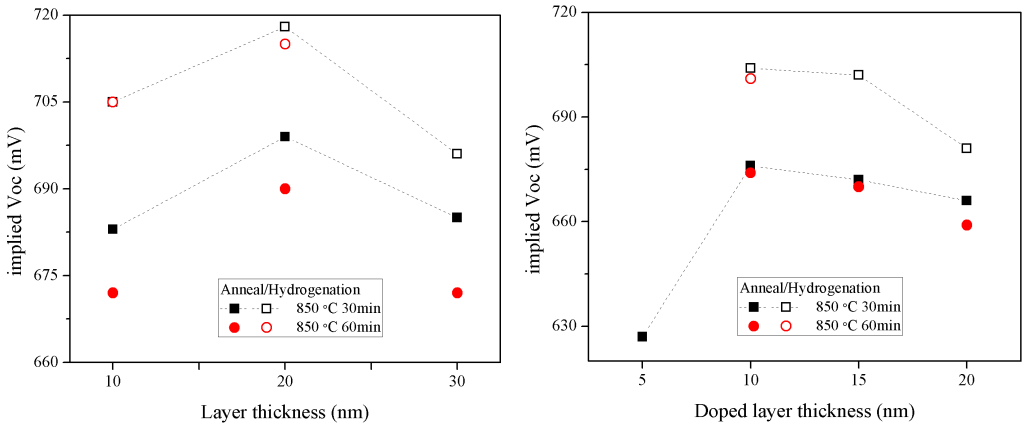
As is demonstrated in section 5.1, the thickness of the doped a-SiO_x:H layer should be controlled at a proper value, as the changes on the thickness of the doping layer influences the dopant diffusion process during the high-temperature annealing. In this section, the doped layer thickness is either increased or decreased while the intrinsic a-SiO_x:H layer thickness is kept constant. An overview of the deposition parameters is shown in table 5.4. The passivation measurements are conducted again, and the results are shown in figure 5.6 in the terms of implied-V_{OC}. For n^+ passivating contacts, the highest implied-V_{OC} (718 mV) is obtained with a moderate doped layer thickness of 20 nm after hydrogenation, while for the p^+ passivating contacts, the optimum doped layer thickness is 10 nm with an implied V_{OC} of 704 mV after hydrogenation.

Table **5.4**: Deposition parameters of passivation test samples with different doped a-SiO_x:H layer thickness.

		n^+	p^+
PECVD parameters	R_{oxygen}	0.62	0.38
	R_{doping}	0.55	0.38
	Intrinsic layer thickness	10 nm	10 nm
	Doped layer thickness	Variable	Variable
High-temperature annealing		850 ℃ 30 mins /60 mins	
Hydrogenation		PECVD SiN_x + FGA 30 mins	

During the investigation, for both n^+ and p^+ passivating contacts, the decline in passivation quality is observed when increasing or decreasing the doped layer thickness, which indicates that there is an optimum doped layer thickness. A too thin or too thick doped layer in fact indicates a too low or too high doping level. As is discussed previously, a too low doping provides poor field effect passivation while a too high doping causes the problems of too deep dopant diffusion to c-Si bulk, both of which

lead to a decrease of the band bending at the interfaces, and the latter also leads to significant Auger recombination. In conclusion, when using a 10-nm thick intrinsic a-SiO_x:H layer, the optimum thickness for doped a-SiO_x:H layer is 20 nm and 10 nm for n^+ and p^+ contacts, respectively.



(a) (b)

Figure **5.6**: The influence of the doped layer thickness on the passivation properties of (a)n^+ and (b) p^+ poly-SiO_x contacts (Dashed lines are only used to guide eyes).

5.2.3 Optimization of high-temperature annealing

As is discussed in chapter 2 and 3, it's important to properly design the high-temperature annealing parameters. A high thermal budget can influence the electrical and optical performance of the passivating contacts by affecting the dopants diffusion and the layer crystallization. With a too high temperature or too long annealing time, break up process can happen in the tunnel oxide layer, and the dopants will heavily diffuse from the poly-SiO_x layer into the bulk material, which will undermine the passivation significantly [25] [69].

Hence, the high-temperature annealing is optimized in order to have a good balance between the crystallization level of the poly-SiO_x layer and the dopant diffusion control. First of all, the symmetric test samples are prepared with the parameters shown in table 5.5. Note that for n^+ passivating contacts, both textured and flat samples are prepared, while for p^+ contacts, only flat samples are prepared. Note that in this section, no hydrogenation process is performed on the test samples.

Table **5.5**: Deposition parameters of n^+ and p^+ passivating contacts with different thermal budget.

		n^+	p^+
PECVD parameters	R_{oxygen}	0.62	0.38
	R_{doping}	0.55	0.38
	Intrinsic layer thickness	10 nm	10 nm
	Doped layer thickness	20 nm	10 nm
High-temperature annealing		Variable	
Hydrogenation		No	

According to the results shown in figure 5.7, all the samples are sensitive to the high temperature annealing process, and the main findings can be summarized as follows:

- ***n^+ poly-SiO_x contacts on textured surface***

1. For n^+ poly-SiO_x contacts on textured wafer, the best passivation is observed at the annealing temperature of 850 ℃ for 30 mins, where an implied-V_{OC} of 683 mV and a saturation current density of 38.3 fA/cm^2 are obtained before hydrogenation.

2. If the sample is annealed at the same temperature but for a different duration, the passivation quality is undermined. For the short annealing time (less than 30 mins), the passivation is improved as the implied V_{OC} is increasing depending on the annealing time, and at the annealing time of 30 mins, the passivation shows the optimum. While by prolonging the annealing time (from 30 mins to 60 mins), a passivation drop is observed. This can be explained by that at the annealing temperature of 850 ℃, the integrity of the tunneling oxide is preserved. However, with a too short annealing time, the dopants will not fully diffuse within the poly-SiO_x layer, which results in a too low doping in the poly-SiO_x material at the SiO_x/poly-SiO_x interface. As a result, it is not enough to provide a good field effect passivation at the c-Si/SiO_x interface. A very large gradient of the dopants distribution will be formed within the poly-SiO_x layer, consequently the passivation quality will be destroyed due to not enough band bending to create a high built-in voltage, and the conductivity of the layer will also be declined [56]. On the other hand, if the annealing time is too long, the dopant can deeply diffuse into the c-Si bulk through the tunnel oxide layer. Therefore, a significant recombination

due to high concentration of charge carriers can happen at the interface, thus reducing the surface passivation.

3. For a higher thermal budget (900 ℃ and 950 ℃ for 5 mins), a reduced passivation can be observed compared with the sample annealed at 850 ℃ for 30 mins, together with a drop of sheet resistance (80.2 Ω/cm^2 at 850 ℃, 65.7 Ω/cm^2 at 900 ℃ and 25.2 Ω/cm^2 at 950 ℃). This can be explained by that with an annealing temperature higher than 900 ℃, the tunnel oxide layer can be damaged, and the so-called pinholes are created along the tunnel oxide layer [44, 56], thus undermining the chemical passivation. The pinholes exist in the tunnel oxide before it breaks up entirely. These small pinholes provide local contact between the bulk c-Si and the heavily doped poly-SiO_x layer, so the transport of the carriers becomes stronger and the Auger recombination becomes more significant. The combined mechanisms result in the increase of the saturation current.

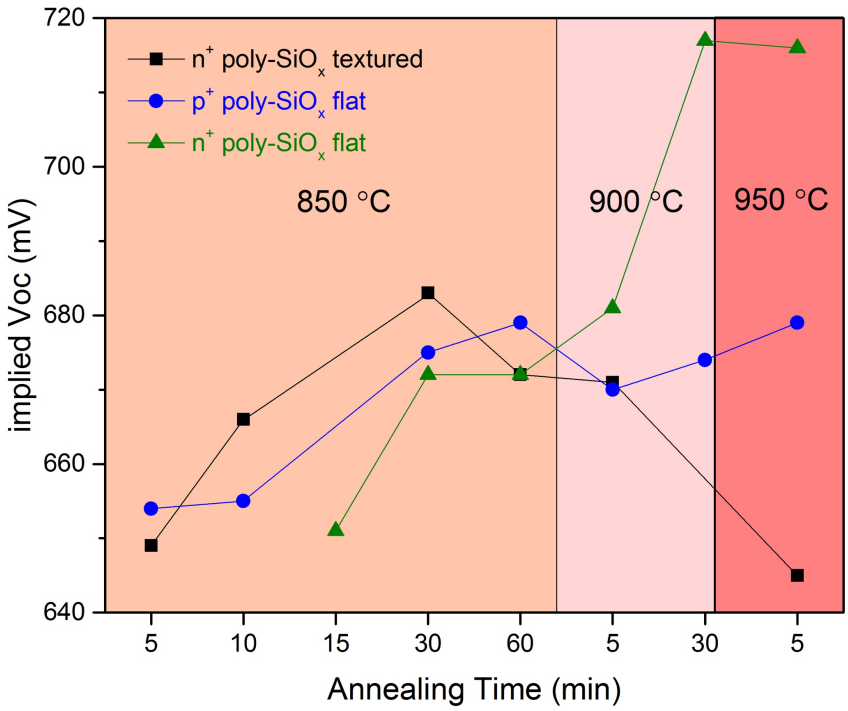


Figure 5.7: Passivation results for samples annealed with various high-temperature anneal parameters before hydrogenation (lines are used to guide eyes).

- ***n^+ poly-SiO_x contacts on flat surface***

The best passivation of the n^+ passivating contact is obtained at a relatively high temperature of 900 ℃ for 30 mins, with an excellent implied-V_{OC} of 717 mV before

any hydrogenation. No significant sheet resistance drop is observed except the one annealed at 950 ℃ (around 80 Ω/cm^2 at both 850 ℃ and 900 ℃ and 76.8 Ω/cm^2 at 950 ℃), which indicates n^+ contacts on flat surface have higher thermal stability. Comparing to n^+ passivating contacts on textured surface, the different dependence of the passivation on the thermal budget can be explained by that, both the growth of the tunnel oxide layer and the a-SiO_x:H layers are different. For instance, the different growth rate will result in different layer thickness and the layer uniformity can also be different, which results in the difference in the layer properties and thus the thermal stability.

- ***p^+ poly-SiO_x contacts on flat surface***

1. As is shown in figure 5.9, at the annealing temperature of 850 ℃, the passivation quality was improved with the increase of the annealing time. At the annealing time of 60 mins, the best passivation for the p^+ passivating contact was obtained which shows an implied-V_{OC} of 679 mV, J_0 of 29 fA/cm^2 and a sheet resistance of 67.1 Ω/cm^2 before hydrogenation treatment. Note that for the annealing time of 30 mins, the sheet resistance was measured around 76.7 Ω/cm^2. By increasing the annealing temperature to 900 ℃, the lower implied-V_{OC} of 670 mV and 674 mV were measured at the annealing time of 5 mins and 30 mins, respectively. The sheet resistances were measured around 76 Ω/cm^2, which indicates the integrity of the tunnel oxide layer is highly preserved at this temperature. For the samples annealed at 950 ℃ for 5 mins, the implied-V_{OC} of 679 mV and a J_0 of 30 fA/cm^2 were measured, with the sheet resistance of 67 Ω/cm^2. The drop in sheet resistance can be ascribed to the induced damage on the tunnel oxide layer or the over-diffusion of the dopants into the c-Si bulk.
2. However, the relatively low implied-V_{OC} indicates a weaker passivation compared with n^+ contacts. This can be ascribed to the fact that the Boron doped passivation layer can have a higher defect density [70]. Furthermore, the extent of the Boron diffusion differs to the Phosphorus because of their sizes, which means Boron, with a smaller atom size, will diffuse through the tunnel oxide layer easier, resulting in a higher defect density of the tunneling oxide layer and too high doping in the c-Si at the interface, where the band bending is decreased.

In conclusion, so far, the optimum high-temperature annealing schemes obtained for n^+ and p^+ are not consistent, and this may cause problems with the passivation

quality of an asymmetric configuration. This indicates that a balance should be set to apply both of them into a solar cell fabrication. Besides, it is still not clear which high-temperature annealing scheme gives the best passivation as the defects at the c-Si/SiO_x interface can be further reduced by the hydrogenation scheme. Hence, the optimum passivation scheme can be finally determined with the combination of the following investigation on hydrogenation.

5.2.4 Optimization of hydrogenation

In order to further improve the passivation properties, the hydrogenation approach is introduced to reduce the defects of the c-Si/SiO_2 interface [49, 71]. It is already shown in the previous optimization that the hydrogenation process is of great significance to the improvement of passivation, which provide additional hydrogen for the chemical passivation of the defects at the c-Si/SiO_2 interface [71]. In this section, the hydrogenation schemes will be investigated, and then the influence of the high-temperature annealing combined with the hydrogenation process will be tested. Finally, the better treatment can be found based on the passivation test.

To see which scheme shows the best passivation improvement on the poly-SiO_x contacts, symmetric n^+ flat samples are prepared based on the same optimized receipt so far. After a high-temperature annealing at 850 ℃ for 30 mins, the samples 1-3 are treated with different hydrogenation schemes:

Sample 1: A direct forming gas annealing (FGA) at 400 ℃ in the furnace for 30 mins.

Sample 2: The second one includes a PECVD SiN_x deposition of 75 nm, which is then followed by a 30-min FGA.

Sample 3: The third one is the combination of an atomic layer deposition (ALD) Aluminum oxide (Al_2O_3) of 10 nm, a PECVD SiN_x deposition of 65 nm and a FGA for 30 mins. Finally, the passivation of these three samples are measured and the results are shown in figure 5.8.

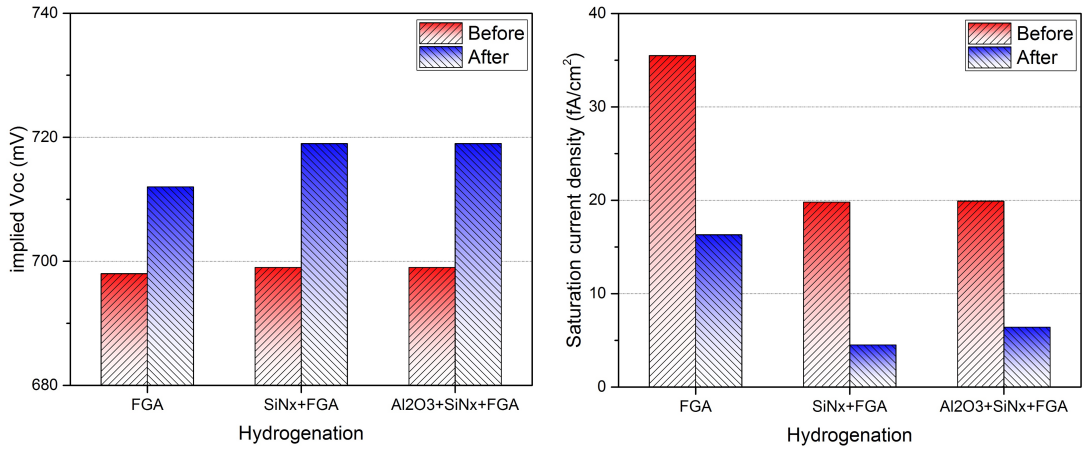


Figure **5.8**: Passivation properties of the samples treated with different hydrogenation schemes.

As is shown, all the samples are benefited from the hydrogenation process, which is indicated by a significant boost in implied-V_{OC} and a drop in J_0. This improvement on passivation quality indicates that the defect rich c-Si/SiO_2 interface is effectively passivated by the additional hydrogen. However, different passivation improvement can be observed from these three samples. With a direct FGA for 30 mins, sample 1 obtained a gain in implied-V_{OC} (from 698 mV to 712 mV) and the drop in J_0 (from 35.5fA/cm^2 to 16.3 fA/cm^2), which are not as significant as the other two samples. While for both sample 2 and sample 3, the implied-V_{OC} increased from 699 mV to 719 mV, with a sharp J_0 drop from around 20 fA/cm^2 to below 6.5 fA/cm^2, indicating that these two schemes give better passivation on the passivating contacts. This can be explained by the fact that either the Al_2O_3 or the SiN_x act as the hydrogen effusion barrier, by which the hydrogen is capped within the contacts, allowing sufficient amount of hydrogen at the c-Si/ SiO_x interface. As a result, the chemical passivation is further improved [71]. Compared with sample 2 and sample 3, a similar passivation improvement is gained. To simplify the fabrication process, the scheme with only a PECVD SiN_x layer introduced is preferred.

Finally, the selected hydrogenation scheme is applied to the symmetric test samples and the passivation results are presented in figure 5.9. Based on the optimized receipts, the excellent passivation can be observed in all of the three different contacts. With the optimization work, for n^+ contacts on textured surface, the best passivation with an excellent implied-V_{OC} of 723 mV and a very low J_0 of 6.9 fA/cm^2 is obtained. For p^+

contacts on flat surface, the best passivation is found to have an implied-V_{OC} of 709 mV and a low J_0 of 13.9 fA/cm^2. For the n^+ contacts on flat surface, the passivation quality is preserved within a very wide region of the thermal budget indicated by the similar implied-V_{OC} of around 727 mV from 850 ℃, 30 mins to 950 ℃ for 5 mins. The best J_0 found is as low as 2.4 fA/cm^2, even in the worst case, the extremely low J_0 of 4.8 fA/cm^2 is obtained, indicating that the n^+ contacts on flat surface can have a very wide process window. Most interestingly, combined with the optimum hydrogenation process (SiN_x+FGA), the best passivation is obtained with a consistent high-temperature annealing parameters at 850 ℃ for 30 mins, which indicates that these three contacts have the similar optimum thermal budget and it is possible to have good passivation quality in a solar cell which is asymmetrically fabricated with both n^+ and p^+ passivating contacts.

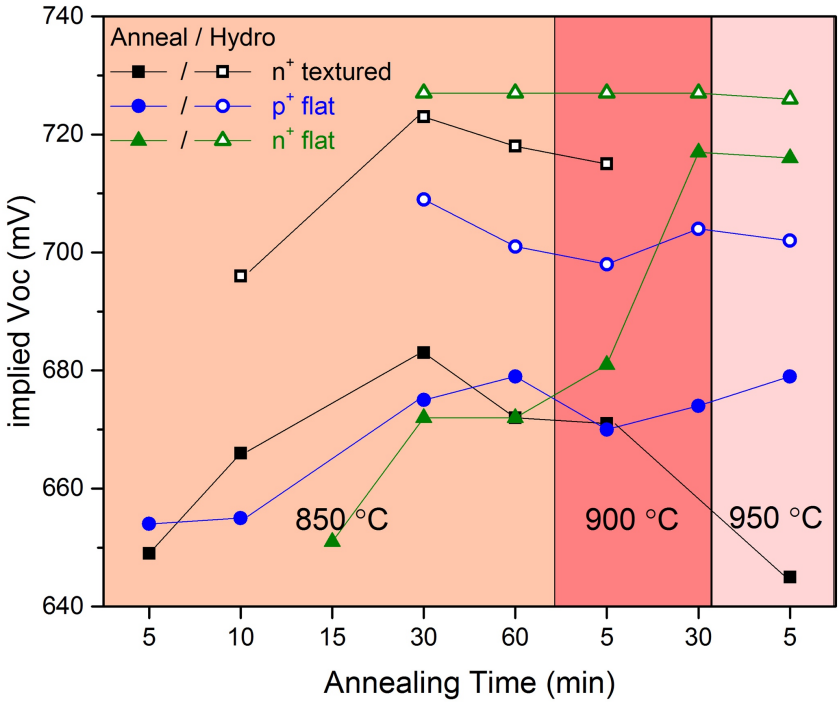


Figure **5.9**: Optimization of the high-temperature annealing combined with hydrogenation (Lines are used to guide eyes).

In conclusion, in section 5.2, experiments are conducted in order to optimize the poly-SiO_x passivating contacts for an excellent passivation quality. It is found that the parameters such as R_{oxygen}, R_{doping}, Doped layer thickness, annealing temperature, annealing time and hydrogenation are correlated to each other, and by setting the correct balance between the passivation quality and the conductivity [24], the optimized poly-

SiO_x passivating contacts is obtained. A summary of the optimized deposition parameters is shown in table 5.6.

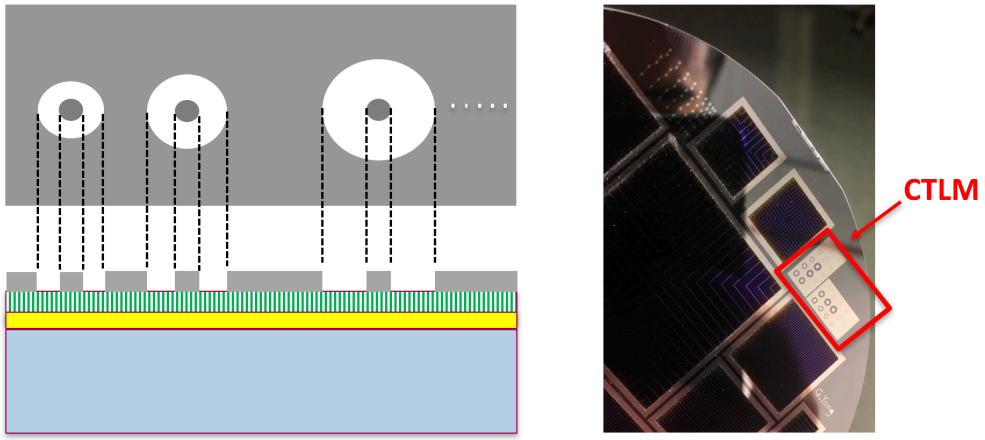
Table **5.6**: Overview of the optimized poly-SiO_x layer deposition parameters

		n^+	p^+
PECVD parameters	R_{oxygen}	0.62	0.38
	R_{doping}	0.55	0.38
	Intrinsic layer thickness	10 nm	10 nm
	Doped layer thickness	20 nm	10 nm
High-temperature annealing		850 ℃ 30 mins	
Hydrogenation		PECVD SiN_x + FGA 30 mins	

5.3 Contact resistivity test

Before starting the fabrication of any solar cells, a contact resistivity test must be performed to evaluate the contact properties of the poly-SiO_x/Metal contact. Contact resistance between the poly-SiO_x and the metal layer should be low enough to show an ohmic behavior, with which the voltage drop in the semiconductor and metal interface can be minimized. Hence, the circular transfer length method (CTLM) is applied to measure the specific contact resistance. Note that for the n^+/aluminum contact, previous work [24] has already shown good ohmic behavior, so only the samples with p^+ and aluminum contact will be prepared with the following steps:

1. Standard cleaning and a 0.55% HF dip for the basic cleaning.
2. Room temperature NAOS for 60 mins to grow the tunnel oxide layer.
3. Intrinsic and p^+ a-SiO_x:H layers deposition with PECVD with the optimized receipt obtained in section 5.2.
4. High-temperature annealing at 850℃ for 30 mins to drive in and activate the dopants.
5. After applying photolithography for the CTLM structure patterning, a 1000 nm aluminum layer is grown by evaporation on top of the poly-SiO_x layer.
6. Finally, the CTLM structure is obtained by a metal lift-off process in acetone as is shown in figure 5.10.



(a) (b)

Figure 5.10: Illustrations of CTLM samples: (a) Schematic representation of circular transfer length method. (b) CTLM structure on FZ c-Si wafer.

To measure the specific contact resistivity, a dark I-V current measurement was performed. The measurement results are collected and analyzed based on the CTLM, which are shown in table 5.7. both test samples show the ohmic behavior, and the contact resistivity of both n^+ and p^+ contacts are relatively low compared with the measurement done by the previous research [37, 72]. Hence, from the contact resistivity measurement, the optimized poly-SiO_x passivating contacts are proved to have good contact directly with the Aluminum metal layer.

During the CTLM, the bulk current flow is neglected, so the specific contact resistivity is a little bit over-estimated. However, a very small contact resistivity is still obtained, indicating that the poly-SiO_x/aluminum contact is good enough to neglect its influence on the fill factor losses.

Hence, the optimized receipts for the deposition of both n-type and p-type poly-SiO_x show good contact with the metal layer, indicating that the optimization results obtained so far is capable of going into solar cell fabrication.

Looking back into the requirements claimed in section 5.1, the poly-SiO_x contacts obtained so far can be processed under the same optimum high-temperature annealing parameters of 850 ℃ for 30 mins. They have relatively high oxygen content to enable a better optical response as well as an excellent passivation.

Table **5.7**: Overview of the CTLM structure measurement.

	Contact resistivity $(m\Omega \cdot cm^2)$	**Contact**
Flat n^+ poly-SiO_x	0.7 [24]	Ohmic
Flat p^+ poly-SiO_x	0.5	Ohmic

5.4 Conclusion

In this chapter, the optimization of the poly-SiO_x passivation contacts is performed. After setting a starting point of the experiment, the requirements of the contacts are claimed to evaluate the results of the optimization. Then the essential deposition parameters of PECVD, high-temperature annealing process as well as the hydrogenation schemes are investigated. The balance between these interacting parameters are finally set for the optimum passivation, which results in the very good passivation (J_0 of 6.9 fA/cm^2 for n^+/n textured contacts, 2.4 fA/cm^2 for n^+/n flat contacts and 13.9 fA/cm^2 for p^+/n flat contacts). Finally, a contact resistivity test is performed, and a low contact resistivity of 0.5 $m\Omega \cdot cm^2$ is found for p^+/Al contact, which is suitable for solar cell fabrications.

6

Solar cells fabrication and discussion

In this chapter, the optimized poly-SiO_x films will be applied as the carrier-selective passivating contacts (CSPCs) for the front and back contacted (FBC) solar cells fabrication. The double side polished (DSP) solar cells are treated in section 6.1, both the fabrication process and the characterization of solar cells will be discussed. Different process schemes (ITO deposition, metallization) are compared in device level. Section 6.2 presents the fabrication of front side textured (FST) solar cells. After an introduction of the fabrication process, the passivation test of the precursors and the performance of solar cells will be discussed. To highlight the gain in applying this novel CSPCs, the comparison against other solar cell configurations will be treated. Finally, a LPCVD a-Si:H layer is inserted in the contacts, which acts as a potential fabrication option.

6.1 Double side polished solar cell

In order to investigate the contacting of poly-SiO_x CSPCs and their carrier collection at the device level, double side polished (DSP) solar cells are fabricated, and the fabrication process is tested. The passivation properties of the cell precursor as well as the performance of the first fabricated FBC solar cell are measured and analyzed in detail. Then different schemes in the ITO deposition as well as metallization are investigated in order to find the optimum contacting approach for the solar cells fabrication.

6.1.1 Fabrication process

The fabrication process of the DSP solar cells, shown in figure6.1, can be summarized with the following steps:

1. For the bulk material, a n-type c-Si wafer (Float-Zone (FZ), <100> orientation, double side polished) with a thickness of around 280μm is used. The wafers are processed with a standard cleaning process to remove the organic and inorganic contamination, then the native oxide is removed by a 0.55% HF dip.
2. The samples are immersed in the 69.5% HNO_3 solution at room temperature for 60 mins, which results in an ultra-thin tunnel oxide layer of around 1.4 nm [56].
3. The samples are then processed in the RF-PECVD chamber for the deposition of the intrinsic and doped a-SiO_x:H layers. Note that for the deposition of these two layers, the parameters are kept consistent except the doping gas flow ([PH_3] = 0 or [B_2H_6] = 0 for intrinsic a-SiO_x:H layers).
4. After the PECVD process, a high-temperature annealing at temperature at 850℃ for 30 mins is conducted to crystallize the a-SiO_x:H layers and drive in the dopants, after which a crystallized poly-SiO_x layer can be obtained. Then a forming gas anneal at 400 ℃ for 30 mins is performed to further reduce the surface recombination.
5. After a 0.55% HF dip, the samples become hydrophobic, which is prior to the ITO deposition process [43]. Then an ITO layer of around 75 nm is sputtered on top of the p^+ poly-SiO_x film, which is shown as figure 6.1 (e1) For a double side ITO precursor, another ITO layer of around 120 nm is sputtered on the top of the n^+ poly-SiO_x film, which is shown in figure 6.1 (e2).
6. The front side metal finger is patterned with the positive photoresist with a photolithography process, which is followed by a 1000-nm aluminum evaporation and a lift-off process to remove the inactive metal region together with photoresist. For the rear side, a full-area aluminum evaporation for 1000 nm is done with a hard mask.

Figure 6.1 shows the schematic representations of each process discussed above, and the pictures taken in the lab for both front and rear sides of the solar cell are shown in figure 6.2 to have a clear view of the cell structure.

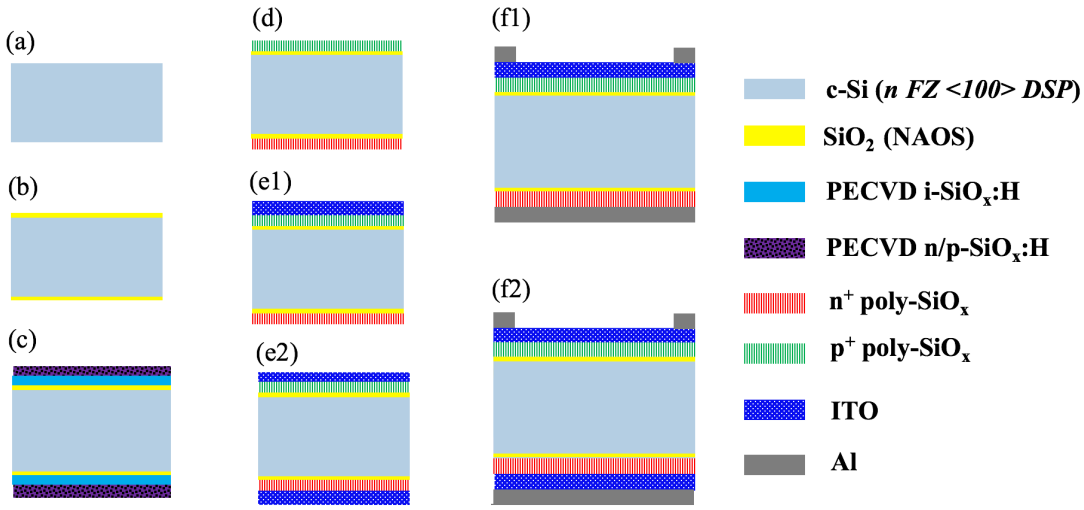
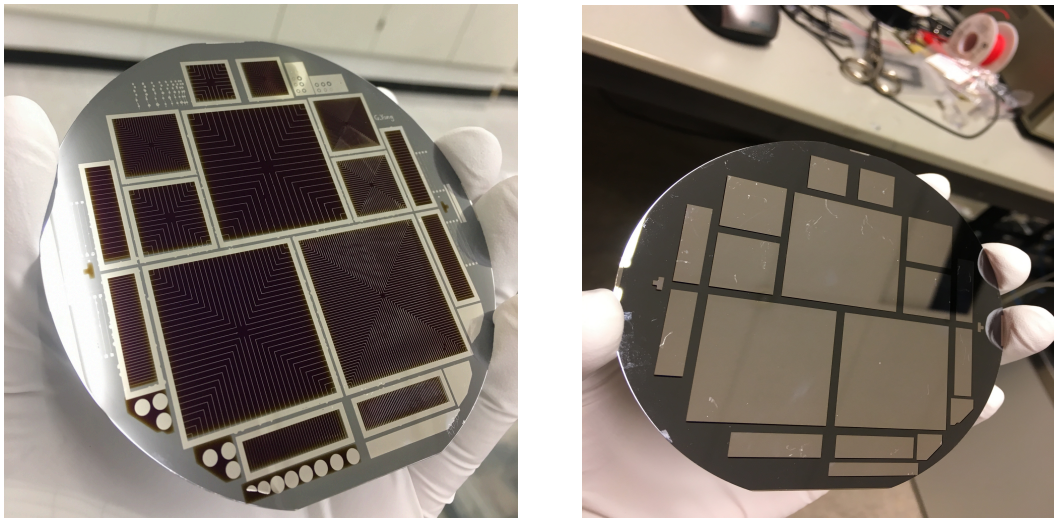


Figure **6.1**: Schematic representations of fabrication process of front and back contacted solar cell with poly-SiO_x passivating contacts.



(a) (b)

Figure **6.2**: Double side flat solar cell with poly-SiO_x passivating contacts: (a) front side. (b)rear side.

6.1.2 Front and back contacted solar cell with a high FF of 83.5%

In this section, the performance of the first front and back contacted (FBC) solar cells fabricated is addressed, which is fabricated with only a front side ITO layer as is shown in figure 6.1(f1). During the fabrication process, the passivation of the solar cell

precursor is tracked to investigate the influence of each treatment. The passivation is measured after high-temperature annealing, after hydrogenation and after the TCO deposition with the Sinton lifetime tester, which is shown in figure 6.3 in the terms of implied-V_{OC} and the saturation current density J_0. After the high-temperature annealing, the precursor is slightly passivated, with an implied-V_{OC} of 677 mV and a saturation current of 50 fA/cm^2. With the following hydrogenation treatment, the c-Si/SiO_2 interface is further passivated, which is indicated by an improvement of implied-V_{OC} (700 mV) and a drop in J_0 (23 fA/cm^2). Then a ITO layer is sputtered on top of the p^+ poly-SiO_x film to enhance the carrier transport as well as light capping (TCO layer). As is expected, the passivation of the precursor is slightly affected by the sputter damage [25] [73] [74], and a drop of i-V_{OC} (695 mV) and an increase of J_0 (29.5 fA/cm^2) can be observed.

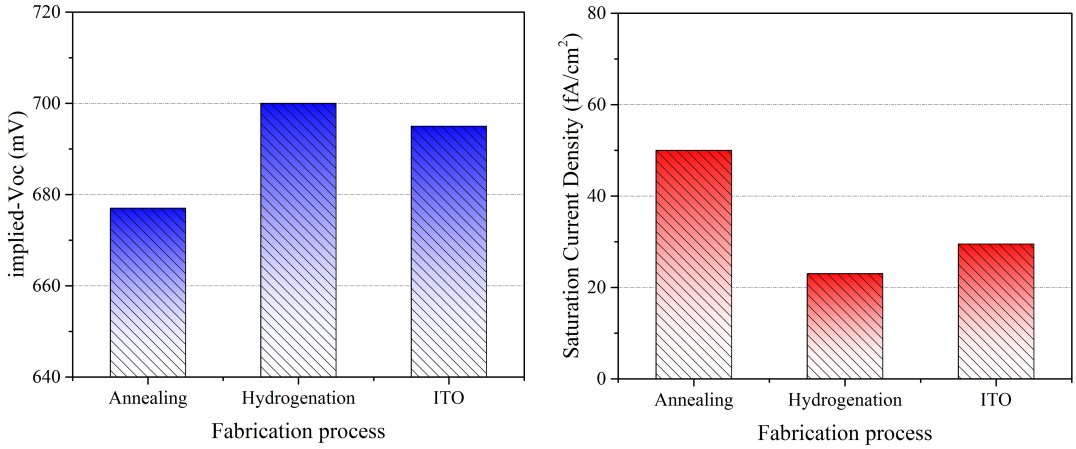


Figure **6.3**: Passivation test of DSP solar cell precursor.

Finally, the first front and back contacted solar cells are successfully fabricated with the aluminum evaporation, which results in a patterned front metal grid and a full area back metal contact. The solar cells are characterized by light J-V measurement, an EQE measurement as well as a SunsV_{OC} test, and the results are summarized in table 6.1. Interestingly, an excellent fill factor of 83.5 % is measured. This indicates that the charge carrier transport is very efficient through the poly-SiO_x, and the ITO as well as the metal layer shows effective carrier collection. However, a significant loss in open-circuit voltage is observed. Compared with the SunsVoc of 695±5 mV measured before metallization process, the solar cell V_{OC} of 681 mV is relatively low. This loss is mainly

ascribed to the defects induced by the photolithography and e-beam evaporation process, which points out the importance of optimizing the metallization process on reducing the loss in V_{OC}. Applying screen printing techniques on the front side metal patterning can be one option to reduce the damage, which will be investigated in section 6.1.3. The efficiency is also limited by relatively low current, which is mainly attributed to a weak light trapping with the flat front surface and possibly a lack of conductivity as the rear side is contacted without an additional ITO layer. Hence, in order to further boost up the current, (1) a double side ITO scheme can be beneficial to creating a more conductive rear contact. (2) a textured front surface should be applied to further enhance light trapping. These two options will be investigated in the following sections.

Table **6.1**: Overview of the performance of the front and back contacted flat cell.

Cell	Area [cm^2]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]	SunsV_{OC} [mV]	pFF [%]
Flat	2	681	33.4	**83.5**	19.0	701	84.3

6.1.3 Optimizations on the process schemes

- ***Influence of an additional ITO layer on the rear side***

In this section, the influence of rear ITO layer on both the passivation and the current gain will be investigated. Solar cells with two different configurations: one with only the front side ITO layer, and the other with front and rear ITO are prepared, and their fabrication process as well as the solar cell configurations are shown in figure 6.1 (f2).

During the fabrication, the passivation quality of the precursors is measured and compared as shown in figure 6.4. The blue bar indicates the precursor without rear side ITO, while the red bar indicates the one with rear side ITO.

For a better comparison, precursors with similar passivation after the high-temperature annealing (i-V_{OC} of 687 and 688 mV, J_0 of 61.2 and 64 fA/cm^2) are selected for the fabrication. As is can be observed, both precursors are again benefited from the hydrogenation process (FGA 30 mins), with a similar gain in passivation (i-V_{OC} of 698 and 699 mV, J_0 of 44.3 and 39.1 fA/cm^2). However, with both side sputtered with ITO, the precursor suffers from a larger loss in passivation as is indicated

by a lower i-V_{OC} as well as a higher J_0 compared with the single side ITO precursor. This is reasonable as a double side ITO layer induces sputter damage on both side, while for the precursor with only a front side ITO, the passivation of the n^+ poly-SiO_x film on the rear side can be preserved.

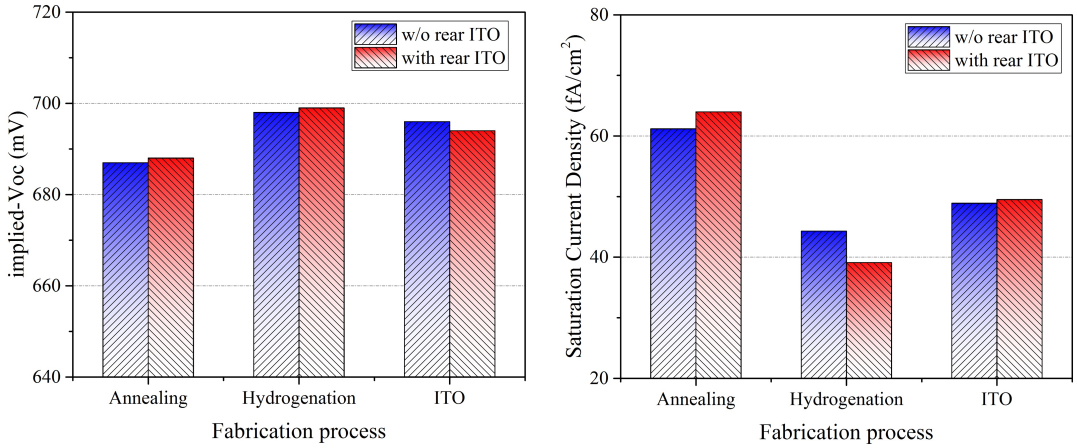


Figure **6.4**: Passivation test of the precursors with or without rear ITO.

The two samples are then compared in the solar cell performance. Firstly, the EQE responses are measured and shown in figure 6.5. As it can be observed, there is a difference in the current gain at the short wavelength of below 550 nm. This is mainly ascribed to the contamination induced during the photolithography processes, which can be eliminated with the improvement in fabrication. However, with the insertion of the rear ITO layer, the recombination (wavelength of 600-900 nm) is suppressed as is indicated by the higher EQE gain. Furthermore, the optical response of the solar cell during the long wavelength is enhanced and a slightly higher EQE can be observed. This can be explained by the fact that an additional ITO layer at the rear side with a proper thickness can enable a more effective reflection at the rear side, which will reduce the absorption of the rear metal layer and prolong the light path in the absorber, thus enabling a higher current [75].

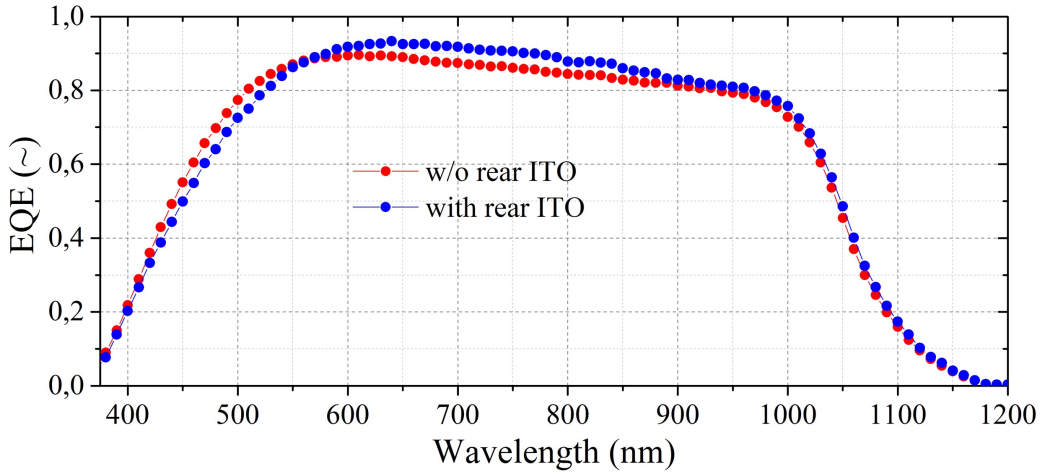


Figure **6.5**: External quantum efficiency of solar cells with or without rear side ITO.

The external parameters are shown in table 6.2, and a gain in J_{SC} of 0.4 mA/cm^2 is measured, which is corresponding to discussion above. In addition, the higher V_{OC} measured in the double side ITO cell shows that the rear contact is protected against the damage induced by the evaporation.

Table **6.2**: External parameters of the front and back contacted solar cells with different fabrication schemes.

		Area [cm^2]	**V_{OC} [mV]**	**J_{SC} [mA/cm^2]**	**FF [%]**	**η [%]**	**SunsV_{OC} [mV]**	**pFF [%]**
e-beam	With rear ITO	1	686	33.2	80.9	18.4	709	84.1
	w/o rear ITO	1	684	32.4	75.3	16.7	708	84.1
Screen printing		9	701	32.8	62.7	14.4	713	82.4

- ***Comparison of metallization schemes***

As is discussed, the metallization process is of great significance to save the passivation quality. Hence, with this motivation, solar cells are first fabricated with front and rear ITO layer, and then the e-beam Al contact on the front side is replaced with a screen-printed Ag contact. The same e-beam evaporation Al contact is applied on the rear side. To evaluate the solar cell performance, the external parameters are measured and shown

in table 6.2. Note that the passivation of this solar cell is also tracked, and before metallization, the implied V_{OC} is measured to be 702 mV. As it is observed, the measured V_{OC} of 701 mV shows almost no drop during screen printing process. However, this solar cell suffers from a significant FF (62.7%) and also pFF (82.4%) loss, which is mainly ascribed to the lateral conductivity of the screen-printed silver fingers and the relatively large cell area. The loss in FF of the cell cannot be recovered by the improvement in V_{OC}, which results in a low conversion efficiency of 14.4%. The screen printing process needs further optimization, but will not be treated in this thesis. Hence, the e-beam evaporation is still be the optimum metallization approach.

In conclusion, it is found that although additional sputter damage can be induced, this layer is beneficial to both suppressing the recombination at the interface of n^+ /metal contact and enhancing the optical response during the long wavelength of above 900 nm, which results in a higher current gain of 0.4 mA/cm^2. Furthermore, the metallization schemes are also compared, as the low FF and the low efficiency are observed in solar cells with the screen-printed silver fingers on the front side.

Hence, for the fabrication of the front side textured solar cells, the ITO layers are deposited on both the front and rear side, and the e-beam evaporation will be applied as the metallization approach.

6.2 Front side textured solar cells

Based on the optimized poly-SiO_x films and the optimum process schemes, it is possible to fabricate the front and back contacts solar cell with high conversion efficiency. As is discussed in section 6.1, the flat front surface of the solar cell can be replaced with a textured surface, by which the light trapping can be significantly enhanced. Firstly, section 6.2.1 will introduce the fabrication process of the front side textured (FST) solar cells, which is followed by the passivation test and the characterization of the fabricated cells in 6.2.2. Then in section 6.2.3, the FST is compared with the double side flat cell as well as a FST cell with front and rear poly-Si passivating contacts. Finally, to further investigate the fabrication approach, an additional LPCVD a-Si:H layer is implemented, and the fabricated solar cells are also characterized.

6.2.1 Fabrication process

The fabrication processes of the FST solar cells are summarized as follows:

1. For the bulk material, a n-type c-Si wafer (Float-Zone (FZ), <100> orientation, double side polished) with a thickness of around 280 μm is used.
2. To obtain a textured front surface, the rear side of the wafer is deposited with a PECVD silicon nitride (SiN_x) as a protected layer. Then the wafer is immersed into the Tetramethylammonium Hydroxide (TMAH) solution at the temperature of 80℃ for around 10 mins to uniformly texture the c-Si surface.
3. Then the wafer is immersed in a buffered oxide etch (BOE) solution for 15 min fully etch the SiN_x layer, which results in the front side textured bulk as shown in figure 6.6 (d). Then The wafer is processed with a standard cleaning process to remove the organic and inorganic contamination, then the native oxide is removed by a 0.55% HF dip.
4. The sample is immersed in the 69.5% HNO_3 solution at room temperature for 60 mins, which results in an ultra-thin tunnel oxide layer of around 1.4 nm.
5. The sample is then processed in the RF-PECVD chamber for the deposition of the intrinsic and doped a-SiO_x:H layers. Note that for the deposition of these two layers, the parameters are kept consistent except the doping gas flow ($[PH_3] = 0$ and $[B_2H_6] = 0$ for intrinsic a-SiO_x:H layers).
6. After the PECVD process, a high-temperature annealing at temperature at 850℃ for 30 mins is conducted to crystallize the a-SiO_x:H layers and drive in the dopants, after which a crystallized poly-SiO_x layer can be obtained.
7. Then a hydrogenation step is conducted, which combines with a PECVD SiN_x layer of 75 nm at 400 ℃ and a forming gas annealing at 400 ℃ for 30 mins.
8. Then the precursor is immersed in a buffered oxide etch solution (BHF) for 5 mins to fully remove the silicon nitride layer.
9. With a 0.55% HF dip, the samples become hydrophobic, which is prior to the ITO deposition process [43]. Then the ITO layers of around 75 nm and 120 nm are sputtered on top of n^+ and p^+ poly-SiO_x film, respectively.
10. The front side ITO layer is patterned with the positive photoresist with a photolithography process, which is followed by a 3000-nm aluminum evaporation

and a lift-off process to remove the inactive metal region together with photoresist. For the rear side, a combination of 400-nm silver (Ag), 30-nm chromium (Cr) and 2000-nm aluminum (Al) is deposited with a hard mask, which results in a full-area metal contact.

Figure 6.6 shows the schematic representations of each process discussed above, and the pictures taken in the lab for both front and rear sides of the solar cell are shown in figure 6.7 to have a clear view of the cell structure.

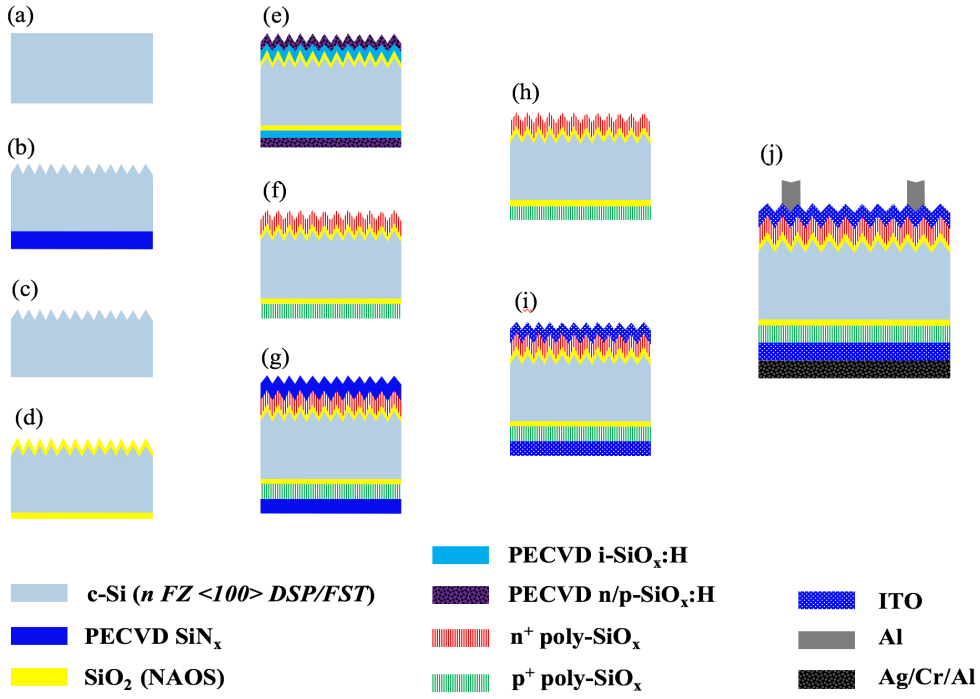
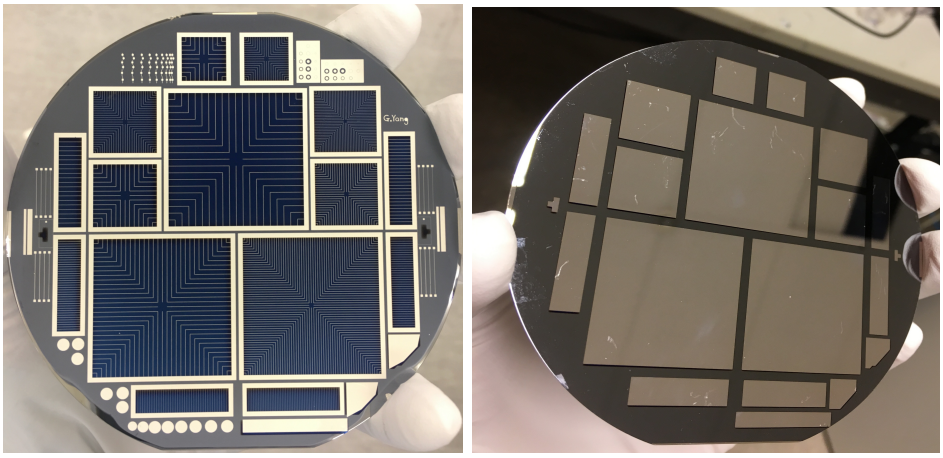


Figure **6.6**: Schematic representations of fabrication process of front and back contacted solar cell with poly-SiO_x passivating contacts.



(a) (b)

Figure **6.7**: FST solar cell with poly-SiO_x CSPCs: (a) front side. (b)rear side.

6.2.2 Solar cell characterization

- ***Passivation test***

The passivation tests during the solar cell fabrication are shown in figure 6.8. Although a low implied-V_{OC} of 673 mV was observed after the high-temperature annealing, the subsequent hydrogenation process significantly improved the precursor passivation as indicated by the high i-V_{OC} of 707 mV. The etch of the SiN_x layer induced damage to the passivated contacts, which resulted in a drop on the passivation (i-V_{OC} of 699 mV). This is mainly ascribed to the BHF etching induced damages to the poly-SiO_x materials. The following ITO sputtering induced an additional damage, and the implied-V_{OC} of 695 mV was measured.

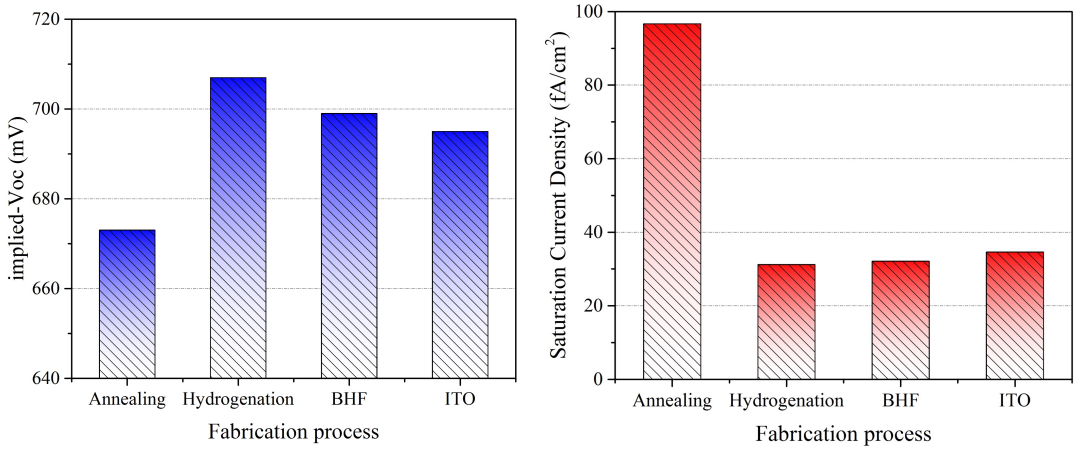


Figure **6.8**: Passivation properties of the front side textured solar cell precursor.

- ***Solar cell characterization***

In order to characterize the fabricated FST solar cells, the light J-V, external quantum efficiency, reflectance as well as the Suns V_{OC} measurements are conducted.

Table 6.3 shows the external parameters of two FST solar cells on the same wafer, where the $J_{SC,active}$ and η_{active} are obtained with a factor of the metal coverage (3.96% for cell 1 and 2.76% for cell 2) on the front side. As it is observed in both cells, the currents are significantly improved mainly because the optical response is enhanced with the textured surface on the front side. However, the solar cells again suffered from the non-optimized metallization process, and a low V_{OC} of 678 mV was measured in cell #2. The FF of 76.4% and 73.1% are measured, which are ascribed to the high series

resistance of around 0.5 $\Omega \cdot m^2$ and the recombination caused by the defects. And with the same deposition receipt, the Al layer can be about 1.73 times thinner on the texture surface, which limits the FF as well. Nevertheless, the front side textured solar cell #1 obtains a measured conversion efficiency of 20.7% and an active area efficiency of 21.5%. Indicated by the pseudo fill factor of 84.0%, the loss of the FF mainly comes from the high series resistance, and this configuration is promising to reach a higher efficiency with the improved fabrication process in a short term.

Table **6.3**: External parameters of the front side textured solar cells.

Cell	Area [cm^2]	V_{OC} [mV]	$J_{SC,active}$ [mA/cm^2]	FF [%]	η [%]	η_{active} [%]	SunsV_{OC} [mV]	pFF [%]
1	2	691	40.8	76.4	20.7	21.5	706	84.0
2	2	678	41.3	73.1	19.9	20.5	700	83.2

Figure 6.9 depicts the external and internal quantum efficiency of the solar cell #1, together with the reflectance response. Most interestingly, for a wide region from around 500 nm to 1050 nm, the cell reflectance measured Is below 10 %. This can be explained by an effective anti-reflection properties of the n^+ poly-SiO_x films integrated with the ITO layer. The IQE remains above 98% at the wavelength between 550 and 1000 nm, indicating the recombination at the front side is effectively suppressed. Last but not least, the parasitic absorption can be observed within the short wavelength with a relatively low EQE.

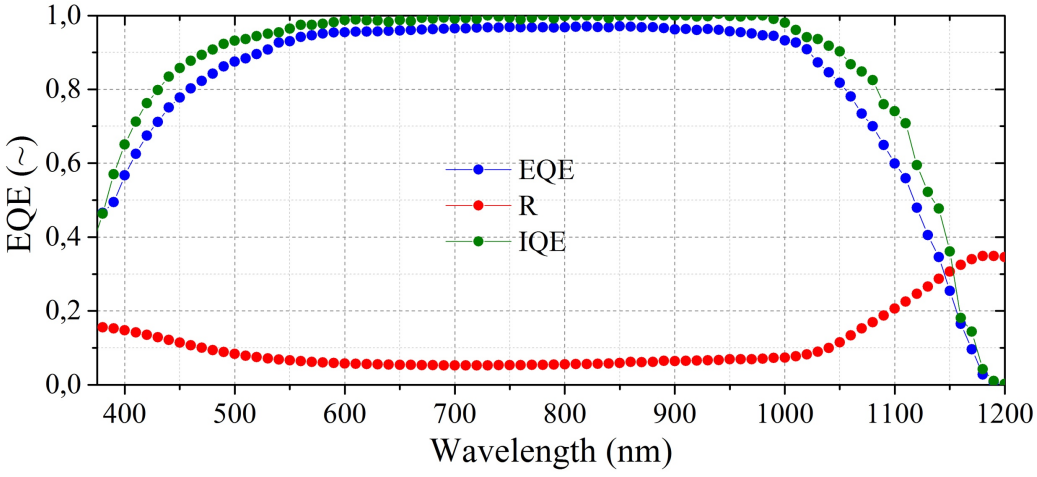


Figure **6.9**: EQE, Reflectance and IQE of the solar cell with textured front surface.

6.2.3 Optical improvements in solar cells

- ***Front side textured cell and double side flat cell***

Figure 6.10 depicts the external quantum efficiency of both the front side textured (FST) cell and the double side polished (DSP) cell, note that these cells have different front side contacts (n^+ poly-SiO_x film for FST cell and p^+ poly-SiO_x film for DSP cell). It is found that the EQE response of the FST cell is higher than the DSP cell through all the measured wavelength. This improvement is mainly attributed to the enhancement thanks to the more efficient light trapping with a front textured surface.

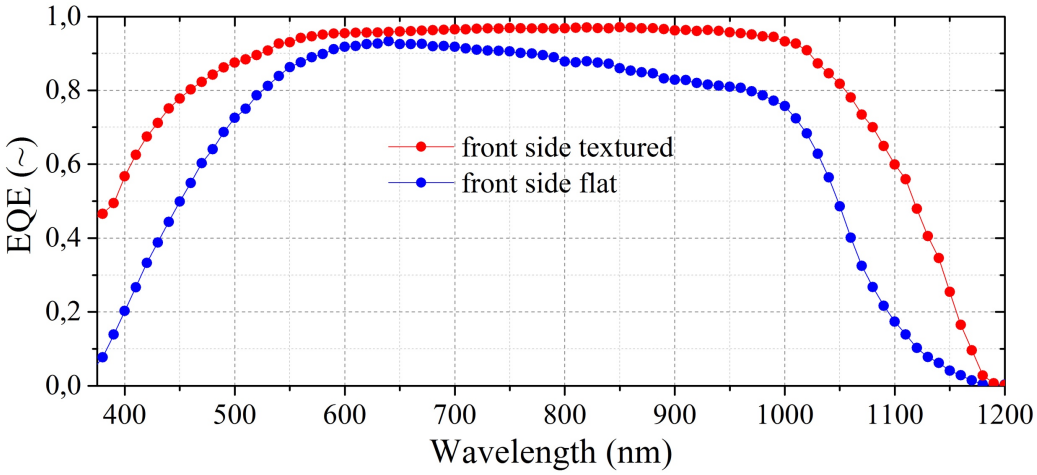
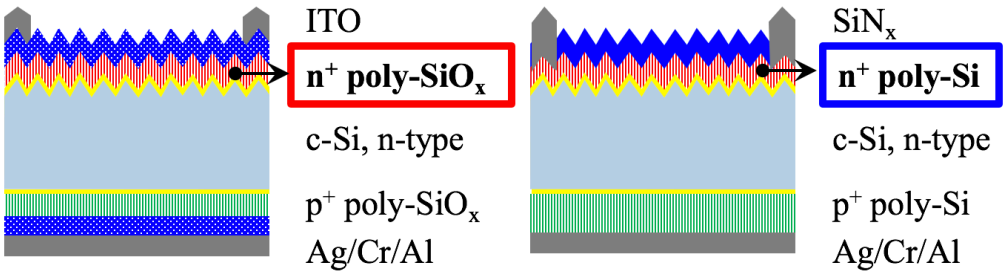


Figure **6.10**: EQE for cells with textured front surface (rear junction cell) and flat front surface (front junction cell).

- ***FBC cell with poly-SiO_x films and FBC cell with poly-Si films***

In order to compare the performance of the poly-SiO_x films with the poly-Si films in solar cells, the front and back contacted solar cell implemented with poly-Si films on both side is added as a reference, which is referred from G. Limodio et al. [76]. To have a clear comparison, the configurations of the cells are shown in figure 6.11. For the reference cell, the SiN_x layer is used as anti-reflection coating layer, and n^+ poly Si film of 35 nm is fabricated on the front side, which is directly contacted with the metal layer. For the rear side, p^+ poly-Si film of 250 nm is used, with a full area contact with the

metal stack. Note that the p^+ poly- SiO_x film on rear side is less than 20 nm.



(a) (b)

Figure **6.11**: Front and back contact solar cell with (a) with poly-SiO_x. (b) with poly-Si films as passivating contacts.

Figure 6.12 depicts the EQE response of these two cells. The main findings are: (1) Within the short wavelength of 400-600 nm, the higher cell EQE is obtained in solar cell #a, which indicates the parasitic absorption is further suppressed at the front side with a more transparent poly-SiO_x contact. (2) High EQE values are observed at the wavelength between 700 and 1000 nm for both cells, indicating a sufficient light trapping at the front side. (3) There is an enhancement within the IR wavelength in cell #a, which can be explained by that the absorption in the poly-Si passivating contacts (for cell #b) are suppressed with a more transparent and a much thinner poly-SiO_x film (for cell #a). All in all, in the configuration of front and back contacts solar cell, an enhancement in the current gain is obtained with the poly-SiO_x films implemented instead of poly-Si films.

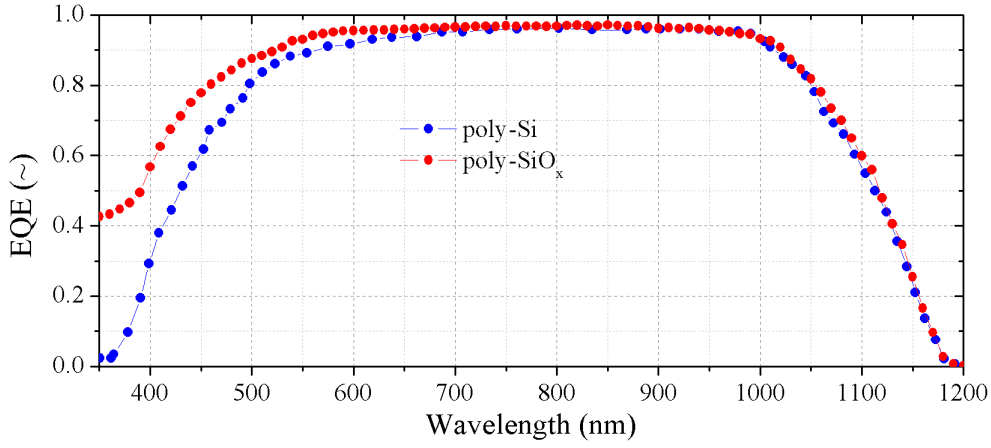


Figure **6.12**: EQE of FBC solar cells (see figure 6.11) with (1) poly-SiO_x films or (2) poly-Si films as passivating contacts.

- ***Replacement of intrinsic a-SiO$_x$:H with intrinsic a-Si:H as interlayer***

During the fabrication of poly-SiO$_x$ CSPCs, the intrinsic a-SiO$_x$:H layers are deposited by PECVD directly on the SiO_2 tunneling layer. Considering that the power density used during the PECVD process, the ultra-thin SiO$_x$ layers may be damaged by the plasma. Therefore, as a test, we replaced the PECVD intrinsic a-SiO$_x$ layer with a LPCVD intrinsic a-Si:H layer. Then the PECVD doped a-SiO$_x$ layers are used to induce dopants for the CSPCs. The different configurations are shown in figure 6.13. The same annealing and hydrogenation as used for poly-SiO$_x$ CSPCs are used as the post process.

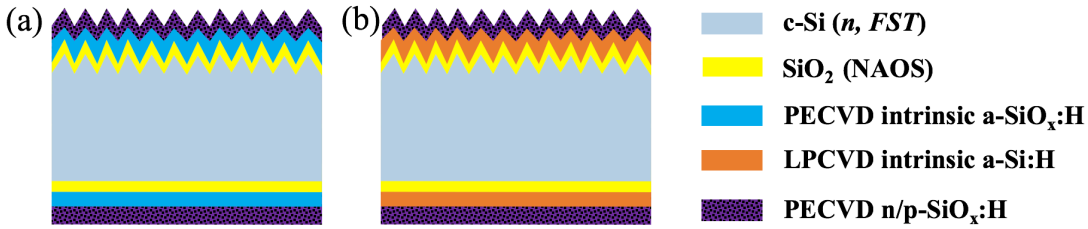


Figure **6.13**: Schematic sketch of the different intrinsic layer. (a) PECVD a-SiO$_x$:H layer. (b) LPCVD a-Si:H layer.

Figure 6.14 depicts the passivation properties of two different solar cell precursors before metallization: Precursor #1: the precursor of the solar cell #1 shown in table 6.3, which is fabricated with a PECVD intrinsic a-SiO$_x$:H layer. Precursor #2: the test precursor fabricated with a LPCVD intrinsic a-Si:H layer. Compared with precursor #1, precursor #2 shows inferior passivation after each treatment. Especially after the high-temperature annealing, a low implied-V_{OC} of 650 mV and a too high J_0 of 254 fA/cm^2 were measured. Although the passivation was improved by the subsequent hydrogenation treatment (implied-V_{OC} of 694 mV and J_0 of 59.3 fA/cm^2), the passivation was strongly influenced by the BHF etching and the ITO sputtering, with the implied-V_{OC} drop of 12 mV and 10 mV, respectively, which is mainly ascribed to the induced chemical and sputter damage during these processes. As a result, the passivation of precursor #2 (implied-V_{OC} of 672 mV and J_0 of 128 fA/cm^2) was much lower than precursor #1 (implied-V_{OC} of 695 mV and J_0 of 34.6 fA/cm^2), which indicates that the LPCVD intrinsic layer is more sensitive to the above-mentioned post

process.

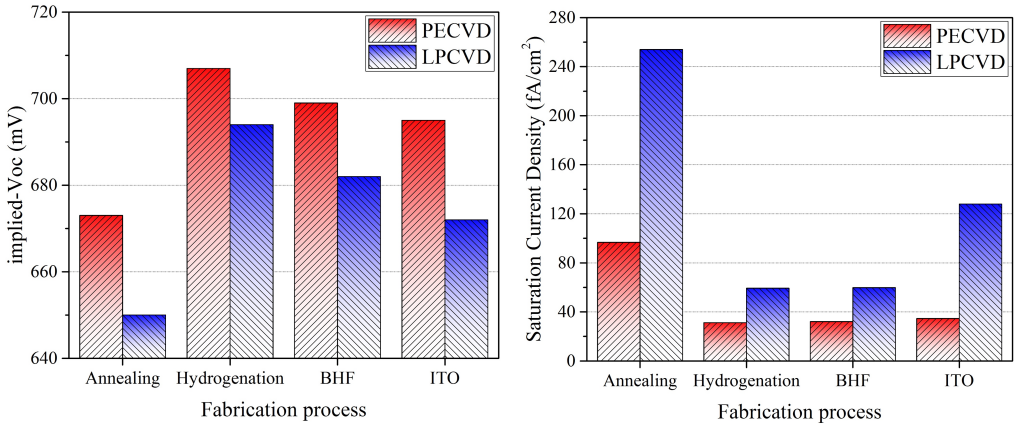


Figure **6.14**: Passivation properties of the front side textured solar cell precursors with PECVD intrinsic a-SiO_x:H layer or LPCVD intrinsic a-Si:H layer.

After the metallization process, the external parameters of the fabricated cells are measured, which are shown in table 6.4. The main findings are summarized as follows:

(1) There is a current loss as is measured with a lower $J_{SC,active}$ of below 40 mA/cm^2. This can be explained by that the a-Si:H layer may decrease the transparency of the passivating contacts, thus increasing the parasitic absorption of the films [23].

(2) With replacement of the LPCVD intrinsic a-Si:H layer, an improvement in FF can be observed, this can be possibly explained by that the poly-Si films are more conductive compared with poly-SiO_x films.

(3) Most interestingly, the conversion efficiencies of 20.2% were measured in a large solar cell (9 cm^2), featuring a FF of 80.6%. This indicates that the LPCVD intrinsic a-Si:H layer can be implemented in solar cell fabrication when the fabrication process is further optimized.

(4) Nevertheless, a PECVD intrinsic layer is still preferred since both the passivation and the current gain with the PECVD intrinsic a-SiO_x:H layer are significant, and there is also a risk of inducing contamination during the additional process.

Table **6.4**: External parameters of the front side textured solar cells #1 and #2 implemented with LPCVD intrinsic a-Si:H layer. Cell #3 is the same as Cell #1 in table 6.3 with a PECVD a-SiO_x:H layer.

Cell	Area [cm^2]	V_{OC} [mV]	$J_{SC,active}$ [mA/cm^2]	FF [%]	η [%]	η_{active} [%]	SunsV_{OC} [mV]	pFF [%]
1	2	675	39.8	79.3	20.5	21.3	676	83.1
2	9	659	39.2	80.6	20.2	20.8	669	83.6
3 Ref	2	691	40.8	76.4	20.7	21.5	706	84.0

6.3 Conclusion

In this chapter, the optimized poly-SiO_x films are applied in solar cells. The fabrication process is first optimized with the double side flat configuration. With the poly-SiO_x passivating contacts implemented, a 19.0 % solar cell featuring an excellent FF of 83.5% is obtained, which shows an efficient carrier transport. Based on the characterization and comparison of solar cells with different process schemes, a combination of double side ITO and e-beam metal evaporation are selected for the fabrication of front side textured cells. Consequently, a front side textured cell was successfully fabricated with a V_{OC} of 691 mV, $J_{SC,active}$ of 40.8 mA/cm^2 and a FF of 76.4%, which result in an active area conversion efficiency of 21.5%. This cell improved the current gain compared with the double side flat cell due to the texturing induced anti-reflection. Compared to the same cell architecture but with poly-Si as CSPCs, the suppressed the absorption due to the poly-Si CSPCs in the front side of cell also shows the superior of poly-SiO_x material with respect to the poly-Si. Finally, the LPCVD intrinsic a-Si:H layer is implemented to replace the PECVD intrinsic a-SiO_x:H layer. It is found to have more current loss due to the higher absorption of poly-Si layer. Although the low V_{OC} is observed due to the non-optimized process, a conversion efficiency of 20.2% was measured featuring a FF of 80.6 % in a 9 cm^2 large solar cell.

7

Conclusions and outlook

7.1 Conclusions

The objectives of this thesis are to first optimize the poly-SiO_x passivating contacts, and then fabricate high-efficiency solar cells with the implementation of the optimized poly-SiO_x passivating contacts. The main achievements during the thesis can be summarized as follows:

- ***1. Optimized n^+ and p^+ poly-SiO_x passivating contacts***

To achieve the first objective of an optimized poly-SiO_x passivating contact, related deposition parameters during the fabrication of this passivating contacts are investigated. For the material properties optimization, the PECVD deposition parameters such as oxygen content, doping gas flow and the layer thickness are investigated under the same annealing temperature at 850 ℃ considering the thermal stability of the tunnel oxide layer. Taking both optical and electrical properties into account, it was found that the best passivation properties can be obtained with the oxygen content $R_{oxygen,n}$ of 0.62 and $R_{oxygen,p}$ of 0.38, the doping gas flow $R_{doping,n}$ of 0.55 and $R_{doping,p}$ of 0.38, the doped layer thickness of 20 nm and 10 nm for n^+ and p^+ passivating contacts, respectively. Then the influence of the high-temperature annealing parameters combined with the hydrogenation schemes are investigated. It was found that with a thermal budget of 850 ℃ for 30 mins, and a hydrogenation scheme combined with PECVD SiN_x layer as the hydrogen effusion barrier and a forming gas annealing at 400 ℃ for 30 mins, the best passivation properties can be obtained. Based on the passivation optimization in this thesis work, for the n^+/n passivating contacts on flat surface, the best passivation with an implied-

V_{OC} of 727 mV and a J_0 of 2.4 fA/cm^2 were obtained, which also shows high thermal stability and a very wide process window from 850 ℃ to 950 ℃. While the best implied-V_{OC} of 723 mV and a J_0 of 6.9 fA/cm^2 were measured for n^+/n passivating contacts on textured surface. In the case of p^+/n passivating contacts, the optimized contact shows an implied-V_{OC} of 709 mV and a J_0 of 13.9 fA/cm^2.

- ***2. Excellent carrier collection***

Based on the achievement of the first objective on passivation, the optimized poly-SiO_x passivating contacts are obtained, which were applied in the fabrication of high-efficiency solar cell in order to achieve the second objective. The first FBC solar cell of this work was fabricated with a double side polished bulk material, and the p^+ poly-SiO_x passivating contact and the n^+ poly-SiO_x passivating contact were deposited as the front side emitter the back-surface field, respectively. With a front side ITO layer to enhance the carrier transport and to reduce the front side reflection, a conversion efficiency of 19.0% featuring an excellent fill factor of 83.5% was obtained. This shows a very efficient charge carrier transport and collection through the poly-SiO_x passivating contacts, the ITO layer and the metal.

To further optimize the fabrication process, an additional rear side ITO layer was implemented, which showed a higher current gain with a higher EQE at the long wavelength thanks to the reduce in recombination as well as the enhancement of reflection at the rear side. In order to preserve the passivation after metallization and enable a higher V_{OC}, the screen-printed sliver was also applied in the front side metal patterning instead of e-beam evaporation aluminum, which resulted in a solar cell V_{OC} of 701 mV. However, the significant loss in FF (62.7 %) was observed.

- ***3. Front side textured FBC solar cell with 21.5% efficiency***

In order to finally achieve the second objective of fabricating high-efficiency solar cells with poly-SiO_x passivating contacts, the FBC solar cells were fabricated with a front side textured bulk material. The n^+ poly-SiO_x passivating contact and the p^+ poly-SiO_x passivating contact were deposited as the front-surface field and the rear emitter, respectively. By integrating the double side ITO layers, a 3-μm front side Al metal and a combination of Ag/Cr/Al (400/30/2000 μm) as the back reflector, an active area conversion efficiency of 21.5% was obtained in a 2-cm^2 solar cell. Such high efficiency

highlights the properties of the configuration: (1) Although the solar cell suffered from the passivation loss during the fabrication, especially during the ITO sputtering and the metallization, a V_{OC} of 691 mV was measured. (2) Thanks to the textured front surface, the ITO layers and the transparent and thin poly-SiO_x passivating contacts, an effective light trapping on the front side and a low parasitic absorption within the passivating contacts were enabled, which resulted in a high $J_{sc,active}$ of 40.8 mA/cm^2. (3) A FF of 76.4 % was measured, indicating the efficient carrier transport through the passivating contacts and the ITO layers as well as the effective carrier collection at the metal contacts. Nevertheless, the pFF of 84.0% and a relatively high series resistance of 0.5 $\Omega \cdot m^2$ shows a big room for improvement with a further optimized fabrication process.

Comparison was made between two FBC solar cells with poly-SiO_x passivating contacts and with poly-Si passivating contacts, respectively. It was found that with the same thickness of the n^+ passivating contact as the front surface field, a higher EQE during the short wavelength of 400-600 nm is measured thanks to the lower parasitic absorption of the n^+ poly-SiO_x film at this wavelength region. By implementing the higher bandgap poly-SiO_x films, thinner layer can be deposited at the rear side while preserving the passivation, thus featuring a lower absorption at the rear passivating contact. Due to a lower free carrier absorption at the long wavelength, a higher current gain was measured in solar cell with poly-SiO_x films compared to solar cell with poly-Si films.

Furthermore, the influence of the intrinsic a-SiO_x:H layer on the solar cell performance was investigated by replacing it with a LPCVD intrinsic a-Si:H layer. As a result, the solar cell with the a-Si:H layer suffered from the significant passivation loss during the fabrication, and a current loss was observed due to the higher absorption coefficient of the LPCVD intrinsic layer. Nevertheless, a conversion efficiency of 20.2 % was measured in a large cell (9 cm^2) featuring a high FF of 80.6%.

7.2 Outlook

According to the loss analysis performed by Yoshikawa et al. [77], the theoretical conversion efficiency limit for a single solar cell is calculated to be 29.1%, with a V_{OC} of 752 mV, a J_{SC} of 43.7 mA/cm^2 and a FF of 88.5 %. Compared with the best solar

cell obtained in this work, there is a big room (15.8% in FF, 11.5% in J_{SC} and 8.8% in V_{OC}) for the improvement. Here we give the following suggestions for the fabrication of higher efficiency solar cells based on poly-SiO_x passivating contacts:

- ***Optimization of ITO deposition to improve V_{OC} and FF***

It was found in this work that the sputtering of the ITO layer invoked a significant loss on the surface passivation of the poly-SiO_x passivating contacts, which strongly reduced the V_{OC} of the solar cell fabricated. This damage is also reported in the previous work of other groups [25] [73] [74]. In order to protect the surface passivation against the sputter damage and enable a high V_{OC}, a thin layer inserted with a softer deposition like atomic layer deposition (ALD) can be applied as it is implemented by [78]. Furthermore, It is found that a large work function misalignment of the a-Si:H layer and the ITO layer leads to a Schottky barrier, which limits the FF of the solar cell [79]. Hence, the above-mentioned insertion layer should also have a low (high) work function to make good contacts with the n^+ (p^+) passivating contacts. With this buffer layer, the ITO layers can be deposited with higher transparency and lower resistivity [20]. For instance, F. Feldmann et al. investigated the ALD deposited AZO contact layers for n-TOPCon. With the deposition of a AZO/ITO stack instead of a single ITO layer on the poly-Si passivating contact, they demonstrated a FF increase of 1% at solar cell level. Hence, the ITO deposition can be further optimized to improve the V_{OC} and FF of the solar cells with poly-SiO_x passivating contacts.

- ***Optimization of metallization to improve V_{OC} and FF***

It was found in this work that the solar cells suffer from the damage on surface passivation during the e-beam evaporation process on the front side, and a loss in V_{OC} is significant. The screen printing process was applied in this work and proved to better preserve the passivation thus enabling a higher V_{OC}. Furthermore, with the optimization of the screen printing and the electroplating techniques in PVMD group, the more conductive and thicker metal layer such as silver and copper can be applied on the front side, which can benefit the FF of the solar cell [80].

- ***Double layer anti-reflection coating (ARC) to improve the J_{SC}***

To minimize the external reflection of the front side, a double layer anti-reflection

coating can be applied. The ITO layer on the front side can be capped with an additional layer such as SiO_2 or MgF_2 with a proper selection of the thickness, the average reflectance can be reduced from 8.19% to 5.4% as it was measured in the PVMD group [64].

- ***Implementation of the poly-SiO_x passivating contacts into IBC configurations***

As is reported in [24, 38], the significant reduce of the absorption coefficient of poly-SiO_x films at longer wavelength indicates the possibility to implement poly-SiO_x passivating contacts into the IBC configuration, which can avoid the current loss due to the shading of the front side metal fingers as well as the parasitic absorption within the short wavelength. Therefore, a higher J_{SC} can be obtained. Furthermore, it was found in this work that so far, the n^+ poly-SiO_x passivating contacts show better passivation on the flat surface, with the IBC configuration, the n^+ contacts can be deposited on flat surface, thus enabling a higher V_{OC}.

Acknowledgement

One year ago, I joined the match up meeting organized by PVMD group. Thanks to the invitation sent by Dr. Olindo Isabella during the PV system lecture, here I met many passionate researchers on photovoltaics, and decided to make my own contribution to the c-Si group. The first three-month SIP2 project was of great fun and I continued with the same topic in my thesis work. I am so fulfilled now because I am inspired to put myself in photovoltaics, no matter if I go on with research or go to industry.

First of all, I would like to thank my supervisors, Olindo and Guangtao, for the instructions you gave with great patience. Your valuable suggestions on the experiments and theoretical analysis on the results guided me into the right direction towards the final target of the thesis. Besides, I would like to thank Gianluca and Paul, the discussions with you were valuable and interesting. You are always willing to share your solid knowledge on semiconductor, and I am so proud of being your team member. I would also like to express my gratitude to all the other PVMD group members for the help you gave, as I will never forget Martijn was always busy fixing Amor, and Steffan was busy with the EQE setup.

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我爱你们！

Peiqing Guo

TU Delft, May 2018

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Poly-crystalline silicon-oxide films as carrier-selective passivating contacts for c-Si solar cells

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The poly-Si carrier-selective passivating contacts (CSPCs) parasitically absorb a substantial amount of light, especially in the form of free carrier absorption. To minimize these losses, we developed CSPCs based on oxygen-alloyed poly-Si (poly-SiO_x) and deployed them in c-Si solar cells. Transmission electron microscopy analysis indicates the presence of nanometer-scale silicon crystals within such poly-SiO_x layers. By varying the O content during material deposition, we can manipulate the crystallinity of the poly-SiO_x material and its absorption coefficient. Also, depending on the O content, the bandgap of the poly-SiO_x material can be widened, making it transparent for longer wavelength light. Thus, we optimized the O alloying, doping, annealing, and hydrogenation conditions. As a result, an extremely high passivation quality for both n-type poly-SiO_x ($J_0 = 3.0$ fA/cm^2 and iVoc = 740 mV) and p-type poly-SiO_x ($J_0 = 17.0$ fA/cm^2 and iVoc = 700 mV) is obtained. A fill factor of 83.5% is measured in front/back-contacted solar cells with both polarities made up of poly-SiO_x. This indicates that the carrier transport through the junction between poly-SiO_x and c-Si is sufficiently efficient. To demonstrate the merit of poly-SiOx layers' high transparency at long wavelengths, they are deployed at the back side of interdigitated back-contacted (IBC) solar cells. A preliminary cell efficiency of 19.7% is obtained with much room for further improvement. Compared to an IBC solar cell with poly-Si CSPCs, a higher internal quantum efficiency at long wavelengths is observed for the IBC solar cell with poly-SiO_x CSPCs, thus demonstrating the potential of poly-SiO_x in enabling higher J_{SC}. *Published by AIP Publishing.*
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Nowadays, the highest conversion efficiencies in crystalline silicon (c-Si) solar cells are enabled by quenching minority carriers' recombination velocity at the c-Si/contact interface by means of carrier-selective passivating contacts (CSPCs). These are technologies based on, for example, a-Si:H (Silicon Heterojunction, SHJ),[1–4] doped poly-Si alloys,[5–7] and metal-oxides.[8–10] Both SHJ and poly-Si technologies have recently led to a world record, >26% interdigitated back-contacted (IBC) solar cells.[11,12] CSPCs based on metal-oxide layers, such as MoO_x and TiO_x, are also rapidly emerging and enable efficiencies beyond 22%.[8,10] Nevertheless, there are still restrictions that limit the applications of such materials in the photovoltaic (PV) industry: (i) poly-Si CSPCs are not transparent, especially when heavily doped, because of the high free carrier absorption (FCA); (ii) metal-oxides are transparent, but since standard high-thermal budget metallization influences their work function, their carrier selectivity and contacting properties may worsen; and (iii) limited transparency and thermal instability also hold in SHJ cells. In fact, parasitic absorption in the amorphous layers results in lower Jsc, and commonly used high-temperature contact firing will be detrimental for the cell efficiency. Therefore, materials such as poly-SiO_x (Refs. 13–16) or crystallized SiC_x (TOPCon concept)[5,17] have been proposed as CSPCs for solar cell applications. Both SiO_x and SiC_x alloys exhibit high thermal stability in passivation. At the same time, they are more transparent than the poly-Si material due to their larger bandgap. For example, by varying the content of oxygen atoms in the poly-SiO_x materials, which will widen the optical bandgap of the material, the transparency of the resulting poly-SiO_x increases. Simulation results suggested that by replacing the poly-Si with high bandgap poly-SiO_x layers within the cells, strong band bending is attainable at the c-Si/poly-SiO_x interfaces. This is mainly due to the enhanced built-in voltage at the n/p^+ interface, when the p^+ poly-Si is replaced by the wider bandgap p^+ poly-SiO_x layer (increasing the valence band energy). Therefore, an improved carrier selectivity is expected. Moreover, by engineering the in-diffused doping profile at the c-Si/poly-SiO_x interface, which enhances the carrier lateral transport, the applications of transparent conductive oxides (TCO) layers for carrier extraction can be avoided.[16]

In this letter, we show the development of highly transparent, high-temperature stable poly-SiO_x CSPCs and their applications in various cell architectures. They are prepared by alloying oxygen within a thin a-Si:H film during the thin-film silicon deposition by plasma enhanced chemical vapor deposition (PECVD). After high-temperature annealing, these amorphous films become poly-crystalline. The deposition conditions and their influences on the optical and electrical properties of the materials are here discussed. As demonstrators, the developed materials are then deployed in front/back contacted (FBC) and IBC cells.

For all the experiments performed in this work, we used n-type Float Zone (FZ) c-Si wafers (thickness: 280 ± 20 μm thick, orientation: ⟨100⟩, and resistivity: 1–5 Ω cm). Focusing