High-Performance Operational and Instrumentation Amplifiers

High-Performance Operational and Instrumentation Amplifiers

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To the Loving Memory of My Late Father, Seyed Mohammad Hasan Shahi
(Apr. 1, 1924 – Oct. 11, 2011)

The schematic on the cover page represents a simplified block diagram of a patented design for Maxim Integrated Products, Sunnyvale, California. MAX4208 / MAX4209 were awarded "The Product of the Year" in 2008 by EN-Genius NETWORK under the category of "The Most Innovative Instrumentation Amplifier".

Table of Contents

Summary 9

Chapter 1: Introduction 9

Chapter 2: Review of Major Error Sources in Op-Amps and Inst-Amps 9

Chapter 3: Techniques to Reduce Offset Error 10

Chapter 4: Dynamic Offset-Cancellation Techniques; Auto-Zeroing: a sampling Technique 10

Chapter 5: Dynamic Offset-Cancellation Techniques; Chopping: a Modulation-Based Approach 10

Chapter 6: Realization 10

Samenvatting 12

1. Introduction 15

1.1 Motivation 15

1.1.1 The Need for Amplifiers in Electronic Sensing and Control 16

1.1.2 Major Requirements of Precision Gain Blocks for Sensors 20

1.2 Challenges with the Three Op-Amp Instrumentation Amplifier as a Conventional Gain Block for Sensors 20

1.2.1 Summary of the Disadvantages Associated with the Three Op-Amp Structure 24

1.3 A Review of Conventional Current Feedback Instrumentation Amplifiers (Conventional CFIAs) 25

1.3.1 Performance Limitations of Conventional CFIA Topology 28

1.4 Challenges with Designing Precision Amplifiers in CMOS Technology, and the Aim of this Thesis 29

1.5 Organization of this Thesis 30

2. Review of Major Error Sources in Op-Amps and Inst-Amps 32

2.1 Background 32

2.2 Major Error Sources in Op-Amps and Inst-Amps 32

2.2.1 Definition of Offset Error 34

2.3 The Origin of the Offset Error in CMOS Op-Amps and Inst-Amps 35

2.3.1 The Effect of Random Process Variations on Offset 36

2.3.2 Drain Current Mismatch and the Consequent Offset Error 39

3. Techniques to Reduce Offset Error 42

3.1 Conventional Approaches to Reduce Offset 42

3.1.1 Offset Trimming at Source Degeneration Resistors of the Input Differential Pair Transistors 43

3.1.2 Offset Trimming by Size Adjustments $\Delta W/L$ of the Input Differential Pair Transistors 44

3.1.3 Offset Trimming at Source Degeneration Resistors of Current Mirror Load or Folded Cascode 45

3.1.4 Offset Trimming by Changing the Load Current Sources at the Drain/Source of the Input Differential Pair Transistors 46

3.1.5 Offset Trimming by Addition of a Trimmable Current to One Side of the Loads of a Differential Pair Transistors 46

3.2 Trimming Step within the Production Flow 47

3.2.1 Wafer-Sort Trimming (WST) and Associated Techniques 47

3.2.1.1 Advantages and Disadvantages of WST 49

3.2.2 Post-Package Trimming (PPT) and Associated Techniques 50

3.2.2.1 Advantages and Disadvantages of PPT 52

3.3 Dynamic Offset Cancellation (Real Time Offset Removal) 53

3.3.1 General Advantages of Dynamic Offset Cancellation (DOC) Techniques 53

3.4 A Short Review of Accuracy Errors in Inst-Amps 54

3.5 A Practical Note on Over-Temperature Performance Assurance and Misinterpretation of Performance Guaranteeing Term GBD 58

4. Dynamic Offset-Cancellation (DOC) Techniques: Auto-Zeroing, A Sampling Based Approach 61

4.1 Auto-Zeroing: A Sampling and Storage Based Technique 61

4.1.1 Output Offset Storage (OOS) 62
4.1.1.1 Advantages and Disadvantages of Output Offset Storage (OOS) 65

4.1.2 Input Offset Storage (IOS) 66
4.1.2.1 Advantages and Disadvantages of Input Offset Storage (IOS) 68

4.1.3 Using an Auxiliary Amplifier in a Closed Loop Configuration 69
4.1.3.1 Advantages and Disadvantages of Using Auxiliary Amplifiers 72

4.1.4 Ping-Pong Configuration 73
4.1.4.1 Advantages and Disadvantages of the Ping-Pong Configuration 74

4.1.5 Self-Calibration or Digital Offset Storage and Control Technique 75
4.1.5.1 Advantages and Disadvantages of Self-Calibration 75

4.1.6 Auto Calibration (Digital Signal Processing Approach) 76
4.1.6.1 Advantages and Disadvantages of the Digital Signal Processing Approach 77

5. Dynamic Offset Cancellation Techniques: Chopping, A Modulation Based Approach 78

5.1 Basic Chopper Operation 79

5.2 Chopper Techniques 82

5.2.1 Conventional Chopper Techniques 82
5.2.1.1 Challenges with Conventional Chopper Techniques 84

5.2.2 Nested Chopper Techniques 85
5.2.2.1 Application Challenges with Nested Chopper Techniques 88

5.2.3 Chopper Techniques with Auto-Zeroing 89

5.2.4 Chopper-Stabilized Techniques 90
5.2.4.1 Challenges with Chopper-Stabilized Technique and Ways to improve the Design 91

5.2.5 Chopper-Stabilized Chopper Techniques 92

5.2.6 Chopper Stabilized Auto-Zeroed Chopper Techniques 94

5.3 Chopper-Stabilized Chopper Inst-Amps Utilizing Indirect Current Feedback Topology 94

5.4 Chopper-Stabilized Auto-Zeroed Chopper CFIA Development 94

5.4.1 Removal of the Input-Referred offset due to the Offset of the Input Transconductances of the High-Frequency path (G_{m7} and G_{m8}) 97

5.4.2 Input-Referred offset due to the offset of the Input Transconductances of the Low-Frequency Path (Gm_5 and Gm_6) 99
5.4.2.1 Offset Removal of the Input Transconductances of the Low-Frequency Path (Gm_5 and Gm_6) 102

5.4.3 Input-Referred Offset due to the offset of the Integrator Block (G_{m4}) 104
5.4.3.1 Offset Removal of the Integrator Block (G_{m4}) 105

5.4.4 Input-Referred Offset due to the Weak transconductance (G_{m3}) 106

5.4.5 Input-Referred offsets due to the offset of the Integrator Gm_9 107
5.4.5.1 Offset Removal of the Integrator Gm_9 108

5.4.6 Input-Referred offset due to the offset of the Sense Amplifier G_{m14} 108
5.4.6.1 Offset Removal of the Sense Amplifier G_{m14} 111

5.4.7 Input-Referred offset due to the offset of the Integrator G_{m15} 111
5.4.7.1 Offset Removal of the Integrator G_{m15} 111

5.4.8 Effects of the offset of the Transimpedance G_{m2} on V_{out} Spikes 112
5.4.8.1 Offset Removal of the Transimpedance G_{m2} 113

5.4.9 Summary of the Effects of Different Transconductance Native Offsets, along with other parameters on the Input-Referred Offset 113

5.4.10 Overcoming Frequency Compensation Issues Caused by the Existence of a Two-Path Amplification 116

6. Realization 118

6.1 Top-Down versus Bottom-Up Design Approaches 118

6.2 Top-Down Design Steps and considerations 120

6.3 Process Technology Considerations 123

6.4 Top-Down Model-Based Design of the Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifier 125

6.4.1 General Specifications of the CFIA design 128

6.4.2 Model-Based Design of the Output Stage and Frequency Compensation Network 129

6.4.3 Model-Based Design of the Input Stage Transconductances, and their First-Level Offset Cancellation loop 131

6.4.4 Model-Based Design of Higher-Level Offset Cancellation Loops 134

6.4.5 Simulation Results for the Model-Based Design of CFIA 138

6.5 Transistor-Level Design of the CFIA in CMOS Technology..... 142

6.5.1 Basic Process Parametric Specifications 142

6.5.2 Transistor-Level Design of Output stage G_{m1} and the Frequency Compensation Network in CMOS Technology 143

6.5.3 Transistor-Level Design of the Driver Stage G_{m2} and the Push-Pull Translinear Bias 145

6.5.3.1 Transistor-Level Design of the Output Over-Current Protection Circuitry within G_{m2} block.....146

6.5.4 An Introduction to the Design of Accurate High-Gain Transconductance Blocks149

6.5.4.1 V-I Converters and prior Arts [35] 149

6.5.5 Transistor-Level Design of High-Gain, Accurate Input and Feedback Transconductance blocks G_{m7} and G_{m8}.....155

6.5.5.1 Gain Setting Options in CFIA Design 158

6.5.5.2 General Trim Considerations in Precision Analog Design.....159

6.5.5.3 Sources of Errors Contributing to Gain Error in CFIA Designs.....160

6.5.5.4 Gain-Error Trim Range and Resolution for the CFIA Design of this Thesis 161

6.5.5.5 Gain-Error Trim Implementation for the CFIA Design of this Thesis 162

6.5.5.6 Estimation of Trim-Links Branch-Off Points at Degeneration Resistors.....163

6.5.6 Transistor-Level Design of the Integrator G_{m4} 166

6.5.6.1 Transistor-Level Designs of the Integrators G_{m9}, G_{m12}, G_{m15}, G_{m18}, G_{m21}, and G_{m23} 167

6.5.7 Transistor-Level Design of G_{m5} and G_{m6} Sense Amplifiers 167

6.5.8 Transistor-Level Design of the Summing Circuits SUM_2 and SUM_4 171

6.5.9 Transistor-Level Design of the Weak Transconductance G_{m3}.....172

6.5.10 Transistor-Level Design of G_{m10}, G_{m13}, G_{m19}, G_{m22}, *and* G_{m24}, ...172

6.5.11 Transistor-Level Design of the Bias Circuitry (Simplified) 175

6.5.12 Transistor-Level Design of the Oscillator Circuit (Simplified).....177

6.5.13 Simulation Results for the Transistor-Level Design of CFIA 179

6.5.13.1 Comparison between the Simulation Results of the Model-Based Design and the Transistor-Level Design.....179

6.6 Measurement Results 184

6.6.1 Input-Referred offset for Model-Based Simulations, Transistor-Level Simulations, and Silicon Measurements 184

6.6.2 Bench Measurements of the Accuracy , DC, and AC Parameters 184
6.6.2.1 Accuracy Parameters 185
6.6.2.2 DC Parameters 185
6.6.2.3 AC Parameters 186

6.6.3 Histograms of Accuracy Parameters 186
6.6.3.1 Input-Referred Offset Voltage Histogram 186
6.6.3.2 Gain Error Histogram 187

6.6.4 Bench Measurement Results Showing Typical Operating Curves (TOC's) for Offset vs. Input Common-Mode and Supply Voltages 187
6.6.4.1 Input-Referred Offset vs. Input Common-Mode Voltage 188
6.6.4.2 Input-Referred Offset vs. Supply Voltage 188

7. Conclusions and Improvements 189

7.1 Conclusions 189

7.1.1 Improvements Offered by the Chopper-Stabilized Auto-Zeroed Chopper Inst-Amps 190

List of Patents 192

List of Early Publications 192

Awards 192

About the Author 193

Acknowledgements 194

List of References 197

List of Figures 200

List of Tables 205

Summary

This subsection describes a summary of the materials presented in each chapter.
Chapters one to four are presented as a foundation, as well as a description of the prior arts and techniques for the patented work of this thesis. These chapters are not part of the work of this thesis. They are presented to provide an overview of the history of the prior art, and to help understand the need for improvements. Advantages and disadvantages of such techniques are presented, with the latter leading to the development of the work of this thesis.

Chapters five and six are entirely devoted to the work of this thesis. Throughout these chapters, the reader is frequently referred to the background chapters to either show a drawback in the existing prior art, or to conduct a comparative evaluation to prove an advantage of the new technique over the previous methods.

A more detailed description of the contents and purposes of each chapter are presented below.

Chapter 1: Introduction

In this chapter we discuss the need for amplifiers in sensing and control electronics. The major requirements of such precision gain blocks are brought forward. Challenges with the older gain enhancement techniques such as the "Three Op-Amp Instrumentation Amplifier", along with its benefits and drawbacks are discussed.

Conventional "Current-Feedback Instrumentation Amplifiers" (CFIAs) are mentioned as the most popular configurations to construct Instrumentation Amplifiers (Inst-Amps). The performance limitations of this widely-used conventional technique are also reviewed throughout this chapter.

Challenges of designing precision amplifiers in CMOS technology are discussed next.

Chapter 2: Review of Major Error Sources in Op-Amps and Inst-Amps

This chapter deals with the major error sources in Op-Amps and Inst-Amps. The voltage offset error and its origin in CMOS based Op-Amps and Inst-Amps are discussed. Fabrication variables such as the effects of random process-parameter variations, as well as the drain-current mismatches and their consequential offset errors are highlighted.

Chapter 3: Techniques to Reduce Offset Error

Conventional techniques to reduce offset errors such as trimming and their associated techniques are discussed in this chapter. Major trim techniques at different steps of chip development such as Wafer-Sort Trimming (WST) and variety of different Post-Package Trimming (PPT) options are presented in this chapter. The advantage and disadvantages of all such techniques are discussed to better understand the issues in-hand.
Some industry-accepted terminology and standards relevant to the subject are covered here.

Chapter 4: Dynamic Offset-Cancellation Techniques; Auto-Zeroing: a sampling Technique

This chapter is concerned with "Auto-Zeroing" as a special class of dynamic offset cancellation, which is based on sampling techniques. A variety of different circuits with their major benefits and drawbacks is discussed in this chapter. Later on and in the following chapters it is shown that the "Auto-Zeroing" technique is partly employed in the design associated with the work of this thesis.

Chapter 5: Dynamic Offset-Cancellation Techniques; Chopping: a Modulation-Based Approach

Techniques discussed here belong to a second category of real-time offset-cancellation methods, that is, chopping. It is about techniques which are based on modulation as opposed to sampling to remove the offset dynamically, or in real time.

In this chapter the approach presented by the work of this thesis is gradually but thoroughly described from a system-level perspective. This is done by developing and improving on the prior art. To better explain the concept, and when required, some mathematical formulas are presented.

Chapter 6: Realization

This chapter covers the realization of the work of this thesis, that is, a design based on the approach presented in chapter five. First the foundation of good design practice is discussed through an introduction to the systematic model-based top-down design approach vs. the older technique of bottom-up design.

The model-based design, from a system-level point of view, is employed to design the entire system with follow-up simulations, for which the results are provided. The simulation results prove the validity of the new architecture from a system-level simulation stand-point. This is the first but critical step for such designs.

The transistor-level design is presented next in this chapter. The important simulation results are provided, and compared with the model-based design for functionality and major characteristics of the design i.e. the input-referred offset voltage. Practical issues with designing precision amplifiers in CMOS technologies are also covered in this chapter.

Accurate V-I converters and the patented approach are given here. Techniques to reduce offset and improve the gain accuracy are presented in addition to actual circuit design examples of gain-trim accuracy. Other blocks such as band-gap and oscillator circuits are briefly discussed for the sake of completeness.

Simulation results are judged by a comparison to the performance of the real silicon. The results in all cases are very similar and consistent across the board as depicted in Table 6-9.

The results show that the input-referred offset has an extremely low value in the range of 0.3μV to 6μV. Furthermore, the CMRR measured about 130dB. Other accuracy specifications such as gain-error and linearity-error were measured as low as 0.01%.

Samenvatting

De hoofdstukken één tot en met vier presenteren de grondbeginselen en een beschrijving van het werk dat voorafging aan het gepatenteerde werk dat de kern vormt van dit proefschrift. Als zodanig vormen deze inleidende hoofdstukken geen onderdeel van het kernmateriaal. Zij verschaffen echter een overzicht van de geschiedenis van hetgeen aan het onderzoekwerk voorafging en helpen om de noodzaak te begrijpen van verbeteringen. Voor- en nadelen van de verschillende technieken worden aangeduid. Dit verschaft het inzicht dat heeft geleid tot de ontwikkelingen die verderop in het proefschrift zijn beschreven.
Hoofdstuk vijf en zes zijn geheel gewijd aan het kernmateriaal van dit proefschrift. Overal in deze hoofdstukken worden de lezers veelvuldig verwezen naar het achtergrondmateriaal, teneinde de nadelen van bestaande technieken te laten zien, ofwel om middels een evaluatie de voordelen van de nieuwe methoden te laten zien in vergelijking met voorgaande methoden.
Nu volgt een gedetailleerde beschrijving van de inhoud en doelstellingen van elk hoofdstuk.

Hoofdstuk 1: Inleiding

In dit hoofdstuk bespreken we nut en noodzaak van versterkers in sensor- en regelelektronica. De belangrijkste eigenschappen van deze precisie versterkereenheden wordt naar voren gebracht. Uitdagingen die zich voordoen met oudere versterkervormen, zoals de “Drie-Opamp Instrumentatieversterkers” worden besproken tezamen met voor-en nadelen.
De conventionele “Current-Feedback Instrumentation Amplifiers” (CFIAs) worden genoemd als de meest populaire configuraties voor de constructie van Instrumentatieversterkers (Inst-Amps). De beperkingen van deze wijdverbreide conventionele configuratie worden overal in dit hoofdstuk naar voren gebracht.
Vervolgens worden de uitdagingen besproken voor het ontwerpen van precisieversterkers uitgevoerd in CMOS technologie.

Hoofdstuk 2: Bespreking van de belangrijkste foutbronnen in Op-Amps en Inst-Amps

Dit hoofdstuk behandelt de belangrijkste foutbronnen in Op-Amps en Inst-Amps. De herkomst van offsetspanningen in CMOS Op-Amps en Inst-Amps, alsmede de fouten die hierdoor worden veroorzaakt worden besproken. Fabricagevariabelen, zoals de effecten van willekeurige variaties van procesparameters, en mismatches van drainstromen en de gevolgen daarvan voor de “offsetfouten” worden belicht.

Hoofdstuk 3: Technieken om offsetfouten te reduceren

Conventionele technieken om offsetfouten te reduceren, zoals trimming en daarmee verwante technieken, worden in dit hoofdstuk besproken. Belangrijke trimtechnieken voor verschillende stadia van chip-ontwikkeling, zoals “Wafer-Sort Trimming” (WST) en verschillende “Post-Package Trimming” (PPT) opties worden in dit hoofdstuk behandeld. De voor- en nadelen van al deze technieken worden besproken, teneinde beschikbare mogelijkheden beter te kunnen begrijpen.

Terminologie en standaarden die relevant zijn voor dit onderwerp komen hier ter sprake.

Hoofdstuk 4: Dynamic Offset Cancellation Techniques; Auto-Zeroing: een bemonsteringstechniek

Dit hoofdstuk behandelt "Auto-Zeroing" als een speciale klasse van "dynamic offset-cancellation" die gebaseerd is op bemonsteringstechniek. Een verscheidenheid aan circuits met hun specifieke voor- en nadelen wordt in dit hoofdstuk besproken. In latere hoofdstukken wordt aangetoond dat een deel van de "Auto-Zeroing" techniek wordt gebruikt bij de ontwerpen die het kernmateriaal vormen van dit proefschrift.

Hoofdstuk 5: Dynamic Offset-Cancellation Techniques; Chopping: een benadering gebaseerd op modulatie

Technieken die hier worden bediscussieerd behoren tot een tweede categorie van "real-time offset-cancellation" methoden, te weten "chopping". Het verschil met de voorgaande benadering om offset real-time en dynamisch te verwijderen is dat het hier een techniek betreft die gebaseerd is op modulatie in plaats van bemonstering.
In dit hoofdstuk wordt de werkwijze die is toegepast bij de ontwerpen die de kern vormen van dit proefschrift stap-voor-stap belicht vanuit systeemperspectief. Dit wordt gedaan met het oog op verdere ontwikkeling en verbetering van bestaande ontwerpen. Voor een beter begrip van het concept, worden zo nodig wiskundige formules gebruikt.

Hoofdstuk 6: Realisatie

Dit hoofdstuk behandelt de realisatie van de ontwikkelde concepten voor versterkers, zoals die zijn gepresenteerd in hoofdstuk vijf. De basis voor een goede ontwerpmethode wordt gevormd door een systematische modelgebaseerde top-down benadering in plaats van de oudere benadering van bottom-up ontwerp.
Vanuit systeemoogpunt wordt het modelgebaseerde ontwerp gebruikt om het gehele systeem te ontwerpen middels simulaties. Simulatieresultaten laten de waarde zien van de nieuwe architectuur vanuit systeemperspectief. Deze ontwerpstap vormt een eerste maar belangrijke stap voor het uiteindelijke ontwerp.
Vervolgens wordt in dit hoofdstuk het ontwerp gepresenteerd op transistorniveau. Belangrijke simulatieresultaten worden verschaft en vergeleken met de resultaten ven het modelgebaseerde ontwerp, voor wat betreft de functionaliteit en de belangrijkste ontwerpkarakteristieken en met name de offsetspanning. Praktische ontwerpoverwegingen voor precisieversterkers uitgevoerd met CMOS technologie komen ook in dit hoofdstuk aan de orde.
Nauwkeurige spanning-stroomomzetters en de gepatenteerde benadering worden hier gepresenteerd. Technieken om offset te verminderen en om de nauwkeurigheid van de versterkingsfactor te verbeteren worden gepresenteerd tezamen met actuele voorbeelden van circuitontwerpen met nauwkeurige versterkingsafregeling. Voor de volledigheid worden ook andere circuitblokken, zoals bandgap-spanningsreferenties en oscillatorcircuits, kort behandeld.
Simulatieresultaten van het ontwerp zijn vergeleken met de meetresultaten voor de echte chips en tonen een hoge mate van overeenkomst, zoals weergegeven in Tabel 6-9.

De resultaten laten zien dat de ingangsoffsetspanning een extreem lage waarde kan bereiken in de orde van 0.3µV tot 6µV. Verder bedraagt de gemeten CMRR meer dan 130 dB. Andere nauwkeurigheidsspecificaties, zoals versterkings- en lineariteitsfouten, blijken niet hoger te zijn dan 0.01%.

1. Introduction

This thesis describes techniques to reduce the offset error in precision instrumentation and operational amplifiers. The offset along with some other major accuracy errors such as gain, linearity and Common-Mode errors, if not properly compensated for, degrade the performance of the precision gain blocks to the extent that severely affects their effectiveness in accurate amplification of sensor signals. The offset error which is considered a major error source associated with gain blocks, together with other errors are reviewed in more details within chapters 2 and 3 of this thesis. Conventional and newer approaches will be discussed, with a focus on "Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifiers". In addition, major advantages and disadvantages of these techniques are described.

1.1 Motivation

Electronic instrumentation and control has long been established as indispensable means to reliably set, monitor, and control physical quantities of interest. Examples of such physical quantities are temperature, torque, and speed, which are encountered in many real-world system applications.

Electronic control has pervaded every aspect of our day-to-day lives, finding itself in things such as home appliances, power tools, and toys, as well as cars, airplanes, ships, and industrial machinery. These control systems comprise basic components that include sensors, amplifiers, data converters, digital processors, and mechanical actuators.

Systems need to sense or measure a physical quantity through a sensor and the associated circuitries. Next is to process the response, make a decision, and perform an appropriate change on a parameter in some part of the system under control to tame the overall response and ensure that the system remains under control.

There are a vast variety of different sensors serving as the front line components to convert the physical quantity of interest to an electrical signal. These sensors are of many types, shapes, and constructions. The choice of particular sensor depends on the measured parameter, expected range of operation, operating characteristics of the system under consideration, and intended overall cost of the system.

A sensor's electrical response to a change in a physical quantity may or may not be a linear function of the physical quantity itself. They are often approximated as linear functions in small regions using piece-wise linear approximation. Another approach is to mathematically model the transfer function in its entire range of operation through embedded digital processors within the system of interest.

Examples of such sensors are thermistors, thermocouples, piezoelectric sensors, light sensors, bridges, Hall sensors, and more. The subject of different types of sensors, their characteristics, and theories of operation is beyond the scope of this thesis.

While the aforementioned sensors are different in shapes, sizes, constructions, or even physical principles behind their operation, they have one characteristic shared by almost all of them. No matter if the response or output signal of a sensor is a voltage or current, its magnitude is generally much too small to be dealt with directly, especially when used in a noisy environment.

1.1.1 The Need for Amplifiers in Electronic Sensing and Control

The low voltage (few mV), or current (fraction of mA) output signal of a sensor is by no means large enough to be processed without amplification. Accurate gain blocks such as Precision Operational Amplifiers (Op-Amps), or Instrumentation Amplifiers (Inst-Amps) are needed to bring the signal levels to values sufficient for their intended applications.

Such gain blocks should be able to deal with very small input signals and amplify the electrical signal without any noticeable alteration in parameters other than amplitude. Moreover, the noise performance of such gain blocks should be superior to assure reliable amplification of the small input signal; otherwise the tiny signal is convoluted with or buried under the noise generated within the system itself.

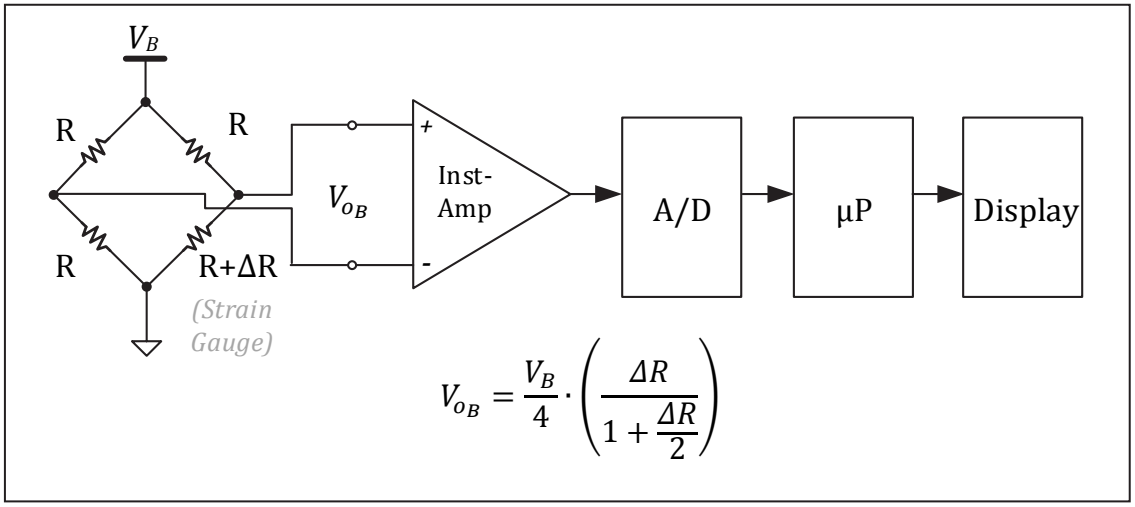

Figure 1-1 – Instrumentation Amplifier in a Sensor Bridge and Display Chain

Amplification is performed prior to drive actuators, or more often prior to digitizing the information by an analog to digital convertor (A/D) for the subsequent digital processing. The processed digital data is going to some display or readout in measuring instrument systems.

In a closed-loop control system, the data may be converted back to an analog signal by a digital to analog converter (D/A) prior to drive an actuator, or being injected at a summing node in the system under control. Not all closed-loop systems employing Inst-Amps are digitally controlled.

Figure 1-2 shows a top-level view of a simple general Analog Closed-Loop Control System. As seen, the system under control has a Sensor to convert a physical parameter of interest -whose controllability is desired, to an electrical signal. The signal is amplified by a precision gain block and passed on to an Analog-Controller / Signal-Conditioning stage. The output of the Analog-Controller block eventually drives an Actuator within the system under control through a Driver or Power-Amplifier. Some Control and Set-Point Signals are added in an analog fashion to either the amplification block, or the controller itself. The above control method is relatively old, therefore today is primarily used in inexpensive systems or those without a microcontroller.

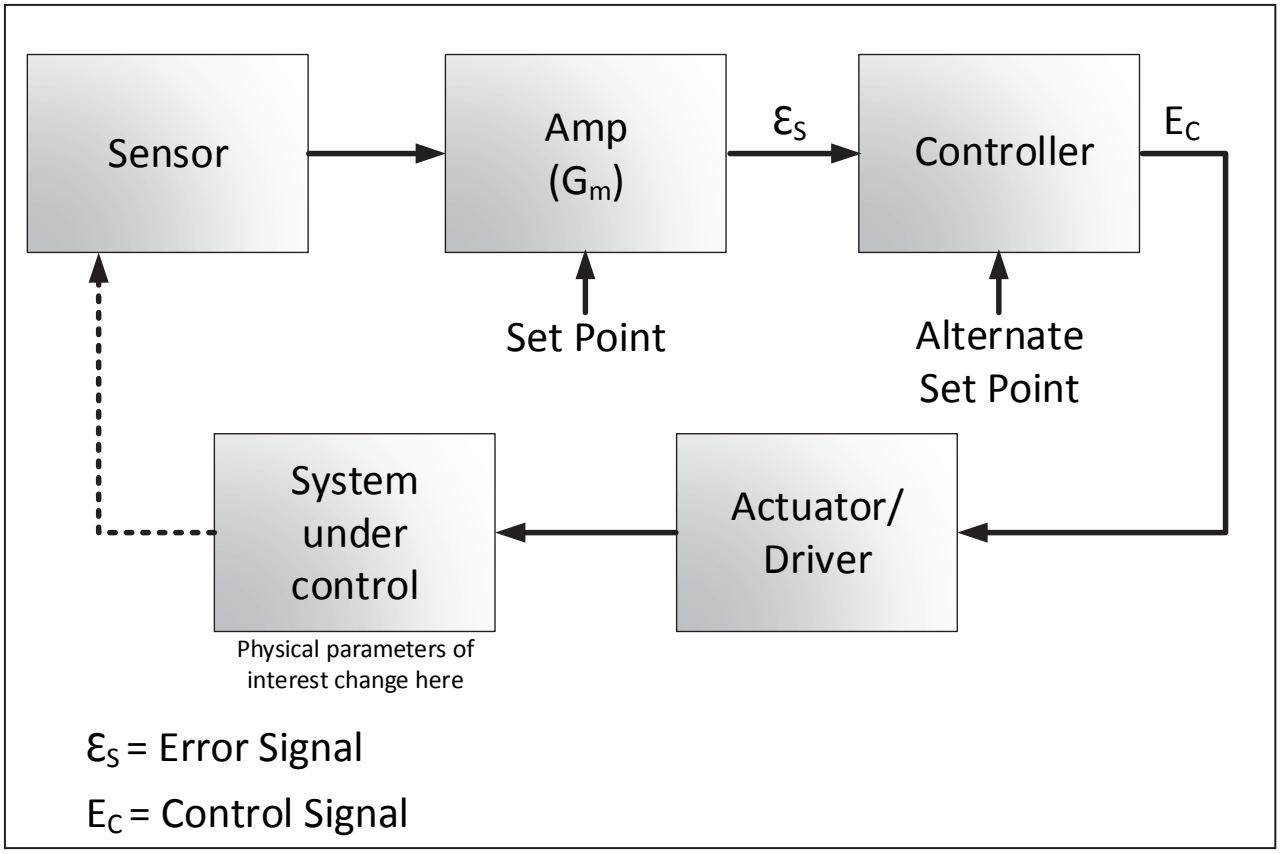

Figure 1-2 – Gain Block (Amp) in a typical Analog Controlled Closed-Loop System

The more adapted systems are the ones using Digital Closed-Loop Control System as depicted in figure 1-3. Here again the system under control has a Sensor together with a Gain-Block (often Inst-Amps) to sense and amplify the physical parameter of interest (voltage, current, charge, temperature, speed, torque, etc…). The output of the amplifier feeds the A/D whose output is driving the Microcontroller's Data Bus through its I/O port. There, the "to be controlled" physical parameter is digitally processed and compared with a Set-Point data.

Finally, a microcontroller provides the necessary output to a D/A convertor for amplification and eventual drive of an Actuator within the system under control to tame the physical parameter.

As can be seen, Precision Gain-Blocks are integral components of both Open-Loop, and Closed-Loop systems. The open-loop systems are mainly for Monitory and Read-Out purposes, whereas the closed-loop systems are not only monitoring, but also controlling a physical parameter of interest to stay at, or within certain desired boundaries through Set-Point inputs.

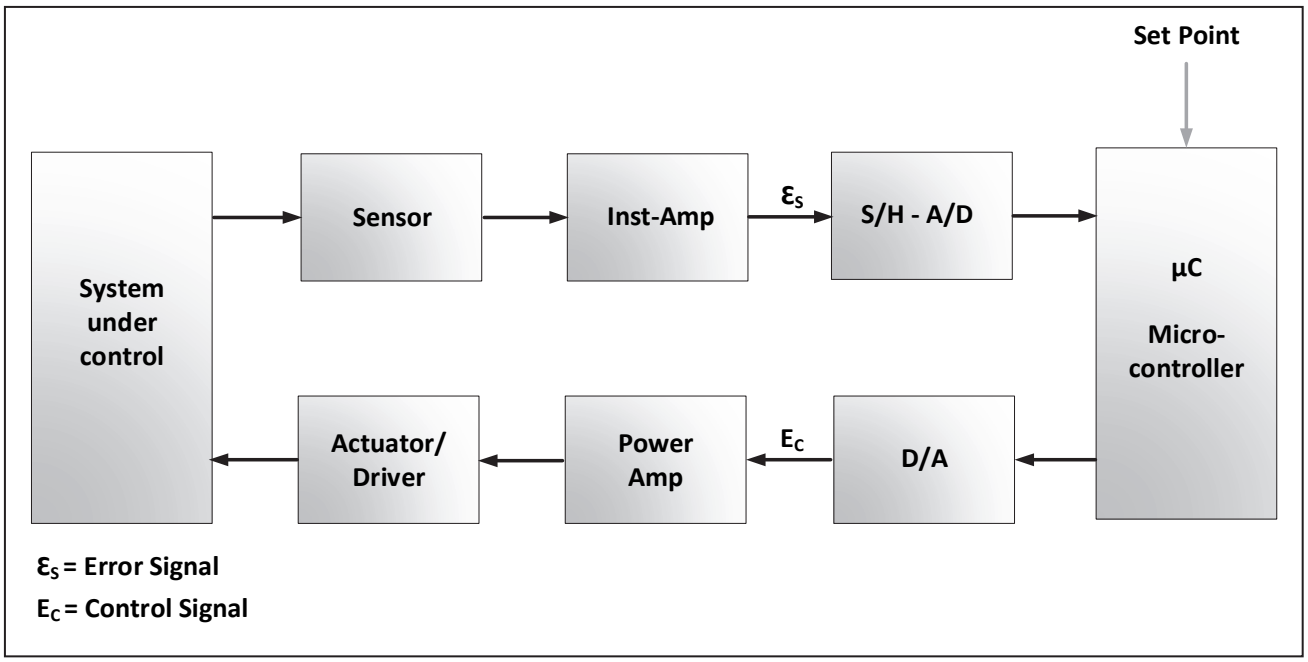

Figure 1-3 – Instrumentation Amplifier in a Typical Digital Controlled Closed-Loop System

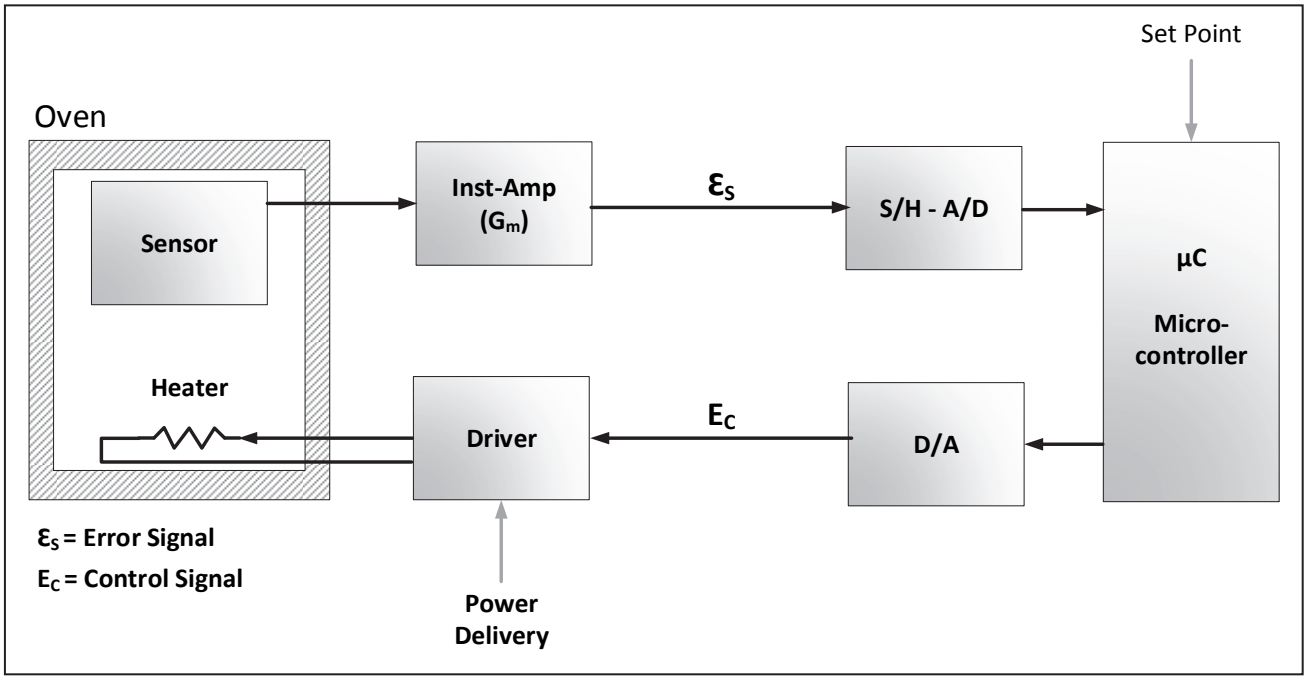

Figure 1-4 – Instrumentation Amplifier used in a common Microcontroller-Based Oven Temperature Control

As the last example, a high level block diagram of an oven temperature control common to many other practical applications such as the temperature control of building's heating systems is shown in figure 1-4.

Notice that in systems based on the diagram presented in figure 1-4 the heating control process is often simply performed by turning the heating element ON and OFF as required so that the system can reach the target Set-Point (desired temperature). However for cooling, one has to rely on heat losses in the system unless provisions for reducing the temperature (such as fans or other cooling techniques) are incorporated and controlled within the system.

Ovens to Bench-Test Integrated Circuits (ICs) are for sure of the second type, that is for those ovens with requirements for cold temperature testing, provisions for reducing the temperature to values below -55°C is certainly included.

1.1.2 Major Requirements of Precision Gain Blocks for Sensors

As the output voltage of a sensor is in the millivolt (mV) range, the input offset voltage ($V_{off\text{-}in;}$ to be described in section 2.2) of the gain block following the sensor, must be at least one or two orders of magnitude smaller than the sensor's output signal itself. This requires an amplifier with an offset voltage specification in the order of few μV to few tens of μV.

Although both Operational Amplifiers (Op-Amps), and Instrumentation Amplifiers (Inst-Amps) can be used as gain blocks following a sensor, the latter are preferred for their capability to directly handle differential signals and reject unwanted common-mode signals.

Instrumentation Amplifiers are generally closed-loop differential amplifiers, with fixed or adjustable gains. Operational Amplifiers, on the other hand, are offered as open-loop gain blocks, with a need for a feedback loop from output to input to set the closed-loop gain.

Since Inst-Amps are differential type amplifiers, they are ideally capable of selectively amplifying only the differential input signal (the output from the sensor), and be insensitive to the undesired common-mode signal. The insensitivity of an amplifier to common-mode signals is demonstrated through a parameter called the Common-Mode Rejection Ratio (CMRR), which is defined as the ratio of Differential Mode to Common Mode Amplifications and often presented in the unit of dB. Inst-Amps generally have excellent CMRR, typically at or in the excess of 120dB.

Another often-required characteristic of the gain blocks following sensors is the ability of the amplifier's input stage to work at or slightly (some few hundreds of mV) beyond the supply rails. This requirement is of prime interest in measuring the supply currents at High-Side (V_{DD}) or Low-Side (V_{SS} or GND) through a Sense-Resistor in the path of current. This Current-Sensing application is very common, especially in Power Management Electronics.

The requirement of sensing at or slightly beyond both rails for an Inst-Amp or Op-Amp simultaneously mandates the use of complementary devices at the input stages. This makes the design more complex compared to sensing at only one rail.

1.2 Challenges with the Three Op-Amp Instrumentation Amplifier as a Conventional Gain Block for Sensors

One of the well-known Inst-Amps topologies historically used for amplification is the "Three Op-Amp Instrumentation Amplifier" shown in figure 1-5.

Due to its circuit simplicity, the topology is a popular one for gain blocks in a variety of different sensor applications. Although the architecture is straightforward, it suffers from several disadvantages.

The Three Op-Amp Instrumentation Amplifier is incapable of sensing any of the two supply rails because otherwise the output of one of the two input Op-Amps in the structure collapses to that

rail. This means that the output device becomes saturated for a BJT output transistor or enters the linear (Ohmic) region for a MOS device.

If there is a need to amplify a differential input voltage near or slightly beyond the rails using a Three Op-Amp Instrumentation Amplifier, the only option would be to use level shifters at the inputs. As an example, if $V_{in_{cm}}$ (see figure 1-5) is set to GND, the negative feedback loops around A_1 and A_2 will force the voltage across resistor R5 to be equal to $V_{in_{dif}}$, which sets a zero potential at the output of A_2 and A_1 for a zero differential input, or will demand a negative swing below the GND at the output of A_1 for a positive differential input.

The *CMRR* of a Three Op-Amp structure is very much dependent on the resistors R_1 to R_4 around the Op-Amp in the second stage as seen below. More or less similar expressions for the worst case *CMRR* of this Ins-Amp structure (assuming a well matched input Op-Amp pairs A1 / A2) are given by [19, 20, 21].

If we use letter "H" to denote the CMRR, then:

$$\frac{1}{H_{Inst-Amp}} = \left[\frac{1}{A_v + 1}\right] \cdot \left[\frac{1}{H_{res}} + \frac{1}{H_{Op-Amp}}\right] \qquad \textbf{(1.1)}$$

where A_v is the voltage gain given by:

$$\begin{aligned} A_v = \frac{V_{out}}{V_{in-dif}} &= -\left(\frac{R_2}{R_1}\right)\left(\frac{R_6 + R_5 + R_7}{R_5}\right) \\ = -\left(\frac{R_2}{R_1}\right)&\left(1 + \frac{R_6 + R_7}{R_5}\right);\ \text{Where } R_1 = R_3 \text{ and } R_2 = R_4 \end{aligned} \qquad \textbf{(1.2)}$$

and:

$$H_{res} = \frac{1+\frac{R2}{R1}}{4\cdot\frac{\Delta R}{R}} \quad ;\ \text{and } \frac{\Delta R}{R} = \text{Resistor´s Relative Tolerance} \qquad \textbf{(1.3)}$$

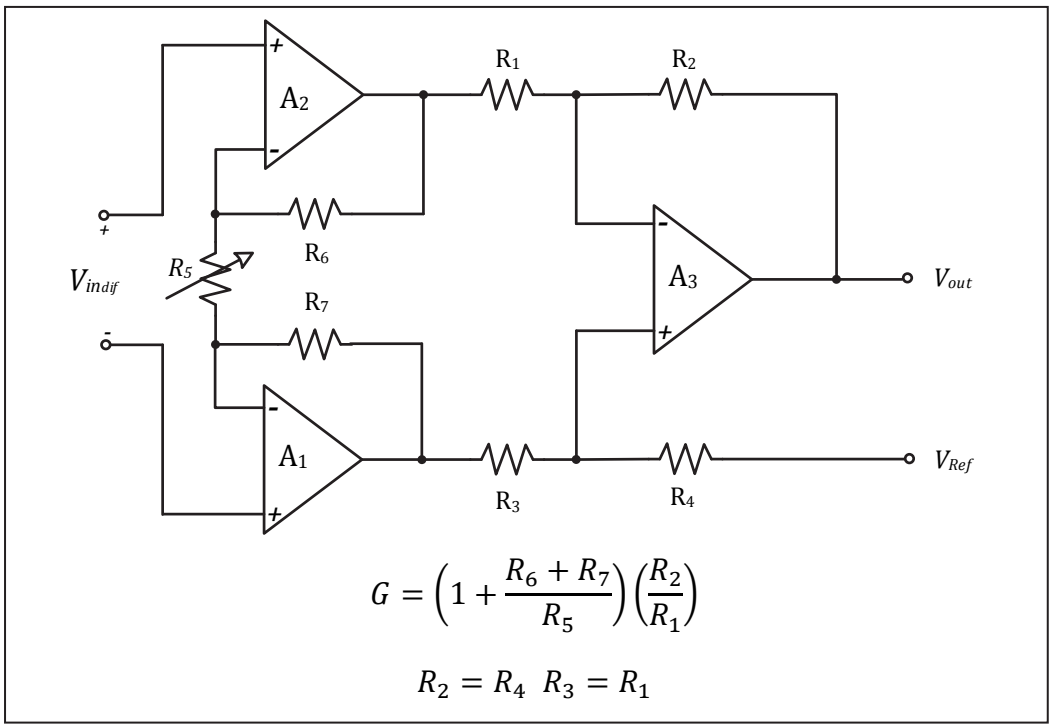

Figure 1-5 – The Three Op-Amp Topology

So, the common-mode error is partly coming from the mismatch of the resistor pairs R_1, R_2 and R_3, R_4; each having a mismatch of $\Delta = \frac{\Delta R}{R}$, in such a way and direction that together, the mismatches make a worst-case imbalance. The $H_{Op\text{-}Amp}$ appearing in the second term of the equation is simply the *CMRR* of Op-Amp A3 in the second stage. Note that if the amplifiers A_1 and A_2 are well matched, the structure is virtually insensitive to the *CMRR* of these input devices.

Here one simply notices that if the Op-Amp *A3* has a *CMRR* of 100 dB, the bridge resistors are matched within %0.1, the Instrumentation is used in a gain of 30 configuration, with an equal resistor values of *R5* through *R7*, and a well matched input Op-Amps *A1* and *A2*, the *CMRR* of the structure, is hardly 70 dB without any trim.

This is due to the strong dependence of the *CMRR* of the circuit on the bridge resistor mismatches, something which is hard to prevent and costly to trim. The difficulty of achieving a high *CMRR* without trimming is considered one of the major drawbacks of this topology.

However, if the cost of the trim is acceptable, it is possible to achieve high values of CMRR in the excess of 100dB. This is possible, in particular, when one error source (bridge mismatch), is purposefully compensated with the other one (Op-Amp common mode error), but in any case, the performance of the Chopper-Stabilized Inst-Amps are far superior in this regard.

The Three Op-Amp Instrumentation often consumes more area or power compared to newer techniques, and provides less optimal performance in many accuracy specifications compared to its rival counterparts. These counterparts comprise the category of amplifiers employing Dynamic Offset Cancellations (DOC) techniques, as will be explained in the following chapters.

In order to achieve a good performance, all the Op-Amps in the Three Op-Amp structure must be of high quality in terms of the accuracy specifications. Often this requirement manifests itself in a demand for higher chip area, increased power consumption, or complex trims.

If the Three-Op-Amp Instrumentation IC is used in a variable-gain configuration, the temperature tracking of the external gain setting resistor R5 compared with those internal ones in the bridge and feedback network could be troublesome.

This issue is not limited to the Three Op-Amp design, but holds true for all structures with a single gain setting resistor outside the chip.

1.2.1 Summary of the Disadvantages Associated with the Three Op-Amp Structure

In summary, the disadvantages of the Three Op-Amp Instrumentation Amplifiers are as follows:

1) Since the structure has Three Op-Amps that all need to have good characteristics to deliver an overall high-quality precision specification, it is usually considered costly and taking a large area, with a likely higher overall current consumption.

2) The CMRR is affected not only by the Op-Amps used, but also by the mismatches of the resistor bridge around the difference amplifier at the second stage, hence the need for complex trimming of the Op-Amp and the bridge for optimal performance

3) In order to get to very low offset values, both of the input Op-Amps need trimming.

4) The Three Op-Amp Instrumentation Amplifier is incapable of sensing at or slightly beyond the supply rails, unless level shifters are used at the inputs. This disadvantage is a major drawback in applications requiring a precise measurement at or slightly beyond the supply voltage rails. Common application examples requiring this feature are high and low side current sensing at VDD, GND, or VSS supply lines in single or dual power supply systems as mentioned before.

5) For adjustable gains with an external resistor (here R5 in figure 1-5), the temperature mismatch between the external and internal gain setting resistors degrades the performance of the Inst-Amp over temperatures. However, this drawback is not limited to Three Op-Amp structure, but for all structures that have their gain setting resistor outside the chip.

In chapter five and six, when the new approaches involving the chopper techniques, in particular the work of this thesis “Chopper-Stabilized Auto-Zeroed Chopper Techniques” are discussed, we will revisit the subject again for a comparison of the old versus new approach.

1.3 A Review of Conventional Current Feedback Instrumentation Amplifiers (Conventional CFIAs)

Another Gain Block commonly used as an instrumentation amplifier is the so called Current Feedback Instrumentation Amplifier (CFIA), also known as the Indirect Current Feedback Instrumentation Amplifier (ICFIA) topology. The simple, yet frequently used architecture, as shown in figure 1-6 consists of two identical transconductance amplifiers G_{m2i}, and G_{m2f}, an output stage G_{m1}, along with the gain setting resistors R_2, and R_1, which constitute the feedback network as well.

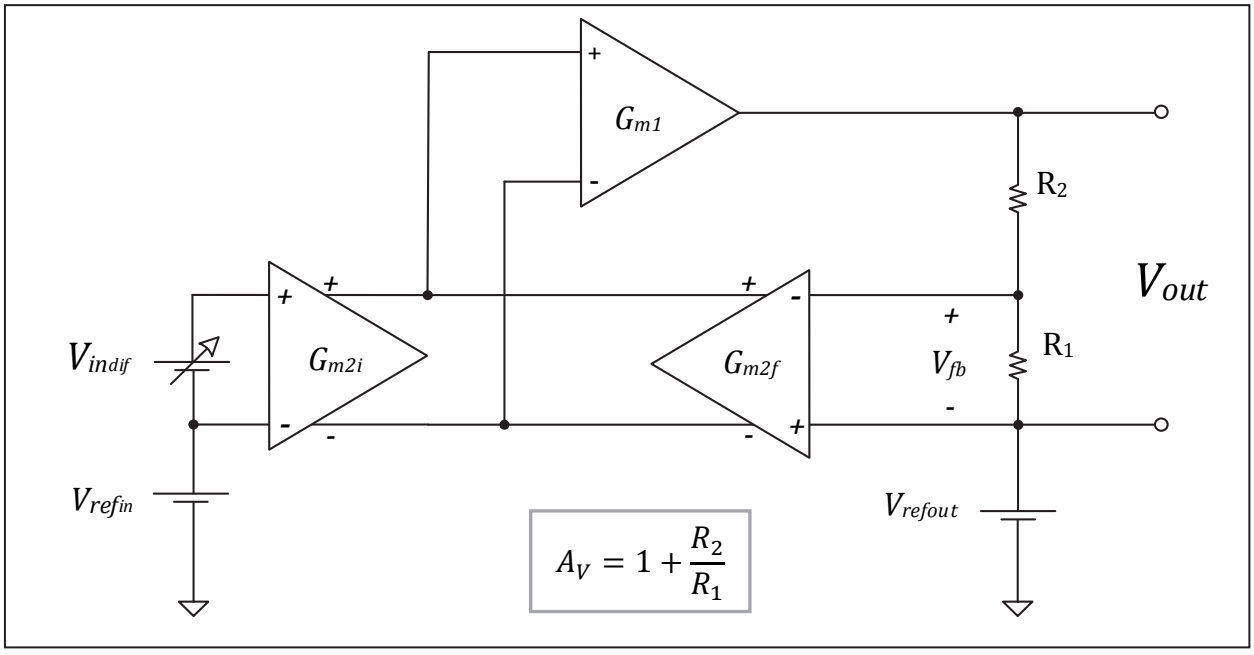

Figure 1-6 – Block View of Current Feedback Instrumentation Amplifier (CFIA)

The input transconductance amplifier G_{m2i} converts the differential input voltage V_{indif} to a differential current, while the second voltage to current converter G_{m2f} (the feedback transconductance), converts a fraction of the output voltage, that is the feedback voltage V_{fb}, to a second differential current.

The two differential currents at the outputs of G_{m2i} and $G_{m2f,}$ which are complementary, are summed up at the input of the output amplifier G_{m1}; ideally leaving zero current entering the output amplifier G_{m1}.

Equating the output currents of G_{m2i} and G_{m2f}, with the assumption that they are free of offset errors, and an infinite open loop gain for G_{m1} stage, reveals the voltage gain of the ideal Inst-Amp.

$$A_V = \left(\frac{G_{m2i}}{G_{m2f}}\right) \cdot \left(1 + \frac{R_2}{R_1}\right) \qquad \textbf{(1.4)}$$

In order to make errors associated with different G_{m2i} and G_{2mf} insignificant, it is customary to make them equal. This simplifies the gain equation to:

$$A_{\mathrm{v}} = 1 + \frac{R_2}{R_1} \;; \qquad For\ G_{m2i} = G_{m2f} \qquad \textbf{(1.5)}$$

Figure 1-7 shows a basic schematic for a current feedback Inst-Amp in CMOS technology, capable of sensing the negative supply rail due to the fact that the input devices are PMOS transistors. An NMOS device at the input, with a flipped folded cascade configuration and summing node compared to the schematic of figure 1-7, would obviously sense the positive supply rail.

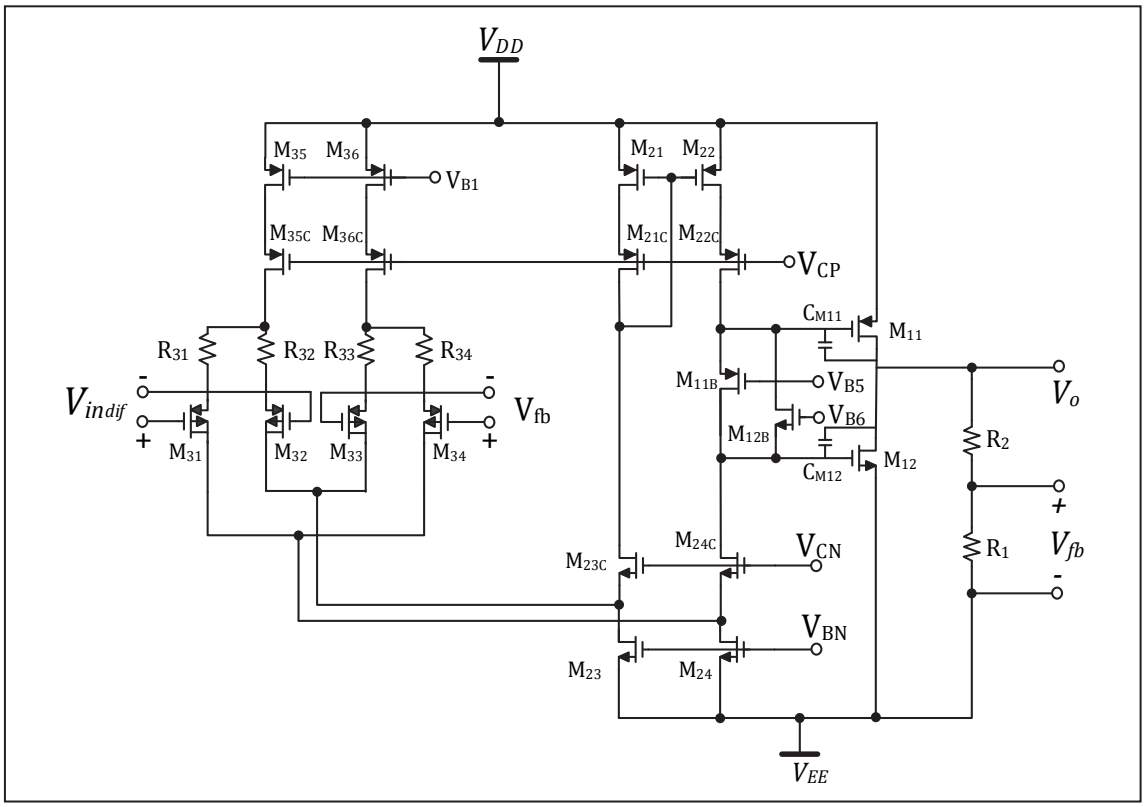

Figure 1-7 – Basic Schematic of a CMOS Current Feedback Instrumentation Amplifier (CFIA)

A simple pioneer bipolar version of this topology is shown in figure 1-8 [3].

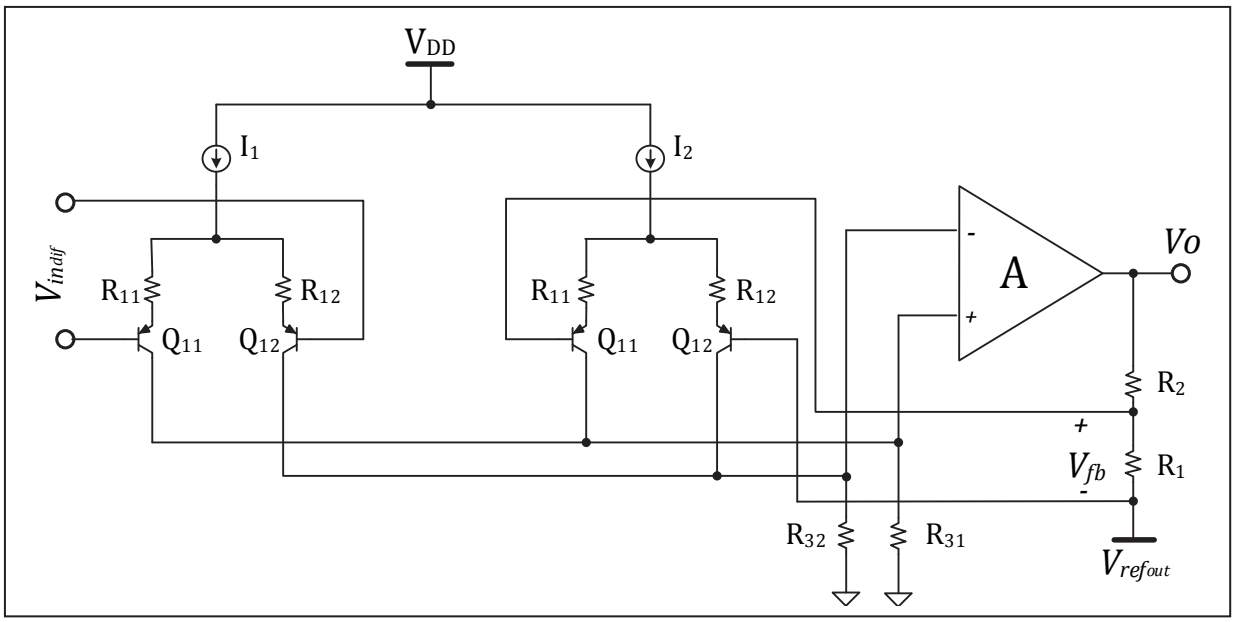

Figure 1-8 – Basic Schematic of a BJT Current Feedback Instrumentation Amplifier (CFIA)

The general symbol for the CFIA is shown in figure 1-9.

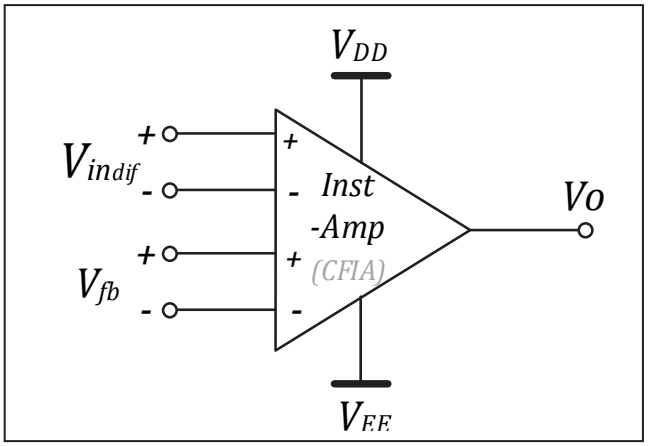

Figure 1-9 – General Symbol for Current Feedback Instrumentation Amplifier (CFIA)

1.3.1 Performance Limitations of Conventional CFIA Topology

Although the Current Feedback Instrumentation Amplifiers (CFIA) is a simple yet efficient topology (it could simply be just a two stage amplifier), the approach generally suffers from the same limitations common among many similar configurations that do not employ Dynamic Element Matching (DEM) or Dynamic Offset Cancellation (DOC) techniques. This is true particularly when CMOS technology is employed as the process of the choice, which more than often has been the case for long.

As will be seen in the next sections, MOS devices suffer significantly from their native mismatches when used in differential pairs at the input stages of amplifiers. This choice will certainly show a far larger input referred offset as compared to designs using their BJT counter parts. Even with BJT devices, without any sort of trim, the performance in terms of input referred offset, and noise (particularly flicker noise), is nowhere sufficient to categorize the amplifier in the class of Precision Inst-Amps or OP-Amps.

An order-of-magnitude improvement for input-referred offset can be assumed when conventional trims are employed to take care of mismatches of the input transistors of the differential pair in addition to the load devices mismatches at this stage. No matter what type of conventional trim (Wafer-Level or Post-Package trim) is used, the trim is done at only one temperature, which is almost always the room temperature. This means that the matching improvement resulting from the trim may not hold true as temperature is changed, resulting in degradation of accuracy specifications, most importantly input-referred offset.

On the other hand, the Dynamic Offset Cancellation techniques, as will be shown, not only work at room with far better accuracy, but are in effect at over temperatures as well. An improvement of two to three orders of magnitudes is common.

Table 1-1 gives a relative measure of the input referred offset specification of a general CFIA, using MOS devices, but with different offset removal techniques.

MOS Dif. Pair Native Input Ref. Offset	With Conventional Techniques	With DOC Techniques
15mV ~ 20mV	0.25mV ~ 1.5mV	0.2µV ~ 20µV

Table 1-1 – Typical Input Referred Offset Specifications for a CFIA in CMOS Technology using Different Trim Techniques

1.4 Challenges with Designing Precision Amplifiers in CMOS Technology, and the Aim of this Thesis

Complementary Metal Oxide Semiconductor (CMOS) Technology has been the process of choice for a few decades now, dominating the analog, mixed signal and power domains. This is due primarily to the size, cost, and ease of integration with digital portions in many mixed signal Integrated Circuit (IC) designs.

Despite the overall advantages of CMOS technology, the Metal Oxide Semiconductor (MOS) transistors are inherently inferior compared to their bipolar counterparts when used in precision analog designs.

First and foremost, the input referred offset error of a CMOS amplifier is often more than an order of magnitude worse than that of its bipolar counterpart. As a relative measure of comparison, the 1-sigma of ΔVbe of Bipolar Junction Transistors (BJTs) at the input differential pair is typically around 100µV to 150µV, whereas the 1-sigma of ΔV_T for the MOS devices of a MOS differential pair is around 2mV to 5mV. While the 3-sigma input referred offset of a MOS input stage is around 5mV to 20mV, the same input referred offset for a BJT input stage is normally around 0.5mV to 1mV. If CMOS devices are to be used, offset reduction techniques are required to overcome this issue. The reduction, depending on the technology and technique, is often around one or two orders of magnitude. The work of this thesis "Chopper-Stabilized Auto-Zeroed Chopper Techniques" is serving this purpose.

There are other disadvantages inherent to MOS transistors. MOSFET devices, unless used in Subthreshold Region, have lower transconductance per unit drain current when compared to BJTs. This is evident from the relationship of the transconductance g_m with drain current in each device. The transconductance of MOS devices operating in strong inversion is proportional to the square root of the drain current, whereas in BJT devices the relationship is linear. The transconductance factor is a critical design parameter which sets the gain, and together with the load or feedback capacitors, determines the bandwidth of the amplifier.

Fortunately, many applications of precision amplifiers are either relatively at low frequencies (below few MHz) or DC, so the application of MOS devices in subthreshold region is not only justified but preferred. This is primarily due to the fact that Transconductance per unit Drain-Current (g_m / I_D) is higher in Weak Inversion (WI) operation than in Strong Inversion (SI) as will be discussed in section 2.3.2, together with a discussion of the parameters affecting the Drain-Current Mismatches in MOS devices. There we conclude that for any application not requiring higher drive capability, speed, or bandwidth, the subthreshold region is considered to be the preferred region of operation for MOS devices.

MOS transistors operating below a corner frequency exhibit the famous Flicker Noise, also called (1/f) noise, which is the dominant noise source at low frequencies for such devices. Among all active semiconductors the MOS-FETs have the highest 1/f noise due to their surface conduction mechanism [2].

Although the flicker noise is heavily process dependent, factors such as geometry area WL (with inverse proportionality), gate oxide capacitance C_{ox} (with inverse proportionality), and the saturation voltage $V_{GS} - V_T$ (with direct proportionality), can be utilized to reduced its effect.

For example, in a differential amplifier with a known tail current, increasing the aspect ratio W/L (practically increasing W) will not only help reduce the flicker noise and native offset of the devices, but also will likely push the operating region of the MOS transistors to the subthreshold region. This maximizes the transconductance per unit drain current, but care must be taken into consideration that no need for high speed operation, or bandwidth are in the way.

Since the low frequency noise is often indistinguishable from the offset itself, any attempt to reduce the offset will improve the low frequency (1/f) noise performance as well.

The work described in this Thesis aims to reduce the offset and low frequency noise in precision instrumentation amplifiers by introducing a new technique: "Chopper-Stabilized Auto-Zeroed Chopper Techniques". The approach can be used in both BJT and CMOS technologies. However due to the inherent large offset and device mismatches in CMOS technology, amplifiers made in this process are the primarily beneficiaries of the technique.

1.5 Organization of this Thesis

This thesis is presented in six chapters. However, chapters one to four are not the contributions of this author, but are presented just as a foundation, and to provide a history of prior arts. Advantages and disadvantages of these techniques are brought forward, with the latter being a motivation to seek for more advanced techniques to overcome the issues with the prior arts. Chapter five and six are about new and patented techniques in designing high performance operational and instrumentation amplifiers. Chapter 7 presents the conclusion and summary.

Chapter one briefly touches the dominant effect of sensing and control electronics in our daily lives. The need for accurate Gain Blocks to amplify the Sensor's weak output signal within the system is also discussed. The major requirements for such Gain Blocks along with the limitations of the flagship of the conventional approaches, the Three Op-Amp instrumentation amplifier, are described. Next the Current Feedback Instrumentation Amplifier, one of the most commonly used Inst-Amps is reviewed. A section is devoted to the major challenges of designing Precision Amplifiers in CMOS Technologies. Finally, the need for the newer techniques and the aim of this thesis is disclosed.

Chapter two reviews the major error sources in amplifiers, revealing the offset error as the dominant source for sensor applications. The origin of the offset error in CMOS amplifiers and the effect of random process variations are presented. Finally, the drain current mismatch and the resultant error at the input of an amplifier are discussed.

Chapter three covers techniques to reduce offset error. Several conventional methods of offset trimmings at Wafer-Level or at Post-Package are presented in short, along with general advantages of Dynamic Offset Cancellation (DOC) techniques.

Chapter Four deals with Dynamic Offset Cancellation techniques, emphasizing the Auto-Zeroing concept as one of the supplementary techniques used in the work of this thesis. Several methods and calibration techniques along with their advantages and disadvantages are presented.

Chapter Five covers Chopper Techniques with heavy emphasis on the work done for this thesis, primarily from a system-level perspective. The idea, the design, and their validity through descriptive mathematical modeling and formulas, or simulation support wherever needed are presented. Care is taken to limit the formulas to a manageable size and format. Complex mathematical modeling, which is impractical to be utilized in design, is generally avoided in this discussion.

Chapter 6
The chapter demonstrates the Realization of the "Chopper Stabilized Auto-zeroed Chopper Instrumentation Amplifiers" using CFIA topology, and presents the results.

Top-down model-Based design approach is discussed against bottom-up design in this chapter. The new patented techniques already described in chapter 5 are validated in this chapter through the model-based, as well as transistor-level designs. Finally both designs are compared against each other for harmony, and later with silicon measurements for validation.

The results of the model-based design were in agreement with the transistor-level design, and both in agreement with silicon measurement results.

2. Review of Major Error Sources in Op-Amps and Inst-Amps

2.1 Background

Real-world operational and instrumentation amplifiers contain error sources that cause their performance to differ from that predicted by the ideal models that are used to simplify the analysis of circuits involving such gain blocks.

Operational amplifiers (Op-Amps) are generally considered to be open-loop gain blocks. However, when they are used in a closed-loop configuration with negative feedback, the voltages at their inverting and non-inverting terminals are separated only by the amount of their total input-referred error, which is usually in the low mV range.

Instrumentation amplifiers, on the other hand, are generally classified as closed-loop gain blocks capable of handling a differential input voltage of a few hundred mV at their inputs, but they suffer from the same error sources as their Op-Amp counterparts.

These error sources cover a range of DC to low-frequency origins such as offset voltage and current, finite DC open-loop gain, linearity, closed loop gain, DC common mode, DC supply rejection, and flicker noise errors. A variety of AC limitations such as finite bandwidth and finite slew rate also contribute to total overall error.

The existence of such errors in both Op-Amps and Inst-Amps limit the performance of these gain blocks in precision analog circuitry, particularly when the small signals often associated with sensor's outputs must accurately be amplified and processed.

2.2 Major Error Sources in Op-Amps and Inst-Amps

It is common to model the major error sources of the amplifiers in a closed loop circuit, in particular the DC errors, as voltage or current sources presented at the input of the amplifier as shown in figure 2-1.

Figure 2-1 shows an Op-Amp in a closed-loop negative feedback configuration with its equivalent total error source shown as V_{err}. This error source is given by [6] :

$$V_{err} = V_{os} + \frac{V_{out}}{A_{ol}} + v_{noise} + \frac{\delta V_{cm}}{H} + \frac{\delta V_{sup}}{Y} + \left(I_{B\_}\right)\left(R_{s\_}\right) + \left(I_{B_+}\right)\left(R_{S_+}\right) \qquad \textbf{(2.1)}$$

In Eq. (2.1) V_{os} is the input-referred offset voltage, A_{ol} is the open-loop gain of the Op-Amp, v_{noise} is total equivalent noise voltage at the input, δV_{CM}, δV_{Sup}, are the changes in the common mode and supply voltages, and finally H, and Y are the common-mode rejection ratio, and power supply rejection ratios of the Op-Amp, respectively.

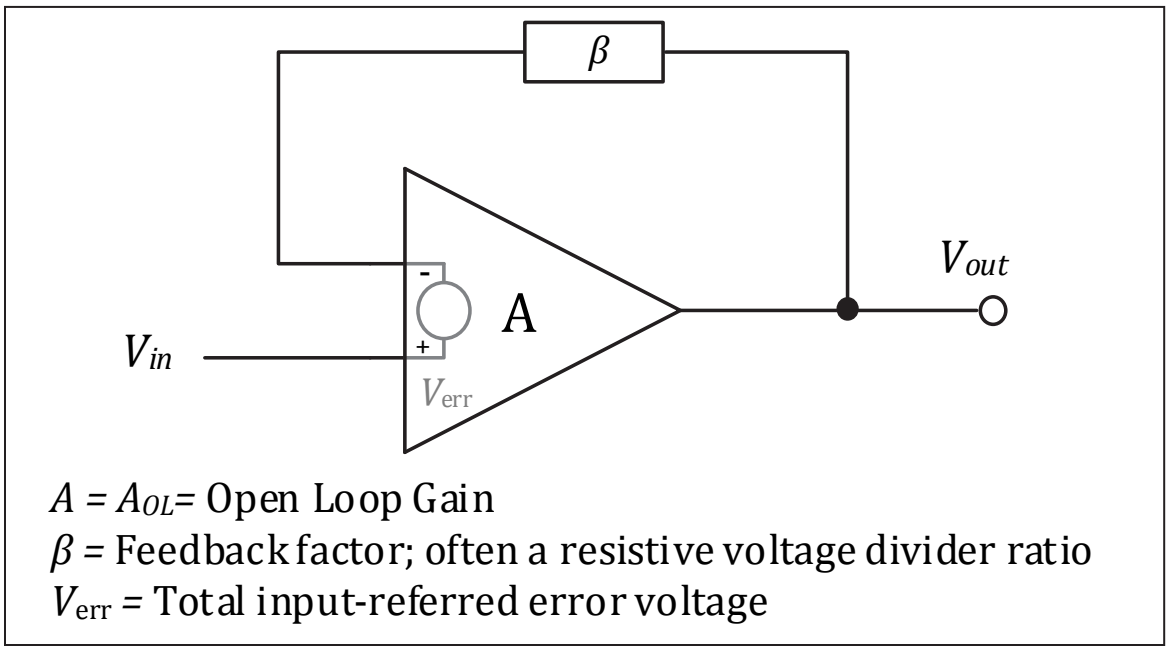

Figure 2-1 – Op-Amp in a Closed Loop Configuration with Errors Modeled as an Input Referred Source

I_{B-}, I_{B+}, R_{s-}, and R_{s+} are the input bias currents to inverting and non-inverting inputs, along with the source resistances of the signal sources connected to these terminals.

Although Eq. (2.1) models the majority of the major error sources of the Op-Amp; the expression falls short of listing other important errors such as distortion, bandwidth, slew rate, linearity, etc., which are also considered as key performance characteristic parameters of amplifiers. Despite this, the equation still fairly depicts a good picture of the most important DC parameters of an Op-Amp, in particular the offset and offset-related parameters.

The errors associated with the input bias currents (the voltage drop across the source resistances of the signal sources at the input terminals of the Op-Amp) are mostly encountered in Op-Amps with bipolar junction transistors (BJT's) at the input stage.

MOS transistors do not have a *DC* bias current at their inputs, since they are voltage-controlled devices with capacitive elements at the input. Therefore the sixth and seventh terms of Eq. (2.1) are removed in a *DC* analysis if MOS devices are used for the input differential pair of the Op-Amp. Throughout this thesis, and in designing of low offset amplifiers via a new technique called "Dynamic Offset Cancellation", the focusing will be on using MOS devices as the primary choice of device.

When offset reduction is realized with a method that affects all the offset errors, the *DC CMRR* can be defined as the ratio of the change in the offset voltage due to a change in common mode voltage. It is then clear that offset performance affects the *CMRR* parameter. The same is also true for *DC PSRR*, which is then defined as the change in offset voltage due to a change in supply voltage. The above are represented by the fourth and the fifth terms of Eq. (2.1).

The noise term at low frequencies is called flicker noise, also known as 1/f noise. This error is often summed up or treated as part of the DC offset error, as it is frequently indistinguishable from the offset error itself.

The second term of Eq. (2.1) represents the input-referred error due to the finite DC open-loop gain of the Op-Amp. As this *DC* gain is normally very high, the effect of the error in a closed-loop circuit of low or moderate gains is usually negligible; especially when compared to the offset error itself. As will be shown, the offset error, the first error term in Eq. (2.1) is noticeably the most important one.

As an example to see the relative weight of different error terms in Eq. (2.1) , we consider a rail-to-rail Op-Amp with a MOS differential pair at the input stage, with an input referred offset error of 10mV, *CMRR* of 80dB, *PSRR* of 60dB, and DC open loop gain of 10,000. If the amplifier is used in system with a 5(1 ± 10%) V power supply, the error terms associated with Common mode change, supply change, and finite gain are 0.5mV, 1mV, 0.5mV respectively. The largest error source is still an order of magnitude less than the offset alone. This example shows that the offset error by far dominates the other error sources in MOS amplifier design.

In the following sections, we will formally define the offset and its effects on circuit performances, the origin of the error, and ways to compensate or reduce it in CMOS amplifier design.

2.2.1 Definition of Offset Error

If the inputs of any real world Op-Amp or Inst-Amp are shorted together at some common-mode voltage, for example ground as shown in figure 2-2 for an Op-Amp, the output will not be at zero voltage as expected. A small voltage V_{os}, called input referred offset, is needed to bring the output voltage to zero, as shown in figure 2-3.

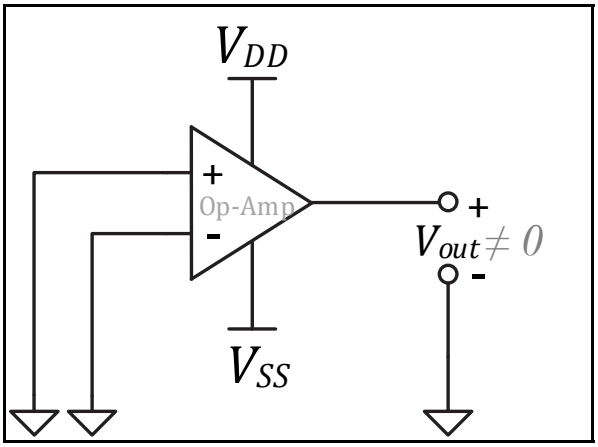

Figure 2-2 – Real Op-Amp with a Non-Zero Output Voltage for a Zero Input Voltage

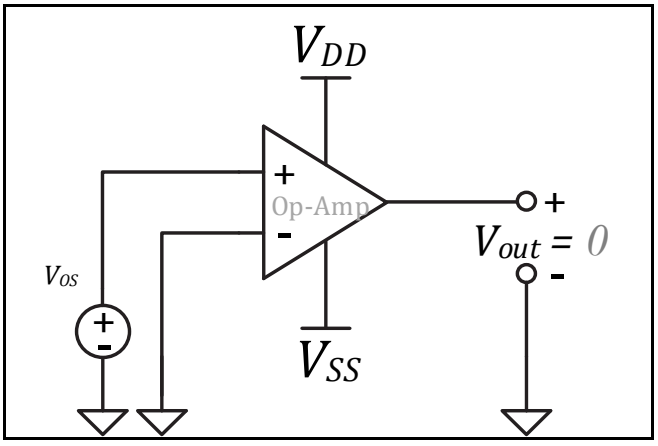

Figure 2-3 – Real Op-Amp with Offset Compensation Bringing V_{out} to Zero (Definition of Offset Error Voltage)

This V_{os} error can be troublesome when the task is to accurately amplify small signals. An example is shown here in which a 15mV signal is to be amplified to a gain of 100 by an Op-Amp with a 5mV offset error, used in a conventional non-inverting configuration as shown in figure 2-4. It is obvious that the 5mV offset is indistinguishable from the small *DC* signal itself. The resultant 10mV at the junction of the gain setting resistors generates a 1V output voltage instead of the expected 1.5V, which could be wrongly misinterpreted as if the gain was set to two-thirds of its intended value. In reality the Gain-Error (GE) is a multiplicative or slope (rotational) error, and can never be compensated by an offset error which is on the contrary an additive (or vertical shift) error within the transfer function of the gain block (V_{out} vs., V_{in}, or alternatively the graph of the Total-Error vs. the input voltage). The concept is presented in section 3.4 with more details.

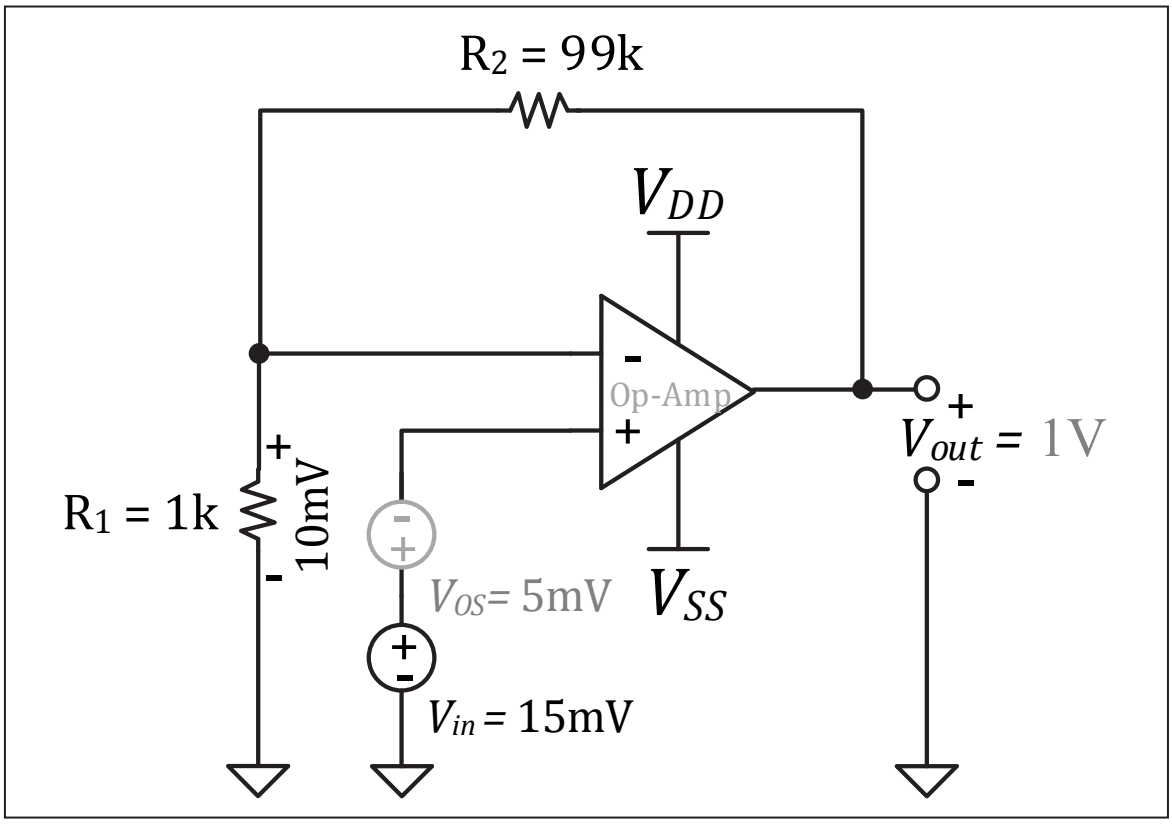

Figure 2-4 – Offset Voltage of the Op-Amp Causes a Total Error in the Output Voltage as if There Exists a Gain Error in the Circuit

2.3 The Origin of the Offset Error in CMOS Op-Amps and Inst-Amps

In order to know how to compensate the offset error in Op-Amps and Inst-Amps, a review of the origin of this error and the dominant contributing factors leading to offset error in CMOS amplifier design is presented. As a first step, an overview of random distribution of MOSFET parameters and their spreads is presented.

MOSFET devices have their drain currents determined by process factors such as μ, C_{ox}, V_T, λ, the geometry factors W and L, and the overdrive or bias condition $(V_{GS} - V_T)$. When a MOS device is used in the Strong Inversion (SI) region, the drain-to-source current is often given by the simple square law model as shown below.

$$I_D = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \approx \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 = \beta(V_{GS} - V_T)^2 \qquad \textbf{(2.2)}$$

Here I_D is the drain (or source) current, μ is the mobility factor, C_{ox} is the gate oxide capacitance per unit area, W, and L are width and length of the device, V_{GS} is the gate source bias voltage, V_T is threshold voltage of the MOS transistor, and finally λ is the channel length modulation factor, which is an indicative of small signal output resistance of the MOS device when used in saturation region. Often, the term $(1 + \lambda V_{DS})$ is dropped, and the process and geometry factors $\frac{\mu C_{ox} W}{2L}$ are combined, and shown as the transconductance factor β given in Eq. (2.2)

If the MOS device is used in Weak-Inversion (WI), which is also called sub-threshold, or exponential region, the dependence of the drain current on its V_{GS}, is more or less similar to a BJT device that is, showing an exponential relationship [7], [8], [9] .

$$I_D = I_{D0} e^{\left(\frac{V_{GS}-V_T}{nk\frac{T}{q}}\right)} \quad ; \quad I_{D0} = 2n\mu C_{ox}\frac{W}{L}V_{th}^2 = 4n\beta V_{th}^2 \qquad \textbf{(2.3)}$$

Here I_D is the drain current, I_{D0} is the specific current which is a function of process and geometry of the device, V_{GS} is the gate source voltage, V_T is the MOS threshold voltage, n is the sub-threshold slope factor, k is the Boltzmann's constant (1.38×10^{-23} J /K), T is the absolute temperature, and q is the electron charge (1.6×10^{-19} C). The term $V_{th} = kT/q$ is the well-known thermal voltage, which is 26mV at room (27ºC or 300K).

2.3.1 The Effect of Random Process Variations on Offset

Process variations in parameters affecting MOSFET drain current such as V_T, and μ, or lithographic errors in the fine geometries of today's MOSFETs transistors create device mismatches. This is critical for devices used at the input of the differential pair, or current mirrors. These mismatches are either directly seen as the input referred offset (such as V_T mismatches), or translated to an offset voltage through the transconductance (g_m) parameter of the first stage. The tighter the control on the process (the smaller the σ), the less is the input-referred offset.

Consider a MOS Transistor biased in Strong Inversion (SI), obeying the square law of Eq. (2.2). Suppose that thousands of such devices which were laid out equally are evaluated to extract the MOSFET parameters V_T, β, etc**.** If the number of transistors having a particular V_T for example, are graphed on a vertical axis with V_T being the horizontal axis, a Gaussian distribution is obtained with a mean value of $V_{T(avg)}$, and a standard deviation σ as a measure of spread of the parameter as shown in figure 2-5.

For a Gaussian distribution, only 0.5% of population has a V_T more than 3-sigma away from the average V_T. Experimental investigations have shown that sigma is inversely proportional to the square root of the area (WL) of the transistor [10], according to the equation:

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \qquad \textbf{(2.4)}$$

Where, A_{VT} is a process parameter.

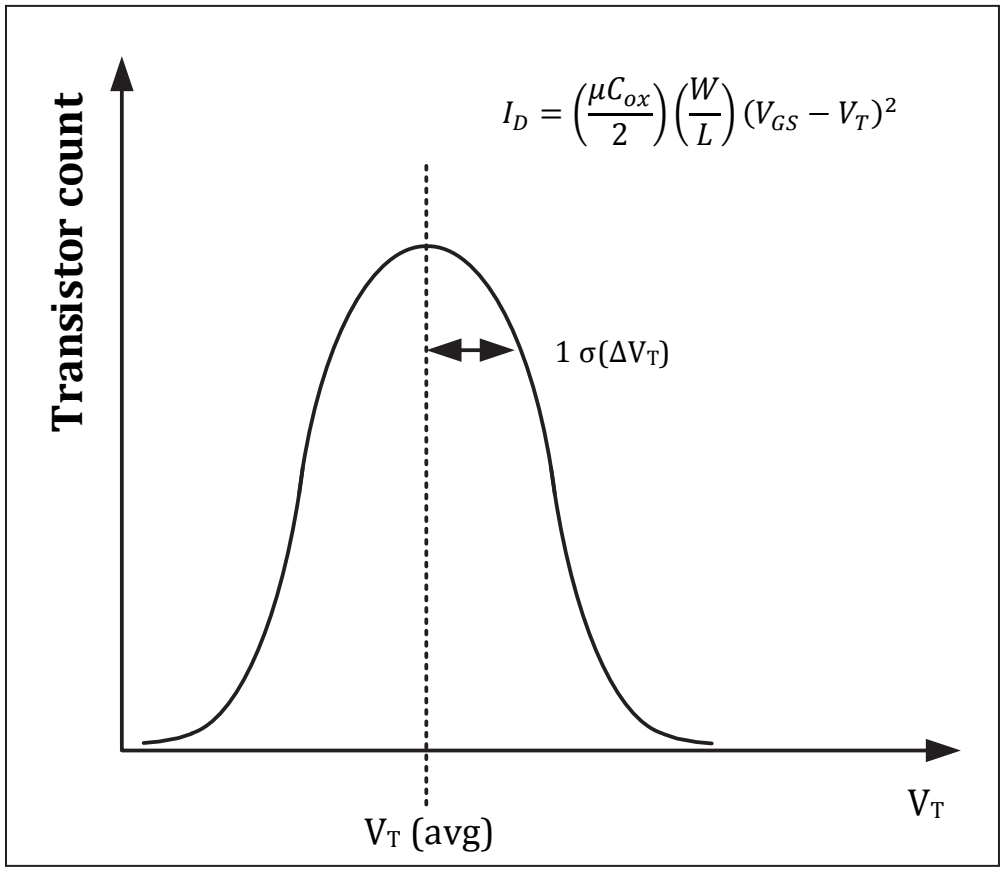

Figure 2-5 – Normal Distribution of Random V_T Mismatch Leading to Offset Error in Applications

As previously mentioned, since the V_T mismatch is seen directly as an offset voltage at the input of a differential pair amplifier, the lower this sigma then tighter is the spread, and the less is the resultant native input referred offset due to the V_T mismatch. For a realistic desired native offset design target, and within a process technology node (that is a known A_{VT}), the area increase is the only tool to reduce the imbalance due to the V_T mismatch at the input.

Since often there is a size limitation and thus cost penalty in achieving very low native offset targets, some sort of trimming or calibration (one time trim, or dynamic error cancellation) is needed to stay within reasonable transistor sizes while still achieving the desired low offset design targets.

Although the parameter A_{VT} is obtained from the design manual for a particular process, and technology node, a few good rules of thumb can be used to predict this parameter fairly accurately down to 0.18µ node. At the time of this thesis, the 0.18µ node is still considered the most widely used technology node in designing analog and power Integrated Circuits. However, the 0.18µ is gradually being replaced by 0.13µ, and beyond over the next few years. Some rule of thumbs to estimate gate oxide and spreading parameters in a given technology node are worth mentioning.

Rule of thumb 1: The Gate Oxide thickness of a MOSFET in a given technology node is roughly 1/50, or 2% of its minimum length L. For example, the gate oxide thickness for NMOS devices in a 0.25µ technology node is about 5nm.

$$t_{ox} \approx K_{t_{ox}}\ L_{\min}\ ; \quad K_{t_{ox}} \approx \frac{1}{50} \qquad \textbf{(2.5)}$$

Rule of thumb 2: The Proportionality constant A_{VT} (to calculate 1-sigma of V_T mismatch), for technology nodes down to about130 nm can be approximated as:

$$A_{VT} \approx K_{VT}\ t_{ox}\ ;\ \ K_{VT}\ \approx 1\text{V} \qquad \textbf{(2.6)}$$

As an example, the A_{VT} for NMOS devices in the above example for technology node of 0.25µ is roughly 5mVµm.

Rule of thumb 3: The spreading parameters (A_{VT}, A_{WL}, etc.) for PMOS devices are about 50% higher than NMOS. For A_{VT} this is mainly because of the higher substrate doping level in an n-well technology which relates A_{VT} to the 4th root of substrate doping.

Table 2.1 shows the mismatch coefficients of NMOS devices as a function of the technology node (minimum device length). The data is more or less in agreement with the above mentioned rules to obtain the gate oxide thickness, and the V_T spreading parameter A_{VT}.

L_{min} [µ]	2.5	1.2	0.7	0.5	0.35	0.25	0.18	0.13	0.09
t_{ox} [nm]	50	25	15	11	8	6	3.5	2.5	1.5
AVT [mVµm]	30	21	13	7.1	6	**?**	7	3.8	3.7
A_{WL} [% µm]	2.5	1.8	2.5	1.3	2	**?**	1	1	1.17

Table 2-1 – NMOS Mismatch Coefficients in Different Technology Nodes

Referring to table 2-1, it is clear that A_{VT} continues to decrease for smaller channel lengths, but the same is not true for A_{WL}, which seems to stay around 1% µm ~ 2% µm level regardless of the technology node [10], [11], and [12].

Figure 2-5 shows only the V_T spread, but similar statistics can be obtained for β or even its components such as W/L, or $\beta' = \frac{\mu\ C_{ox}}{2}$. Table 2-1 also identifies the spread for the geometry factor A_{WL}, which as mentioned, seems to stay constant independent of the technology node. All

such errors normally cause some imbalances in the drain currents of the input transistors in the input differential pair. These errors are translated to the input, often through the input stage transconductance (g_m) as an input-referred offset voltage. The next section describes in more detail the general effect of such parameters on the drain currents of MOSFET devices.

2.3.2 Drain Current Mismatch and the Consequent Offset Error

In the previous sections, the relationship between the drain current of a MOSFET and its gate-source controlling voltage for both Strong Inversion (SI) and the Weak Inversion (WI) was discussed. Here, the simplified version of Eq. (2.2) is rewritten for convenience.

$$I_D \approx \beta(V_{GS} - V_T)^2; \qquad \beta = \mu \frac{C_{ox}}{2}\frac{W}{L} = \text{Transconductance Factor} \tag{2.7}$$

In order to see the effect of process and geometry parameters on I_D, we take the total derivative with respect to V_T, and β as shown here.

$$dI_D = (V_{GS} - V_T)^2 \; d\beta - 2\beta(V_{GS} - V_T)\, dV_T \tag{2.8}$$

This simplifies to:

$$\frac{dI_D}{I_D} = \frac{d\beta}{\beta} - \frac{dV_T}{\frac{1}{2}(V_{GS} - V_T)} \tag{2.9}$$

The transconductance per unit drain current ($\frac{g_m}{I_D}$) in strong and weak inversions are given by:

$$\frac{g_m}{I_D} = \frac{1}{\frac{1}{2}(V_{GS} - V_T)} \qquad \text{For SI} \tag{2.10}$$

$$\frac{g_m}{I_D} = \frac{1}{n \cdot V_{th}} \qquad \text{For WI} \tag{2.11}$$

Substituting Eq. (2.10) in Eq. (2.9) reveals the changes in the drain current with respect to changes in β, and V_T. Also, in spite of the fact that we used SI equation to obtain this dependency, Eq. (2.12) is valid for WI as well, provided that Eq. (2.11) is used for g_m/I_D.

$$\frac{dI_D}{I_D} = \frac{d\beta}{\beta} - \left(\frac{g_m}{I_D}\right) dV_T \qquad \text{For both SI and WI} \tag{2.12}$$

Eq. (2.12) clearly reveals the dependency of I_D on transconductance factor β, transistor's bias transconductance g_m, and the threshold voltage V_T. Several immediate results are deduced here:

i. If only the effect of transconductance factor β is to be considered (dV_T is assumed to be negligible or zero), we obtain: in fact

$$\frac{\Delta I_D}{\Delta \beta} = \frac{I_D}{\beta} \qquad \text{for both SI and WI} \qquad \textbf{(2.13)}$$

This shows that the effect of the transconductance mismatch in both strong and weak inversions is directly scaled by the drain current itself. Hence, the effect of β mismatch is reduced with lowering the I_D. Normally in designs with lower I_D when speed and bandwidth are not of primary concern, the operating points are set in the sub-threshold region.

It is interesting to examine the contribution of the changes in β in Eq. (2.13) to a corresponding change in the offset voltage by assuming that the changes in I_D is just coming from an equivalent change in the offset voltage at the input (meaning that both V_{GS} and V_T are kept constant).

$$\Delta V_{os}\, g_m = \frac{\Delta \beta}{\beta}\, I_D \qquad \text{for both SI and WI} \qquad \textbf{(2.14)}$$

$$\Delta V_{os} = \frac{\Delta \beta}{\beta} \frac{1}{(\frac{g_m}{I_D})} \qquad \text{for both SI and WI} \qquad \textbf{(2.15)}$$

Eq. (2.15) indicates that any percentage of mismatch in β is going to be scaled by the inverse of $\frac{g_m}{\Delta I_D}$ to be seen as an input offset voltage. This means, the more the $\frac{g_m}{\Delta I_D}$ the smaller the effects of β mismatch. This condition is met in subthreshold region of operation for which the transconductance per unit drain current (g_m / I_D) is higher than that of the strong inversion.

We recall that for subthreshold operation, the transconductance g_m is proportional to the drain current itself, whereas it is proportional to the square-root of the drain current in strong inversion.

ii. If the effect of V_T mismatch is the dominant effect on I_D ($\Delta\beta$ is negligible or zero), then Eq. (2.12) becomes:

$$\frac{\Delta I_D}{\Delta V_T} = -g_m \qquad \text{for both SI and WI} \qquad \textbf{(2.16)}$$

This suggest that the changes in I_D due to V_T mismatch is directly scaled with ($-g_m$), in both strong and weak inversions. Moreover, since imbalances of the drain currents of any differential pair at the input stage of an amplifier are divided by gm in order to be seen as an input-referred offset, the mismatch in V_T in fact is directly seen as input-referred offset as expected.

Moreover, Eq. (2.16) suggest that the higher $\frac{g_m}{\Delta I_D}$, the larger $\frac{1}{\Delta V_T}$, or the smaller ΔV_T itself is, which again indicates that designing in weak-inversion could result in a lower sensitivity to this ΔV_T mismatch. Again as mentioned, this is due to the higher transconductance per unit drain current ($g_m / I_{D)}$ for weak-inversion in comparison to strong inversion.

iii. In general, both V_T, and β factor mismatches exist as Eq. (2.12) suggests. Since these parameters are non-correlated, the standard deviations of the above parameters are added in a root-mean-square (rms) fashion as shown here.

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_T)\cdot\left(\frac{g_m}{I_D}\right)^2 \quad \text{For both SI and WI} \qquad \textbf{(2.17)}$$

One has to remember to use the correct equation for $\frac{g_m}{I_D}$ in Eq. (2.17); that is Eq. (2.10) for SI, and Eq. (2.11) for WI as mentioned before.

3. Techniques to Reduce Offset Error

In previous sections it was shown that the native offset of CMOS amplifiers (usually the 6σ offset without any trim whatsoever) could easily be as high as 15 ~ 20 mV. Since multiple sigma statistical analysis for a production-worthy design is the common preferred choice (often 4σ for room and 6σ for over temp) the designer must bring the above large offset down to whatever is needed for the particular sensor class of interest; often by 1 ~ 3 orders of magnitudes. Other accuracy errors such as gain error and linearity error may also need trimming; however a detailed discussion of such error compensations is beyond the scope of this writing. A subsection is devoted to define such errors in Inst-Amps for reference.

Any error-removal technique that is based on a one-time trimming (adjusting the value of components or bias conditions just once to achieve a target performance specification) has the major disadvantage that the value of the trimmed component will change with temperature and time, causing a shift in the performance parameter itself. For example, if a trim of the source degeneration resistors in a transistor differential pair is done at room temperature to compensate for the offset error, the offset may not stay within specifications at extreme operating temperatures due to the shift in the value of the trimmed resistor. As a matter of fact, the tracking over the temperature, and time, are out of the picture in such trim schemes.

There are two main techniques to compensate the offset in Op-Amps and Inst-Amps, as follows:

i. Conventional Approaches to Remove Offset

ii. Dynamic Offset Cancellation Techniques

Only the first category is discussed in this chapter not only as a reminder, but also to appreciate the second category which is thoroughly discussed in the subsequent chapters.

3.1 Conventional Approaches to Reduce Offset

Most of these techniques involve a trim that is performed at a particular temperature, often room, and only once. All such methods are generally sensitive to a change in temperature as well as component aging. Some of the common locations within the circuit to perform the trim are:

1. Offset trimming at source degeneration resistors of the input differential pair transistors.

2. Offset trimming by size adjustment $\left(\frac{\Delta W}{L}\right)$ of the input differential pair transistors.

3. Offset trimming at degeneration resistors of current mirror load, or folded cascade.

4. Offset trimming by adjustment of the load current sources at the drain of differential pair transistors.

5. Offset Trimming by Addition of a Trimmable Current to one side of the Loads of a Differential Pair Transistors.

All the above trim-based offset cancellations suffer from the same issue of parameter shift over temperature range, as well over time from their adjusted trimmed values. This is in addition to incurring extra cost for the trim during production. Dynamic Offset Cancellation techniques do not have these disadvantages.

3.1.1 Offset Trimming at Source Degeneration Resistors of the Input Differential Pair Transistors

If transistors at the input differential pair of an amplifier have degeneration resistors at their sources, then a simple way to compensate for offset is to trim such resistors as shown in figure 3-1. This technique is more applicable to Inst-Amps, since most likely such degeneration resistors are added to improve linearity, and the span of the differential voltage at the input.

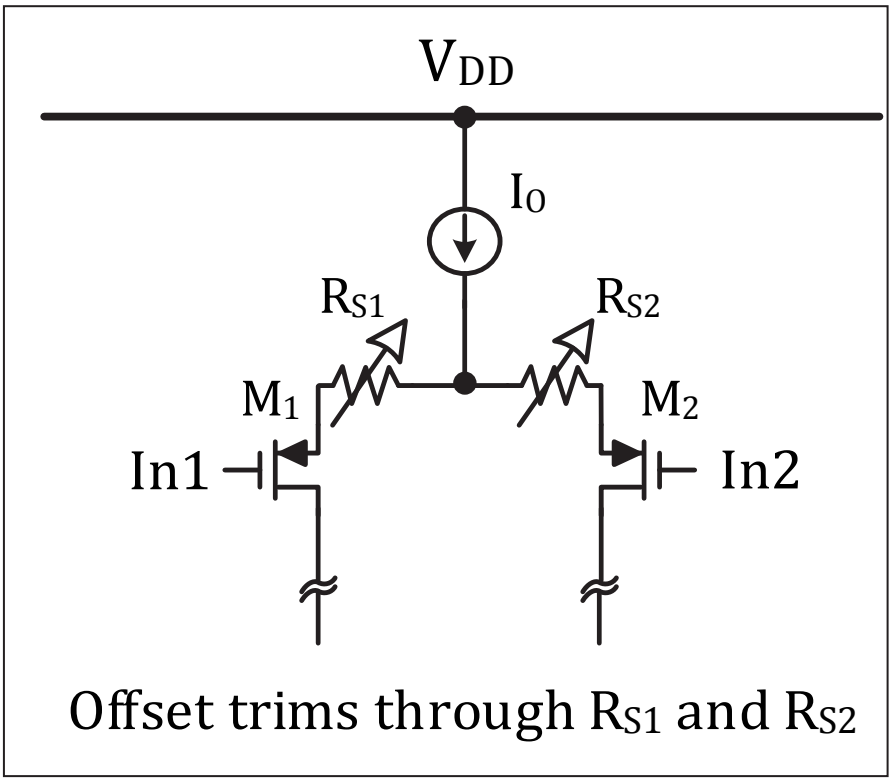

Figure 3-1 – Source Degeneration Trimming at Input Differential Pair

If degeneration resistors are thin film (Zero-TC) type, laser trimming at Wafer-Sort is an option (Wafer-Sort, and Post-Package Trims, along their advantage, and disadvantages will be discussed in the subsequent sections of this chapter). If instead of thin film, Poly resistors are used, then Resistor Network Trimming (RNT) can be used to tame the offset.

Also use is made of Zener-Zapping, Metal, or Poly-Fuses, to bring in or remove a resistor segment of the RNT into the circuit.

Knowing the fairly low resistance values of the RNT segments, CMOS switches are not the best candidates here, not only due to their large sizes for the required small resistance, but also for their $R_{DS\text{-}ON}$ being largely dependent on the supply voltage and temperature.

3.1.2 Offset Trimming by Size Adjustments $\Delta W/L$ of the Input Differential Pair Transistors

It is possible to adjust the current at each leg of the input differential pair, therefore trimming the offset, by adding or removing fractional size $\left(\frac{\Delta W}{L}\right)$ transistors to the main differential pair transistors. Poly-Fuse Links, or Laser Cutting Technique at Wafer-Sort can be used to disconnect a segment form the main transistors. When switches are employed for the task, they likely need to be PMOS and NMOS combinational analog switches due to the frequent requirement that the input stage of the amplifier operate from rail to rail.

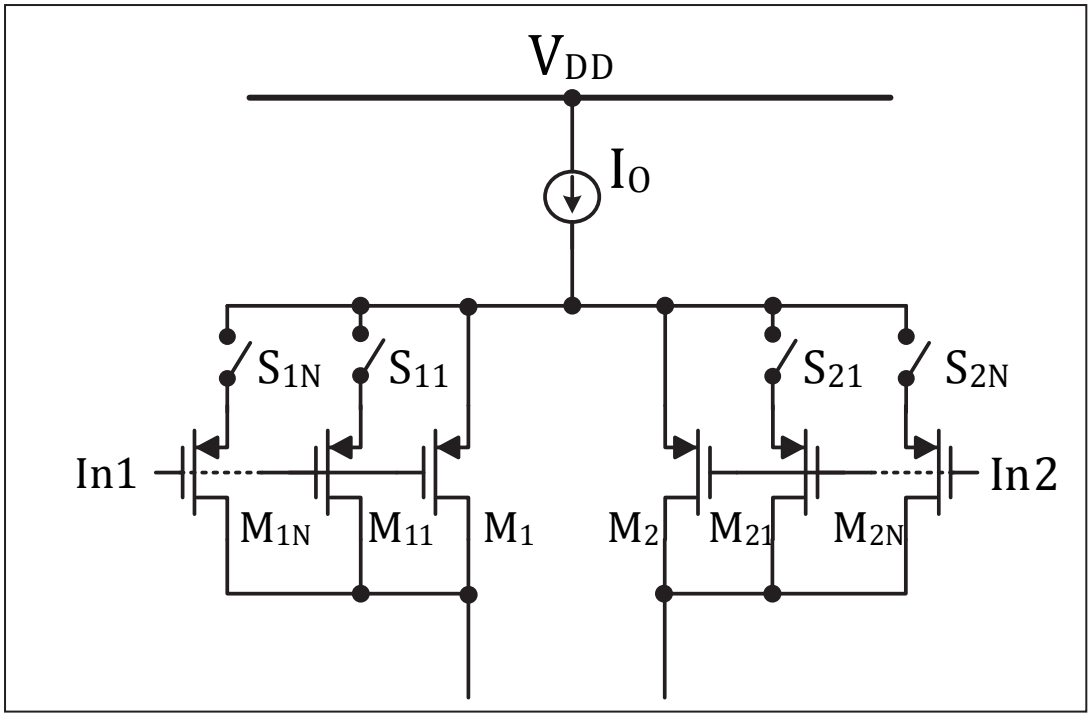

Figure 3-2 – Size Adjustment Trimming $\Delta W/L$ at Input Differential Pair

Figure 3-2 shows the principle of size adjustment using segmental transistors switched at their sources. It is also an option to switch the segmental transistors at their drains; but care should be taken not to use laser cutting due to their link residual resistances. The drains of the disconnected fractions should connect to the supply rail to prevent parasitic effects. Switches with only one

type of transistors are usually sufficient, as drain voltages are usually close to one of the rails [4].

3.1.3 Offset Trimming at Source Degeneration Resistors of Current Mirror Load or Folded Cascode

This trim can be done at the source degeneration resistor of a current mirror load for the input transistors of a differential pair, or equivalently, at the source degeneration resistors of a folded cascode configuration as shown in figure 3-3.

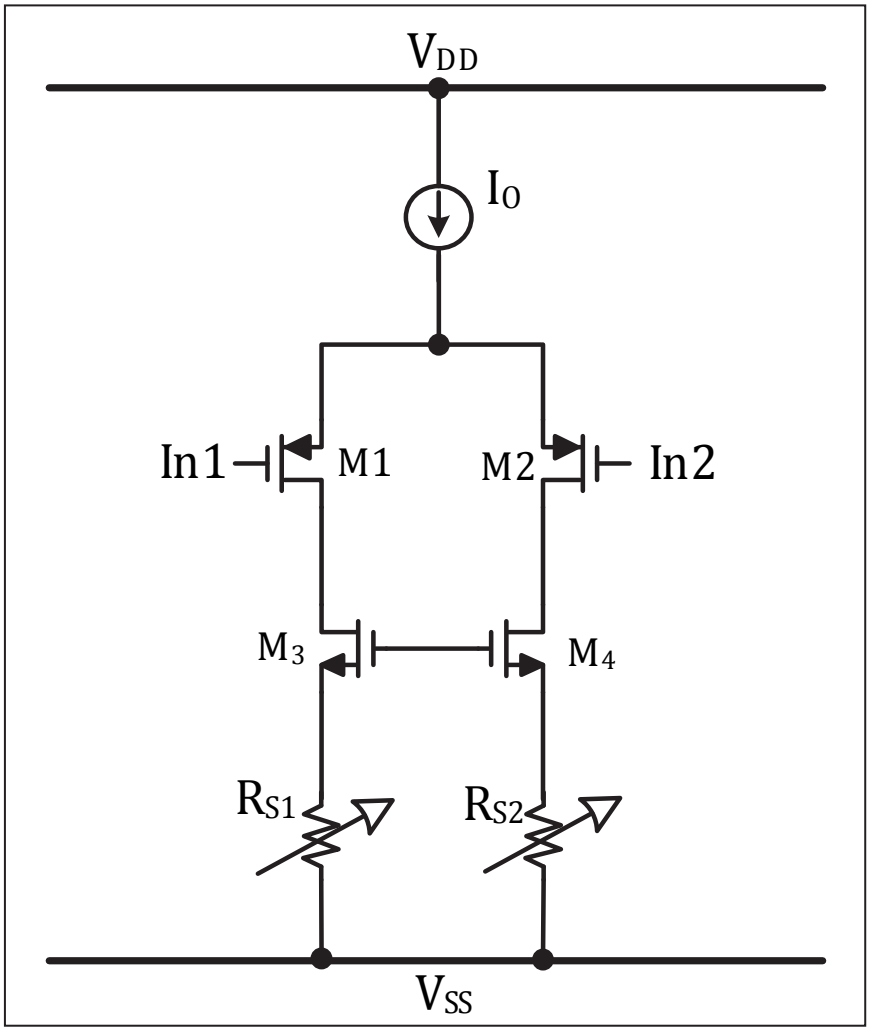

Figure 3-3 – Offset Trimming at Source Degeneration Resistors of a Current Mirror Load

Thin film resistors and laser trimming at sort are well-suited for this purpose. Resistor network trimming (RNT) can also be applied using metal or poly fuses and Zener zapping. CMOS switches are not optimal due to their RDSON dependence on supply and temperature.

3.1.4 Offset Trimming by Changing the Load Current Sources at the Drain/Source of the Input Differential Pair Transistors

This technique, similar to offset trimming at source degeneration resistors of current mirror loads, changes the load currents of the input transistors of a differential pair. Figure 3-4 shows such adjustments. Although the figure illustrates placement of the switches at the sources of the fractional transistors in parallel with the main current source transistors, it is also possible to move the switches to the drains of these fractional transistors as well.

The switches are fusing metal, poly links, or Zener-zap links as usual. If such switches are placed at the drains of fractional transistors, laser cut technology is not recommended due to the possible residual resistance of the link after cutting. The drains of the unused fractional transistors are connected to the supply rail to prevent parasitic effects. Using only one type CMOS switches (P or N) is allowed as the drain voltages are usually close to one of the supply rails [4].

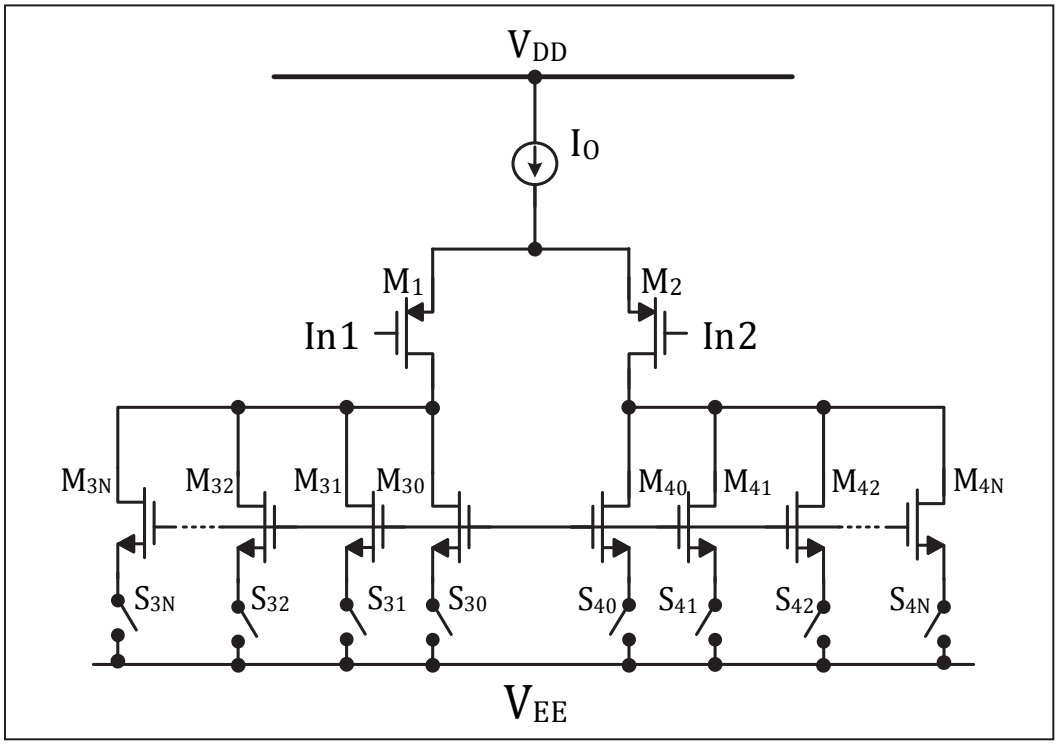

Figure 3-4 – Offset Trimming at Drain of Input Differential Pair through Load Adjustments

3.1.5 Offset Trimming by Addition of a Trimmable Current to One Side of the Loads of a Differential Pair Transistors

Again, an intentional mismatch in the currents of the main transistors of an input differential pair is achieved by addition of a trimmable current source to one side of the current sink load, as shown in figure 3-5. This current mismatch counterbalances the offset voltage when reflected back to the input through the transconductance of the input stage of the amplifier. If switches are

not used to steer the additional current to either side of the current mirror load, then the current mirror leg with the additional adjustable current source (here M3) is set to a lower current by at least the amount of $\Delta I = g_m \cdot V_{os_{(6\sigma)}}$. The adjustable current source itself is set to have a minimum variation of twice the difference, that is $2g_m V_{os_{(6\sigma)}}$. The term $V_{os_{(6\sigma)}}$ is referred to the 6-sigma value of the offset error in a normal/Gaussian distribution curve similar to figure 2-5.

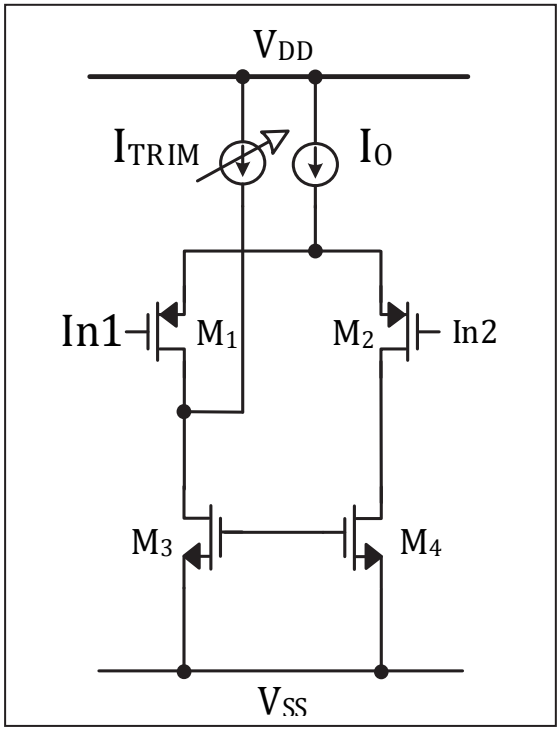

Figure 3-5 – Offset Trimming by Addition of a Trimmable Current Source to One Side of a Differential Pair Load

3.2 Trimming Step within the Production Flow

With regards to where in the production flow the trim is performed, there are two main options: Wafer-Sort Trimming (WST) and Post Package Trimming (PPT) as briefly discussed here.

3.2.1 Wafer-Sort Trimming (WST) and Associated Techniques

This method is rather old and costly. The trim, as the name suggests, is performed at Wafer-Sort by adjusting the values of some relevant components, through laser cutting of thin film resistors (such as source degeneration resistors of a differential pair), Zener Zapping a reversed p-n junction, size adjustments $(\frac{\Delta W}{L})$ on the input transistors of a differential pair, or by burning some metal or poly fuse links to remove the offset error. Any trim at Wafer-Sort requires extra trim contact pads for prober tips to do the job. The area consumed by such pads may often be significant, especially since they are not going to be part of the active circuitry right after trimming.

Also wear and tear, on the prober's tip, particularly when high currents are passing through them (Zener-Zap, or metal link fusing) is an ongoing issue at the production floor. Figure 3-6 shows the Zener-Zap trimming. Figure 3-7 is a representative of a metal link fuse trimming; and finally figure 3-8 shows a thin film laser trimming at sort.

Thin film resistors have extremely low temperature coefficients (almost zero), and as such are very popular, especially when laser technology is used for trimming.

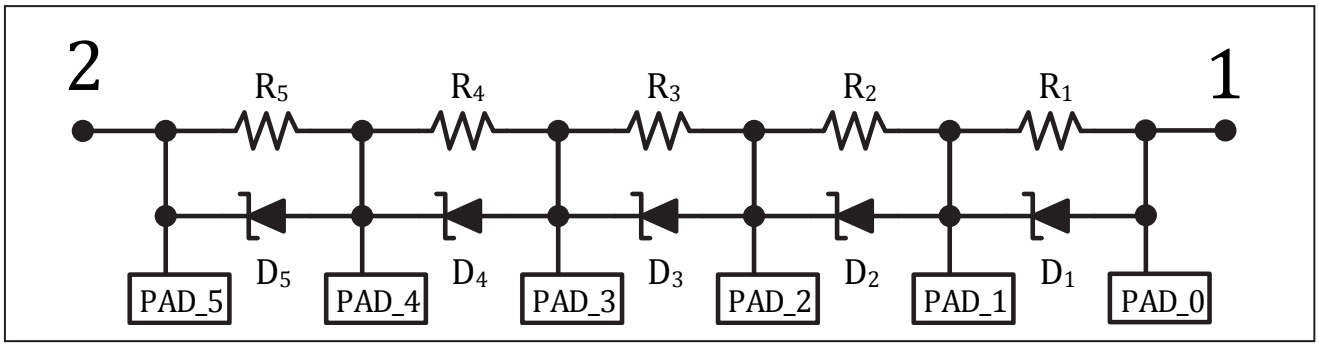

Figure 3-6 – Zener-Zap Trimming at Wafer-Sort

Note that not all process technologies have thin film resistors, as such the designer has to use poly resistors, sometimes complimentary (P-type and N-type which have different temperature coefficient polarities) to deal with the effect of temperature. This technique is preferred in the absence of thin film resistors, even if the trim is not performed at sort (for example PPT), or even in the case of dynamic element matching, when the designer prefers to start with a lower native drift with temperature.

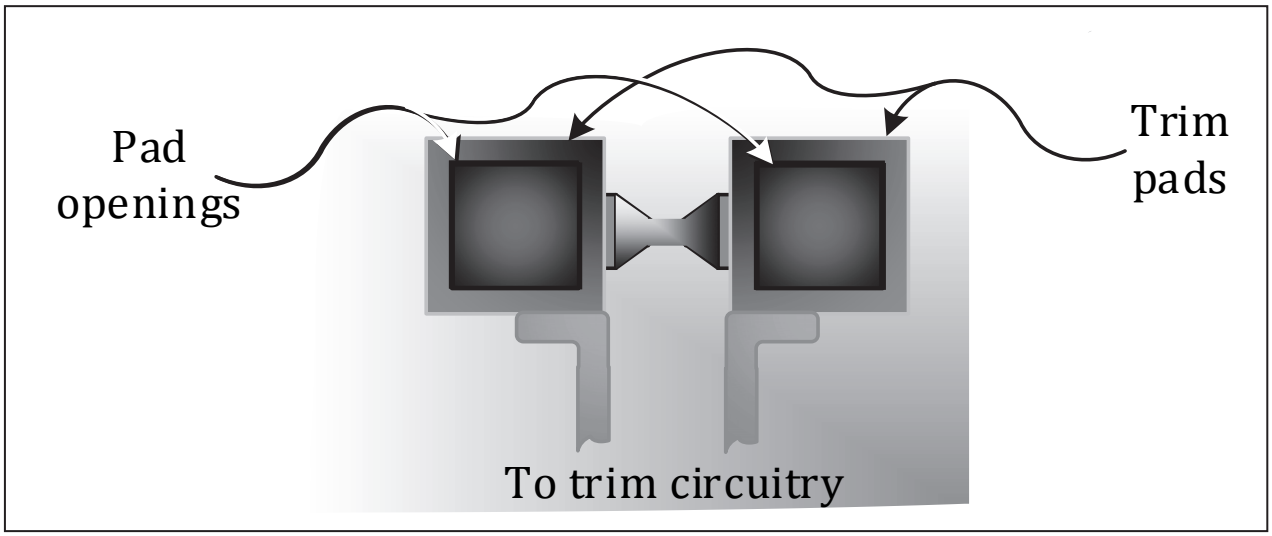

Figure 3-7 – Trimming through Burning a Metal Link Fuse

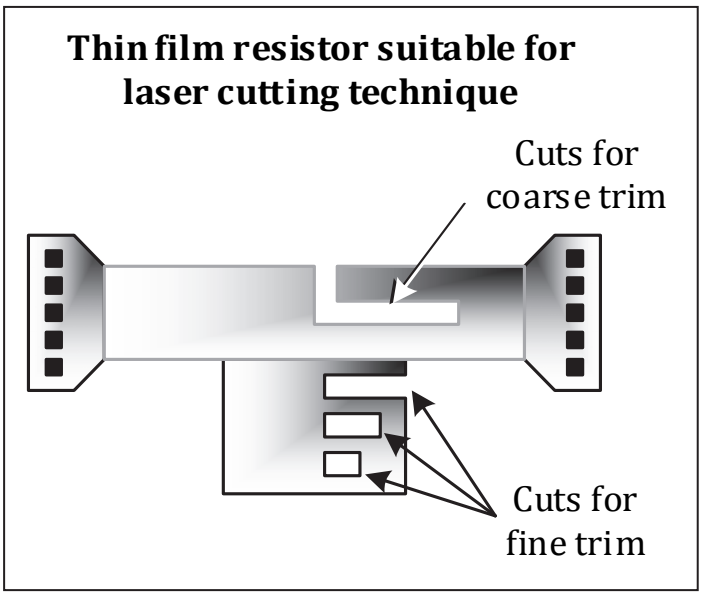

Figure 3-8 – Trimming Thin Film Resistor at Wafer-Sort

3.2.1.1 Advantages and Disadvantages of WST

The main advantages of Wafer-Sort trimming are its circuit simplicity and the maturity of the technique. However, many disadvantages have pushed the technique outside the mainstream of the cost-conscious flows of modern day production steps. Moreover, today's commercial, and industrial flows hardly cover any Wafer-Sort step, due to cost considerations (except big die for expensive packages), let alone trimming at this level. The exceptions are big die in expensive packages, or custom flows for special cases such as military products, or Wafer-Level Chip-Scale Packaging (WLCSP, also called WLP or CSP for short) for which the trim is performed on an already finished and bumped wafer.

Any such trim requires additional process steps to protect the silicon underneath of the component being trimmed, due to the heat generated at the component. In addition, often an opening in the top passivation above the component is needed for the trim. This is usually considered a reliability issue since in plastic packages (non-hermetic packages) moisture can penetrate into the package and become trapped underneath as well as above the unavoidable cavity around the trimmed component. Corrosions, and/or creations of thin Aluminum traces (Whiskers) causing conduction through an already-fused link are well known examples of such reliability issues.

One of the most troublesome issues with Wafer-Sort trimming is the assembly shift in the trimmed value after the die is packaged. No matter how accurate the trim, assembly and Post-Package shifts will almost always throw the centered value often way off.

If the shift caused by the pressure on the top surface of the die due to rough plastic grains against the surface of the chip, the remedy is likely to use a Polyamide layer, also known as Die-Coat, which acts like a cushion to absorb the pressure. However this requires an additional step in the production process (Die-Coat Mask), and thus an added expense to the die cost. The inexpensive Drop-On / Spin Polyamide technique is no longer used in today's thin packages due to the thickness of the Die-coat layer generated with this technique.

Another disadvantage of WST, which is shared with the next best one-time trimming approach (Post-Package Trimming, PPT) is the drift with temperature and time as previously mentioned.

3.2.2 Post-Package Trimming (PPT) and Associated Techniques

With Wafer-Sort being essentially phased-out of the production flow, designers have to use other means to perform trimming, if dynamic cancellation is not used for offset or other error compensation. The trim is performed after the die is packaged, so it has the obvious advantage of eliminating any assembly shift in the values of components at the die level.

One of the most commonly used PPT technique is zapping a Poly or a Metal Fuse Link within a Read Only Memory (ROM) cell. The output of this cell drives a switch in the actual trim circuitry. The change in the logic state of the ROM cell is made by burning a Fuse element. This is done by passing a relatively large current through the Fuse, via the enabling of a relatively strong but small switch (a MOS device capable of handling fusing current of 20 mA ~ 50 mA) which is in series with the Fuse itself. At the same time a sufficiently-high voltage (*V*-Zap; often 5V ~ 12V) is used as the power supply for the series combination of the Fuse and the Switch as shown in figure 3-9.

The current to fuse a Metal-Link is generally much higher than that for poly fuses (in the order of 100mA ~ 300mA), therefore Metal-Links are less likely to be used if the lower current Poly-Fuses are available. In designing the Zap circuitry for the ROM, read-back circuitry is added to assure that the Poly-Link is properly burned, and its resistance is higher than the minimum acceptable resistance (normally set to few hundreds of kΩ) to insure the proper state of the logic desired.

Generally the Poly-Fuse technique does not require extra mask steps in fabrication.
Today almost all major foundries / technology nodes offer Poly-Fuses with no additional cost, except if use is made of their patented / proprietary IP to perform trimming.

The number of bits required to store a trimmed value to cancel offset or any other accuracy error is limited to some few tens of bits, which adds only minimal cost to the die.

Most recently, One-Time Programming (OTP), Multiple-Time Programming (MTP), EEPROM, and Flash Memories, which are all digital based techniques, are gradually pushing the Metal and Poly-Fuses out of the picture.

All the newer methods are based on logic memory cell techniques. They generally offer lower programming currents and the same or lower programming voltages, as well as much smaller size for a much larger bit counts when compared to their Poly or Metal-Fuse ROM counterparts.

The programming voltages, which are normally higher than the supply voltage of the chip, can be either generated internally through a charge pump or similar circuitries, or provided externally through an unused or reassigned package pin.

All PPT circuitries need necessary digital signals and power for the trim circuitries. These signals are generally the clock (CLK), Data, and Programming, or the Zap voltage source. If there are not enough package pins available to bring the CLK, Data, and Programming Voltages to the on-chip trim circuitry, then other pins which are normally assigned for other functions are required to be reconfigured, and reassigned functions to bring these signals to the trim circuitries inside the chip.

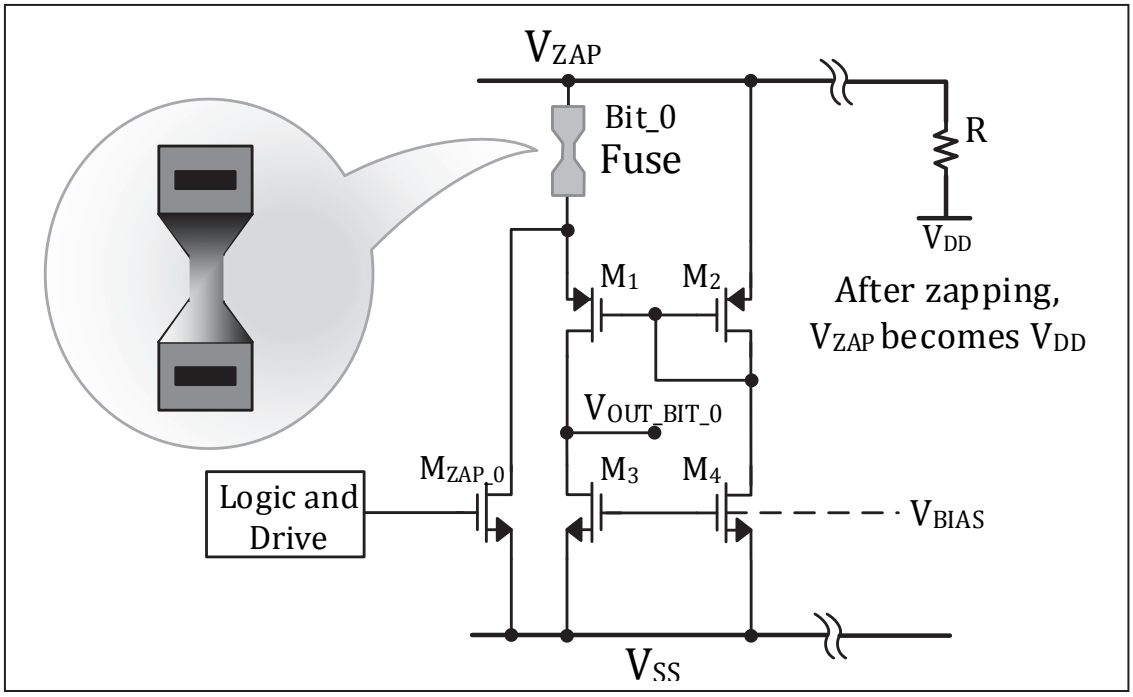

Figure 3-9 – ROM Poly-Fuse Link in PPT and its Associated Mismatched Current Mirror Read Circuitry. Here $(W/L)_{M1} > (W/L)_{M2}$. The Out_Bit0 Changes from High to Low After the Trim

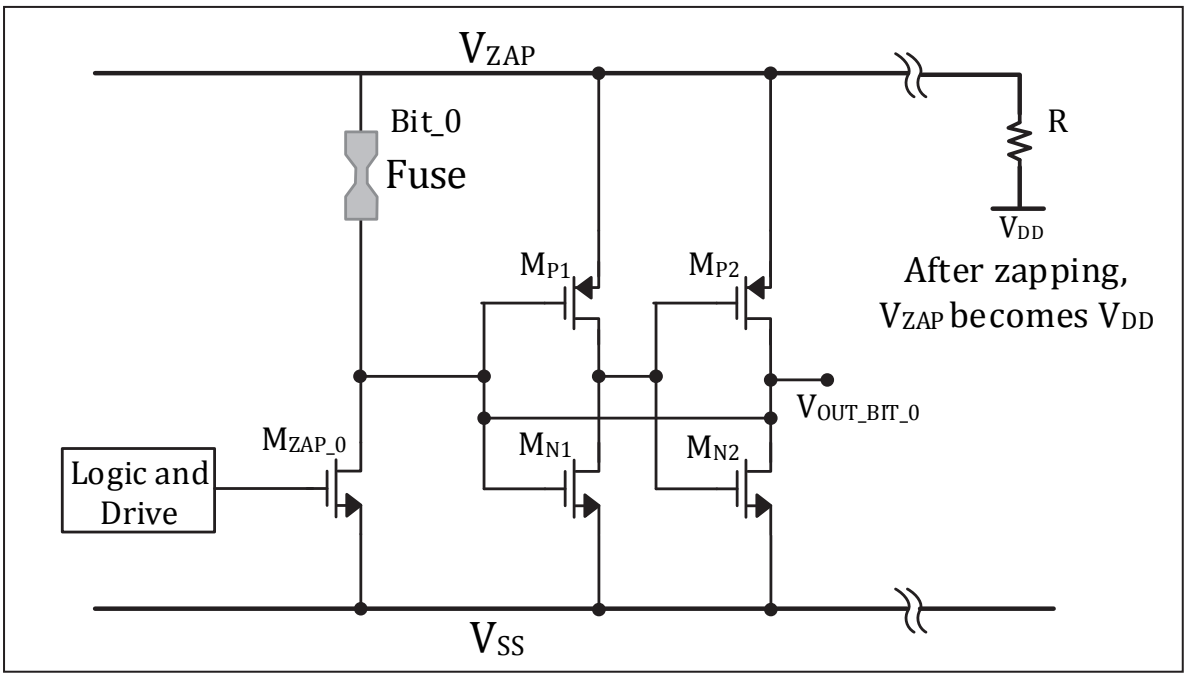

Figure 3-10 – ROM Poly-Fuse Link in PPT and its Associated Latch Read Circuitry

3.2.2.1 Advantages and Disadvantages of PPT

The main advantage of the PPT is the fact that the trim is performed after the chip is assembled into to its intended package; therefore the assembly shift issue seen with WST is completely removed. Nonetheless, PPT still suffers from the shift in the trimmed parameter (offset) with temperature and time.

PPT is generally more reliable than WST because there is no opening in the passivation, similar to the likely case of laser trimming. However the reliability of Poly-Fuse type PPT has always been a concern. Incompletely burnt fuses, or full or partial re-conduction of a previously blown fuse, especially if a non-optimal programming current is used, have occasionally been observed and reported throughout the industry. All suppliers of Poly-Fuse, Flash, or EEPROM based memories must provide their reliability and retention data to the user, preferably prior to the project launch (design start), and certainly way before the production qualification, and ramp up begins.

There is still an added cost at Final Test (FT) step of production, no matter what trim technology is used. Further, if some more modern PPT techniques such as Flash, or EEPROM are used, there would be an added die cost due to the extra additional steps and required masks during the fabrication of the chip.

3.3 Dynamic Offset Cancellation (Real Time Offset Removal)

As the name suggests, this is a technique that removes the offset dynamically in real time, as such to a good degree of accuracy, its performance is temperature and time independent. The two know methods for such a technique are:

i. Auto-Zeroing, which is based on sampling technique.

ii. Chopping, based on modulation technique.

Since the chapters five and the subsequent chapters of this writing are about the newer Chopper Stabilized Chopper Techniques, the detailed discussions of such methods are described in the aforementioned chapters.

3.3.1 General Advantages of Dynamic Offset Cancellation (DOC) Techniques

Before even getting to the detailed descriptions and circuitries of such methods, we can generally foresee the great advantage of the method compared to the conventional approaches.

As the main advantages of this technique, one can pinpoint to the independency of the trimmed offset in regards to temperature, and time. Any conventional trim (WST or PPT) is performed at one particular temperature (normally room); as such is very sensitive to the changes in the environmental temperature, or the shift of the component values from their original value with time due to aging.

Another advantage of the DOC is its insensitivity with respect to the assembly shifts such as Post-Package plastic mold pressure. This sensitivity, and the resultant change in the original trimmed value is due to plastic mold grains pressure against the die surface, and is normally seen to be more sever for NMOS as compared to PMOS devices. Although using Die-Coat is a known solution, it is costly, and yet another added step to the process. The DOC is more effective than PPT in removing plastic pressure, since the first method is performing the trim in real-time and reacts to any such changes just continuously.

Generally speaking, all the DOC techniques can achieve higher accuracies than conventional offset removal methods, provided that careful circuit and layout designs have been taken into considerations.

Table 3-1 shows a general view on the comparison of different Offset removal techniques.

Technique	Achievable Offset Range	Circuit Complexity	Package & Assembly Shift	Temperature Drift	Time Drift	Reliability
Wafer-Sort Trimming	~0.5mV	Simple	High	High	High	Medium
Post-Package Trimming	~100μV	Medium	Low	High	High	Medium
Dynamic Offset Cancellation	~10μV	Medium to Complex	Very Low	Very Low	Low	High

Table 3-1 – Comparison of Different Offset Removal Techniques for CMOS Amplifiers

3.4 A Short Review of Accuracy Errors in Inst-Amps

As per the previous discussion, the major performance parameters of a MOS amplifier in DC or low frequency applications are the offset and low frequency noise characteristics.
Moreover, in instrumentation amplifiers, besides the offset it is common to specify two other *DC* accuracy errors which are called Gain Error (sometimes referred to as slope error, or rotational error), and linearity error.

In summary, the three accuracy errors are:

i. Offset Error

ii. Gain Error

iii. Linearity Error

As mentioned, Op-Amps data sheets generally specify the offset error only, however Inst-Amp data sheets usually present all three to cover *DC* accuracy specification parameters.

When a small signal is amplified, the total error , i.e. the difference between the ideal or expected amplified value and the measured quantity (the real value), is often decomposed to the above three error types as shown in the following figures.

Figure 3-11 shows the test bench to determine such errors. The decomposed errors, along with the coordinates for total error with respect to the differential input voltage are shown in Figure 3-15. The differential input voltage on the horizontal axis is swept around its common mode value in both directions. This is performed only if the Linearity error is to be determined as the

offset and gain error are single point ($V_{in} = 0$), and two points $\left(V_{in_{dif}} = V_{in_{dif-min}}\right.$; and $V_{in_{dif}} = V_{in_{dif-max}}\left.\right)$ for offset and gain errors respectively.

The vertical axis shows the total error associated with instrumentation amplifier.
The simplest way to look at this total error ($V_{err_{tot}}$) is actually to subtract a scaled down version of the measured or simulated differential output ($V_{out_{dif}}$) from the differential input ($V_{in_{dif}}$) itself. The scaled down factor is the ideal gain (G_I), as shown in below.

$$V_{err_{tot}} = \frac{V_{out_{dif}}}{G_I} - V_{in_{dif}} \quad \textbf{(3.1)}$$

If the input-referred offset and linearity errors are V_{os} and $V_{e_{lin}}$ respectively, and the measured (actual) gain is (G_a), then we can rewrite the Eq. (3.1) as:

$$V_{err_{tot}} = \left(\frac{G_a}{G_I} - 1\right) V_{in_{dif}} + V_{os} + V_{e_{lin}} \quad \textbf{(3.2)}$$

Or:

$$V_{err_{tot}} = \varepsilon_{\text{gain}}\, V_{in_{dif}} + V_{os} + V_{e_{lin}} \quad \textbf{(3.3)}$$

Where $(\varepsilon_{\text{gain}})$ is the Gain Error, or alternatively the slope factors in figure 3-12 to figure 3-15, and $V_{e_{lin}}$ is the added value for all non-linear error terms referred to the input. If non-linearity is negligible and is ignored, the two other errors fit a straight line with the slope equal to gain error and vertical shift equal to offset. If the transfer function plot of the Inst-Amp, that is $V_{out_{dif}}$ vs. $V_{in_{dif}}$ is considered and not the total error voltage ($V_{err_{tot}}$) vs. $V_{in_{dif}}$, then the slope factor is gain itself, and not the Gain Error.

Figure 3-12 shows Total Error Characteristics for an ideal Inst-Amp with no accuracy errors. The curve for $V_{err_{tot}}$ is actually a horizontal line passing through the origin. This means there is no vertical shift (no Offset Error), zero slope (no Gain Error), and no deviation from a straight line (no Linearity Error), unlike what is shown in all the other figures for Total Error Characteristics.

Figure 3-13 shows the Total Error Characteristics for an Inst-Amp with offset error only. Added to this error is the gain error, which together with the offset error is shown in figure 3-14. As said, the gain error is a slope (rotational) type of error, and as such can never be compensated by offset error which is a vertical shift type of error on the same coordinates. This is why gain error and offset errors have different trims within the design.

Finally, figure 3-15 depicts the real-world case with all three error components present.

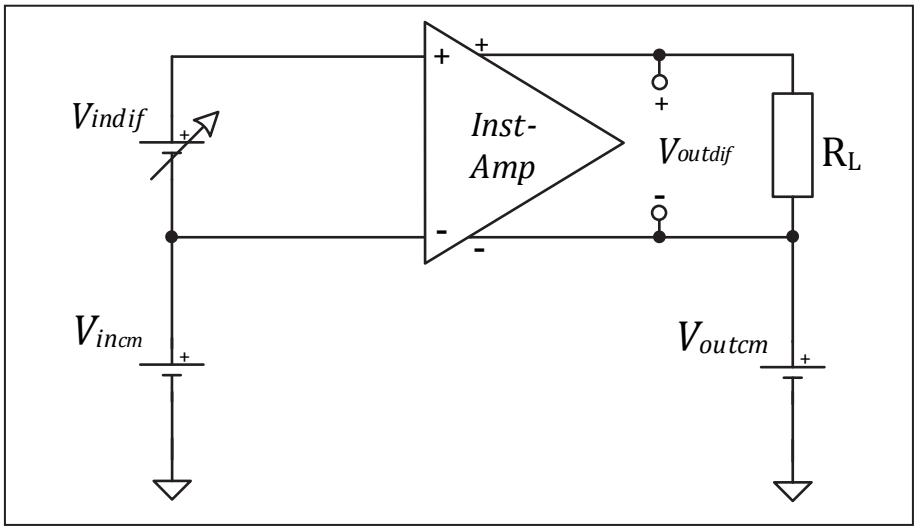

Figure 3-11 – Test Circuit to Measure Accuracy Errors in Inst-Amps

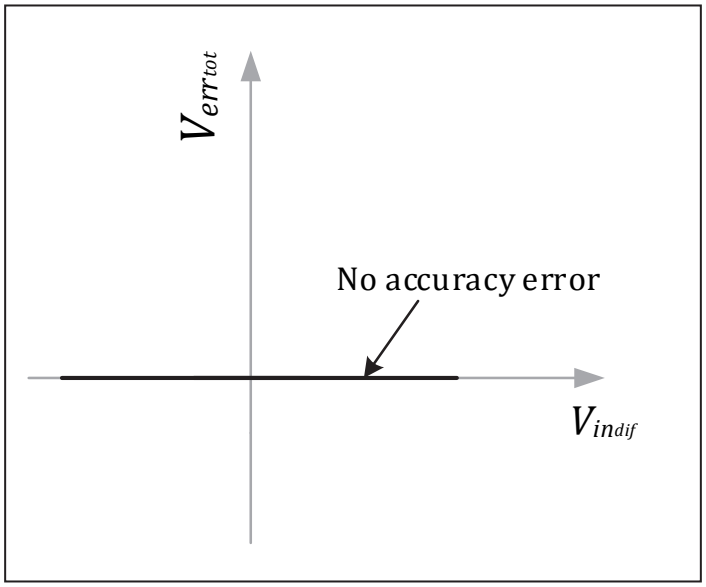

Figure 3-12 – Total Error Characteristics for an Inst-Amp with No Accuracy Errors (Ideal Inst-Amp)

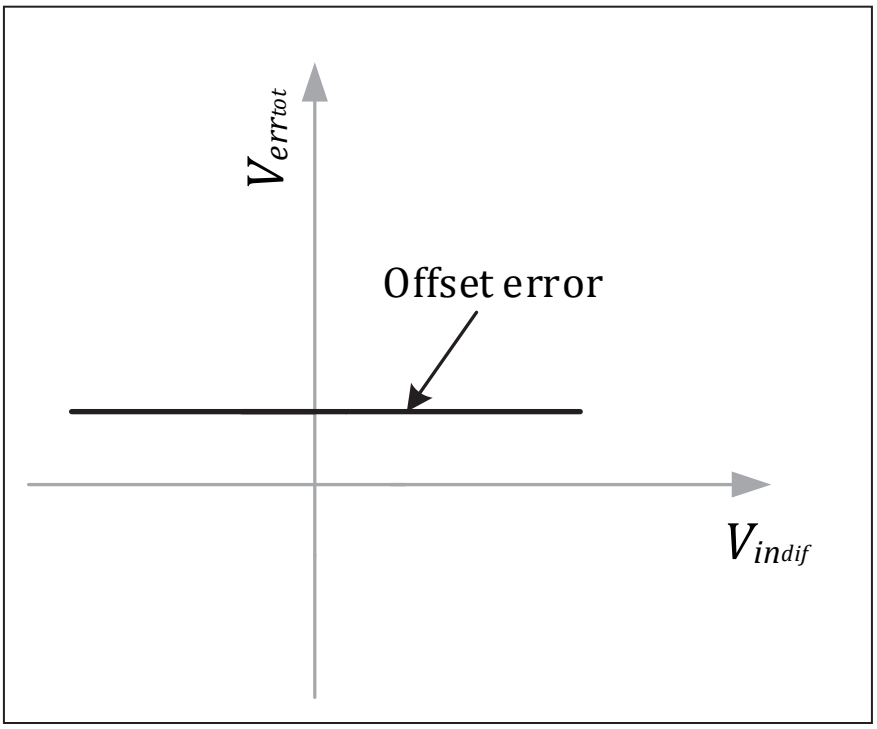

Figure 3-13 – Total Error Characteristics for an Inst-Amp with Offset Error Only

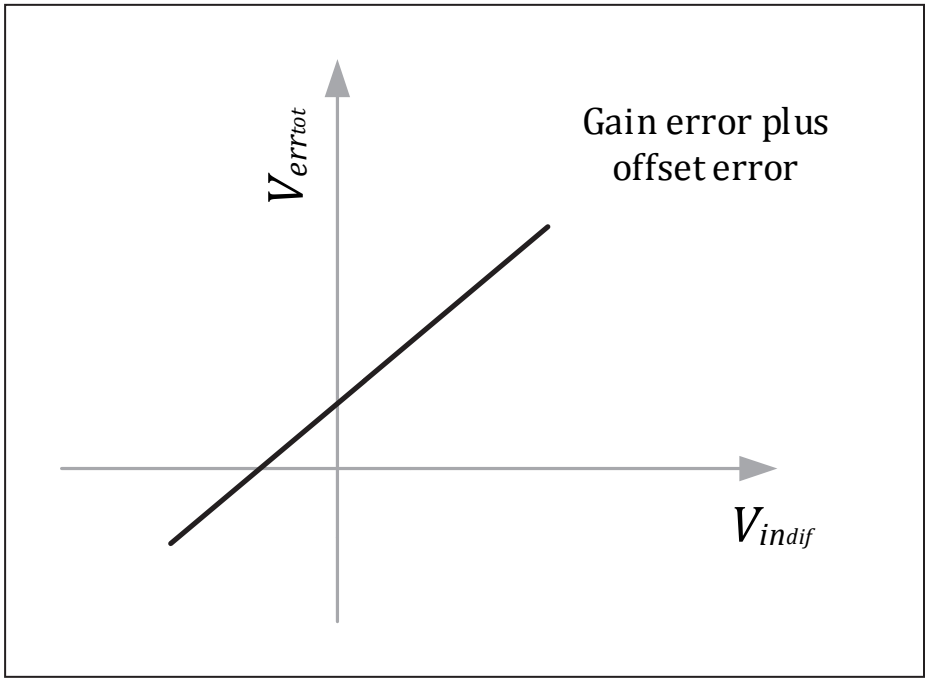

Figure 3-14 – Total Error Characteristics for an Inst-Amp with Offset and Gain Error

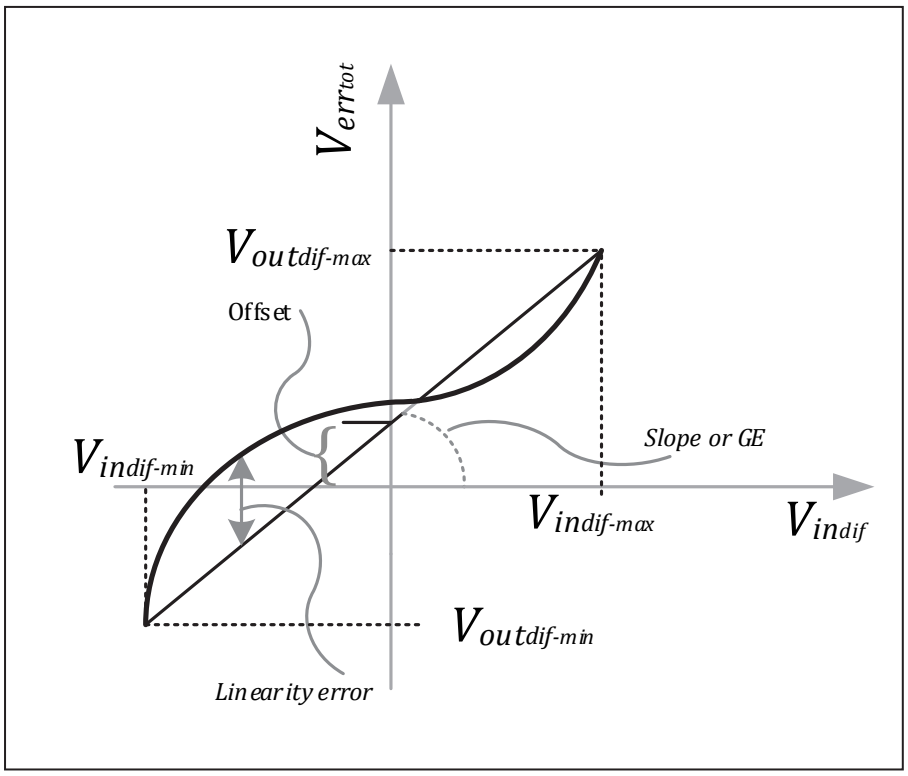

Figure 3-15 – Total Error Characteristics for a Real World Inst-Amp with Offset, Gain, and Linearity Errors

3.5 A Practical Note on Over-Temperature Performance Assurance and Misinterpretation of Performance Guaranteeing Term GBD

Since the subject of IC temperature testing was only briefly discussed in section 1.1.1, it is worthwhile to just mention a few remarks here, in particular since the performance of any Inst-Amp or Op-Amp is often required to be assured over some specific temperature range**(s)**.

Unless the chips are tested with a military standard such as MIL-STD-883 (which mandates production testing to cover the range of -55°C to +125°C), outgoing testing of today's manufacturing flows are mostly concerned the Industrial Flow Testing only (that is temperature range of -40°C to +85°C).

Moreover, the actual testing outside room temperature (27°C) is often performed for the purpose of characterization (on a limited sample size only), and not as a step in the production flow for every outgoing unit shipped to customers.

This single insertion outgoing Final Test (FT) approach for which the outgoing units are only tested at room is adapted for the purpose of cost saving and fast delivery to intended customers.

Nonetheless, most of the datasheets (D/S) for almost any product in any category (including Inst-Amps and Op-Amps) claim functional and parametric performances over a temperature range, which is often the Industry range shown in table 3-2.

How is this Possible? At first it looks as if this over-temperature performance guaranteeing is out of reach; however the issue is taken care by means of statistical analysis on practical data from an accepted sample size to be discussed shortly.

As known to many, the performance of the parts over the temperature is just Guaranteed By Design (GBD) and not production tested. However the term (GBD) is often severely misunderstood or misinterpreted, even by many less experienced Design Engineers (DE) and Product Engineers (PE) within the industry.

A misunderstanding often arises here as some engineers and business managers interpret GBD as the "Simulation Work and Results" performed by the design engineer throughout the design phase of the chip. This is absolutely wrong**,** and no customer would be convinced ordering millions of parts based on just simulation results performed by designers.

What is more**,** the model inaccuracies for some parameters in a new design, and more dangerously in a new process could be real killers. The only acceptable performance guarantee is getting the results of a statistical analysis on the testing of a good sample size of units. This means looking at the functionality and performance of the real silicon itself; therefore:

The term Guaranteed By Design (GBD) refers to a statistical analysis of an acceptable sample size of units tested at Room, Hot, and Cold (See table 3-2), preferably containing all parameters within the datasheet, but certainly those parameters with a specified value in the Minimum ("Min") or Maximum ("Max") columns of the Data-Sheet (D/S).

Product and Design Engineers will analyze the statistical data on every single parameter within the D/S and often set the final D/S limits based on a Six Sigma Distribution and analysis, in addition to taking into consideration all other error sources.

These error sources are associated with testers and their inaccuracies, tester to tester variability, test hardware to test hardware variability, tester and hardware repeatability, manufacturing test site to site variability so on and so forth.

This Six Sigma analysis is mostly considering those parameters with at least a "Min" or "Max" value in the D/S, not necessarily those with typical ("Typ") values.

The above is true since often there is no liability for the manufacturers in regards to any deviation from one or all typical values in the D/S, but care must be taken not to misuse this freedom as otherwise it rightfully reflects negatively on the quality of the D/S.

The higher the Sample Size for GBD the better and more reliable the D/S and Final Test Program limit settings become. If the samples are tested at room and over temperature by an Automatic Test Equipment (ATE), few hundred, or even thousands of units are preferred with

the slightest impact on the time spent on the tester or on analyzing the data. Often the ATE setup-time is more time-consuming than merely the time required for testing a few hundred units themselves.

If the GBD is done by an engineer or a technician on the bench, the number of units tested is significantly lower, especially if no automated bench testing tool or software is available.

In the past, a minimum of 33 units (32 sample and one control unit) were often quite acceptable by many Quality-Assurance (QA) departments at chip manufacturers here in Silicon Valley, Bay Area California.

Last, the following Table lists the major grade categories along with their Temperature Ranges which for long have been adapted by the worldwide IC industry.

Grade Category	Temperature Range (°C)	Remarks
Commercial	0 to +70	Some Manufacturers increase the upper range to +85°C.
Old Industry	-25 to +85	This grade is seldom used nowadays.
Industry	-40 to +85	This is the most widely used category for consumer and industrial products. Very few manufacturers increase the upper limit to +100°C
Automotive-Dashboard	-40 to +110	"Infotainment" or "Dashboard" Temperature high side is lower than "Under the Hood" automotive. The dash-board higher range is often limited to 105°C or 110°C.
Automotive-Under the Hood	-40 to +125	Under the Hood Electronic and Temperature Range
Extended	-40 to +125	Non-Consumer Industrial Products / Industrial Control.
Military	-55 to +125	Often for Military use according to U.S. Department of Defense (U.S. DOD) governed by the military standard MIL-STD-883.

Table 3-2 – Common Industry Grades and their Temperature Ranges

4. Dynamic Offset-Cancellation (DOC) Techniques: Auto-Zeroing, A Sampling Based Approach

As mentioned earlier, conventional techniques for cancelling of offset errors and their indistinguishable counterpart, low-frequency noise, are based on methods that remove the process and random errors at only a particular temperature (usually room: 27°C or 300K). These techniques do not offer the same performance accuracy over temperature or time as they do at room, simply because such costly trims are not real-time error removing techniques. Obviously, they offer the best accuracy just at the temperature for which trimming is done. The result is rather large errors over temperature and time, commonly known as drift over time and temperature.

In contrast, there are techniques which continuously measure such low frequency errors and cancel them by almost real-time subtraction of the measured error values from the mixture of signal plus error within the amplifier. It is as if one is constantly trimming the circuit for removing the offset and low frequency noise, regardless of temperature, or time. As such, to the first degree of approximation, there would be no temperature, or time dependency (drift) for offset, and noise. These Techniques are known by various terms such as "Dynamic Offset Cancellation" or sometimes "Dynamic Element Matching".

As stated earlier, the two known types of such offset cancelation techniques are:

i. Auto-Zeroing (Analog or Digital), which is based on sampling and is discussed in this chapter.

ii. Chopping, which is a modulation based technique; this is the subject of discussion in following chapters.

4.1 Auto-Zeroing: A Sampling and Storage Based Technique

This sampling technique to remove offset and low frequency noise is based on the subtraction of errors from the desired signal in a circuit with at least two successive clock phases:

1) Sampling the offset and low frequency noise and storing the charge associated with the error as a voltage in a capacitor called the sampling capacitor during a phase Φ1.

2) Applying this voltage to the input or output of the amplifier during a second phase Φ2, along with the amplification operation. This phase is called the amplification or execution phase.

During this phase, the sampled offset, and low frequency $\left(\frac{1}{f}\right)$ noise data held at the capacitor is getting subtracted from the signal source; cancelling the offset and noise to the first degree of approximation.

Based on the configuration, there are few main types of Auto-Zeroing approaches to be considered:

1. Output Offset Storage (OOS)
2. Input Offset Storage (IOS)
3. Using an Auxiliary Amplifier in a Closed Loop Configuration
4. Ping-Pong Configuration

In addition to this, also some techniques performed at system level will be considered, such as:

5. Self-Calibration or Digital Offset Storage and Control Technique
6. Auto Calibration (Digital Signal Processing Approach

4.1.1 Output Offset Storage (OOS)

In output offset storage technique, as the name suggests, the storage capacitor is placed at the output of the amplifier to remove its offset by subtracting the output referred offset from the amplified signal.

Two topologies shown in figure 4-1 and figure 4-2 are for single-ended and differential amplifiers, respectively. Figure 4-3 shows the non-overlapping clock for driving the switches.

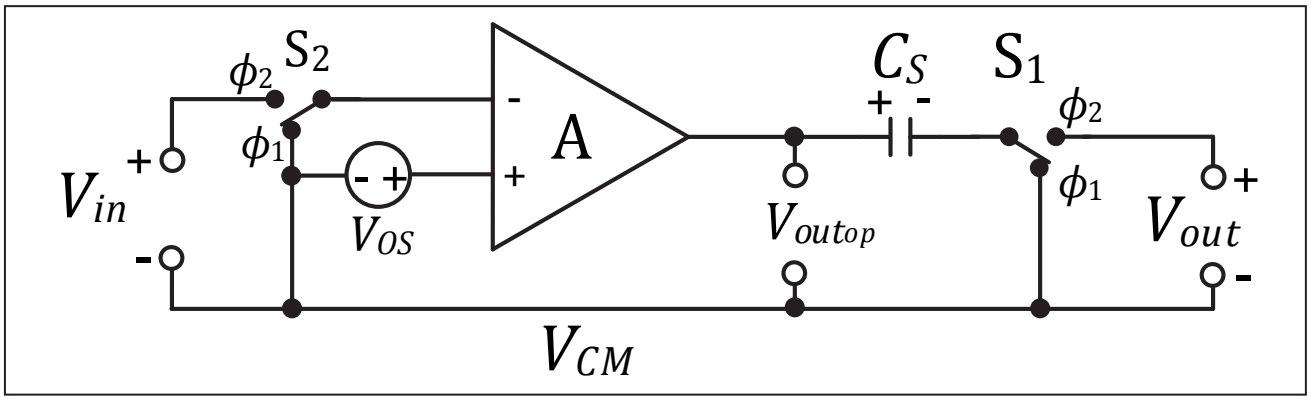

Figure 4-1 – Output Offset Storage for a Single-Ended Amplifier (OOS-SE)

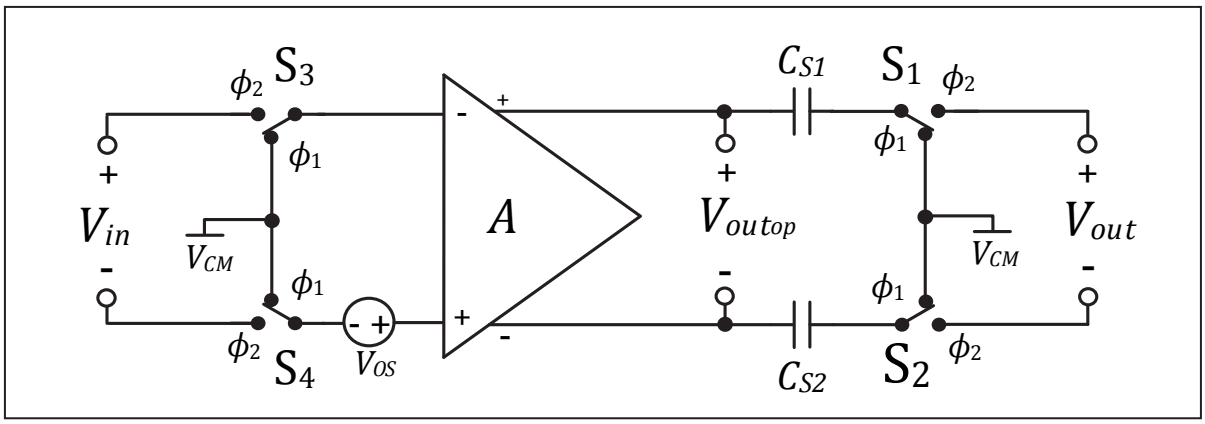

Figure 4-2 – Output Offset Storage and Cancellation for a Differential Amplifier (OOS-DF)

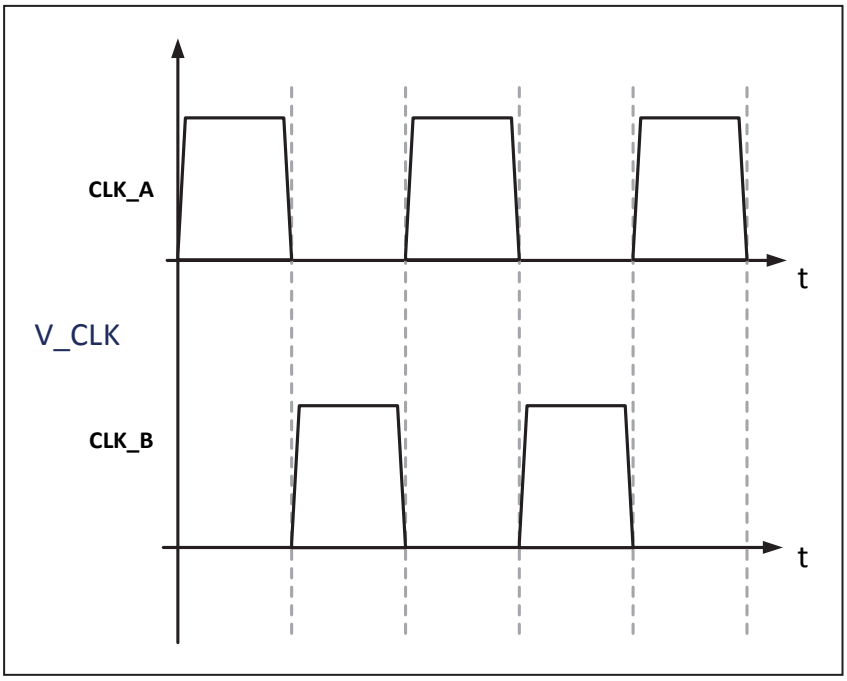

Figure 4-3 – Non-Overlapping Clock to Drive the MOS Switches

Two distinguished non-overlapping clock phases are:

i. Φ1, the sampling phase

ii. Φ2, the amplification phase.

During the sampling phase Φ1, the inputs of the amplifier are shorted together. After the voltages are settled in the circuit, the amplified version of the input referred offset will appear at the output of the amplifier and is stored in the sampling capacitor C_s.

Neglecting the non-idealities of the switches and the capacitors, (these will be discussed later), we have:

$$V_{out_{op}} = V_{Cs} = AV_{os} \quad \textbf{(4.1)}$$

where $Vout_{op}$ and V_{os} , are the output voltage and offset of the amplifier, respectively, and V_{Cs} is the voltage stored in the capacitor.

During the second phase Φ2 (Amplification phase), the input of the amplifier is connected to the input voltage V_{in} through switch S_2, whereas the output of the amplifier is connected to the output of the circuit through the sampling capacitor C_s and switch S_1.

It is clear that:

$$V_{out_{op}} = -A(V_{in} - V_{os}) \quad \textbf{(4.2)}$$

Therefore:

$$V_{out} = -V_{Cs} + V_{out_{op}} = -AV_{os} - A(V_{in} - V_{os}) = -AV_{in} \quad \textbf{(4.3)}$$

Thus to the first degree of approximation, offset error is out of the picture; however non-idealities of the circuit, primarily those of the switch and sampling capacitor, will introduce some residual offset that can be modeled as:

$$V_{os_{resi}} = \frac{(\Delta q_{inj1}) + (\Delta q_{Cs})}{A\ C_s} \quad \textbf{(4.4)}$$

Here, Δq_{inj1} is the total charge-injection stored in sampling capacitor C_{s1} through switch S_1, and Δq_{Cs} is the average capacitor's charge loss in the leakage paths during the amplification phase. The latter has an effect of lowering the capacitor voltage (the sampled offset) during the amplification phase. The droop rate of the capacitor voltage is a function of the leakage currents, capacitor value, and the time period for which the amplifier is in its amplification phase. The most straightforward way to reduce the residual offset error in general is to choose a smaller switch and, within allowable practical boundaries, a bigger sampling capacitor. Other practical considerations, in particular those associated with the layout of the chip, should also be taken into account.

The differential circuit shown in figure 4-2 is working based on the same principle as the single-ended version with the same sampling and amplification phases, however the offset is stored in capacitors C_{s1} and C_{s2}, and the residual offset is given by:

$$V_{os_{resi}} = \frac{\left(\frac{\Delta q_{inj1}}{C_{S1}} - \frac{\Delta q_{inj2}}{C_{S2}}\right) - \left(\frac{\Delta qc1}{C_{S1}} + \frac{\Delta qc2}{C_{S2}}\right)}{A} \quad \textbf{(4.5)}$$

Where Δq_{inj1} and Δq_{inj2} are the charge injections through the switches S_1, and S_2 stored in C_{S1} and C_{S2} respectively, and A is the voltage gain of the amplifier.

The losses Δq_{Cs1} and Δq_{Cs2} are the average charge losses in the sampling capacitors C_{S1}, and C_{S2} due to the voltage drooping throughout the amplification phase, caused by leakage paths. Often the second terms in the numerators of Eq. (4.4) and Eq. (4.5) are ignored, especially when sampling is performed at higher frequencies.

It is clear that if switches S_1, and S_2, as well as capacitors C_{S1} and C_{S2}, are completely matched, the first term in Eq. (4.5) will also vanish. In reality this is never the case and the choice is to reduce charge injection, and select larger sample capacitors for a known voltage gain. The latter is limited by the amount of the initial offset and supply voltage as will be seen shortly.

4.1.1.1 Advantages and Disadvantages of Output Offset Storage (OOS)

The advantage of the output offset storage is its simple implementation.

For the disadvantages, we notice that according to (4.1), during the sampling phase the output of the amplifier equals the input offset voltage multiplied by the gain of the amplifier. For large offset values and smaller supply voltages (a typical case in CMOS battery-operated handheld devices), the voltage gain of the amplifier is bounded by the inequality:

$$A \leq \frac{V_{sup_{min}} - \Delta V}{2\left(V_{os} + V_{in_{\max}}\right)} \quad \textbf{(4.6)}$$

where ΔV is the headroom needed to keep the internal transistor(s) at the output stage in their amplification region (saturation region for MOS devices, and linear region for Bipolar counterparts). This limits the usefulness of Auto-Zeroing at the output to lower gain applications. $Vsup_{min}$ is the minimum supply voltage, and V_{os}, and $V_{in_{\max}}$ are the offset voltage and the maximum signal voltage at the input of the amplifier.

As an example to quantify this limitation, assume the (OOS) technique is used in a battery-operated device with a supply voltage of 3V with a +/- 10% variation. If the headroom ΔV is 200 mV and the peak input voltage and offset are 100mV, and 20mV, respectively, using (4.6) reveals that the gain should be 10 or less to prevent saturation at the output stage of the amplifier.

Another disadvantage common to all output storage and cancellation techniques is the fact that input differential pair is still unbalanced even though the offset is removed at the output, thus degrading the CMRR of the amplifier.

The Auto-Zeroing at the output of an amplifier has also the common disadvantage of switched capacitor circuits; which is having a capacitor in the signal path for a fraction of the clock period. This makes the amplifier ac type, and discontinuous, often leading to presence of spikes at the output synchronized with the clock edges. The choices of smaller switches and larger capacitors would reduce this effect.

4.1.2 Input Offset Storage (IOS)

In this technique sampling capacitor is placed at the input of the amplifier, as shown in figure 4-4 and figure 4-5 for single-ended and differential topologies, respectively.

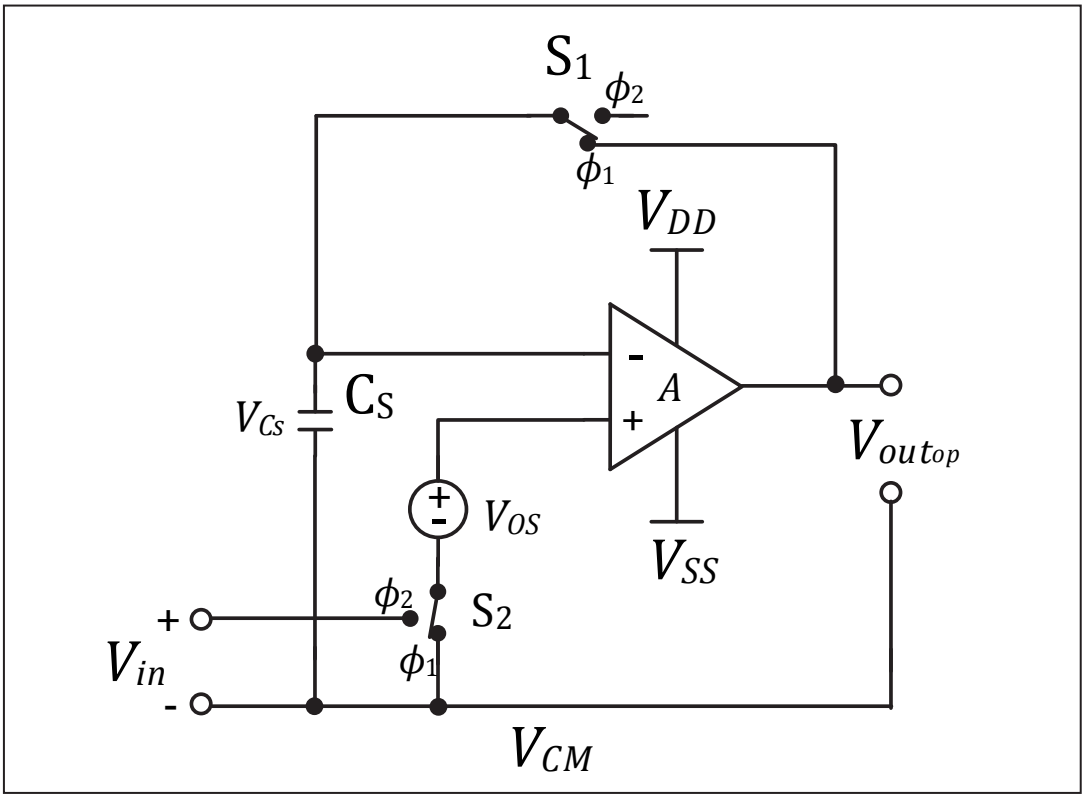

Figure 4-4 – Input Offset Storage – Single-Ended Amplifier (IOS-SE).

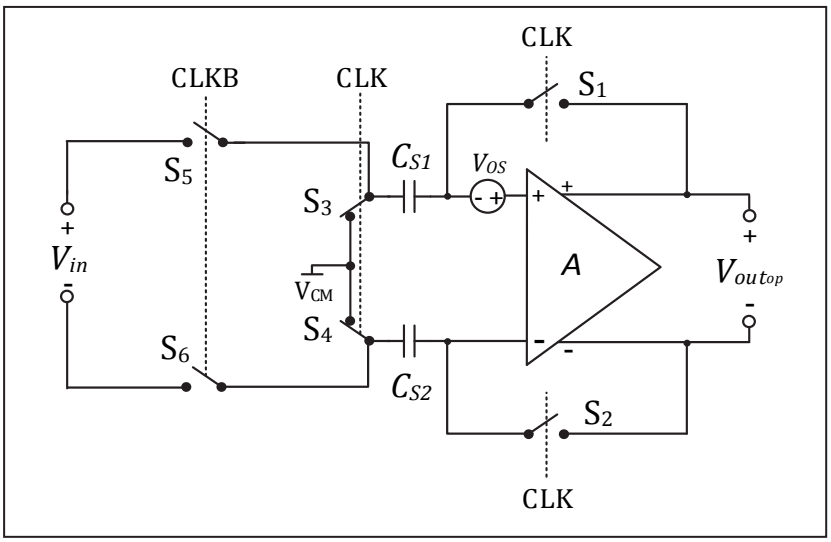

Figure 4-5 – Input Offset Storage – Differential Amplifier (IOS-DIF)

Looking at figure 4-4, and during the sampling phase Φ_1 it is clear that:

$$-V_{out_{op}} - \frac{V_{out_{op}}}{A} + V_{os} = 0 \tag{4.7}$$

Or:

$$V_{out_{op}} = V_{Cs} = \frac{AV_{os}}{A+1} \tag{4.8}$$

During the amplification phase Φ_2, and applying Eq. (4.8), $Vout_{op}$ can be written as:

$$V_{out_{op}} = A(V_{in} + V_{os} - V_{Cs}) = AV_{in} + \frac{AV_{os}}{A+1} \tag{4.9}$$

Therefore the residual offset is expressed as:

$$V_{os_{resi}} = \frac{V_{os}}{A+1} + \frac{\Delta q_{inj1} + \Delta q_{Cs}}{C_s} \tag{4.10}$$

In Eq. (4.10) the second term is added to account for switch charge injection and the charge loss of the sampling capacitor during the amplification phase.

Here again, the Δq_{inj1} and Δq_{Cs} are the charge injection through switch S_1, and charge loss in C_s throughout the amplification phase, which is caused by leakage paths.

Note that for a high gain amplifier the residual offset is practically determined by the second term of Eq. (4.10), which is independent of the amplifier's gain (a result of the fact that the

sampling capacitor is no longer at the output). Therefore in order to reduce such errors, the sampling capacitor size should be increased within its practical limits. Moreover, the increase in the value of C_s reduces the effect of parasitic capacitances at the input of the amplifier, which are another source of error in the circuit.

A relative measure of quantization of the magnitude of the error associated with the combined charge injection of the switch and charge losses of the sampling capacitor, that is the second error term in Eq. (4.10), can be estimated as such: for each femto-Coulomb of the combined ($\Delta q_{inj1} + \Delta q_{Cs}$), together with a pico-Farad size of a sampling capacitor, a one milli-Volt residual offset would result. In practice, the value of the sampling capacitor is about an order of magnitude bigger.

Auto-Zeroing at the input of a differential amplifier shown in figure 4-5 is based on the same principle as that of the single-ended amplifier.

It can be shown that residual offset in this case is: check polarities, third term +(+,-).

$$V_{os_{resi}} = \frac{V_{os}}{A+1} + \left(\frac{\Delta q_{inj1}}{C_{S1}} - \frac{\Delta q_{inj2}}{C_{S2}}\right) - \left(\frac{\Delta qc1}{C_{S1}} + \frac{\Delta qc2}{C_{S2}}\right) \qquad \textbf{(4.11)}$$

Again we notice that the input-referred offset is reduced with an increase in gain of the amplifier, however the second and third terms which represent the charge injection of the switches S_1 and S_2, and the charge losses of the capacitors C_{S1}, and C_{S2}, are not affected by gain since the capacitors are at the input of the amplifier. However in the differential amplifier case, the charge injection of the switches are trying to cancel each other, so if the switches are exactly matched, the charge injection error vanishes completely.

4.1.2.1 Advantages and Disadvantages of Input Offset Storage (IOS)

The main advantage of Input Offset Storage (IOS) is the fact that unlike its (OOS) counterpart, it does not limit the gain of the amplifier. Moreover, the higher the gain is, the lower the input-referred offset voltage.

Another advantage is the improvement of the CMRR, since the offset is removed right at the very input of the amplifier and the differential pair remains balanced.

As a disadvantage, the second and third error terms (charge injection, and charge losses errors) are not suppressed by the gain of the amplifier. Moreover, the amplifier is required to be unity-gain stable because during the sampling phase it is configured as a unity-gain stage. Another disadvantage, which is common in all switching circuits, is the existence of the sampling capacitors in the signal path. This makes the amplifier discontinuous in time.

4.1.3 Using an Auxiliary Amplifier in a Closed Loop Configuration

The presence of the sampling capacitors in the signal path for both OOS and IOS techniques are considered a disadvantage. The bottom plate parasitic capacitance may reduce the magnitude of the poles in the circuit, therefore adversely affecting the phase margin [14], however an alternative technique can be used to eliminate this shortcoming.

This technique to remove the offset and $\frac{1}{f}$ noise is based on using an external amplifier (called Auxiliary Amplifier) in a feedback loop, which in essence separates the signal path from the storage capacitors, as described in this section.

There are different types of "auxiliary amplifier loop" configurations depending on whether the feedback loop is terminated at the input or the output of the main amplifier. Figure 4-6 shows this offset cancellation technique with the feedback signal returned to the input of the main amplifier, whose voltage gain, and offset voltage are A, and V_{os} respectively.

Looking at figure 4-6, the auxiliary amplifier with the voltage attenuation $A_{a,}$ and the offset Vos_a is at work during sampling phase Φ_1, where the inputs of the main amplifier with voltage gain A, and offset voltage V_{os} are shorted together at a common-mode voltage level V_{CM} through switch S_2.

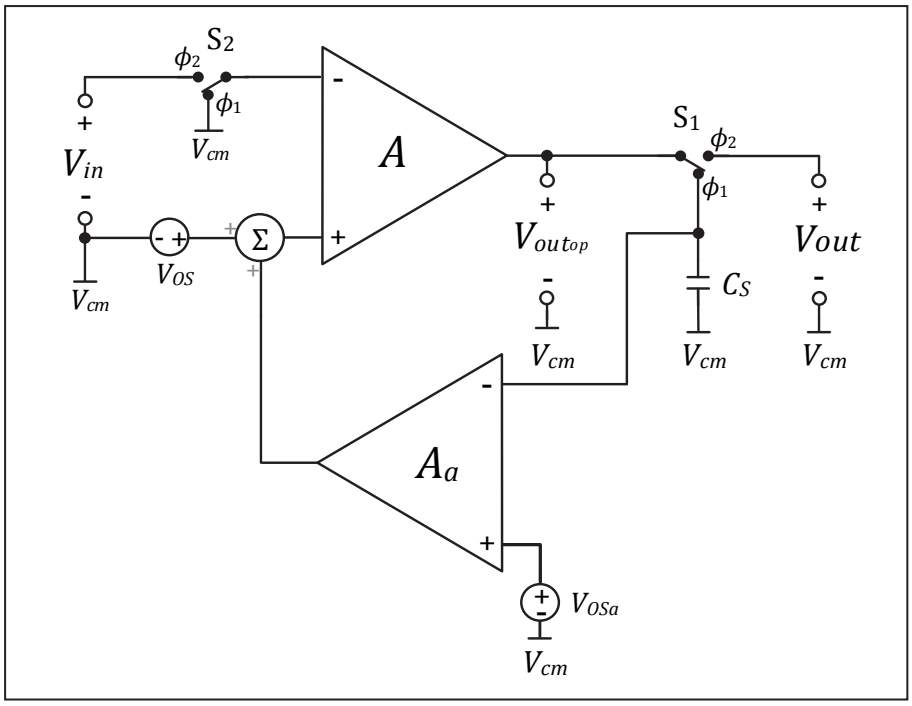

Figure 4-6 – Offset Cancellation using an Auxiliary Amplifier at the Input of the Input Stage of the Main Amplifier

During this sampling phase, the main amplifier is disconnected from the signal path, and its output voltage, or the voltage across the sampling capacitor which is now connected to the output of the amplifier through switch S_1, can be determined from:

$$V_{out_{op}} = AV_{os} + A\,A_a\left(V_{os_a} - V_{out_{op}}\right) \quad \textbf{(4.12)}$$

The above yields:

$$V_{out_{op}} = \frac{AV_{os}}{1 + A\,A_a} + \frac{A\,A_a V_{os_a}}{1 + A\,A_a} \approx \frac{V_{os}}{A_a} + V_{os_a} \quad \textbf{(4.13)}$$

Where the approximation is based on the assumption that $A\,A_a \gg 1$.

In the amplifying phase Φ_2, when the amplifier is placed in the signal path through S_1, and S_2, the output of the circuit V_{out} is expressed as:

$$V_{out} = A(V_{os} - V_{in}) + A\,A_a\left(V_{os_a} - V_{out_{op}}\right) \quad \textbf{(4.14)}$$

Substituting (4.13) into (4.14) results in:

$$V_{out} = -AV_{in} \quad \textbf{(4.15)}$$

So to the first degree of approximation, the offset of the main amplifier is completely removed. However in reality, when the switch S_1 moves from Φ_1 to Φ_2 position, there would be some charge injection Δq transferred to C_s through the parasitic capacitances of the switch. Since the feedback loop is now open, this error is not suppressed by the auxiliary amplifier, therefore a residual offset will directly be present at the input of the main amplifier, proportional to A_a, and expressed as:

$$V_{os_{resi}} \approx A_a \frac{\Delta q}{C_s} \quad \textbf{(4.16)}$$

This is why the gain of the auxiliary amplifier is set to be an order or two of magnitude below unity, whereas the product $A\,A_a$ is chosen to be much more than unity. Moreover, similar to all switching circuits, the charge Δq stored in C_s (caused by charge injection of switch S_1 when disconnected from C_s at the end of the sampling phase) is a function of sampling frequency. Higher clock frequencies will more frequently inject charges into C_s, increasing the average Δq, and the resulting residual offset at the input.

Another technique using an auxiliary amplifier is to return the feedback loop (containing the auxiliary amplifier) to the output of the main amplifier, as depicted in figure 4-7. Moreover, since in low voltage circuits the addition of currents are less troublesome than voltages, transconductance (G_m) stages are used instead of voltage gain amplifiers, which are now terminating in a transimpedance amplifier as shown in the same figure. The addition of voltages often means stacking of the components, posing a clear issue in low-voltage design.

During the sampling phase Φ_1, when the switches disconnect the amplifier from the signal path, the output of the transimpedance amplifier R, that is, $Vout_1$, which is the same as the voltage stored in sampling capacitor C_{s1} and C_{s2} ,can be written as:

$$V_{out_1} = \left(G_m V_{os} - G_{m_a}\left(V_{out_1} - V_{os_a}\right)\right) R \tag{4.17}$$

$$V_{out_1} = \frac{\left(G_m V_{os} + G_{m_a} V_{os_a}\right) R}{1 + G_{m_a} R} \approx \frac{G_m V_{os}}{G_{m_a}} + V_{os_a} \tag{4.18}$$

where for the simplified right-hand side of the Eq. (4.18), it is assumed that $Gm_a R \gg 1$. Parameter R is the input impedance of the transimpedance amplifier in figure 4-7. During the amplification phase Φ_2, when switches S_1, S_2, S_3, and S_4 are in Φ_2 position, the voltage V_{out1} stored in C_{s1}, and C_{s2}, is applied to the output of the main transconductance amplifier Gm. The input-referred offset is derived by dividing the Eq. (4.18) by the voltage gain of the first stage ($G_m\ R$) as presented by Eq. (4.19).

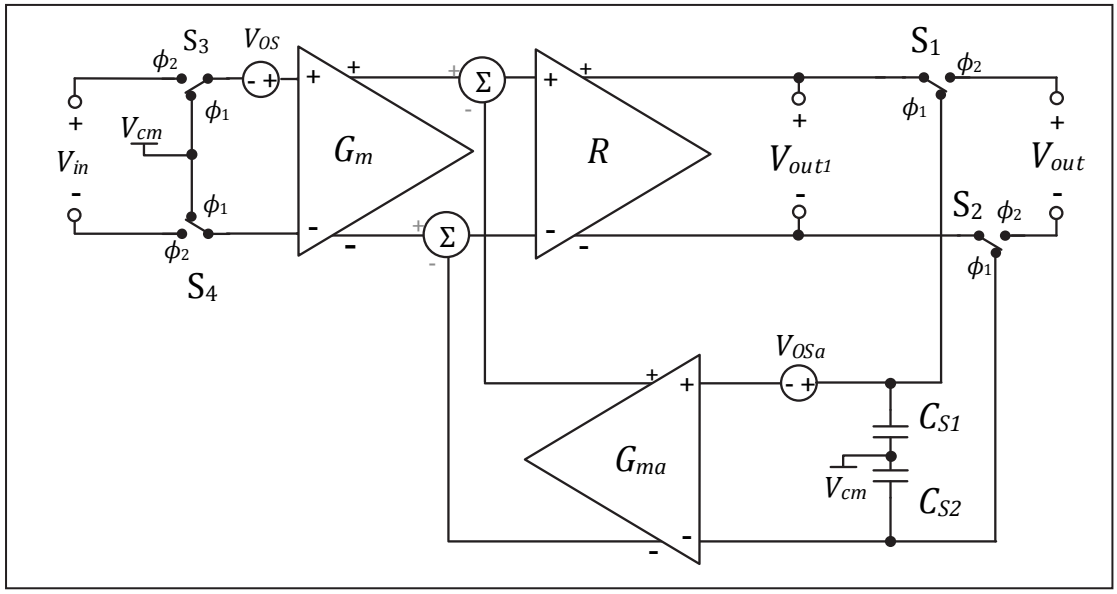

Figure 4-7 – Offset Cancellation Using an Auxiliary Amplifier at the Output of the Input Stage of the Main Amplifier

If the switches are mismatched, the charge injection of the switches S_1, S_2 will inject charges into capacitors C_{s1}, and C_{s2}, creating an error voltage which is not being suppressed by the feedback loop since the loop is open at this point. The injected charges will increase the input-referred offset by addition of a third term for the input referred offset, that is:

$$V_{os_{input_{ref}}} \approx \frac{V_{os}}{G_{m_a}R} + \frac{V_{os_a}}{G_m R} + \left(\frac{G_{m_a}}{G_m}\right)\left(\frac{\Delta q_1}{C_{s_1}} - \frac{\Delta q_2}{C_{s_2}}\right) \quad \textbf{(4.19)}$$

where Δq_1, and Δq_2 are the charge injection in capacitors C_{s_1} and C_{s_2} through switches S_1, and S_2. It is clear that in order to reduce the effect of charge injection in (4.19), G_{m_a} needs to be much smaller than G_m, at least by an order of magnitude.

4.1.3.1 Advantages and Disadvantages of Using Auxiliary Amplifiers

The main advantage of using Auxiliary Amplifiers for removing the offset and 1/f noise is avoiding the use of capacitors in the signal path.

The disadvantage compared to OOS and IOS techniques is the added component counts, which generally is understood as more complexity, extra area, and cost if the technique is repeatedly used throughout the entire design.

Another disadvantage, which arises in the case that the nulling correction signal is referred back to an intermediate stage as opposed to the very input of the main amplifier, is that the input pair is still imbalanced, therefore the common mode rejection is not improved. Normally the correction signal is applied to the output of the first sage at a summing point.

4.1.4 Ping-Pong Configuration

A general drawback in all Auto-Zeroing techniques, as previously mentioned, is the fact that the process of amplification is discontinuous in nature. During each clock cycle, time-wise, the amplifier is only partially in the signal path. At other times (sampling phase), the amplifier is no longer existed in the signal path; therefore, such amplifications are discontinuous by character. In order to overcome the issue of time-discontinuity in amplification, a topology known as Ping-Pong technique is introduced [26].

This technique is based on using two discontinuous Auto-Zeroing amplifiers in a parallel combination, such that one of the amplifiers always exists in the signal path, as shown in figure 4-8. This means when one amplifier is in sampling phase the other is in amplification phase, and vice versa. In other words, a continuous-time amplifier is created by the time-domain multiplexing of two Auto-Zeroing amplifiers [9].

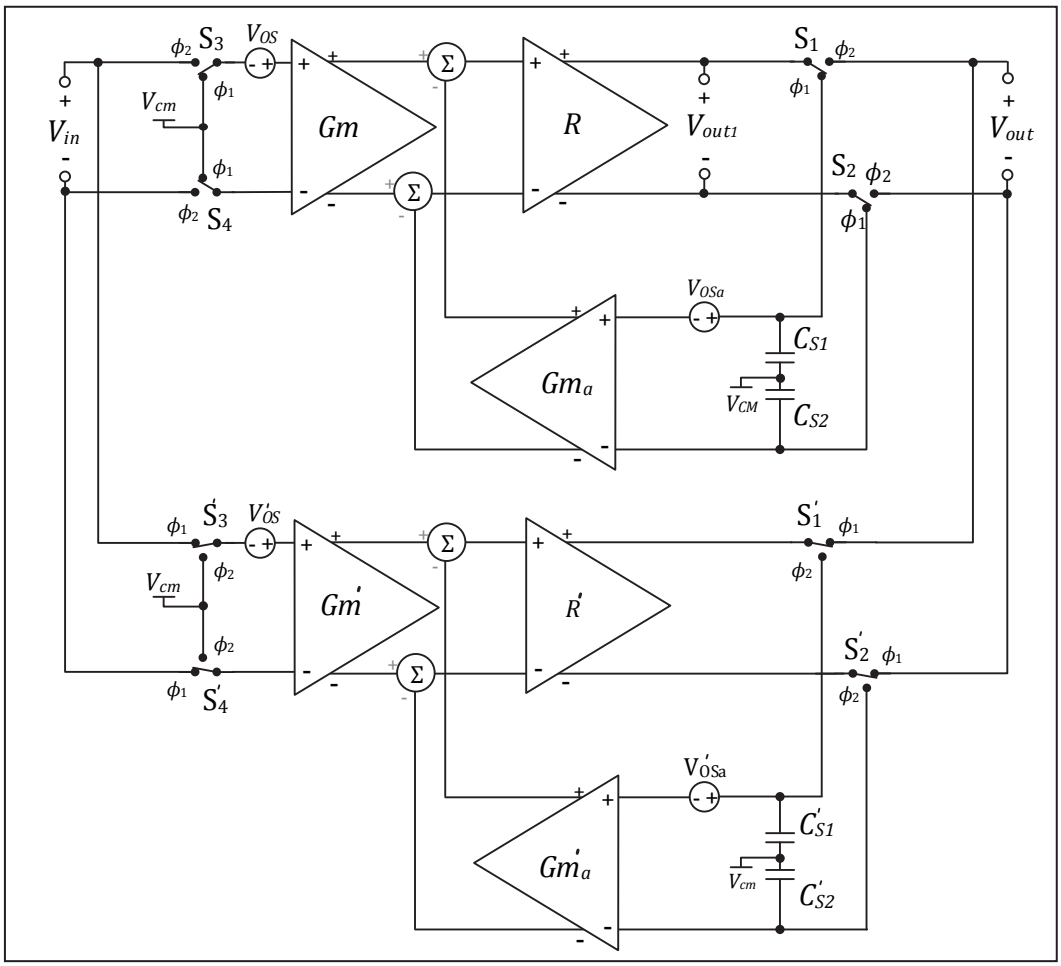

Figure 4-8 – Conceptual Ping-Ping Configuration and its Two Parallel Auto-Zeroing Amplifiers

The residual offset referred to the input, assuming a 50% duty cycle, is approximated as:

$$V_{os_{input_{ref}}} \approx \frac{\left(\frac{V_{os}}{G_{m_a}R} + \frac{V_{os_a}}{G_m R} + \left(\frac{G_{m_a}}{G_m}\right)\left(\frac{\Delta q_1}{C_{s_1}} - \frac{\Delta q_2}{C_{s_2}}\right) + \frac{V_{os}^{'}}{G_{m_a}^{'}R^{'}} + \frac{V_{os_a}^{'}}{G_{m_a}^{'}R^{'}} + \left(\frac{G_{m_a}^{'}}{G_m^{'}}\right)\left(\frac{\Delta q_1^{'}}{C_{s_1}^{'}} - \frac{\Delta q_2^{'}}{C_{s_2}^{'}}\right)\right)}{2} \quad \textbf{(4.20)}$$

where Δq_1, Δq_2, $\Delta q_1'$, $\Delta q_2'$ are the charge injection stored in sampling capacitors C_{s_1}, C_{s_2}, C_{s_1}', and C_{s_2}', through switches S_1, S_2, S_1', S_2', and V_{os}, V_{os}', G_m, and G_m' are the offsets and transconductances of the two Auto-Zeroing amplifiers G_m and G_m' respectively. R and R' are the transimpedance stages at the output of transconductance amplifiers. The latter terms here shown separately, could be the input impedances of the G_{ma} and G_{ma}' or any other impedances seen at the output of Auto-Zeroing amplifiers.

For a case when $G_m = G_m'$; $G_{ma} = G_{ma}'$; and $R = R'$, Eq. (4.20) simplifies to:

$$V_{os_{input_{ref}}} \approx \frac{V_{os} + V_{os}^{'}}{G_{m_a}R} + \frac{V_{os_a} + V_{os_a}^{'}}{G_m R} + \left(\frac{G_{m_a}}{G_m}\right)\left(\frac{\Delta q_1}{C_{s_1}} - \frac{\Delta q_2}{C_{s_2}} + \frac{\Delta q_1^{'}}{C_{s_1}^{'}} - \frac{\Delta q_2^{'}}{C_{s_2}^{'}}\right) \quad \textbf{(4.21)}$$

4.1.4.1 Advantages and Disadvantages of the Ping-Pong Configuration

A drawback of the ping-pong configuration is the added component counts compared to other similar topologies. Another disadvantage of the Ping-Pong technique is the increased spikes due to the fact that the output of transconductance/transadmittance combinations, (V_{out1} and V_{out2},) have to switch between the voltage levels of sampling capacitors required by the offset compensation loops and the voltage at the input of the output amplifier. This effect can be reduced by replacing the sampling capacitors with active integrators having the same common mode voltage as the output stage; however, spikes still remain in the circuit as the result of switching in the signal path [9].

The main advantage of Ping-Pong topology is the fact that there is no capacitor in the signal path, and a continuous-time architecture is achieved, even though the circuit is based on sampling technique which is discontinuous in nature.

4.1.5 Self-Calibration or Digital Offset Storage and Control Technique

Another technique to remove the offset error is self-calibration, or the use of data converters in a closed-loop configuration as depicted in figure 4-9. This technique is also called Digital Offset Storage and Control [22], or for short Digital Trimming in the literatures [16] , [17].
During the sampling phase Φ_1, Switches S_1 and S_2 short the inputs of the amplifier, where the offset is sampled, converted to a digital word by the analog to digital converter (A/D), and stored into the registers preceding the digital to analog (D/A) converter.

During the amplification phase Φ_2, the offset is placed at the nulling input of the amplifier through D/A, cancelling the offset to the first degree of approximation.

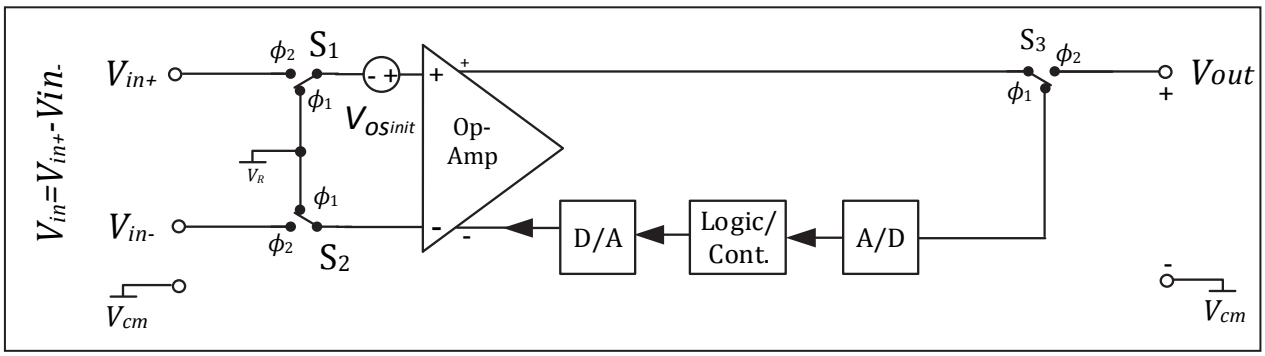

Figure 4-9 – Data Converters in a Feedback Loop with Digital Control.

It can be shown that the residual offset referred to the input is inversely proportional to 2^N, where N is resolution of the converter, and can be approximated as:

$$V_{os_{resi}} = \frac{V_{os_{init}}}{2^N} \qquad \textbf{(4.22)}$$

where $V_{os_{resi}}$ is the input-referred offset, and $V_{os_{init}}$ is the initial offset before calibration.
Differential amplifiers with DC open loop gain of 95dB and residual offset of less than 30μV have been reported using this technique [24].

4.1.5.1 Advantages and Disadvantages of Self-Calibration

The advantage of the self-calibration method is similar to all other configurations having no capacitors in the signal path. In this case, storing of the sampled offset is through digital words in registers as opposed to the analog method of storing a charge in a capacitor.
Another advantage of the technique is that doesn't limit the bandwidth [17].

A disadvantage of this technique is the need for data converters whose accuracy specifications determine the residual offset of the amplifier.

Also since the input stage is still intact because the offset cancellation is performed somewhere between the input and output at an auxiliary input, the differential stage (the main input of the amplifier) is still imbalanced and the common-mode rejection is not improved.

4.1.6 Auto Calibration (Digital Signal Processing Approach)

Another technique to achieve a low residual offset in signal amplification is the use of a microcontroller to digitally process and compute the offset, gain, and input at any given time, synchronized with the sampling clock as shown in figure 4-10. The general approach on such system level approaches are extensively discussed in chapter 2 of reference [16].This approach is also called "The 3 Signal Method" [16 **],** [17].

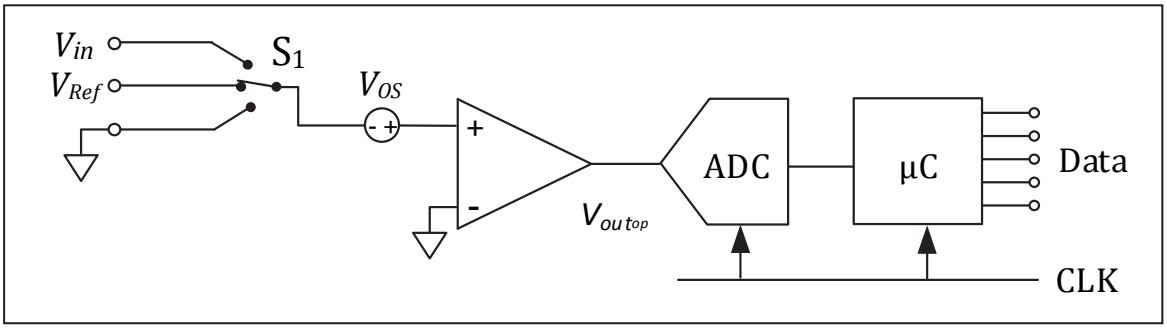

Figure 4-10 – Digital Signal Processing Approach on Sampled Offset and Input Voltages

As can be seen, the Sampling is performed in three distinct phases:

Phase Φ_1: The output of the amplifier produces a voltage equal to:

$$V_{out_{op}} = A(V_{os} + V_{in}) \quad \textbf{(4.23)}$$

Phase Φ_2: The output of the amplifier is given by:

$$V_{out_{op}} = A\left(V_{os} + V_{Ref}\right) \quad \textbf{(4.24)}$$

Phase Φ_3: The output of the amplifier is only a gained version of the offset alone.

$$V_{out_{op}} = AV_{os} \quad \textbf{(4.25)}$$

V_{Ref} is a known Reference Voltage, V_{in}, and the gain (A) can be calculated by the microcontroller, in addition to any likely mathematical operation and storage needed to be performed on these parameters. This approach is easy to implement when a µC is available [16], and [17].

The input-referred residual offset is determined by the resolution of the A/D converter N, and is given by:

$$V_{os_{resi}} = \frac{V_{os_{init}}}{2^N} \quad \textbf{(4.26)}$$

4.1.6.1 Advantages and Disadvantages of the Digital Signal Processing Approach

An advantage of using this technique is the lack of capacitors in the signal path.
In addition to offset, flicker noise is also reduced. However, the reduction of the latter is only for frequencies below the operating frequency of the switch S_1 in figure 4-10.

Also the technique gives the ability of handling any mathematical operations on the amplified signal within the digital domain, as well as storing the results in a memory, which often is needed in a mixed-mode applications and designs.

On the other hand, the circuit is more complicated and costly if the μC is not available. However, more often than not, in many of today's end-user applications, the μC itself, and many of its house-keeping or peripheral blocks such as ADCs, timers, DACs, and registers, already exist in the system so the implementation is quite easy in such cases.

5. Dynamic Offset Cancellation Techniques: Chopping, A Modulation Based Approach

Chopping is a continuous time modulation technique using two Synchronized Polarity-Swapping Switches called Choppers at the input and output of an amplifier to provide offset and 1/f noise cancellations. The Technique will be discussed throughout this chapter. A high level block diagram of a chopper amplifier without the required filtering block is shown in figure 5-1

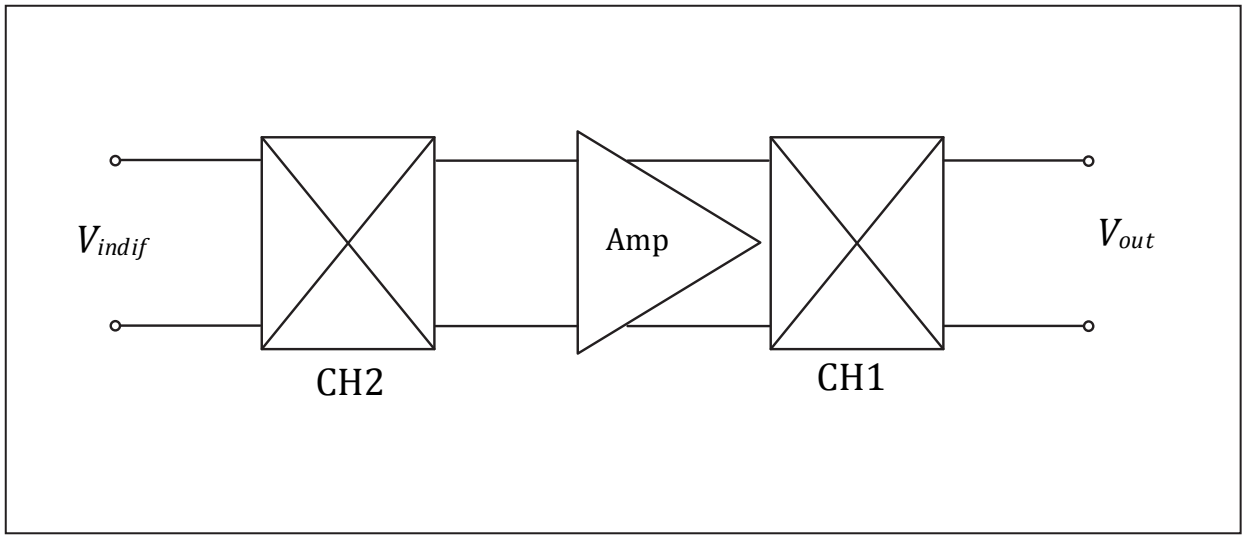

Figure 5-1 – A High Level Block Diagram of a General Chopper Amplifier

Each polarity-swapping switch as a whole can be thought as two Single-Pole Double-Through (SPDT) switches. The outputs of the switches (the Double-Through terminals) are connected in parallel in a cross-coupled way. This is such that a signal passing through the two poles at one end can either pass through straight, or crossed (swapped) at the other end. These polarity-swapping switches (choppers) are generally composed of four small MOS-FET devices controlled by a pair of complementary clock signals driving their gates as shown in figure 5-2.

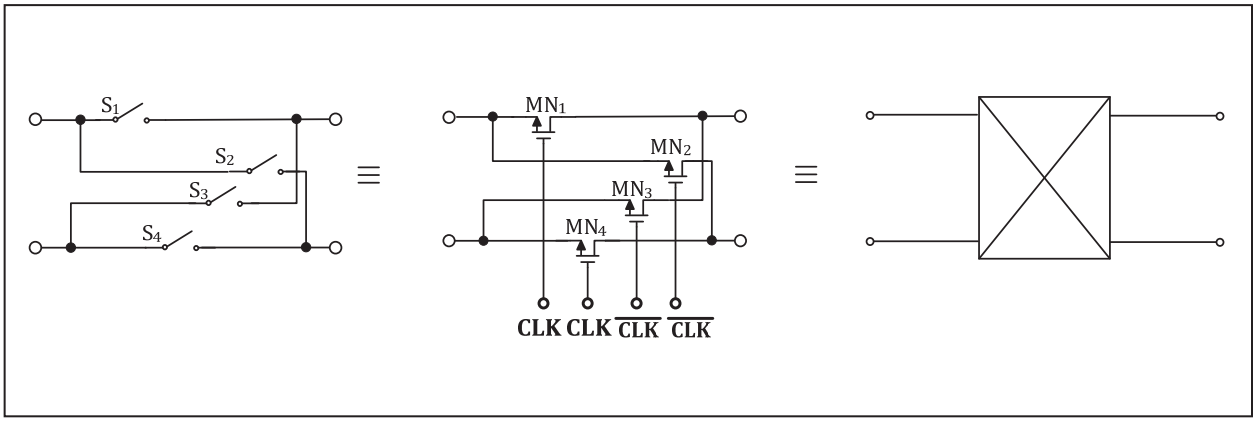

Figure 5-2 – Chopper Schematic, NMOS Implementation, and General Symbol

The clock frequency at which the two complementary clocks are driving the MOS switches is called the chopping frequency.

5.1 Basic Chopper Operation

As mentioned chopping is a modulation technique. But in order to eventually separate the signal from the offset and low frequency noise, we need to modulate the signal of interest differently from the offset and low frequency (flicker) noise.

Referring to figure 5-4, the band-limited signal $V_{in}(t)$ with the bandwidth BW passes through the input chopper CH_2 which acts as a modulator multiplying the input signal by a 50% duty cycle rectangular signal m(t), with the amplitude of unity as shown in figure 5-3.

Due to this modulation process, signal is modulated at odd harmonics of the chopping frequency right after the chopper CH_2 as shown in figure 5-4. Now the offset and low frequency noise of the amplifier A is added to the chopped signal, and the summation is amplified.

The modulated signal is then demodulated at the output of the amplifier by the output chopper CH_1 at odd harmonics of the clock frequency. However the flicker noise and offset are modulated just once by this same output chopper at odd harmonics of the chopping frequency.

The amplitude of the modulation signal is inversely proportional to the harmonic number.

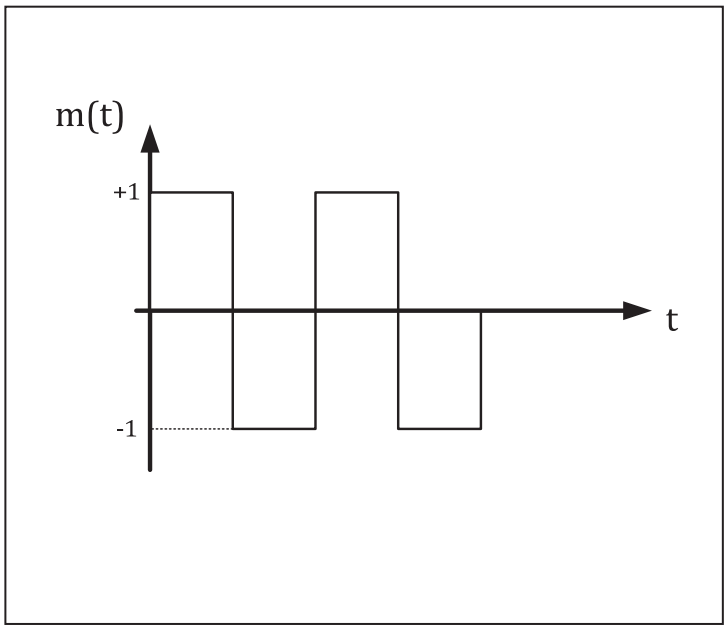

Figure 5-3 – Modulation or Chopper Signal

If f_{ch} is the chopping frequency, and the f_{cor}represents the flicker-noise corner frequency, then a low-pass filter with a cut-off frequency slightly more than the BW of the signal, but less than "$f_{ch} - f_{cor}$" at the output of the amplifier will remove the unwanted higher harmonics caused by the modulation act of the choppers. This will reconstruct the original signal without the offset and flicker noise presence [28].

Obviously the necessary condition to significantly reduce the flicker noise in the baseband is that the chopping frequency be chosen according to Eq. (5.1) as is clear from figure 5-5.

$$f_{ch} \geq BW_{signal} + f_{cor} \qquad \textbf{(5.1)}$$

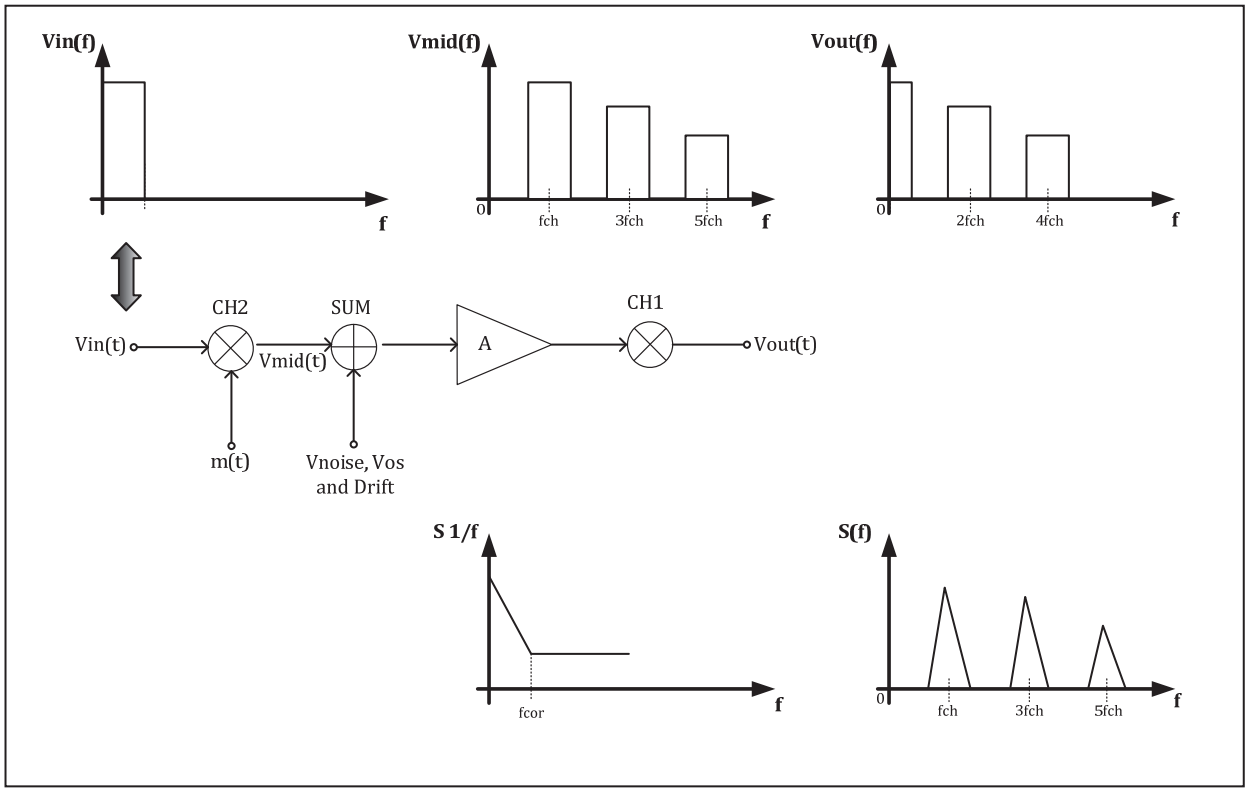

Figure 5-4 – Frequency Domain Representation of the Signal and Flicker Noise in a Chopper Amplifier

The chopped offset has also no component at DC level; therefore it is filtered out after the low-pass filter. The low-pass filter is often at the output as shown in figure 5-6.

It should be noted that the effective gain of the amplifier is actually the gain at the chopping frequency "f_{ch}" as opposed to the DC gain of the amplifier. This gain $A(f_{ch})$ should not be lower than the DC gain *A(0)* of the amplifier, hence the use of a broadband amplifier ($BW_{(A2)} > 5\ f_{ch}$), or multistage amplifiers are justified. Also the phase should not be delayed by more than few degrees, otherwise the input and output choppers are not synchronized any more in regards to the

signal. After the second chopper CH_1, the signal is demodulated at the baseband. The total DC gain of the two-stage amplifier is therefore the gain of the first stage at the chopping frequency times the DC gain of the output stage.

$$A_{tot} = A_2(f_{ch})\ A_1(0) \quad \textbf{(5.2)}$$

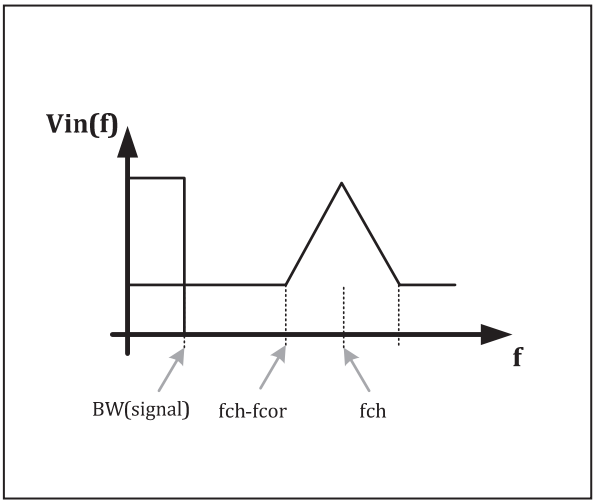

Figure 5-5 – The Baseband Spectrum Shows that the Chopper Frequency Must be Bigger than the Summation of the Signal BW and Flicker Noise Corner Frequency.

Chopping generally does not introduce extra noise [30]. The main noise source associated with the chopping operation can then be considered as on-resistance of the chopper itself. Here, lowering the resistance of the input chopper (CH_2) will improve the noise performance of the amplifier. The output chopper (CH_1) is in series with the high impedance output of the transconductance amplifier A_2, therefore its on-resistance will not matter much.

5.2 Chopper Techniques

As mentioned before, there are several Chopper Techniques, both classical, and new, each with their own architectures, figures of merit, and shortcomings.

For Obvious reasons, the classical approaches are not dealt with in details in this thesis. However a brief view is presented for the sake of continuity, as well as an appreciation for the new approach. The approach is called "Chopper-Stabilized Auto-Zeroed Chopper Technique", which is the work of this thesis.

The technique is equally applicable to Op-Amps, or Inst-Amps of other architectures besides CFIA. The latter has been the architecture of the choice here, which has first been presented in Section 1.3.

Below is a list of some of these methods, which cover both classical, as well as the more modern approaches.

1. Conventional Chopper Techniques
2. Nested Chopper Techniques
3. Chopper Techniques with Auto-Zeroing
4. Chopper-Stabilized Techniques
5. Chopper-Stabilized Chopper Techniques
6. Chopper Stabilized Auto-Zeroed Chopper Techniques

5.2.1 Conventional Chopper Techniques

Figure 5-6 shows one of the oldest techniques used in both chopper Op-Amps, and chopper Inst-Amps. In a conventional chopper amplifier, the modulator and demodulator (basically switches) are placed at the input and output of the amplifier. The associated waveforms are shown in figure 5-7 [15], [17], & [18].

The implementation is not different from the general case presented in figure 5-1 except here a two-stage amplifier is shown along with its low-pass filter at the output. Some important parasitic capacitors affecting the performance of the chopper amplifier, often unavoidable but manageable, are also shown in the picture. The discussion on the effects of such parasitic elements is left for discussion of the new architecture in section 5.4. Throughout the section we reveal some adverse effects of such parasitics in more details with few simple mathematical formulas. Note that the choppers are placed in the main path (signal path) of the amplifier.

As mentioned earlier, this conventional technique can potentially reduce the offset by a factor of 100 to 1000 times in many implementations. As such, an Op-Amp or Inst-Amp with an initial six sigma offset of 10mV, will have a *DC* offset in the order of 100 µV to 10µV at its input [18].

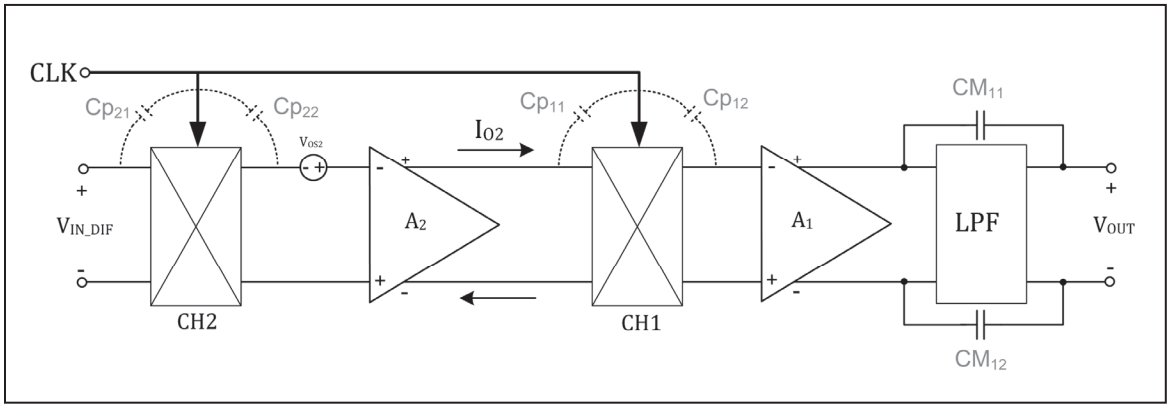

Figure 5-6 – Conventional Chopper Inst-Amp and its Main Parasitic Capacitances

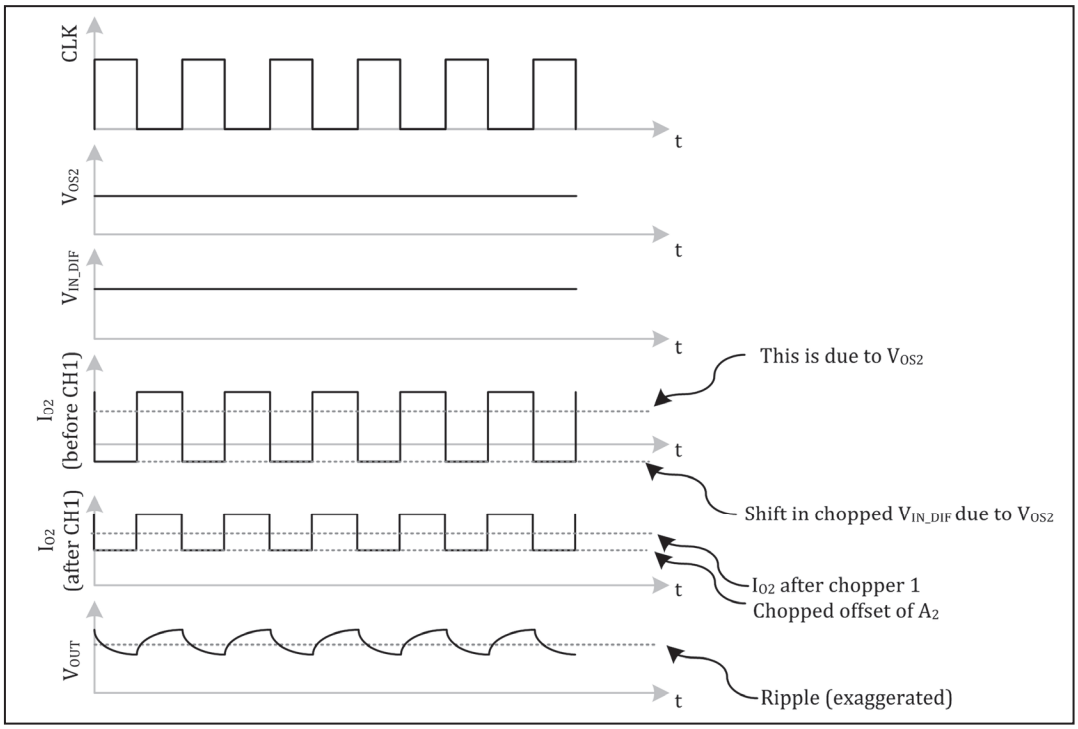

Figure 5-7 – Typical Waveforms of the Signal and Error at the Output and Input of a Chopper Inst-Amp. May modify a little.

5.2.1.1 Challenges with Conventional Chopper Techniques

The technique suffers from several limitations as listed below:

1) Unless removed by a low pass filter at the output of the chopper Inst-Amp, (or chopper Op-Amp), a square wave at clock frequency of the size of the original input offset will be superimposed on the average input signal. Use of the required filter often will significantly reduce the bandwidth of the amplifier to well below the chopping frequency.

   An amplifier with a chopper frequency of 30kHz, will likely suffer from a limited BW of few kHz, due to the filtering requirements, as well as flicker noise corner frequency limitations as shown in Eq. (5.1). This can be a severe BW limitation in applications requiring a fast settling at the output of the amplifier.

2) Integrating the above filter with the chip itself is impractical due to the huge area (cost) considerations.

3) The rather large initial offset will not be fully averaged out due to the parasitic capacitances at the input of the first chopper, in conjunction with the existing of the signal source resistances. The lower this initial offset, the lower the associated error. Reducing this error requires lowering the original offset by expensive trimming, or Auto-Zeroing as we have discussed before. This offset reduction can be performed in an elegant way by the new approach, as will be seen later.

4) Any deviation from a perfect 50% duty-cycle for the chopper clock due to imperfections in the circuit will cause the square wave offset not to be averaged out to zero, but rather to some residual offset. The lower the original offset, the lower the amplitude of the square wave, and hence the lower the average of the square signal or its residual offset.

5) There are charge injections, and clock skew errors which are common to many types of such switching circuits (continuous or discontinuous). A 10mV native offset with a clock skew of 0.01% will result in a 1μV residual offset at the input just by itself, regardless of other sources of offset errors.

5.2.2 Nested Chopper Techniques

The Nested Chopper Technique primarily addresses some of the issues with conventional choppers related to the effects of parasitics and non-idealities of real-world components and signaling. Both clock skew and charge injections, together with imbalances of the parasitic capacitances within the choppers (mainly the parasitic gate capacitances of MOSFET transistors in figure 5-6) will potentially create residual offset errors [31]. Generally these parasitic capacitors which are connected at the gates of the switches within the choppers at one side, and to the drains and sources (signal paths) on the other side, constitute simple RC differentiators considering the impedance of the signal paths to ground.

The square-wave clock signals driving the gates create alternating spikes on the signal path due to the action of these differentiators. The alternating spikes will average out to zero, assuming the positive going spikes cancel the negative going ones, but this is not true for all parasitics due to the rectification action of the choppers on the alternating current spikes.

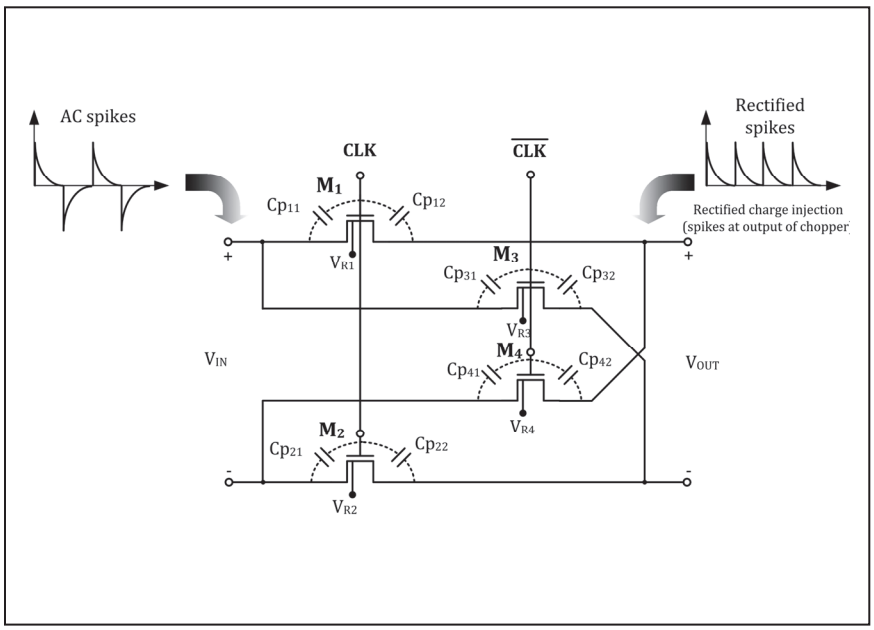

Figure 5-8 – Charge Injection Spikes Through Certain Parasitic Capacitances within a Chopper, Create a Residual Offset at Chopper's Output due to its Rectification Act.

As an example, consider the Chopper CH1in figure 5-6. The effects of charge injection due to the parasitic capacitors C_{p11}, and C_{p12} (for switch M_1 only) are shown in figure 5-8. Any square-wave clock signal at the gate of the transistor M_1, will create an alternating current spike at the output of the chopper CH_2, due to the charge injection through C_{p12}. However a rectified spike current will be created at the output of this chopper due the presence of an alternating current spike through parasitic capacitor C_{p12}, and the rectification action of the chopper CH_1 itself.

These rectified spikes are averaged out to an offset voltage. If one is careful with the layout of the choppers, using shielded clock and signal lines, along with choppers closely resembling a fully balanced ideal chopper (that is the effects of all parasitics are the same, and more importantly minimal), then practical nominal offset values around 1μV or less [31] can be achieved. It is clear that the higher the clock frequency is selected, the bigger this residual offset turns out to be. A good estimation for the residual offset created by such spikes are shown in several references listed at the end of this thesis [22], [23], [28], [32].

$$V_{os_{resi}} = \frac{V_{spike}}{0.5\,T} \int_0^{0.5T} e^{-t/\tau}\ dt \qquad \textbf{(5.3)}$$

Where $V_{os_{resi}}$ is the residual offset due to charge injection induced spikes, V_{spike} is the magnitude of the spike, T is the period of the chopping frequency, and τ is the RC time-constant associated with the signal source impedance and the parasitic gate-overlap capacitances. If the clock period is much longer than this time constant; that is T >> τ; then (5.3) reduces to:

$$V_{os_{resi}} = \frac{2\,\tau}{T} V_{spike} \qquad \textbf{(5.4)}$$

From equations (5.3), and (5.4) it is clear that reducing the chopping frequency will reduce the spikes-induced residual offset. On the other hand, Table 5-2 suggests that often it is desirable to increase the chopping frequency in order to reduce the input-referred offsets and flicker noise caused by the native offset errors associated with the chopper amplifier itself. Besides, Eq. (5.1) puts a constraint on the lower limit of the chopping frequency dictated by the flicker noise corner frequency and the signal bandwidth. For a specific signal bandwidth, the only way to achieve a lower chopping frequency is to reduce the flicker noise corner frequency; that is bearing the cost of larger input transistors. So it is clear that we have contradictory constraints in choosing the chopping frequency.

Moreover the above equations indicate that for a certain spike magnitude, the only other variable affecting the residual offset besides the chopping frequency, is the time-constant which is not considered a design variable to manipulate. This time-constant depends on the process technology (gate capacitances) and the impedance of the signal source, none of which are under the control of the designer.

A simple solution to overcome these conflicting constraints is to replace each chopper in figure 5-6 with a pair of choppers operating at different frequencies as shown in figure 5-9.
The chopping frequency of the outer choppers CL_2 and CL_1 is not restricted by the flicker noise corner frequency, and can be chosen as low as possible, usually twice the signal bandwidth [32].

Due to the linear-direct relationship of the spike-originated residual offset and chopping frequency as seen in Eq. (5.4), the effects of such spikes are now significantly reduced by selecting a much lower frequency ($f_{ch_{low}}$) to drive the outer choppers. On the other hand, the inner choppers are driven by a chopping frequency ($f_{ch_{high}}$) which obeys the Eq. (5.1); that is this chopping frequency is dependent on signal bandwidth and flicker noise corner frequency.

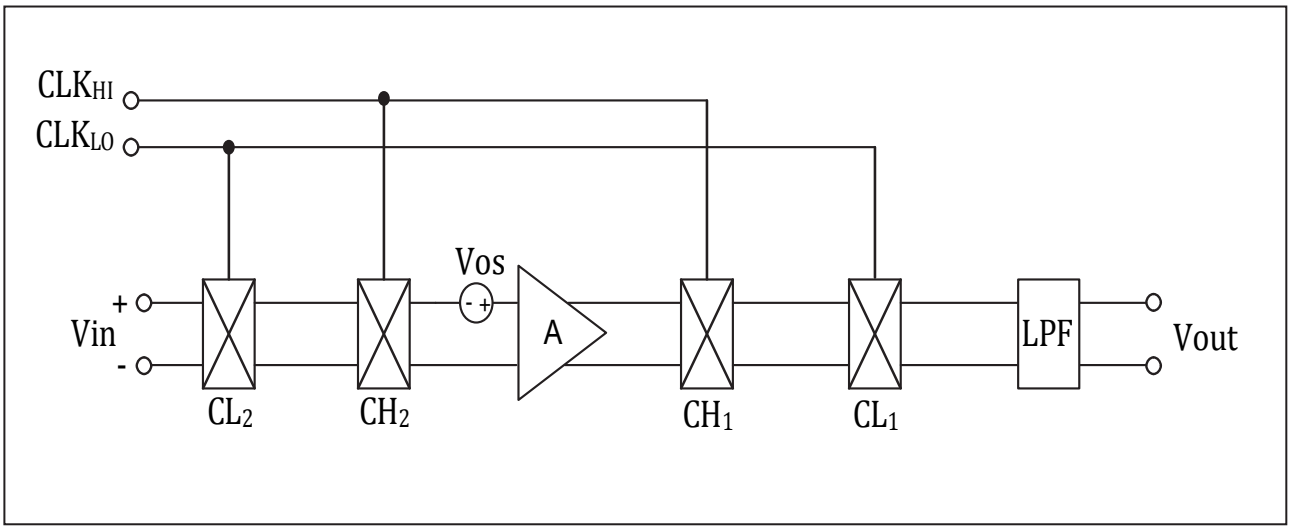

Figure 5-9 – Nested Chopper Amplifier with its Inner and Outer Choppers Operating at Two Different Frequencies.

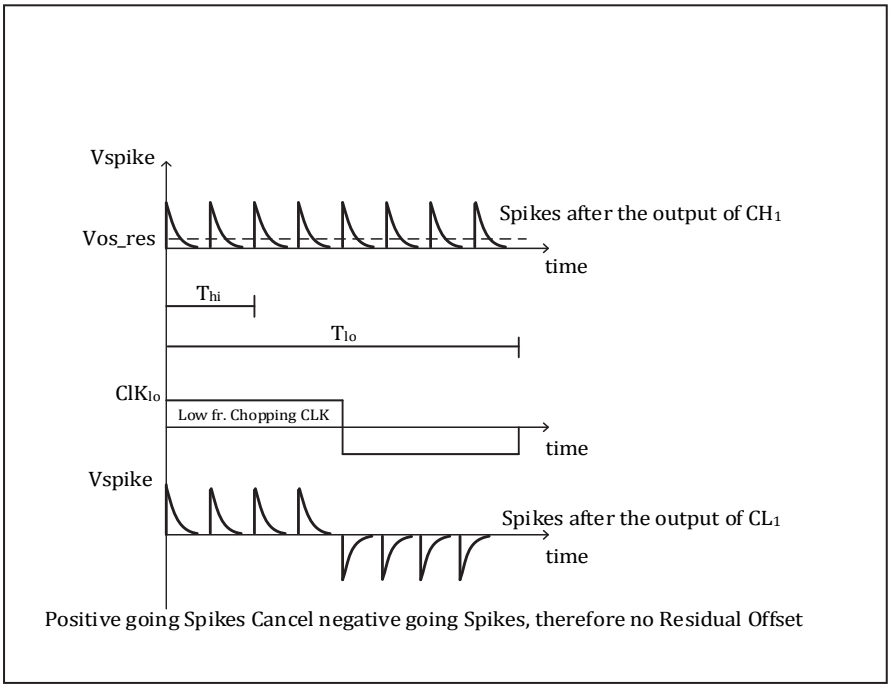

Figure 5-10 – Using Nested Chopper Technique for Reduction of Charge Injection Residual Offset.

The inner choppers are there to remove the ripple and flicker noise as usual. They are clocked at a frequency much higher than the outer choppers who are used just to overcome the charge injection originated spikes and their resultant residual offset.

The low frequency choppers convert back to the alternating format, those rectified spikes generated by the inner chopper's charge injection and rectification action as shown in figure 5-10 c. This practically makes the average of the above spikes equal to zero, therefore solving the charge injection issue. The charge injections through the gate overlap capacitances of low frequency choppers are negligible due to the lower frequency of such choppers.

Theoretically, the improvement factor(K_{impv}) in suppressing the charge injection initiated residual offset through the nested chopper approach is the ratio of the high and low chopping frequencies.

$$K_{impv} = \frac{f_{ch_{high}}}{f_{ch_{low}}} \geq \frac{BW_{signal} + f_{cor}}{2\,BW_{signal}} \qquad \textbf{(5.5)}$$

For DC and very low frequency applications, more than an order of magnitude of improvement in reducing charge injection initiated residual offset over conventional chopper approaches is possible using nested chopper techniques.

As an example of setting chopper clock frequencies, in a temperature sensor with a 10Hz bandwidth, the low frequency chopper clock is set to twice this bandwidth; i.e. 20 Hz. If the high frequency chopper clock is set to 2 kHz based on the flicker noise requirements, then a factor of 100 times improvement is achieved by this nested chopper technique [32].

5.2.2.1 Application Challenges with Nested Chopper Techniques

A challenge with the nested chopper technique that is most relevant in practice is the requirement for balanced source impedances at both input terminals of the amplifier. This generally is not guaranteed and as such there would be unequal positive and negative spikes, which in turn results in a residual offset for the nested chopper technique. This source impedance imbalance issue is a problem with chopper techniques in general.

5.2.3 Chopper Techniques with Auto-Zeroing

Auto-Zeroing Techniques can be used along with Chopper Techniques to achieve a better performance in reduction of both residual offset and the flicker noise.

One common topology here is to combine an Auto-Zeroed amplifier in a ping-pong configuration with a chopper amplifier [31], as shown in figure 5-11.

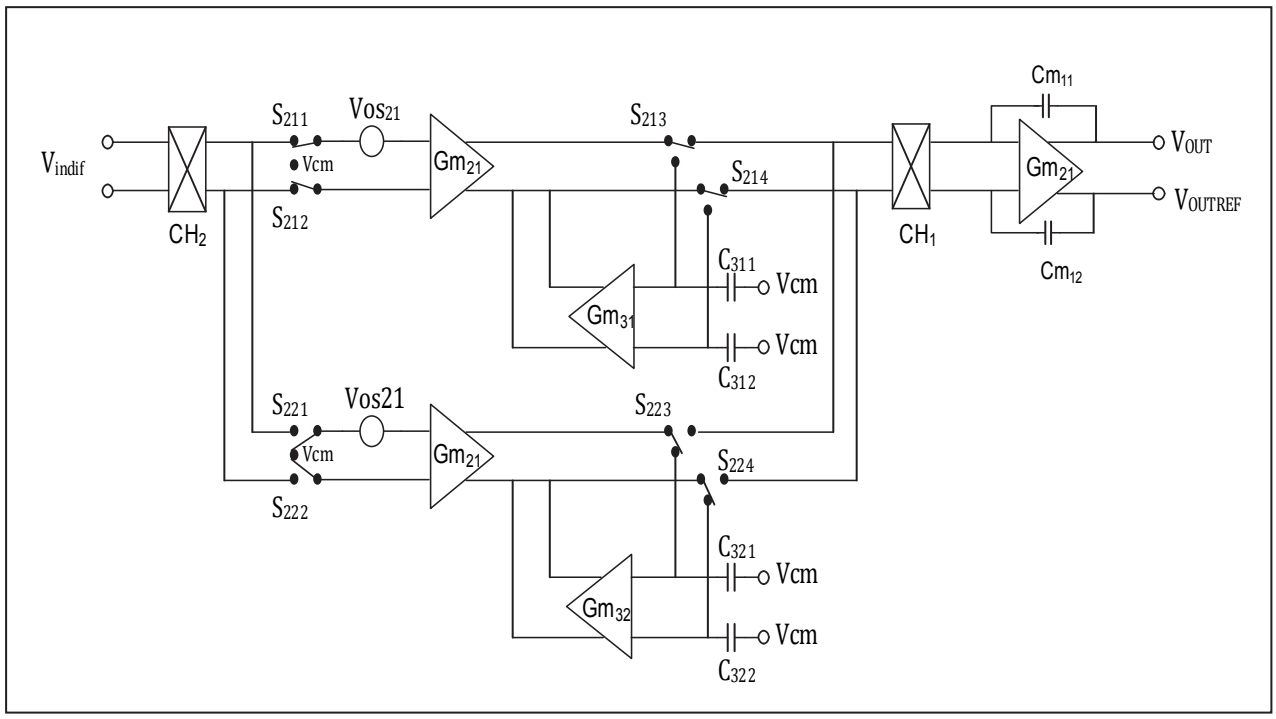

Figure 5-11 – Chopper Amplifier with an Auto-Zeroed Ping-Pong Configuration.

Input and output choppers CH_2 and CH_1 simultaneously embrace just one of the two main transconductances Gm_{21} or Gm_{22}, along with their Auto-Zero correction transconductance Gm_{31} or Gm_{32} and their storage capacitors C_{311} and C_{312}, or C_{321} and C_{322}; through a set of synchronized switches, in a known ping-pong configuration as shown if figure 5-11.

Through each successive clock cycles, only of the two sets of (Gm_{21}, $Gm_{31,}$ C_{311}, C_{312}) or (Gm_{22}, $Gm_{32,}$ C_{312}, C_{312}) is in the signal transfer mode by the act of the switches shown in the figure. At the same time the other set is in Auto-Zeroing mode, ready to be connected to the input and output choppers in the subsequent clock cycle in the familiar ping-pong configuration described in section 4.1.4.

The choppers are acting one at the time on one of the two main transconductances Gm_{21} or Gm_{22} in alternative clock cycles. The chopper clock frequency (f_{ch}) is twice the Auto-Zeroing frequency (f_{AZ}). The chopping act will transfer the Auto-Zeroed residual offset and low

frequency noise of Gm_{21}or Gm_{31} to the odd harmonics of chopper frequency as opposed to transferring the native offset and flicker noise of Gm_{21}or Gm_{31} themselves.

Such amplifiers can achieve an offset of 2μV and an input referred ripple of around 10μV.
An advantage of the ping-pong continuous-time topology is the simplicity of the frequency compensation, which is based on one set of Miller-Compensation capacitors [31].
Chopper techniques with Auto-Zeroing could still need low-pass filtering to remove the residual offset modulated at chopping frequency; however the requirement of the filter is somewhat relaxed compared to conventional chopper techniques with no Auto-Zeroing.

5.2.4 Chopper-Stabilized Techniques

The chopper-stabilized technique is introduced to lower the output ripple of a conventional chopper amplifier. The technique is considered one of the most effective as it tries to reduce the native offset and low frequency noise prior to modulation by the output chopper.

Compared to conventional choppers, in a chopper-stabilized amplifier, the choppers are moved from the main signal path to an auxiliary path as shown in figure 5-12; [15] & [31].

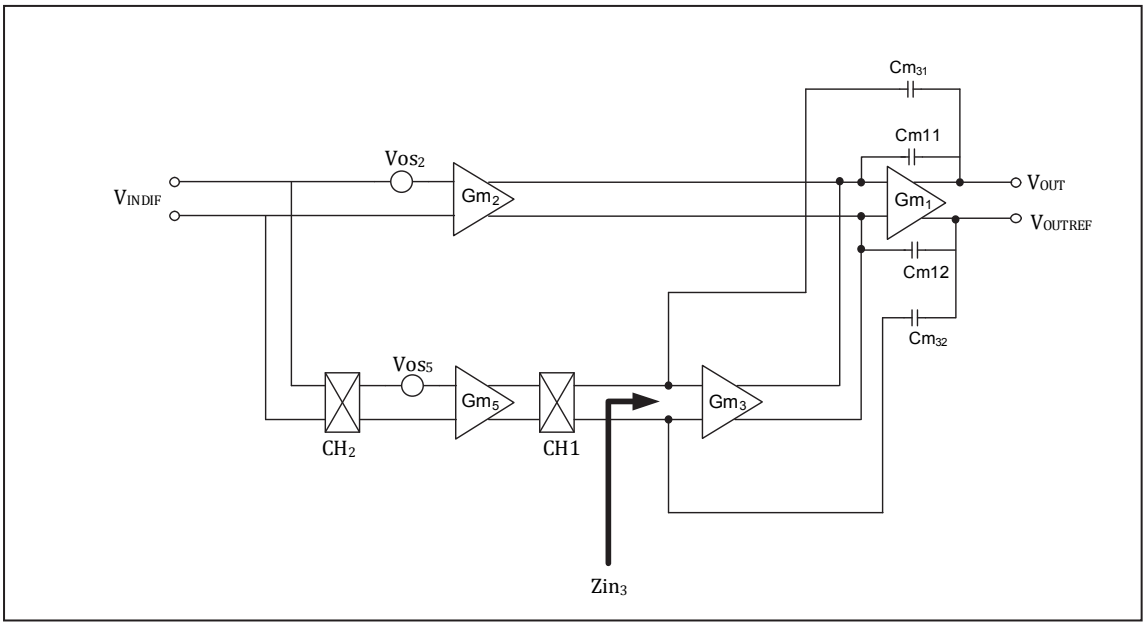

Figure 5-12 – Chopper-Stabilized Amplifier with Multipath Nested Miller Compensation.

Referring to figure 5-12, the main path of amplification is composed of Transconductance Gm_1 as the output stage, and Gm_2 as the input stage or high frequency path.

The output stage Gm_1 is differentially Miller compensated, and the low frequency path of CH_2, Gm_5, CH_1, and Gm_3 which are there to remove the offset of Gm_2 is using the nested Miller compensation scheme.

The offset of Gm_2, $V_{os2,}$ is chopped by chopper CH_2 to appear as a square-wave ripple with a peak to peak value of twice V_{os2} at the input of Gm_5. The transconductance Gm5 performs a voltage-to-current conversion and delivers a square-wave current of the value (V_{os2} Gm_5) to chopper CH_1, which rectifies this alternating current back to a DC current via the action of CH_1, and finally to a DC voltage by passing through a total impedance Z_{in3} seen at the input of Gm_3.

Transconductance Gm_3 converts this V_{os2} originated DC voltage back to a DC current right at the common output of Gm_2 / Gm_3, with such a polarity that it cancels out the V_{os2} originated offset current by the Gm_2 itself. This will be the case if the following equality holds true.

$$Gm_5\, Gm_3\, Z_{in3} = \; Gm_2 \qquad \textbf{(5.6)}$$

In the above analysis, the offset of Gm_5 itself, that is $V_{os5,}$ is considered not to have any major role as it is converted to a square current offset by the action of Gm_5 and CH_1, and eventually gets filtered out by integrator Gm_4, and also the Miller capacitors CM_{11} & CM_{12}.

The amplifier now has two gain paths. The first is the high frequency low gain path of Gm_2, and the second is the low frequency high-gain path consisting of Gm_5 and Gm_3. The offset can only be reduced as long as the high-gain path has a higher gain than the low-gain path [15] & [31].

5.2.4.1 Challenges with Chopper-Stabilized Technique and Ways to improve the Design

The technique as described in section 5.2.4; and by figure 5-12 has few disadvantages.
First, the gain of Gm_3 is generally low (around 20% of the gain of the main input transconductance Gm_2) due to the need for correction of the offset Gm_5 without adding too much noise to the summing point. This means that the offset is not significantly reduced.

Another issue is that the integration action of the Miller / nested Miller capacitances may not be effective enough in filtering the ripple associated with alternative current offset of Gm_5.

For this reason, it is preferred to have an extra integrator block in the low frequency path, right after the output chopper CH_1 in figure 5-12. In so doing, we now have a chopper-stabilized amplifier with multipath hybrid-nested Miller compensation as shown in figure 5-13.

This improvement has been presented in this thesis by the integrator block Gm_4 shown in figure 5-13 and figure 5-14 of this section, as well as figure 5-15 of section 5.4. The same improvement is repeated throughout the work of this thesis when dealing with multiple correction loops within the design of Chopper-Stabilized Chopper Inst-Amp using Indirect Current Feedback Instrumentation Amplifiers (ICFIA or CFIA), as presented in this chapter and the next.

With this addition, the square-wave ripple of Gm_5 is suppressed even more due to the action of the integrator Gm_4. Also the integrator capacitors can freely be selected for the needed filter's time-constant. Furthermore, the weak transconductance Gm_3 reduces the ripple at the output of Gm_4 even more, and eventually supplies a DC current proportional to the offset of Gm_2 in such a polarity that cancels out the offset current at the output of Gm_2 initiated by its own offset.

One of the known issues with the frequency compensation schemes of chopper-stabilized topologies is the non-straight 20dB / decade roll-off of such amplifiers. The remedy for this is to follow the rules of hybrid nesting by adding two extra capacitors from the output to the input of Gm_4, and make sure that the time-constants of the low and high frequency paths are made equal as has been described for the work of this thesis in section 5.4.10 and figure 5-21 [13].

5.2.5 Chopper-Stabilized Chopper Techniques

This is a continuous time technique with choppers in both the main and the auxiliary path of the amplifier as shown in figure 5-14 . The chopper amplifiers modulate the offset and low frequency noise over the chopping frequency and away from the baseband; however the native offset of the input stage (6 sigma in production) could be as high 10mV ~ 20mV depending on the process technology. Generally the higher this initial offset, the more stringent the characteristic of the low-pass filtering at the output of the conventional chopper amplifier is required to be.

If the conventional chopper is chopper-stabilized, the initial offset will be significantly suppressed, which is highly desirable. The first stage of the amplifier; that is Gm2 shown in either figure 5-13 (chopper-stabilized) or figure 5-14 (chopper-stabilized-chopper) amplifier determines the input referred noise at low and high frequencies. However the chopper-stabilization loop determines the noise and ripple at the clock frequency [31].

This technique by itself, especially when combined with Auto-Zeroing, as will briefly be mentioned in the section 5.2.6, are the subject of the work of this thesis. The system level description of the technique, and the block level analysis is described in details throughout section 5.4 and thereafter.

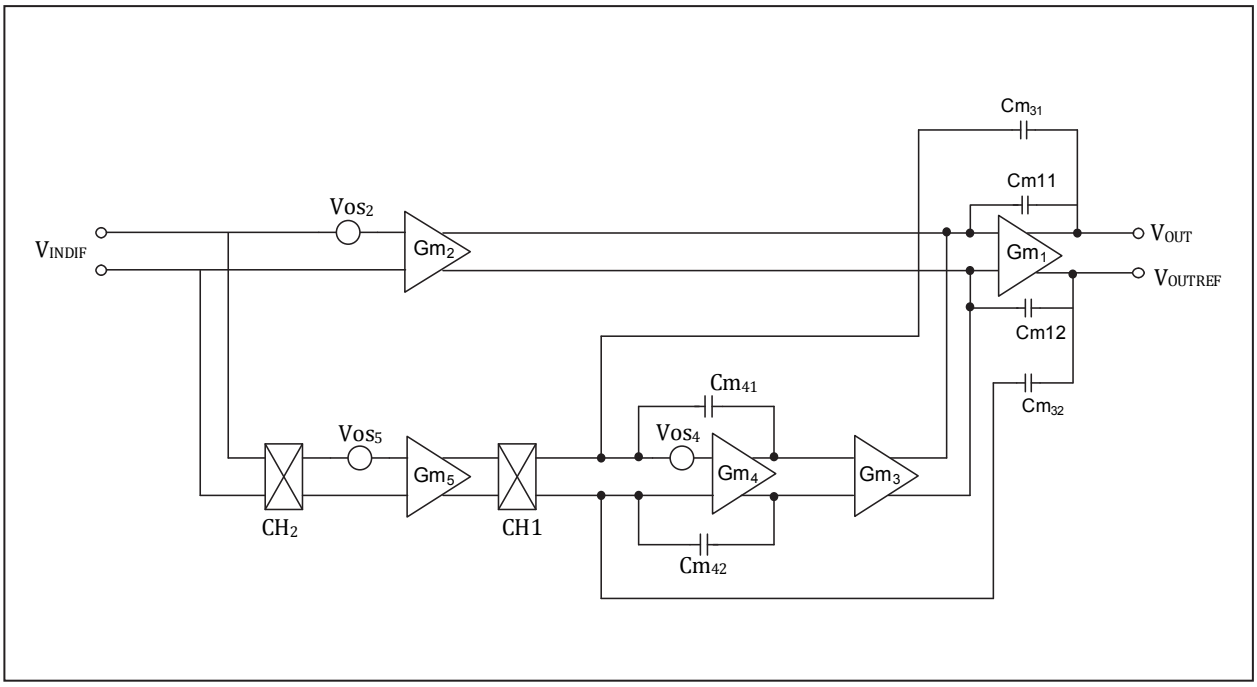

Figure 5-13 – Chopper-Stabilized Amplifier with Multipath Hybrid-Nested Miller Compensation.

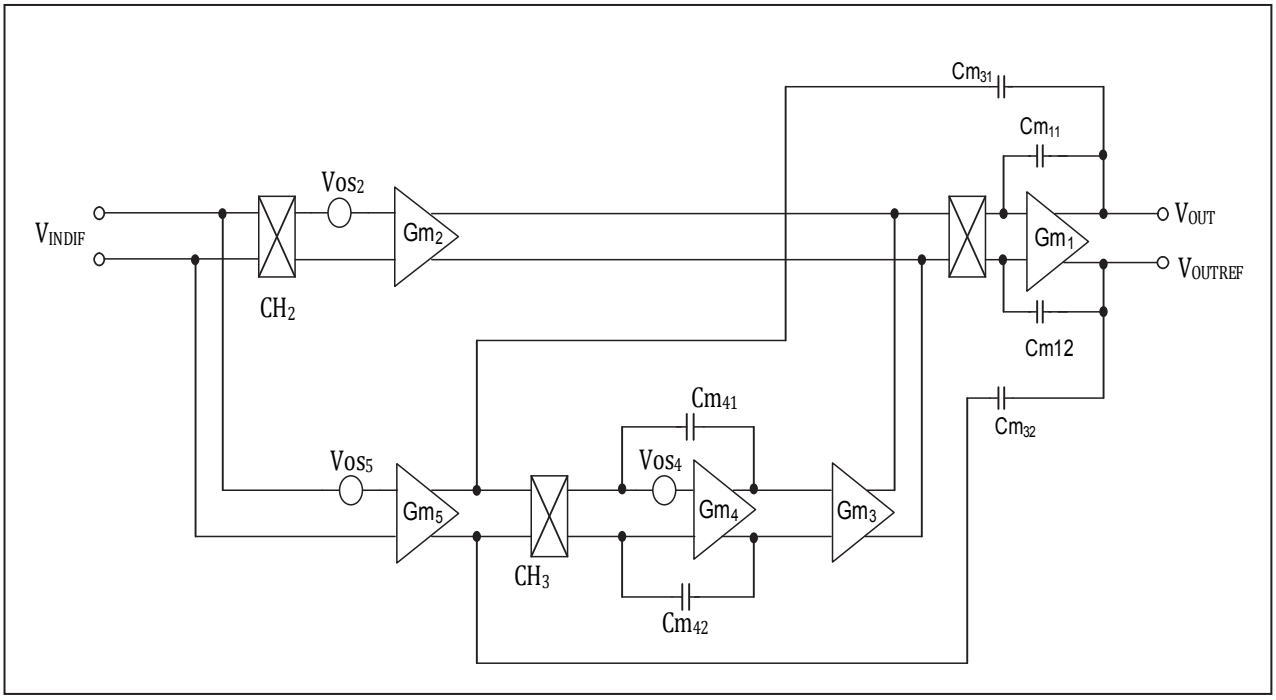

Figure 5-14 – Chopper-Stabilized Chopper Amplifier with Multipath Hybrid-Nested Miller Compensation.

5.2.6 Chopper Stabilized Auto-Zeroed Chopper Techniques

Addition of Auto-Zeroing technique further enhances the performance of the chopper-stabilized chopper technique for both Op-Amps and Inst-Amps. This addition of Auto-Zeroing is also presented in this thesis in the sections 5.4.2.1, and 5.4.6.1 as shown in figure 5-18, figure 5-19, and figure 5-20 for offset cancellations within the second and third order offset cancellation loops. No further discussion is needed as this approach as part of this thesis will be revisited later on in this chapter, and through implementation in chapter 6.

5.3 Chopper-Stabilized Chopper Inst-Amps Utilizing Indirect Current Feedback Topology

By now, some of the major disadvantages of the previous techniques have already been discussed, therefore the need and motivation behind a new approach becomes evident. A preliminary top-level description of the new approach is given in the next section. A more comprehensive treatment to the architecture and design will gradually be presented in the subsequent sections of this chapter, as well as in chapter 6 when realization and actual circuit designs are discussed. Throughout this design, the Indirect Current Feedback Inst-Amp topology, also known as Current Feedback Instrumentation Amplifier (CFIA) is chosen to demonstrate the technique. However the technique is applicable to other topologies as well.

In order to introduce the technique, we'll start with a simple CFIA which then will be gradually developed into a Chopper-Stabilized Chopper type with its various Dynamic Offset Cancellation (DOC) loops to compensate for the input-referred offset of the Amplifier. In so doing, the emphasis will be on analyzing the effects of the offsets of different major blocks on the input-referred offset, and ways to reduce or practically eliminate them.

To better convey the concept, simple mathematical formulas are presented whenever possible.

5.4 Chopper-Stabilized Auto-Zeroed Chopper CFIA Development

Figure 5-15 shows the block diagram of a Chopper-Stabilized Chopper CFIA, with first level offset cancellation loop. No Auto-Zeroing is employed in this figure.

The architecture, like all the other chopper topologies, is considered a continuous time technique; however, it has an additional Chopper stabilization loop to cancel the offsets of the main input transconductance amplifiers. It will be shown that similar loops are used for other transconductance amplifiers and integrators in the circuit as needed.

Later on in this chapter, it is observed how the Auto-Zeroing technique is additionally employed to remove offsets of transconductance amplifiers in the offset compensation loops themselves. This reduces the residual offset and ripple referred to the input of the Inst-Amp.

Since the principal of the Current Feedback Instrumentation Amplifiers (section 1.3), together with Chopper Stabilized Inst-Amps (section 5.2.4) have already been discussed, there will be no need to spend much time describing the detailed aspects of these topologies again, rather the emphasize will be on the Chopper-Stabilized Chopper part of the design.

For the sake of continuity, a very short overview of the Indirect Current Feedback Inst-Amp (ICFIA), or for short (CFIA), and its input-output relationship is given.

It has shown before that the voltage to current convertor Gm_7 senses the differential input voltage $V_{in_{dif}} = V_{in+} - V_{in-}$ and converts it to a differential current. Likewise the transconductance Gm_8 senses, and converts an attenuated version of the differential output voltage of the value ($\frac{R_1}{R_1+R_2}\ V_{out_{dif}}$), to a differential current. Assuming $Gm_7 = Gm_8$, the high loop gain of the amplifier forces these two voltages and therefore currents to be equal, so once again the amplification factor of this topology is derived as:

$$Gain = 1 + \frac{R_2}{R_1} \qquad \textbf{(5.7)}$$

By looking at the circuit, one can recognize a high frequency chopper paths consisting of Gm_7 and Gm_8, in conjunction with their pre and post choppers CH_3 /CH_1 and CH_4/CH_1.

These paths are followed by the transconductance blocks Gm_2 and Gm_1after the chopper CH_1 (the demodulator). This is the main circuitry, which together with the gain setting resistors R_2 and R_1 in the feedback loop, constitutes the familiar Indirect Current Feedback Instrumentation topology. However, in this case, when compared to a conventional ICFIA, there are additional components, i.e. choppers at the inputs and outputs of Gm_7 and Gm_8, similar to conventional chopper designs (section 5.2.1).

For the rest of this chapter and throughout different subsections, first the effects of the native offsets of major blocks are studied and then techniques are introduced to remove such effects on the input referred offset of the Inst-Amp.

We start with the main transconductance blocks Gm_7 and Gm_8in figure 5-15, and will further transform the circuit into its final shape. Throughout this transformation simple mathematical formulas will be presented as needed, but not to the extent that exceedingly overshadows the intuition.

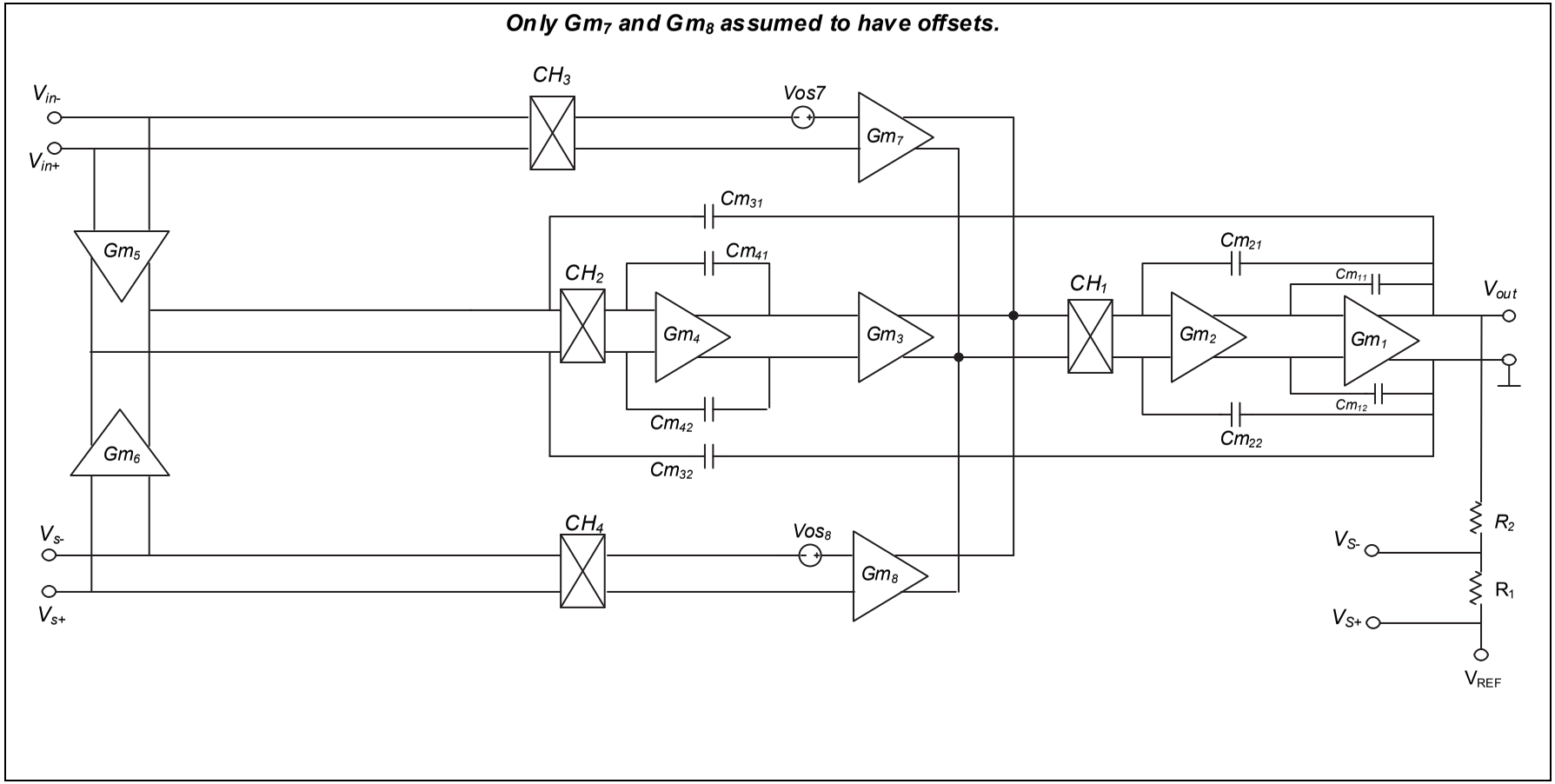

Figure 5-15 – Block Diagram of a Chopper-Stabilized Chopper Instrumentation Amplifier with First Level Offset Cancellation

5.4.1 Removal of the Input-Referred offset due to the Offset of the Input Transconductances of the High-Frequency path (G_{m7} and G_{m8})

Shown in figure 5-15 there is a low frequency path consisting of Gm_5 / Gm_6, CH_2, Gm_4, and Gm_3, as an additional gain path, to perform Chopper Stabilization on Gm_7 and Gm_8, in order to remove their offsets.

With the exception of Gm_7 and Gm_8, assuming that all the blocks are free of offsets, any offset of Gm_7 and Gm_8 will be chopped into square waves at the input of their choppers. The Transconductance Amplifier Gm_6 senses a ripple at its input, the feedback terminals, which is the result of the combined chopped offsets of Gm_7 and Gm_8. This is due to the high loop gain, in conjunction with the existence of the external signal source, which will force the input of CH_3 to its voltage at any given time, here equal to zero.

Since this combined square wave originates from the offsets of Gm_7 and Gm_8 (i.e., Vos_7 and Vos_8) its amplitude, is therefore proportional to the algebraic some of the two offset error voltages. This square wave error voltage at the input of Gm_6 is converted to a square wave current by this transconductance, and is passed through CH_2, where it gets rectified to a *DC* current proportional to the sum of the offsets of Gm_7 and Gm_8. The current is then filtered (integrated) by the integrator Gm_4, and a *DC* output voltage (per clock cycle) is built across integrator capacitors $Cm_{41}$and Cm_{42} equal to:

$$\Delta V_{(Cm_{41}),(Cm_{42})} = \frac{V_{os_{(7+8)}}\, Gm_6}{Cm_{41}} \cdot \frac{1}{f_{ch}}; \quad \text{per intergrator capacitor per cycle} \qquad \textbf{(5.8)}$$

Here, $V_{os_{(7+8)}}$ is the combined offsets of Gm_7 and Gm_8, that is,$(V_{os7} + V_{os8})$, f_{ch} is the chopping frequency, Gm_6 is the transconductance value of amplifier Gm_6 itself, and Cm_{41} is the value of the integrator capacitor.

Over many clock cycles (several hundred or more), this incremental capacitor voltage at the output of the integrator is finally settled to a *DC* voltage level, just enough to get the offsets of Gm_7 and Gm_8 within their residual values at the summing point of Gm_7 and Gm_8 outputs.

This happens as follows: the differential output voltage of the integrator, that is, $(V_{Cm_{41}} - V_{Cm_{42}})$ is converted back to a *DC* current by the weak transconductance Gm_3, and is applied to the summing point at the outputs of Gm_7 and Gm_8, where their offset originated error current is mainly cancelled out and removed prior to the chopper CH_1.

After so many clock cycles, the charging current for the integrator capacitors, which had the original value $(I_{Gm_6} = V_{os_{(7+8)}}\, Gm_6)$, is now so low in value that going forward, the incremental voltages to be added and stored in the integrator capacitors are at the same order of the leakages and voltage droop rates for the same capacitors between successive clock cycles. This is the

current level for which the compensation loop has reached its equilibrium, and therefore defines the residual offset due to the offsets of $Gm_7$and Gm_8.

The signal-dependant voltage component at the input of Gm_6 is compensated and removed by the signal-dependant portion of the voltage at the input of Gm_5, hence its use. This is done to make the error compensating loop independent of the input signal [15] & [18].

It should be noted that with all ideal offset-free Gm_i blocks but Gm_7 and Gm_8, the offsets of Gm_7 and Gm_8 are practically removed. Therefore what is modulated by CH_1 (in a conventional chopper sense) is just the residual offset error of the combined V_{os7} and V_{os8}. This is orders of magnitude less than the original square wave offset error which would have otherwise existed before CH_1, and modulated by this chopper. This means that there is no need for low pass filtering at the output of this Chopper-Stabilized Chopper Instrumentation Amplifier, because the error is practically removed before CH_1. In fact, the input referred offset voltage (ripple), as a result of the offsets of Gm_7 and Gm_8, i.e., $V_{rip_{in\,(7+8)_{pp}}}$ is very low and given by:

$$V_{rip_{in\,(7+8)_{pp}}} = 2\,V_{os_{(7+8)}} \cdot \frac{A_7}{A_3 \cdot A_4 \cdot A_5}; \qquad \text{peak input referred ripple} \qquad \textbf{(5.9)}$$

Where, A_3, A_4, A_5, and A_7 are the *DC* gains of Gm_3, Gm_4, Gm_5, and Gm_7 respectively.
It is clear that the lower the initial offsets and the higher the above mentioned gains, the lower is the residual offset seen at the input. Notice that the term $V_{os_{(7+8)}}$, (or similar offset terms, when used elsewhere in this thesis) refers to the combined or algebraic sum of the offset voltages V_{os7} and V_{os8}, (or the likes). This means that their offset magnitudes could be added or subtracted, depending on the random offset polarities of these error sources.

5.4.2 Input-Referred offset due to the offset of the Input Transconductances of the Low-Frequency Path (Gm_5 and Gm_6)

Now assume that low-frequency (Chopper-Stabilized) path input Transconductances Gm_5 and Gm_6 have their offset errors V_{os5} and V_{os6} as depicted in figure 5-16 . Furthermore, suppose that these are the only offsets seen within the entire circuit. These error sources will generate two additional *DC* currents ($Gm_5 . V_{os5}$) and ($Gm_6 . V_{os6}$), which are algebraically added before CH_2. This chopper will convert the *DC* current into a chopped current (square wave) and will pass it on to the integrator Gm_4, where it is integrated and appears as a small triangle-voltage at its output as shown in figure 5-17. The magnitude of this triangle-voltage at the output of Gm_4 depends on its origin, i.e., the combined offsets of V_{os5} and V_{os6}, the transconductance values $Gm_6 = Gm_5$, the integrator capacitor values $Cm_{41} = Cm_{42}$, and the chopper clock frequency f_{ch}.

$$Vtri_{56_{pp}} = 2V_{os_{(5+6)}} \cdot \frac{Gm_6}{Cm_{41}} \cdot \frac{T}{2}; \quad \text{at the differential output of } \mathrm{Gm_4} \qquad \textbf{(5.10)}$$

Or:

$$Vtri_{56_{pp}} = \frac{V_{os_{(5+6)}} \cdot Gm_6}{Cm_{41} \cdot f_{ch}}; \qquad \text{at the differential output of Gm4} \qquad \textbf{(5.11)}$$

This small triangle-voltage is symmetric around the *DC* output voltage of the integrator, and as such is averaged to zero. However, it has a very pronounced and adverse effect when referred to the instrumentation amplifier's input. The triangle-voltage is converted to a triangle current by Gm_3, reflected back to the input through Gm_7 and CH_3, where it is now converted to a small saw tooth wave (through the act of CH_3), at twice the chopping frequency. The magnitude of this saw tooth voltage referred to the input of the Inst-Amp is therefore:

$$Vst_{in_{(5+6)_{pp}}} = \frac{V_{os_{(5+6)}} \cdot Gm_6 \cdot Gm_3}{Cm_{41} \cdot f_{ch} \cdot Gm_7}; \qquad \text{input referred} \qquad \textbf{(5.12)}$$

Note here that in order to reduce this effect, there is a need to reduce the values of Gm_3 and Gm_6, increase Gm_7, and choose a bigger integrator capacitor, in addition to increasing the chopping frequency. It is not always easy to take some or all of these measures to reduce the above saw-tooth ripple, as the penalty could be an increase in another ripple and or spikes due to the offsets presented by other transconductance amplifiers. Also, as always the increase in chip area and cost is another concern. Nonetheless this ripple must be removed.

As an example of examining the magnitude of such a ripple, note that for a clock frequency of 40kHz, an integrator capacitor value of 30pF, transconductance values of 1/1.2M, 1/0.6M, and 1/12kΩ for Gm_3, Gm_6, and Gm_7 respectively, along with a combined offset $\left|V_{os_{(5+6)}}\right|$ of 20mV, the peak-to-peak saw tooth voltage referred to the input reaches 270μV. This is not acceptable and must be taken care of, as will be shown shortly.

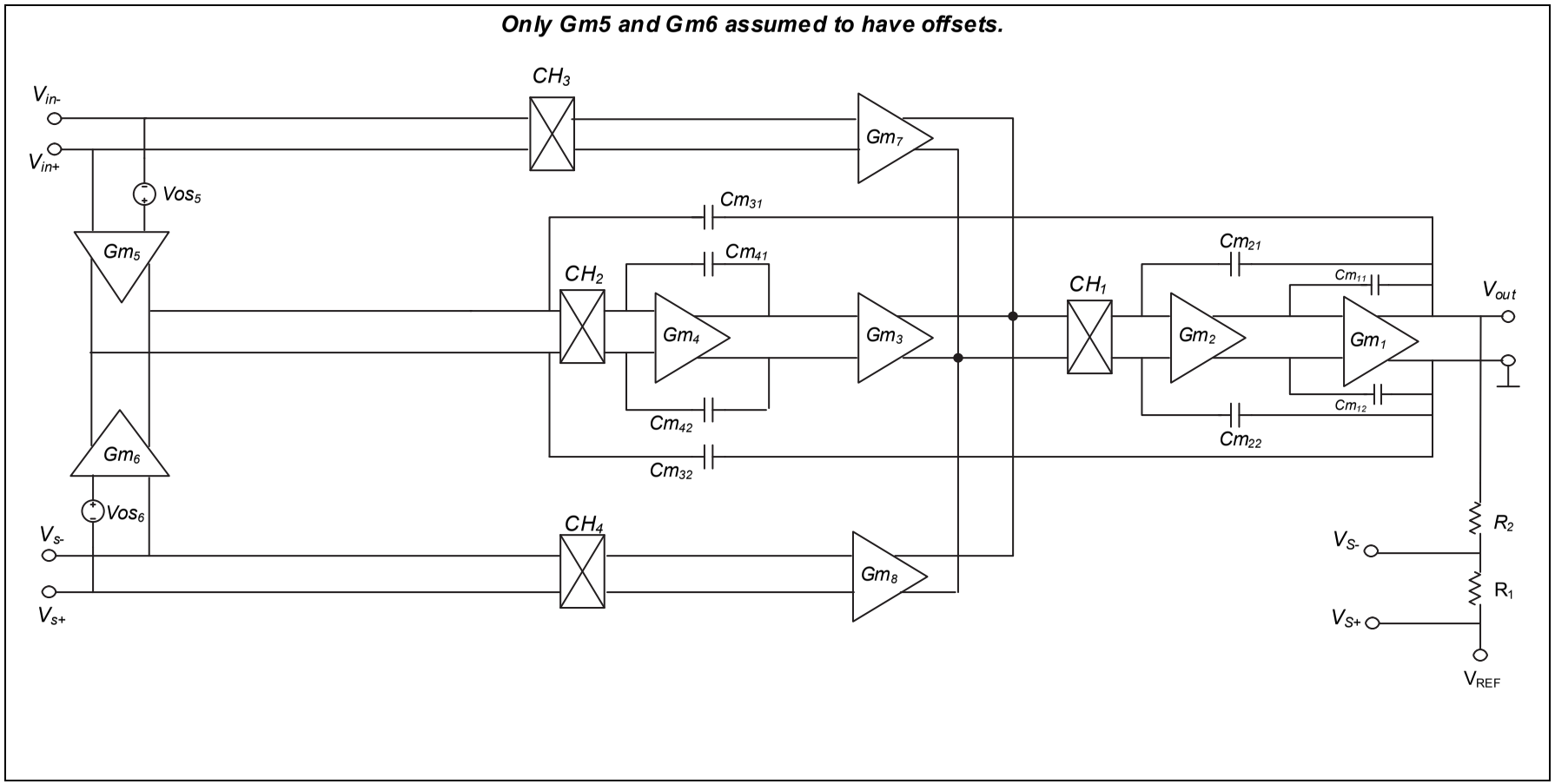

Figure 5-16 – Block Diagram of Chopper-Stabilized Chopper Instrumentation Amplifier – Only Gm_5 and Gm_6 have offset errors.

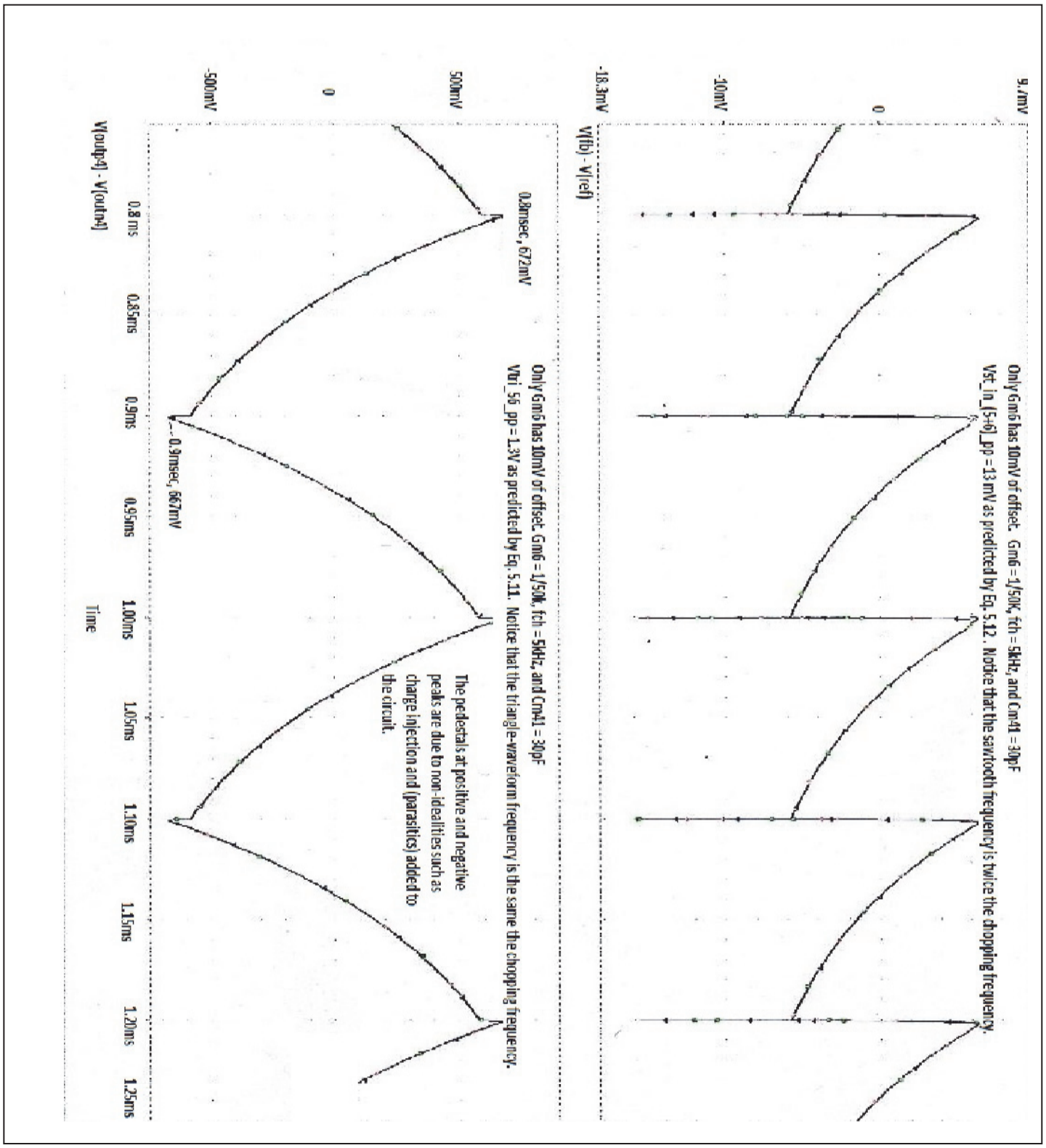

Figure 5-17 – Errors Due to $V_{os(5+6)}$ throughout the Chopper-Stabilization path

5.4.2.1 Offset Removal of the Input Transconductances of the Low-Frequency Path (Gm_5 and Gm_6)

We now examine the compensation loop used to remove the offset of the sense transconductances Gm_5 and Gm_6 in figure 5-18. The integrator Gm_9 receives (through an added multiplexer switch, MUX_1), a *DC* differential input current proportional to the offsets of Gm_5 and Gm_6 combined, but converted to a current by these same transconductance amplifiers themselves. This occurs at every half a cycle of the multiplexer's clock. Gm_9 integrates this differential *DC* current and through many cycles of the chopping clock, gradually stores a *DC* voltage across its capacitors.

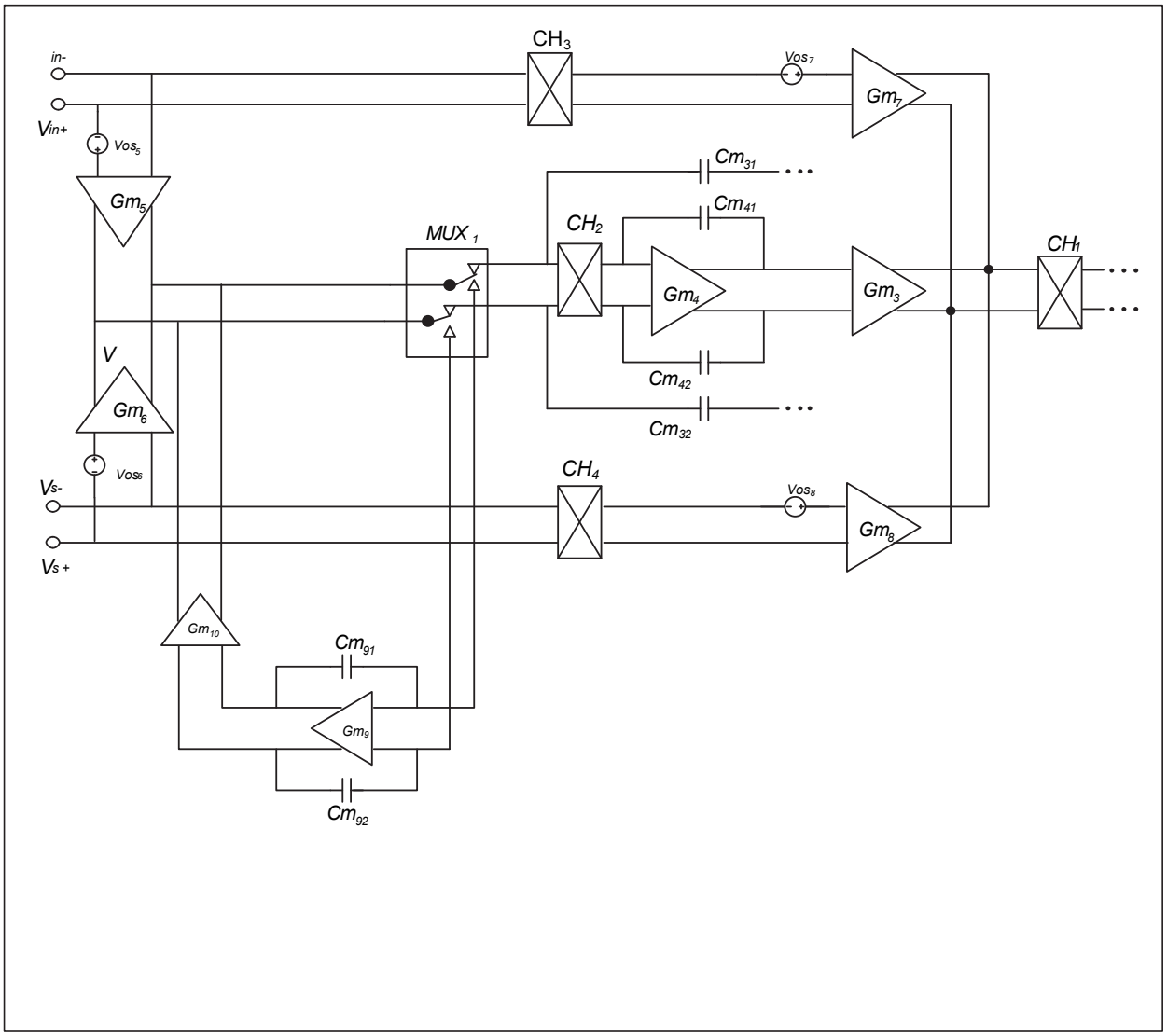

Figure 5-18 – Removal of Offsets of Gm_5 / Gm_6 through a Second Order Compensation Auto-Zeroing (Gm_9 / Gm_{10})

Transconductance Gm_{10} converts this correction voltage into a current and applies it to the summing junction of the outputs of Gm_5 and Gm_6. This is similar to the action of $Gm_4$and $Gm_3$to remove the offsets of Gm_7 and Gm_8; however the additional second-order compensation loop
(MUX_1, Gm_9, and Gm_{10}) is a type of Auto-Zeroing Compensation Technique.

MUX_1 is a multiplexer switch to share the summing junction of the outputs of $Gm_5$and Gm_6, between the inputs of Gm_9 and CH_2. For half of the time, this summing junction is connected to the input of Gm_9 to allow the correction of the offsets of Gm_5 and Gm_6, and for the other half, the multiplexer connects this summing point to the input of CH_2 in order for the main low frequency compensation loop to be able to remove the offsets of Gm_7 and Gm_8.

The MUX_1 switch is operating at a frequency f_{mux} equal to one half of the chopping frequency $f_{ch}$to perform its function. With the addition of this MUX_1, the integrator Gm_4 charges up twice slower compared to when MUX_1 did not exist, simply because the other half time is used to compensate the offset of Gm_5 and Gm_6 themselves. Considering this sharing, the Eq. (5.8) is now updated as:

$$\Delta V_{(Cm_{41}),(Cm_{42})} = \frac{V_{os_{(7+8)}}\, Gm_6}{Cm_{41}} \cdot \frac{1}{f_{mux}};\ \text{per intergrator capacitor per cycle} \qquad \textbf{(5.13)}$$

or:

$$\Delta V_{(Cm_{41}),(Cm_{42})} = \frac{V_{os_{(7+8)}}\, Gm_6}{Cm_{41}} \cdot \frac{2}{f_{ch}};\ \text{per intergrator capacitor per cycle} \qquad \textbf{(5.14)}$$

Eq. (5.14) simply indicates that with the addition of MUX_1, in order to charge the Gm_4 capacitorsCm_{41} and Cm_{42} to the same voltage as prior to the addition of MUX_1, but within the same time as prior to this addition, one has to double the value of Gm_6 previously suggested by Eq. (5.8).

5.4.3 Input-Referred Offset due to the offset of the Integrator Block (G_{m4})

Another troublesome source of error is the offset of the integrator Gm_4 itself. Assume that Gm_4 is the only transconductance having an offset error of V_{os_4}. This error has to appear as a square-voltage across the parasitic capacitor $Cpar_{56}$ at the output of Gm_5 andGm_6, through the action of CH_2 in front of Gm_4 in figure 5-19.

This means Gm_6 has to charge and discharge Cp_{ar56} to V_{os_4} in each and every clock cycle, which in turn requires a charging and discharging current at the output of Gm_6, or to say a proportional voltage at its input.

Each time there exists a voltage across one of the input or feedback transconductance amplifiers (sayGm_6), the other (Gm_5), will carry the same signal (Gm_5), in opposite direction; so the ripple voltage at the input ofGm_6, as a result of the offset ofGm_4, is considered the ripple at the very input of the instrumentation amplifier as well.

The magnitude of this input referred ripple$V_{rip_{4pp}}$, caused byV_{os_4} is approximated as:

$$V_{rip_{in4pp}} = \frac{8\, V_{os_4} Cpar_{56}\, f_{ch}}{Gm_6}; \quad \text{input referred} \tag{5.15}$$

The factor of 8 above is due to:

a) The charge accumulation in ½ cycle,

b) The single-ended equivalent capacitor seen at the output of Gm_5 and Gm_6, which is twice the differential value of $Cpar_{56}$, and

c) The peak to peak calculation of the ripple at the input.

It is as if one had assumed that the parasitic capacitor$Cpar_{56}$, when chopped at the output of Gm_5 andGm_6, resembles a resistor (in a switch capacitor sense) of the value of:

$$R_{eq_{56}} = \frac{1}{8\, Cpar_{56}\, f_{ch}} \tag{5.16}$$

Therefore:

$$V_{rip_{in4pp}} = \frac{V_{os_4}}{R_{eq_{56}}\, Gm_6}; \quad \text{input referred} \tag{5.17}$$

5.4.3.1 Offset Removal of the Integrator Block (G_{m4})

Note that in order to reduce this ripple which is due toV_{os_4}, there is a need to have:

a) A low offset value of Gm_4 itself; that is a lower native offset, which means a tendency towards designing in Sub-Threshold region;

b) A low parasitic capacitance at the outputs of Gm_5 and Gm_6(which means careful design and layout of these blocks);

c) A lower chopping frequencyf_{ch} and;

d) A higher value forGm_6 .

The last two constrains are in contradiction with the measures proposed previously in Equation (5.12) to reduce the value of the undesired input referred saw-tooth voltage caused by the offsets of Gm_5 and Gm_6 themselves. This means care must be taken when designing such blocks to avoid the implementation of the reduction of one offset, via worsening of the other one.

Also note that the *DC* gain of Gm_4 itself, ($A_4 = Gm_4\, R_{out4}$), to the first degree of approximation, does not have any effect on the ripple caused byV_{os_4}. In Chapter 6, it will be shown that a simulation of the circuit with *A4* values of 100, 1000, and 5000, will show no noticeable effect on $V_{rip_{4pp}}$, but profound effects on $V_{rip_{in\,(7+8)pp}}$ as expected.

As an illustration of the magnitude of the input referred ripple caused by the offset ofGm_4, we now present an example.
Assume that V_{os_4} is 10mV, with a $Cpar_{56}$ total parasitic capacitance of 1.1pF which includes the series combination of compensation capacitors Cm_{31} and Cm_{32}, each1.7pF. If the chopper frequency is 40kHz with a Gm_6 transconductance value of $\frac{1}{50}$ KΩ, then the resultant input referred ripple due to V_{os_4}, that is $V_{rip_{in4pp}}$ is ±80μV.

Although the above offset value may look fine in some applications, in many other precision analog systems is considered unacceptable, and should be eliminated or reduced significantly.

To remove the offset of Gm_4, a chopped version of this offset by CH_2 is fed to the sense amplifier Gm_{14}. This square wave offset error of Gm_4, after passing through another multiplexer, MUX_2, (not shown in figure 5-19), is rectified by CH_7, integrated by Gm_{15}, and finally converted back to a current by Gm_{16}, which is then applied to the output of $Gm_4$to remove its offset as shown in figure 5-19.
It should be noted here that to improve on a first order offset cancellation design, we could add these secondary loops, such as the one with sense amplifier Gm_9 added for compensation of the offsets of Gm_5 /Gm_6 , or Gm_{14} for that of integrator *Gm4*. However care should be taken to watch for the offsets of such sense amplifiers or the integrators of these second order loops themselves.

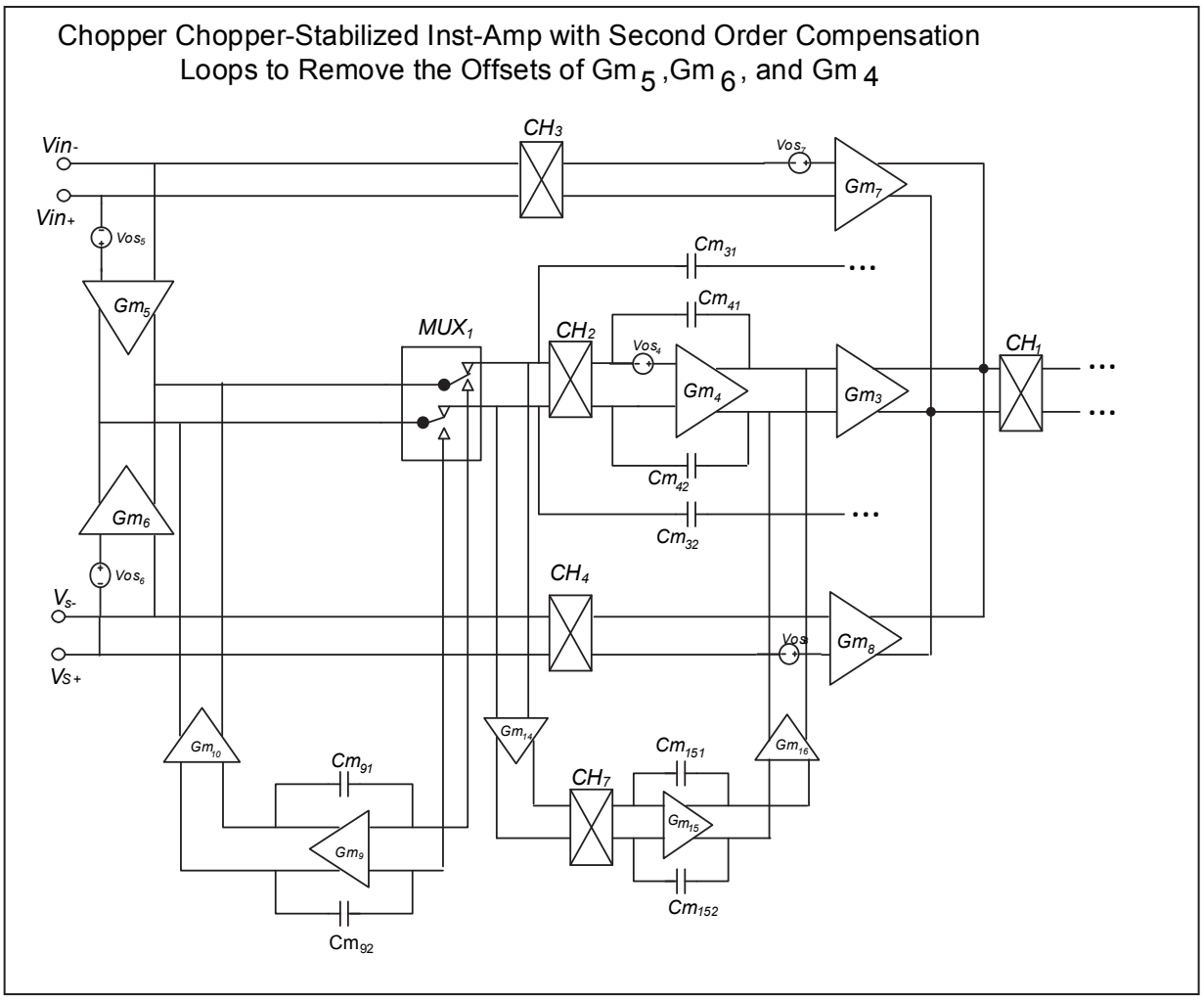

Figure 5-19 – Second Order Cancellation Loops to Remove the Offsets of Gm_4, Gm_5 / Gm_6

5.4.4 Input-Referred Offset due to the Weak transconductance (G_{m3})

It is shown here that any real life offset error of weak transconductance Gm_3 has no effect on the performance of the Inst-Amp for three reasons:

1) The value of Gm_3 is normally chosen to be very low as will be shown in chapter 6.

2) Any offset of Gm_3 , that is V_{os_3} (in the range of mV) when added to the integrator output voltage (in the range of Volts), is negligible due to being orders of magnitude lower.

3) The product (multiplication) of (1) and (2) above is divided by the high gain of the forward path from input of Inst-Amp to the output of Gm_3, which makes the input-referred offset insignificant for any application.

The combined effects of all the above will practically eliminate the influence of the Gm_3 offset to the extent that it can be considered non-existent. This argument is also true for any other weak transconductance amplifier preceded by an integrator in this design. Later, it will be shown that any offset of Gm_2, together with CH_1 and the total capacitances at this input, will generate spikes at the output of the instrumentation amplifier which can be reduced by compensating for the offset of Gm_2. Also any capacitive load at the output of Inst-Amp is beneficial in removing such spikes.

As shown earlier and at times, the methods used to mitigate the input referred error voltages caused by the offsets of different transconductance amplifiers are contradictory in nature. This means reducing these effects by careful design for low inherent offset voltages (once again design and operation in subthreshold), and addition of extra compensation loops and/or utilizing Auto-Zeroing technique is in order.

5.4.5 Input-Referred offsets due to the offset of the Integrator Gm_9

Any offsets of Gm_9 transconductance will cause a residual offset (ripple) at the input with the value:

$$V_{rip_{in9_{pp}}} = \frac{V_{os_9}\, A_9\, G_{m_{10}}}{G_{m_6}}; \qquad \text{referred to the input} \qquad \textbf{(5.18)}$$

A practical way to look at the above formula considering the parasitic capacitances at the output of G_{m_5}, and G_{m_6}, that is $Cpar_{56}$, as well as G_{m_9} integrator capacitors $Cm_{91}$and Cm_{92}, is simply to replace the G_{m_9} gain, that is A_9 , by the capacitor ratio which sets the gain. That is:

$$A_9 = \frac{Cpar_{56}}{Cm_{91} \perp Cm_{92}}; (\perp = \text{in series with}); \qquad \text{input referred} \qquad \textbf{(5.19)}$$

therefore:

$$V_{rip_{in9_{pp}}} = \frac{V_{os_9}\, Cpar_{56}\, G_{m_{10}}}{(Cm_{91} \perp Cm_{92})G_{m_6}}; \qquad \text{input referred} \qquad \textbf{(5.20)}$$

As an example to demonstrate the application of Eq. (5.18), if A_9 is in the order of $2 \cdot 10^3$, and $G_{m_{10}}$and $G_{m_6}$are 1/50MΩ and 1/25kΩ respectively, the offset of Gm_9 will just be equally referred to the input of the Inst-Amp. Obviously this is again an issue to be resolved.

Eq. (5.20) gives a good first hand estimation of the input referred offset caused by the offset of the integrator G_{m_9}, but when single ended parasitic capacitances Cp_{ar56} at the outputs of G_{m_5} and G_{m_6} are also taken into consideration.

It is interesting to see the counterbalancing effect of the equivalent capacitors around G_{m_9}, that is the series combination of Cm_{91} and Cm_{92}, to reduce the undesirable effect of $Cpar_{56}$ on the input referred offset caused by V_{os_9}.

Equation (5.20) was used to calculate the input referred offset due to V_{os_9}, under the exaggerated conditions of $V_{os_9} = 100mV$, with $Cpar_{56}$ = 0.45pF, $G_{m_{10}} = \frac{1}{5\text{M}\Omega}$, $G_{m_5} = G_{m_6} = \frac{1}{50\text{k}\Omega}$, along with Cm_{91} = Cm_{92} = each 1.2pF , 5pF, 10pF , and 30pF. The calculated values came reasonably close to the simulation results under the very same conditions as listed in Table 5-1.

Values of Cm_{91} / Cm_{92}	Input-Ref. Offset (Calculation)	Input-Ref. Offset (Simulation)
1.2 pF	750 µV	740 µV
5 pF	180 µV	190 µV
10 pF	90 µV	100 µV
30 pF	30 µV	50 µV

Table 5-1 – Eq. (5.20) Predictions of the Effects of the Integrator Capacitors *Cm91* and *Cm92* on the Input-Referred Offset for Exaggerated *Vos9*=100mV. See Other Parameter Values in the Text.

5.4.5.1 Offset Removal of the Integrator Gm_9

The offset of Gm_9 is compensated by the offset cancellation loop consisting of chopper *CH5*, sense amplifier Gm_{11}, chopper *CH6*, integrator Gm_{12} , and finally the weak transconductance Gm_{13}. Together, these components make a third order cancellation loop, which is employed to remove the offset of Gm_9 as shown in figure 5-20. It should be noted that the effect of the offset of Gm_{11}, or any other 3rd level loop throughout this design is often negligible and doesn't warrant any compensation.

5.4.6 Input-Referred offset due to the offset of the Sense Amplifier G_{m14}

The Transconductance Gm_{14} senses the chopped offset of Gm_4 through *CH2* to eventually provide a correction current of the value ($Gm_4\ V_{os_4}$) through the help of the rectifier chopper *CH7*, the integrator $G_{m_{15}}$, and the weak transconductance $G_{m_{16}}$.

Now if $G_{m_{14}}$ itself has an offset, it will be reflected as a saw-tooth residual at the input of the Inst-Amp through the actions of the choppers CH_7, and CH_3. The magnitude of such an input-referred offset can be estimated by:

$$Vst_{in_{14_{pp}}} = V_{os_{14}} \cdot \frac{A_{14}\, A_{15}\, A_{16} \cdot A_3}{A_7}; \quad referred\ to\ the\ input \qquad \textbf{(5.21)}$$

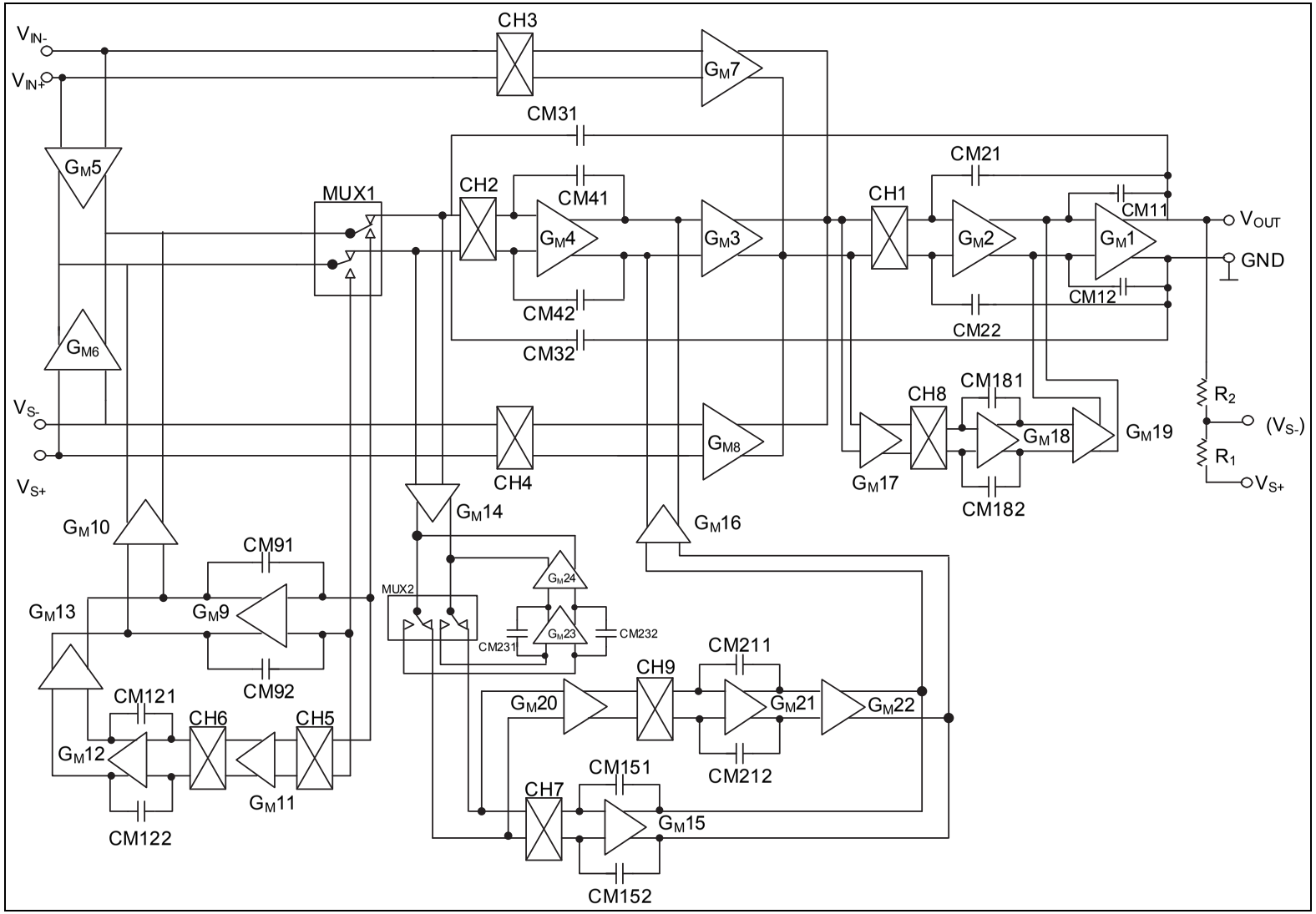

Figure 5-20 – Addition of Third Order Offset Cancellation Loops and Remedy for Spikes (Offset Error Sources are not Shown)

5.4.6.1 Offset Removal of the Sense Amplifier G_{m14}

Referring to figure 5-20 to compensate the offset of $G_{m_{14}}$ use is made of a multiplexer MUX_2 to divert the offset current of $G_{m_{14}}$ equal to ($Gm_4\ V_{os_4}$) at its output to an Auto-Zeroing compensation loop. The loop is composed of the integrator Gm_{24} and the weak transconductance $G_{m_{23}}$ working in a similar manner as the case of compensation loop for Gm_5 and Gm_6.

The multiplexer MUX_2 is also used to redirect the output of $G_{m_{14}}$ to the compensation loop for G_{m_4} as discussed previously in section 5.4.3.1.

Here again, similar to case of MUX_1, the MUX_2 switch is operating at a frequency f_{mux} equal to one half of the chopping frequency $f_{ch}$to perform its function.

5.4.7 Input-Referred offset due to the offset of the Integrator G_{m15}

It is interesting to note that any offset of $G_{m_{15}}$ will look like an input-referred ripple at the chopping frequency by the reflection to the input through $G_{m_{16}}$, G_{m_3}, G_{m_7} , and the action of chopper CH_3 . For this reason, the offsets of these secondary loops are compensated as well. Equation (5.22) estimates the magnitude of this input-referred ripple caused by the offset of m_{15} .

$$V_{rip_{in15_{pp}}} = V_{os_{15}} \cdot \frac{A_{15}\, A_{16}\, A_3}{A_7}; \quad referred\ to\ the\ input \tag{5.22}$$

5.4.7.1 Offset Removal of the Integrator G_{m15}

The compensation loop to remove the offset of Gm_{15} in figure 5-20 consists of Gm_{20}, CH_9, Gm_{21}, and Gm_{22}. The loop reacts to this offset voltage and performs in the very familiar way which has been discussed for several loops thus far. Note that not all the offset voltages to be compensated are shown in figure 5-20.

5.4.8 Effects of the offset of the Transimpedance G_{m2} on V_{out} Spikes

The offset of Gm_2 will have less impact on the input-referred offset as opposed to spikes at the output of the Inst-Amp generated by the presence of this offset as will be explained here. One should also note that any amplifier placed after a chopper will have its offset chopped by that chopper which then appears across the parasitic capacitors at these nodes.

These parasitic capacitors could be the one at the output of the previous amplifier, or any extra capacitance connected there, such as compensation capacitors. Normally the previous amplifier has to supply a current to produce this chopped offset (a square wave) to these capacitors.

Applying any square wave to a capacitor directly with no significant resistor in the path, will cause spikes at the impedances following the capacitors, as capacitors cannot change voltages instantly. This, in a sense, is similar to the action of a differentiator consisting of the capacitors and the follow up impedances, acting on the chopped offset.

If one looks at the transimpedance Gm_2 in this design, CH_1 will chop its offset, and Gm_7 has to supply the current to make up for it. This means:

There would be a ripple at the input of the transconductance Gm_7, but a residual offset before CH_3, or at the input of the Inst-Amp, due to the action of this chopper. However, the value of this residual offset is extremely low compared to any other input-referred offset; therefore this residual offset can safely be considered non-existent.

The chopped offset of Gm_2 causes the parasitic capacitances prior to CH_1 (capacitances of the summing nodes) to get charged and discharged rapidly, which in turn will produce spikes at the output, through the Miller Capacitors $C_{m_{21}}$ and $C_{m_{22}}$.

The magnitude of these spikes are eliminated or lowered, if somehow, the original cause of it, that is, the offset of Gm_2 is eliminated or reduced. Also lowering the parasitic capacitances prior to CH_1 and increasing the Miller Caps (when possible), as well as the use of any likely capacitive load at the output, will reduce these spikes significantly.

From a charge conservation principle and charge sharing between the parasitic capacitance $C_{par_{78}}$ and Miller capacitors $C_{m_{21}}$ and $C_{m_{22}}$ it is evident that:

$$V_{spikes_{out}} = \frac{V_{os_2} C_{par_{78}}}{C_{m_{21}} \perp C_{m_{22}}}, \qquad (\perp = \text{in series with}) \qquad \textbf{(5.23)}$$

Where $V_{spikes_{out}}$ show the magnitude of spikes at the output of the amplifier. It is interesting to note that this formula is quite accurate and matches the simulation results for ideal choppers with no parasitic capacitors from the clock driving points (gates of the choppers) to the inputs and outputs of the choppers themselves.

In a real implementation of choppers, due to the existence of such parasitic capacitors, the magnitude of spikes are much larger and could reach values of an order of magnitude bigger compared to what is predicted by the above equation. This is again considered an undesirable nuisance and better be corrected by a cautious design for switches (as minimum sizes as possible), and a careful layout symmetry consideration for such components.

The addition of the second order compensation loop of Gm_{17},Gm_{18}, and Gm_{19} around Gm_2 in the design is primarily for compensating V_{os_2}, and therefore reducing the output spikes.

5.4.8.1 Offset Removal of the Transimpedance G_{m2}

Referring to figure 5-20 again, one recognizes the familiar offset compensation loop consisting of the sense amplifier Gm_{17} prior to chopper CH_1, followed by the chopper CH_8 and integrator Gm_{18}, and finally the weak transconductance Gm_{19} in the known configuration that has been discussed so far. Notice that the chopped offset of Gm_2 is converted back to a DC current by the rectification action of CH_8 prior to building the required rectified voltage across m_{18} , as well as the rectified current out of Gm_{19} to dynamically cancel the offset of Gm_2 .

5.4.9 Summary of the Effects of Different Transconductance Native Offsets, along with other parameters on the Input-Referred Offset

At this point we can tabulate and summarize a high level snapshot of what has been shown so far. In particular we would like to know the effects of the offsets of different individual blocks within the CFIA design on the Input-Referred Offset or Spike.

Some immediate observations are:

i- The original or native offset should be as low as possible to begin with. This means design in subthreshold region is desirable, if speed and bandwidth are not in the way.

ii- Parasitic capacitances in the signal path, in particular prior to choppers must be kept as low as possible. This is very much layout and device size dependent.

iii- Effects of the offsets of the weak transconductances after the integrators are often negligible due to the summation of this offset with the large voltages across integrators (often a fraction of volt).

iv- Bigger integrator and Miller capacitors help reduce the effects of the individual offsets of the internal blocks on the Input-Referred offset. However area, cost and speed limitations impose an upper boundary on the practical values for such capacitors.

v- The offsets within the third level compensation loops can often be disregarded due to the negligible effect at the input.

vi- Some parameters (transconductances, chopping frequency, voltage gains of the blocks) might have contradictory effects on the Input-Referred offsets caused by their individual offsets; therefore care must be taken to pick a sweet-spot for such parameters, often fine-tuned, and finalized by simulations.

vii- Table 5-2 is a summary table to show the effects of the individual offsets of different blocks on the input-referred offset of the CFIA Inst-Amp under study.

In chapter 6, when we talk about Realization, we further discuss these topics.

Input-Ref Effects of the V_{os_x} is lower if:	Gm_2	Gm_3	Gm_4	Gm_5 & Gm_6	Gm_7 & Gm_8	Gm_9	Gm_{10}	Gm_{14}	Gm_{15}	A_3	A_4	A_5 & A_6	A_7 & A_8	A_9	A_{14}	A_{15}	A_{16}	f_{ch}	Cm_{21} & Cm_{22}	Cm_{41} & Cm_{42}	Cm_{91} & Cm_{92}	$C_{par_{78}}$	$C_{par_{56}}$
$Native\ V_{os_2}$ ↓ (Seen as Spikes)																			↑			↓	
$Native\ V_{os_4}$ ↓ (Seen as Ripple)				↑														↓					↓
$Native\ V_{os_5}$ ↓ (Seen as Ripple)		↓		↓	↑													↑		↑			
$Native\ V_{os_6}$ ↓ (Seen as Ripple)		↓		↓	↑													↑		↑			
$Native\ V_{os_7}$ ↓ (Seen as Ripple)										↑	↑	↑	↓										
$Native\ V_{os_8}$ ↓ (Seen as Ripple)										↑	↑	↑	↓										
$Native\ V_{os_9}$ ↓ (Seen as Ripple)				↑			↓							↓							↑		↓
$Native\ V_{os_{14}}$ ↓ (Seen as Ripple)										↓			↑		↓	↓	↓						
$Native\ V_{os_{15}}$ ↓ (Seen as Ripple)										↓			↑			↓	↓						

Table 5-2 – Effects of the Offsets of Different Transconductance Blocks, and other Components on the Input-Referred Offset.

5.4.10 Overcoming Frequency Compensation Issues Caused by the Existence of a Two-Path Amplification

At this point it is important to pinpoint an aspect of the frequency compensation regarding such designs. More detailed discussions of how to design the frequency compensation network is discussed in chapter 6 when we deal with the implementation of our design.

Recall that this architecture is a two-path amplifier, having a high frequency low gain signal path (Gm_7 ,Gm_2 , Gm_1), along with it low frequency high gain signal path of (Gm_5 , Gm_4 , Gm_3 , Gm_2 , Gm_1), as shown in figure 5-15 or figure 5-20.

Due to the existing of these two signal paths, and the inequality of their time constants, any signal at the common input of the amplifier will experience different delays throughout these paths. This difference in delays could lead to instabilities in certain band of frequencies, noticeably towards the lower frequencies.

The above instability can be seen, together with its range of unstable frequencies, in a gain vs. frequency plot of the amplifier (Magnitude Plot) shown in Figure 5-21.

The plot clearly shows a break point in the otherwise 6dB straight role-off curve at lower frequencies, due to the existence of the low frequency gain path and its added pole to the overall frequency response of the amplifier.

Moving along the magnitude plot from higher to lower frequencies, there comes a certain frequency (f_3)at which the low frequency path has now more gain that the main high frequency path of the amplifier, and its extra pole calls for a 12dB / octave roll-off at frequencies lower than f_3. When reaching the 3dB frequency of the main path (f_1), where afterwards the gain of the main path is flat, the overall characteristic of the amplifier shows a 6dB / octave roll-off again.

Continue moving along leftwards, at some low frequency (f_2), the non-idealities of the integrator and leakage prevent the integration function, and the response becomes flat from that point on towards extremely low frequencies. Using such an amplifier at low frequencies, where the slope is 12dB / octave could be troublesome and causing instability [13]. This problem can be resolved by applying the principle of hybrid nesting as presented in [13] & [18].

If one connects two hybrid nested Miller capacitors of Cm_{31} and Cm_{32}, from the very output to the inputs of Gm_4 in the *DC* path, and make the bandwidth of the three stage Miller Compensated high frequency (AC path) of Gm_7, Gm_2, Gm_1, equal to the bandwidth of multi stage Hybrid Nested Miller path of Gm_5 , Gm_4, Gm_3, Gm_2, Gm_1, the overall frequency response becomes a straight roll-off of 6dB / octave, over the entire bandwidth of the Inst-Amp.

For the above to happen, the following relationship should hold true:

$$\frac{G_{m_5}}{2\pi(Cm_{31} \perp Cm_{32})} = \frac{G_{m_7}}{2\pi(Cm_{21} \perp Cm_{22})} \quad \textbf{(5.24)}$$

Notice that the capacitors Cm_{31} and Cm_{32} are not directly connected to the inputs of Gm_4, but through the chopper CH_2 in front of Gm_4. This is done to counter-balance the effect of CH_1, which otherwise would have switched the polarities of the signal returned back toGm_4.

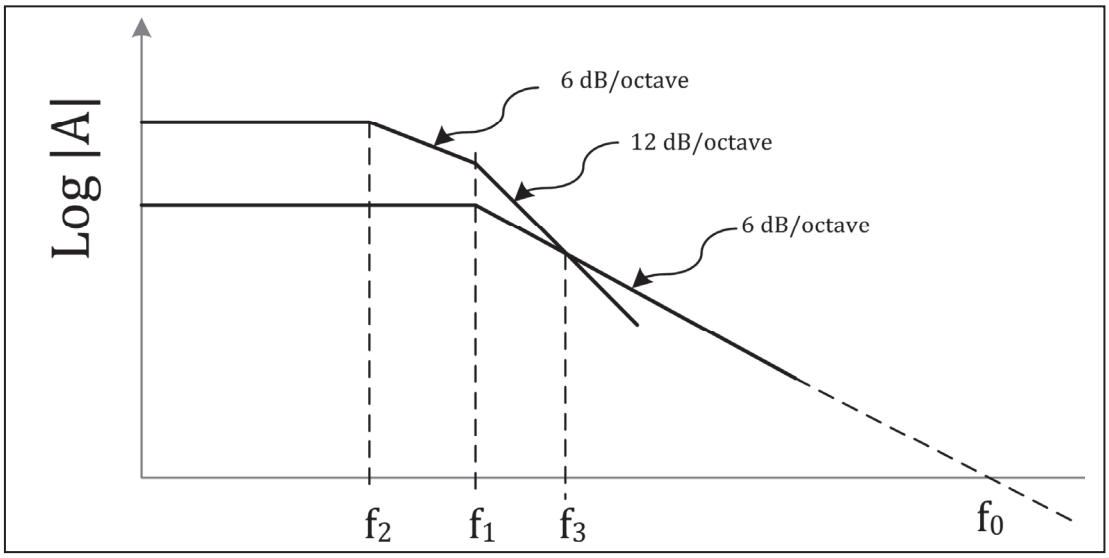

Figure 5-21 – Magnitude Plot of a Two Path Amplifier before Cure

6. Realization

This chapter is devoted to the implementation of the subject of this thesis "Chopper-Stabilized Auto-Zeroed Chopper Techniques". As described in chapter 5, the vehicle to demonstrate the technique is a Current Feedback Instrumentation Amplifier (CFIA), designed in a 0.6µ CMOS Technology.

The choice of the technology node has solely been based on the availability of the process to the designer at the time of the implementation. There is no restriction in applying this method and design implementation into other process technology nodes as desired.

6.1 Top-Down versus Bottom-Up Design Approaches

Nowadays it is well known that the old style of bottom-up design has been replaced by the more coherent top-down design approach. In fact for more complex chips, or system-level designs, this is the only viable alternative to the designer.

In a bottom-up approach, the designer makes all the blocks designed at the transistor-level with presumed specifications. Most simulations are performed in advance, and at the block levels. The second stage of the design consists of connecting all such transistor-level designs together in a partial top-level, and eventually the final top-level schematic. Using this bottom-up approach, design troubleshooting at these top-level stages (partial or final) could be a nightmare for a complex chip.

In top-down design on the other hand, the designer models and perhaps simulates some blocks in advance at this stage. He or she uses simple behavioral models for these blocks with only major characteristic parameters (gain, transconductance, input and output impedances, etc…) defined as simulation parameters. This makes the simulations much faster, and gives the flexibility to change few main parameters for optimal performance.
The next step is connecting all such blocks together in a partial top-level, and eventually into a final top-level to evaluate the performance of the whole chip as a model based design at system-level.

The bottom-up approach has many shortcomings; some listed here.

i. The bottom-up approach is only suitable for block-level or very small designs.

   The method is practically incapable of gauging the effects of internal design parameters associated with different blocks on the overall design.
   It lacks the flexibility to easily adjust the critical parameters of interests (within the blocks) to obtain an optimal overall performance.

This optimization is very difficult to achieve without going through a huge effort involving transistor-level redesign of some of the already completed blocks.

Model based top-down design techniques do not suffer from the above limitation. The parameters within each block can freely and independently be changed for achieving functionality, or better performance.

ii. In a complex chip (system-level chips) the bottom-up approach often fails to predict the effects of the connections of the individual blocks at the top level, early on. In other words, a bottom-up approach will not expose the problems that might result when different blocks are interfaced together at the top-level of the design.

In a model based top-down design, the critical interface parameters such as input and output impedances can always be easily adjusted for the right functionality or an improved performance; provided that changes stay within acceptable and practical ranges.

iii. The bottom-up approach is neither a practical tool for a meaningful feasibility analysis at the start of the project, nor a viable means for design optimizations throughout, and towards the end of the design phase.

The above two tasks are unconditionally required for any real-world project, in particular the feasibility analysis which is needed right before any sign-off and go-ahead on the project in a working environment.

Top-down design methods are much more forgiving in doing both of the above tasks.

iv. In a bottom-up approach and at the top-level, the design modifications or optimizations tasks take a tremendous toll on the simulation tools.

As an example, the simulation time for any modifications in a circuit like this design at the very top-level, with all transistor-level blocks, could take days to finish. This is true even if the circuit parasitics are not included, and the clocks are replaced with their equivalent ideal square-wave clock generators.

By contrast, the model based top-down approach likely needs only a few hours to finish the same task. In a working environment, where there are limited shared licenses available to design communities, this is a big advantage for cost considerations.

v. With the bottom-up approach and complex chips, troubleshooting of the system (at the design phase of the project) is extremely difficult.

This is due to the lack of visibility to recognize the cause and effect in any particular issue. When all the transistor-level blocks are already connected, they affect and interact with each other to make the troubleshooting a tedious job.

On the other hand, in a model based top-down approach troubleshooting at the design phase is natural and simple. Since the transistor-level design starts only when the model based top-down design has already been deem to work correctly, a replacement of a model based block with its transistor-level counterpart is quite revealing. It immediately shows if this newly substituted transistor-level is functional or not. It also determines if the already accepted performance of the behavioral design has been deteriorated by this substitution.

The process of replacing each block with its transistor counterpart continues until all the blocks are replaced with their actual transistor-level designs without any degradation in functionality or performance of the chip. Note however, that some very minor degradation associated with the limitations of the physical components compared to model based definitions is unavoidable and accepted.

The above indicates the reasons for selecting a top-down design approach in implementing the subject of this thesis.

6.2 Top-Down Design Steps and considerations

In a top-down design approach, the task usually starts with performing some key hand calculations to obtain major characteristic parameters such as transconductances, gains, or frequency compensation network component requirements on a high level basis only.

Care must be taken not to get carried away with too many formulas and hand calculations as simulation tools and models are way more sophisticated and accurate than any hand calculations. Hand calculations are valuable to estimate the initial value of some key parameters. Thereafter, they are useful for guidance and insight as what parameter (knob) within a formula should be adjusted, and in what direction (higher or lower) in order to get the desired results. Exactly how much change or fine-tuning is needed for this particular knob (parameter) should be shown by the simulation tool, not the formula itself.

In a top-down design approach, the designer is not specifically concerned about the actual transistor level implementations of the blocks, even at the model top-level. However he or she does consider the right choice of the process technology, and the preferred technology node, as this eventually impacts the size and cost of the product. Some of the important aspects of the process technology selection are described in section 6.3.

In choosing the design parameters for each block, the focus is on the parameter itself and the sensibility of its value. Unless there is an impractical assignment for the value of a parameter, an indication against the commonly accepted “good design practices”, or perhaps a requirement

outside the capability of the chosen process technology, simple hand calculations should be sufficient to start the design and get the project going.

Throughout the design, the designer has the freedom to frequently change any and all parameters within a block or blocks of interest. This is not only at the beginning of the project (feasibility analysis), but as mentioned before, can be repeated throughout the actual design phase many times for the optimization purposes.

Figure 6-1 shows a Flow-Diagram of a Top-Down design. It is important to notice that the parasitic extraction step for switching circuits in general, and chopper circuits in particular is crucial.

Large unexpected errors in the form of ripples or spikes, often at the clock frequency could result if one is not careful with the design of choppers, with considering the general parasitic effects, or with shielding the sensitive analog nodes and traces from clock and noisy digital circuits in the layout.

Causing such errors is very possible in the final days of wrapping up the layout, and getting the database ready for tapeout. During this time, the circuit and layout designers can be moving blocks around and altering the distance between trances to eliminate the many usual DRC flags encountered at this stage.

Even though the layout designer has been extremely careful with designer's instructions at the block level layout design, here at the top-level there exists no prior check and balance.

Parasitic extractions, if their models are more or less accurate, are invaluable to expose any feed-through and unwanted couplings or loadings which could potentially lend themselves to undesired results. In the author's own experience, an instance with the proximity of a tiny trace to a 5 volt clock line (with a total coupling capacitance of less than 4fF) caused a spike with a magnitude of about +/-20mV superimposed on a DC offset of few micro volts.

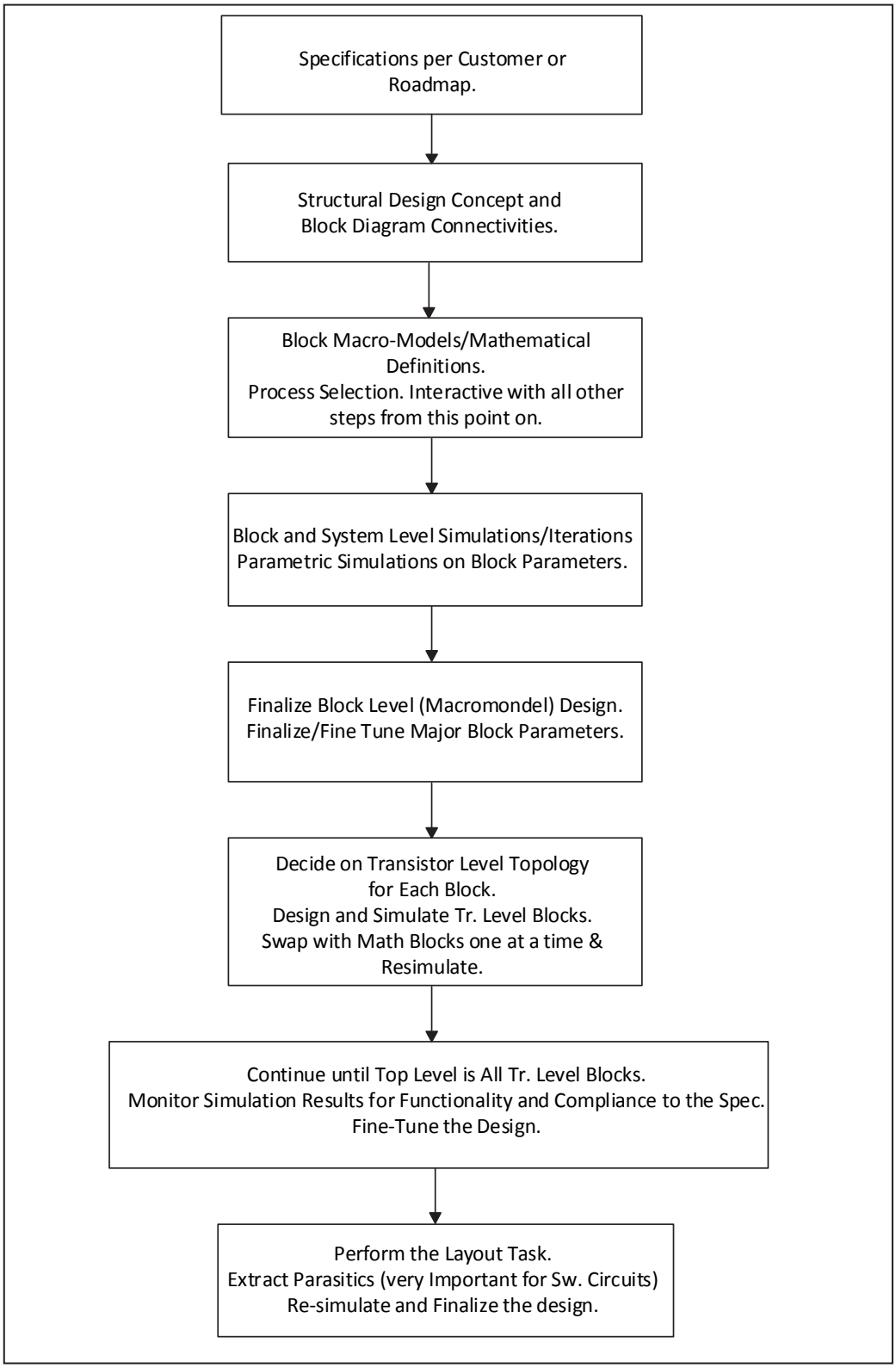

Figure 6-1 – Top-Down Design Flow-Diagram

6.3 Process Technology Considerations

A number of aspects of the process technology must be considered at this stage. The wafer cost, wafer size, and number of layers in the baseline process for a modular process technology are considered first. Most modern processes of today are modular. In a modular processes the designer has the choice of adding different layers to a suggested minimum base layers called the baseline, to obtain a process technology suitable for a particular product line. As an example, a chip with a relatively small digital amount of content may not need a low-voltage (1.8V) transistor kit, for an addition of 5 more mask layers, simply because it will not justify the cost.

Similarly, a designer willing to design a low or medium voltage mixed signal chip with no need for Power MOS-FET transistors will avoid using such devices by sticking to the baseline or CMOS processes option, as opposed to having a more complex and expensive choice of Bipolar-CMOS-DMOS (BCD) process. The cost of the latter process is much higher, especially with the addition of high voltage device kits in the modular process.

The cost per layer, and the total wafer cost differs from foundry to foundry, however a general guideline of an average cost of $20 per layer, with a rough estimate of $100 cost for raw material will place the wafer cost at its minimum of $450 for an 18 layers baseline process (at the time of this writing in 2015).

It is worthwhile to mention that such prices vary across the globe and change very much from one foundry to another. Physical location of the foundry also plays a role here. There are foundries in East Asia that offer some 13 ~ 14 layer processes with almost half of the above prices, suitable for various general purpose IC's.

Metal layers are generally more expensive and costly. They cost about 1.5 ~ 2 times more compared to the other layers. The exception is the thick top metal layer, sometimes called "Analog Metal", if exists in the process or design. Thick top metal is described in this section shortly. Baseline processes, often as a minimum have one poly and 3 metal layers (1P3M).

In reality, due to the complexity of the modern power, or mixed signal chips, some extra layers in particular a second poly layer and few additional metal layers are often added to the baseline process. If there is a need for a particular layer, such as a high-sheet-rho poly resistor layer, or a Metal-Insulator-Metal capacitor (MIM cap), these have to be added to the modular process recipe as well. Such additions could increase the wafer cost by a factor of 30% to 50%, particularly for high voltage or high power integrated circuits.

In a Power Management Integrated Circuit (PMIC) chip, the top most metal layer is often a thick layer of about 3µ (30kA°) as opposed to a normal top metal layer with a thickness of 0.8µ, or a general intermediate metal layer with a thickness of around 0.4µ. The thick (30kA°) metal layers are expensive and unless absolutely needed like the case of power chips, they should be avoided.

Many generic processes of today, as part of their trim kits, have naturally poly or metal fuse links as discussed in section 3.2.2. This is likely in addition to the more advanced and compact digital OTP or MTP kits to handle the required trims. Almost all foundries port some third party's OTP

and MTP kits into their baseline process. In all such cases qualification and 10 years retention (withholding) data are available to the end user. However there is a cost adder associated with the use of the above mentioned Intellectual Properties (IPs) which must be considered in the total cost analysis.

In spite of the existence of such more advanced trim kits, in the case of designs employing Dynamic Offset Cancellation (DOC) techniques of some sort, the use of the older methods such as poly fuse links can still be justified due to following reasons:

i. Due to the nature of a DOC designs, the numbers of required trims are minimal if any. Therefore there is no concern in regards to the relatively larger areas consumed by the poly or metal fuses compared to the more compact digital OTP trims.

ii. As mentioned, OTP and MTP trim kits are often cost adders, especially if they are ported from a third party vendor as an Intellectual Property to the baseline process of the choice. The cost can be based on onetime usage, or application of the IP multiple times within different chips.

For the design associated with the work of this thesis, poly fuses have been used for the above mentioned reasons.

Another consideration besides the sensitive cost analysis is usually the availability of a good device kit within the process. Examples are the existence of a good PNP device (or complementary BJT devices if needed), or the availability of low and high threshold MOS devices. The latter is very useful to make “self-biased” cascode mirrors, or high output impedance output devices. This is then achieved without the need of a separate bias-line for cascode transistors, or giving up on the voltage head-room requirements for such devices. The design associated with this thesis has benefitted from the above in many occasions.

Other very important aspects of the process are reliability and maturity of its Device Kit (PDK) and Models, proven verification tools such as Design Rule Check (DRC), and Layout vs. Schematic (LVS) decks, and Good Design Manual, and Model Validation Reports.

Some “statistical yield charts”, and “defect history”, as well as foundry’s “back-end support” and “Process Control Monitor (PCM)” test kits and records are helpful when available.

Process Control Monitors are a set of different components and devices tailored to be placed on every single wafer for a specific technology node within the foundry, regardless of the type of design or the customer. These are foundry monitor kits to make sure the process is under control. In the old days, the PCM kits were placed at 5 locations within the chip, that is top, center, bottom, left and right.

Nowadays many foundries have adapted to the insertion of their monitory kits within the scribe lines on the wafers in order to save area for the die itself.

6.4 Top-Down Model-Based Design of the Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifier

Figure 6-3 shows the top-level block diagram and connectivity of the design associated with this thesis. The design has already been described in detail throughout chapter 5. The task of the model based design is to facilitate the determination of the values of the major parameters within each block, in addition to identify the values of the compensation network, and integrator's capacitors.

To achieve this goal, we will follow the guide-lines and steps of a top-down design presented in figure 6-1. We'll rely on some hand calculations for major required parameters, but will follow up with relevant simulation tools to complete the task.

We start with the simplest model possible for each block. This means just identifying the main parameters in the model. For each transconductance block in figure 6-3, we specify only the transconductance parameter (G_m) itself, the input impedance (R_i), the output impedance (R_o), and finally the output capacitances. This is satisfactory for the purpose of a top-down model-based design. A general behavioral model for most transconductances shown in figure 6-3 is presented in figure 6-2. Unless specified otherwise, all the transconductance blocks in the model-based design of figure 6-3 have a similar definition.

As can be seen, the general behavioral model is a differential-in, differential-out model with only the major parameters identified. The inclusion of the output impedance and output capacitances in a differential form are not absolutely required, however such additions are desirable for two reasons:

i. They bring to the model the flexibility of representing the physical device and layout parasitics, as well as their mismatches when their single ended values are selected differently.

ii. The model for the transconductance uses a voltage-controlled current source as the current generator with a current value proportional to the input voltage of the G_m block. From a simulation point of view, it is often beneficial to have an output impedance path in parallel with such current sources. Ideal current sources are known to be responsible for many non-convergence issues in SPICE.

Later on, when all such blocks are macro-modeled, and the feedback loops are connected together as shown in figure 6-3 , we will start fine-tuning these parameters one at the time. This is achieved by means of parametric simulations to obtain the optimal points with the best system performance, primarily for the lowest offset and spikes at the input, and the minimum gain-error ($\varepsilon_{\text{gain}}$) characteristic possible.

After we're satisfied with the values selected for the major parameters, we can introduce parasitics, and imbalances at sensitive locations such as input and output of the choppers or transconductance blocks.

For the sake of compactness, not every detail of such calculations or simulations is given, but the end results will be presented as necessary.

It should be noted that for this design, the gain-error is not reduced by any dynamic corrections, but through a post package trimming method similar to the general approaches discussed in section 3.2.2. Besides the gain, some other parameters such as oscillator frequency, supply current, and obviously band-gap voltage reference are also PPT (see section 3.2.2) trimmed as well.

More specific details about the techniques to implement a good gain trim methodology with practical design examples are discussed in this chapter.

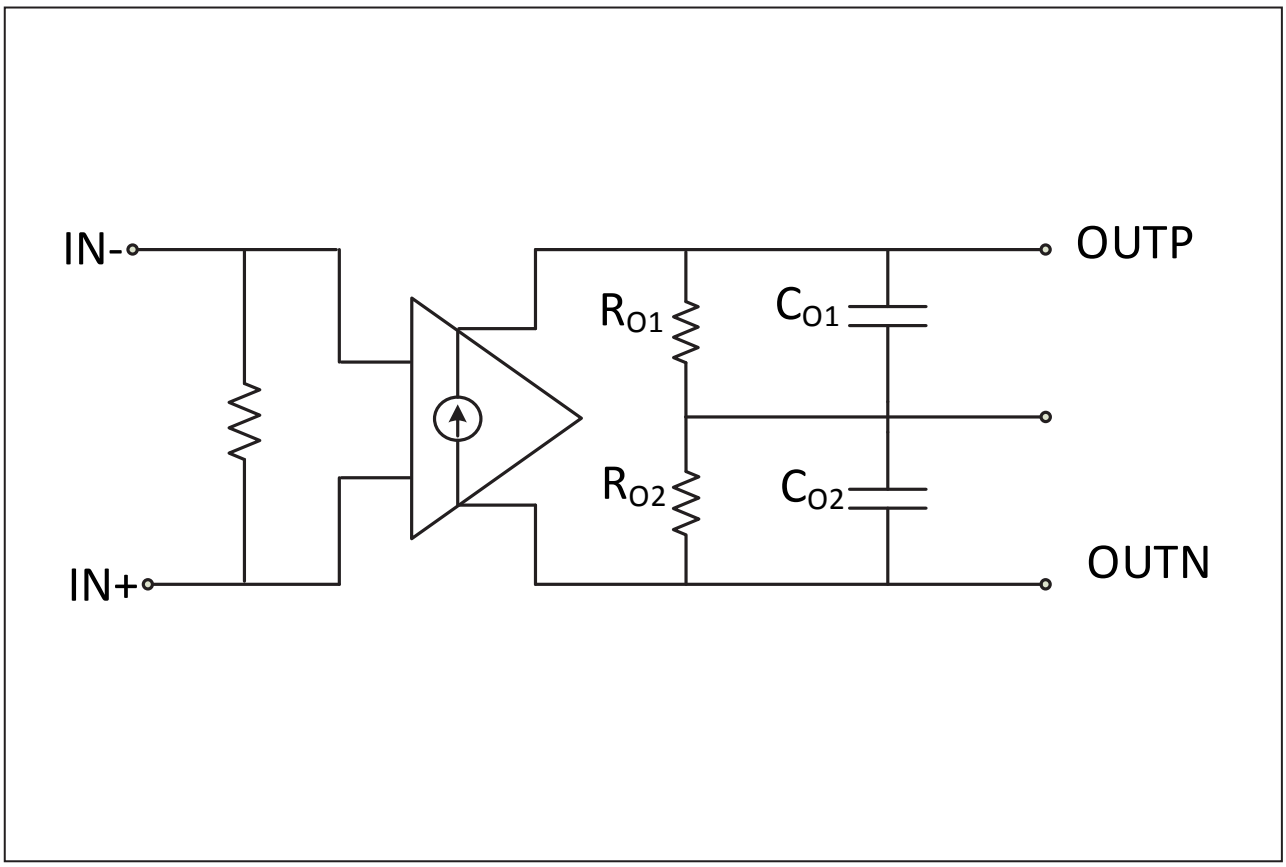

Figure 6-2 – The Schematic Describing the Behavioral Model of a Transconductance Block

Any design starts with a set of desired specifications. The top-down design flow-diagram of figure 6-1is no exception. The following table is part of an intended target specification for this design. The complete set of the specification is usually available in the Data-Sheet of a Product, often under the name of “Electrical Characteristics Table” or EC-Table for short.

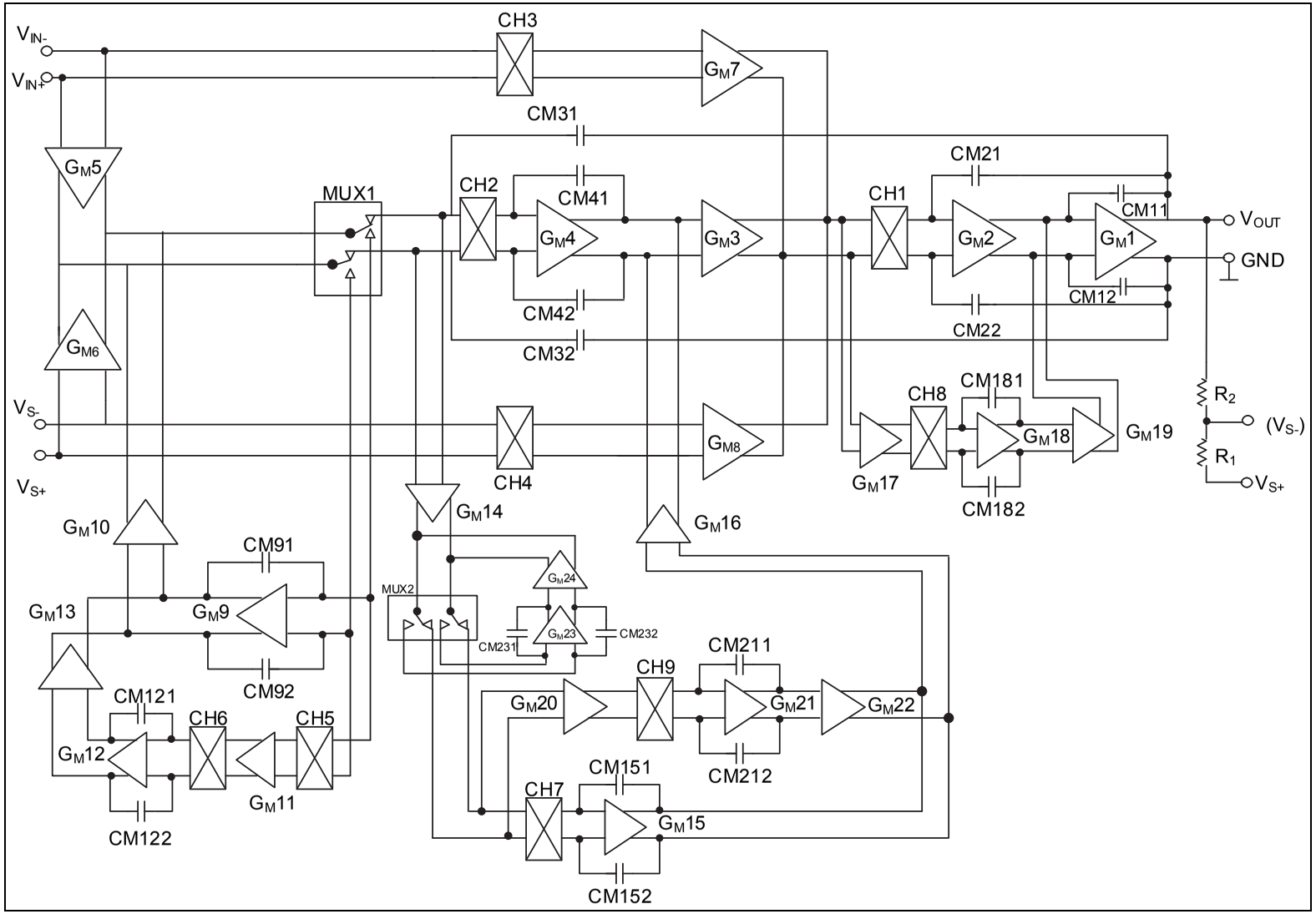

Figure 6-3 – Top-Level Block-Diagram of the Proposed Architecture for the Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifier

6.4.1 General Specifications of the CFIA design

A preliminary specification for the design associated with this thesis is presented in Table 6-1.However in this particular model-based design, the focus during this stage of the design is only on the main characteristic of the precision instrumentation amplifier, i.e., the input-referred offset. All the other parameters must be validated at the time of transistor level design. This is mainly due to the fact that the macro-model definitions of the components in the model-based design are chosen to be very simple, with a focus on the offset cancellation aspects of the design only.
Later on, at the transistor-level design, other specifications are taken into considerations.

V_{DD} = 5V, V_{SS} = 0, V_{CM} = V_{DD}/2, R_L = 100kΩ, C_L=100pF, V_{indif} = V_{in+} - V_{in-}, T_A = 25°C

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	Inferred From PSRR Test		2.85	5	5.5	V
Supply Current	I_{DD}	V_{indif} = V_{in+} - V_{in-} = 0			0.75	1.30	mA
Input Offset Voltage	V_{os}	V_{indif} = V_{in+} - V_{in-} = 0			+/-1	+/-20	µV
Gain Nonlinearity	GNL	Best Straight Line, G=100			10	50	ppm
Gain Error	ε_{gain}	-100mV ≤ V_{indif} ≤ 100mV Gain = 1			0.01	0.05	%FSR
Input Common-Mode Range	V_{CM}	Inferred From CMRR Test		-0.1		V_{DD}-1.3	V
Common-Mode Rej. Ratio	CMRR	-0.1V ≤ V_{CM} ≤ V_{DD}-1.3V		106	135		dB
Power-Supply Rej. Ratio	PSRR	V_{DD}=2.85 to V_{DD}=5		120	140		dB
Output Voltage Swing	V_{OH}	V_{DD} - V_{OUT}	R_L = 100k		25	50	mV
			R_L = 10k		50	100	
			R_L = 1k		250	400	
	V_{OL}	V_{OUT} – V_{SS}	R_L = 100k		25	50	
			R_L = 10k		50	100	
			R_L = 1k		250	400	
Input Voltage Noise Thermal Noise	E_n	f = 0.1Hz to 10Hz			2.5		μV_{p-p}
		f = 1kHz			30		nV/√Hz
Gain-Band-width	GBW				750		kHz
Slew Rate	SR	Gain = 1			0.1		V/µs
Short Circuit Current	I_{SC}	Sink or Source			25		mA

Table 6-1 – Target Design Specifications or Electrical Characteristics Table (EC Table)

Although the above EC table is for room temperature; the project is designed and validated for a temperature range from -40°C to 125°C. The extended temperature range has a different EC table with a slightly relaxed specification.

Systematic amplifier design always starts with the design of the output stage and compensation network, followed by the design of the intermediate and input stages. For this reason, in the next subsection, we first start with the model-based design of the output stage, together with its frequency compensation network.

6.4.2 Model-Based Design of the Output Stage and Frequency Compensation Network

The output stage of an amplifier must be able to drive a load, often a combination of a resistor and a capacitor in parallel. The design process of the output stage is primarily about choosing a transconductance capable of adequately driving the load, and meeting the frequency response criterion.

According to top-level block-diagram of figure 6-3, we are dealing with a three stage amplifier. The first stage of the amplifier consisting of G_{m_7}, G_{m_8}, and the nested Miller Capacitors $C_{m_{21}}$, and $C_{m_{22}}$ set the band-width or the unity gain frequency f_0 . The combination of G_{m_2} / G_{m_1}, along with capacitors $C_{m_{21}}$, and $C_{m_{22}}$, can be considered as an integrator following the first stage. The output current of the first stage $I_{o_7} = G_{m_7} V_{in}$ builds the output voltage across the above capacitors. The voltage gain from the output to the input of the amplifier is then:

$$\frac{V_{out}}{V_{in}} = \frac{G_{m_7}}{2\,\pi\, f\, C_{m_{21}}} \approx \frac{G_{m_7}}{6\, f\, C_{m_{21}}} \qquad \textbf{(6.1)}$$

For a unity gain, the frequency f_0 is:

$$f_0 = \frac{G_{m_7}}{2\,\pi\, C_{m_{21}}} \approx \frac{G_{m_7}}{6\, C_{m_{21}}} \qquad \textbf{(6.2)}$$

The second stage with G_{m_2} and Miller capacitors $C_{m_{11}}$ and $C_{m_{12}}$ impose a limiting pole f_{02} to the right of the unity gain frequency (f_0), which for the purpose of achieving a better than 60° phase-margin, must be set at least twice the unity gain frequency.

$$f_{02} = \frac{G_{m_2}}{2\,\pi\, C_{m_{11}}} \approx \frac{G_{m_2}}{6\, C_{m_{11}}} = 2\, f_0 \qquad \textbf{(6.3)}$$

The third stage or final output stage G_{m_1} along with the output capacitive load C_L must have a limiting pole frequency f_{01} which is twice the first limiting pole; that is twice f_{02}.

$$f_{01} = \frac{G_{m_1}}{2\,\pi\,C_L} \approx \frac{G_{m_1}}{6\,C_L} = 2f_{02} = 4f_0 \qquad \textbf{(6.4)}$$

$$G_{m_1} = 6\ f_{01}\,C_L = 24\,f_0\,C_L \qquad \textbf{(6.5)}$$

Assuming a bandwidth of $BW = f_0 = 1$ MHz > 750 kHz, and using Eq. (6.2) we get:

$$f_{01} = 4\text{MHz}$$

$$f_{02} = 2\text{MHz}$$

With a load capacitor of C_L = 100pF, the transconductance of the output stage G_{m_1} is calculated from Eq. (6.5) to be:

$$G_{m_1} = 2.4\ \text{mA/V} = \frac{1}{416}\ \text{A/V}$$

Working backwards towards the input, as mentioned, f_{02} needs to be 2 MHz for a 60° phase margin. With selected Miller capacitors of $Cm_{11} = Cm_{12} = 7$pF, and using Eq. (6.3) we obtain:

$$G_{m_2} = 83\mu\text{A/V} = \frac{1}{12\text{k}\Omega}$$

A word of caution is in order here. The designer should be aware that later on and at transistor-level design, care must be taken that other criteria for complying with a proper output stage design be considered. These criteria include aspects such as the drive capability of the output, which translates into having enough of the width for a carefully selected length of the output stage transistors. This is explained shortly.

Another important aspect of the output stage is the distance or head-room of the output to either of the V_{DD} or V_{SS} rails during output voltage swings. These are called V_{OH} and $V_{OL,}$ which are the headroom values to V_{DD} and V_{SS} respectively. The specifications should be met without the output devices enter into their Ohmic region of operations, that is the linear region for a MOS device, or the saturation region for its bipolar counterpart.

Care must be taken in selection of the minimum length for the output device; or else they will likely get damaged after an ESD stress test at the factory, or an ESD event later on during the life of the product. A sufficient length, as well as a sufficient width (W) must both be considered early on to assure the reliability of the device. This consideration is important both at the time of process technology selection, as well as during the transistor-level design phase.

In some output stages and power IC designs, it is not unusual to see that an output pad within the chip does not have an ESD clamp because the output transistors are large enough to withstand the ESD stress.

The location of the pads (or any pad for the sake of discussion) in the layout, and the distance to the main V_{SS} or GND pad is of prime importance for the pin to meet the ESD requirements.

The above is often translated into a total resistance of the bus between the pad and the VSS or GND, which is often mandated to be less than 2 ohms. In the past the JEDEC standard required a 2kV Human Body Model (HBM) ratings, but nowadays with the ever shrinking technology nodes, and the reduced operating voltages, a 1kV HBM is often accepted by the standards (JEDEC or Internal Company Specifications), in addition to some end users. Since the ESD ratings for all the pins are often specified in the datasheets, such exceptions are clear to the end users.

6.4.3 Model-Based Design of the Input Stage Transconductances, and their First-Level Offset Cancellation loop

The transconductances $G_{m_7} = G_{m_8}$ are calculated from Eq. (6.2), assuming a selected $Cm_{21} = Cm_{22} = 14\text{pF}$, and a known bandwidth of $f_0 = 1\text{MHz}$. This yields to:

$$G_{m_7} = G_{m_8} = 83.3\ \frac{\mu A}{V} = \frac{1}{12k\Omega}$$

With a10mV offset, the output currents of $G_{m_7}$and $G_{m_8}$are going to be 0.833µA.

This 10mV offset of the input transconductances appears as a square-wave (block-wave) at the inputs of $G_{m_5}$and G_{m_6} in a closed loop configuration. The transconductances $G_{m_5}$and G_{m_6} are chosen to be weaker than the main input transconductances G_{m_7} and G_{m_8}. This helps to reduce the ripple of the error-compensating voltages across the capacitors $C_{m_{41}} = C_{m_{42}}$. The correction voltage will gradually build up through several clock cycles of the chopper frequency. The error-compensating charge per chopper clock cycle $Q_{C_{m_{41(per\ cycle)}}}$ is shown in Eq. (6.6).

$$Q_{C_{m_{41(per\ cycle)}}} = \frac{1}{2}\ G_{m_6}\ V_{os_{(7+8)}} T_{ch} \qquad \textbf{(6.6)}$$

The factor of $\frac{1}{2}$ is due to the existence of MUX_1 as explained in 5.4.2.1.

From Eq. (6.6), with a chopper clock frequency of 10 kHz, if the $G_{m_5}$and G_{m_6} are chosen to be $\frac{1}{1.2\text{M}\Omega}$, the total charge per integrator G_{m_4} capacitor, per clock cycle, for a $V_{os_{(7+8)}}$of 10mV is half of a Pico Coulomb. The voltage step per clock cycle for $C_{m_{41}} = C_{m_{42}}$ is given by:

$$V_{step_{C_{m_{41}}}} = \frac{Q_{C_{m_{41(per\ cycle)}}}}{C_{m41}} = \frac{\frac{1}{2}G_{m_6}V_{os_{(7+8)}}T_{ch}}{C_{m41}} \qquad \textbf{(6.7)}$$

With a 0.42 pC charge per chopper cycle as shown above, and if capacitors $C_{m_{41}} = C_{m_{42}}$ are chosen to be 30pF each, the amount of $V_{step_{Cm_{41}}} = V_{step_{Cm_{42}}}$ is about ≈ 14mV.

The number of clock cycles (*N*) required for $Cm_{41}$and Cm_{42} to reach a final voltage per capacitor is determined from Eq. (6.8).

$$N = \frac{V_{final_{C_{m_{41}}}}}{V_{step_{C_{m_{41}}}}} \qquad \textbf{(6.8)}$$

For a 0.7V final voltage across each capacitor, the number of chopper clock cycles is 50.
This means the main compensation loop reduces the square-wave and triangle ripple by a factor of 50.

Continuing this approach to determine the weak transconductanceG_{m_3} we arrive at Eq. (6.9).

$$G_{m_3} = \frac{G_{m_7}V_{os_{(7+8)}}}{V_{final_{C_{m_{41-42}}}}} \qquad \textbf{(6.9)}$$

Where $V_{final_{C_{m_{41-42}}}}$ is the differential output voltage at the output of the integrator G_{m_4}.

With $a\ G_{m_7} = \frac{1}{12\text{k}\Omega}$, $V_{os_{(7+8)}} = 10\text{mV}$, and $V_{final_{C_{m_{41-42}}}} = 1\text{V}$, we obtain:

$$G_{m_3} = \frac{1}{1.2\text{M}\Omega}$$

The value of $G_{m_4}$is not of any significance as long as the gain of the integrator is sufficiently large. We select the values , with a large gain of A_4 = 10,000.

$$G_{m_4} = \frac{1}{50\text{k}\Omega}$$

$$A_4 = 10{,}000$$

For a lot of other transconductances in this design, the voltage gains and output impedances are assigned very high initial values. Unless otherwise specified, the gain is assumed 10,000, and the output impedance is given a value in the range of 100MΩ, or in some cases several GΩ. This is to ensure that the performance evaluation at the beginning is not affected by any gain deficiency, or loading effects. Later on these values are altered as needed.

Even though the design is still at the model-based stage, all the choppers and the two MUX switches are chosen to be transistor-level designs for the following reasons:

i. Ideal switches are more likely to give the designer SPICE non-convergence problems, often due to the lack of a DC path to ground.

ii. The simulation time is much faster when choppers and MUXs are all real-world transistor-level designs.

iii. The transistor-level design of a switch accounts for some parasitics, which can later on be altered for the purpose of parasitic mismatch analysis. This is true even at this model-based stage of the design.

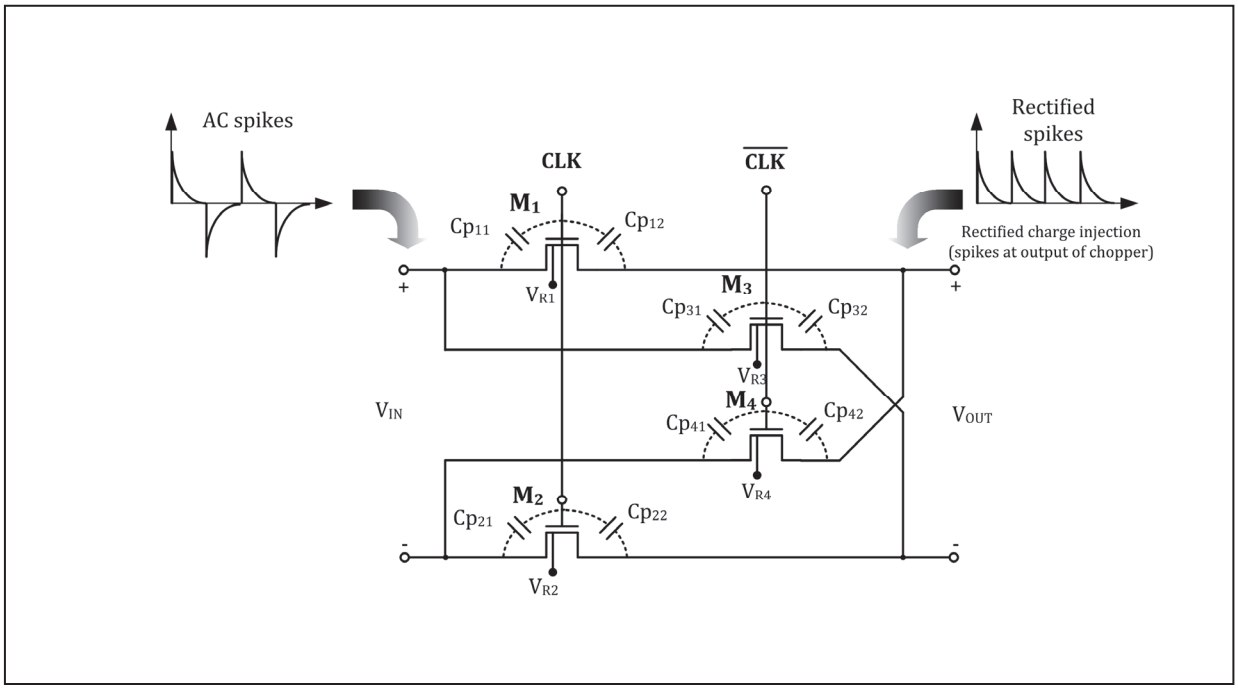

Figure 6-4 – Transistor-Level Schematic of a Chopper

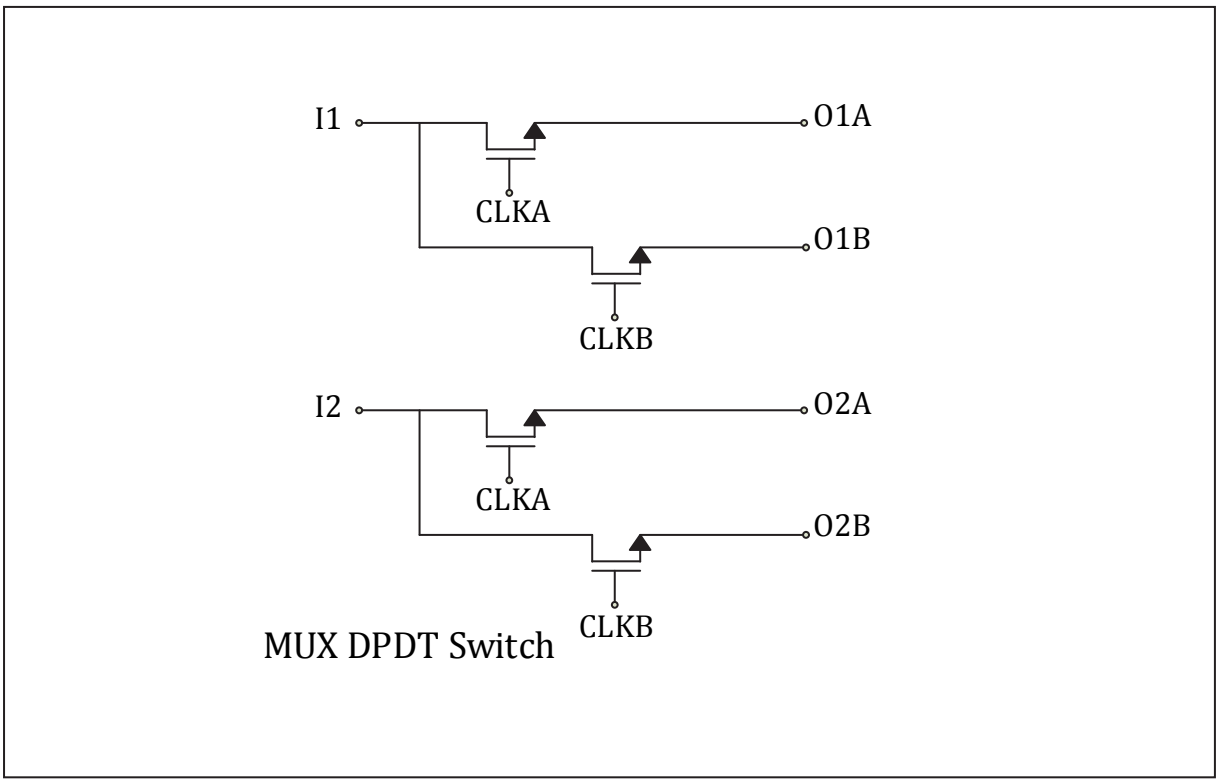

Figure 6-5 – Transistor-Level Schematic of a MUX

The values of $C_{m_{31}}$ and $C_{m_{32}}$ can be obtained from Eq. (5.24) for known values of Cm_{21} , G_{m_5}, and G_{m_7}. However due to existence of MUX_1 one needs to multiply the value of G_{m_5} in the formula by (1/2) as practically its strength is halved by the existence of the MUX_1 switch.

$$C_{m_{31}} = C_{m_{32}} = \frac{0.5\, G_{m_5}\, C_{m_{21}}}{G_{m_7}} = 0.07\text{pF} \qquad \textbf{(6.10)}$$

It is important to note that these initially "calculated" or "selected" values for parameters and components must be verified thoroughly through simulation tools. During this process, most of these values, if not all, are altered, and optimized for a better performance of the model-based design. Eventually all these parameters are finalized by the simulation tools at the transistor-level design as previously discussed.

6.4.4 Model-Based Design of Higher-Level Offset Cancellation Loops

Similar approaches as discussed in section 6.4.3 are used to obtain the values of other components in the model-based design.

$G_{m_{16}}$ is a weak transconductance within the second-level cancellation loop for removing the offset of the integrator G_{m_4}. Its value is calculated from :

$$G_{m_{16}} = \frac{G_{m_4} V_{os_4}}{V_{final_{C_{m_{152}}}}} \qquad \textbf{(6.11)}$$

With $G_{m_4} = \frac{1}{50\text{k}\Omega}$, $V_{os_4} = 10\text{mV}$, and a final voltage of 1V across the capacitors$Cm_{152} = Cm_{153}$, the calculated value for $G_{m_{16}}$ is $\frac{1}{5M\Omega}$.

For the sense amplifier$G_{m_{14}}$, the following holds true:

$$G_{m_{14}} = \frac{C_{m_{232}}\ V_{final_{C_{m_{232}}}}}{N\ T_{ch}\ V_{os_{14}}} \qquad \textbf{(6.12)}$$

Cm_{232} is the value of the Auto-Zeroing capacitor within the integrator $G_{m_{23}}$ as part of the second-level offset cancelation loop to remove the offset of $G_{m_{14}}$. Its final voltage after N cycle of chopper clock is $V_{final_{C_{m_{232}}}}$.

For a 10mV offset of $G_{m_{14}}$, a $V_{final_{C_{m_{232}}}}$ of 1V after 30 cycles of chopper clock, and a 5pF capacitor for the Auto-Zeroing capacitors $Cm_{231} = Cm_{232}$ we obtain from (6.12):

$$G_{m_{14}} = \frac{1}{6\text{M}\Omega}$$

Similarly:

$$G_{m_{10}} = \frac{V_{os_{56}} G_{m_6}}{V_{final_{C_{m_{91}}}}} \qquad \textbf{(6.13)}$$

Where $V_{os_{56}}$ is the combined offsets of G_{m_5} and G_{m_6}, and $V_{final_{C_{m_{91}}}}$ is the final voltage across capacitors $C_{m_{91}} = C_{m_{92}}$; which is assumed to be 1V for some 30 cycles of the chopper clock, as has been the assumption in many other calculations. This gives:

$$G_{m_{10}} = \frac{1}{100\text{M}\Omega}$$

The values of$C_{m_{91}}$and $C_{m_{92}}$ could be some few pF, here we set the values to be 5pF each.

The transconductance value of the integrator G_{m_9}, similar to other integrators within this design, is not critical, however all such integrators must have a high gain, here set to A=10,000.
We select $G_{m_9} = \frac{1}{50\text{k}\Omega}$ for its initial value prior to performing model-based simulations.

We pick the sense amplifier $G_{m_{11}}$ to have the same value as $G_{m_{14}}$. Also we make the weak transconductance $G_{m_{13}}$ to be equal to $G_{m_{16}}$. This yields:

$$G_{m_{11}} = G_{m_{14}} = \frac{1}{6\text{M}\Omega}$$

$$G_{m_{13}} = G_{m_{16}} = \frac{1}{5\text{M}\Omega}$$

The approach to estimate the values of other parameters and component of the model-based design of figure 6-3 follows the same path.

Table 6-2 summarizes the initial estimations for all the transconductances within the model-based design of the Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifier of figure 6-3. These values will be used in the model-based simulation as the starting-point, and will be altered as needed to improve the performance.

Since this model-based design is primarily developed to validate the work of this thesis, other accuracy errors such as gain-error or linearity-error are not included in this model-based design. However a gain-error PPT trim based on the technique discussed in section 3.2.2 is implemented at the transistor-level design, as can be seen in section 6.5.5.4.

Parameter	Value	Unit	Description
G_{m_1}	$\frac{1}{416}$	A/V	Output Stage Transconductance
G_{m_2}	$\frac{1}{12\text{k}}$	A/V	Transconductance of the Output Driver
G_{m_3}	$\frac{1}{1.2\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of G_{m_7} and G_{m_8}
G_{m_4}	$\frac{1}{50\text{k}}$	A/V	Integrator G_m for removal of the offset of G_{m_7} and G_{m_8}
G_{m_5}	$\frac{1}{0.6\text{M}}$	A/V	Balancing Sense Amplifier to sense the offset of G_{m_7} and G_{m_8}
G_{m_6}	$\frac{1}{0.6\text{M}}$	A/V	Sense Amplifier to sense the offset of $G_{m_{7/8}}$
G_{m_7}	$\frac{1}{12\text{k}}$	A/V	Input Transconductance
G_{m_8}	$\frac{1}{12\text{k}}$	A/V	Feedback Transconductance
G_{m_9}	$\frac{1}{50\text{k}}$	A/V	Integrator G_m for removal of the offset of $G_{m_{5/6}}$
$G_{m_{10}}$	$\frac{1}{100\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of $G_{m_{5/6}}$
$G_{m_{11}}$	$\frac{1}{6\text{M}}$	A/V	Sense Amplifier to sense the offset of $G_{m_{7/8}}$
$G_{m_{12}}$	$\frac{1}{25\text{k}}$	A/V	Integrator $G_{m_{12}}$ for removal of the offset of G_{m_9}

$G_{m_{13}}$	$\frac{1}{5\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of G_{m_9}
$G_{m_{14}}$	$\frac{1}{6\text{M}}$	A/V	Sense Amplifier to sense the offset of $G_{m_{14}}$
$G_{m_{15}}$	$\frac{1}{25}$	A/V	Integrator G_m for removal of the offset of G_{m_4}
$G_{m_{16}}$	$\frac{1}{5\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of G_{m_4}
$G_{m_{17}}$	$\frac{1}{5\text{M}}$	A/V	Sense Amplifier to sense the offset of G_{m_2}
$G_{m_{18}}$	$\frac{1}{25\text{k}}$	A/V	Integrator G_m for removal of the offset of $G_{m_{18}}$
$G_{m_{19}}$	$\frac{1}{1.7\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of G_{m_2}
$G_{m_{20}}$	$\frac{1}{500\text{M}}$	A/V	Sense Amplifier to sense the offset of $G_{m_{15}}$
$G_{m_{21}}$	$\frac{1}{25\text{k}}$	A/V	Integrator G_m for removal of the offset of $G_{m_{15}}$
$G_{m_{22}}$	$\frac{1}{2.6\text{M}}$	A/V	Weak Transconductance of the loop ending at the output of $G_{m_{15}}$
$G_{m_{23}}$	$\frac{1}{25\text{k}}$	A/V	Auto-Zeroing Integrator G_m for removal of the offset of $G_{m_{14}}$
$G_{m_{24}}$	$\frac{1}{500\text{M}}$	A/V	Auto-Zeroing Weak Transconductance of at the output of $G_{m_{23}}$

Table 6-2 – Initial estimations of the transconductances of the model-based design of figure 6-3

Parameter	Value	Unit	Description
C_L	100	pF	Load Capacitor
Cm_{11}	7	pF	Miller Capacitor
Cm_{12}	7	pF	Miller Capacitor
Cm_{21}	14	pF	Nested Miller Capacitor
Cm_{22}	14	pF	Nested Miller Capacitor
Cm_{31}	0.07	pF	Multipath Nested Miller Capacitor
Cm_{32}	0.07	pF	Multipath Nested Miller Capacitor
Cm_{41}	30	pF	Integrator Gm_4 / Hybrid Miller Capacitor
Cm_{42}	30	pF	Integrator Gm_4 / Hybrid Miller Capacitor
Cm_{91}	5	pF	Integrator Gm_9 Capacitor
Cm_{92}	5	pF	Integrator Gm_9 Capacitor
Cm_{121}	5	pF	Integrator Gm_{12} Capacitor
Cm_{122}	5	pF	Integrator Gm_{12} Capacitor
Cm_{151}	5	pF	Integrator Gm_{15} Capacitor
Cm_{152}	5	pF	Integrator Gm_{15} Capacitor
Cm_{181}	5	pF	Integrator Gm_{18} Capacitor
Cm_{182}	5	pF	Integrator Gm_{18} Capacitor
Cm_{211}	5	pF	Integrator Gm_{21} Capacitor
Cm_{212}	5	pF	Integrator Gm_{21} Capacitor
Cm_{231}	10	pF	Auto-Zeroing Integrator Gm_{23} Capacitor
Cm_{232}	10	pF	Auto-Zeroing Integrator Gm_{23} Capacitor

Table 6-3 – Initial Capacitor Values for the Block-Diagram of the Model-Based Design of figure 6-3

Parameter	Value	Unit	Description
R_L	1,10,100	kΩ	Load Resistor Values from heavy to light Load
R_2	Short	N/A	Closed-Loop Gain = 1
R_1	Open	N/A	
R_2	9	kΩ	Closed-Loop Gain = 10
R_1	1	kΩ	
R_2	99	kΩ	Closed-Loop Gain = 100
R_1	1	kΩ	
R_2	999	kΩ	Closed-Loop Gain = 1000
R_1	1	kΩ	

Table 6-4 – Load Resistor and Initial Gain Setting Resistor Values for the Block-Diagram of the Model-Based Design of figure 6-3

6.4.5 Simulation Results for the Model-Based Design of CFIA

The simulation of the top-down model-based design of figure 6-3 was performed using the initial values for parameters and components suggested by Table 6-2, Table 6-3, and Table 6-4.
With the exception of the choppers and MUX switches, which are transistor-level based, all the other components are simple model-based blocks.

Figure 6-6 shows the transient simulation result for the model-based top-down design of figure 6-3, when configured as a unity gain instrumentation amplifier with a combined R_L / C_L load of 1kΩ / 100pF. All the blocks used within the model are assigned an offset of 10mV.

Since the gain is set to unity, the differential output voltage, that is V(out) – V(ref) is in fact equal to the differential input voltage of the amplifier. Any offset seen at the differential output can be considered as the input-referred offset.

The result shown in figure 6-6 is quite close to expectations. The amplifier starts off with a large offset, and dynamically removes the offset in a gradual manner until it reaches its residual offset (ripple), here equal to zero. This is expected since we're dealing with ideal models for the blocks, and not real components with their associated non-idealities.

The spikes however are not zero (+40μV / -50 μ V) due to the existence of the real chopper and MUX switches, as opposed to ideal ones. Some of these switches have parasitic capacitances at their terminals, which are set slightly off-balance to observe such real-world effects in advance.
A close-up view of the above input-referred ripple and spikes are shown in figure 6-7.

At half way through the design, we summarize our results of the model-based simulations in Table 6-5. Later on when the transistor-level design and simulation results are available, we'll revisit both the graph of figure 6-6, as well as the Table 6-5 for the purpose of comparison.

Simulation Results	Design Approach	Intentional Vos	Gain	RL/CL
$V_{rip_{in_{pp}}} = +/-15\mu V$ $V_{spikes} = +20\mu V \ / -140\mu V$	Model-Based	10mV for All G_m's	10	1kΩ/100pF

Table 6-5 – Table of Simulation Results for the Model-Based Design of figure 6-3

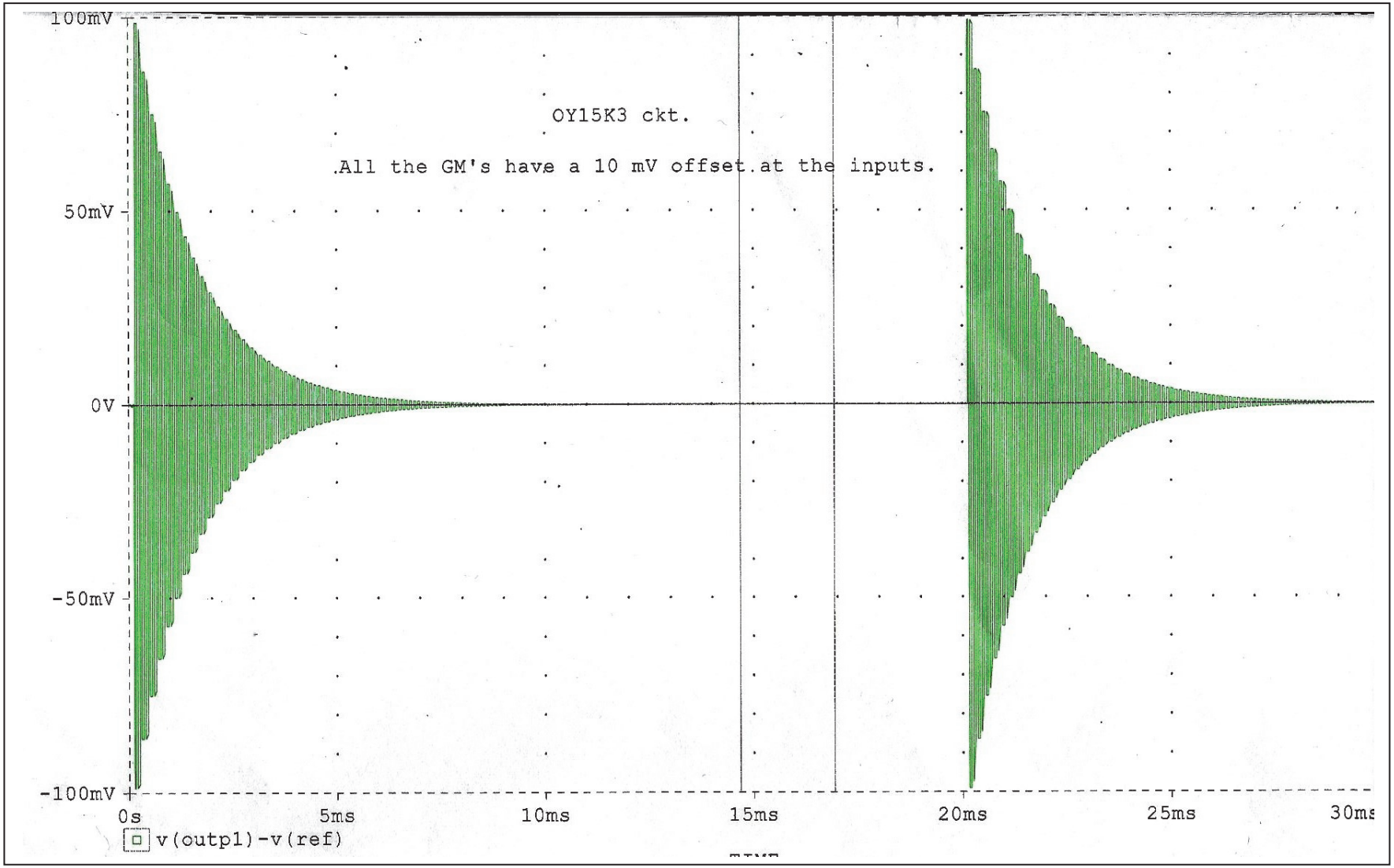

Figure 6-6 – An informative Picture Showing the Simulation Results of the Model-Based Design Presented in figure 6-3.

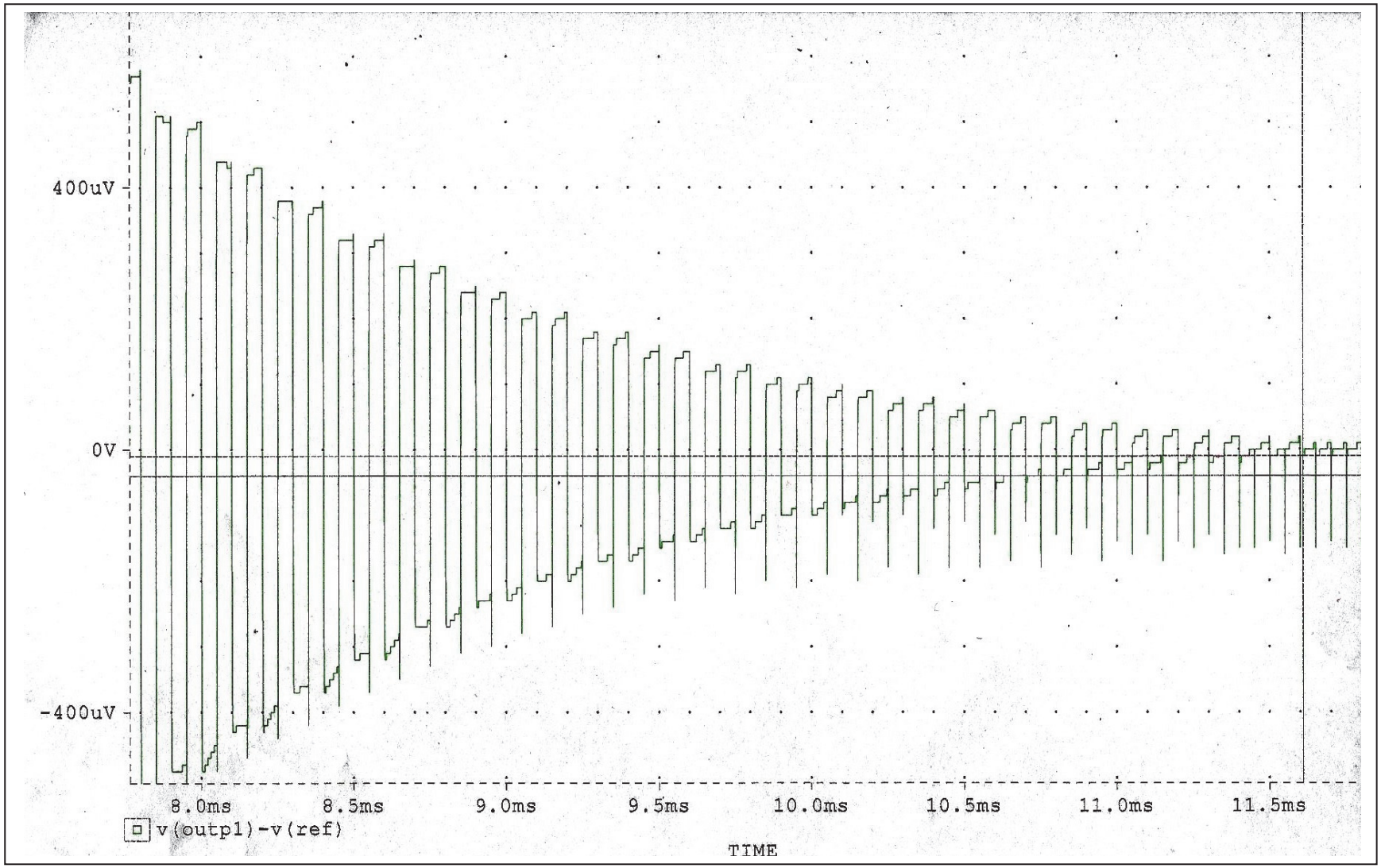

Figure 6-7 – A Close-UP View of the Input-Referred Ripple and Spikes of the Model-Based Graph of figure 6-6

6.5 Transistor-Level Design of the CFIA in CMOS Technology

Transistor-level design of this thesis is performed in a CMOS 0.6µ technology node. In order to achieve a predicted design, the designer must know the main parameter's specifications for the process in use, besides the knowledge about the design. It is assumed that other critical aspects such as cost, reliability, wafer capacity, delivery, and support history have already been considered.

6.5.1 Basic Process Parametric Specifications

Some specifications for the basic parameters of the above CMOS process are listed here:

Parameter	Value	Unit
μ_n	475	$cm^2/V\ s$
μ_p	225	$cm^2/V\ s$
$\mu_n\ C_{OX}$	118	$\mu A/V^2$
$\mu_p\ C_{OX}$	56	$\mu A/V^2$
$\frac{\mu_n\ C_{OX}}{\mu_p\ C_{OX}}$	2.1	-
V_{t_n}	650	mV
V_{t_p}	750	mV
C_{OX}	2.5	$fF/\mu m^2$
t_{OX}	140	A°
$L_{min\ Hot\ Carrier}$ *(NMOS)* $V_{DD} = 5.5V$	2.6	µm
n	≈1.8	-
4λ	0.6	µm

Table 6-6 – Table of the Main Process Specifications

These parameters are mainly used as guidelines for hand analysis and calculations, even though their applicability may not explicitly be shown throughout the design.

Of prime importance is the dimensionless process parameter " $\boldsymbol{n}$ " in Table 6-6.This parameter is often used to determine the values of transconductances operating in the weak-inversion according to the Eq. (2.11) presented in section 2.3.2.

It is also worthwhile to mention that this design is a lambda (λ) based design with $4\lambda = 0.6\mu m$. This means that all the widths and the lengths of all the components within all the schematics have a unit of the scale factor $\lambda = 0.15$ μm. Moreover, the minimum allowable dimension is 4 λ, or 0.6 μm.

6.5.2 Transistor-Level Design of Output stage G_{m1} and the Frequency Compensation Network in CMOS Technology

The most logical choice for a transistor-level output stage to replace G_{m_1} in the model-based design of section 6.4.2 is a class AB push-pull design as shown in figure 6-8.

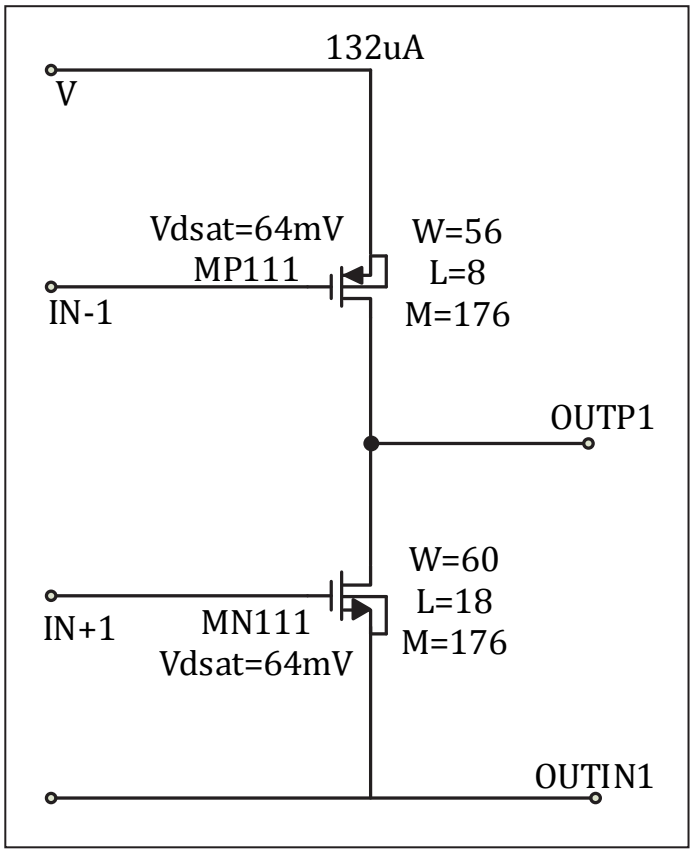

Figure 6-8 – Push-pull Output Stage to replace G_{m_1} block in top-level model-based block-diagram of figure 6-3

The expectation is that the output devices will work at, or in the vicinity of Weak Inversion (WI) due to its large device sizes, and relatively small V_{OH} and V_{OL} requirements.

When a very large device is operating in WI, the transconductance parameter is not a strong function of the W/L, and is almost independent of this aspect ratio as Eq. (2.11) of section 2.3.2 suggests. In contrast, the same parameter is directly proportional to the square-root of the aspect ratio for a device operating in Strong Inversion (SI).

Using $g_m = \frac{I_D}{n \cdot V_{th}}$ of the WI case, with the known values of $G_{m1} = 2.4$ mA/V from section 6.4.2 and Table 6-2, $n = 1.8$, $V_{th} = 26\text{mV}$, the drain current is estimated to be at least 112µA.

At this point we calculate the minimum aspect ratio required for the known $G_{m1} = 2.4$ mA/V, $\mu_n C_{ox} = 118$ µA/V^2, and $I_D = 112$ µA, but using $g_m = 2\sqrt{\mu \frac{C_{ox}}{2} \frac{W}{L} I_D}$ in the SI region. This will give a $\frac{W}{L} = 220$ as the minimum aspect ratio to meet the transconductance and drain current requirements of the design. In order to stay in subthreshold, we must select the $\frac{W}{L}$ much higher than the above calculated value.

In practice, and as can be seen in figure 6-8, the aspect ratio could be a factor of 2 or more higher than what is predicted by the equation $g_m = 2\sqrt{\mu \frac{C_{ox}}{2} \frac{W}{L} I_D}$ in SI region. The reason is to make sure that the output devices are in deep subthreshold, with a saturation voltage (V_{dsat}) well below the V_{OH} and V_{OL} requirements of Table 6-1.

With a choice of $L_{min(NMOS)} = 2.7$ µm (which is higher than the 2.6 µm recommended in Table 6-6), and $\lambda = 0.15$ µm, The lambda based length is equal to 18, and the width is 60 with a multiple (M) of 176 for NMOS device. Notice that aspect ratio here is 586 » 220. This is to ensure that the device is in the subthreshold region, and the VOH and VOL requirements are met.

Referring to the ratio of $\frac{\mu_n C_{ox}}{\mu_p C_{ox}} = 2.1$ in Table 6-6, the PMOS device aspect ratio should be 2.1 times higher than that of the NMOS device for the same current and saturation voltage (V_{dsat}); but the minimum length for PMOS doesn't need to be 2.7 µm; it is chosen as $L_{min(PMOS)} = 8\lambda = 1.2$ µm. The final results are:

$\frac{W_P}{L_P} = \frac{56}{8}$, M = 176 ; $I_D = 132$ µA and $\frac{W_N}{L_N} = \frac{60}{18}$, M = 176 with the same $I_D = 132$ µA drain current. The calculated V_{dsat} is 64mV, however both the simulation, and later on the measured data indicate a much lower value in the range of 10mV.

Similar calculations and analysis to determine the aspect ratios for the transistors within other blocks have been used throughout the entire design. However going forward, we'll skip most of the details of such calculations in the interest of limiting the scope of this thesis.

6.5.3 Transistor-Level Design of the Driver Stage G_{m2} and the Push-Pull Translinear Bias

Without getting into detail of determination of the aspect ratios for transistors, we present a description of the transistor-level design here. The detailed procedure and steps for finding the aspect ratios have already been thoroughly discussed in the previous section.

The input stage for this transconductance block is a folded-cascode consisting of transistors MP1 and MP2 as the differential pair, feeding the sources of the folded-cascode MOS devices of MN11C and MN12C.

A single-ended to differential conversion is performed by the PMOS current mirror MP11 and MP12, which also act as the upper loads / mirrors, along with their cascode devices MP11C and MP12C. The conversion is performed by the mirroring action of the MP11/MP12, through connecting their common gates node to the drain of the cascode device MP11c. This insures that we benefit from the full signal current swing (up to the differential pair tail current) right at the differential output of G_{m_2}. This output is also the end terminals of the cascoded mesh circuit consisting of MP13, MP13C, MN13, and MN13C. The transistors in the mesh are part of the two translinear loops, which set the bias currents in the output push-pull devices of the next stage, that is G_{m_1}.

The PMOS translinear loop consists of the gate-source voltages of MP111, MP13, MP22, and MP21. The NMOS loop goes around the gate-source voltages of MN111, MN13, MN22, and MN21 as can be seen in figure 6-9.

Since both of the transconductance blocks G_{m_1} and G_{m_2} are operating in the subthreshold region, the translinear loops for PMOS and NMOS devices obey a BJT loop relationship, that is:

$$I_{MP_{111}}\, I_{MP_{113}} = I_{MP_{21}}\, I_{MP_{22}} = Constant \qquad \textbf{(6.14)}$$

$$I_{MN_{111}}\, I_{MN_{113}} = I_{MN_{21}}\, I_{MN_{22}} = Constant \qquad \textbf{(6.15)}$$

The "Constant" in the above equations are the square of the drain currents of either one of the diode connected transistors in the schematic. Moreover, the following relationship between the aspect ratios must hold true:

$$\frac{\left(\frac{W}{L}\right)_{P_{111}}}{\left(\frac{W}{L}\right)_{N_{111}}} = \frac{\left(\frac{W}{L}\right)_{P_{13}}}{\left(\frac{W}{L}\right)_{N_{13}}} = \frac{\left(\frac{W}{L}\right)_{P_{22}}}{\left(\frac{W}{L}\right)_{N_{22}}} = \frac{\left(\frac{W}{L}\right)_{P_{21}}}{\left(\frac{W}{L}\right)_{N_{21}}} \qquad \textbf{(6.16)}$$

In order to prevent a change in the next stage (G_{m_1}) push-pull bias current with a change in the supply voltage, the mesh circuit is cascoded. This is very important as sometimes in a non-cascoded mesh bias loop, a push-pull bias current change of about 20% ~ 30% is noticed for a supply voltage change of only few volts.

The cascode mesh benefits from the application of a low-threshold MOS device ($V_t \approx 0.3V$), in series with the normal threshold MOS transistor ($V_t \approx 0.65V$). The combination is a self-biased cascode with no need for a bias line to feed the cascode transistors, here MP13C and MN13C.

The Translinear loop for a MOS device in SI does not follow Eq. (6.14), but rather follows a sum of the squares of the currents relationship, as presented in the references [33] & [34].

The MP34 and MP34C are the cascoded pair for the input differential pair. Also the MN11 and MN12 along with their cascoded transistors MN11C and MN12C are the constant current sources at the folded cascode nodes; therefore the signal current will entirely pass through the cascode transistors MN11C and MN12C without any attenuation.

The rest of the devices within the schematic of G_{m_2} are mainly for the purposes of biasing, therefore we omit any further explanation here. However it is important to note that the Miller capacitorsCm_{11} , and Cm_{12} between the outputs of G_{m_1} and $G_{m_2}$are not present in any of the schematics of G_{m_1} or G_{m_2}, but rather are shown on the chip top-level schematic, along with the other capacitors of the frequency compensation network.

6.5.3.1 Transistor-Level Design of the Output Over-Current Protection Circuitry within G_{m2} block

Transistors MN60 and MP60 within G_{m_2} block are the current limiting transistors for the G_{m_1} push-pull output devices MP111 and MN111 respectively. The operation of MN60 to act as a current limiter for MP111 is described below. Similar operation can be assumed for MP60 to limit the short circuit current of MN111.

$$V_{GS_{N60}} = V_{SG_{P22}} - V_{SG_{P13}} \quad \textbf{(6.17)}$$

Also for the gate-source voltage of the PMOS push-pull output device within G_{m_1} block we have:

$$V_{GS_{P111}} = 2\,V_{SG_{P22}} - V_{SG_{P13}} = V_{SG_{P22}} + V_{GS_{N60}} \quad \textbf{(6.18)}$$

When there is no signal present at the input, the push-pull output devices are in an equilibrium state, and carry just the quiescent currents. In this situation, the current densities of transistors MP22 and MP13 are the same so their gate-source voltages are equal, therefore $V_{GS_{N60}}$ is equal to

zero. The overdrive for MPOS push-pull output device is similar to the overdrive of MP21, or MP22.

When there is a higher current in the output push-pull MP111 for any reason, its gate-source voltage increases. The gate source voltage of the MP13 should now be reduced due to the action of the translinear loop, while the gate-source voltage of MP22 remains constant at all times.

According to Eq. (6.18), this will result in the generation of some voltage across the gate-source terminals of the protection transistor MN60. At some point, the increase in output current will build enough of a voltage ($\approx V_{t_n}$) across this MN60, which turns the protection transistor on. This in turn causes a current flow from MN60 to MP13, to increase its current, and therefore reducing the output current in MP111 as the result of the action of the translinear loop.

The short circuit current for PMOS output device, according to above explanation can then be estimated from the strong inversion drain equation (see the note below) as the following:

$$I_{SC_P} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{GS_P} - V_{t_p}\right)^2 = \beta\left(V_{ODQ_P} + V_{t_n}\right)^2 \qquad \textbf{(6.19)}$$

Where V_{ODQ_P} is the overdrive voltage at quiescent current for the PMOS push-pull device of the output stage G_{m_1}.

For an overdrive of 0.1V and a $V_{t_n} = 0.65V$, the short circuit current is equal to Isc $\approx$ 20 mA.

A similar expression can be found for the NMOS push-pull MN111, in conjunction with its MP60 current limiter transistor.

$$I_{SC_N} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{GS_N} - V_{t_n}\right)^2 = \beta\left(V_{ODQ_N} + V_{t_p}\right)^2 \qquad \textbf{(6.20)}$$

Here, V_{ODQ_N} is the overdrive voltage at quiescent current for the NMOS push-pull device of the output stage G_{m_1}.

For an overdrive of 0.1V and a $V_{t_p} = 0.75V$, the short circuit current is equal to Isc $\approx$ 25 mA.

Note: In both equations (6.19) and (6.20), use is made of MOS equations in strong inversion. This is justified as during a short circuit, or over-current event, the MOS device is pushed towards its strong inversion.

In the Schematic of Gm_2 presented in figure 6-9, like many other schematics in this design, the self-biased cascode pairs are frequently used. These cascode pairs are made of low and normal threshold devices in series to eliminate the need for a cascode bias line.

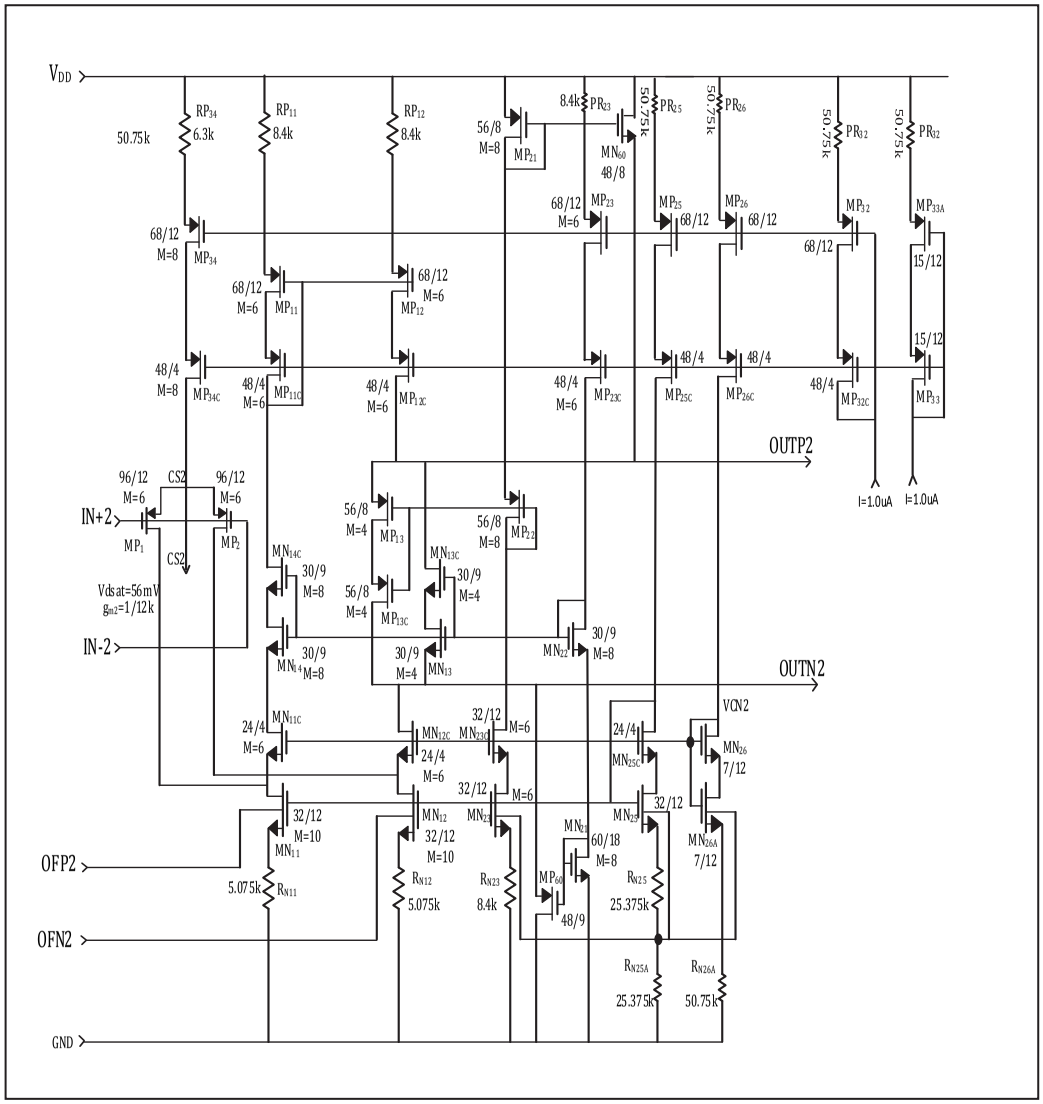

Figure 6-9 – Transistor-level design of the transconductance block G_{m_2} presented in the Model-Based Design of figure 6-3

6.5.4 An Introduction to the Design of Accurate High-Gain Transconductance Blocks

In order to design the input (G_{m_7}) and feedback (G_{m_8}) stages, we need to develop a technique to achieve very high gains, in addition to superior gain-accuracy characteristics. In so doing, the technique "Accurate V-I converter for rail-sensing Current-Feedback Instrumentation Amplifiers" has been developed and patented [35] . A history of prior art is also briefly described here.

6.5.4.1 V-I Converters and prior Arts [35]

Instrumentation amplifiers with current feedback for sensing at the rail voltages conventionally use simple voltage-to-current (V-I) converters, as shown in figure 6-10 [3].

The non-linearity of these simple V-I converters cancel each other when used in a CFIA as first shown in figure 1-7. The relative high offset, and poor common-mode rejection ratio (CMRR) of this simple V-I converter can largely be improved by the chopper Inst-Amp architecture of figure 6-11. However residual inaccuracies and non-linearities of such simple differential amplifier stages in the order of 0.1% are still a drawback for many accurate applications. Therefore, we look for means to improve the accuracy.

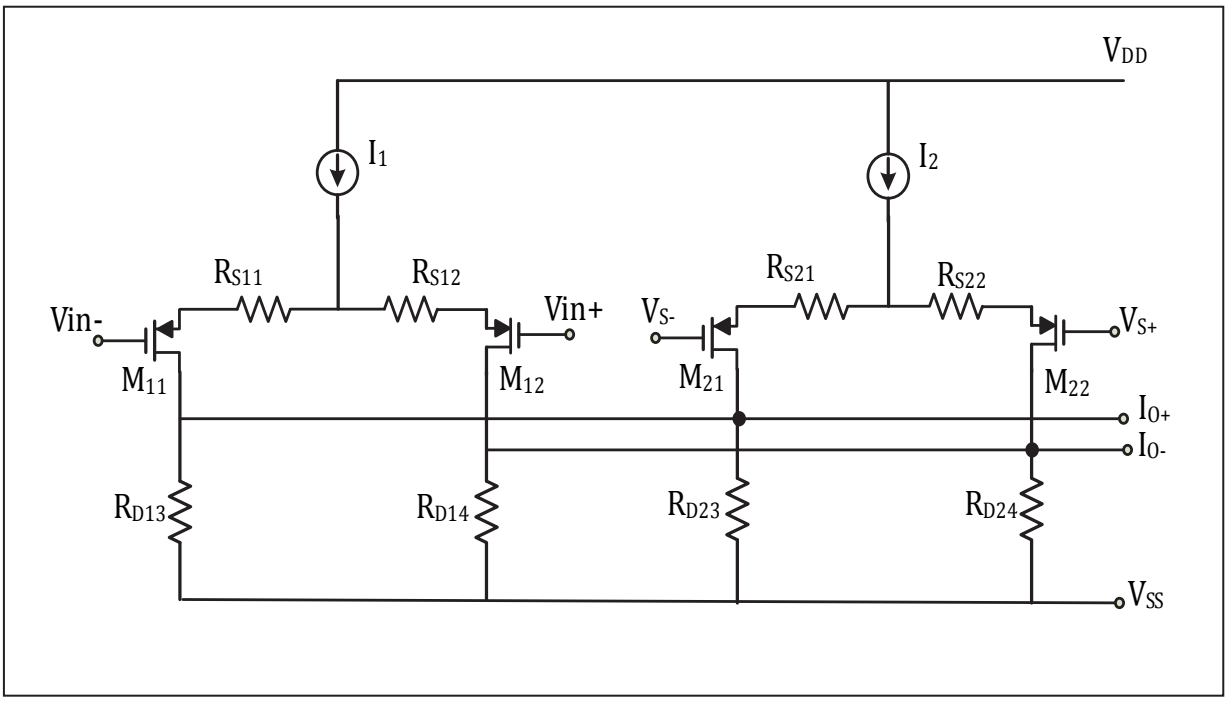

Figure 6-10 – Conventional V-I Converter for a CFIA with Sensing Capability around the Negative Rail

Voltage feedback or voltage boosting can be applied around the P-channel input transistors to improve their accuracy, as shown in **figure 6-12**. Without any gain-boosting, the transconductance of a conventional stage similar to the one shown in figure 6-10 is a function of the transconductance ($\mathbf{g_{m_{Tr}}}$) of the input transistors as well.

$$G_{m_{tot}} = \frac{1}{\frac{1}{g_{m_{Tr}}} + R_S} \qquad \textbf{(6.21)}$$

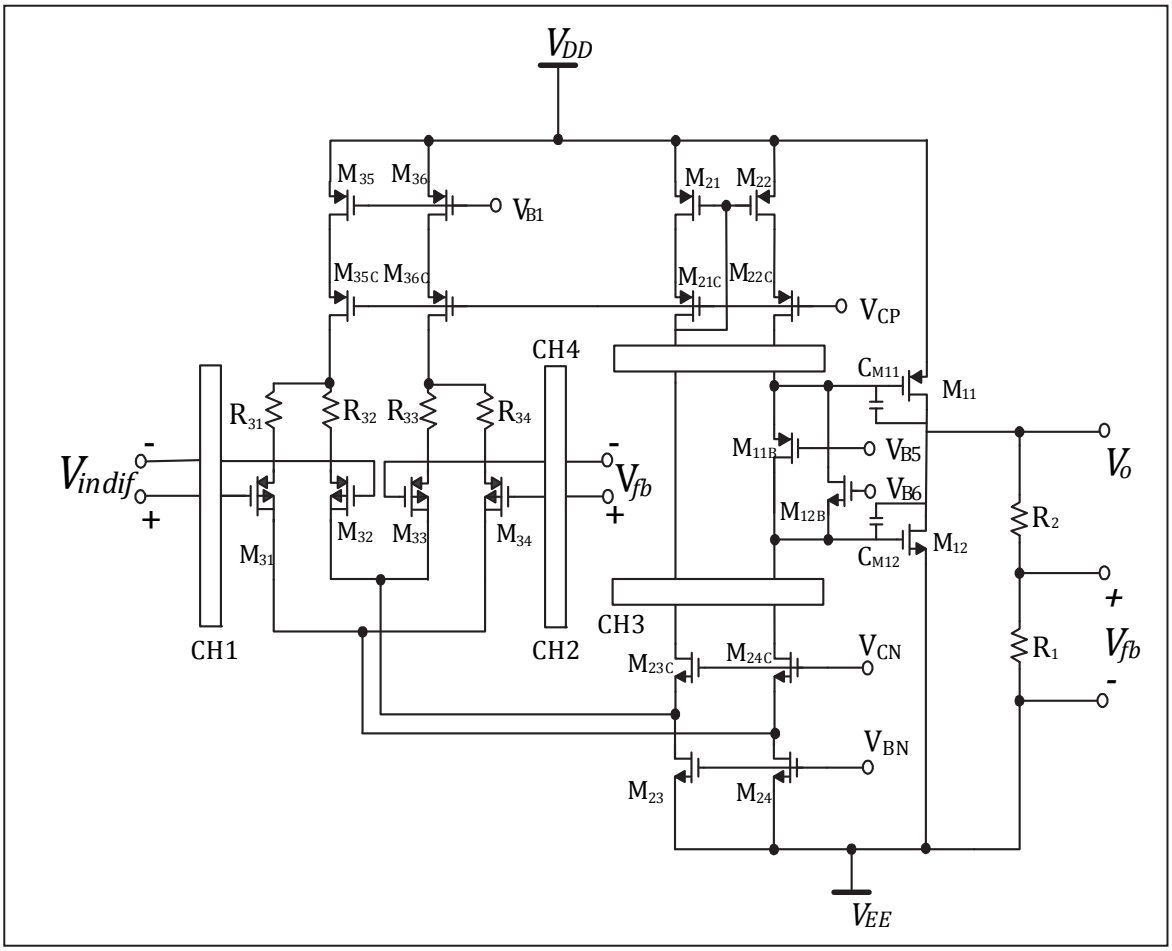

Figure 6-11 – A Chopper Version of CFIA with Sensing Capability around the Negative Rail

where $g_{m_{Tr}}$ is the transconductance of the input transistor, and R_S is the value of the degeneration resistor. It is obvious that $g_{m_{Tr}}$ is a strong function of transistor bias, size, temperature and other parameters. Also $g_{m_{Tr}}$ is never as linear as R_S as it is not a resistor. Voltage feedback reduces the influence of the input transistors on the accuracy and linearity by magnifying the $g_{m_{Tr}}$ by the loop gain of the feedback circuit, that is the voltage gain provided by the Op-Amp.

The result is that the transconductance $G_{m_{tot}}$ of the input stages is fully determined by the source degeneration resistors $R_{S_1} = R_{S_2} = R_S$, that is $G_{m_{tot}}$ becomes equal to $G_{m_{tot}} = \frac{1}{R_S}$.
These degeneration resistors can be chosen to be accurate and linear, with minimal temperature coefficient effects, such as the case of using thin-film or low tempco poly resistors. However, in this case the ability to sense around the negative supply rail is lost again in the architecture of figure 6-12, because the output voltages of the Op-amps cannot be pulled below the negative supply rail voltage.

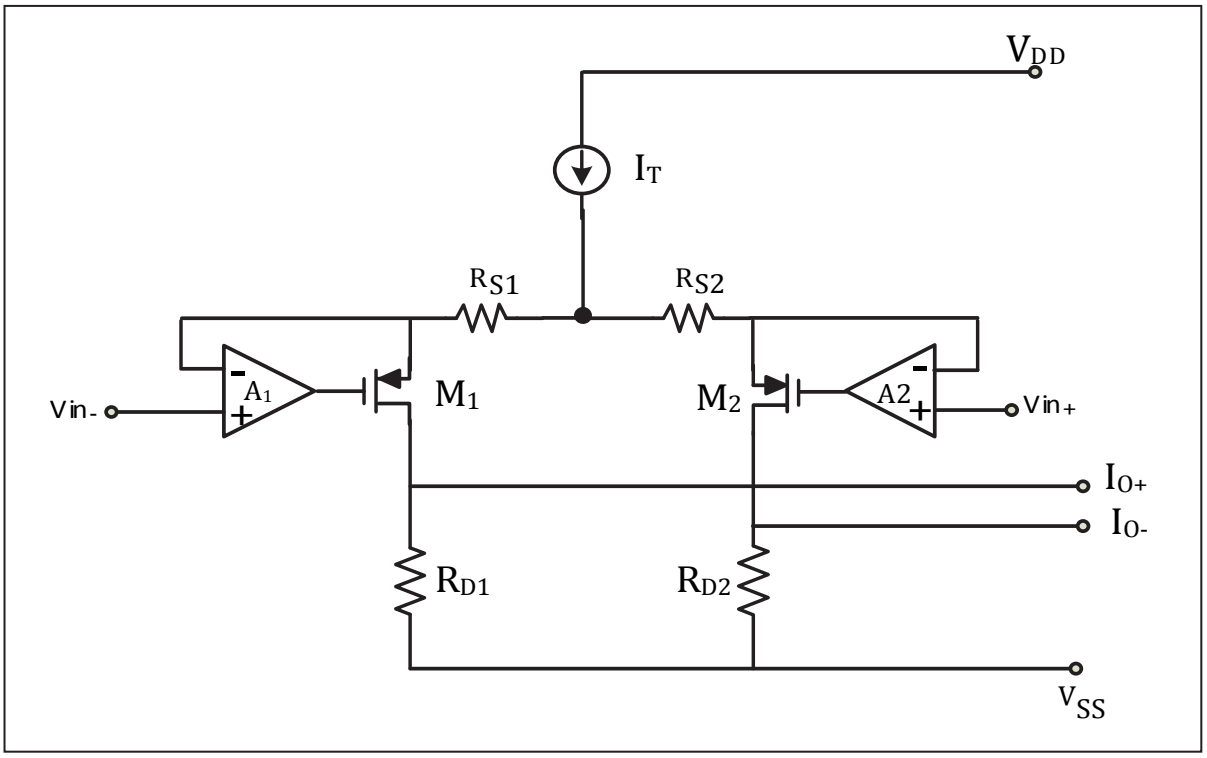

Figure 6-12 – The Conventional V-I Converter with Voltage Feedback (Voltage Boosting) is Suffering from the Lack of sensing capability for the Negative Rail

To solve these problems, one can reverse the polarity of the connection to the inputs of the Op-amps and use complementary N-channel output transistors, as depicted figure 6-13.

If the negative inputs of the Op-amps are able to sense around the negative rail, and if we apply one internal transistor voltage shift upwards to the positive input of the Op-amps, then the circuit of figure 6-13 approaches our goal.

However, the solution of figure 6-13 has still a number of disadvantages. Firstly, the noise of the differential input pair of the Op-amps is added to the noise of the Inst-Amp. Secondly, we desire to obtain a simple circuit; particularly, when we use this V-I converter in the chopper Inst-Amp of figure 6-11, we cannot afford many parasitic capacitors. Thirdly, the loop gain is decreased by

the source degeneration resistors R_{S_1} and R_{S_2} of the output transistors M_1 and M_2. Hence, the Op-amps need a high voltage gain.

The circuit of figure 6-14 shows the transistor implementation of the patented architecture [35] mentioned is section 6.5.4. Only one sense transistor per side M_{11} or M_{12} is in between the input and the gain and linearity setting resistor R_{11} or R_{12}. So the noise and offset contribution is nearly equal to the simple differential pair of figure 6-10.

The input sense transistors are terminated to the negative supply rail by drain resistors R_{15} or R_{16}. The folded cascodes M_{15} and M_{16} collect any excess current by which the output transistor M_{13} and M_{14} are driven. The circuit is simple. However the transconductance of the composite input transistor $G_{1,2} = A_{V15,16}/R_{13,14}$ is still relatively low. The voltage gain in the loop is: $A_{V15,16} \approx \mu_{11,12}\, \mu_{15,16}$, with $\mu_{11,12} \approx G_{m11,12} \times R_{DS11,12}$ and $\mu_{15,16} \approx G_{m15,16} \times R_{DS15,16}$. The transconductance of the input transistors has roughly been increased by the maximum voltage gain $\mu_{15,16} \approx 30$ in comparison to the conventional circuit of figure 6-10. The circuit basically satisfies the specification. But we like to further improve the loop gain.

In order to further increase the loop gain the folded cascode transistors M_{15} and M_{16} have been cascoded by M_{151} and M_{161}. This is depicted in figure 6-15. Now the transconductance of the composite input transistors is increased by a factor $\mu_{15,16} \times \mu_{151,161} \approx 1000$ in comparison to the conventional circuit of figure 6-10. Finally, to decrease the influence of a common-mode voltage on the output current the output transistors M_{13} and M_{14} have also been cascoded by M_{131} and M_{141}. The result is an accurate and linear overall transconductance $G = 2/(R_{11} + R_{12})$.

The resulting offset and CMRR are still comparable with those of a single pair as shown in figure 6-10. A large decrease of the offset and increase of the CMRR can be obtained if the accurate composite V-I converter is used together with choppers in a similar manner as shown in figure 6-11.

In conclusion, we have now an accurate and linear V-I converter with composite input transistors for use in current-feedback Inst-Amps. The V-I converter is able to sense differential input voltages in a range around the negative supply rail.

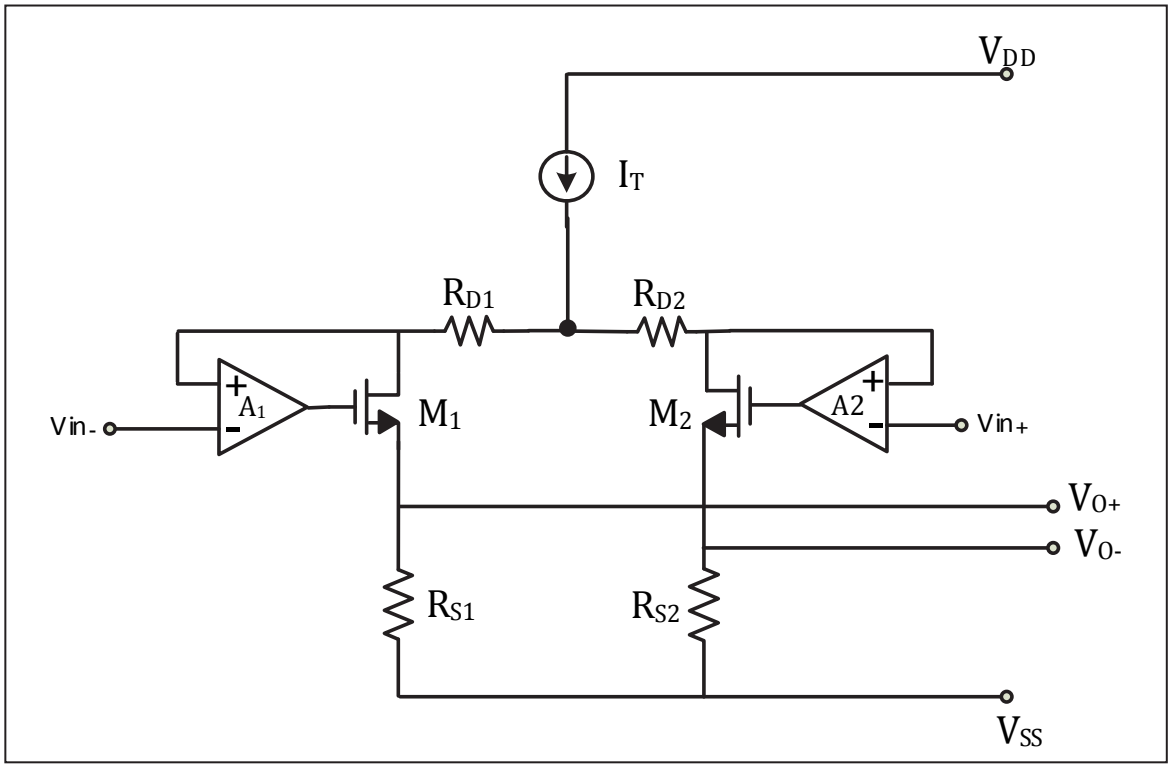

Figure 6-13 – Improvement of the Architecture of figure 6-12 by Changing the P-channel device at the input to its N-channel counterpart to be able to sense the negative rail

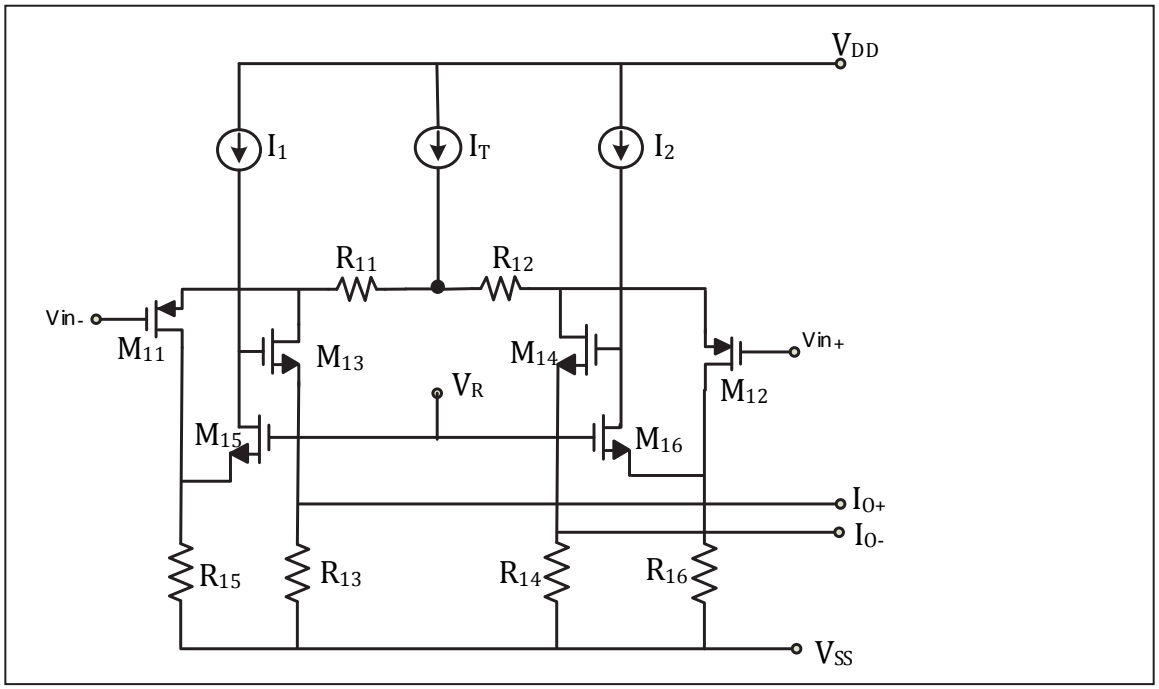

Figure 6-14 – Improvement on the Architecture of figure 6-13 through several modifications discussed in the text

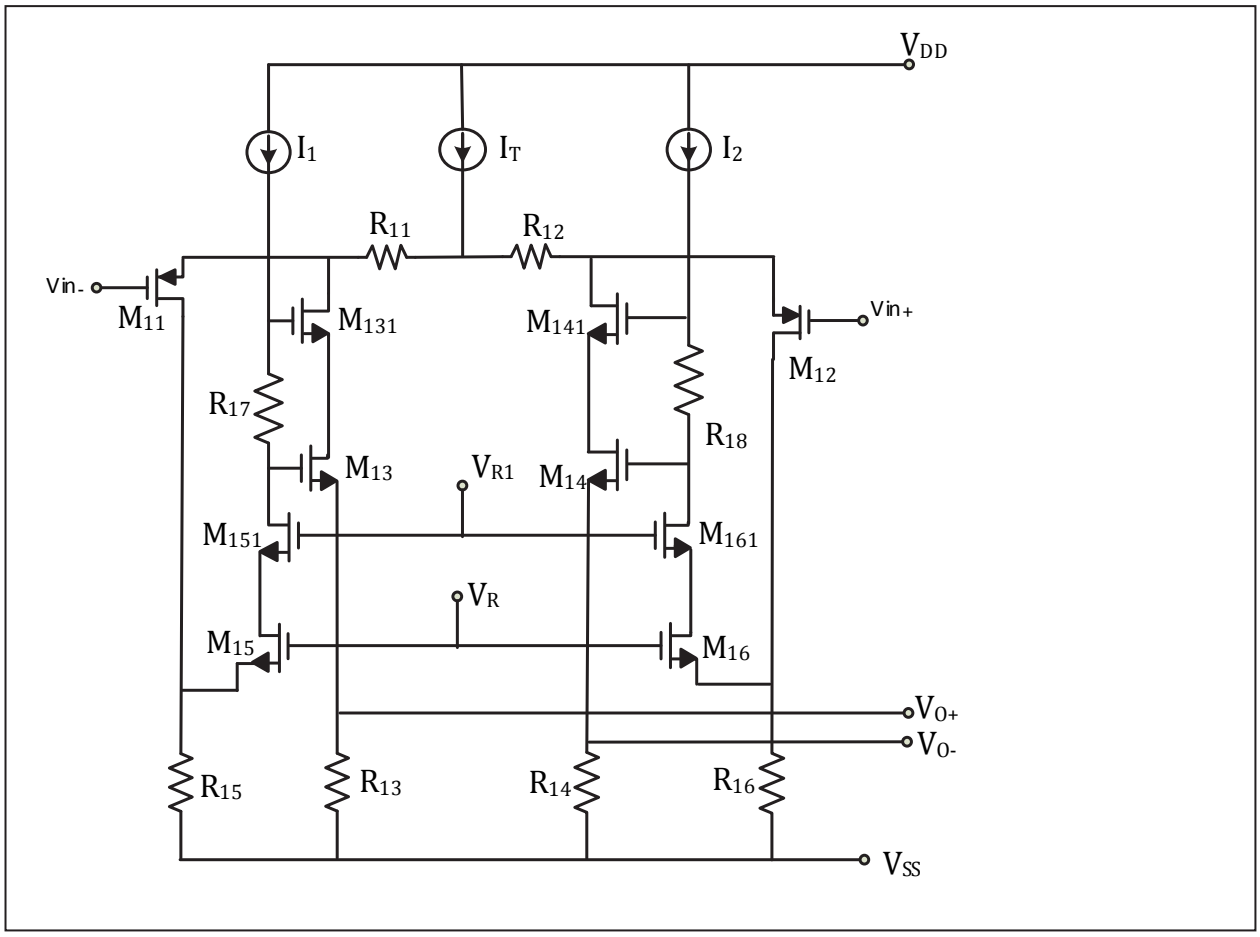

Figure 6-15 – Further Improvements on the Architecture of figure 6-15 through cascoded design

6.5.5 Transistor-Level Design of High-Gain, Accurate Input and Feedback Transconductance blocks G_{m7} and G_{m8}

We proceed with the design of G_{m_7} and G_{m_8}, using the patented architecture [35] as discussed in figure 6-15 of section 6.5.4.1. These two voltage-to-current converters are the main input, and feedback transconductance blocks of CFIA design.

The transistor-level schematic of G_{m_7} (or G_{m_8})is shown in figure 6-16. The heart of each block consists of two super composite-transistor loops, providing a very high gain from the input of each transistor of the differential pair, to its associated degeneration resistor at its source, exactly the same way as discussed for the circuit of figure 6-15.

The loop at the inverting input (IN-) consists of transistors MP711, Cascoded combination MN715 / MN715C, and finally the Cascoded combination MN713 / MN713C, terminating at source degeneration resistor R711 with a value of 12 kΩ. Similarly, the loop for the IN+ input consists of MP712, Cascoded combination MN716 / MN716C, and lastly the Cascoded combination MN714 / MN714C, eventually terminating at the source degeneration resistor R712. These loops each provide a loop gain of about 5000 to make the transconductance of the stage practically independent of the transconductances of the input devices, and entirely defined by the source degeneration resistors.

With setting the above source degeneration resistors to 12 kΩ, we obtain the desired value of $G_{m_7} = G_{m_8} = \frac{1}{12\text{k}\Omega}$ for the transconductances of G_{m_7} and G_{m_8} as was demanded by the model-based design, summarized in Table 6-2.

The above indicates that the matching requirement of $G_{m_7} = G_{m_8}$, and their tracking over temperature, which is a measure of the gain accuracy, is translated to the matching of R711 / R712 of G_{m_7} to R811 / R812 of G_{m_8}. This is much easier to achieve as opposed to matching of two conventionally designed G_{m_7} and G_{m_8}. Also any mismatch of the two source degeneration resistors such as R711 and R712, or R811 and R812 will be translated to an initial offset error for the associated block.

It should be obvious that the loop-gain also has a profound effect on all the accuracy parameters such as gain-accuracy, gain tempco, linearity and its temperature coefficient. Therefore voltage gains of several thousands are desirable.

The overall gain of either one of G_{m_7} or G_{m_8} is set by the ratios of R713's and R711's for G_{m_7}, and R813's and R811's for G_{m_8}. This gain is set by several constrains, and usually is not very high. Since the outputs of G_{m_7} and G_{m_8} are connected in parallel at their summing nodes, the above gain is further divided by two

The maximum input differential voltage should be lower than the span of voltage across each degeneration resistors in each leg. This means that the maximum differential input voltage

should be less than half of the tail current multiplied by the value of each degeneration resistor. Usually a factor of about 20% ~ 30% margin is considered.

In this design, the tail current is 20μA, and the degeneration resistor is 12k; therefore the span of voltage for when the signal drives the amplifier completely at one ear is 120mV. This is more than the 100mV specified maximum differential input voltage by a margin of 20%.

Since the span of the voltage (half of the tail current times the value of source degeneration resistor) must not change over the temperature range of operation (-40°C to 125°C), the tail current is biased from a reference current (zero TC), as opposed to the otherwise desired PTAT current source, which is often preferred in Op-Amos for the purpose of keeping the bandwidth constant over temperature (BJT and MOS in weak inversion).

As this design is not using dynamic gain error trimming, there should be provisions to perform the gain-error trim to obtain the required gain accuracy. In the next section, we briefly discuss both the gain-setting and gain-trimming approaches with such designs.

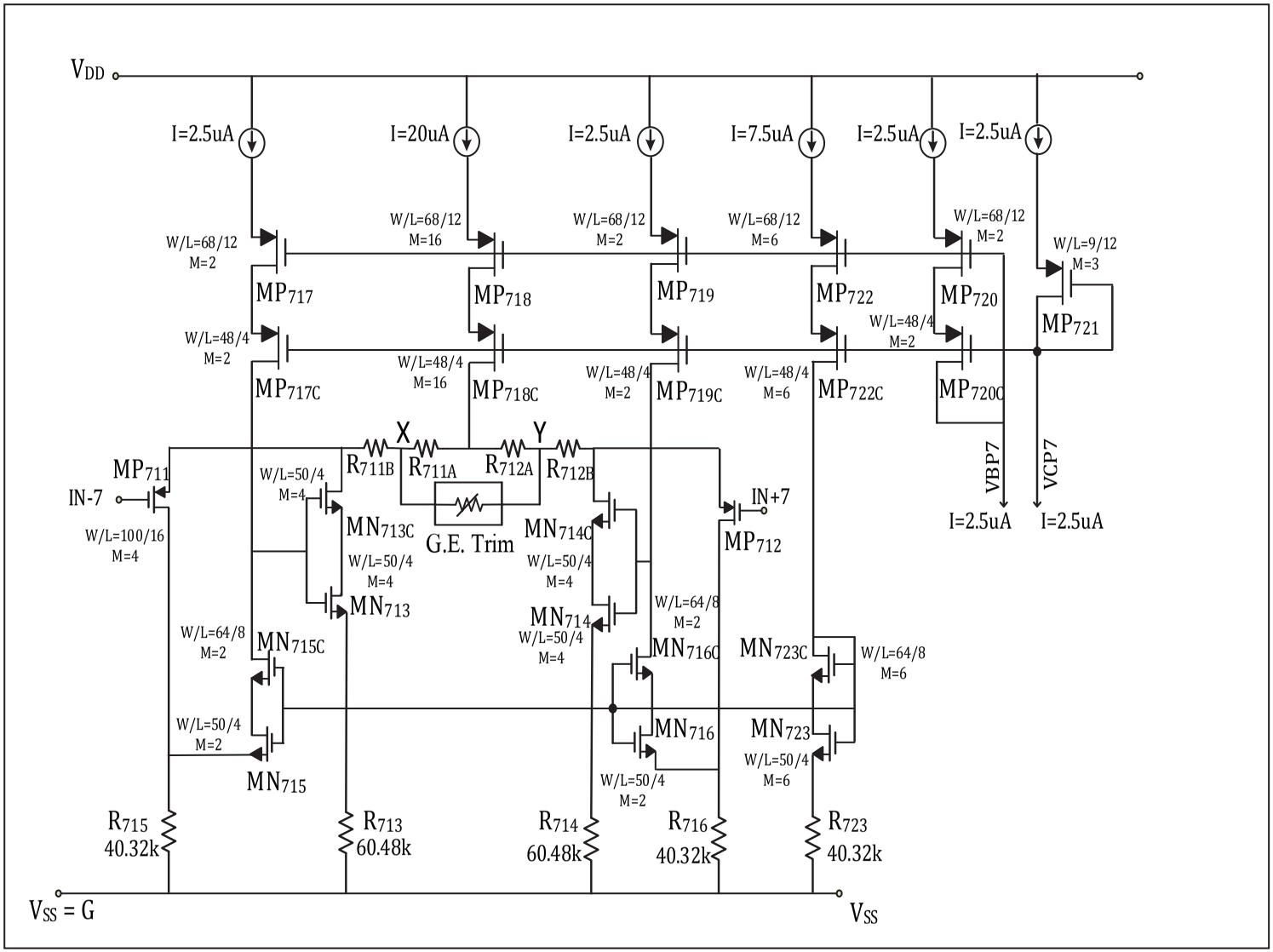

Figure 6-16 – Simplified Transistor-level Schematic of the blocks G_{m_7}/ G_{m_8} presented in the Model-Based Design of Figure 6-3

6.5.5.1 Gain Setting Options in CFIA Design

From equations (1.4) and (1.5) of section 1.3 it is clear that the gain can be set by the ratio of the gain setting resistors R_2 and R_1. The simplest approach is using a voltage divider to do the task. However in designs with a requirement for a large gain settings range (G=1 ~ G=1000), as is the case for this project, the simple approach may not be suitable.

In an internal gain setting to achieve a gain of 1000, with a reasonable selection of R_2 = 90 kΩ for example, the value of R_1 is set to $R_1 = 90.09\ \Omega$. Low value resistors can be troublesome due to errors associated with parasitics such as contact resistances, etc. Higher value selections for R_1 on the other hand, may result in impractical choices for R_2. Although there are ways to mitigate such problems, better approaches must be examined to insure the ease of implementation.

In this design, inspired by an early-days lab-work, a "vernier-resembled" divide by 10 resistive-ladder network is used to set the gains at fixed values of 1, 10, 100, and 1000 as shown in figure 6-17. The simple, yet elegant circuit is quite self-explanatory here. Metal-link options will select the desired tap among X10, X100, and X1000 taps to be connected to FB point. In a unity gain configuration, the FB node is simply connected to the output.

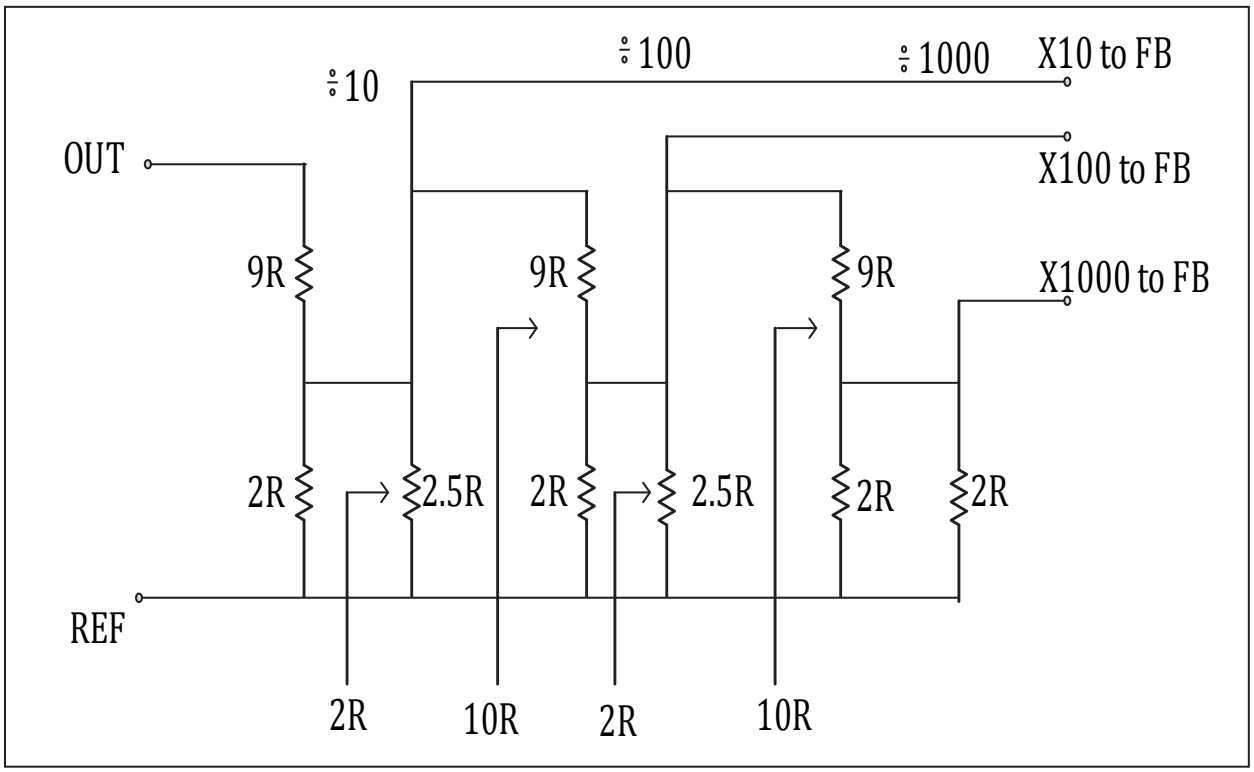

Figure 6-17 – "Vernier" Type Gain Setting Resistor Network Suitable for Large Gain Ranges

6.5.5.2 General Trim Considerations in Precision Analog Design

In the area of precision analog, trimming is a required operation when the Dynamic Error Cancellation Techniques (DECT) are not utilized. If error cancelations are not through DECT, several considerations must be taken into account before a decision is made as to how the trimming is performed.

In general any trim has several characteristics, each with its own significance. Here are the most important ones:

i. **Trim Type**:

This is usually the step of manufacturing in which trim takes place.

a. Wafer Sort Trimming (WST)

b. Post-Packaged Trimming (PPT)

As mentioned in sections 3.2.1and 3.2.2 of chapter 3, the choices of trims of today are mostly PPT, but still could be WST for large die and packages to save the cost of otherwise rejected expensive package fallouts.

ii. **Trim Direction**:

This considers the direction (increase or decrease) of the parameter of interest with trimming. There are two choices:

c. Center-Weighted Trim

d. One-Sided Trim

Center-Weighted Trim can trim a parameter up or down, whereas One-Sided Trim, trims only in one direction; either up or down. One-Sided trims are rarely used today because among other reasons, each part out of the factory would have to be fully trimmed since it will set to be off-center from the target specification.

iii. **Trim Coverage and Step**:

e. Trim Range

f. Trim Resolution

Trim range concerns the coverage of the trim; such as +/-5% of the Full-Scale-Range (FSR).

Trim Resolution is the smallest possible step adjustment in a trim. It determines how precisely the trim can adjust the parameter of interest.

The trim range and trim resolution are considered the most important characteristics of the intended trim.

iv. **Trim Order and independency (Orthogonality)**:

Trim order is important when trimming a parameter affects the value of another already-trimmed parameter. This is the case when the trim mechanisms selected for different parameters have dependency on each other. In this case the trim is referred to as non-orthogonal and should be avoided if possible. If trim dependency can not be avoided, trims must be performed in the correct order to minimize this dependency.

v. **Trim Bit Redundancy**:

This is usually additional bits added to the trim to make sure there are no missed - regions in between successive trims. Trim bit redundancy concerns providing some overlaps of trim steps, and usually increases the number of required trim-bits (a measure of cost and complexity of the trim) by one or few bits.

Although there are many ways to perform gain trimming for general purpose applications, there are only few viable options for precision trimming of the gain when considering some of the aspects of the trims discussed above.

6.5.5.3 Sources of Errors Contributing to Gain Error in CFIA Designs

Referring to Eq. (1.4) in chapter one, the closed loop voltage gain of this CFIA is :

$$A_V = \left(\frac{R_{811}}{R_{711}}\right) \cdot \left(1 + \frac{R_2}{R_1}\right) \qquad \textbf{(6.22)}$$

Therefore, the sources of error are summarized as:

i. The mismatch of the source degeneration resistors R_{711} and R_{811} in G_{m_7} and G_{m_8} respectively.

ii. Mismatch and deviation of the gain setting resistors R_2 and R_1 from their intended value.

iii. Loop-gain of the feedback network, which is not shown in Eq. (1.4), since it is assumed to be very high; therefore we disregard this error source.

The tail currents of G_{m_7} and G_{m_8} do not play any role here as the transconductance of these blocks are entirely defined by their degeneration resistors via the application of the technique discussed throughout section 6.5.4.1.

The design of this thesis uses thin-film resistors for gain setting, as well as degeneration resistors in transconductance blocks. Thin-film resistors are known for their extremely low temperature coefficients, about (4 ~8) ppm/°C, and stability over time.

6.5.5.4 Gain-Error Trim Range and Resolution for the CFIA Design of this Thesis

Equation (6.22) has two terms (resistor ratios). If we assume a1sigma mismatch of about 0.10% for thin-film resistors (typical for thin-film resistors in many processes) then each ratio in the above equation accounts for a 0.2% mismatch. The total mismatch error is finally estimated to be equal or less than 0.4%

In many designs, in particular a precision design, provisions must be in place to cover a 6σ variation in process. This is particularly important when the production final test program (ATE / FT) does not cover the testing of the parameter of interest at its outgoing final test step. This means a 6σ GBD is in order as described in section 3.5.

As a result of the above consideration, a variation of 6 (0.4%) = 2.4% is needed to cover the gain-error trim. We pick a 2.5% range for our gain-error trim range, to be validated later through simulations.

From the EC table (Table 6-1), the gain-error specification is 0.01% (typ.), and 0.05% (max.). It is a good practice to choose the resolution of the trim to be significantly lower than this maximum specification. This is to cover the temperature, and process variations (a factor of 5 ~6 lower than the maximum over-temp limit is not unusual).

Selecting a trim target of 0.01% for this design is sufficient. With a bidirectional trim 0.5 LSB is theoretically achievable, however we pick the LSB of the trim to be 0.01%. With this selection, the number of the required trim bits (N) for a binary weighted trim, knowing the Trim Range (T_{Range}) and Trim Resolution (T_{Res}):

$$N \geq \log_2 \frac{T_{Range}}{T_{Res}} = \log_2 \frac{2.5}{0.01} = 8 \text{ Bits}$$

With the addition of 2 redundancy bits (lowering the bit weight's ratio to less than 2), the final gain-error trim specification for the design of this thesis is given in Table 6-7.

Since the gain-error trim circuitry is added to both G_{m_7} and G_{m_8} , this trim is a bidirectional trim. Moreover, the trim is a WST (Laser-Links) type, with added die coat to alleviate the effect of assembly shifts. Thin-film resistors are excellent candidates for precision laser trimming

Trim Characteristics	Value	Unit
Achievable Trim (0.5 LSB)	0.005	% FSR
Trim Range	2.5	% FSR
Trim Resolution (1 LSB)	0.01	% FSR
Nuber of Trim Bits	$8 + 2 = 10$	Bits
Trim Direction	Bidirectional	N/A
Trim Type	WST / Laser-Links	N/A

Table 6-7 – The Calculated G.E. Trim Characteristics for the CFIA Design of This Thesis

This subsection concludes by fulfilling the requirements for the five major characteristic of a systematic trim design brought forward in section 6.5.5.2.

6.5.5.5 Gain-Error Trim Implementation for the CFIA Design of this Thesis

Although in general the gain trim can be performed on gain setting resistors, the approach should be challenged in designs similar to the one in hand as described below. An on-chip gain trim is needed for precision designs, even if the gain is variable, meaning that the customer can set the gain with an external precision resistor divider.

A perfect customer chosen ratio of "9.000" for the above divider, in an attempt to achieve a perfect gain of "10.000" may, in the sense of precision analog, result in a gain significantly different than "10.000". This is because the chip introduces its own gain-error components to the system.

The above explains why the gain trim in the work of this thesis is not performed on the gain setting resistors presented in section 6.5.5.1, as the design was indeed intended to have both fixed and variable gain options.

Referring to our G_{m_7} (or G_{m_8}) schematic of figure 6-16, it is clear that a good place to insert a gain-error trim is actually at the source degeneration resistors R_{711} / R_{712} (R_{811} / R_{812} for G_{m_8}). However one should be careful in the implementation as a change (a trim) in one of the source degeneration resistors at one side will introduce an offset into the system.

The gain-error trim for each block of G_{m_7} or G_{m_8}should be designed in such a way that both degeneration resistors within each transconductance block be affected exactly equal and simultaneously, in order to avoid tampering with the offset which is introduced otherwise.

A simple approach is taken by the designer to achieve this goal, keeping the orthogonality of the gain-error and offset compensations intact. In so doing, each degeneration resistor is segmented into two pieces, and a trim-link network (a trim dependent variable resistor) is added to each G_{m_7} and G_{m_8}, connecting the middle points of the two degeneration resistors (points X and Y) together as shown in the schematic of figure 6-18.

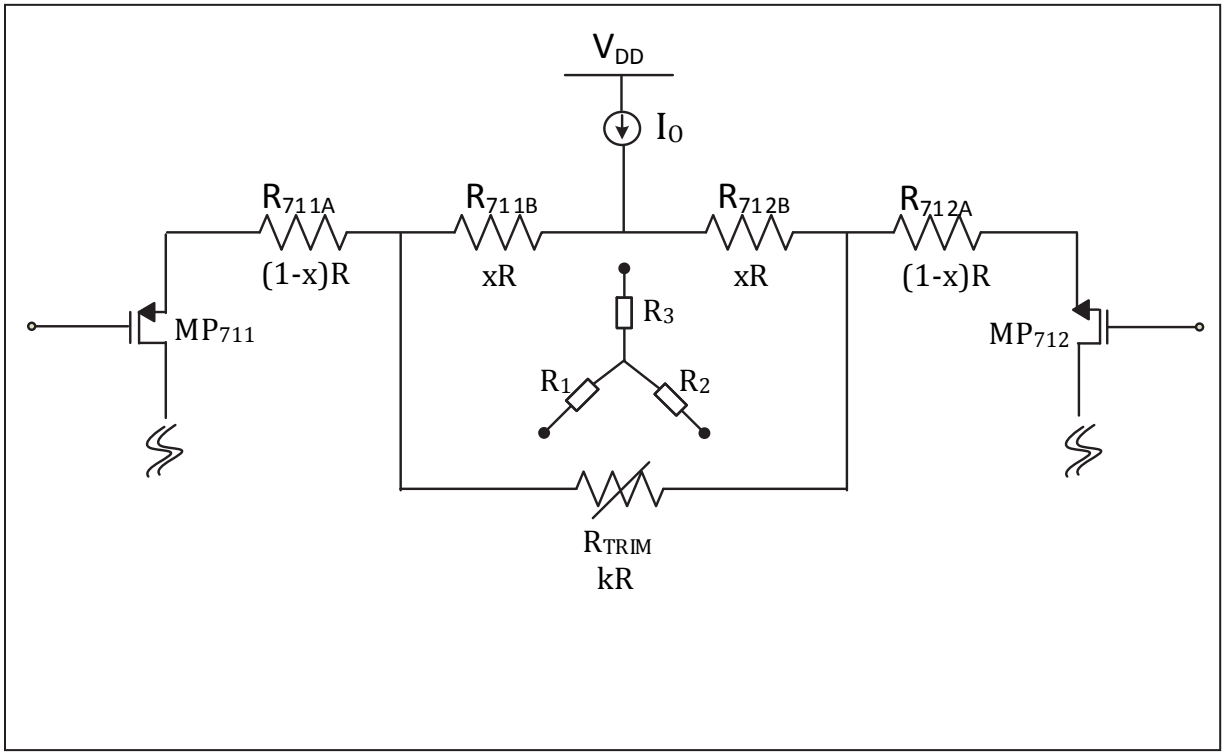

Figure 6-18 – Portion of the Schematic of G_{m_7}(Accurate V-I Converter) Showing its Gain-Error Trim Taps with its Star–Delta equivalent Resistors

6.5.5.6 Estimation of Trim-Links Branch-Off Points at Degeneration Resistors

In order to better visualize the circuit, we show in figure 6-19 the equivalent star (Y) connection of the delta (Δ) connections formed by R711B, R712B, and the added trim-link R_T for transconductance G_{m_7} .

If we denote the total resistance of each R711 and R712 by parameter R, then the following holds true:

$$R_1 = R_2 = \frac{x\,R\;\; kR}{2xR + kR} = \frac{x\;k}{2x + k}\;R \qquad \textbf{(6.23)}$$

$$R_3 = \frac{x^2\,R^2}{2xR + kR} = \frac{x^2}{2x + k}\,R \qquad \textbf{(6.24)}$$

The transconductance of G_{m_7} is therefore equal to:

$$G_{m_7} = \frac{1}{R_1 + (1-x)R} = \frac{1}{[\frac{k\,x}{2x+k} + (1-x)]R} \qquad \textbf{(6.25)}$$

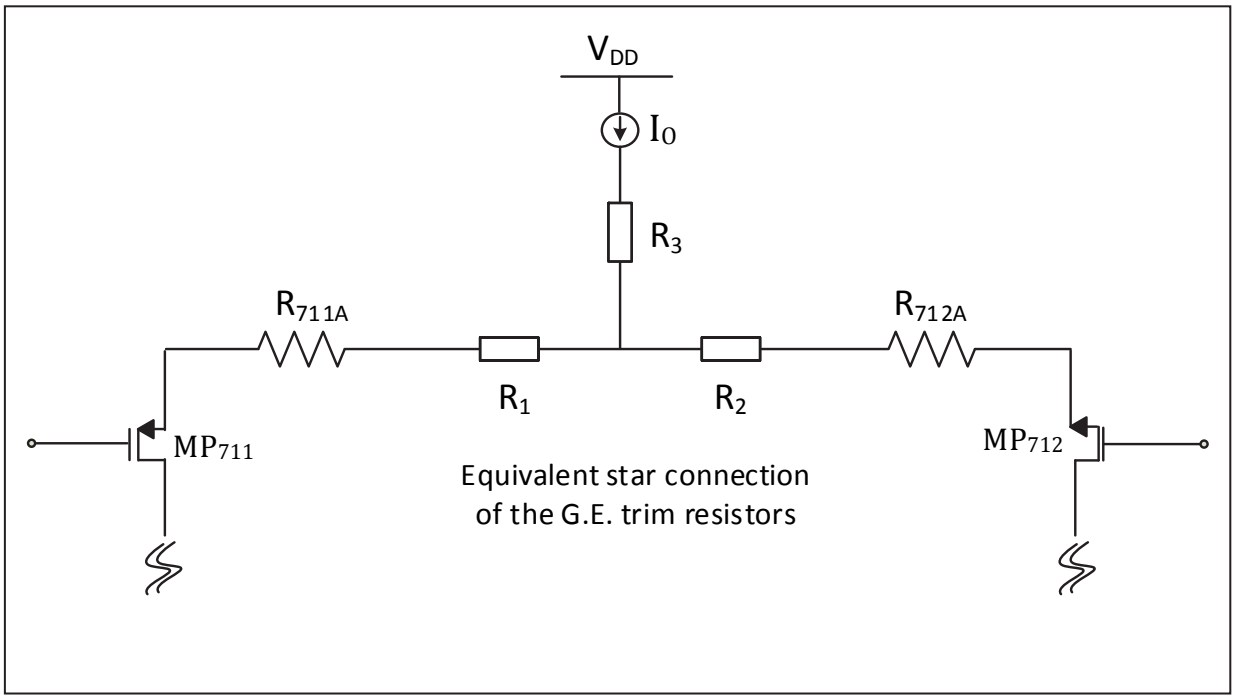

Figure 6-19 – Simplified Schematic of the equivalent Star Connection of the G.E. Trim of G_{m_7}

If the trim range (in fractions of FSR) is equal to α (in this design α = 2.5% per estimation of section 6.5.5.4), then the transconductance G_{m_7} of Eq. (6.25) equals to:

$$G_{m_7} = \frac{1}{[\frac{k\,x}{2x+k} + (1-x)]R} = \frac{1}{(1-\alpha)R} \qquad \textbf{(6.26)}$$

This leads to the final quadratic equation in terms of the trim branch-off location "*x*":

$$x^2 - \alpha x - 0.5\alpha\, k\ = 0 \qquad \textbf{(6.27)}$$

Let's use Eq. (6.27) to calculate the values of R_{711B} and R_{712B} at branch-off points X and Y for the design of this thesis, based on the information acquired so far.

$Number\ of\ Trim\ Bits = 10;$ $(this\ means\ ten\ trim\ links\ are\ available)$

$Trim\ Range = .025$

$Min.TrimLink\ Resistance = 30K;$ $(this\ is\ a\ foundry\ recommendation)$

This indicates that the total resistance of the trim link network is (10) (30k) = 300kΩ; moreover we have:

$k\ .R = Total\ TrimLink\ Resistance = 300\text{k}\Omega$; and $R = R_{711_{total}} = 12\text{k}\Omega$

Then: $k = \frac{300\text{K}\Omega}{12\text{K}\Omega} = 25$; (k is the number of segments of 12kΩ in the total trim-link)

If we substitute the values of α =0.025 and $k\ = 25$ into the quadratic equation of (6.27) we finally reach at:

$$\boxed{x = 0.51}$$

This means that the branch-off points to connect the trim-link in the design of this thesis is at the half points of the sources degeneration resistors.

The technique is elegant, and will only change the gain, with no effect on the offset, i.e. orthogonality of the trim is observed.

Finally it is always a good practice to sacrifice a trim bit to exchange resolution for range (double the range with half as good of a resolution as before). This can sometimes adversely affect the yield for the required accuracy, but it allows at least a product to be available for sampling to customers on first silicon.

The trim-link itself is a simple resistive network similar to the trim circuitry shown in figure 3-6 of the section 3.2.1 in chapter 3, with Zener-Zaps replaced by thin-film laser trim-links.

6.5.6 Transistor-Level Design of the Integrator G_{m4}

G_{m_4} is the Integrator transconductance block inside the first-level compensation loop to take care of the offsets of G_{m_7} and G_{m_8}.

In addition to G_{m_3} the loop consists of the transconductances G_{m_5} , G_{m_6} , and the weak transconductance G_{m_3}, in addition to the summing point circuits at the outputs of (G_{m_5} , G_{m_6}) as well as the outputs of (G_{m_7} , G_{m_8}).

The integrator stage G_{m_4}, like other integrators in this design, is a PMOS input folded cascode stage with a common-mode feedback loop consisting of the source followers MN301 and MN303, as well as MN302 and MN304 in the following G_{m_3} block, which is the voltage attenuator stage.

The input stage of G_{m_4} and that of the similar integrators in this design use low-threshold PMOS devices for an increased upper limit on their common-mode voltage range. The stage is designed for a final transconductance of $G_{m_4} = \frac{1}{25\text{k}\Omega}$, after some refinements in the initial estimation of the model-based design of sections 6.4.3 and 6.4.4.

This transconductance value remains fairly constant over its wide temperature range of operation (-40°C to 125°C) due to the fact that the stage is biased by a PTAT current source, and the MOS transistors operate in their weak inversion regions as is clear from Eq. (2.11) of chapter 2.

The cascode output of this stage has a good output swing capability. Its differential output is capable of charging the integrator capacitors Cm_{41} and Cm_{42} to their final DC voltages of 1.6 volts. This is essential to have a lower filtering capacitor at this stage, as well as a smooth and low ripple operation of the integrator. The capacitor values are the same as in model-based design summarized in Table 6-3, which is also valid for all the other capacitors in this design.

The common-mode input range is from about 0.2V above V_{SS} to approximately 1V below V_{DD}. The bias for this stage is through two 1μA PTAT current sources off of PTAT bias circuit.

The PMOS gate biasing of this stage is also used to bias some adjacent neighboring integrators such as $G_{m_{15}}$, $G_{m_{18}}$, $G_{m_{21}}$, and $G_{m_{23}}$.

The common-mode feedback circuit of G_{m_4} uses the source-followers of the block G_{m_3} as part of its common-mode feedback loop. This is through the loops of gate-to-drains of the source-followers of G_{m_3} which are connected to the summing points at the upper cascode within G_{m_4}.

6.5.6.1 Transistor-Level Designs of the Integrators G_{m9}, G_{m12}, G_{m15}, G_{m18}, G_{m21}, and G_{m23}

As briefly touched in the previous section, all integrators are more or less similar, and have the same architectures with identical or very close specifications; therefore no further discussion on such designs is needed.

6.5.7 Transistor-Level Design of G_{m5} and G_{m6} Sense Amplifiers

These two sense amplifier blocks are used to detect the offset voltages of G_{m_7} and G_{m_8} transconductances. Their outputs are summed up at a simple summing network with the outputs of the weak transconductance $G_{m_{10}}$, along with the inputs of a DPDT (MUX_1) switch.

The transconductance $G_{m_{10}}$ as described before is used to compensate the offsets of G_{m_5} and G_{m_6} through a simple summing circuit (SUM_4). The chopper after the MUX_1 switch, that is CH_2, rectifies the offset correction current coming from the sense amplifiers G_{m_5} and G_{m_6} to build the required correction voltage across the G_{m_4} integrator capacitors Cm_{41} and m_{42} .

This correction voltage is scaled down by the attenuator G_{m_3}, and is fed back to the bodies of MOS transistors MN215 and MN216 of the associated summing circuit (SUM2), to generate the correction current to cancel the offsets of G_{m_7} and G_{m_8}. The transfer function for this V-I conversion is therefore the body transconductances of the MOS device MN215 and MN216, that is $g_{mb_{N215}}$and $g_{mb_{N216}}$. The correction current is therefore dependent on both the value of G_{m_3} , as well as the values of body transconductances of MOS devices MN215 and MN216 within the summing circuit SUM_2. This current will eventually cancel out the offsets of G_{m_7} and G_{m_8} through several tens of chopper clock cycles.

With respect to the architectures used for G_{m_5} and G_{m_6}, they are very similar to the architectures of the patented circuit for G_{m_7} and G_{m_8},with just different bias and transconductance requirements. The scaled-down factor for bias and transconductances of G_{m_5} and G_{m_6} with respect to those of G_{m_5} and G_{m_6}, is a factor of 2.5. This means $G_{m_5} = G_{m_6} = \frac{1}{30\text{K}\Omega}$.

This will generate a total transconductance of $\frac{1}{0.6\ \text{M}\Omega}$ each from the inputs ofG_{m_5} and $G_{m_6}$to the output of SUM_4, as demanded by the model-based design, and listed as the final and refined values for the transconductances G_{m_5} and G_{m_6} in Table 6-2.

The G_{m_5} and G_{m_6} blocks do not require any gain-trim as opposed to the case for G_{m_7} and G_{m_8}.

The much more dominant effects of G_{m_7} and G_{m_8} on the gain accuracy overshadow such errors introduced by G_{m_5} and G_{m_6}. Further the gain-error trim circuitry within G_{m_7} and G_{m_8} is compensating for the over-all gain inaccuracies for the whole amplifier. Detailed simulation results out of the scope of this writing have confirmed the above.

As much as the gain inaccuracies of G_{m_5} and G_{m_6} are irrelevant on the gain accuracy performance, their offsets have a profound effect on the offset performance of the instrumentation amplifier, as their inputs are directly connected to the inputs of the amplifier itself. This why they need their own compensation loop as has been discussed in prior sections.

The loop of $G_{m_{12}}$ and $G_{m_{10}}$ is used half of the times to correct the offset of G_{m_5} and G_{m_6} through the connection of $G_{m_{10}}$ outputs to the bodies of the NMOS device MN415, and MN416 within SUM_4. This is similar to the connections of G_{m_3} outputs to the bodies of MN215 and MN216 in SUM_2 as described previously, therefore SUM4 circuitry is not presented.

The DPDT switch MUX1 for half of the time redirects the output of the summing circuit SUM_4 to the chopper CH_2, and the other half to the inputs of the integrator G_{m_9} with a frequency of exactly one half of the chopper frequency.

The chopper frequency can be selected to be either 10kHz or 45kHz through trim options in the oscillator circuitry.

The G_{m_5} / G_{m_6} blocks, similar to G_{m_7} / G_{m_8} blocks are biased by a zero TC reference current as opposed to PTAT to keep the span of the voltage across their degeneration resistors relatively constant and independent of the temperature range as is the case for G_{m_7} / G_{m_8}.

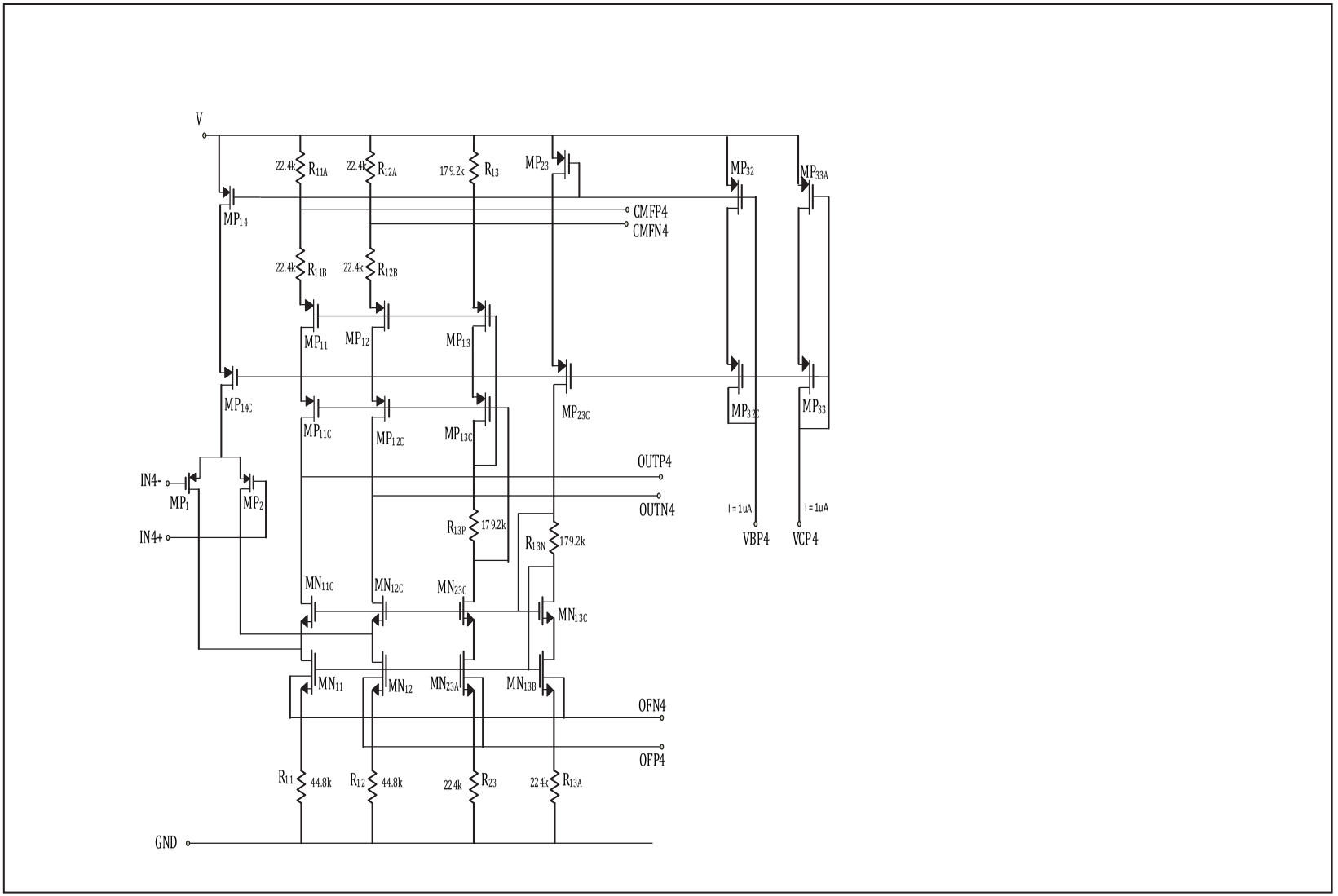

Figure 6-20 – Transistor-level design of the Integrator block G_{m_4} presented in the Model-Based Design of figure 6-3

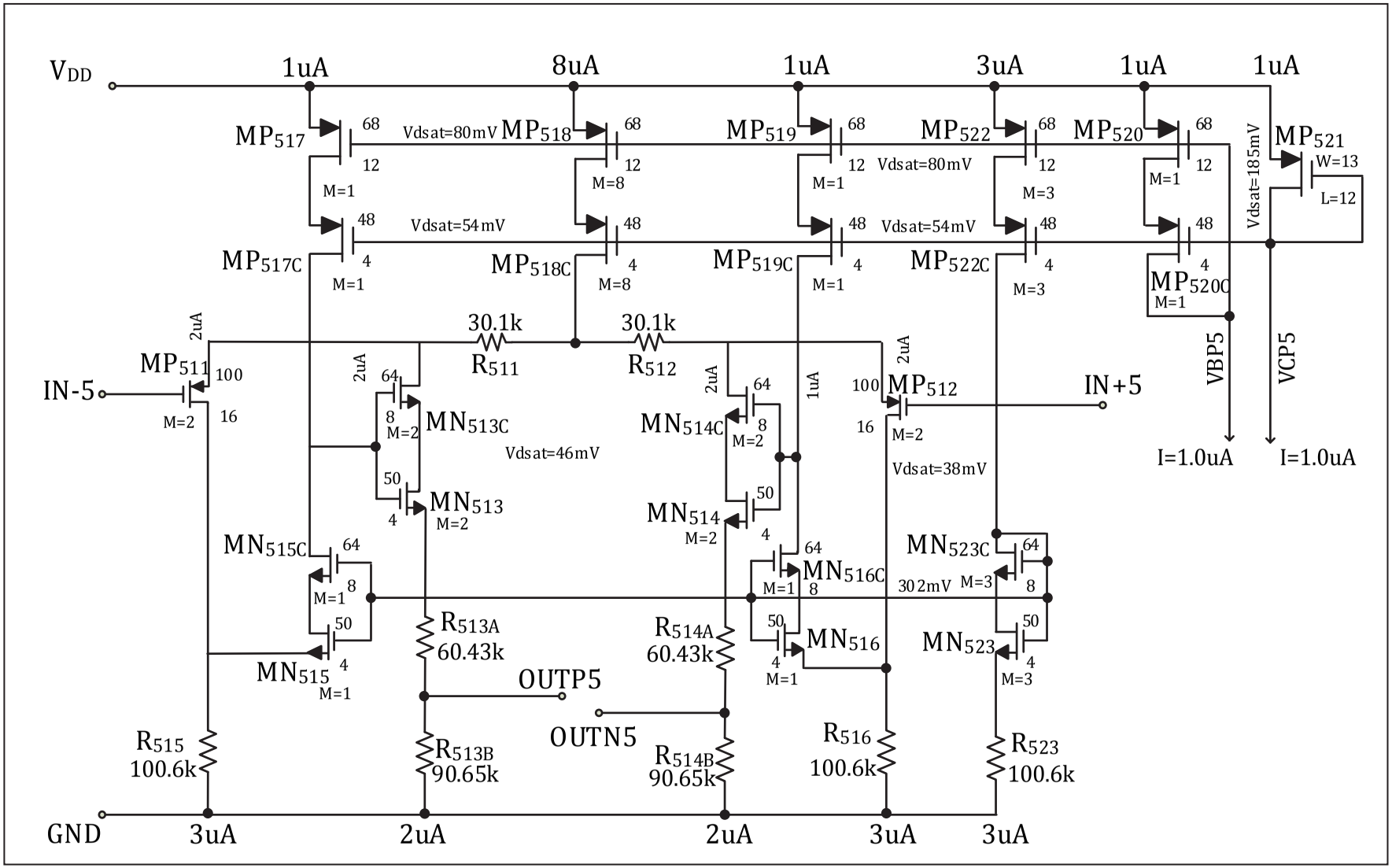

Figure 6-21 – Transistor-level design of the blocks G_{m_5} and G_{m_6} presented in the Model-Based Design of figure 6-3

6.5.8 Transistor-Level Design of the Summing Circuits SUM_2 and SUM_4

Both SUM_2 and SUM_4 have three differential inputs and one differential output. The block-level representations of these summers are shown in figure 6-22.

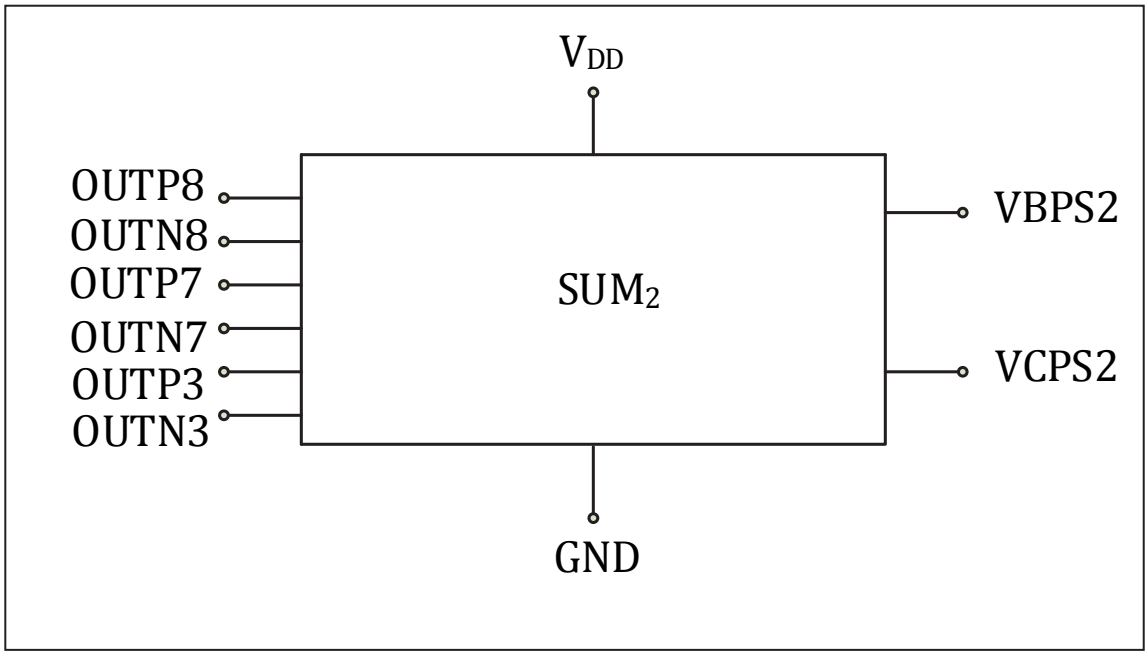

Figure 6-22 – Simplified Block-Diagram Representations of the Summers SUM_2 (SUM_4 is very similar)

The transistor-level schematic of these similar blocks is shown in figure 6-23. The circuit has two pairs of differential inputs taking the outputs of G_{m_5} and G_{m_6}, summing them up at mid-points of the degeneration resistors R415A/R415B, and R416A/R416B located at sources of MOS devices MN415C and MN416C. The third input takes the $G_{m_{10}}$ outputs and connects them to the bodies of the same MOS devices. These together, comprise the three differential inputs to the summer circuit. The resistor dividers in the path of the signals as well as the $g_{mb_{N415}}$ and $g_{mb_{N416}}$ will set the output to input transfer function of the block.

The resistor networks and biases are set in a way that they eventually provide the over-all transconductances needed from the inputs of G_{m_5} / G_{m_6} to the inputs of G_{m_4}(SUM_4), or the inputs of G_{m_3} to the outputs of G_{m_7} / G_{m_8}. These values have already been established by the model-base design presented in Table 6-2. Here the circuit implementation makes sure to get as close as possible to these predetermined values with some final refinements through simulation tools.

The common-mode at the output of these summers is determined by the gate-source voltage of PMOS devices MP417B and MP418B, along with the drop across their source degenerations resistors. The typical Output common-mode for these summer circuits is $V_{DD} - 1.2V$.

The currents in all branches are 0.2μA. Cascode devices make use of the effective combination of low threshold / normal threshold MOS devices, setting the typical supply voltage needed for this summing circuit as low as 2V.

6.5.9 Transistor-Level Design of the Weak Transconductance G_{m3}

Figure 6-24 shows the transistor level schematic of G_{m_3}. The circuit is simply a differential source follower, with resistor dividers of the ratio 17/1. This circuit acts as a buffered voltage divider. The input to this device comes from the integrator G_{m_4} , and the output is directed to the summer circuit SUM_2. As mentioned before, this buffer is also part of the common-mode circuit of the previous stage, that is the integrator G_{m_4}through the loops of gate to drain of the source followers. The drains of the source followers within this circuit are connected to the summing points at the upper cascode within the G_{m_4}.

All the branch currents are set to 1μA. All the transistors are low threshold MOS devices to achieve the required input common-mode voltage of about 1.4V.

The large source degeneration resistors and their current division at the output of this circuit help achieve the extremely over-all low transconductance needed for the operation of such blocks..

6.5.10 Transistor-Level Design of G_{m10}, G_{m13}, G_{m19}, G_{m22}, and G_{m24},

All of the above weak transconductances have similar architectures and at times same circuits as the one described for G_{m_3}block. As such, no further discussion on these blocks is needed.

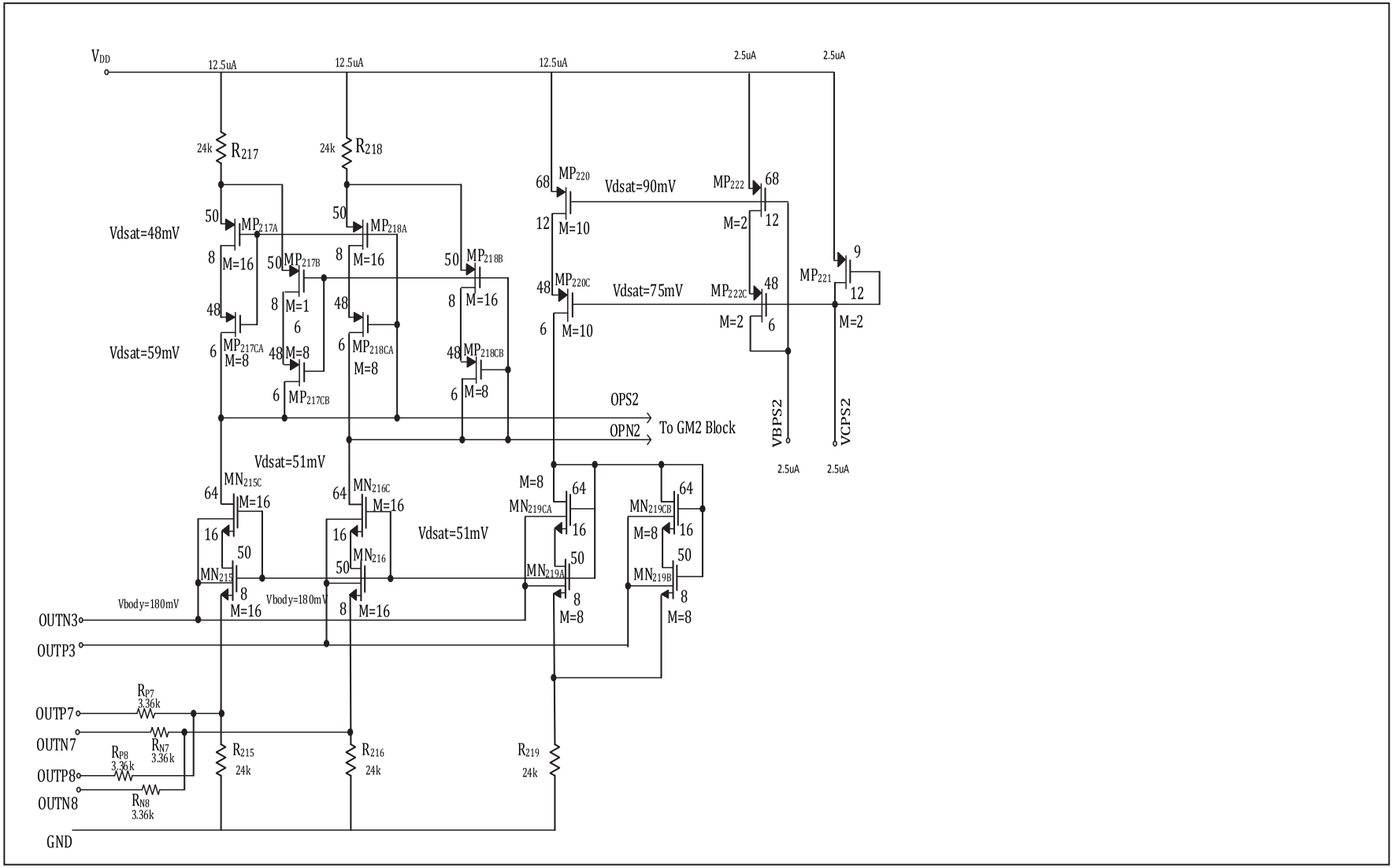

Figure 6-23 – Transistor-Level Schematic of the Summer Circuit SUM_2 (SUM_4 is similar), None are shown in figure 6-3 for simplicity

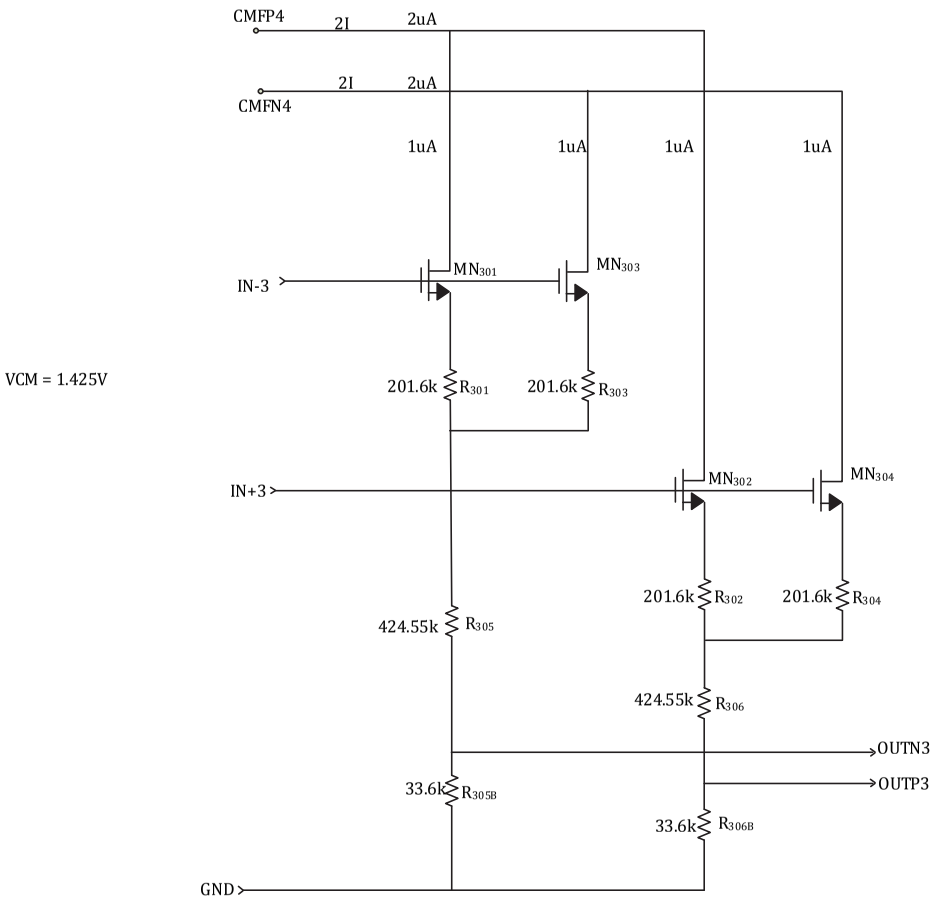

Figure 6-24 – Transistor-Level Schematic of the Weak Transconductance G_{m_3}

6.5.11 Transistor-Level Design of the Bias Circuitry (Simplified)

There are multiple bias circuits within this design. Both reference (zero TC) and PTAT biasing circuits are employed to feed different blocks of this chip as suitable.

Figure 6-25 shows the simplified schematic of the reference (zero TC) current generator bias circuit [36]. The PTAT generator core is made of the PNP devices Q_1 to Q_4, with Q4 selected as a 4X device. Writing the familiar V_{BE} loop equation, and keeping in mind that $I_{C1} = I_{C3}$, $I_{C2} = I_{C4}$, and I_{S2} equals four times the $I_{Sx;\,(x=1,3,4)}$, we obtain:

$$V_T \ln 4 \approx 36\ \text{mV} = I_{PTAT}\, R_{PTAT}$$

Also:

$$\frac{V_{BE1}}{R_{CTAT}} + \frac{V_T \ln 4}{R_{PTAT}} = I_0 = I_{Ref}$$

$$\frac{d/dT(V_{BE1})}{R_{CTAT}} + \frac{d/dT(V_T \ln 4)}{R_{PTAT}} \approx 0$$

With a reasonable estimation of $\frac{d}{dT}(V_{BE1}) = -2\ \text{mV/°C}$:

$$R_{CTAT} = 16\, R_{PTAT}$$

Using this last equation into the I_{Ref} equation, and For a Reference current of $I_{Ref} = 7.5\ \mu\text{A}$ we obtain:

$$R_{CTAT} \approx 170\ \text{k}\Omega$$

$$R_{PTAT} \approx 10.6\ \text{k}\Omega$$

$$I_{CTAT} \approx 4.1\ \mu\text{A}$$

$$I_{PTAT} \approx 3.4\ \mu\text{A}$$

$$I_0 \approx 7.5\ \mu\text{A}$$

Resistor R_{CAS} is to bias the cascode line. It is value for a rational value of $V_{dsat_{MN}} \leq 200\ \text{mV}$ is estimated to be:

$$R_{CAS} \approx 26.7\ \text{k}\Omega$$

Several current sources are derived from this bias line, which have been omitted for simplicity.

This reference current bias feeds the high accuracy V-I blocks of G_{m_7}, G_{m_8}, G_{m_5}, and G_{m_6}, in addition to the two summing blocks of SUM_2 and SUM_4.

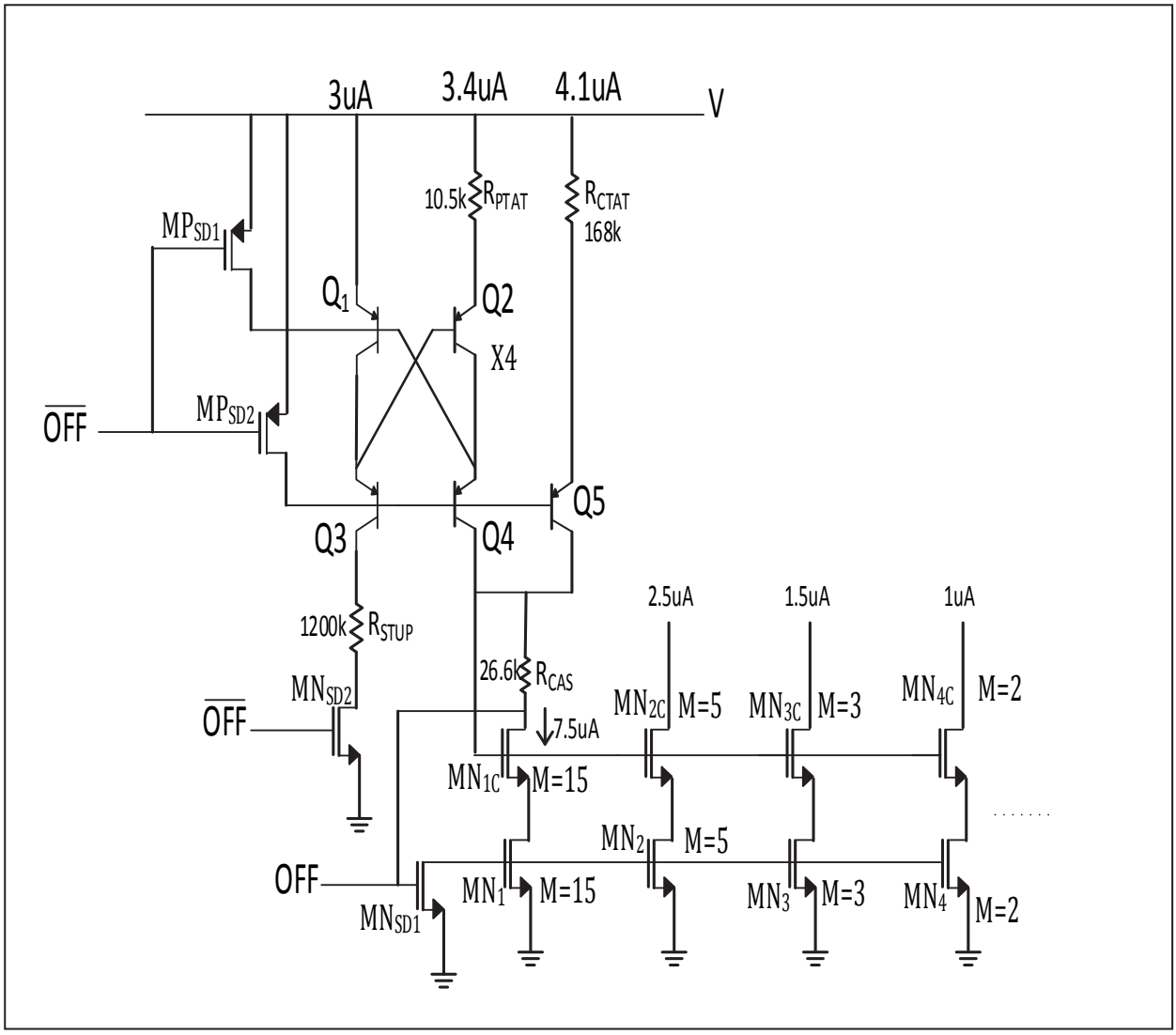

Figure 6-25 – Simplified Schematic of the Reference (Zero TC) Current Bias Circuitry

6.5.12 Transistor-Level Design of the Oscillator Circuit (Simplified)

Lastly, a simplified schematic of the oscillator circuit to generate the clocks for driving the choppers and multiplexers is presented in figure 6-26.

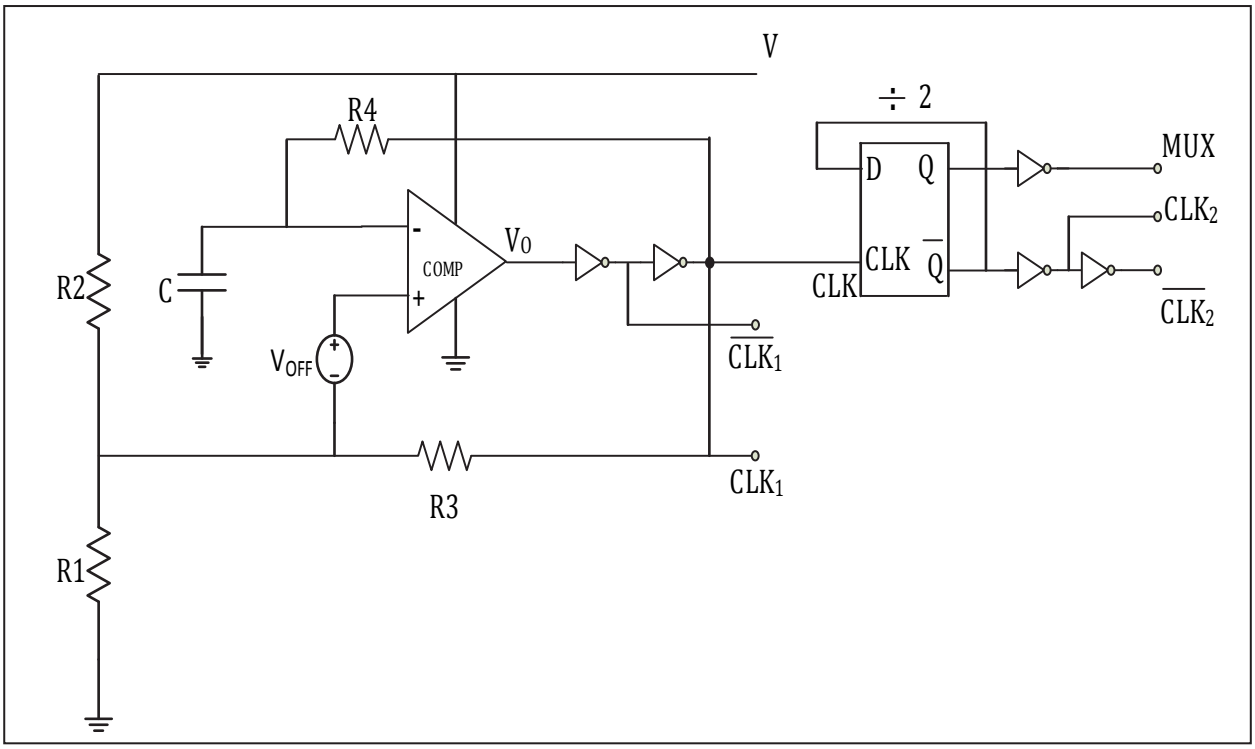

Figure 6-26 – Simplified Schematic of the Main Oscillator Circuitry

The heart of the oscillator circuitry is a relaxation oscillator tailored to work off of a single supply. The comparator within the circuit should be an output rail-rail type to assure a square output voltage with an output at the two levels of V_{SS} and V_{DD}. Addition of inverters could guarantee this, even if the comparator has small head-rooms to the rails. Also the inverters supply the complementary clock signals needed to drive the switches. A divide-by two circuit (just a Flip-Flop) is used to divide the frequency down for MUX switches.

The operation of the circuit is trivial and is not discussed. However the selection of the thresholds (trip point of the comparator) is critical if the operation at minimum V_{DD} over the process variations and temperature range has to be guaranteed.

The higher trip point is set by the ratio $R_1/(R_1 + R_4 \parallel R_2)$, and the lower one by the ratio $(R_4 \parallel R_1)/(R_2 + R_1 \parallel R_4)$. These limits are some voltages between the supply rails, which must

be carefully picked based on the type of the input stage (PMOS or NMOS), and their V_t values.

The followings should hold through for a proper design:

$V_{DD} - (V_{GS_P} + V_{dsat_P}) \geq V_{DD}\,(R_1/(R_1 + R_4 \parallel R_2)$ For PMOS input Comparator, and:

$V_{SS} + (V_{GS_N} + V_{dsat_N}) \leq V_{DD}(R_4 \parallel R_1)/(R_2 + R_1 \parallel R_4)$. For NMOS input Comparator

If a PMOS input comparator is used, a regular V_t MOS will severely limit the higher threshold voltage setting at low supply voltages. The sum of the saturation voltages of the comparator's tail current (≈ 0.15V), plus the process worst case V_t value for PMOS (≈ 1V), in addition to the extra V_t demand at cold (65°C x 2mV/ °C = 130mV), will add up to about 1.3V. In a 2.7V supply, this is almost half of the supply budget; therefore low V_t devices are preferred in such cases as has been followed throughout the work of this thesis.

It can be shown that for $R_3 = R_4 = R/2$; the higher and lower thresholds are $\frac{3}{4}\,V_{DD}$, and $\frac{1}{4}\,V_{DD}$ respectively. Moreover, the period (T) is independent of V_{DD}, and equal to $T = 2\,R\,C$.

Resistors R_3 and R_4 are chosen variable to function as trim-up and trim-down knobs to adjust the oscillator's frequency. Much about the trim network design has already been discussed in sections 6.5.5.2 and 6.5.5.3., therefore no further discussion is needed.

6.5.13 Simulation Results for the Transistor-Level Design of CFIA

AT this point it makes sense to compare the simulation results of the transistor-level design of this thesis to those of the model-based design presented in section 6.4.5. Here, in figure 6-27, we first show the most important simulation result of this work which is the over-all offset cancellation action of the whole design as a system. The gain of the Inst-Amp is set to ten, and the SPICE models are all "Typical" models. Furthermore, the simulation is performed at room temperature. This is the exact counterpart of figure 6-6, of the model-based design presented in section 6.4.5. The results of the simulation in figure 6-27 shows an input referred ripple of +/- $10\mu V$, and spikes of +/-50 μV after 15ms.

Figure 6-28 shows the performance of the above Inst-Amp when the SPICE models are all "Fast" models, and the temperature is elevated to +125°C(hot). The Design demonstrates a solid performance, with a ripple of +/-30 µV after 30ms. The spikes are observed to be +70 µV / -40 µV.

Figure 6-29 demonstrates the performance of the same design at -40°C (cold), with all the SPICE models set to "Slow" models. The outcome is an input referred ripple of +/-10µ V, and spikes of +50 µV / -20 µV.

In both pictures mentioned above, the offset removal is happening throughout many chopper clock cycles as expected. The similarities of the results between the model-based simulations, and the transistor-level design counterparts are not accidental. This is a strong evidence to prove the validity of the top-down model based design approach.

As the last simulation graph for the transistor-level design of this thesis, we show in **Error! eference source not found.** that the Bode-Plots of magnitude and phase perfectly meet the design requirements of BW $\geq$ 750 kHz, and PM $\geq$ 60 deg.

6.5.13.1 Comparison between the Simulation Results of the Model-Based Design and the Transistor-Level Design

Finally we complete the Table 6-5 of section 6.4.5 by adding the analogous simulation results of the transistor-level design of this subsection as shown in Table 6-8.

Simulation Results	Design Approach	Intentional V_{os}	Gain	R_L/C_L
$V_{rip_{in_{pp}}} = +/-15\mu V$ $V_{spikes} = +20\mu V / -140\mu V$	Model-Based Temp. = 25°C	10mV for All G_m's	10	1kΩ/100pF
$V_{rip_{in_{pp}}} = +/-10\mu V$ $V_{spikes} = +50\mu V / -50\mu V$	Transistor-Level Temp. = 25°C	10mV for All G_m's	1	1kΩ/100pF

Table 6-8 – Comparison of final Simulation Results for the Model-Based Design vs. the Transistor-Level Design of figure 6-3

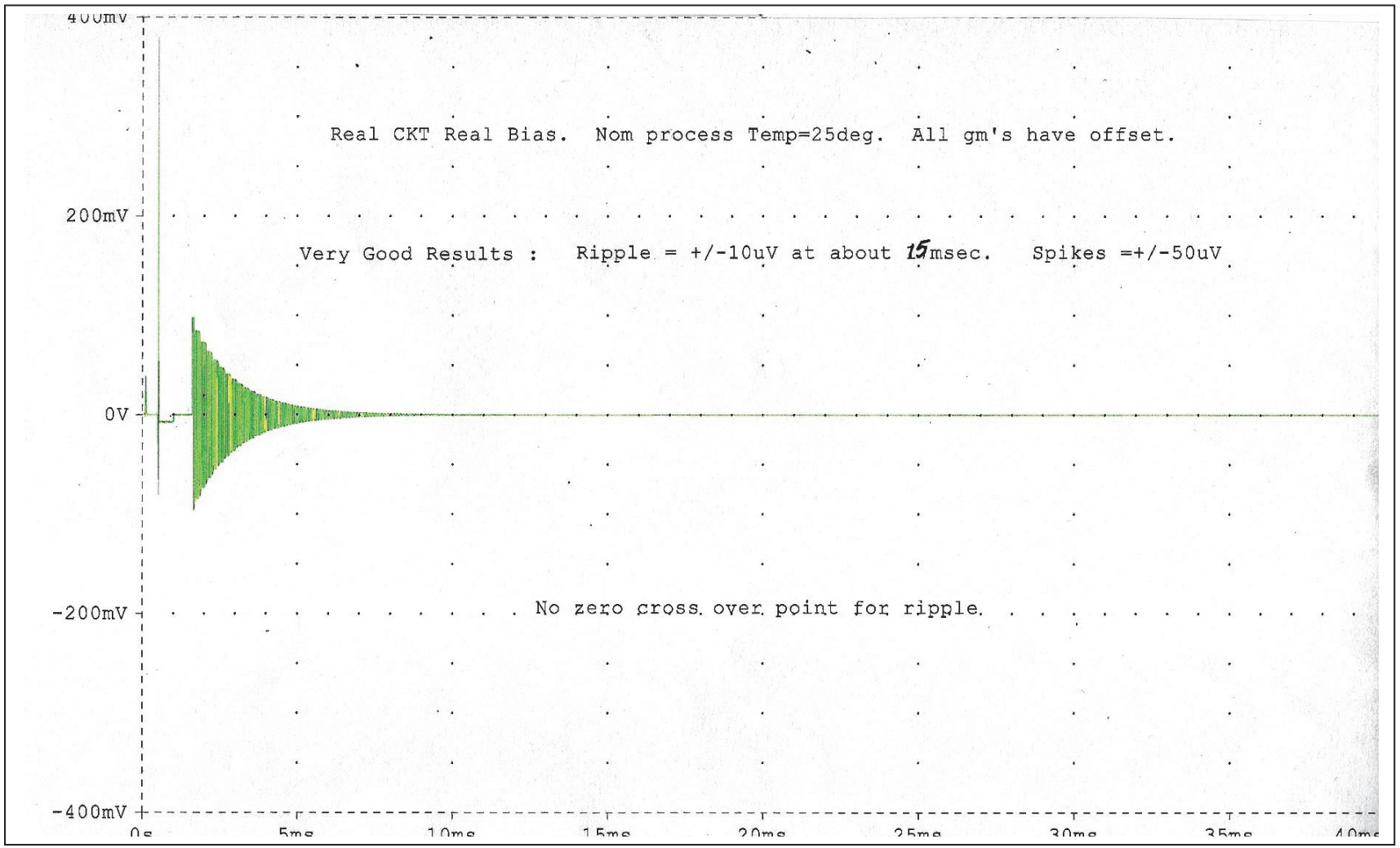

Figure 6-27 – An informative Picture Showing the Simulation Results of the Transistor-Level Design which is the counterpart of figure 6-6 shown for the model-based design. This is for 25°C and Nominal Process, with Real Clock Circuit as opposed to Ideal Clocks.

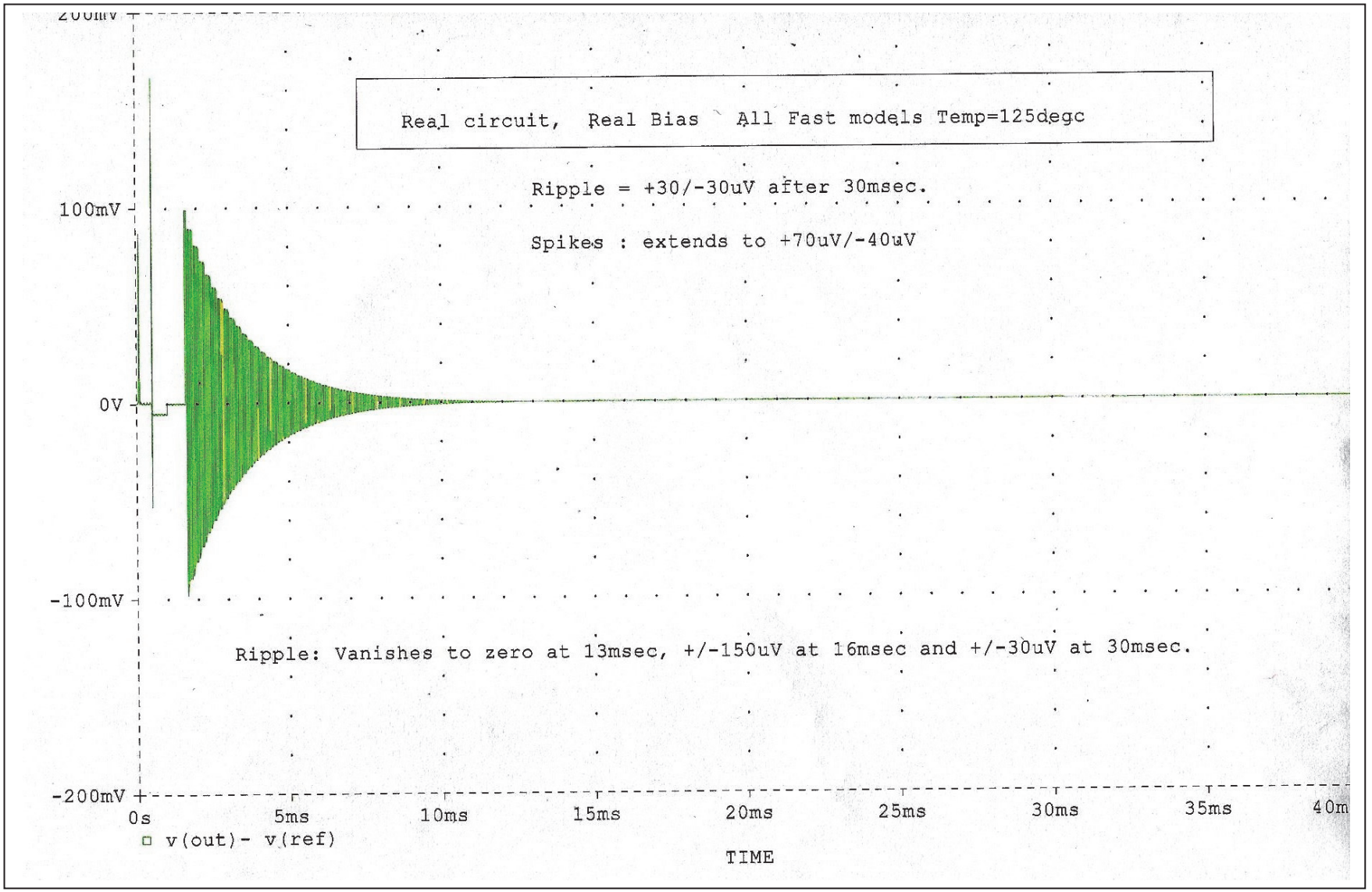

Figure 6-28 – Simulation Results of the Transistor-Level Design of figure 6-27 for "Fast" SPICE Models at +125°C

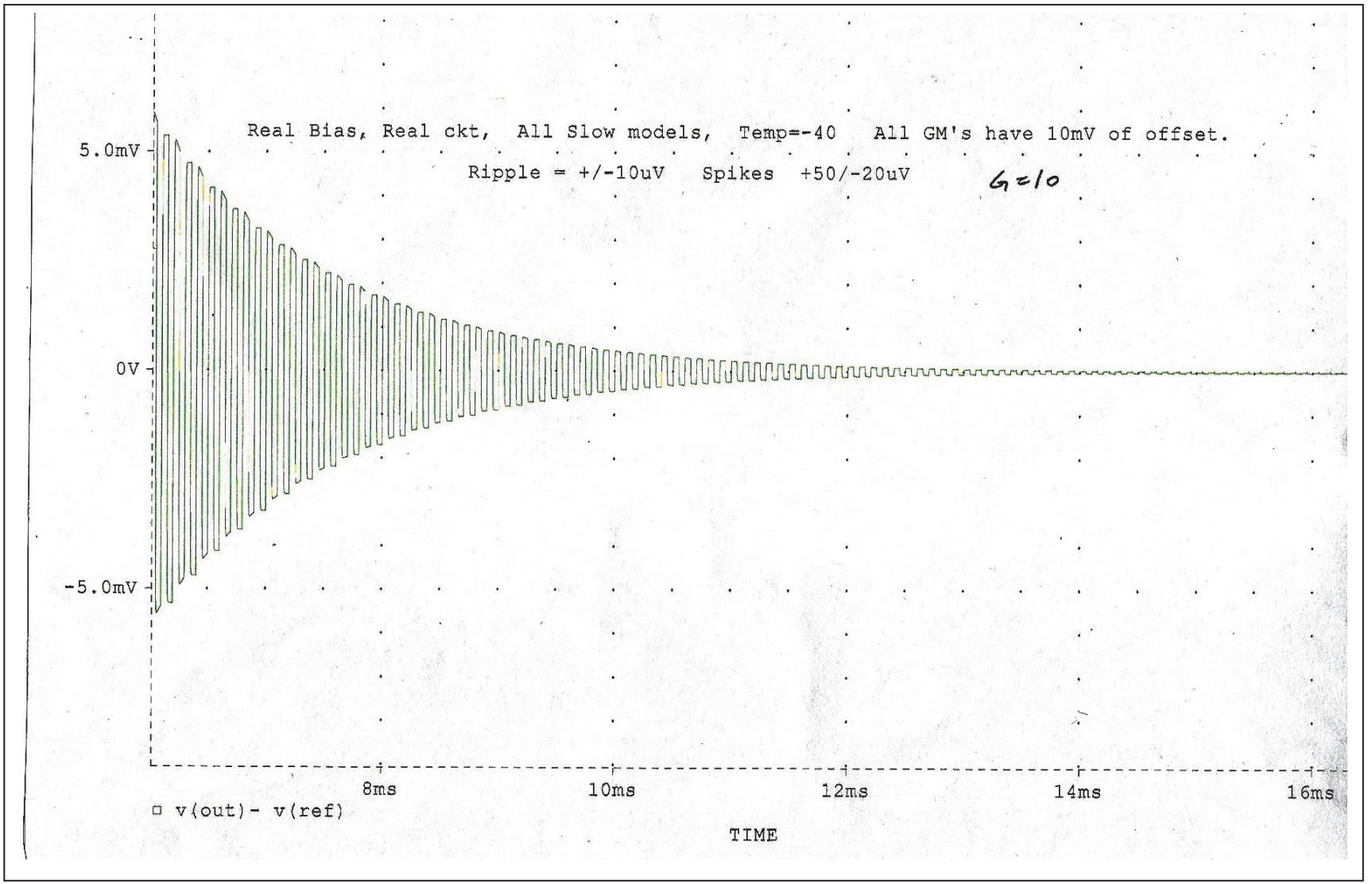

Figure 6-29 – Simulation Results of the Transistor-Level Design of figure 6-27 for "Slow" SPICE Models and -40°C

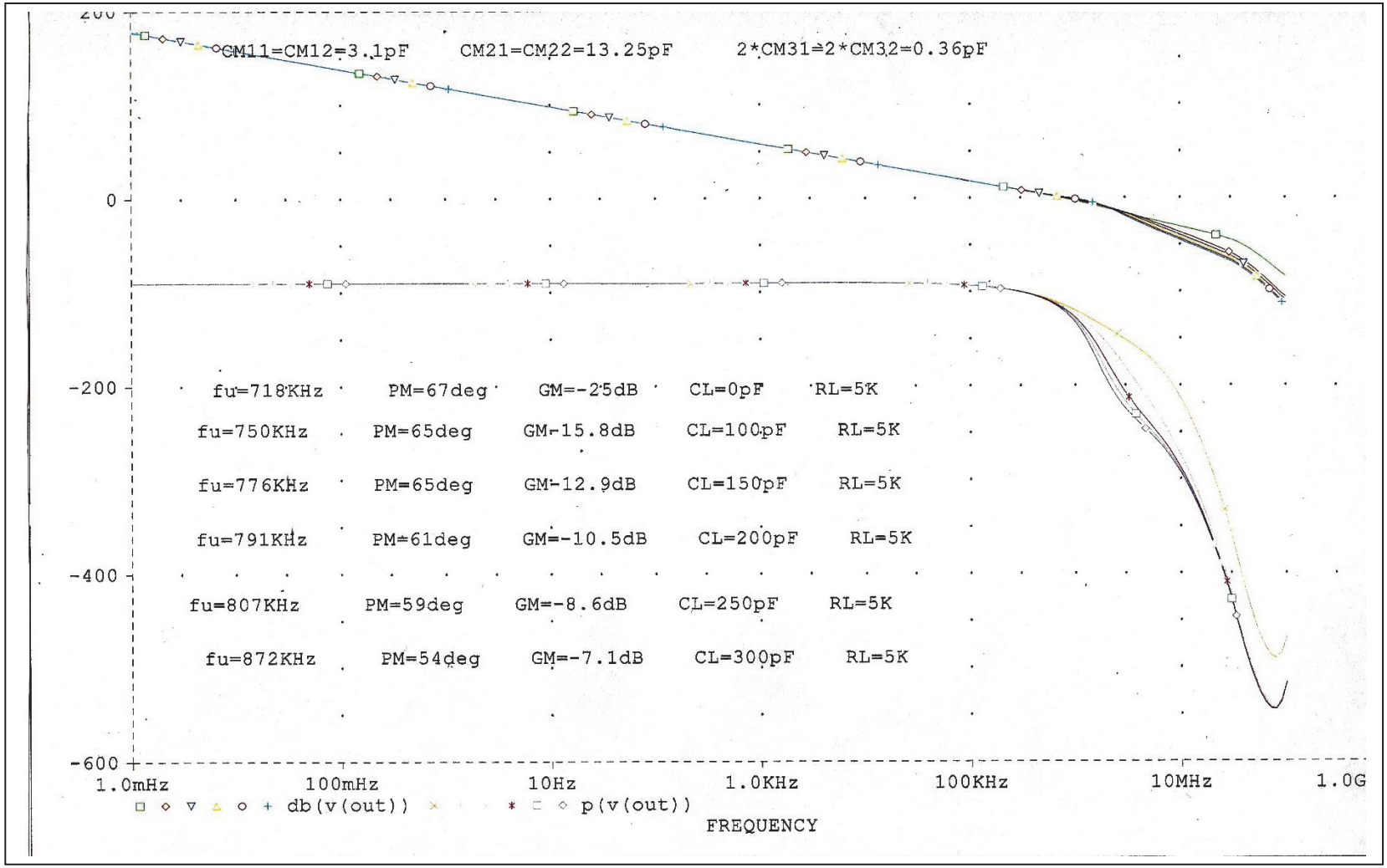

Figure 6-30 – Bode-Plots of the Transistor-Level Design of this Project as a Function of the Load Capacitance. The Design is Stable with Load Capacitances Much Higher than the Target Specification of C_L=100pF. The Phase Margin is 65deg for C_L=100pF.

6.6 Measurement Results

In this section we present the silicon measurement results, as well as some statistical data taken on large samples. Accuracy parameters, i.e. Offset, Gain-Error, and linearity are the most important parameters of closed-loop gain blocks.

Most precision analog applications are at DC or low frequencies. Therefore other DC parameters of interest such as Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are also considered critical parameters in such applications.

The following tables list the measured data on some of these parameters.

6.6.1 Input-Referred offset for Model-Based Simulations, Transistor-Level Simulations, and Silicon Measurements

First we represent the input-referred offset since in most application it is considered the most dominant error as discussed in 2.2. In doing so we revisit table 6-8, however we add the measured silicon results to the table.

Results	Simulated /Measured	Forced Offset	Gain	R_L/C_L
$V_{rip_{in_{pp}}} = +/-15\mu\, V$ $V_{spikes} = +20\mu V\ /\ -140\mu\, V$	Model-Based Simulation. Temp. = 25°C	10mV for All G_m's	10	1kΩ/100pF
$V_{rip_{in_{pp}}} = +/-10\mu\, V$ $V_{spikes} = +50\mu V\ /\ -50\mu\, V$	Transistor-Level Simulation. Temp. = 25°C	10mV for All G_m's	10	1kΩ/100pF
$V_{off_{in}}(DC) \approx 0.3\mu\, V \sim\ 6\mu\, V$	Silicon Results. Temp. = 25°C	N/A (Random)	10	1kΩ/100pF

Table 6-9 – Input-Referred offsets showing Simulation Results for the Model-Based Design, Transistor-Level Design, and the Silicon Measurements.

6.6.2 Bench Measurements of the Accuracy , DC, and AC Parameters

Next we tabulate important accuracy, DC, and AC parameters of two devices measured on the bench.

6.6.2.1 Accuracy Parameters

Parameter	SN1	SN2	Unit
Input-Referred Offset	-0.29	6.1	µV
Gain-Error	0.005	0.01	% FSR
Linearity-Error	0.01	0.01	ppm
CMRR	138	133	dB
PSRR	118	111	dB

Table 6-10 – Measurement Results on Accuracy Parameters for 2 Units Tested at Room

6.6.2.2 DC Parameters

Parameter	SN1	SN2	Unit
IDD @ 5V	719	754	µA
V_{OH} ; RL=100K	0.20	0.20	mV
V_{OH} ; RL=10K	1.09	1.14	mV
V_{OH} ; RL=1K	9.37	9.94	mV
V_{OL} ; RL=100K	0.48	0.18	mV
V_{OL} ; RL=10K	0.90	0.78	mV
V_{OL} ; RL=1K	6.7	6.95	mV

Table 6-11 – Measurement Results on DC Parameters for 2 Units Tested at Room

6.6.2.3 AC Parameters

Parameter	SN1	SN2	Unit
Bandwidth	760	810	kHz

6.6.3 Histograms of Accuracy Parameters

The histograms of accuracy parameters for a sample of 300 units tested by Automatic Test Equipments (ATE) showed solid results for this design.

6.6.3.1 Input-Referred Offset Voltage Histogram

The tester results of the measured input-referred offset for 300 units are graphed in the histogram of figure 6-31. The histogram shows that about 98% of the units have an offset voltage between -6μV to +4 μV. The range of offset for the entire population is between -8 μV to +4 μV.

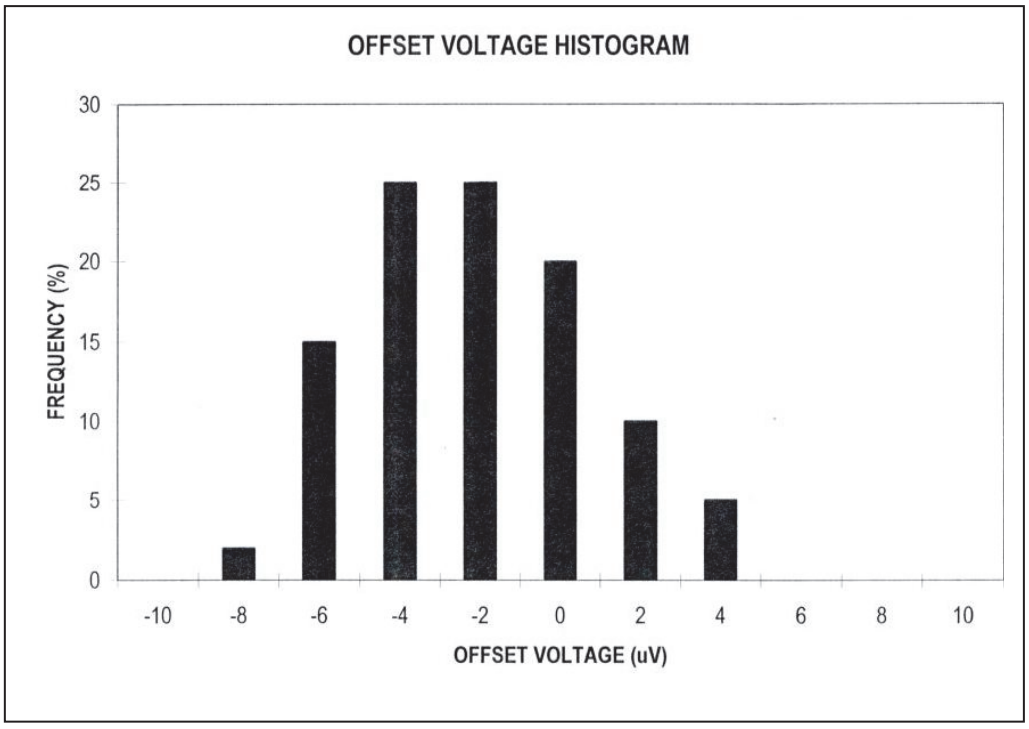

Figure 6-31 – Histogram of Input-Referred Offset Voltage for 300 Units Tested by the Final Test (FT) Program Using Automatic Test Equipments (ATE)

6.6.3.2 Gain Error Histogram

Figure 6-32 shows the histogram of the Gain-Error for the same units as in figure 6-31. The results show a distribution for this parameter between the range of -0.04% to +0.06%. However about 85% of the units show Gain-Errors values of less than 0.02%.

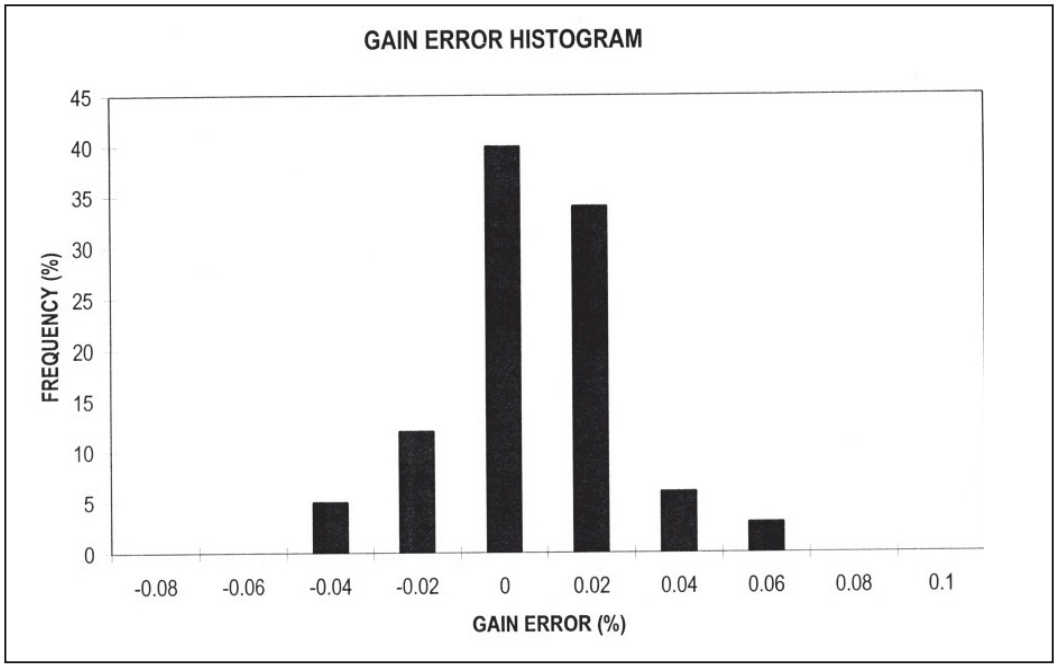

Figure 6-32 – Histogram of Gain Error for 300 Units Tested by the Final Test (FT) Program Using Automatic Test Equipments (ATE)

6.6.4 Bench Measurement Results Showing Typical Operating Curves (TOC's) for Offset vs. Input Common-Mode and Supply Voltages

In the following section we present some typical operating curves showing the changes in the input-referred offset with the changes in the input common-mode or power supply voltages.

The above are in fact the indicative of the typical values for the known parameters Common Mode Rejection Ration (CMRR), and Power Supply Rejection Ratio (PSRR) for the design.

Approximate estimations from the graphs indicate typical values of CMRR and PSRR of about 126dB and 110dB for these measured units respectively.

6.6.4.1 Input-Referred Offset vs. Input Common-Mode Voltage

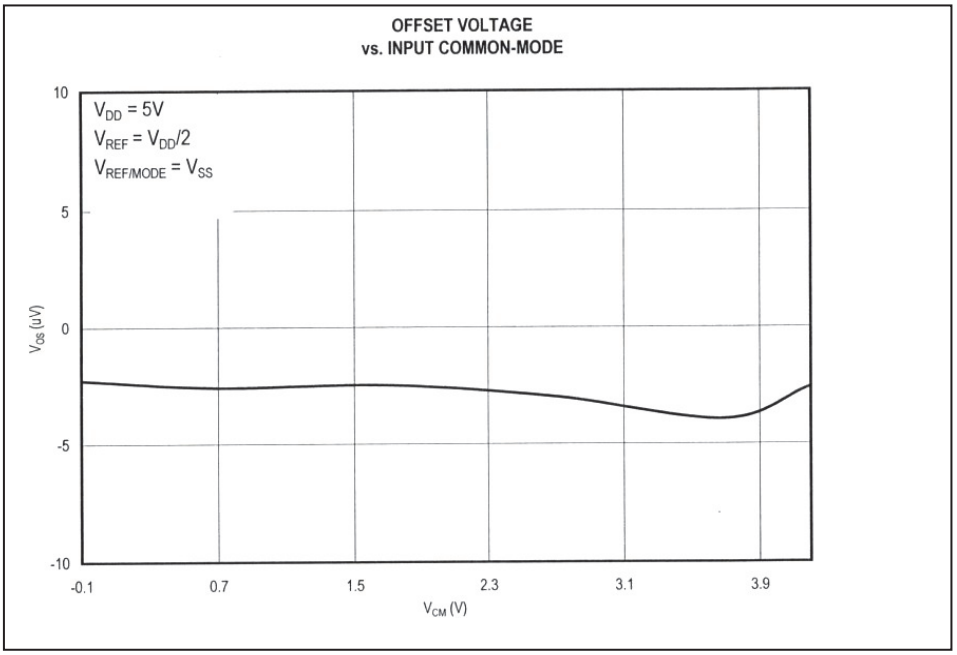

Figure 6-33 – Variations of the Input-Referred Offset with the Input-Common Mode Voltage

6.6.4.2 Input-Referred Offset vs. Supply Voltage

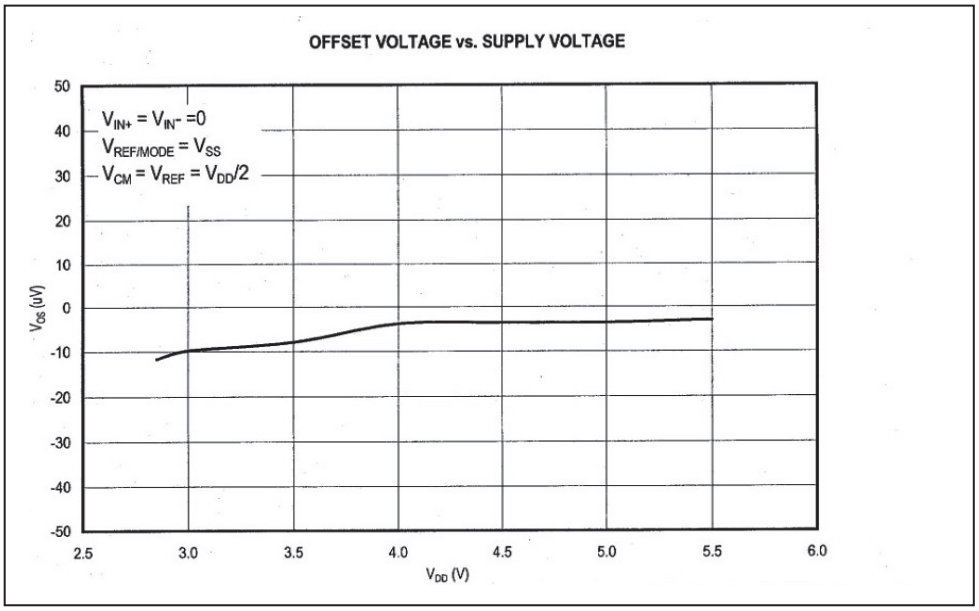

Figure 6-34 –Variations of the Input-Referred Offset with the Supply Voltage

7. Conclusions and Improvements

The work of this thesis to enhance the performance of Operational and Instrumentation amplifiers is mainly described in chapters five and six. The previous chapters are represented as background and to show the other techniques as prior art in order to demonstrate the need for improvements.

The concepts are described in simple and straightforward language. However, when required, mathematical derivations are presented to assist establish the concept.

7.1 Conclusions

This thesis describes “High Performance Operational and Instrumentation Amplifiers” using the patented [15] “Chopper Chopper-Stabilized Instrumentation and Operational Amplifiers " Technique described in section 5.2.6.

The Technique is applicable to both Operational and Instrumentation amplifiers. However, the topology chosen for discussion in this thesis is “Current Feedback Instrumentation Amplifier” or CFIA topology simply because the CFIA is just an Op-Amp with two input stages.

CFIA topology is the easiest way to build an Instrumentation Amplifier with Operational Amplifiers. The work of this thesis is the first in class to apply the above patented technique with CFIAs, to significantly enhance their performance.

In addition, to further improve the accuracy performance, a patented [35] “Accurate V-I converter for rail-sensing Current-Feedback Instrumentation Amplifiers” is also presented and applied, thoroughly described in section 6.5.4.

Lastly, improvements on frequency characteristics of the multi-path hybrid nested Miller compensation used within the design of the thesis are made by applying the patented technique [13] described in section 5.4.10.

In parallel with the discussions on the main topic of the thesis, the importance of top-down model based design has been discussed and emphasized. Moreover, the model-based design predictions of the performance characteristics of the design associated with this thesis have been demonstrated, compared with their transistor-level counterpart, and finally confirmed by the results from silicon. .

New gain setting options in CFIA design for wide range gain settings, as well as their trim considerations are discussed in sections 6.5.5.1 through 6.5.5.6.

As far as end results are concerned, the following measurements have been observed:

The input-referred offset has an extremely low value in the range of 0.3μV to 6μV. Furthermore, the CMRR measured around 130dB. Moreover, the PSRR shows an average of 110dB. Accuracy specifications such as gain-error and linearity-error were measured about 0.01%.

Lastly we summarize the improvements offered by this new design over the conventional methods.

7.1.1 Improvements Offered by the Chopper-Stabilized Auto-Zeroed Chopper Inst-Amps

Now it is beneficial to look at the overall performance improvements offered by this new "Chopper-Stabilized Auto-zeroed Chopper" technique. A Chopper-Stabilized Auto-zeroed Chopper Inst-Amp will overcome the majority of issues with conventional choppers, and Three Op-Amp Inst amps discussed in 5.2.1.1 and 1.2 , thanks to its inherent built-in offset removal method. Summarizing few advantages of this technique:

i. Compared to the Conventional Chopper Inst-Amps topology:

Chopper-Stabilized Auto-zeroed Chopper Inst-Amps do not need any filtering after the second chopper (the demodulating). This is due to the fact that the offset is practically eliminated as opposed to being modulated at the chopper frequency, and seen as a ripple with the amplitude of the original offset error referred to the input. This is the case for the Conventional Choppers if no filtering is used.

If the offset and low frequency noise were to be eliminated before the Demodulator in the first place, there would have been no need for a low-pass filter for removal of the associated ripple.

With the new technique, the residual offset is practically eliminated before the second chopper, as it is orders of magnitude lower than that of a conventional chopper at the same point in the circuit. With no such filtering, the band-width of the amplifier is preserved, as in the case of non-chopper designs.

Lower input-referred offset means less interaction with the input parasitic capacitors of the first chopper and the signal-path resistors, therefore lower residual offset or input-referred ripple results. A skew in the clocks to the choppers, or a deviation in duty cycle is now significantly less pronounced.

Charge injection effects are inherent to all switching circuits. However spikes may be reduced by additional measures.

ii. Compared to Three Op-Amp Instrumentation amplifier Architecture:

Unlike the Three Op-Amp topology (see Figure 1-5) the Chopper-Stabilized Auto-zeroed Chopper Inst-Amp can sense up and down to the supply rails. In particular, with P-type devices

at the input, the architecture is capable of sensing the GND rail, which is desirable in many power-management and current-sensing applications.

iii. In contrast to the untrimmed Three Op-Amp Inst-Amp, the Chopper-Stabilized Auto-zeroed Chopper design can achieve extremely higher values for CMRR (above 130dB) due firstly to lack of the need for a precisely balanced bridge and to a much lower offset and offset variation over its input common mode range.

The Chopper-Stabilized Auto-zeroed Chopper Inst-Amp takes less area as it doesn't need any operational amplifiers with extremely high performance in its structure. This is possible due to the act of chopping, chopper-stabilizing, and Auto-zeroing built-in to the design.

Often the noise performance of a Chopper Stabilized Auto-zeroed Chopper Inst-Amp is better than its 3-Op-Amp counterpart, due to real-time noise cancellation for very low frequencies and to lower component counts at the input stage of the amplifier for white noise. The latter doesn't always hold true and depends on the actual design construction and choices of components.

The design of this thesis is based on patented techniques [13], [15], [35] for a new product introduced to the market by Maxim Integrated Products. The design was awarded "The Most Innovative Instrumentation Amplifier" by EN-Genius NETWORK at market introduction in 2008.

List of Patents

J. H. Huijsing, M.J. Fonderie and **B. Shahi** "Frequency Stabilization of Chopper-Stabilized Amplifiers", Publication Number: US 7209000; Publication Date: Apr 24, 2007.

J. H. Huijsing and **B. Shahi** "Accurate Voltage to Current Converters for Rail-Sensing Current-Feedback Instrumentation Amplifiers", Publication Number: US7202738B1; Publication Date: Apr 10, 2007.

J. H. Huijsing, and **B. Shahi**, "Chopper-Stabilized Chopper Instrumentation and Operational Amplifiers", Publication Number: US patent Nr. 7132883 B2; Publication Date: November 7, 2006.

J. H. Huijsing and **B. Shahi** "GM-Controlled Current-Isolated Indirect-Feedback Instrumentation Amplifier", Publication Number: US 6559720B1; Publication Date: May 06, 2003.

J. H. Huijsing and **B. Shahi**, "Device with Common Mode Feedback for a Differential Output", Publication Number: US6118341A; Publication Date: Sep 12, 2000.

List of Early Publications

B. Shahi, "Practical Applications of transistors", Publisher: Honar Publications; Tehran Iran, 1980.

B. Shahi, "A Short Review of Electronic Tubes as Early Voltage Controlled Transconductance Amplifiers", Publisher: Tehran Technical Institute; Tehran Iran,1980.

Awards

The design architecture described in chapters five and six of this thesis was for the first time implemented in a family of products (MAX4208 / MAX4209) by the author at Maxim Integrated Products.

MAX4208 / MAX4209 were awarded "The Product of the Year" in 2008 by EN-Genius NETWORK under the category of "The Most Innovative Instrumentation Amplifier" .

About the Author

Behzad Shahi received his BSEE from Iran University of Science and Technology in 1978. From 1978 to 1984, he worked as an electronics instructor at several Technical Institutes in Tehran, Iran while consulting with various local and international companies in the area of communications and analog design.

Behzad received his MSEE from Santa Clara University, California in 1989.
Since 1987 he has worked at several integrated circuit manufacturers, such as Siliconix, Micro Power Systems, Signetics, Philips, Maxim, Freescale, and IDT in the areas of design, application, product development, and failure analysis of integrated circuits.

Behzad is currently working at Integrated Device Technology (IDT) in San Jose, California as a Sr. Director of Design and Technology Development within the CTO office. Prior to that, he has been the Sr. Design Director of Analog and Power Division (APD) within IDT.

Acknowledgements

It is the author's personal experience that pursuing a PhD degree and working as a full-time employee, are at times contradictory in nature and often difficult to manage.
Completing this task would have not been possible without the great guidance and help from my professors, and a number of my former and present managers and colleagues. Therefore a word of appreciation is sincerely due.

First and foremost, I would like to thank my first Promoter Prof. Johan Huijsing of Delft University. I started this Journey with Prof. Huijsing during my employment at Philips Semiconductor North America Division. I had the honor to be a PhD student under him for many years during which I learned a lot of fundamental concepts in precision analog design, particularly in the interesting and advanced area of high performance precision operational and instrumentation amplifiers.

Prof. Huijsing's great mentorship was not limited to just discussions of technical subjects, or some newly developed circuits, but also in regards to general approaches in design methodologies related to my own shortcomings as then a conservative designer.

I have also benefited from his generosity in sharing with me his own personal life experiences, especially when he thought I could learn from them. For all you have done for me, I sincerely appreciate you Prof. Huijsing.

Upon Prof. Huijsing's retirement in 2008, I was accepted as a PhD student by my current promoter Prof. Gerard Meijer. I should first truly appreciate his generous acceptance to honor me as his PhD student, and also for the fact that otherwise I had no alternative but refrain from the program.

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would have certainly had a very difficult time to finish the huge task with my own methods.

My colleague Sanjaya Maniktala is well known in the industry as a professional engineer and an excellent technical writer. However, none of us were aware that Sanjaya by himself is almost a complete publishing company altogether! I appreciate his generous assistance with a lot of Visio figures in this thesis which he did in his personal spare time.

I should also thank another colleague of ours at IDT for his help in English to Dutch translation of the original title page of this thesis. Although I must admit that by just looking at the Dutch text I have no clue what Anton Baker has written at the first page of my thesis, I am sure he has done a marvelous job for its purpose.

Last but certainly not the least I thank my wonderful family, wife Neda, and our daughters Nava, Ava, and Bita, for their patience and continuous caring and support throughout the entire program, and at the time of the writing of the thesis. Moreover, in addition to her continuous support and encouragement from the beginning, Neda has been instrumental in creating and managing many of the Visio figures within this thesis.

Thank you Neda, I love you and our three wonderful daughters for who you truly are, and I appreciate all the help and support all along.

Behzad Shahi
San Jose Ca, May 25, 2015

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List of Figures

Figure 1-1 – Instrumentation Amplifier in a Sensor Bridge and Display Chain 16

Figure 1-2 – Gain Block (Amp) in a typical Analog Controlled Closed-Loop System 17

Figure 1-3 – Instrumentation Amplifier in a Typical Digital Controlled Closed-Loop System....18

Figure 1-4 – Instrumentation Amplifier used in a common Microcontroller-Based Oven Temperature Control.....18

Figure 1-5 – The Three Op-Amp Topology 22

Figure 1-6 – Block View of Current Feedback Instrumentation Amplifier (CFIA).....25

Figure 1-7 – Basic Schematic of a CMOS Current Feedback Instrumentation Amplifier (CFIA)26

Figure 1-8 – Basic Schematic of a BJT Current Feedback Instrumentation Amplifier (CFIA) 27

Figure 1-9 – General Symbol for Current Feedback Instrumentation Amplifier (CFIA).....27

Figure 2-1 – Op-Amp in a Closed Loop Configuration with Errors Modeled as an Input Referred Source 33

Figure 2-2 – Real Op-Amp with a Non-Zero Output Voltage for a Zero Input Voltage.....34

Figure 2-3 – Real Op-Amp with Offset Compensation Bringing V_{out} to Zero (Definition of Offset Error Voltage).....34

Figure 2-4 – Offset Voltage of the Op-Amp Causes a Total Error in the Output Voltage as if There Exists a Gain Error in the Circuit 35

Figure 2-5 – Normal Distribution of Random V_T Mismatch Leading to Offset Error in Applications.....37

Figure 3-1 – Source Degeneration Trimming at Input Differential Pair 43

Figure 3-2 – Size Adjustment Trimming $\Delta W/L$ at Input Differential Pair.....44

Figure 3-3 – Offset Trimming at Source Degeneration Resistors of a Current Mirror Load 45

Figure 3-4 – Offset Trimming at Drain of Input Differential Pair through Load Adjustments.....46

Figure 3-5 – Offset Trimming by Addition of a Trimmable Current Source to One Side of a Differential Pair Load.....47

Figure 3-6 – Zener-Zap Trimming at Wafer-Sort.....48

Figure 3-7 – Trimming through Burning a Metal Link Fuse....48

Figure 3-8 – Trimming Thin Film Resistor at Wafer-Sort 49

Figure 3-9 – ROM Poly-Fuse Link in PPT and its Associated Mismatched Current Mirror Read Circuitry. Here $(W/L)_{M1} > (W/L)_{M2}$. The Out_Bit0 Changes from High to Low After the Trim 51

Figure 3-10 – ROM Poly-Fuse Link in PPT and its Associated Latch Read Circuitry....52

Figure 3-11 – Test Circuit to Measure Accuracy Errors in Inst-Amps....56

Figure 3-12 – Total Error Characteristics for an Inst-Amp with No Accuracy Errors (Ideal Inst-Amp)....56

Figure 3-13 – Total Error Characteristics for an Inst-Amp with Offset Error Only....57

Figure 3-14 – Total Error Characteristics for an Inst-Amp with Offset and Gain Error 57

Figure 3-15 – Total Error Characteristics for a Real World Inst-Amp with Offset, Gain, and Linearity Errors....58

Figure 4-1 – Output Offset Storage for a Single-Ended Amplifier (OOS-SE)....62

Figure 4-2 – Output Offset Storage and Cancellation for a Differential Amplifier (OOS-DF) 63

Figure 4-3 – Non-Overlapping Clock to Drive the MOS Switches....63

Figure 4-4 – Input Offset Storage – Single-Ended Amplifier (IOS-SE). 66

Figure 4-5 – Input Offset Storage – Differential Amplifier (IOS-DIF)....67

Figure 4-6 – Offset Cancellation using an Auxiliary Amplifier at the Input of the Input Stage of the Main Amplifier 69

Figure 4-7 – Offset Cancellation Using an Auxiliary Amplifier at the Output of the Input Stage of the Main Amplifier....71

Figure 4-8 – Conceptual Ping-Ping Configuration and its Two Parallel Auto-Zeroing Amplifiers73

Figure 4-9 – Data Converters in a Feedback Loop with Digital Control....75

Figure 4-10 – Digital Signal Processing Approach on Sampled Offset and Input Voltages....76

Figure 5-1 – A High Level Block Diagram of a General Chopper Amplifier....78

Figure 5-2 – Chopper Schematic, NMOS Implementation, and General Symbol....78

Figure 5-3 – Modulation or Chopper Signal....79

Figure 5-4 – Frequency Domain Representation of the Signal and Flicker Noise in a Chopper Amplifier.....80

Figure 5-5 – The Baseband Spectrum Shows that the Chopper Frequency Must be Bigger than the Summation of the Signal BW and Flicker Noise Corner Frequency.....81

Figure 5-6 – Conventional Chopper Inst-Amp and its Main Parasitic Capacitances 83

Figure 5-7 – Typical Waveforms of the Signal and Error at the Output and Input of a Chopper Inst-Amp. May modify a little. 83

Figure 5-8 – Charge Injection Spikes Through Certain Parasitic Capacitances within a Chopper, Create a Residual Offset at Chopper's Output due to its Rectification Act. 85

Figure 5-9 – Nested Chopper Amplifier with its Inner and Outer Choppers Operating at Two Different Frequencies. 87

Figure 5-10 – Using Nested Chopper Technique for Reduction of Charge Injection Residual Offset. 87

Figure 5-11 – Chopper Amplifier with an Auto-Zeroed Ping-Pong Configuration. 89

Figure 5-12 – Chopper-Stabilized Amplifier with Multipath Nested Miller Compensation.....90

Figure 5-13 – Chopper-Stabilized Amplifier with Multipath Hybrid-Nested Miller Compensation. 93

Figure 5-14 – Chopper-Stabilized Chopper Amplifier with Multipath Hybrid-Nested Miller Compensation. 93

Figure 5-15 – Block Diagram of a Chopper-Stabilized Chopper Instrumentation Amplifier with First Level Offset Cancellation.....96

Figure 5-16 – Block Diagram of Chopper-Stabilized Chopper Instrumentation Amplifier – Only Gm_5 and Gm_6 have offset errors. 100

Figure 5-17 – Errors Due to $Vos_{(5+6)}$ throughout the Chopper-Stabilization path.....101

Figure 5-18 – Removal of Offsets of Gm_5 / Gm_6 through a Second Order Compensation Auto-Zeroing (Gm_9 / Gm_{10}).....102

Figure 5-19 – Second Order Cancellation Loops to Remove the Offsets of Gm_4, Gm_5 / Gm_6.....106

Figure 5-20 – Addition of Third Order Offset Cancellation Loops and Remedy for Spikes (Offset Error Sources are not Shown).....110

Figure 5-21 – Magnitude Plot of a Two Path Amplifier before Cure.....117

Figure 6-1 – Top-Down Design Flow-Diagram 122

Figure 6-2 – The Schematic Describing the Behavioral Model of a Transconductance Block...126

Figure 6-3 – Top-Level Block-Diagram of the Proposed Architecture for the Chopper-Stabilized Auto-Zeroed Chopper Instrumentation Amplifier.....127

Figure 6-4 – Transistor-Level Schematic of a Chopper.....133

Figure 6-5 – Transistor-Level Schematic of a MUX.....134

Figure 6-6 – An informative Picture Showing the Simulation Results of the Model-Based Design Presented in figure 6-3.....140

Figure 6-7 – A Close-UP View of the Input-Referred Ripple and Spikes of the Model-Based Graph of figure 6-6.....141

Figure 6-8 – Push-pull Output Stage to replace $\boldsymbol{Gm1}$ block in top-level model-based block-diagram of figure 6-3.....143

Figure 6-9 – Transistor-level design of the transconductance block $\boldsymbol{Gm2}$ presented in the Model-Based Design of figure 6-3.....148

Figure 6-10 – Conventional V-I Converter for a CFIA with Sensing Capability around the Negative Rail.....149

Figure 6-11 – A Chopper Version of CFIA with Sensing Capability around the Negative Rail 150

Figure 6-12 – The Conventional V-I Converter with Voltage Feedback (Voltage Boosting) is Suffering from the Lack of sensing capability for the Negative Rail.....151

Figure 6-13 – Improvement of the Architecture of figure 6-12 by Changing the P-channel device at the input to its N-channel counterpart to be able to sense the negative rail 153

Figure 6-14 – Improvement on the Architecture of figure 6-13 through several modifications discussed in the text.....153

Figure 6-15 – Further Improvements on the Architecture of figure 6-15 through cascoded design154

Figure 6-16 – Simplified Transistor-level Schematic of the blocks $\boldsymbol{Gm7}$/ $\boldsymbol{Gm8}$ presented in the Model-Based Design of Figure 6-3.....157

Figure 6-17 – "Vernier" Type Gain Setting Resistor Network Suitable for Large Gain Ranges 158

Figure 6-18 – Portion of the Schematic of $\boldsymbol{Gm7}$(Accurate V-I Converter) Showing its Gain-Error Trim Taps with its Star–Delta equivalent Resistors 163

Figure 6-19 – Simplified Schematic of the equivalent Star Connection of the G.E. Trim of $\boldsymbol{Gm7}$164

Figure 6-20 – Transistor-level design of the Integrator block $\boldsymbol{Gm4}$ presented in the Model-Based Design of figure 6-3.....169

Figure 6-21 – Transistor-level design of the blocks $\boldsymbol{Gm5}$ and $\boldsymbol{Gm6}$presented in the Model-Based Design of figure 6-3 170

Figure 6-22 – Simplified Block-Diagram Representations of the Summers SUM_2 (SUM_4 is very similar) 171

Figure 6-23 – Transistor-Level Schematic of the Summer Circuit SUM_2 (SUM_4 is similar), None are shown in figure 6-3 for simplicity 173

Figure 6-24 – Transistor-Level Schematic of the Weak Transconductance $\boldsymbol{Gm3}$ 174

Figure 6-25 – Simplified Schematic of the Reference (Zero TC) Current Bias Circuitry 176

Figure 6-26 – Simplified Schematic of the Main Oscillator Circuitry 177

Figure 6-27 – An informative Picture Showing the Simulation Results of the Transistor-Level Design which is the counterpart of figure 6-6 shown for the model-based design. This is for 25°C and Nominal Process, with Real Clock Circuit as opposed to Ideal Clocks. 180

Figure 6-28 – Simulation Results of the Transistor-Level Design of figure 6-27 for "Fast" SPICE Models at +125°C 181

Figure 6-29 – Simulation Results of the Transistor-Level Design of figure 6-27 for "Slow" SPICE Models and -40°C 182

Figure 6-30 – Bode-Plots of the Transistor-Level Design of this Project as a Function of the Load Capacitance. The Design is Stable with Load Capacitances Much Higher than the Target Specification of C_L=100pF. The Phase Margin is 65deg for C_L=100pF. 183

Figure 6-31 – Histogram of Input-Referred Offset Voltage for 300 Units Tested by the Final Test (FT) Program Using Automatic Test Equipments (ATE) 186

Figure 6-32 – Histogram of Gain Error for 300 Units Tested by the Final Test (FT) Program Using Automatic Test Equipments (ATE) 187

Figure 6-33 – Variations of the Input-Referred Offset with the Input-Common Mode Voltage 188

Figure 6-34 –Variations of the Input-Referred Offset with the Supply Voltage 188

List of Tables

Table 1-1 – Typical Input Referred Offset Specifications for a 28

Table 2-1 – NMOS Mismatch Coefficients in Different Technology Nodes.....38

Table 3-1 – Comparison of Different Offset Removal Techniques for CMOS Amplifiers 54

Table 3-2 – Common Industry Grades and their Temperature Ranges 60

Table 5-1 – Eq. (5.20) Predictions of the Effects of the Integrator Capacitors Cm_{91} and Cm_{92} on the Input-Referred Offset for Exaggerated Vos_9=100mV. See Other Parameter Values in the Text. 108

Table 5-2 – Effects of the Offsets of Different Transconductance Blocks, and other Components on the Input-Referred Offset. 115

Table 6-1 – Target Design Specifications or Electrical Characteristics Table (EC Table) 128

Table 6-2 – Initial estimations of the transconductances of the model-based design of figure 6-3137

Table 6-3 – Initial Capacitor Values for the Block-Diagram of the Model-Based Design of figure 6-3 137

Table 6-4 – Load Resistor and Initial Gain Setting Resistor Values for the Block-Diagram of the Model-Based Design of figure 6-3 138

Table 6-5 – Table of Simulation Results for the Model-Based Design of figure 6-3.....139

Table 6-6 – Table of the Main Process Specifications 142

Table 6-7 – The Calculated G.E. Trim Characteristics for the CFIA Design of This Thesis.....162

Table 6-8 – Comparison of final Simulation Results for the Model-Based Design vs. the Transistor-Level Design of figure 6-3 179

Table 6-9 – Input-Referred offsets showing Simulation Results for the Model-Based Design, Transistor-Level Design, and the Silicon Measurements. 184

Table 6-10 – Measurement Results on Accuracy Parameters for 2 Units Tested at Room.....185

Table 6-11 – Measurement Results on DC Parameters for 2 Units Tested at Room.....185