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Fabrication of Nanoslits with <111> Etching TSWE Method

Hao Hong, Li Ye, Ke Li, Pasqualina M. Sarro, Guoqi Zhang and Zewen Liu*

***Abstract*— In this paper, we report a modified three step anisotropic wet etching (TSWE) method to fabricate solid-state silicon nanoslits. The slit-opening process is performed by <111> crystal plane etching. The etching rate of the <111> crystal plane is reasonably slow as it is only 1/45 of the <100> etching rate, thus allowing and therefore good slits-opening controllability. By slowly etching the <111> crystal plane, the over-etching was effectively reduced. Perfectly rectangular nanoslits with different dimensions were successfully obtained. The smallest achieved feature size of the nanoslit is 8.3 nm.**

I. Introduction

Solid-state nanopores/nanoslits have been used to study the fundamentals of ionic and polymer transport through nanofluidic channels [1], to develop detection tools for studying nucleic acids, proteins, and small molecules [2], and to characterize DNA nanostructure [3] over the past few years. More than that, various other applications for nanopores/nanoslits have also been demonstrated, such as gas separation [4], nanostencil lithography [5] and so on [6-10]. In principle, solid-state silicon is more robust, amenable to a larger range of operating conditions, compatible with semiconductor technology, so it is easier to integrate into electronics and embedded systems.

Common preparations of nanoslits mainly include dry and wet etching. Dry etching such as FIB and FEB could process sub-10nm nanoslits in a short time [11-14]. However, the high cost associated with it, has severely restricted the possibility of large-scale fabrication of nanoslits. Furthermore, the fabrication of nanoslits is difficult by FIB/FEM due to their serial manufacturing characteristics.

It has been demonstrated that the TSWE method, which is based on conventional semiconductor processing and MEMS wet etching techniques, could fabricate hollowed nanostructure effectively. By reducing the etching rate and improving the sensitivity of monitoring slit-opening events, good slits-opening controllability could be realized, thus nanoslits with different dimensions could be obtained. Feedback-based chemical etching method, as a simple and cost-effective strategy, has been successfully used to manufacture single crystal silicon (SCS) nanopores. Current feedback mechanism is an optional method, which monitors the pore-opening event by measuring the time dependence of the electrical current across the silicon chip [15-16]. A bias voltage should be applied across the chip, and a measuring instrument with high sensitivity is needed to detect the electrical current in the liquid. Both the two methods could improve the sensitivity of monitoring slit-opening events and obtained extremely small feature size nanopores/nanoslits. Chen et al. use a color-feedback mechanism based on phenolphthalein mixed with KOH to turn red to monitor the slit-opening event, obtained the smallest nanoslit with the feature size of 5 nm [17]. Ye et al. detected the slit-opening event by a current feedback method and also got a small feature size nanoslit down to 3.8 nm [18]. In order to further reduce the over-etching, in this paper, the TSWE method is used to perform slow etching from the <111> crystal plane, thanks to the lower etching rate, and a nanoslit with feature size down to 8.3 nm is obtained.

II. Experiments

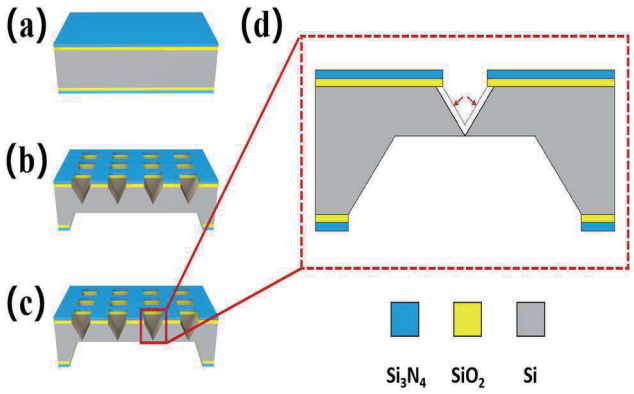

Fig. 1. Schematic illustration of the main process steps of the TSWE method: a) double-sided SiO_2 and Si_3N_4 deposited; b) the front cavity array and the back side etching window formed; c) the back-side thinning of silicon; d) etching model of the <111> planes.

The main process steps of the TSWE method are illustrated in Fig. 1. Single crystal silicon wafers with diameters of 4 inches and thickness of 300 μm were used as original substrates, all the wafers are double-polished, N-

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type. The concentration of KOH etching solution in each step was 33 wt.%.

At first, SiO_2 and Si_3N_4 layers were deposited on both sides of the silicon wafer grown by thermal oxidation and low-pressure chemical vapor deposition to be used as a stress buffer and mask layer respectively (refer to Fig. 1a). Then 33 wt.% KOH was used to form the front etching cavity array and the back side etching window as shown in Fig. 1b. Next, the back side thinning of silicon was conducted by the same KOH solution until it remaining about 2 µm. Finally, slow rate wet etching was in progress through the <111> crystal plane was performed until the nanoslits were opened. The slow etching rate could be explained as that two adjacent <100> crystal planes peel off each other, each silicon atom needs to break two chemical bonds. The density of dangling bonds is large, and it has higher surface energy and lower activation energy. For the <111> crystal plane, the separation of two adjacent <111> crystal planes require a chemical bond to be cut. So the <111> crystal plane has a low density of dangling bonds and low surface energy. And each silicon atom in the <111> plane is connected by three chemical bonds, so that it has a higher activation energy. As the etching rate increases with the increase of the dangling bond density, the dangling bond density of the <111> crystal planes is lower than for the <100> crystal planes. Thus the etching rate of the <111> crystal plane is reasonably slow as it is only 1/45 of the <100> etching rate at room temperature. Thanks to the lower etching rate, the over-etching was reduced effectively.

III. Results and Discussions

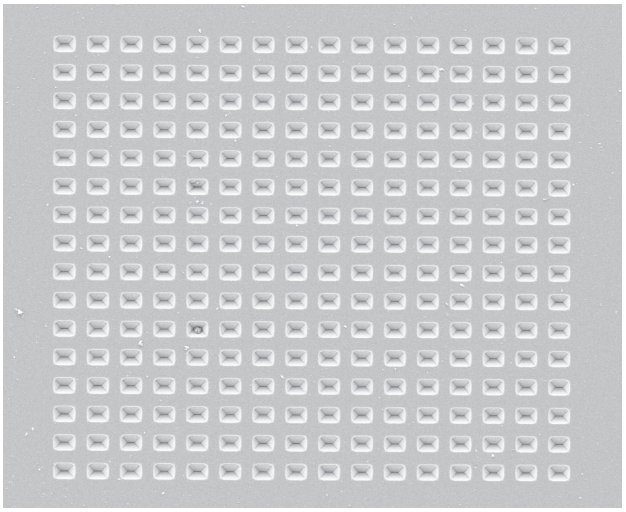

Fig. 2. SEM micrograph of the 16 × 16 etching cavity array.

After the first step of the wet etching, Fig. 2 exhibits a scanning electron microscope (SEM) micrograph of 16 × 16 etching cavity array, which could demonstrate that the front side etching cavity has been fabricated successfully over a large area. The size of each cavity is about 8 × 4 µm. Fig. 3 also shows a back side etched window, with a 0.5 × 0.5 mm^2 exposed area. From this enlarged figure, it could be seen that some nanoslits have been opened, which proves the proposed method could fabricate nanoslits effectively.

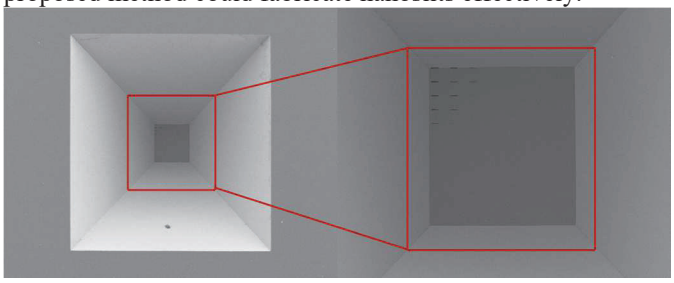

Fig. 3. SEM micrograph of the back etching window.

Furthermore, Fig. 4 gives a close-up of the obtained nanoslits. The shape of the nanoslits is rectangular, which is in accordance with the designed mask, and the distance between the upper and lower nanoslits is 8.035 µm. In addition, there still have some nanoslits which are not strictly rectangular. It could be explained by inhomogeneous etching, both the slit-opening time node of each side and the over-etching after the slit-opening event are different. Better controllability of uniformity in the wet etching process is necessary.

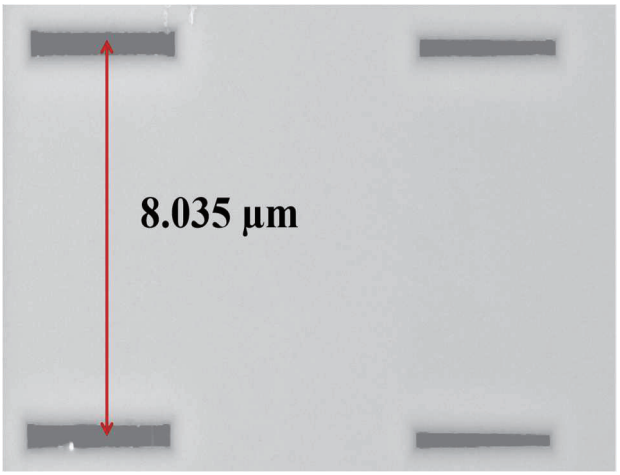

Fig. 4. SEM micrograph of the fabricated nanoslits array.

The best result is shown in Fig. 5, where the smallest feature size obtained 8.3 nm, is shown. Due to the slow rate etching performed from the <111> crystal plane, the over-etching is effectively reduced, and the sizes of the obtained nanoslits are also reduced in a controllable and reproducible way.

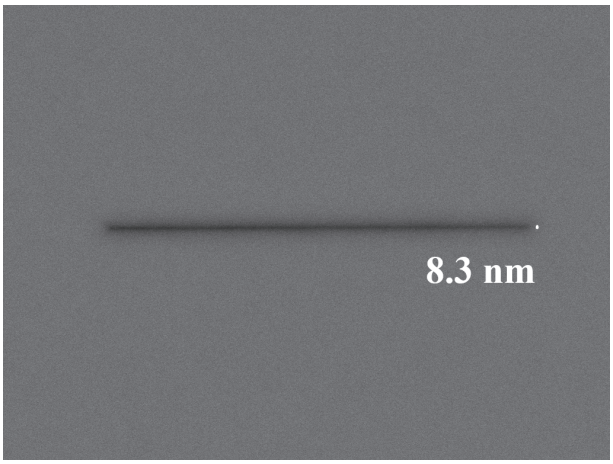

Fig. 5. The SEM micrographs of individual nanoslit fabricated by the TSWE method, with a feature size of 8.3 nm.

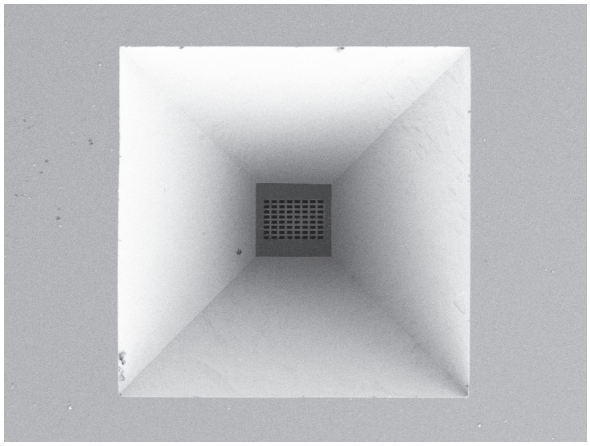

Fig. 6. SEM micrographs of fully opened nanoslit array.

In order to study the morphology and sizes of the completely opened nanoslits, Fig. 6 exhibits the SEM micrograph of the fully etched nanoslits. From the back etching window, an 8 × 8 nanoslit array has been obtained, all the nanoslits are rectangular as the front etching cavity is shown in Fig. 2. It could be demonstrated that all the nanoslits are opened. The next part will show the detail of the fully opened nanoslit.

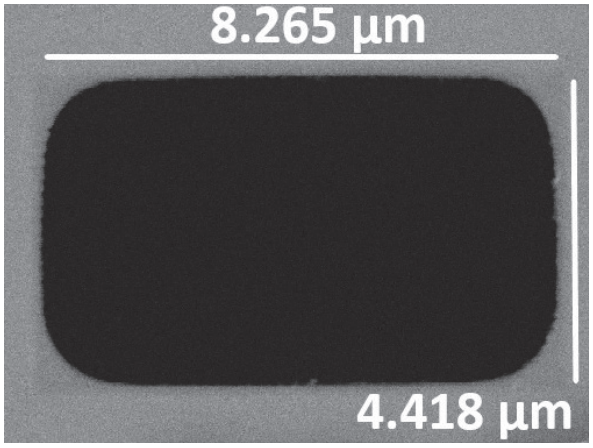

Fig. 7. SEM micrographs of a fully opened individual nanoslit.

Finally, after enough over-etching, the nanoslit with small dimension was fully opened, Fig. 7 shows a completely opened nanoslit, with the size of the nanoslit is 8.265 µm in length and 4.418 µm in width, which is corresponded with the front cavity.

IV. Conclusion

A modified TSWE method to fabricate solid-state silicon nanoslits was reported in this paper. The slit-opening process is performed by <111> crystal plane etching. Thanks to the reasonably slow <111> crystal plane etching rate compared with the <100> etching rate, the over-etching was reduced effectively and the good controllability of the slit-opening was realized. Perfectly rectangular nanoslits with different dimensions were successfully obtained. The smallest achieved feature size of the nanoslit is 8.3 nm. Duo the inhomogeneous etching, there still have some nanoslits which are not strictly rectangular. The proposed method provides a controllable and reproducible way obtain various nanostructure.

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