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Fully Soft Switched Nonisolated High Step-Up Single Magnetic Core Multiport Converter With Reduced Voltage Stress

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***Abstract*—This article presents a fully soft switched, nonisolated high voltage gain single magnetic core multiport converter based on boost three port structure for renewable energy applications. The developed voltage multiplier cell integrates switched capacitor and coupled inductors techniques to achieve high voltage gain and more design freedom. Furthermore, only a single magnetic core is employed which contributes to higher power density while an active clamp cell is integrated to provide fully soft switching condition and eliminate capacitive turn-on loss. All switches operate at zero voltage switching and diodes turn off at zero current switching. This approach minimizes switching losses and clamps the voltage spikes which enables the use of low forward voltage diodes. Also, the switches voltage stress is reduced through utilizing coupled inductors technique and thus, switches with low drain-source resistance can be utilized to achieve high efficiency along with high power density. To validate the theoretical analysis, a 200 W prototype with 400 V output port is implemented and the experimental results are presented.**

***Index Terms*—Energy storage system, renewable energy applications, soft switching, three-port boost.**

I. Introduction

OVER the past several decades, there has been a noticeable and steady increase in the renewable energies primarily due to their low carbon emissions and abundant availability [1]. However, renewable energies sources (RESs) exhibit intermittency characteristics as observed in solar and wind energy, or demonstrate slow transient responses, as exemplified by fuel cells [2]. Thus, RESs are equipped with energy storage systems (ESSs), such as batteries and ultra-capacitors, to facilitate power regulation [3]. Managing power between energy generator sources (EGSs) and ESSs necessitates many single input converters and as a solution, multiport converters (MPCs) are introduced. These converters can integrate and control multiple power ports simultaneously, offering advantages such as high power density, high efficiency, cost-effectiveness, and a compact structure [4], [5], [6], [7].

The low output voltage characteristic of RESs poses a significant challenge in meeting the demands of high voltage dc bus systems and electrical equipment. Employing high and near to unity duty cycles increases instability, current stress and power loss and therefore, employing high step-up converters is unavoidable [8] and various high step-up techniques such as switched capacitor/inductor, coupled inductors, and quadratic structures are integrated in MPCs [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Switch/diode capacitor cells are employed in [9] and [10] that double the output voltage gain. However, these converters suffer from inrush current within switched/diode capacitor cells and the MPC main switch due to capacitive loop which reduces the converter efficiency and high power applications are avoided due to extreme current spikes. A proposed solution in [10] involves integrating an additional magnetic core on the load side to mitigate the inrush current, at the expense of reduced voltage gain. In [11] and [12], nonisolated high step-up MPCs with quadratic voltage gains are introduced to achieve high voltages with no extreme duty cycles while the converter in [13] quadruples the output voltage. However, the power density of these converters reduces sharply as the input sources number increase due to noticeable required components to incorporate new sources.

Boost three port (BTP) based MPC as shown in Fig. 1(a) is among the most compact structures, offering modularity and flexibility to incorporate additional input ports with an appropriate component count [14], [15], [16], [17], [18], [19], [20], [21]. Achieving higher voltage gain using switched capacitor/inductor techniques necessitates more cells, thereby reducing power density. In [14], a high step-up BTP converter is proposed by sharing an inductor between the input ports, which contributes to the converter volume reduction. However, the

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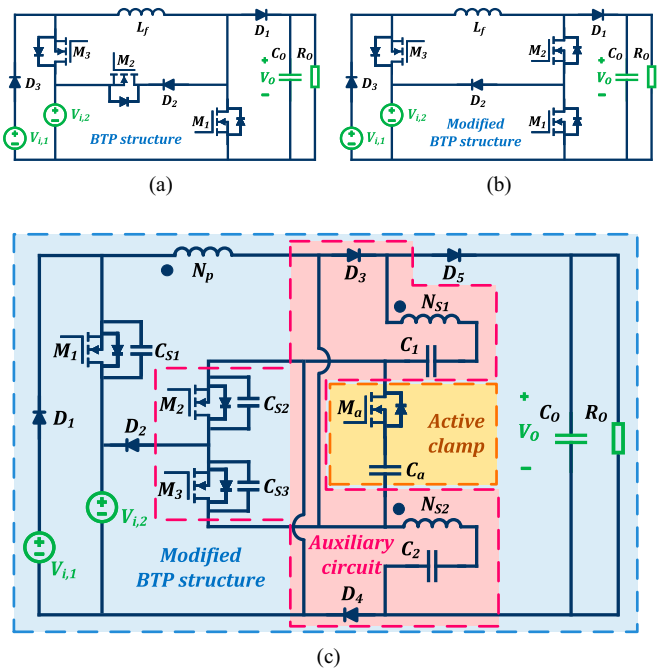

Fig. 1. (a) Boost three port structure [7]. (b) Modified boost three port structure [21]. (c) Proposed multiport converter.

design requires an additional magnetic core with two windings and three extra capacitors to achieve high voltage gain, thereby limiting power density. In [15], a single magnetic core high step-up BTP converter with only two capacitors is proposed and higher power density is achieved. Nonetheless, operating the semiconductor devices at hard switching is the main drawback of converters in [9], [10], [11], [12], [13], [14], [15].

Increasing the switching frequency results in smaller passive elements and hence, high power density MPCs are attained. Consequently, various soft switching techniques are employed in MPCs [16], [17], [18], [19], [20], [21]. In [16], a high step-up MPC based on the BTP structure is presented that provides switches zero current switching (ZCS) condition. This converter utilizes voltage lift and switched capacitor techniques to enhance the voltage gain, while a passive clamp circuit is included to achieve soft switching condition. Nevertheless, the converter switches turn on under ZCS condition, which cannot eliminate the capacitive turn-on loss and limits the converter efficiency and switching frequency. In [17], a high step-up soft switched MPC based on TPC is developed. This converter utilizes an active clamp cell and integrates coupled inductors technique to achieve high voltage gain, while only one magnetic core is utilized. Main and auxiliary switches turn on under zero voltage condition (ZVS) which eliminates the capacitive turn-on loss. However, the ESS charging switch [M_2 in Fig. 1(a)] in single-input double-output mode (SIDO) turns on at ZCS, resulting in capacitive turn-on loss. Also, the converters in [18] and [19] provide ZVS operation for the main switch without any auxiliary switch but two magnetic cores are required and the MPCs still suffer from capacitive turn-on loss across the ESS charging switch. In [20], a soft switched MPC based on BTP is proposed to mitigate the capacitive turn-on loss in SIDO mode by adding a diode to the basic BTP topology. However, soft switching is achieved via zero current transient technique, which suffers from capacitive turn-on loss and thus, the efficiency and switching frequency is limited, and the converter voltage gain resembles to a simple boost converter. The switch capacitive turn-on loss issue in SIDO mode is observed in many soft switched MPCs based on BTP like [18], [19], [20]. Hence, a modified version of BTP is presented in [21], which eliminates the capacitive turn-on loss by relocating the ESS charging switch as illustrated in Fig. 1(b). Additionally, the switches M_1 and M_2 voltage stresses are reduced since the switches are placed in series. Consequently, switches with better characteristics, especially lower drain-source resistance in ON-state ($R_{\mathrm{DS,on}}$) are selected and higher efficiency is achieved along with utilizing smaller heat sinks.

This article presents a fully soft-switched high step-up single magnetic core MPC based on the modified BTP structure, as illustrated in Fig. 1(c) for hybrid energy applications. To achieve high voltage gain and mitigate the switched capacitor technique inrush current, a novel voltage multiplier cell (VMC) is developed. This VMC combines coupled inductors and switched capacitor techniques and seamlessly integrated with the existing modified BTP structure switches and magnetic core. Coupled inductors technique provides high design freedom through tunable turn ratios and reduces the switch voltage stress [22] and consequently, the proposed MPC avoids using extreme duty cycles. Hard switched converters applications are limited in high frequency scenarios due to issues such as voltage surge, electromagnetic interference (EMI) noise and switching loss [23] and since, the coupled inductors leakage inductances can lead to voltage spikes [24], necessitating the integration of a soft-switching cell to absorb the leakage inductance energy. Therefore, an active clamp cell (M_a and C_a) is incorporated, which provides soft switching condition and also can contribute to the voltage gain increment [25]. In the proposed converter, all switches turn on/off under ZVS condition due to the active clamp cell and snubber capacitors. Moreover, all diodes turn off at ZCS and thus, fully soft switching operation for all semiconductor elements is achieved in operating modes. Additionally, the switches voltage stresses are reduced. Consequently, switches with low $R_{\mathrm{DS,on}}$ and diodes with low forward voltage can be selected which contributes to the converter efficiency.

II. Converter Analysis

In the proposed converter, EGS and ESS are represented by $V_{i,1}$ and $V_{i,2}$, respectively as illustrated in Fig. 1(c). The modified BTP structure consists of switches M_1, M_2, and M_3 and diodes D_1, D_2, and D_5 while switches M_2 and M_3 are shared with the VMC. To simplify the converter operation, all components are assumed ideal and dc capacitors are considered large enough so that their voltages remain constant during a switching cycle. The coupled inductors are modeled using an ideal transformer model with three windings, magnetizing inductance (L_m) and leakage inductance (L_k). The windings turns ratios are denoted by $n_1 = (N_{S1}/N_P)$ and $n_2 = (N_{S2}/N_P)$ while

TABLE I
DIFFERENT OPERATING MODES OF THE CONVERTER

Mode	SISO-I[1]	SISO-II	SISO-III	DISO[2]	SIDO
Input 1	EGS	ESS	EGS	EGS	EGS
Input 2	-	-	-	ESS	-
Output 1	Load	Load	ESS	Load	Load
Output 2	-	-	-	-	ESS

Note: [1]. = Single-Input Single-Output [2].Double-Input Single-Output

M_1, M_2, M_3 and M_a duty cycles are denoted by d_{M1}, d_{M2}, d_{M3} and d_{Ma}, respectively. The C_1 and C_2 values are selected equal and also, $n_1 = n_2 = n$. The proposed converter operates in different modes depending on the conditions of EGS, ESS, and load as reported in Table I.

A. DISO Mode

The proposed converter DISO mode is divided into six intervals as described in the following. M_2 and M_3 regulate the load voltage while M_1 controls each input source power absorption. The key waveforms are shown in Fig. 2(g).

Interval 1 (t_0–t_1) [Fig. 2(a)]: In this interval, switches M_1, M_2, and M_3 are in ON-state and the $V_{i,2}$ delivers energy to L_m causing i_k to increase as described by (1). Also, the input energy is delivered to the output through N_p, N_{S1}, and N_{S2} windings. This mode ends at t_1 by turning M_1 off under ZVS condition due to C_{S1}

$$i_k(t) = i_k(t_0) + \frac{1}{L_k}\left(V_{i,2} - \frac{V_o - 2V_{C1}}{2n}\right)(t - t_0). \quad (1)$$

Interval 2 (t_1–t_2) [Fig. 2(b)]: By turning M_1 off, ESS absorbing energy stops, and energy transfer from EGS to the load begins through D_1. Similar to the previous interval, i_k continues with $((V_{i,1} - (V_o - 2V_{C1})/(2n))/L_k)$ slope until M_2, and M_3 are turned off at ZVS due to C_{S2} and C_{S3} at t_2.

Interval 3 (t_2–t_3) [Fig. 2(c)]: By turning M_2, and M_3 off, i_k flows through the M_a body diode as described by (2). Therefore, M_a can be turned on under ZVS condition. During this mode, i_k energy is absorbed by C_a causing i_k, and the secondary side windings N_{S1} and N_{S2} current to decrease linearly. At t_3, the N_{S1} and N_{S2} current reach zero and D_5 turns off under ZCS condition

$$i_k(t) = i_k(t_2) - \left(\frac{V_o + (1+2n)V_{Ca} - 2V_{C1}}{2nL_k} - \frac{V_{i,1}}{L_k}\right)(t - t_2). \quad (2)$$

Interval 4 (t_3–t_4) [Fig. 2(d)]: During this mode, the N_{S1}, N_{S2}, and N_p currents are reversed, and diodes D_3 and D_4 are conducting. Hence, a fraction of L_m current charges C_1 and C_2 via N_{S1} and N_{S2}, respectively and i_k reduces as described by (3). Then, the M_a current is reversed and then, at t_4, i_k becomes zero and D_1 turns off under ZCS condition

$$i_k(t) = i_k(t_3) - \frac{1}{L_k}\left(\frac{(1+n)V_{Ca} - V_{C1}}{n} - V_{i,1}\right)(t - t_3). \quad (3)$$

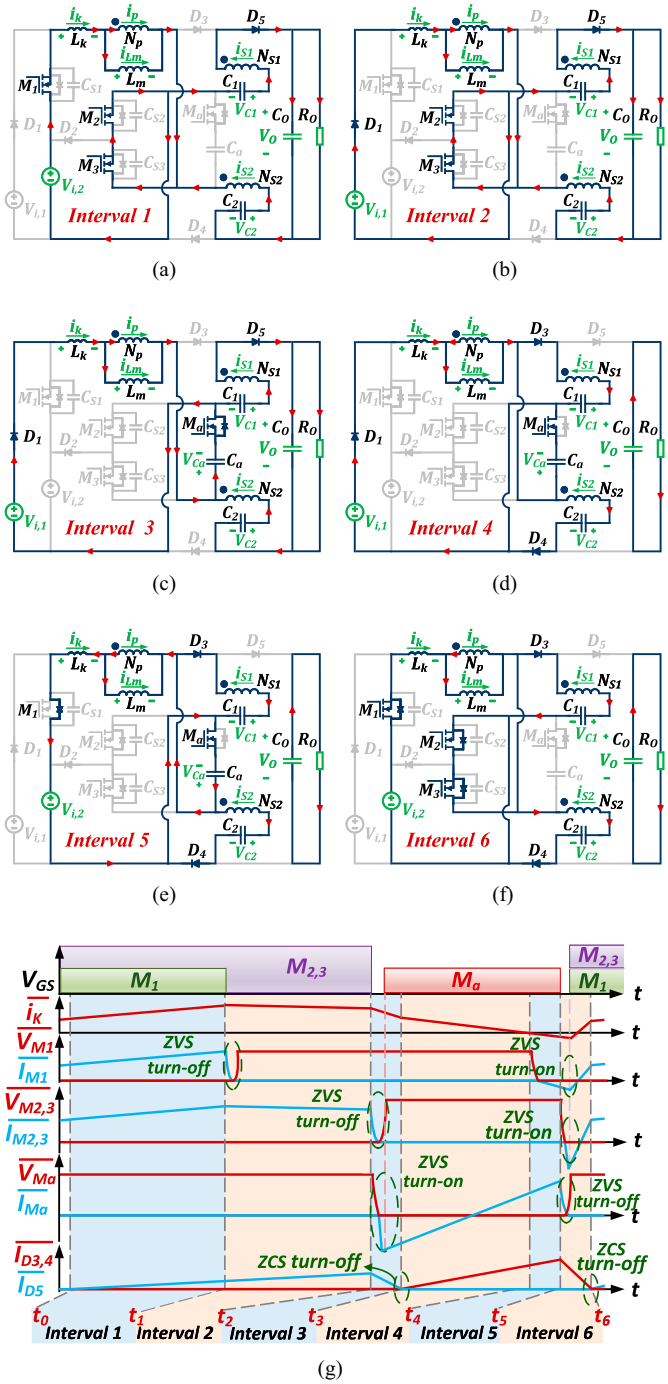

Fig. 2. (a)–(f) Proposed converter equivalent circuit in each DISO mode interval. (g) DISO mode theoretical waveforms.

Interval 5 (t_4–t_5) [Fig. 2(e)]: In this mode, i_k is reversed according to (4) and discharges C_{S1}. Then, the body diode of M_1 conducts and thus, M_1 can be turned-on under ZVS condition. At t_6, M_a is turned off under ZVS condition due to the capacitive loop consisting of C_{S3}, C_{S2}, and C_a

$$i_k(t) = -\frac{1}{L_k}\left(\frac{(1+n)V_{Ca} - V_{C1}}{n} - V_{i,2}\right)(t - t_4). \quad (4)$$

Interval 6 (t_5–t_6) [Fig. 2(f)]: By turning M_a off, i_k discharges C_{S2} and C_{S3} which causes M_2 and M_3 body diodes to conduct. Hence, M_2 and M_3 can be turned on under ZVS condition. Therefore, ($V_{i,2} + V_{\mathrm{Lm}}$) voltage is placed across L_k which causes i_k to increase linearly according to (5), until N_{S1} and N_{S2} currents reach zero and D_3 and D_4 turn off under ZCS condition. At t_6, D_5 starts conducting and the next switching cycle begins

$$i_k(t) = i_k(t_5) + \frac{1}{L_k}\left(V_{i,2} + \frac{V_{C1}}{n}\right)(t - t_5). \tag{5}$$

B. SIDO Mode

The converter operation in SIDO mode is divided into six intervals as described in the following while M_3 controls the ESS charging. The key waveforms are presented in Fig. 3(g).

Interval 1 (t_0–t_1) [Fig. 3(a)]: In this mode, switches M_2 and M_3 are in ON-state and $V_{i,1}$ energy is delivered to L_m, while, the EGS energy is transferred to the load through N_p, N_{S1}, and N_{S2} windings. This mode ends by turning M_2 off under ZVS condition due to C_{S2} while i_k increases as follows:

$$i_k(t) = i_k(t_0) + \frac{1}{L_k}\left(V_{i,1} - \frac{V_o - 2V_{C1}}{2n}\right)(t - t_0). \tag{6}$$

Interval 2 (t_1–t_2) [Fig. 3(b)]: By turning M_2 off, D_2 starts conducting and the L_m and L_k deliver power to $V_{i,2}$. The i_k decreases according to (7) until it reaches i_{Lm} and the N_{S1} and N_{S2} windings currents become zero causing D_5 to turn off at ZCS with the slope of $((V_{i,2} + V_{\mathrm{Lm}} - V_{i,1})/L_k)$

$$i_k(t) = i_k(t_1) - \left(\frac{V_o + (1+2n)V_{i,2} - 2V_{C1}}{2nL_k} - \frac{V_{i,1}}{L_k}\right)(t - t_1). \tag{7}$$

Interval 3 (t_2–t_3) [Fig. 3(c)]: At the beginning of this interval, power transfer to the load is terminated and ESS is charged via EGS thus, i_k slowly decreases according to (8). At t_3, M_3 is turned off under ZVS condition due to C_{S3} and consequently, D_2 turns off at zero voltage zero current switching (ZVZCS)

$$i_k(t) = i_k(t_2) - \frac{V_{i,2} - V_{i,1}}{L_m + L_k}(t - t_2). \tag{8}$$

Interval 4 (t_3–t_4) [Fig. 3(d)]: At t_3, M_a body diode starts conducting, and M_a can be turned on under ZVS condition. During this mode, D_3 and D_4 are conducting and C_1 and C_2 are charged through N_{S1} and N_{S2}, respectively. Also i_k decreases according to (3) and the M_a current is reversed. At t_4, i_k becomes zero and D_1 turns off under ZCS condition.

Interval 5 (t_4–t_5) [Fig. 3(e)]: At t_4, i_k is reversed according to (4) and discharges C_{S1} and the body diode of M_1 conducts. At t_5, M_a is turned off under ZVS condition due to the capacitive loop consisting of C_{S3}, C_{S2}, and C_a.

Interval 6 (t_5–t_6) [Fig. 3(f)]: By turning M_a off, i_k discharges C_{S2} and C_{S3} leading M_2 and M_3 body diodes to conduct and M_2 and M_3 can be turned on under ZVS condition. Thus, ($V_{i,2}$ - V_{Lm}) voltage is placed across L_k and i_k increases linearly until the M_1 body diode turns off at ZCS and D_1 starts to conduct. At t_6, N_{S1} and N_{S2} currents reach zero causing D_3 and D_4 to turn off at ZCS. Then, D_5 starts conducting and the next switching cycle begins.

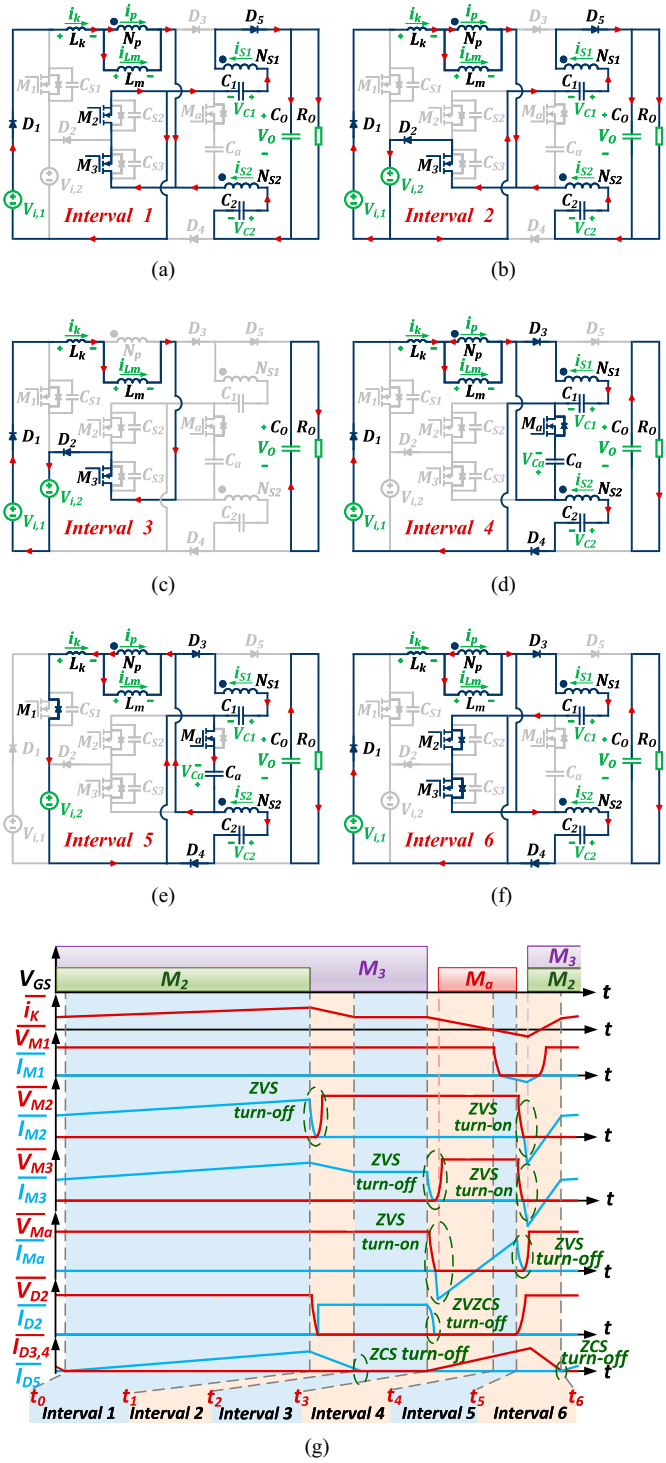

Fig. 3. (a)–(f) Proposed converter equivalent circuit in each SIDO mode interval. (g) SIDO mode theoretical waveforms.

C. SISO Modes

SISO operation can be divided into three modes which are similar to the DISO and SIDO modes. To avoid redundancy, all SISO modes descriptions are summarized as follows. The first mode (SISO-I) is the DISO mode when the switch M_1 is not turned on while the second mode (SISO-II) is similar to the

DISO mode when the switch M_1 is kept on. Finally, the third mode (SISO-III) is similar to SIDO mode when the output voltage is high enough that D_5 stays off in interval 2 and switch M_3 stays on in all intervals.

III. Design Consideration

A. Voltage Gains

According to the operating principles, the proposed converter has different voltage gains in DISO, SIDO, and SISO modes which are obtained as follows. In DISO mode, M_1 controls the received energy from $V_{i,1}$ and $V_{i,2}$. Thus, by writing the Kirchhoff's voltage law (KVL) for intervals 1, 2, and 4 (other intervals are ignored due to their small time duration) of DISO mode, and using the magnetizing inductance Volt-second balance, the DISO output voltage is attained as

$$V_o = \frac{2(n+1)}{1-d_{M3}}(d_{M1}V_{i,2} + (1-d_{M1})V_{i,1}). \tag{9}$$

The SIDO mode voltage gain can be calculated by writing the KVL principle at intervals 1 and 4 (other intervals are ignored due to their small time duration) of SIDO, and using the magnetizing inductance Volt-second balance as follows:

$$V_o = \frac{2(n+1)}{1-d_{M3}}((d_{M2}-d_{M3})V_{i,2} + d_{M2}V_{i,1}). \tag{10}$$

SISO contains SISO-I, SISO-II, and SISO-II modes where, during SISO-I and SISO-III M_1 is off while it is continuously conducting during SISO-II. The voltage gain of SISO-I and SISO-II modes are obtained in a similar procedure as (9)

$$V_{o(\mathrm{SISO-I,SISO-II})} = \frac{2(n+1)}{1-d_{M3}}V_{i,j} \quad j\,\varepsilon\{1,2\}. \tag{11}$$

SISO-III mode is similar to SIDO mode except that the output voltage is high enough to cause the diodes D_3, D_4, and D_5 stay off while switch M_3 continuously conducts in all intervals. Therefore, the voltage gain of SISO-III mode is obtained just as the conventional boost converter.

B. Semiconductor Devices Voltage Stresses

The switches and diodes voltage and current stresses are reported in Table II. Notations $I_{o(\max)}$ and $I_{Vi,2(\max)}$ represent the maximum of average output current and ESS current, respectively. Since the converter operates in different modes of SISO, SIDO, and DISO, the highest semiconductors devices voltage stress between all operating modes is considered as the worst-case scenario.

C. Soft Switching Condition

In this topology M_a and C_a compose an active clamp circuit which absorbs L_k energy and provides ZVS turn-on condition for M_1, M_2, and M_3. Also, to provide ZVS condition at turn-off for all switches, snubber capacitors C_{S1}, C_{S2}, and C_{S3} are placed across the main switches. The proper value of snubber capacitors is designed just as the any snubber circuit [26]

$$C_S \geq C_{S_{\min}} = \frac{i_{SW}t_f}{2V_{SW}} \tag{12}$$

TABLE II
Voltage/Current Stress of Semiconductor Devices at Worst-Case

Voltage Stress	Element	Current Stress
$V_{i,2}-V_{i,1}$	M_1 & D_1	$2nI_{o(\max)} \times \frac{d_{M3}(n-1)+2}{d_{M3}(1-d_{M3})}$
$V_{i,2}$	D_2	$\frac{I_{Vi,2(\max)}}{d_{M3}-d_{M2}}$
	M_2	$2I_{o(\max)} \times \frac{d_{M3}(n^2-n-1)+2n}{d_{M3}(1-d_{M3})}$
$\frac{V_o}{2(n+1)}-V_{i,2}$	M_3	
$\frac{V_o}{2(n+1)}$	M_a	
$\frac{V_o}{2}$	D_3 & D_4	$\frac{2I_{o(\max)}}{(1-d_{M3})}$
V_o	D_5	$\frac{2I_{o(\max)}}{d_{M3}}$

where i_{SW} is the switch current before the turn-off instant and V_{SW} is the switch voltage when the switch current reaches zero at t_f (switch fall time). It should be noted that the M_a gate signal is applied when its body diode is conducting and consequently, ZVS turn-on condition is achieved without any limitation. To provide ZVS turn-on condition for switches M_1, M_2 and M_3, their snubber capacitors should be completely discharged and then switches body diodes should conduct before applying the switches gate signals. Hence, the condition in (13) should be satisfied in each operating mode. Please note that snubber capacitors in the following relation, includes the switches output capacitors (C_{OSS})

$$C_{S1}V_{M1}^2 + C_{S2}V_{M2}^2 + C_{S3}V_{M3}^2 + C_{OSS}V_{Ma}^2 < L_k i_k^2(t) \tag{13}$$

where switches voltages and i_k at M_2 turn-on moment should be considered. Therefore, to attain soft switching from full load to 40% of full load, a coupling coefficient (k) equals to 0.96 is selected. Also, according to the operating modes, most of the times, M_a acts as a synchronous rectifier, and ZVS turn-on condition is achieved without limitation.

D. Design Procedure

To obtain a proper converter operation at continuous conduction mode (CCM) in all different operating modes, the average current and current ripple of the magnetizing inductance are calculated as follows:

$$i_{\mathrm{Lm(ave)}} = \frac{2(n+1)I_o}{1-d_{M2}} \tag{14}$$

$$\Delta i_{\mathrm{Lm}} = \frac{d_{M2}V_{i,2}}{f_s L_m} \tag{15}$$

where I_o and f_s represent the output average current and switching frequency, respectively. Hence, regarding (14) and (15), the magnetizing inductance value is obtained as

$$L_m \geq \frac{d_{M2}(1-d_{M2})^2 R_{L(\mathrm{critical})}}{8(n+1)^2 f_s} \tag{16}$$

where $R_{L(\text{critical})}$ is the maximum load resistance at boundary condition (according to 15% of nominal load). Then, the primary winding turn number is attained as

$$N_P = \frac{L_m i_{\text{Lm(max)}}}{\text{BA}} \tag{17}$$

where B and A are the flux density and core effective density, respectively. Also, the air gap length (l_{gap}) is calculated according to (18)

$$l_{\text{gap}} = \frac{\mu N_P i_{\text{Lm(max)}}}{B} \tag{18}$$

where μ is the permeability of free space ($4\pi \times 10^{-7}$). The C_a voltage is attained by employing Volt-second balance formula as follows:

$$V_{Ca} = \frac{V_o}{2(1+n)}. \tag{19}$$

Simply, the C_1 and C_2 voltages are achieved by utilizing L_m Volt-second balance formula according to (20)

$$V_{C1} = V_{C2} = \frac{G - 2n}{2G} V_o \tag{20}$$

where G demonstrates the converter voltage gain in operating modes as simplified from (9) and (10) as follows:

$$\left.\begin{aligned} G &= \tfrac{2(n+1)(d_{M1}(\alpha-1)+1)}{1-d_{M3}} && \text{(DISO mode)} \\ G &= \tfrac{2(n+1)(d_{M_2}(\alpha+1)-\alpha d_{M3})}{1-d_{M3}} && \text{(SIDO mode)} \end{aligned}\right\} \tag{21}$$

where α is the $V_{i,2}/V_{i,1}$ ratio. The capacitors charge variation (ΔQ) are attained according to $\Delta Q = C\Delta V$, where ΔQ is obtained based on the average charging/discharging current multiplied to the corresponding duration ($I\Delta t$). Therefore, the C_o value is achieved based on the following equation:

$$C_o \geq \frac{(1-d_{M3})I_{o(\max)}}{\Delta V_o f_s} \tag{22}$$

where ΔV_o is the output voltage ripple and selected 1% of the output voltage at the steady state condition and similarly, the capacitors C_1 and C_2 values are obtained according to (23)

$$C_1 \,\&\, C_2 \geq \frac{2I_{o(\max)}}{\Delta V_C f_s} \tag{23}$$

where ΔV_C is the C_1 and C_2 voltage ripple and considered about 10%. Moreover, the L_k energy at M_3 turn-off moment [$i_k(t)$ in (24)] charges C_a and hence active clamp capacitor value with considering 20% voltage ripple is attained as

$$C_a \geq \frac{(n+1)L_k i_k^2(t)}{\Delta V_{Ca}((n+1)\Delta V_{Ca} + V_o)}. \tag{24}$$

E. Control and Mode Selector Unit

A control diagram for the proposed converter is illustrated in Fig. 4(a). There are four controllers in the proposed method: maximum power absorbing (MPA) controller for absorbing EGS maximum energy, state of charge (SOC) controller for ESS voltage limitations, load voltage regulator (VR) controller for output voltage control and master controller for handling all the mentioned controllers. The master controller prioritizes

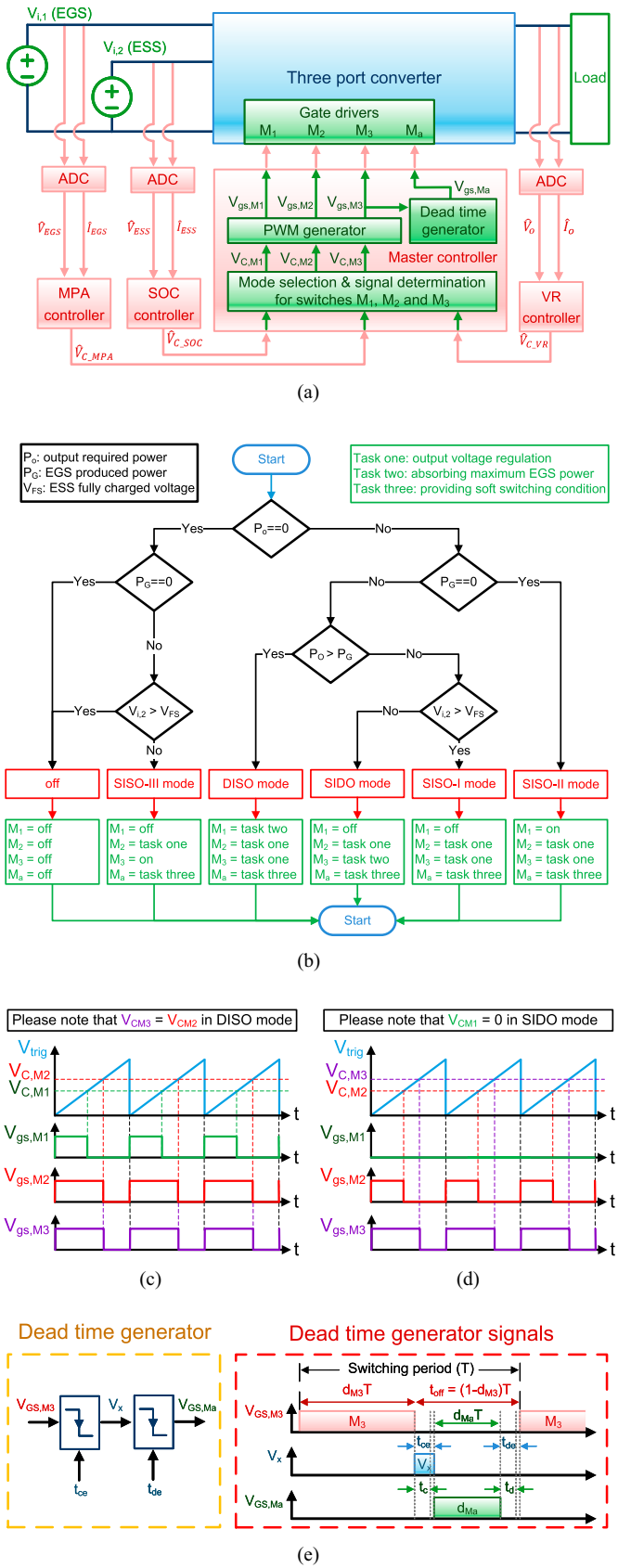

Fig. 4. (a) Control diagram for the proposed converter. (b) Proposed converter mode selector unit. (c) PWM generator unit signals in DISO mode. (d) PWM generator unit signals in SIDO mode. (e) Dead time generator unit and its signals.

the three other controllers via its constituent units. The MPA and SOC controllers are designed according to the requirements of each specified application. Then, the converter is set at the appropriate operating mode by mode selector unit which checks the output required power, EGS produced power and ESS state of charge, repeatedly as shown in Fig. 4(b). Consequently, control level voltages ($V_{C,M1}$, $V_{C,M2}$, and $V_{C,M3}$) are produced and defines the duty cycles for the switches M_1, M_2, and M_3 which are utilized in the pulse width modulator (PWM) generator unit to generate these switches gate-source signals as depicted in Fig. 4(c).

The auxiliary switch gate-source signal is easily generated by inserting the dead times t_{ce} (after M_3 turn-off moment) and t_{de} (before M_3 turn-on moment), as illustrated in Fig. 4(b). Dead times t_{ce} and t_{de} are adjusted using two monostable blocks, each set to 1.2 times the snubber charging and discharging duration (t_c and t_d), respectively. As a result, M_a duty cycle (d_{Ma}) is given by

$$d_{Ma} = (1 - d_{M3}) - \frac{t_a + t_d}{T} \tag{25}$$

where T is the converter switching period.

IV. Experimental Results and Efficiency Analysis

To evaluate the proposed converter performance and validate the analysis, a 200 W prototype converter based on the key parameters reported in Table III is implemented at 200 kHz switching frequency as shown in Fig. 5(a). The converter experimental waveforms in DISO and SIDO modes are shown in Fig. 5(d)–5(i) and 5(j)–5(o), respectively. Also, a closed-loop response in DISO and SIDO modes are illustrated in Fig. 5(b) and 5(c), respectively. As illustrated in Fig. 5(d), M_1 turns on/off under ZVS condition to control the ESS power absorption in DISO mode while the D_1 ZCS turn-off in the EGS power path is shown in Fig. 5(g). Switches M_2 and M_3 have the same switching patterns in DISO mode and M_2 ZVS turn-on/off is illustrated in Fig. 5(e). Meanwhile, M_a turns off at ZVS due to the capacitive loop consisting of C_{S3}, C_{S2}, and C_a providing soft switching condition for main switches in both DISO and SIDO modes as illustrated in Fig. 5(f) and 5(l), respectively. M_a ZVS turn-on is achieved when its body diode is conducting. Moreover, diodes D_3 and D_4 have similar waveforms while D_3 waveforms and ZCS turn-off in DISO and SIDO modes are represented in Fig. 5(h) and 5(n), respectively. Also, D_5 ZCS turn-off in DISO and SIDO modes is illustrated in Fig. 5(i) and 5(o), respectively. In SIDO mode, switches M_2 and M_3 turn-on at ZVS, simultaneously as shown in Fig. 5(j) and 5(k), respectively due to their body diodes conduction. M_2 turns off at ZVS due to C_{S2} while M_3 stays on longer to charge ESS through D_2. When charging ESS is over, M_3 turns off at ZVS due to C_{S3} and D_2 turns off at ZVZCS.

The loss breakdown analysis for DISO and SIDO modes is performed using equations provided in [27] and considering the key parameters reported in Table III. The results are illustrated in Fig. 5(p) while other losses include small losses like switches body diodes and capacitors conduction losses and core hysteresis loss. Additionally, the equivalent efficiency diagram is depicted in Fig. 5(q). Finally, the converter power density is calculated and 2.02 mW/mm^3 is achieved.

TABLE III
Key Parameters of the Implemented Prototype

Symbol	Value	Symbol	Symbol
M_1	SISA40DN	Magnetic core	ER 28/17/11
M_2 & M_3	CSD19536KTT	$N_P : N_{S1} : N_{S2}$	28:42:42
M_a	IPP051N15N5	C_1 & C_2 & C_a	680 nF
D_1	STPS20L15GR	C_o	1 μF
D_2	V12P6	C_{S1}	3.3 nF
D_3 & D_4	AES2EF-HF	C_{S2} & C_{S3}	470 pF
D_5	AES2HF-HF	$V_{i,1}$	36 V
f_s	200 kHz	$V_{i,2}$	48 V
L_m	90 μH	V_o	400 V
Windings litz wire diameter			0.3 mm

V. Comparison

A comprehensive converter performance and feature comparison is conducted between the proposed converter and multiport counterparts, as reported in Table IV. The converters in [14], [18], [19], and [21] are developed based on BTP structure similar to the proposed MPC, allowing for high modularity and possibility of adding extra sources with a suitable component count. Utilization of only a single magnetic core in the proposed converter contributes to achieving high power density while the other converters require at least two magnetic cores. The proposed converter voltage gain is twice the converters voltage gain based on inductor techniques in [14], [18], [19], and [21], due to integration of switched capacitor technique in the VMC. Consequently, the proposed converter and [13] achieve the highest voltage gain among the converters in Table IV even surpassing the quadratic based structures in [11] as illustrated in Fig. 6. The proposed converter voltage gain benefits from an extra degree of design freedom due to tunable turn ratios and hence, the proposed converter voltage gain can exceed that of [13] with higher than unity turn ratio. The main switch voltage stress in [11] is equal to the output voltage which necessitates utilizing switches with high $R_{\mathrm{DS,on}}$. Also, the main switch voltage stress in converters of [9], [13], [14], [18], [19] and [21] (when duty cycle surpass 0.5) is higher than the input voltage and thus, utilizing switches with high $R_{\mathrm{DS,on}}$ is unavoidable. Conversely, the proposed converter reduces the main switch voltage stress to the ESS port which contribute to higher efficiency.

The converters in [9], [11], [13], and [14] achieve high voltage gains without extreme duty cycles, however, these converters suffer from hard switching condition which limits the converters efficiency, power density and switching frequency. The converters in [18] and [19] provide soft switching with an auxiliary circuit, but their voltage gain is half of the proposed converter while the ESS charging switch suffer from capacitive turn-on loss. Meanwhile, these MPCs require two magnetic

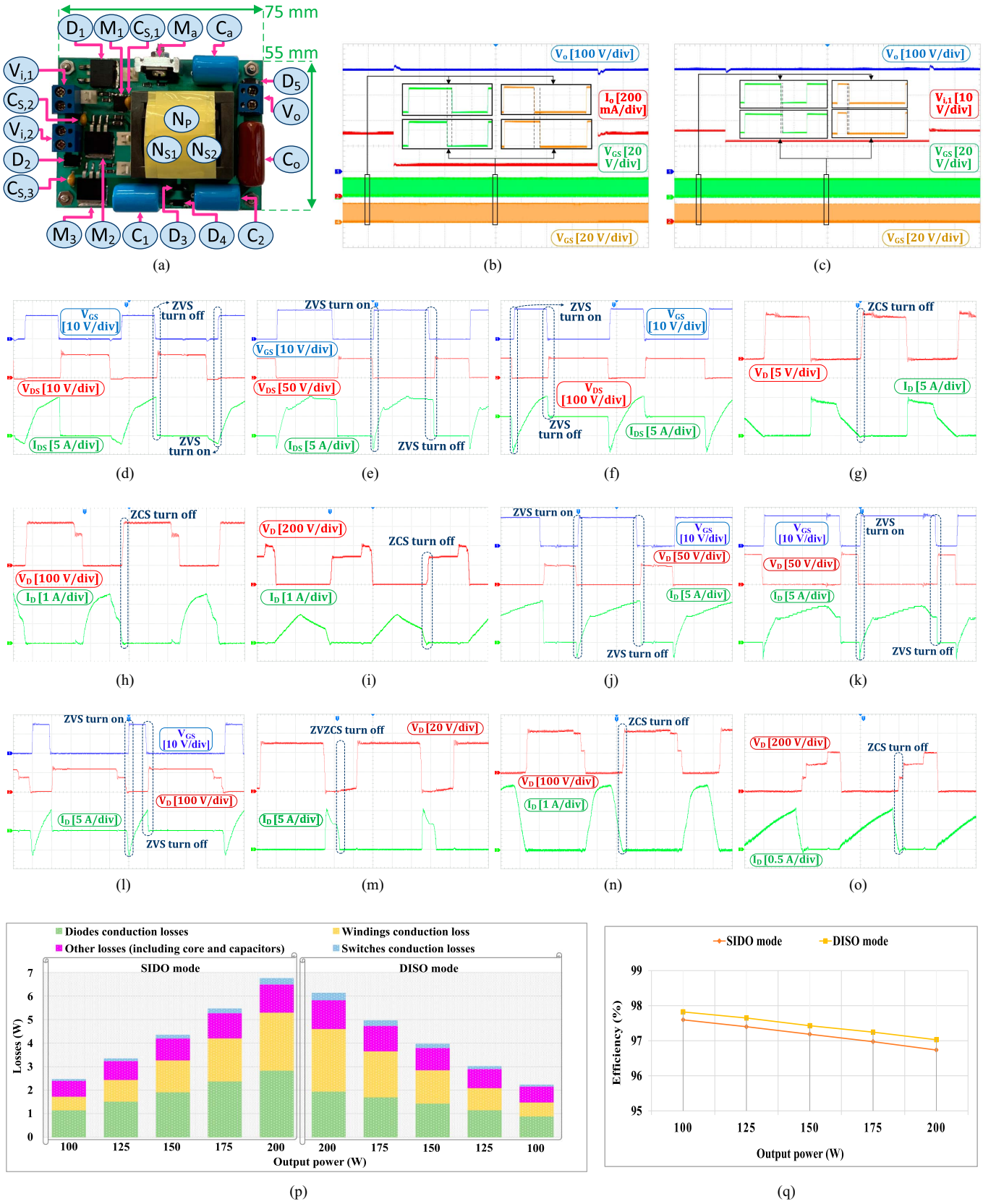

Fig. 5. (a) Implemented prototype converter photograph (height = 24 mm). (b) DISO mode step load response. (c) SIDO mode step input response. (d)–(i) Implemented prototype waveforms in DISO mode. (d) M_1. (e) M_2. (f) M_a. (g) D_1. (h) D_3. (i) D_5. (j)–(o) Implemented prototype waveforms in SIDO mode. (j) M_2. (k) M_3. (l) M_a. (m) D_2. (n) D_3. (o) D_5. ((b) and (c) time scales are 5 $\mathrm{ms/div}$ while (d)–(o) time scales are 2.5 $\mu\mathrm{s/div}$. (p) Loss-breakdown analysis at various powers in DISO and SIDO modes. (q) Efficiency versus output power in DISO and SIDO modes.)

TABLE IV
PERFORMANCE COMPARISON OF THE PROPOSED MPC AND OTHER COUNTERPART CONVERTERS IN [9], [11], [13], [14], [18], [19], [21]

References	[9]	[11]	[13]	[14]	[18]	[19]	[21]	Proposed
Type	Other	Other	Other	BTP	BTP	BTP	BTP	BTP
Element count[1]	5/5/5/2/2/19	5/3/4/4/4/20	4/4/6/2/2/18	3/5/4/2/3/17	3/7/4/2/4/20	3/5/4/2/3/17	4/4/3/1/2/14	4/5/4/1/3/17
Voltage gain[2]	$\frac{3}{1-d}$	$(\frac{1}{1-d})^2$	$\frac{4}{1-d}$	$\frac{1+n}{1-d}$	$\frac{1+n}{1-d}$	$\frac{1+n}{1-d}$	$\frac{1+n}{1-d}$	$\frac{2(1+n)}{1-d}$
Main switch VS[3]	$\frac{V_o}{2}$	V_o	$\frac{V_i}{(1-d)}$	$\frac{V_i}{(1-d)}$	$\frac{V_o}{(1+n)}$	$\frac{V_i}{(1-d)}$	$\frac{V_i}{2(1-d)}$	$V_{i,2}$
Input port current[4]	Con	Con	Dis	Dis	Dis	Dis	Dis	Dis
Main switch SS[5]	Hard/Hard	Hard/Hard	Hard/Hard	Hard/Hard	ZCS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS
Auxiliary switch SS	Hard/Hard	Hard/Hard	Hard/Hard	-	-	-	ZVS/ZVS	ZVS/ZVS
Diodes SS	Hard	Hard	Hard	Hard	ZCS	ZCS	ZCS	ZCS
Turn-on loss[6]	√	√	√	√	√	√	×	×
Nominal Power	160	200	35	300	200	200	125	200
f_s (kHz)[7]	30	40	50 & 100	50	100	50	100	200
Efficiency (%)[8]	91-91.4	91	89.6	94.3-95.9	93-93.9	92.1-94	91.8-94.2	96.7-97

Note: [1]. Switches/Diodes/Capacitors/Magnetic cores/Windings/Total count are represented, respectively. Snubber capacitors are ignored due to low weight and volume. [2]. Voltage gain in SISO-I mode is reported. [3]. Voltage stress. [4]. Con = Continuous and Dis = Discontinuous. [5]. Soft switching: "on/off" for switches and "off" for diodes. [6]. Switches capacitive turn-on loss. [7]. Main switch switching frequency. [8]. Efficiency at nominal power for different operating modes or a single mode.

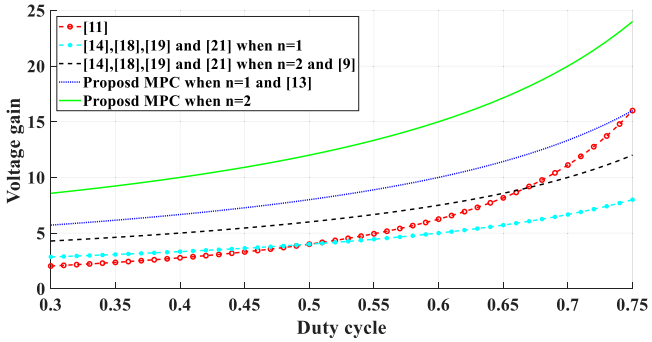

Fig. 6. Voltage gain versus duty cycle of converters in Table IV.

cores to provide soft switching condition. Despite facing high voltage stress, the main switch in [18] turns on at ZCS and experiences capacitive turn-on loss, in contrast to all switches in the proposed MPC which operate under ZVS condition.

VI. CONCLUSION

This article introduces a fully soft switched nonisolated high step-up multiport converter based on modified boost three port structure. As demonstrated in comparison section, the proposed converter achieves higher voltage gain compared to the counterpart converters while avoids switched capacitor inrush current. The integrated voltage multiplier cell combines the switched capacitor and the coupled inductors techniques symmetrically and hence, achieves reduced semiconductors voltage stress along with high design flexibility for various applications due to tunable turn ratios. Moreover, an integrated active clamp cell ensures soft switching condition and contributes to the higher voltage gain. Utilizing the modified boost three port structure along with the active clamp cell enables the fully soft switching operation and mitigates the capacitive turn-on loss which is a considerable contribution over the soft switched counterparts, as revealed in the comparison section. A design procedure is outlined to develop a prototype with 36 V EGS port, 48 V ESS port, and 400 V output port at 200 W nominal power. The results demonstrate the achievement of soft-switching conditions, high voltage gain, and significant reduction in diodes reverse recovery issues. The converter efficiencies at nominal load reach to 97% and 96.7% in DISO and SIDO modes, respectively with 2.02 mW/mm^3 power density of the laboratory prototype.

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