IM3 Linearity Improvement Techniques for Bipolar Power Amplifiers

by

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This thesis is confidential and cannot be made public until November 29, 2021.

Declaration of Authorship

I, Marco D'Avino, declare that this thesis titled, 'IM3 Linearity Improvement Techniques for Bipolar Power Amplifiers' and the work presented in it are my own. I confirm that:

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Abstract

The increasing number of users of wireless devices over the world requires the development of new communication technologies, which can enable ultra-high speed data-rates and enhancing the efficiency of the currently used networks. In order to accomplish these goals, one of the most important requirements for RF transceivers is a high linearity of the transmitted signal; which allows to make an efficient use of the available frequency spectrum. Currently, GaAs Heterojunction Bipolar transistors are being used in power amplifier blocks to guarantee high linearity and good power handling capability. However, silicon-based devices like SiGe HBTs enable the complete integration of the system, significantly reducing the costs. In this thesis work, RF circuit linearization techniques based on the out-of-band IM3 cancellation are investigated and developed in order to improve the linearity performance of SiGe HBT Medium Power Amplifiers. The application of the Derivative Superposition linearization technique to bipolar amplifiers is proposed, and the circuit solution for the IM3 cancellation through this method is derived. A Medium Power Amplifier based on the developed technique is designed and implemented to test its effectiveness. The results demonstrate the applicability of the Derivative Superposition technique for the enhancement of the IM3 linearity of Bipolar Power Amplifiers.

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To everyone else who I forgot to mention but, knowing me, will forgive me for this forgetfulness: Thank You!

Marco d'Avino, Delft, November 2016

"L'Amore è fondamentale."

Nardino Giampietro

Contents

List of Figures

List of Tables

Abbreviations

BB	Base Band
CB	Common Base
CCCS	Current Controlled Current Source
CE	Common Emitter
DS	Derivative Superposition
DUT	Device Under Test
GP	Gummel-Poon
GSG	Ground-Signal-Ground
GSGSG	Ground-Signal-Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistor
HPA	High Power Amplifier
HV	High Voltage
LV	Low Voltage
MPA	Medium Power Amplifier
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PVT	Process-Voltage-Temperature
RAN	Radio Access Network
RF	Radio Frequency
SA	Spectrum Analyzer

Symbols

a_i	general amplifier Taylor coefficients	
β_f	small-signal common-emitter current gain	
C_{bc}	base-collector capacitance	F
C_{de}	base-emitter diffusion capacitance	F
C_{dec}	common-base stage base decoupling capacitor	F
C_{deg}	degeneration capacitance	F
C_{jc}	base-collector junction capacitance	F
C_{je}	base-emitter junction capacitance	F
C_{π}	base-emitter capacitance	F
C_{res}	LC-resonator capacitor	F
C_{stab}	stabilization capacitor	F
f	frequency	Hz
f_0	fundamental frequency	Hz
f_c	center frequency	Hz
Δf	modulation frequency	Hz
f_t	cut-off frequency	Hz
F	feedback factor	
ϕ	phase	rad
ϕ_{OoB}	Out-of-Band phase relation	rad
G	gain	
g_m	linear transconductance	S
H_n	n^{th}-order nonlinear transfer function	
I	current	A
I_c	collector current	A
I_{cq}	quiescent collector current	A

$i_{c,IM3}$	IM3 collector current	A
$IM2$	second-order intermodulation	
$IM3$	third-order intermodulation	
J_c	collector current density	A
J_n	electron current density	A
k	Rollet stability factor	
L_{bw}	bondwire inductance	H
L_{db}	downbond inductance	H
L_e	emitter inductance	H
L_{par}	parasitic inductance	H
L_{res}	LC-resonator inductor	H
m	scaling factor	
M	avalanche multiplication factor	
$Mult$	number of parallel devices	
$OIP3$	output third-order intercept point	dBm
P_{1dB}	1dB output compression point	dBm
P_{avs}	power available from the source	dBm
P_{in}	input power	dBm
P_{out}	output power	dBm
Q	quality factor	
Q_A	bipolar device A	
Q_B	bipolar device B	
R_b	base resistance	Ω
R_{deg}	degeneration resistance	Ω
R_e	emitter resistance	Ω
R_L	load resistance	Ω
r_π	base-emitter resistance	Ω
R_S	source resistance	Ω
R_{series}	series resistance	Ω
R_{stab}	stabilization resistance	Ω
s	Laplace varible	
T	delay	
τ_f	forward base-emitter transit time	s

V	voltage	V
v_{be}	base-emitter voltage	V
v_{be_2}	second-order base-emitter voltage	V
v_{be_3}	third-order base-emitter voltage	V
V_b	base voltage	V
V_c	collector voltage	V
V_{OoB}	Out-of-Band voltage relation	V
v_s	source voltage	V
V_T	thermal voltage	V
Z	impedance	Ω
Z_L	load impedance	Ω
ω	angular frequency	rads^{-1}
ω_p	pole angular frequency	rads^{-1}
ω_z	zero angular frequency	rads^{-1}

To my Family, for their unconditional support.

Chapter 1

Introduction

The use of wireless devices is continuously and rapidly growing over the world. In order to cope with the increasing amount of users and data, the global market is driving the current wireless technologies towards more power and spectrum efficient systems [1]. The expected release of the 5G network in 2020 will impose even more strict requirements on the transceivers bandwidth and efficiency as discussed in [2], [3]. These tendencies directly translate for RF and microwave engineers in very stringent circuit specifications. The improvement of transceivers performance has been therefore a main research topic in the RF community in the last decade. Among the different blocks that compose a transceiver, the Power Amplifier (PA) is committed to amplify the signal and provide the right amount of power that will be then transmitted by the antenna. Because of its requirements on power delivery and its position in the chain, the key figures for PAs are efficiency and linearity. The linearity of the transmitter is crucial for the correct transmission and reception of modern, spectrum efficient digitally modulated signals. These signals are characterized by a very high peak-to-avarage power ratio (PAPR), therefore a very linear amplification of the signal up to very low levels of power back-off is required.
This thesis project focuses on the investigation of circuit techniques to improve the state-of-the-art linearity performance of PAs .

1.1 Motivation

In this section, a description of the circuit to be studied is given together with its performance parameters to be optimized. A comparison between two of the most used technologies for low/medium power PA implementation is given to explain the motivation for the choice of the research topic.

1.1.1 Medium Power Amplifiers

The circuit that we aim to prototype in this thesis work is a Medium Power Amplifier (MPA). As shown in figure 1.1, this block is located at the transmitter back end, and it is either used for driving a High Power Amplifier (HPA) or, in lower power systems, as the last amplifying block before the antenna. As mentioned, the most important

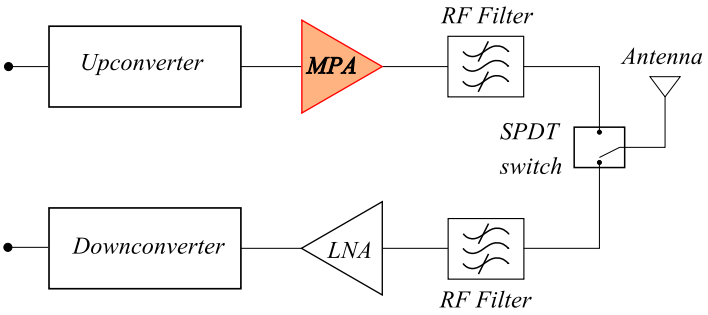


FIGURE 1.1: A block diagram representation of an RF transceiver front end

figures of merit for this block are efficiency and linearity, which have to be maximized while providing the required level of output power. The classical trade-off found in the simultaneous optimization of efficiency and linearity [4] represents a fundamental limitation that creates the need for circuit techniques which aim to overcome it.

1.1.2 SiGe vs GaAs

Over time, various technologies have been developed for radio frequency (RF) power amplifiers. The RF active devices are characterized by a high cut-off frequency f_t and maximum oscillation frequency f_{max}, in order to provide sufficient gain at high operating frequencies. At the same time the breakdown voltage (BV) needs to be optimized to ensure a reliable power handling. In practical devices, the product of the two parameters f_t and BV is limited by a fundamental physical relation known as the Johnson Limit: $BV \cdot f_t = \frac{E_m v_{sat}}{2\pi}$ which is constant for a determined semiconductor material [5]. Typically a choice must be thus made between high speed and high power handling capability.

For the design of this MPA, SiGe Heterojunction Bipolar Transistor (HBT) devices in BiCMOS technology will be used in this work. Silicon devices (like SiGe HBTs) can ensure a higher integration at a significantly reduced cost when compared to III-V devices like GaAs HBTs. However, the latter have several advantages on their silicon counterparts: the $f_t BV$ product of GaAs is generally higher due to their higher bandgap and electron mobility, providing more reliable and efficient operation in power amplifiers. Moreover, GaAs devices show an intrinsically more linear power transfer

compared to SiGe, thanks to the different base charge modulation of the signal swing over the base-collector junction. More specific, the electron mobility in GaAs shows a peak for relatively low values of the electric field ($\approx$ 3x10$^3 V/cm$). The effect of this phenomenon is to reduce the charge carrier concentration in the base-collector depletion region at lower values of the applied electric field, yielding a significant reduction in the base-collector parasitic capacitance of GaAs compared to Si-based devices. We will show later that the base-collector charge modulation has a large impact on the overall linearity of an amplifier.

1.2 Objectives

Based on the comparison in the previous paragraph, the ultimate goal of this work is to fill the gap in the linearity performance between SiGe and GaAs power amplifiers by investigating both existing and new circuit linearization techniques. In the past, many works related to this problem have been published: [6], [7] [8] [9]; the work [10] collects the most common linearization approaches. Among them, we report: *Digital or Analog pre- and postdistortion*: which make use of circuit blocks characterized by an inverse non-linear function that, when multiplied by the one of the amplifier results in a linear output; *Feedback*: that defines the transfer function according to the feedback loop gain and to the feedback network. Depending on the nature of the feedback network, we distinguish between linear and non-linear feedback. *Feedforward*: which uses a replica of the distorted signal, shifted by 180° with respect to the original one, to cancel out the original distortion by signal summation. *In-band cancellation*: in which active or passive components are used to linearize the amplifier, working in the fundamental signal band; *Out-of-band cancellation*: where active or passive components are used to provide determined conditions at the out-of-band frequencies, yielding the cancellation of the non-linear signal. The last technique has an important advantage on the others because it allows to optimize for linearity by only tuning the out-of-band parameters of the amplifier. In this way, the circuit characteristics in the fundamental signal band can still be used to maximize figures like gain and efficiency, without compromising these performance with linearity optimization. For this reason, this work focuses on the investigation of analog techniques which make use of the out-of-band cancellation [8].

1.2.1 Project Goals and Specifications

Here we set a quantitative goal for the MPA performance, representing the final specifications for the circuit. These specifications are derived from a commercialized GaAs based MPA. The targeted amplifier is intended to operate over a bandwidth of 400 MHz,

at a carrier frequency of 2 GHz. These values are chosen because it is the transmission channel utilised for 4G and 4.5G radio access network (RAN) applications. It needs to provide a peak output power of 0.5W, with a gain of 18 dB. A peak output power of half a Watt is a typical value for pico/femto cells base station applications. The amplifier needs to have a single-ended structure and to operate in class AB. For what concerns linearity, a PA is mostly characterized by a figure of merit called "*third order intercept point*" (IP3), which will be precisely defined in Chapter 2. In this thesis work, in which the target output power at the 1 dB compression point is 27 dBm (0.5 W), we aim to achieve an output IP3 (OIP3) of 45 dBm.

1.2.2 Research Questions and Thesis Outline

Based on the considerations made so far, we can define the research questions driving this thesis work: "Which analog circuit techniques, making use of the Out-of-Band concept, can be applied to improve the linearity of SiGe RF amplifiers?", and "Are these techniques feasible to be implemented for the specified practical MPA application?". In this report we try to give an answer to these questions. The contents are divided in seven chapters, which are here briefly summarized:

- **Chapter 1** has introduced the research field, with a zoom into the topic of Power Amplifiers linearization. The reasons for the choice of this topic are explained and the research goals are described.
- **Chapter 2** is used to give a general picture of the problem of bipolar amplifiers linearization. In the first part a review of the nonlinear distortion fundamentals is given. In the second part we characterize the linearity of a bipolar amplifier for simple configurations, highlighting the most important distortion contributions for the target application.
- **Chapter 3** is dedicated to present the starting point of the investigation: the Out-of-Band linearization theory and concepts are explained, and a low power design example is given to show the cancellation condition in simulation. This designed circuit is then scaled up and adjusted to reach the power specifications. The limitations of this approach are described and the conclusions achieved in this way will be used in the performance comparison for the following chapters.
- **Chapter 4** is dedicated to discuss the first of the linearisation techniques developed in this project, which goes under the name of "Out-of-Band Active Injection Compensation". The chapter starts with the derivation of the conditions on the in

band and out-of-band base-emitter voltages for the cancellation of the IM3 collector current. This condition will be then used to describe the operating principle of the linearization technique. Several circuit examples are given and the results of their simulations are discussed. The main limitations that have been encountered using this circuit technique are reported, and several conclusions are drawn upon them.

- **Chapter 5** focuses on the application of the Derivative Superposition technique to Bipolar Amplifiers. First the general concept behind the linearization technique is qualitatively explained, and its implementation using bipolar transistors is introduced. Next, an amplifier topology is proposed and studied making use of a Volterra Series representation. Initially the memory effects are removed from the amplifier, and the solution in this situation is derived; in a second stage these effects are included, and the circuit solution for IM3 distortion cancellation is reported. For each of these cases, a design example is given and the results of its simulation are shown. Also for this technique the main limitations will be finally listed and commented, and suggestions will be given on the directions to take for further investigations.

- **Chapter 6** describes the design process followed for the implementation of the test chip, based on the Derivative Superposition method. First the design choices are explained, and the schematic simulation based on the circuit obtained in this way are shown. Next the layout implementation is described: an analysis of the circuit's most sensitive parts is performed to identify the sources of linearity degradation; and in the meantime the chip layout is designed, according to the sensitivity analysis and the results of Momentum simulations. The final performance achieved with the designed amplifiers is presented and several conclusions are given.

- **Chapter 7** reports the results of the measurements performed on the designed test chips. Initially the used measurement setup is described: the printed circuit board (PCB) used to supply the power to the chip is presented together with the system used to actually measure the linearity in terms of power distributed in the IM3 components. The measurement tools are characterised by a certain dynamic range, which is considered here in relation to the power levels of the chip. Finally the results of the measurements will be shown, and several conclusions on their meaning will complete the chapter.

- **Chapter 8** is where the overall thesis content is summarized and the main conclusions are reported, first for the different linearization enhancement techniques investigated in this work, and finally in relation to the topic of PA linearization as a general research field.

Chapter 2

Background Theory

Before starting to investigate a new linearization technique, we will first review the basic linearity concepts and metrics. Next, we will identify the main mechanisms that contribute to distortion in a bipolar transistor, and study their impact on the linearity when it is configured as a simple common emitter (CE) amplifier stage.

2.1 Linearity Fundamentals

Here we give a review of the basic theory of nonlinear distortion analysis. The introduced notation will be used in the rest of this report to quantify and compare the linearity performance. For all the notation and equations defined in this section we refer to the books [11] and [12].

2.1.1 Power Series Analysis

Let us start considering a general non-linear system. When the output value of this system $y(t)$ at the moment t_0 only depends on the value of the input $x(t_0)$ at the same time moment, we can analytically describe its non-linear behavior using the Power Series representation:

$$y(t) \approx a_0 + a_1 x(t) + a_2 x^2(t) + ... + a_m x^m(t) \tag{2.1}$$

where the terms a_i are the Taylor coefficients of the function $y(x(t))$. When a time varying signal is used to excite such a system, the non-zero Taylor coefficients result in

the generation of spurious components in the output frequency spectrum. For example, if we excite our nonlinear system with an input signal made of two sinusoids:

$$x(t) = Acos(\omega_1 t) + Acos(\omega_2 t) \tag{2.2}$$

we will find that the output is composed of several sinusoids at frequencies which are a linear combination of ω_1 and ω_2. If we truncate the power series representation 2.1 at the third order, we can write the output signal representation replacing equation 2.2 in 2.1:

$$\begin{aligned} y(t) =& a_2 A^2 + \left(a_1 A + \frac{9}{4} a_3 A^3\right) cos(\omega_{1,2} t) + \frac{1}{2} a_2 A^2 cos(2\omega_{1,2} t) + \\ & \frac{1}{4} a_3 A^3 cos(3\omega_{1,2} t) + a_2 A^2 cos((\omega_{1,2} \pm \omega_{2,1}) t) + \\ & \frac{3}{4} a_3 A^3 cos((2\omega_{1,2} \pm \omega_{2,1}) t) \end{aligned} \tag{2.3}$$

In this expression, only the term $a_1 Acos(\omega_{1,2} t)$, proportional to the first order Taylor coefficient a_1, is the wanted output component resulting from the linear amplification of the input signal. All the other terms originate from higher order coefficients and are therefore "distorting" the overall output signal. Those terms which fall at a multiple of one of the input frequencies ($n\omega_{1,2}$) are called *Harmonic Distortion* (HDn) components, while the ones whose frequency is a combination of the input tones ($n\omega_1 \pm m\omega_2$) are called *Intermodulation Distortion* (IMn) components. If we include in eq 2.1 the terms up to the fifth power, we will observe in the output frequency spectrum additional spurious components generated by fourth and fifth order mixing. Figure 2.1 shows the output frequency spectrum of a 5^{th} order non-linear system excited by a two-tone input signal, up to the second harmonic band. Of major importance in the applications of RF power amplifiers are the terms generated by 3^{rd} and 5^{th} order intermodulation distortion: IM3 and IM5, depicted in red in figure 2.1. This is because these components fall at the frequencies $2\omega_{1,2} - \omega_{2,1}$ (IM3 & IM5) and $3\omega_{1,2} - 2\omega_{2,1}$, (only IM5); therefore they are adjacent to the fundamental signal band and cannot be easily filtered out.

The amount of distortion in PAs is typically quantified by the ratio between the fundamental and the IM3 and/or IM5 output power components. The output third order intercept point *OIP3* is the most used metric to quantify power distortion at high back-off level, which is defined as

$$OIP3 = P_{out,fund} + \left(\frac{P_{out,fund} - P_{out,IM3}}{2}\right) \tag{2.4}$$

where $P_{out,fund}$ and $P_{out,IM3}$ are the output power components at the fundamental and IM3 frequency respectively, expressed in dBm. The *IM3* figure is used instead to define

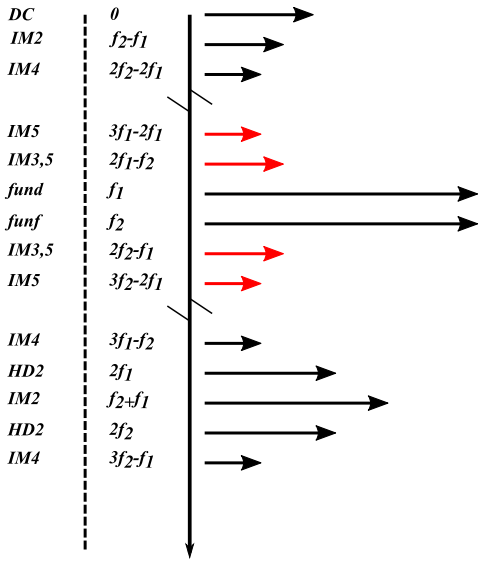


FIGURE 2.1: The output frequency spectrum of a fifth order nonlinear system excited by a two-tone input signal.

linearity over a range of input power, and it is defined as:

$$IM3_{P_{in0}} = |P_{out,fund} - P_{out,IM3}|_{P_{in0}} \tag{2.5}$$

where the output power quantities are again expressed in dBm, and the IM3 in dBc. This latter figure of merit is more useful in systems that include higher order effects and as such does not always follow the 3:1 slope relation between input and output power. The same figures can be defined to quantify the distortion present at the IM5 frequencies. In this work we focus on the optimization of the OIP3 linearity parameter, as this is the one specified in the amplifier performance requirements.

2.1.2 Volterra Series Analysis

When memory effects are present in the system in exam, the power series analysis has to be generalized to take into account the frequency dependency of the system response. In this project, this will be accomplished making use of the Volterra Series representation. In this representation, a non-linear system is described by a combination of operators of various order: H_1, H_2, H_3, ..., H_n. The first order operator is the linear transfer function of the system, while the higher order operators are responsible for the non-linear part contained in the output signal. In this sense we can think about the Volterra Series as a generalized case of the Taylor Series, where the non-linear coefficients are replaced by "non-linear transfer functions". The overall output is obtained by the sum of the first

and higher order transfer functions. In the time domain:

$$y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + ... \tag{2.6}$$

The representation through Volterra Series will be used to analyze the different mechanisms of distortion generation in a bipolar device and to analytically describe the investigated linearization techniques. In particular, a method to analyse nonlinear electrical networks through the Volterra Series Analysis called the *nonlinear current sources method* will be used. This method makes use of current signals which are generated by the mixing of several frequency components, which are exciting the non-linear system. These resulting nonlinear currents are modelled in the schematic as current sources and their effect on the overall circuit can be described using small-signal analysis, superposing the effect of each current source. In this way, each distortion contribution can be studied separately, allowing to compare their interaction and their influence on the overall amplifier linearity. For a more detailed explanation of the Volterra Series Analysis and the non-linear current sources method we refer to [11].

2.2 Linearity of Bipolar Amplifiers

In this section, we describe the principles that are causing distortion in a bipolar transistor. First, the physical mechanisms that generate distortion are identified. Next, the effects of these non-linear relations on the power transfer of an amplifier in CE configuration are studied.

2.2.1 Physical Causes of Distortion

If we assume the transistor to be biased in the forward active region[1], the main non-linear contributions inside a bipolar device are [13]:

- the exponential base-emitter voltage to collector current transfer characteristic:

$$I_c = I_s \exp\left(\frac{V_{be}}{n_F V_T} - 1\right)\left(1 + \frac{V_{cb}}{V_{AF}}\right) \tag{2.7}$$

  where n_F is the forward emission coefficient, $V_T = \frac{kT}{q}$ is the thermal voltage and V_{AF} is the forward Early voltage. This simplified equation can be used when the

[1] this assumption is justified assuming class AB operation of the amplifier

transistor is operating in the low injection region and the Early effect is linear. Together with the collector current, we group the tracking nonlinearities governed by the same exponential relation: the base current

$$I_b = \frac{I_c}{\beta_f} + I_{SE} \exp\left(\frac{V_{be}}{n_E V_T}\right) \tag{2.8}$$

where the second term in the expression accounts for the recombination current and is generally negligible, and the base-emitter injected charge

$$Q_d = \tau_f I_c \tag{2.9}$$

in which τ_f is the minority carriers forward base-emitter transit time;

- the voltage dependence of the base-collector depletion capacitance:

$$C_{jc} = \frac{C_{j0}}{\left(1 - \frac{V_{bc}}{V_{bi}}\right)^{m_j}} \tag{2.10}$$

where C_{j0} is the value of the small-signal capacitance when no bias is applied across the junction, V_{bi} is the junction built-in voltage, V_{bc} is the applied base-collector voltage and m_j is a parameter that depends on the junction doping profile. In practical devices, the C_{jc} is also dependent on the collector current density due to the base-collector junction charge modulation that is caused by high current effects;

- the avalanche current generation in the base-collector depletion region:

$$I_{cb} = I_c(M - 1) \tag{2.11}$$

in which M is called the *avalanche multiplication factor* and is given in [13] as an empirical function

$$M = \frac{1}{1 - (V_{cb}/V_{cbo})^m}, \tag{2.12}$$

- the dependence of the base-emitter transit time τ_f on the collector current density J_c:

$$\tau_f = q \int_0^{W_b} \frac{\Delta n(x)}{\Delta J_n(x)} dx \tag{2.13}$$

where q is the electron charge, W_b is the base neutral region width, $n(x)$ is the minority carrier density in the same region and $J_n(x)$ is the electron current density within the base. The variations of $\frac{n(x)}{J_n(x)}$ as a function of the depth x determine the dependency of τ_f on J_c [14] .

These non-linear effects can be more or less visible depending on the operation of the amplifier. In the next paragraph, we will show which contributors dominate the distortion in the different biasing regions.

2.2.2 Linearity Characterization of a CE stage

We discuss here the influence of the various distortion contributors on the overall linearity by analysing a simple CE amplifier topology. To simulate the behavior of this circuit

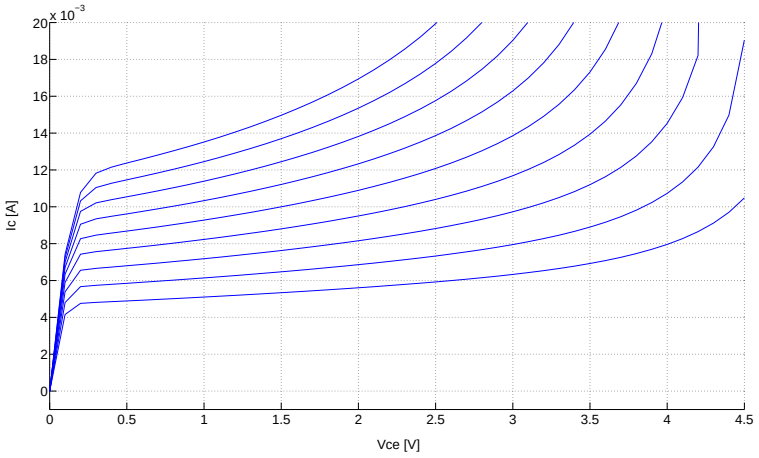


FIGURE 2.2: DC characteristic curves for the bnpahv SiGe HBT with an emitter area of 0.5x20.7x2μm^2.

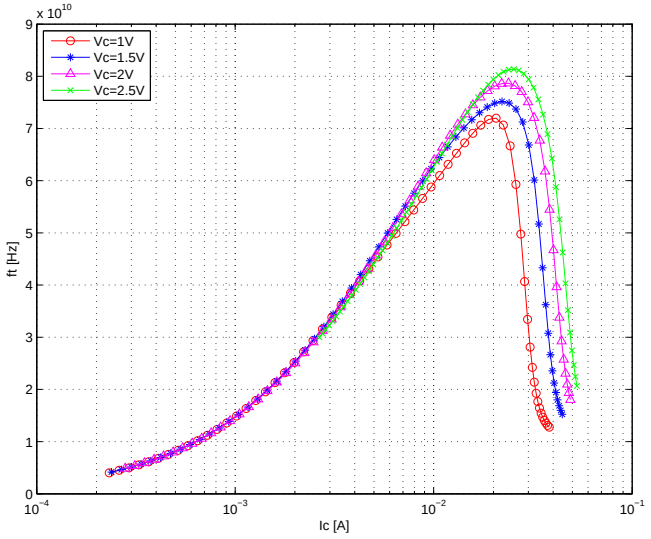


FIGURE 2.3: Transition frequency f_t curves versus collector current for different values of the collector voltage for the bnpahv SiGe HBT with an emitter area of 0.5x20.7x2μm^2.

in realistic conditions, we use the Mextram model of a SiGe HBT. This model does not allow to separate single non-linearity contributions described in the previous paragraph.

To get some insight in the way the distortion contributions influence the linearity for different biasing points, we plot the IP3 contours behaviour versus both DC collector current I_c and voltage V_c. For our simulations, we will use as a reference device a QUBiC4Xi *bnpahv* SiGe HBT from NXP with two emitter fingers, each one having an area of 0.5x20.7μm^2 . The figures 2.2 and 2.3 show some basic characterization curves to give an idea of the current and voltage handling capability of the device. As may be seen, the level of applied V_{ce} at which avalanche breakdown effects start to be visible depends on the current level. We can anyhow define an approximate threshold value of $V_{ce} < 3V$ for a safe operation. In fig 2.3 the f_t over the collector biasing current I_c is plotted for different values of V_c. The figure shows that a peak in the value of f_t occurs for a current of approximately $I_{c,@peak f_t} = 25mA$, when $V_c = 2.5V$. The circuit used to test the linearity contributions is shown in figure 2.4 and represents a simple CE stage terminated with 50Ω source and load impedances. On the described schematic, a 2-tone simulation is performed when the quiescent current I_c and collector biasing voltage V_c are swept. The details of the simulation are reported in table 2.1. Fig 2.5

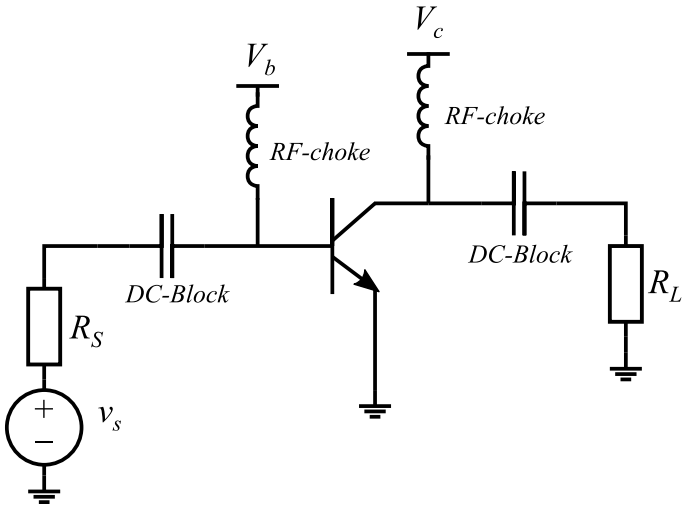


FIGURE 2.4: Circuit used to characterize the IM3 linearity of the SiGe HBT device employed in this research project.

P_{avs}	-40	dBm (per tone)
f_c	2	GHz
Δf	1	MHz

TABLE 2.1: The simulation parameters used to plot the OIP3 contours of the circuit in exam.

shows the IP3 contours resulting from this simulation in the output plane. In this plot we can distinguish 3 macro regions, where 3 different distortion mechanisms dominate the overall linearity of the amplifier:

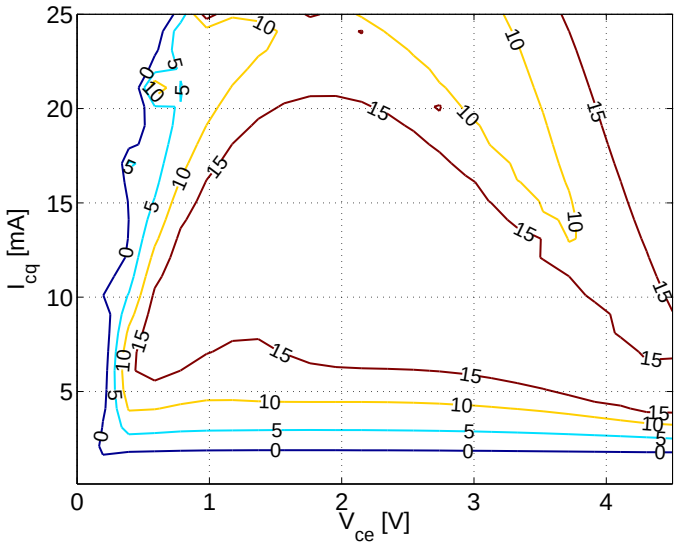


FIGURE 2.5: OIP3 contours (in dBm) plotted versus collector current and voltage for a 0.5x20.7x2μm^2 *bnpahv* SiGe HBT.

1. **The exponential dominated region**: we can observe that at very low current densities ($Ic < 4mA$) the OIP3 curves hardly depend on the V_{ce} biasing voltage, while they show a clear dependency on the level of current. This suggests that in this region the dominant contributor to distortion is the exponential voltage-to-current relation.

2. **The base-collector capacitance dominated region**: as the current density becomes larger, the curves start to show a more evident dependence on the V_{ce}. This is due to the non-linear voltage-to-charge relation of the base-collector capacitance, which starts to dominate in this region.

3. **The avalanche dominated region**: at values of the collector voltage higher than $V_{ce} \approx 3V$, the distortion is strongly influenced by avalanche breakdown effects occurring due to the high electric field in the base-collector space charge region.

In general, operation in the avalanche-dominated region is avoided in amplifiers design for reliability constraints. We focus thus on the exponential and the base-collector depletion capacitance distortion contributions, and their relation to the amplifier topology and region of operation. We start with a CE stage, and study in which biasing regions the exponential distortion is dominating, and in which others the C_{bc} is limiting the linearity. We have seen from figure 2.5 that at low current levels the exponential relation dominates the IP3 level. Now we study in more detail the influence of the C_{bc} distortion on the extension of this region. In particular, since the C_{bc} distortion comes from the voltage swing developed over the load impedance, we plot the OIP3 versus the current density for different values of an ohmic load impedance. In doing this we measure the

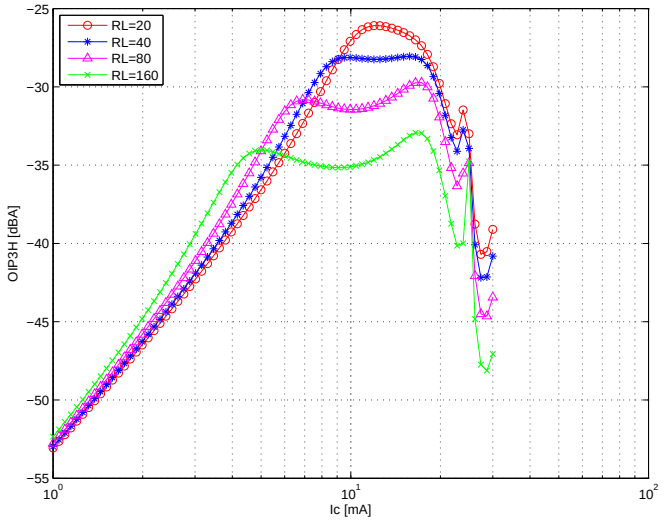


FIGURE 2.6: The CE stage output current IP3 curves in dBA plotted versus collector current for different values of the load impedance.

OIP3 linearity of the amplifier in dBA, which is expressed as:

$$OIP3_{dBA} = 20log\left(\frac{I_{OIP3}}{1A}\right) \tag{2.14}$$

where I_{OIP3} is the current at the output third order intercept point. This figure quantifies the amplitude ratio between the fundamental and the IM3 current signals coming out of the transistor, so it solely gives information on the device transfer linearity. Instead, the power OIP3 expressed in dBm is dependent on the load impedance value as this transforms the output current in power, losing the information on the amount of distortion which comes only from the device. Therefore, the current OIP3 expressed in dBA only shows the influence of the load on linearity rather than on the level of output power. For this reason it will be used here to show the effect of the load impedance on the device transfer linearity alone, independently on the overall output power. As we can see in figure 2.6, the C_{bc} distortion starts to dominate at values of the collector current I_c that, while depending on the value of R_L, are above 5 mA. This represents

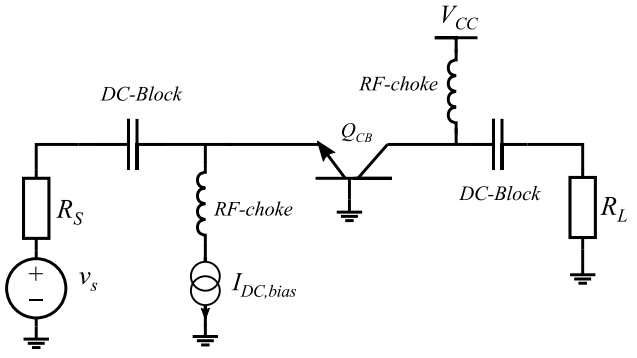


FIGURE 2.7: The test bench used to characterize the distortion of a CB stage.

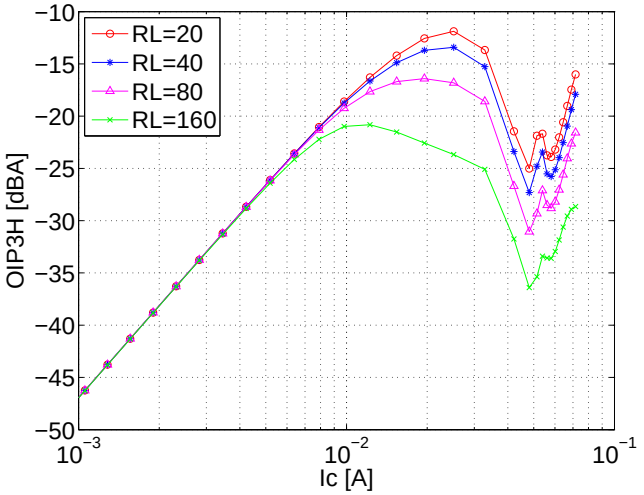


FIGURE 2.8: The CB stage Output current IP3 curves in dBA plotted versus collector current for different values of the load impedance.

a major problem in PA design, since high current density operation is usually employed to boost the amplifier efficiency. This limitation may be partially solved by applying a cascode configuration, where the CE stage is loaded with a CB stage. The latter is characterised by a very low input impedance, which reduces the voltage swing over the collector of the CE stage and consequently also the C_{bc} distortion. However, in all cases the output voltage swing needs to be high enough to provide the wanted amount of power; so that also in a cascode configuration the CB stage needs to be loaded with a relatively high R_L. To check how this limits the performance of a cascode topology, we analyse the linearity dependency of the CB stage on the collector current, collector biasing voltage and load impedance. For this test, the schematic of figure 2.7 has been used, where the source impedance is set to 50Ω and the emitter current is swept to check the linearity behaviour over bias. We bias the collector at $V_c = 1.8$ V and plot the OIP3

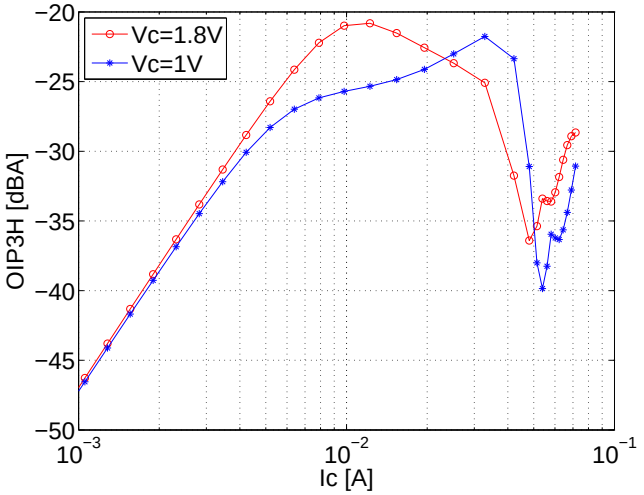


FIGURE 2.9: The CB stage output current IP3 curves in dBA plotted versus collector current for different values of the collector biasing voltage.

versus collector current for several values of R_L. We can see in figure 2.8 that in this case the achievable linearity in terms of dBA is higher than the CE stage. However, it is still possible to see the same kind of dependency of the linearity on the value of the load impedance. Also in this case this is due to the increasing voltage swing over the base-collector junction as the load value increases. Now, to check the influence of the collector biasing voltage on the C_{bc} distortion we simulate again the circuit of figure 2.7, this time using a fixed value for the load impedance while changing the collector biasing voltage. In figure 2.9 the OIP3 curves are plotted over collector current for a value of $R_L = 160\Omega$, but for different value of V_c. It is possible to observe that for lower DC values of V_c the C_{bc} starts to dominate the distortion at a lower current density. It becomes then crucial in the choice of the load impedance and of the output biasing voltage to understand the limitation encountered in minimizing the exponential and C_{bc} generated distortion and maximizing the output power.

2.3 Conclusions

In this chapter, the background theory for the bipolar amplifiers distortion analysis has been introduced. First a review of the linearity definitions and analysis methods was given. Second, we reported a general summary of the main non-linearities in bipolar devices, studying their effects on a CE stage amplifier. In particular, we saw that the CE stage distortion is dominated by the exponential voltage to current relation at low current levels, while the C_{bc} distortion starts dominating at high current levels and is highly dependent on the value of the load impedance. We then introduced the cascode topology as a solution to suppress C_{bc} distortion of a single CE stage, emphasizing the importance of the load impedance value in the optimization of the linearity/efficiency trade-off. In the following chapters, we will focus on the linearization of the exponential distortion in CE topologies, assuming that the application of a cascode architecture suppresses the C_{bc} distortion to a satisfactory level. For techniques that aim to the suppression of the distortion generated by the base-collector capacitance, we refer to the work [15].

Chapter 3

Out-of-Band Matching and Power scaling

As discussed in Chapter 2, especially when used in a cascode configuration, the linearity of a CE stage is dominated by the exponential voltage-to-current relation of bipolar transistors.
In past years, this non-linear phenomenon has been studied [16] [6] and several approaches to linearize it have been presented [8], [7]. In this chapter we introduce the technique proposed in [8] for the linearization of the exponential distortion in bipolar amplifiers. A design example based on this method is given, and subsequently scaled in order to achieve the power specifications described in the first chapter. A conclusion is eventually drawn on the advantages and the limitations of this approach. We will see that the constraints encountered by this technique limit its application in practical amplifiers, and will represent the starting point for the investigation in the following chapters.

3.1 Out-of-Band Linearization

Let us consider again a simple CE stage, in which we include the transistor parasitic resistances and capacitances, as well as general terminations at the transistor nodes. The small-signal model of this configuration is depicted in figure 3.1. In this model we neglect the collector-base capacitance to simplify the equations. The generality of the solution is preserved insofar as a low R_L is used, which ensures a low collector voltage swing and consequently reduces the feedback effect of the C_{bc}. When only the exponential contribution to distortion is considered, assuming an excitation signal composed by two tones at the frequencies ω_1 and ω_2, the 3^{rd} order non-linear collector current $i_{c,NL3}$ can

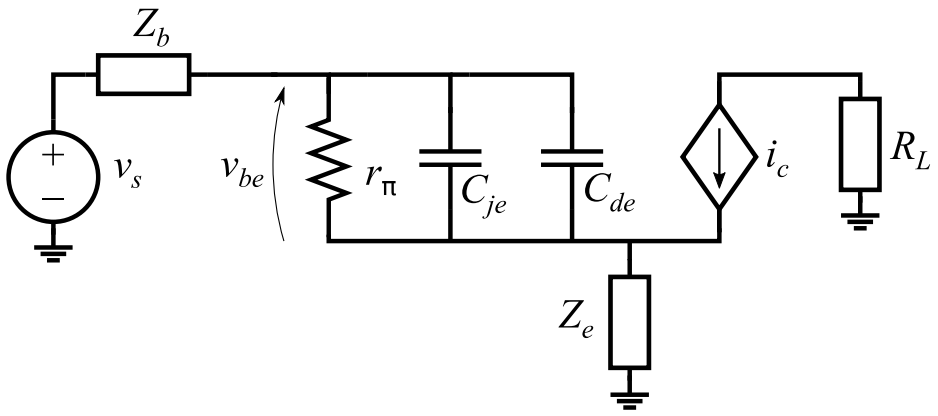


FIGURE 3.1: Simplified small signal model of a CE stage used for the analytical description.

be expressed in the Laplace domain using a Volterra Series expansion in the following way [6]:

$$\begin{aligned} i_{c,NL3} &= K_{3gm} v_{be}(s_a) v_{be}(s_b) v_{be}(s_c) + \\ &+ \frac{2}{3} K_{2gm} \left[v_{be2}(s_a, s_b) v_{be}(s_c) + v_{be2}(s_a, s_c) v_{be}(s_b) + v_{be2}(s_b, s_c) v_{be}(s_a) \right] + \\ &+ g_m v_{be3}(s_a, s_b, s_c) \end{aligned} \tag{3.1}$$

where:

$$g_m = \frac{\partial I_c}{\partial V_{be}}; \qquad K_{2g_m} = \frac{1}{2} \frac{\partial^2 I_c}{\partial V_{be}^2}; \qquad K_{3g_m} = \frac{1}{6} \frac{\partial^3 I_c}{\partial V_{be}^3} \tag{3.2}$$

and $s = j\omega$ is the Laplace variable. The term $v_{be}(s_i)$ is the AC component at the frequency ω_i of the voltage across the base-emitter junction; while $v_{be2}(s_i, s_j)$ and $v_{be3}(s_i, s_j, s_k)$ are the AC components at the frequencies $(\omega_i \pm \omega_j)$ and $(\omega_i \pm \omega_j \pm \omega_k)$ respectively. Equation 3.1 represents any third-order mixing product, both IM3 and HD3, at the frequency $\omega_a \pm \omega_b \pm \omega_c$. Here a, b, c can be any combination of the input tones and are interchangeable as the expression is symmetric. Since we are interested in the inband low and high IM3 components, we set $\omega_a = \omega_b = \omega_1$, $\omega_c = -\omega_2$ for the IM3L, and $\omega_a = \omega_b = \omega_2$, $\omega_c = -\omega_1$ for the IM3H.

When the actual frequency values are replaced into the equation, we obtain the expression of the IM3 low and high collector current:

$$
\begin{aligned}
i_{c,IM3} &= K_{3gm} v_{be}(s_{1,2}) v_{be}(s_{1,2}) v_{be}(-s_{2,1}) + \\
&+ \frac{2}{3} K_{2gm} \left[v_{be2}(s_{1,2}, s_{1,2}) v_{be}(-s_{2,1}) + v_{be2}(s_{1,2}, -s_{2,1}) v_{be}(s_{1,2}) + v_{be2}(s_{1,2}, -s_{2,1}) v_{be}(s_{1,2}) \right] + \\
&+ g_m v_{be3}(s_{1,2}, s_{1,2}, -s_{2,1})
\end{aligned}
\tag{3.3}
$$

Here the notation $v_{be}(s_{1,2})$ is used to specify that each term should be used with the first numbering to express the IM3 low, or with the second numbering for the IM3 high. In the right hand side of equation 3.3 we can separate three terms, that also represent the different mechanisms in which IM3 components are generated:

1. The first term, proportional to K_{3g_m}, is the part of $i_{c,IM3}$ that results from a third order interaction of the input frequency components $v_{be}(s_{1,2})$;
2. The second term, proportional to K_{2g_m}, originates instead from a second-order interaction between the input excitations $v_{be}(s_{1,2})$ and the components generated by second order mixing $v_{be2}(s_{1,2}, s_{1,2})$ and $v_{be2}(s_{1,2}, -s_{2,1})$;
3. The last term, proportional to the transconductance g_m, is the linear transfer of the base-emitter voltage component at the IM3 frequencies $v_{be3}(2s_{1,2}, -s_{2,1})$

One important conclusion we can draw from this analysis is that IM3 signals can also appear at the output of a system whose power series representation only contains terms up to the second order. This phenomenon occurs whenever a feedback network is placed in combination with the main transfer. In this case, the feedback effect is caused by the emitter degeneration impedance and the base current. The mixing of feedback components with the input excitation signals is called *indirect mixing* and will be a topic of major focus in this and in the next chapters because of its role in the linearization techniques. Now we rewrite the expression of the IM3 nonlinear collector current to underline and analyse the contribution of the indirect mixing. We refer all the terms in eq 3.3 to the fundamental voltages, and disregard the last term proportional to $v_{be3}(2s_{1,2}, -s_{2,1})$. This is justified because we aim to set $i_{c,NL3} = 0$, therefore , when this is achieved, no 3rd order currents are fed back to the input and no modulation of the base-emitter voltage at the IM3 frequencies occurs. The first and second order voltages can be grouped, yielding the expression 3.4 of the IM3 collector current [8]. For ease of notation we only express the IM3L, but the same analysis holds for the IM3H.

$$
i_{c,IM3L} = \epsilon(s_1, s_1, -s_2) v_{be}(s_1) v_{be}(s_1) v_{be}(-s_2) \tag{3.4}
$$

In this expression, ϵ is equal to :

$$\epsilon(s_1, s_1, -s_2) = K_{3gm} - \frac{2}{3}K_{2gm}^2 \left[2B(s_1 - s_2) + B(s_1 + s_1)\right] \tag{3.5}$$

and

$$B(s) = \frac{\frac{Z_b}{\beta_f} + Z_e + s[\tau_f(Z_b + Z_e)]}{1 + g_m\left(\frac{Z_b}{\beta_f} + Z_e\right) + s[C_\pi(Z_b + Z_e)]} \tag{3.6}$$

In the schematic of figure 3.1, the function $B(s)$ represents the feedback transfer from the (nonlinear) collector current back to the base-emitter voltage, and it has therefore the dimensions of an impedance. In equation 3.5 it appears at the frequencies $s_1 - s_2 = \Delta s$ and $s_1 + s_1 = 2s_1$, which are responsible for the contribution of the indirect mixing to the total IM3 current. From equation 3.5 we can note that the indirect mixing contribution to IM3 has opposite sign of the direct mixing. This means that if we set the impedances Z_e and Z_b in the IM2 bands such that $2B(s_1 - s_2) + B(2s_1) = \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}^2}$, we can make the two terms cancel each other, yielding $i_{c,IM3L} = 0$.

3.1.1 Emitter and Base Compensation

This concept, called out-of-band matching, is used and explained in [8]. In this work, the conditions on the value of B(s) at the baseband $\Delta s = s_1 - s_2$ and at the 2$^{\text{nd}}$ harmonic band $2s1$ to cancel the exponential distortion are derived for low and high frequency operation. In general, the function B(s) contains both the base and the emitter impedances, meaning that a combination of the two should be set in order to achieve the cancellation. In [8] a distinction is made between *base compensation* (or base-tuning), in case we set the wanted base impedance and short the emitter terminal; and *emitter compensation* (or emitter-tuning), in the dual case. We first write here the cancellation conditions when ohmic impedances are utilised. When base compensation is used ($Z_e = 0$), the condition for IM3 cancellation is [8]:

$$Z_b = R_b = \frac{\beta}{2g_m} \tag{3.7}$$

If we use emitter compensation instead ($Z_b = 0$), we need to set [8] :

$$Z_e = R_e = \frac{1}{2g_m} \tag{3.8}$$

These conditions equalise the magnitude of the direct and indirect IM3 components. They are sufficient in low frequency operation, i.e. when the impact of the nonlinear base-emitter diffusion charge is negligible. At high frequency operation, the reactive part has to be compensated as well, which can be done by setting a ratio between the

diffusion and the depletion base-emitter capacitances [8]:

$$2g_m\tau_f = C_{je} \tag{3.9}$$

This latter condition, combined with the one for the ohmic part, ensures phase alignment between the direct and indirect IM3 components. The use of emitter compensation is in general preferable over the base compensation for the following reasons:
First, when we utilize base compensation, we need to provide well defined out-of-band impedances at the base, which may interfere with biasing circuitry at the base node as well as with the network used to provide input matching. Using emitter compensation instead, the base node can be shorted for the out-of-band frequencies, which is an easier condition to implement and it makes the cancellation independent on external loading at the input port. Second, if the reactive part is not properly compensated, i.e. $2g_m\tau_f \neq C_{je}$, emitter compensation provides a linearity improvement over a broader bandwidth thanks to the β times higher frequency roll-off [8]. We will therefore make use of the emitter compensation technique in this work. When equation 3.9 cannot be satisfied, for example because we want to set a different bias current to optimize other performance parameters, we can still compensate the reactive part by allowing complex values for the 2$^{\text{nd}}$ harmonic impedance $Z_e(2s)$:

$$Z_e = \frac{1}{2g_m + s(2\tau_f g_m - C_{je})} \tag{3.10}$$

Equation 3.10 shows that when $C_{je} < 2\tau_f g_m$, Z_e can be implemented by the parallel combination of a resistor $R_e = 1/2g_m$ and a capacitor $C_e = 2\tau_f g_m - C_{je}$. In the case that $C_{je} > 2\tau_f g_m$, the circuit solution consists of a resistor in series or in parallel with an inductor. In this last case, for each frequency ω_x there is only one value L_{ex} of the inductor which satisfies the equation. Therefore this solution is not applicable to practical wideband implementations.

3.2 Power and Linearity Scaling

In this section we try to understand the suitability of an Out-of-Band based circuit when used in the implementation of the MPA described in Chapter 1. To do this, we make use of an example design with a unit area device, and then scale it up in order to achieve the wanted power levels.

3.2.1 Emitter-Compensated Design Example

For the linearity improvement of the circuit, the emitter-compensation method introduced in the previous section is used. The source and load impedance are set to 50Ω. In order to show the effectiveness of the Out-of-Band technique, we first utilize in our simulations a Gummel-Poon (GP) model of a bipolar transistor. This model allows to set the value of the parasitic components inside a bipolar transistor. Table 3.1 shows the param-

Parameter	**Value**	**Dimension**
Area	2	mult
I_s	$1.2 \cdot 10^{-15}$	A
β_f	2000	-
C_{je}	0.3	pF/mult
V_{je}	0.7	V
m_{je}	1/3	-
C_{jc}	0	pF/mult
Vjc	0.7	V
m_{jc}	1/3	-
τ_f	2	ps

TABLE 3.1: Gummel-Poon device model parameters used for the simulation of the emitter-tuning design example.

eters used to characterize the model. Note that in this example we set $C_{jc} = 0$ to exclude the influence of the base-collector capacitance from the simulation. The schematic used

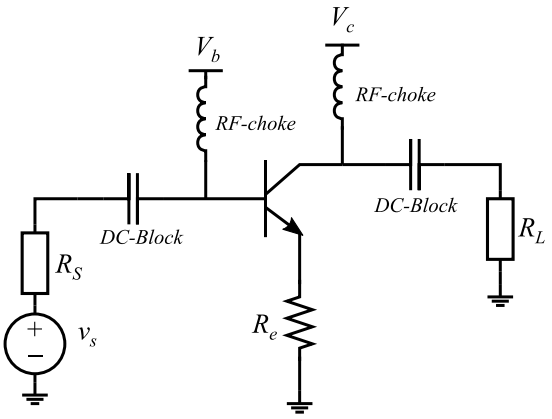


FIGURE 3.2: Schematic of the emitter-tuning design example.

to test the technique is represented in figure 3.2, and the simulation parameters are listed in table 3.2. If we sweep the degeneration resistance R_e and the collector current I_c, we can observe in figure 3.3 a sharp optimum combination of these values for which the OIP3 peaks. These values correspond to the theoretical ones: $R_e = 1/2g_m$ and $g_m = C_{je}/2\tau_f$. We set the degeneration resistance to its optimum value $R_e = 1.7\ \Omega$. Consequently, the low power optimum biasing current is $I_c = 7.6$ mA.
If we plot the OIP3 over an increasing input power, we observe in figure 3.4 that a sweet

f_0	2	GHz
Δf	10	MHz
R_S	50	Ω
R_L	50	Ω

TABLE 3.2: Simulation parameters used for the simulation of the emitter-tuning design example.

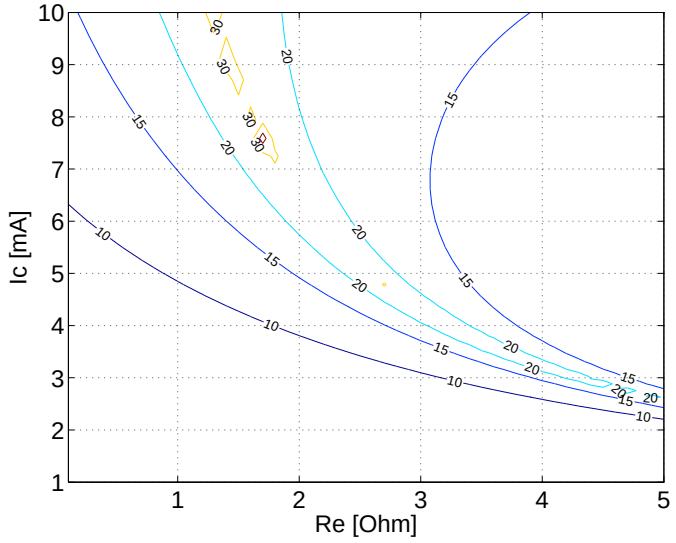


FIGURE 3.3: The OIP3 contours in dBm resulting from a 2-tone simulation of the described emitter-compensated circuit.

spot exists when the biasing point is shifted to slightly higher values of the collector current. This phenomenon is due to the (partial) cancellation of 3^{rd} and 5^{th} order mixing

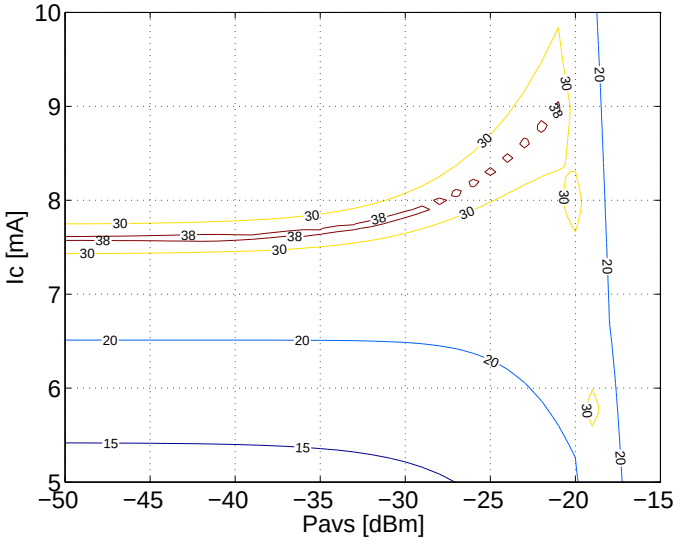


FIGURE 3.4: The OIP3 contours in dBm for the described circuit for different levels of input power and collector quiescent current.

products, which are opposite in phase and, for a certain amplitude of the input signal, approximately equal in magnitude [8]. For this reason, when out-of-band matching is

used, a choice must be made on exploiting the cancellation either at lower power or at higher power [17].

3.2.2 Effects of Base-Collector Capacitance

Now we include in the device model the base-collector parasitic capacitance. We first introduce a capacitance with a linear voltage-to-charge relation, to see its impact on the amplifier linearity. We take again our emitter compensated CE stage, and add

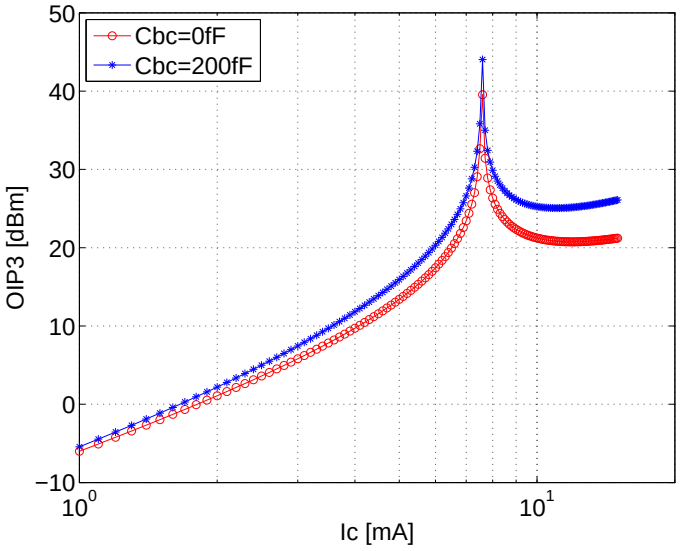


FIGURE 3.5: Comparison of the OIP3 figure plotted against the quiescent collector current for a device with no C_{bc} and one with a linear C_{bc}.

a linear capacitor between the base and collector nodes with a value of $C_{bc} = 200$ fF, as shown in figure 3.6. We plot the OIP3 vs collector current, and compare the

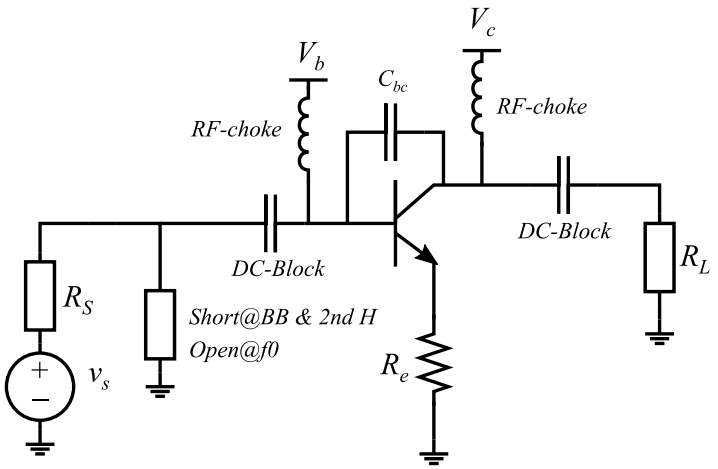


FIGURE 3.6: The circuit used to simulate the effect of the base-collector capacitance on the amplifier linearity.

results with the case where $C_{bc} = 0$ in figure 3.5.As can be seen, the IP3 peak is

maintained. This is because the base node is shorted at the BB and 2ndH band, such that the IM2 currents fed back through the C_{bc} cannot generate indirect mixing. We will see in Chapter 6 how the separation of the IM2 collector currents loop from the input influences the implementation of layout of the designed amplifier. Now we want

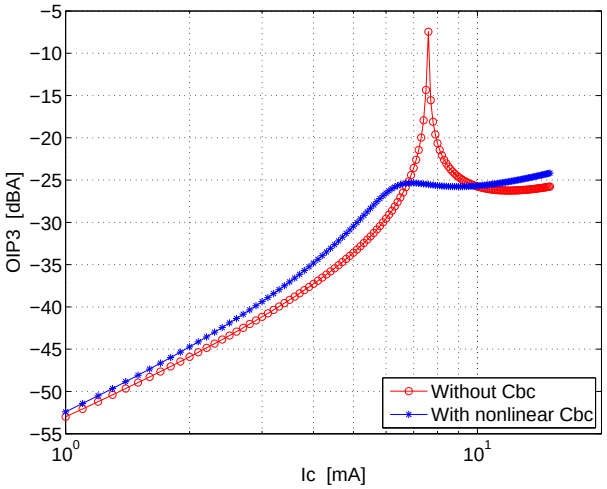


FIGURE 3.7: OIP3 versus collector current comparison between a device with and without the non-linear C_{bc} .

to see the effect of the non-linear base-collector depletion capacitance on the emitter compensated circuit, and we set therefore $C_{jc} = 300$ fF in the GP model, which results in a total C_{bc} of about 200 fF for the used biasing conditions. As can be seen in figure 3.7, the distortion introduced by the C_{bc} eliminates the IP3 optimum generated by the exponential distortion cancellation. This means that in this operating region, and with these device parameters, the C_{bc} distortion dominates. To show the influence of the

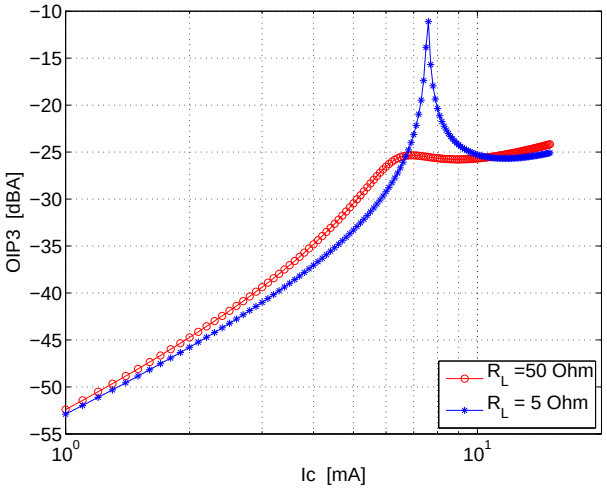


FIGURE 3.8: OIP3 versus collector current comparison between a device with and without the non-linear C_{bc} .

output load on the distortion introduced by the C_{bc}, we repeat the same simulation for

a different value of the load impedance R_L. In order to make a fair comparison, we use the dBA unit defined in Chapter 2 to measure the linearity of the stage. Figure 3.8 shows the OIP3 curves over the collector current for the two cases: the first shows the degradation in the linearity level introduced by the non-linear C_{bc}, and the second curve plots the OIP3 level for the same device, terminated with a load impedance of $R_L = 5\Omega$. We can see that in the last case the dBA linearity level is back to the values of the circuit with no C_{bc}. This result shows that output power can be traded for collector current linearity in a CE stage amplifier. This is the motivation that will lead to opt for a cascode configuration in Chapter 6.

3.2.3 Circuit Power Scaling

The emitter compensated design example with the GP BJT model reported in the previous paragraph achieves a peak output power much lower than the one mentioned in the specifications. In order to increase the level of delivered power at the output, we need to up-size the design. For this purpose, we make use of the Mextram model of a SiGe HBT, since it includes 2^{nd} order effects which make the simulation results more realistic when dealing with high current/power levels. In particular this model already includes the intrinsic parasitic resistances at the device terminals. We start from the design of a unit-cell circuit with the Mextram model. To find the optimum combination of R_e and I_c we sweep these parameters and plot the IP3 contours. Figure 3.9 shows that an optimum exists for a value of $R_e = 2.3\ \Omega$, which is smaller than the theoretical one. This is because the Mextram model includes already the series emitter resistance of the device. Once we have found the optimum operating point for linearity at low

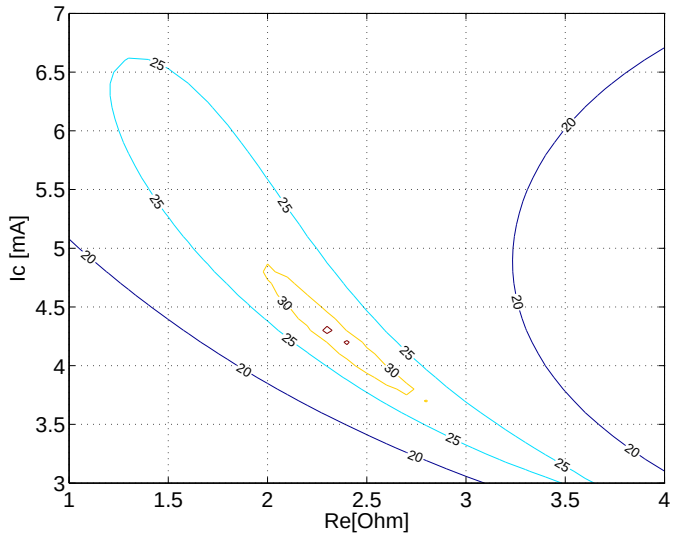


FIGURE 3.9: The OIP3 contours in dBm of the unit-cell CE amplifier using the Mextram model of a SiGe 0.5x20.7x2μm^2 HBT.

current/power levels, we scale up the circuit by placing a number m (which we will call scaling factor) of times the same circuit in parallel. In this way, the current flowing in each branch becomes m times larger while the impedance values reduces by the same amount, resulting in a constant voltage swing at each node. The power level (both DC and RF) becomes a factor m larger, or $10log(m)$ dB larger when expressed in dBm. We can see how the $OIP3$ changes using its definition 2.4 and identifying the quantities related to the scaled circuit with the subscript m. Since $P_{out,fund_m} = P_{out,fund}+10log(m)$ and $P_{out,IM3_m} = P_{out,IM3} + 10log(m)$, the output IP3 becomes

$$OIP3_m = P_{out,fund_m} + \left(\frac{P_{out,fund_m} - P_{out,IM3_m}}{2}\right) = OIP3 + 10log(m) \tag{3.11}$$

We can show this in simulation by scaling the emitter-tuned circuit described in the previous paragraph. Figure 3.10 shows the total output power, the transducer gain and the output IP3 as function of power available from the source:

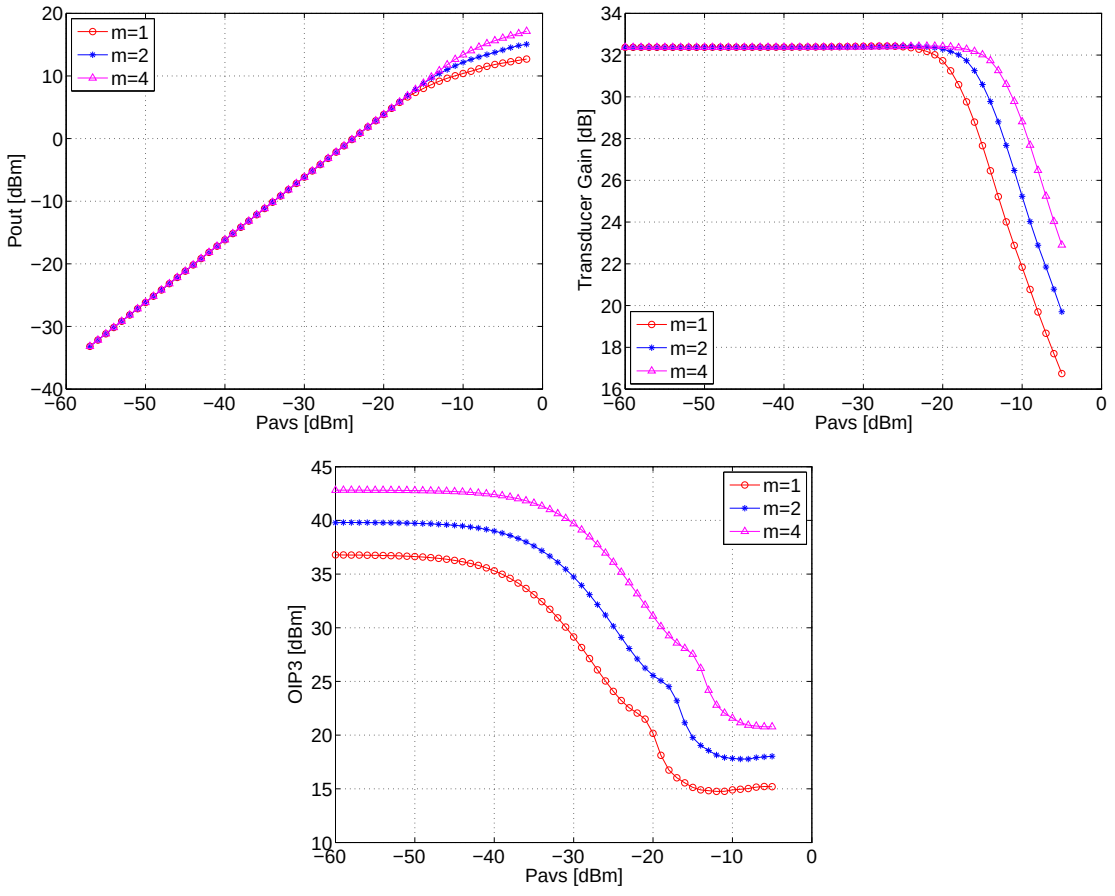


FIGURE 3.10: The output power, transducer gain and OIP3 figure of the emitter-compensated CE stage for several values of the scaling factor m.

The simulation results show indeed an increase of 3 dB in both P1dB and OIP3 each time the transistor size is doubled and its terminations are proportionally reduced. Proceeding

in this way, to achieve a P1dB of 27dBm (which corresponds to 0.5W), we need to set a scaling factor m=190. For this value of the scaling factor, the achieved OIP3 is about 60 dBm. This method can be exploited to achieve very high levels of output $P1dB$ and $IP3$; however, in practical circuits applications, it is limited to a maximum scaling factor m_{max}. This is because of the following reasons: the degeneration resistance R_e is, to satisfy the condition of emitter compensation, inversely proportional to the collector current $I_{c,q}$. This, when scaling is applied, leads to impractically small values of the R_e, which is in actual implementations limited to the internal resistance of the device and by the emitter ground inductance. In this example, a value of m=190 would result in a value of $R_e = 12m\Omega$, which is already smaller than typical values of the intrinsic resistance. At the same time, the source and load impedance also reduce by a factor m, yielding very high impedance transformation ratios to satisfy the general requirement of 50 Ohm input and output impedance in RF circuits. Matching networks that can provide high transformation ratios are limited in their frequency range, affecting the overall bandwidth of the amplifier. For this reasons, this straightforward power scaling method is not applied in the following chapters as presented in this paragraph, but it will be used with the proper adjustments to overcome the mentioned limitations.

3.3 Conclusions

From the studies carried out in this chapter, we can draw some useful conclusions: the emitter compensation is a more robust linearization solution than the base compensation since its conditions can be achieved by means of a 2nd harmonic short at the base terminal which precisely define the impedance presented at the input of the device. Moreover, its implementation is independent from the design of an input matching network. We saw that the effect of a linear C_{bc} is to feedback part of the output current, whose IM2 frequency components generate indirect mixing and therefore IM3 distortion. This distortion mechanism is though suppressed by the out-of-band short connected to the base node. Instead a non-linear C_{bc}, representing the modulation of the base charge by the voltage and current swings in the base-collector junction, introduces distortion which becomes dominant when the load impedance is close to the optimum value for maximum P1dB. The power scaling of the circuit is a simple and effective solution to increase the IP3 level. However, it is limited by the minimum values of impedances that can be reliably implemented for the input and output transformation ratios and, most of all, by the emitter parasitic series resistance of the device itself. In addition, because of the nature of the cancellation method, the Out-of-Band technique is very sensitive on variations of the PVT parameters. In the next chapters we will investigate linearization techniques that can overcome these problems.

Chapter 4

Out-of-Band Injection Compensation

As we have seen in Chapter 3, the Out-of-Band linearization technique suffers from a high sensitivity on various effects. For example, an offset in the quiescent current or a parasitic element in the emitter lead would cause the cancellation to be less effective, and consequently a significant decrease in the IP3 levels. Here we aim to develop a technique that can compensate for variations in the optimum operating point for linearity, when this has been shifted by one or more of these unwanted effects. The approach that is investigated uses the active injection of signals at the IM2 frequencies in the amplifier. These signals are adjusted to compensate the deviation and restore the optimum operating point for linearity in the amplifier. To show these principles, we structure the chapter as follows: first, the condition on fundamental and IM2 base-emitter voltages that satisfy the Out-of-Band cancellation point will be derived. Next the signal injection compensation technique is introduced and two possible alternatives are given: baseband injection, when the signal is injected in the amplifier at the baseband frequency; and the 2^{nd}-harmonic injection, when instead the signal is injected at the 2^{nd} harmonic frequency. Examples of circuits using the IM2 injection technique will be presented, together with the results of their simulations. Eventually several conclusions are drawn upon this approach, and suggestions for possible future work are given.

4.1 Base-Emitter Voltage Conditions

Let us consider again the small-signal model of an emitter-compensated CE stage, as depicted in figure 4.1. From equation 3.1 we can conclude that, when the K_{ig_m} factors of the Taylor expansion are fixed, the resulting overall IM3 current is only a function of

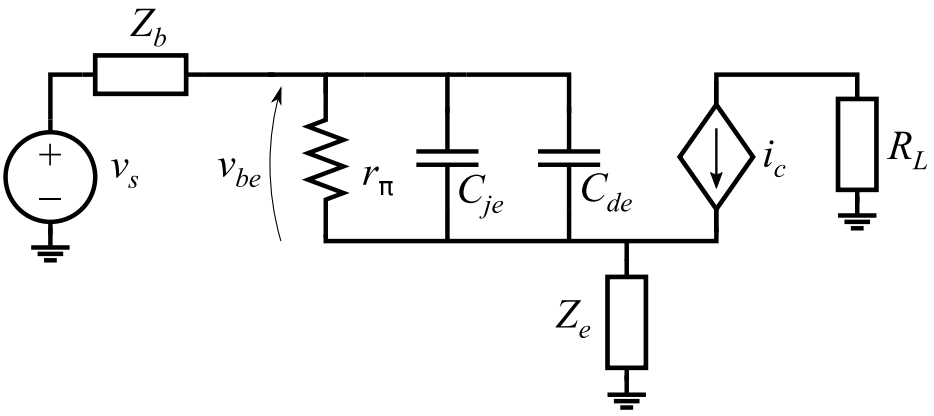


FIGURE 4.1: The small-signal model of an emitter-compensated CE stage.

the base-emitter voltages at baseband, fundamental and 2nd-harmonic frequencies. In this perspective, we can think about the out-of-band impedances as one way to achieve those voltages by means of terminating the internally generated non-linear currents. The idea behind this linearization approach is that, regardless the way these base-emitter voltages are generated, the direct and secondary mixing should cancel out each other when a condition on the phase and magnitude of those voltages is satisfied. To find this condition, assuming a narrowband input signal made of two tones at the frequencies s_1 and s_2, we start from the equation of the 3rd order non-linear collector current [8]:

$$\begin{aligned} &i_{c,NL3} = \\ &K_{3gm} v_{be}(s_{1,2}) v_{be}(s_{1,2}) v_{be}(-s_{2,1}) + \\ &+ \frac{2}{3} K_{2gm} \left[2 v_{be}(s_{1,2} - s_{2,1}) v_{be}(s_{1,2}) + v_{be}(2s_{1,2}) v_{be}(-s_{2,1}) \right] = 0 \end{aligned} \tag{4.1}$$

With the notation $s_{i,j}$ we want to indicate that the equation holds when all the i pedices are considered, or when all the j pedices are considered. To simplify the calculation, we make the following assumptions[1]:

$$\phi\{v_{be}(s_{1,2})\} = -\phi\{v_{be}(-s_{1,2})\} \tag{4.2}$$

$$v_{be}(\pm s_1) = v_{be}(\pm s_2) \tag{4.3}$$

$$\phi\left\{v_{be}(s_{1,2} - s_{2,1})\right\} \simeq \phi\left\{v_s(s_{1,2})\right\} + 180^\circ \tag{4.4}$$

Here, $v_s(s)$ is the voltage source at the general frequency s. If we normalize all the phases to the phase of the voltage source, then $\phi\left\{v_s(s_{1,2})\right\} = 0$ and assumption 4.4 becomes: $\phi\left\{v_{be}(s_{1,2} - s_{2,1})\right\} \simeq 180^\circ$. This last conditions comes from the assumption that the phase of the baseband term $v_{be}(s_{1,2} - s_{2,1})$ is only determined by the phases of the fundamental terms $v_{be}(s_{1,2})$, which are involved in the mixing. This is true if

[1] The validity of these assumption limits the application of the found equations to narrowband systems

we consider the frequency spacing between s_1 and s_2 to be narrow, such that $s_1 \approx s_2$. After some manipulation, which is reported in appendix A, we can rewrite the condition of equation 4.1 in terms of the magnitude and phase of the in-band and out-of-band base-emitter voltages as:

$$\frac{|v_{be_{f0}}|^2}{|v_{be_{BB}}| + |v_{be_{2F}}|} = 4V_T \tag{4.5}$$

$$2\phi_{f0} - \phi_{2F} = 180^\circ \tag{4.6}$$

where for ease of notation we introduced $v_{be_{f0}} = v_{be}(s_{1,2})$, $v_{be_{BB}} = v_{be}(s_{1,2} - s_{2,1})$ and $v_{be_{2F}} = v_{be}(2s_{1,2})$. Moreover $\phi_{f0} = \phi\{v_{be}(s_{1,2})\}$ and $\phi_{2F} = \phi\{v_{be}(2s_{1,2})\}$. We will refer to equations 4.5 and 4.6 as "*magnitude condition*" and "*phase condition*" respectively. For convenience, we define here the quantities V_{OoB} and ϕ_{OoB} as:

$$\begin{aligned} V_{OoB} &= \frac{|v_{be_{f0}}|^2}{|v_{be_{BB}}| + |v_{be_{2F}}|} \qquad [\text{V}] \\ \phi_{OoB} &= 2\phi_{f0} - \phi_{2F} \qquad [\text{degrees}] \end{aligned} \tag{4.7}$$

The derived results were tested in a circuit simulator, using a Gummel-Poon model of a NPN BJT.

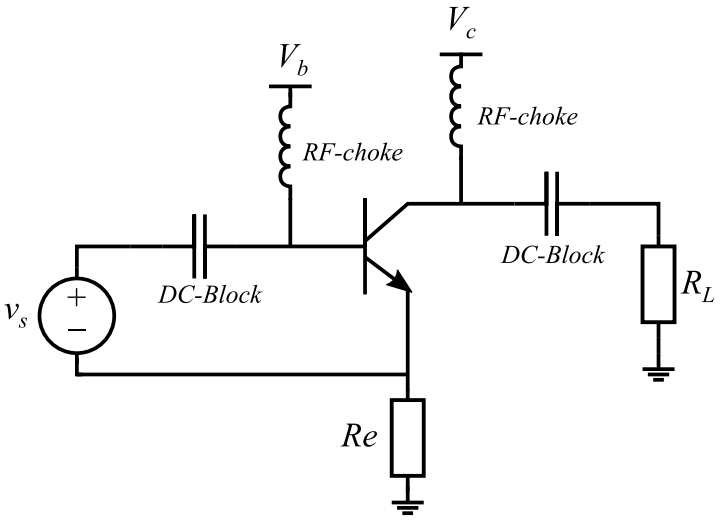


FIGURE 4.2: The schematic used for testing the derived condition.

The circuit schematic topology is depicted in figure 4.2. It consists of a simple degenerated CE stage: the base and the collector are biased through an RF choke, large capacitors are used at the input and output for RF coupling. The amplifier is excited by an ideal voltage source ($R_S = 0$) which is directly connected to the base-emitter nodes and generates 5 tones at the frequencies:

- f_{01} (first fundamental tone);
- f_{02} (second fundamental tone);
- $2f_{01}$ (second harmonic of the first fundamental tone);
- $2f_{02}$ (second harmonic of the second fundamental tone);
- f_{BB} (baseband tone).

By adding to the fundamental signals the tones at the frequencies $2f_{01}, 2f_{02}$ and f_{BB}, we are able to manipulate the mixing mechanisms which generate the $IM3$ low & high components. No component at the sum frequency $f_{01} + f_{02}$ is used for the excitation, as this is not involved in the indirect mixing generation of IM3 frequency components. The load impedance is set to 50Ω. The transistor parameters are listed in table 4.1. To show

Parameter	**Value**	**Dimension**
Area	2	mult
I_s	$1.2 \cdot 10^{-15}$	A
β_f	2000	-
C_{je}	0.3	pF/mult
V_{je}	0.7	V
m_{je}	1/3	-
C_{jc}	0	pF/mult
Vjc	0.7	V
m_{jc}	1/3	-
τ_f	2	ps

TABLE 4.1: Gummel-Poon device model parameters for the simulation.

the validity of the phase and magnitude equations, we perform a two-tone simulation and sweep simultaneously the phase ϕ_{2F} of the 2^{nd}-harmonic components f_{01}, f_{02}, and their magnitude $|v_{be_{2F}}|$. The Baseband component magnitude is $|v_{be_{BB}}| = |v_{be_{2F}}|$ and its phase $\phi\{v_{be_{BB}}\} = 180°$. The fundamental voltage is constant and equal to: $|v_{be_{f_{01}}}| = |V_{be_{f_{02}}}| = 10\ mV$, while its phase is 0°. The simulations parameters are shown in table

I_{cq}	15	mA
V_c	3	V
f_0	2	GHz
Δ_f	10	MHz
Z_L	50	Ω

TABLE 4.2: Simulation parameters for the test of the base-emitter voltage conditions.

4.2. Figure 4.3 plots the contours of the output IP3 figure over the phase and magnitude conditions defined in 4.7. The contour plot shows that an optimum in the OIP3 exists when $\phi_{OoB} = 180°$ and $V_{OoB} = 103.2\ mV = 4V_{T,@300K}$. In the next section we describe

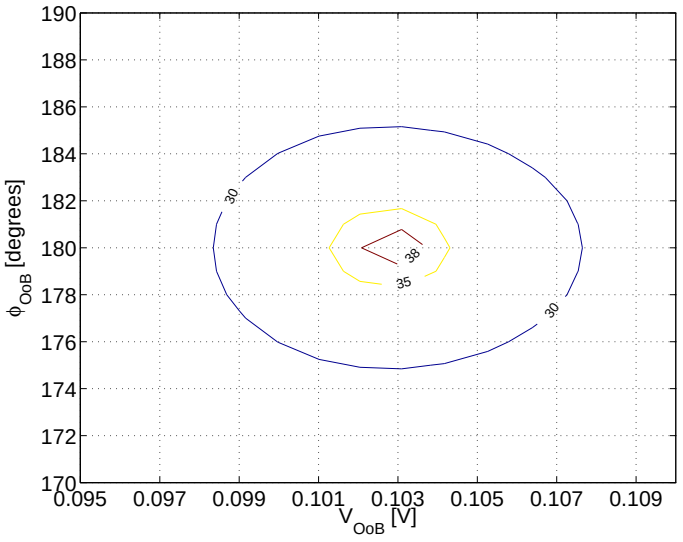


FIGURE 4.3: OIP3 contours in dBm versus the value of the magnitude and phase conditions for a CE stage with GP model.

the IM2 injection compensation method. The derived condition for the magnitude and phase equation represents the base of the concept behind this linearization technique. Its role will be described using several circuit examples.

4.2 IM2 Injection Compensation

When the described optimum conditions on the magnitude and phase relation of the base-emitter voltages are satisfied, the direct mixing contribution to the IM3 collector current is equal in magnitude and opposite in phase to the indirect mixing contribution, providing the wanted cancellation. Nevertheless, we know from the observations in Chapter 3 that the operation of the amplifier can easily shift from the optimum point due to various causes. We can show this graphically making use of the vector representation as in figure 4.4: the IM2 base-emitter voltages are the dashed vectors, while the fundamental is the solid one. These vectors need to have a certain relation to satisfy the IM3 cancellation condition: their reciprocal orientation and amplitude are determined by the phase and magnitude conditions respectively. When a variation modifies these relations, e.g. the presence of a parasitic reactive component modifies the 2^{nd} Harmonic voltage, the difference vector between the optimal and the actual IM2 voltage can be provided by an external signal injection, as depicted in 4.5.

If we inject a current signal at the IM2 frequencies, its contribution sums with the internal non-linear current to the overall IM2 voltage. The advantage is that its magnitude and phase can be freely adjusted according to what is needed for the compensation. We can write the IM2 voltage as a function of both the internal non-linear current and the

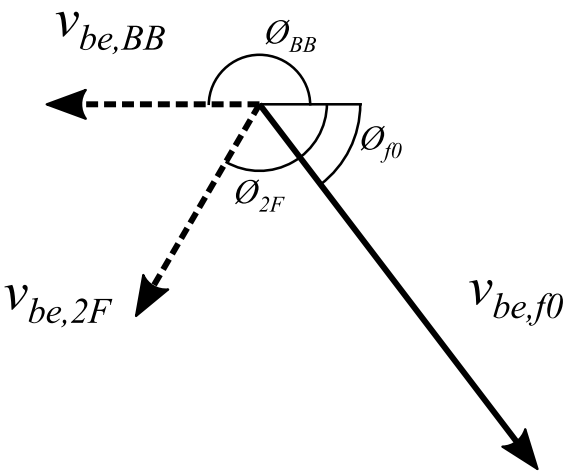


FIGURE 4.4: Phasor representation of the base-emitter voltages condition.

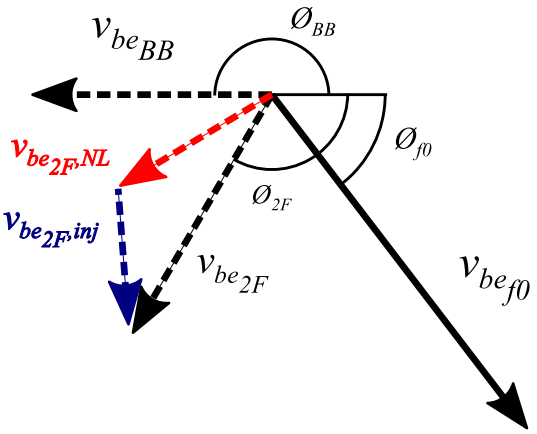


FIGURE 4.5: Phasor representation of the base-emitter voltages condition when injection is used.

injected current in this way:

$$v_{be}(s_a, s_b) = i_{NL2} \circ H_{NL2}(s_a + s_b) + i_{inj} \circ H_{inj}(s_a + s_b) \tag{4.8}$$

Here, H_{NL2} is the 2$^{\text{nd}}$ order transfer function from the nonlinear collector current to the base emitter voltage, and $H_{inj}(s)$ is the transfer function from the injected current to the base-emitter voltage. The second term represents therefore the contribution of the injected signal to the 2$^{\text{nd}}$ order base-emitter voltage. In general, there are many different possibilities to implement an IM2 signal injection. The choice in this experiment was to place a current signal source in parallel with the emitter degeneration, and as such inject it in the emitter node of the transistor. In this way, neglecting the intrinsic emitter resistance r_e and assuming a low load impedance R_L, we have that:

$$H_{inj}(s) = H_{NL2}(s) \tag{4.9}$$

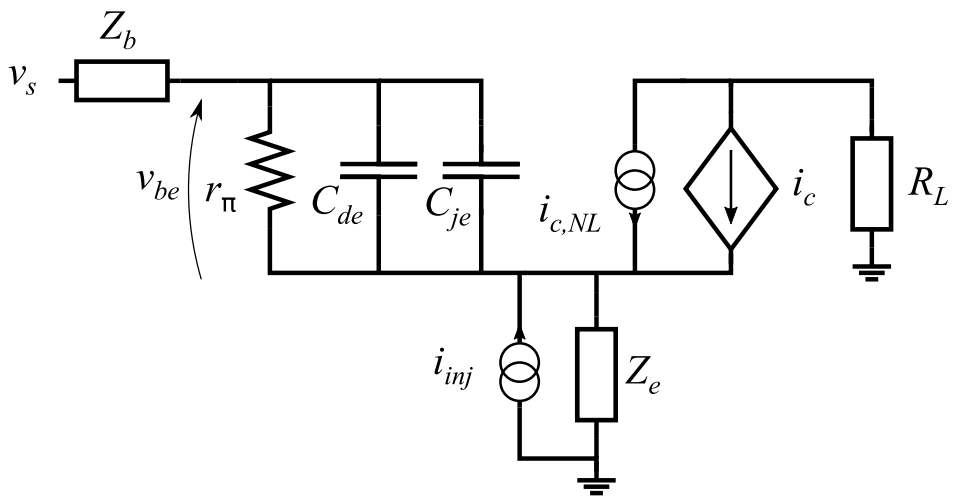


FIGURE 4.6: Small signal model of the CE stage representing the internally generated nonlinear collector current and the externally injected IM2 current.

Figure 4.6 shows in a schematic the meaning of equation 4.9. We can indeed observe that when the load impedance is $R_L \approx 0$, the two current sources are placed in parallel. Depending on the frequency of the injected current signal we distinguish between two alternatives, namely :*Baseband Injection*, when the current is injected at the BB frequency; *2nd Harmonic Injection*, when it is injected at 2nd harmonic frequency. In the following paragraphs these two techniques are described.

4.2.1 Baseband Injection

Here we discuss the injection of the signal at BB frequency. The advantage of the BB injection lies in the ease of phase and magnitude adjustment for the injected signal. Baseband circuitry can be accurately controlled to provide the wanted signal values. If the internally generated BB signal is influenced by an external source, we need to allow a general value for $\phi_{BB} \neq \pi$, which means that the assumption 4.4 is not satisfied, and a more general situation has to be studied. In doing this, we realize that since for the property of symmetry

$$\phi\{v_{be}(s_1 - s_2)\} = -\phi\{v_{be}(s_2 - s_1)\} \tag{4.10}$$

we have that $\phi\{v_{be}(s_1 - s_2)\} = \phi\{v_{be}(s_2 - s_1)\}$ only when they are both equal to 0 or π. From equation 4.8 and 4.9, assuming that for narrowband systems $H_{NL2}(s_1 - s_2) \approx H_{NL2}(s_2 - s_1) \approx H_{NL2}(0)$, we can state that the sign of the baseband voltage phase ϕ_{BB} entirely depends on the sign of the phase of the injected current $\phi\{i_{inj,BB}\}$. Therefore, the optimum phases of the injected current for the compensation of the IM3L and of

the IM3H, have opposite signs, in formula:

$$\phi\{i_{inj,BB}\} = \begin{cases} \phi_{opt}, & \text{for IM3L} \\ -\phi_{opt}, & \text{for IM3H} \end{cases} \tag{4.11}$$

This constraint makes the simultaneous compensation of both the high and low sideband IM3 components through Baseband injection not viable.

4.2.2 2nd Harmonic Injection

The current may also be injected in the 2nd harmonic band. The low and high IM3 components are independently related to the different 2nd harmonic signals: the IM3L is influenced by the component at the frequency $2s_1$, while the IM3H is influenced by the component at the frequency $2s_2$. Thanks to this separation, we can independently compensate the low and high IM3 distortion by injecting a current formed by the two 2nd harmonic frequency components $2f_{01}$ and $2f_{02}$. In this way a general value for ϕ_{BB} can be compensated by adjusting the phases of the injected currents.

4.2.3 Schematic Simulation

For the testing of the out-of-band injection technique, the schematic circuit of figure 4.7 has been built. It consists of a degenerated CE stage, using emitter-tuning to linearize

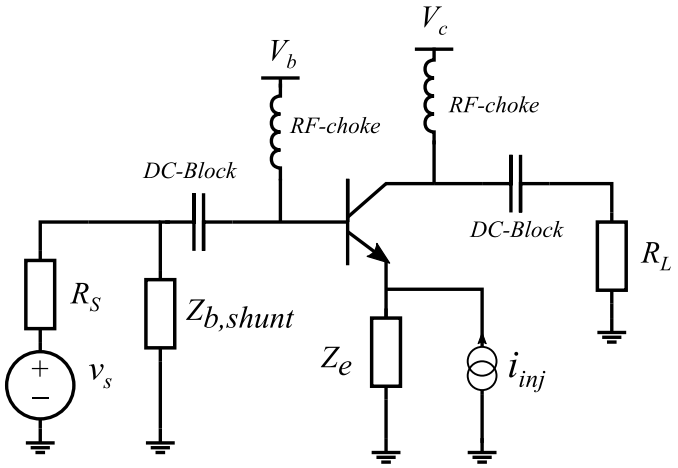


FIGURE 4.7: Schematic for testing the out-of-band injection linearization technique.

the IM3 generated by the exponential distortion. A GP model is used to characterize the bipolar device. Table 4.3 lists the parameters used for the model in this simulation, which are the same used in Chapter 3. The procedure we follow to show the effectiveness of the out-of-band injection technique is here explained: First the linearity performance

Parameter	Value	Dimension
Area	1	mult
I_s	$1.2 \cdot 10^{-15}$	A
β_f	2000	-
C_{je}	0.3	pF/mult
V_{je}	0.7	V
m_{je}	1/3	-
C_{jc}	0	pF/mult
Vjc	0.7	V
m_{jc}	1/3	-
τ_f	2	ps

TABLE 4.3: Gummel-Poon device model parameters for the simulation of the out-of-band injection linearization technique.

of the circuit operating in its optimal point for out-of-band cancellation is shown; then we introduce a deviation from the optimum point to resemble the action of un unwanted effect; eventually we show the effectiveness of the linearization technique by injecting the IM2 signal that can compensate for this deviation.

Ideal Circuit

To simulate the optimal operation of an emitter-tuned CE stage, we reuse the values used in paragraph 2.2.1 for the circuit in figure 4.7. These values are reported again in table 4.4 for completeness.

We perform a sweep of the biasing base voltage, and plot the results on figure 4.8 It is

Component	Frequency Band	Value
R_S	All	50 Ω
R_L	All	50 Ω
$Z_{b,shunt}$	BB	0 Ω
	fund	∞
	2^{nd}H	0 Ω
Z_e	BB	1.7 Ω
	fund	1.7 Ω
	2^{nd}H	1.7 Ω

TABLE 4.4: List of the values of the circuit components for each frequency band.

possible to observe the presence of a sharp optimum point for

$$I_c = V_T/2R_e \approx 7.6mA \tag{4.12}$$

This value of the quiescent current corresponds to the conditions described in Chapter 3 for out-of-band IM3 cancellation, for an emitter-tuned design: $g_m = 1/2R_e$ and $2g_m\tau_f = C_{je}$.

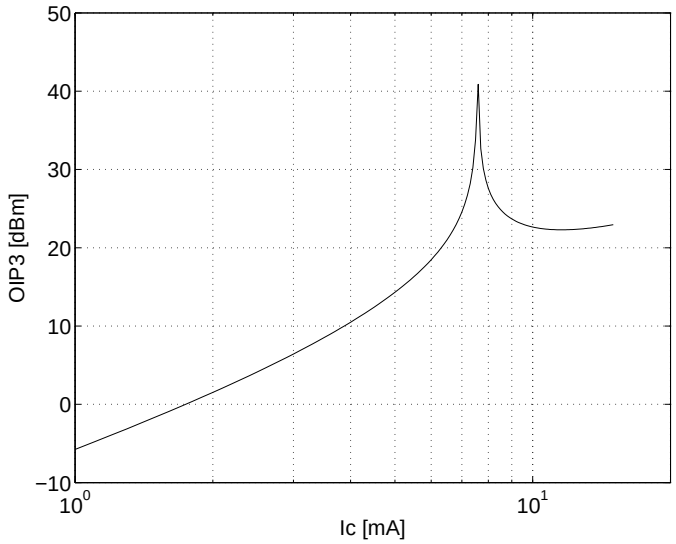


FIGURE 4.8: The OIP3 figure versus quiescent collector current obtained for the emitter-tuned CE stage.

Practical Circuit

Now we modify the circuit to emulate a practical situation. In this case, we add an inductive element $L_e = 10\ pH$ in series with the emitter degeneration, which is usually introduced as a parasitic in the layout; and leave the rest of the elements unaltered: Figure 4.9 compares the OIP3 figure versus collctor current for the ideal circuit and

Component	**Frequency Band**	**Value**
R_S	All	50 Ω
R_L	All	50 Ω
$Z_{b,shunt}$	BB	0 Ω
	fund	∞
	2^{nd}H	0 Ω
Z_e	BB	1.7 Ω
	fund	$1.7 + j0.125$ Ω
	2^{nd}H	$1.7 + j0.25$ Ω

the one affected by the parasitic inductance. When simulating this circuit, we note a degradation of 14 dB in the peak OIP3 point, due to the influence of the inductance in the emitter degeneration path.

Compensated Circuit

Now we inject the IM2 signal to compensate for the deviation introduced by the parasitic inductance. We first do it with a signal BB at the BB frequency, and then with a signal composed by the two 2^{nd} harmonic tones.

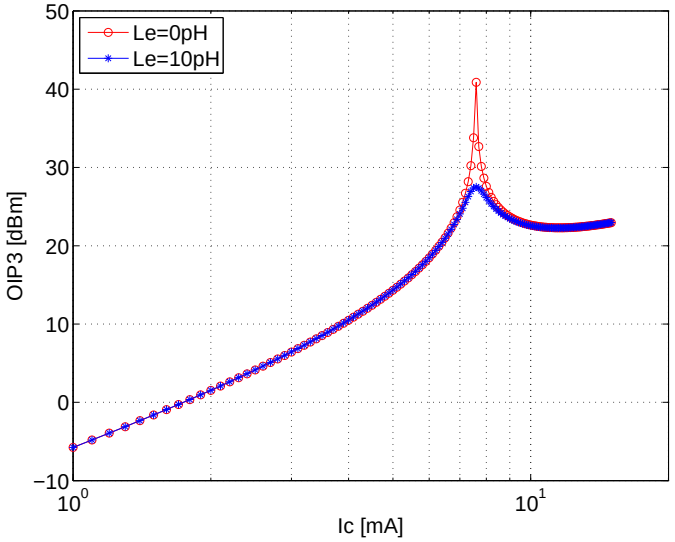


FIGURE 4.9: The OIP3 versus collector current for the ideal and the practical circuits.

- *BB Injection*

  When a sweep is done on the magnitude and phase of the injected BB current, we can see from figure 4.10 that 2 different optimum values exist: one for the compensation of the low IM3 and a different one for the compensation of the high IM3 component. In particular, the optimum amplitude of the injected Baseband

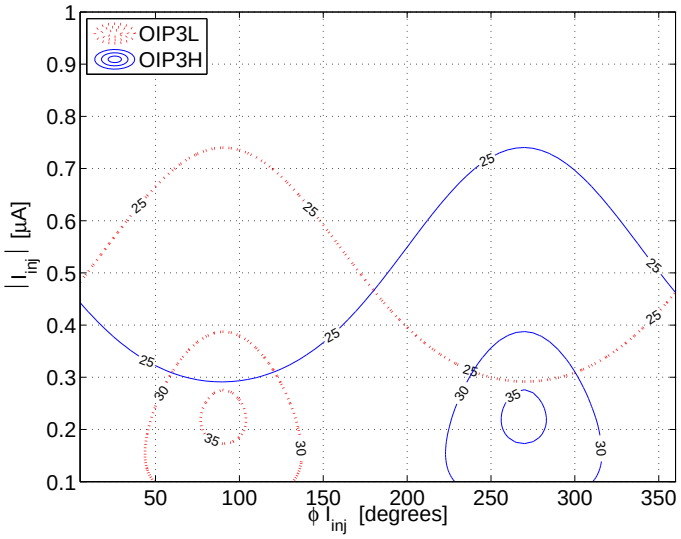


FIGURE 4.10: Low and high OIP3 contours in dBm plotted versus the phase and magnitude of the injected baseband current.

signal is the same, while for the phase it holds that:

$$\phi_{opt}\left\{i_{inj,BB}\right\} = \begin{cases} 90^\circ & \text{, for IP3L} \\ 270^\circ & \text{, for IP3H} \end{cases} \tag{4.13}$$

We can note that the IP3 behavior for the low and high sides are symmetric with respect to 180°. As mentioned earlier in this paragraph, this is due to the property 4.10. This means that, to ensure the symmetry of the IM3 components, the base-emitter baseband voltage phase must be $\phi_{BB} = \pi$.

- *2^{nd} Harmonic Injection*

  Now we make use of the 2nd harmonic injection for the compensation. In order to show that the injection of 2 tones at the frequencies $2f_{01}$ and $2f_{02}$ can be used to compensate for any value of the baseband base-emitter voltage phase ϕ_{BB}, we add a tone at the Baseband frequency to the excitation source, with a randomly chosen power and phase of $-100\ dBm$ and 200° respectively. We also set $Z_{b,shunt} = \infty$ for the baseband frequency range, to allow the transfer of the additional tone from the power source to the base-emitter voltage. Table 4.5 reports the components values used here: With this condition we simulate the effect of the injection to the

Component	**Frequency Band**	**Value**
R_S	All	50 Ω
R_L	All	50 Ω
$Z_{b,shunt}$	BB	∞
	fund	∞
	2nd H	0 Ω
Z_e	BB	1.7 Ω
	fund	$1.7 + j0.125$ Ω
	2nd H	$1.7 + j0.25$ Ω

TABLE 4.5: List of the components value used for the simulation of the circuit compensation by 2nd harmonic injection.

  IP3 figure. The results are plotted in figure 4.11. It can be observed that we can simultaneously achieve the optimum condition for the OIP3 low and high when:

$$|i_{inj,2f_{01}}| = 3.62\mu A \tag{4.14}$$

$$\phi\{i_{inj,2f_{01}}\} = 105° \tag{4.15}$$

$$|i_{inj,2f_{02}}| = 3.86\mu A \tag{4.16}$$

$$\phi\{i_{inj,2f_{02}}\} = 144° \tag{4.17}$$

  When we set these values for the current sources in the schematic, and make a sweep of the biasing current, the plot of figure 4.12 is achieved. We can see that the optimum point for both low and high OIP3 is restored at $I_{cq} \approx 7.6\ mA$

The compensation example given for the 2nd harmonic injected signal has been simulated for a level of power available form the source $P_{avs} = -50\ dBm$ per tone. We can see

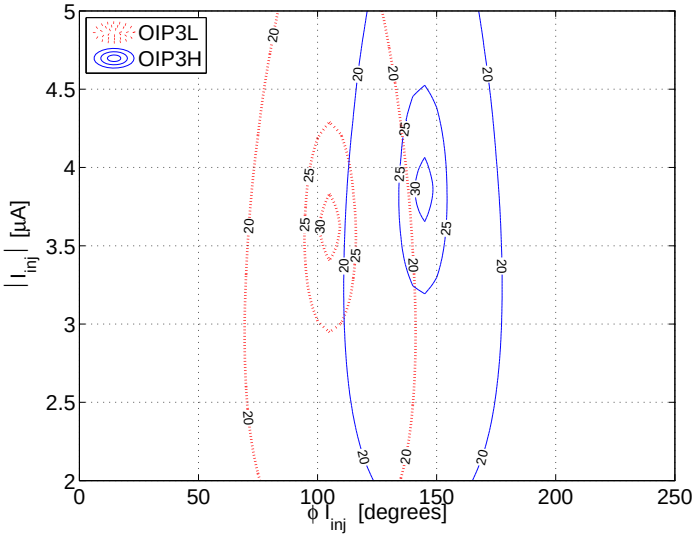


FIGURE 4.11: The OIP3 figure in dBm of the compensated circuit. The OIP3L is plotted versus phase and magnitude of the current injected at $2f_{01}$, while the OIP3H versus phase and magnitude of the current injected at $2f_{02}$.

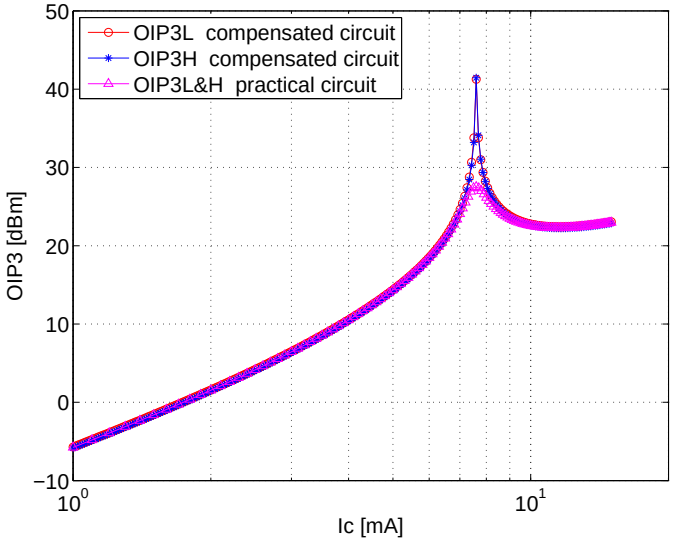


FIGURE 4.12: A comparison of the OIP3 low and high figures between the emitter-tuned circuit in practical conditions and the circuit after compensation is applied.

from figrue 4.13 that the compensation is only achieved for the simulated input power level. For the compensation to be effective over the whole input power range, the square of the magnitude of the injected signal should be proportional to the input power level. In formulas:

$$|i_{inj}|^2 \propto P_{in} \tag{4.18}$$

To ensure this condition, there are several possible alternatives. One of them is the re-utilization of the output current 2$^{\text{nd}}$ harmonic content. The next paragraph is dedicated to describe this method.

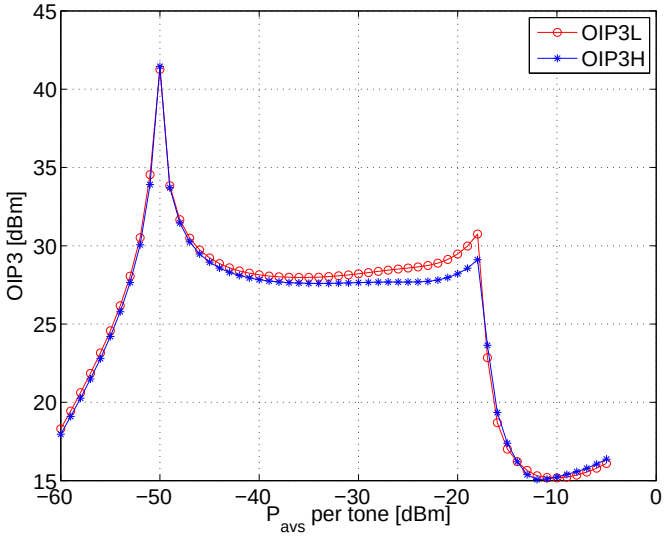


FIGURE 4.13: The OIP3 figure plotted versus input power for a fixed value of the injected compensation current.

4.2.4 2nd Harmonic Signal Feedback

One possible way to achieve the proportionality stated in equation 4.18 is to use the output power content in the 2nd harmonic band and feed it back to the input after the proper adjustment. This technique was investigated by creating a schematic which implements the out-of-band signal feedback using ideal controlled sources and impedance blocks. This is shown in figure 4.14. To create a feedback path for the 2nd harmonic

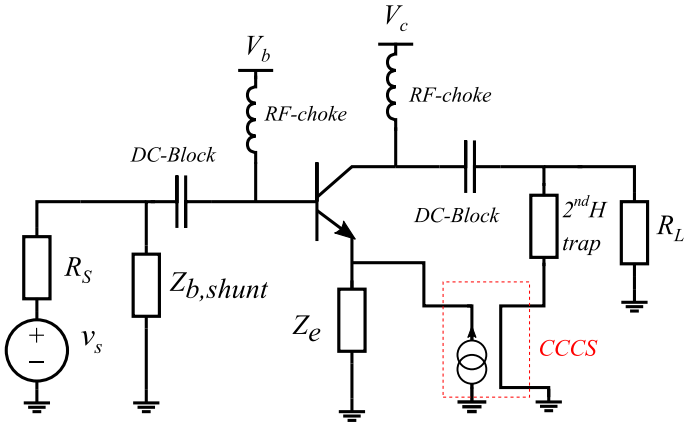


FIGURE 4.14: The test bench used for the simulation of the 2nd harmonic feedback injection.

output current content, a current-controlled current source (CCCS) is used in combination with an equation-defined impedance, which is used to implement a 2nd harmonic trap. To adjust the injected signal, we make use of the gain G and delay T introduced by the CCCS to the IM2 output current. An optimum value was found for $G = 0.16$ and $T = 0.305$ ns. When this values are used in the characterization of the CCCS block,

we obtain the OIP3 vs power behavior represented in figure 4.15. It can be observed

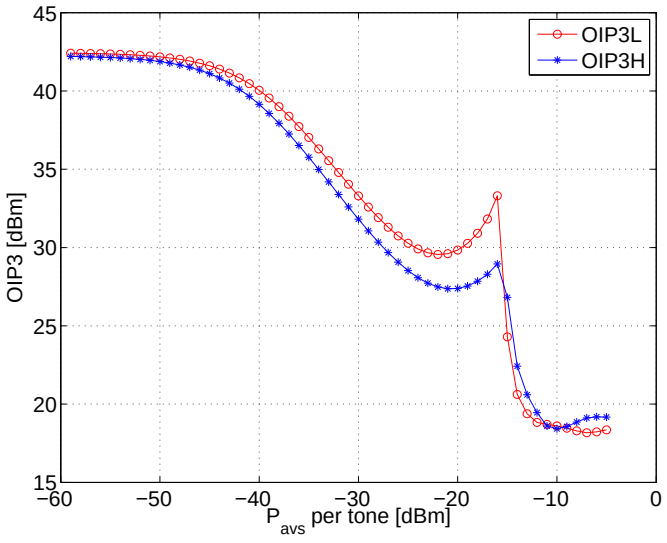


FIGURE 4.15: The OIP3 low and high plot versus power available from the source for the circuit using 2nd harmonic feedback compensation.

that the OIP3 level is flat for low power and it starts to roll off above $P_{avs} \approx -40$ dBm, as fifth order mixing becomes the dominant mechanism in the generation of IM3 components.

4.3 Conclusions

In this section the described techniques are summarised, highlighting their advantages and drawbacks:

BaseBand Injection

We mentioned that a Baseband signal can be more accurately controlled in terms of the exact magnitude and phase of the signal to be injected. However, since the Baseband base-emitter voltage influences the low and high IM3 components of the collector current in an opposite way, its phase cannot be freely chosen but it needs to be 180° shifted from the voltage source phase.

2nd Harmonic Injection

When the compensation signal is injected at the 2nd harmonic band, we can make use of the separate influence that the components at $2f_{01}$ and $2f_{02}$ have on the IM3 low and high components respectively. In this way, any deviation from the optimum operating point of the Out-of-band cancellation can be compensated. In the example it has been shown that also when $\phi_{BB} \neq \pi$, the IP3 can be restored to its peak value.

2nd Harmonic Signal Feedback

Finally an example has been described in which the signal injection is achieved by means of feedback of the output IM2 content. This method provides an IM2 signal which is proportional to the input power level, as it is generated by the mixing of the input signals.

4.4 Future Work

In general, the main limitation of this approach consists of the need to know *a priori* the magnitude and phase of the signal to be injected, according to the deviation of the circuit operation from the optimum value. An approach to overcome this problem is to use a feedback mechanism that adjusts magnitude and phase of the injected signal until it gives the optimal voltage conditions for cancellation. An example of the signal to be fed back is the 3rd Harmonic (HD3) output signal. Since they are generated in the same way, HD3 and IM3 components are somehow proportional. Given this, the power of the 3rd Harmonic signal can be used as a measure of the amount of IM3 distortion and fed back to suppress IM3 distortion. In particular, it can be used to adjust the IM2 signal to be injected. During this project, this solution was not developed into an actual implementation because of lack of time.

Chapter 5

Bipolar Derivative Superposition

In this chapter, the Derivative Superposition (DS) linearization method applied to Bipolar amplifiers is described. A CE stage circuit topology implementing the developed technique is proposed and studied through a simplified Volterra Series analysis. The low power optimum operating point for linearity is derived for the proposed circuit, first when only the ohmic part in considered and secondly when memory effects are included in the circuit model. The developed CE stage amplifier is then simulated and its linearity is compared to a conventional out-of-band matched design example, which makes use of the same DC current budget. Some considerations upon the high power operation of the proposed amplifier are reported. Finally several conclusions are given on the linearization technique, and the directions to take in future investigations are suggested.

5.1 Approximation of a Quadratic Characteristic

Let us consider a general nonlinear system. If we assume it to be only weakly nonlinear, we can fairly approximate its transfer function by truncating its polynomial expansion at the third power of the input signal. Let us also assume that the system is unilateral, i.e. no external feedback contributes to the overall output value. Given these constraints, the IM3 output components can be nullified by setting the system's third order Taylor coefficient $K_3 = 0$. When the system in consideration is a transconductance, we can express the output using the power series representation as:

$$I_{out} = K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 \tag{5.1}$$

where K_i are the system's Taylor coefficients. To set $K_3 = 0$ means to transform the $I_{out}(V_{in})$ transfer function into a quadratic one. The Derivative Superposition (DS)

technique functionality can be used to perform this transformation in RF amplifiers for a certain interval of the input signal domain ΔV_{in}. In fact we will see later that, when applied to a device characterized by an exponential transconductance, the exact condition $K_3 = 0$ can only be achieved for one particular value V_{in0} (and thus only for the correspondent value of biasing current I_{out0}). However the main advantage of the DS method is that it can result in $K_{3TOT} \approx 0$ for a large interval ΔV_{in} (and therefore ΔI_{out}). The technique of shaping the transfer function to improve the linearity has already been used and reported: in works [8] and [18] multiple FET devices are used to accomplish the desired linearization. Practical FET devices naturally show a region of biasing slightly above the pinch-off voltage where the K_{3g_m} coefficient of the transconductance function becomes negative. If we then place in parallel several transistors in a common source (CS) configuration, namely M_1, M_2, ..., M_N, we can bias and scale them in such a way that the overall third order Taylor coefficient $K_{3g_m,TOT} = \sum K_{3g_m,1,2,...,N}$ is nullified. Note that, in order to achieve this condition, at least one of the $K_{3g_m,i}$ coefficients must be negative. A schematic diagram of the above technique is depicted in figure 5.1, which was taken from [19]. Another work that is strictly related to this concept is the Multi-tanh principle from B. Gilbert [7]. This technique makes use of several bipolar differential pairs connected in parallel, which are biased at different points. These biasing offset are chosen to transform the overall transfer function into a more linear one by the summation of each single transfer function. In this way, an approximately quadratic $i(v)$

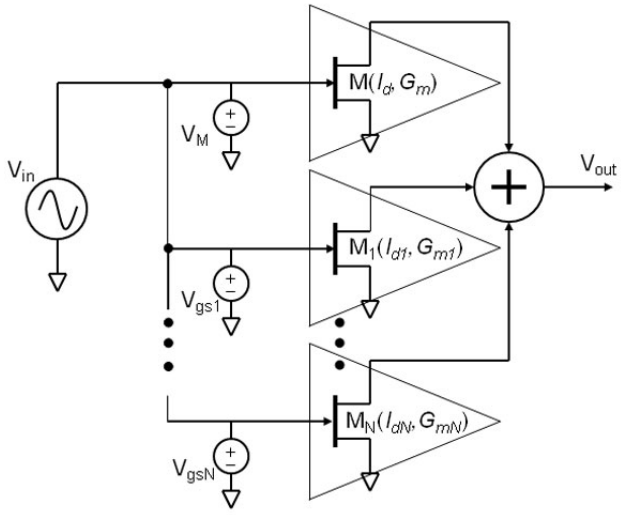


FIGURE 5.1: A block diagram representation of the Derivative Superposition method.

curve can be achieved, and no IM3 components are generated through direct mixing. However, for this technique to be effective, it is very important that the transfer function is unilateral, which means that no feedback paths for signals can cause indirect mixing by feeding IM2 products back to the input. If this were the case, secondary mixing would

take place between these feedback components and the fundamental ones through the 2nd order coefficient K_{2g_m}, yielding undesired IM3 distortion. To avoid this, the input voltage of the amplifier has to be shorted in the frequency bands that are responsible for indirect (secondary) mixing, which are the Baseband and 2nd-harmonic band.

5.2 Bipolar Derivative Superposition

The DS concept can also be applied to bipolar amplifiers. The ideal $I_c(V_{be})$ transconductance function of bipolar devices is exponential, and so are all the n$^{\text{th}}$ order derivatives, which could lead to the conclusion that DS is not applicable to bipolar transistors. However, if we analyse the transfer function of a degenerated CE configuration we will notice that the effect of the local feedback introduced by a degeneration resistance is to "shape" the $I_c(V_{be})$ curve, and thus all of its n$^{\text{th}}$ order derivatives. We can see this analytically by considering the degenerated CE stage as feedback system, as represented in figure 5.2. In this case $V_b(t) = x(t)$, $I_c(t) = y(t)$, $V_{be}(t) = e(t)$, $B = R_e$ and the Taylor

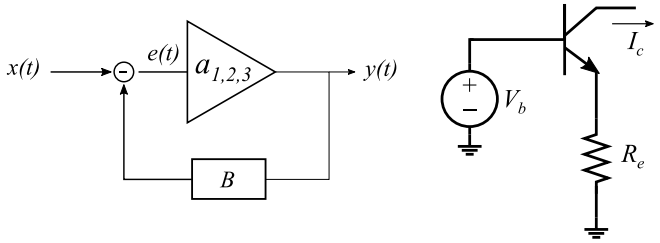


FIGURE 5.2: A block diagram representation of a feedback system and the equivalent schematic representation of a degenerated CE stage.

coefficients a_i are equivalent to the K_{ig_m}. Knowing that:

$$I_c(t) = g_m V_{be}(t) + K_{2g_m} V_{be}^2(t) + K_{3g_m} V_{be}^3(t) \tag{5.2}$$

and that, assuming $I_e \approx I_c$, we can write $V_{be}(t) \approx V_b(t) - R_e I_c(t)$; we can rewrite the output current as only a function of the input base voltage as:

$$I_c(t) = K_{1deg} V_b(t) + K_{2deg} V_b^2(t) + K_{3deg} V_b^3(t) \tag{5.3}$$

Here the terms K_{ideg} are the Taylor coefficients of the transconductance function of the degenerated CE stage block, and have the following expressions :

$$K_{1deg} = \frac{g_m}{1 + g_m R_e}; \tag{5.4}$$

$$K_{2deg} = \frac{K_{2g_m}}{(1 + g_m R_e)^3}; \tag{5.5}$$

$$K_{3deg} = \frac{K_{3g_m}(1 + g_m R_e) - 2K_{2g_m}^2 R_e}{(1 + g_m R_e)^5} \tag{5.6}$$

We can see that the presence of an $R_e \neq 0$ modifies the expression of the first as well as all the higher order coefficients. Since $K_{2g_m} = \frac{g_m}{2V_T}$ and $K_{3g_m} = \frac{g_m}{6V_T^2}$; equation 5.6 becomes:

$$K_{3deg} = \frac{g_m}{6V_T^2} \frac{(1 - 2g_m R_e)}{(1 + g_m R_e)^5} \tag{5.7}$$

This equation results in the well known low frequency condition for out-of-band emitter-tuning cancellation introduced in Chapter 3: $g_m = \frac{1}{2R_e}$, derived here in the time domain. In the frequency domain, we may think of this condition as the value of the product $g_m R_e$ at which the out-of-band 2$^{\text{nd}}$ order contribution equalizes and therefore cancels out the 3$^{\text{rd}}$ order contribution. For ease of notation, we introduce here a new quantity called *Feedback factor*, defined as:

$$F = g_m R_e \tag{5.8}$$

This quantity also gives a measure of the series feedback loop gain of the degenerated CE stage. In order to apply the DS technique, we are looking for a region where K_{3deg} is negative. Plotting equation 5.7 as a function of g_m in figure 5.3 we can see that this

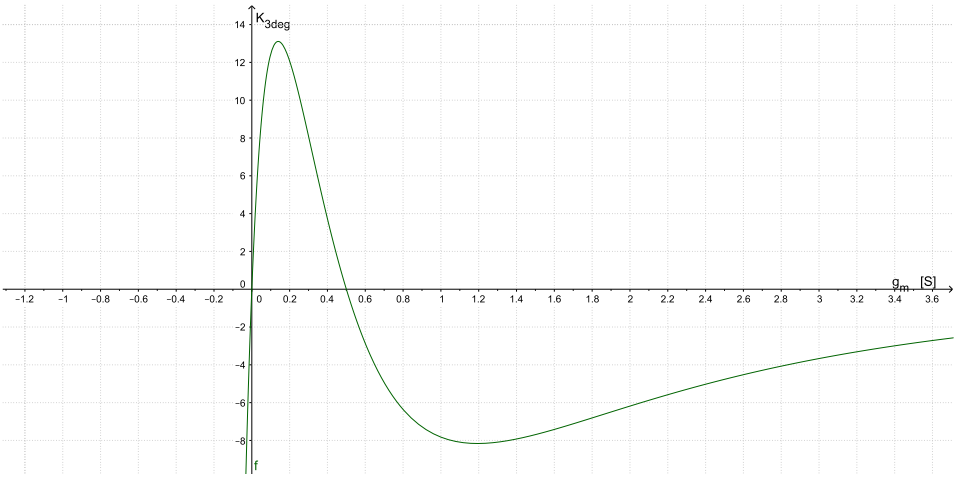


FIGURE 5.3: The third order Taylor coefficient K_{3deg} of the transconductance of a degenerated CE stage as a function of g_m.

occurs for values of $F > 0.5$. We can use therefore one device biased in this region, in combination with a second device biased in the positive K_{3deg} region to exploit the

aforementioned DS linearisation method. This technique is used in works such as [18]. In particular, we want that the K_{3deg} coefficients of the two devices have the same amplitude, such that $K_{3deg,TOT} = K_{3deg,1} + K_{3deg,2} = 0$. To make the cancellation robust over variations of the biasing current, we look for the points where the variation of K_{3deg} with the biasing current is minimised, which correspond to the maximum and the minimum of the curve in figure 5.3. In formulas we can write that we are looking for the values of g_m where $\frac{\partial K_{3deg}}{\partial g_m} = 0$. To implement this technique using bipolar transistors,

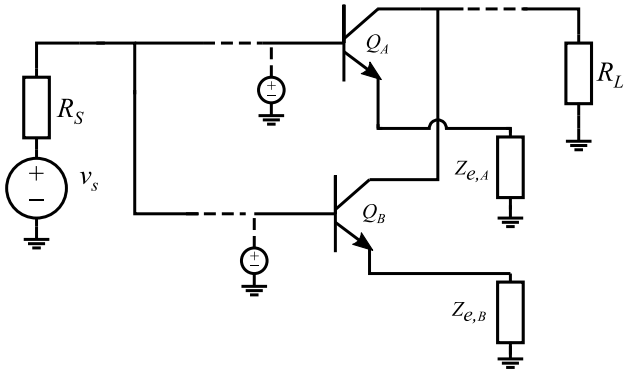


FIGURE 5.4: CE topology used to implement the DS technique.

the topology shown in figure 5.4 is proposed. It consists of two CE branches, namely A and B, placed in parallel to sum their output currents. In the coming analysis, we aim to find the cancellation points through a Volterra Series analysis on the chosen circuit topology, using the nonlinear current sources method. The final cancellation condition that we want to achieve can be written in the form:

$$i_{cIM3L,A} = -i_{cIM3L,B} \tag{5.9}$$

$$i_{cIM3H,A} = -i_{cIM3H,B} \tag{5.10}$$

In general, these are complex equations, which results in two equations for the real part and two for the imaginary part (or two for magnitude and two for the phase). The approach adopted to derive the solution of these equations will follow three basic steps in this order:

1. Volterra Series analysis of a single transistor CE stage using the non-linear current sources method.
2. Derivation of maximum and minimum of the 3$^{\text{rd}}$ order Taylor coefficient of the degenerated CE stage as a function of g_m, that is to solve the equation $\frac{\partial K_{3deg}}{\partial g_m} = 0$.
3. Set the magnitude and the phase of the IM3 currents in these two biasing points equal to each other and solve for g_m and R_e.

For the analysis of the single transistor CE stage, we will consider the following simplified large signal model of figure 5.5, which represents the model of only one CE branch. The

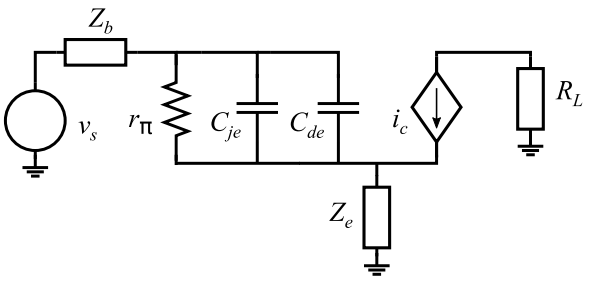


FIGURE 5.5: Small signal model of the used CE stage

separation of the branches in the analysis can be done if we consider the common base node to be shorted at BB and 2$^{\text{nd}}$-Harmonic, and the load R_L to be low enough, such that the collector voltage swing is low and no feedback occurs through the base-collector capacitance of the two devices.

5.2.1 Ohmic Solution

For simplicity, we will start considering the circuit to have no memory effects. For an intrinsic bipolar transistor, this assumption translates into the following simplifications:

- the base transit time τ_f is negligibly small, and thus also the base-emitter diffusion capacitance $C_{de} = g_m \tau_f \approx 0$;
- the base-emitter and base-collector depletion capacitances are disregarded too: $C_{je} \approx 0, C_{jc} \approx 0$.

Without losing generality, we will also assume that the two transistors are driven with the same RF voltage at the (external) base node, that is the two DC blocking caps at the input of the circuit in figure 5.4 are large enough to be considered as a short circuit for any $\omega > 0$. The actual situation can be easily accounted for by including in the calculation the voltage division that these RF-coupling capacitors introduce. Having eliminated all the memory effects in the circuit, equations 5.9 and 5.10 only have real values, and their solutions coincide. We start therefore from the general expression of the IM3L collector current for a CE stage, knowing that the final solution also applies for the cancellation of the IM3H current. This can be written as:

$$i_{cIM3L} = K_{3g_m} v_{be}(s_1) v_{be}(s_1) v_{be}(-s_2) + 2K_{2g_m} \overline{v_{be} v_{be_2}} + g_m v_{be_3}(s_1 + s_1 - s_2) \tag{5.11}$$

where

$$\overline{v_{be} v_{be_2}} = 2v_{be_2}(s_1, -s_2) v_{be}(s_1) + v_{be_2}(s_1, s_1) v_{be}(-s_2) \tag{5.12}$$

If we group the first two terms of the right-hand part of equation 5.11 as done in Chapter 3, we obtain:

$$i_{cIM3L} = \epsilon(s_1, s_1, -s_2)v_{be}(s_1)v_{be}(s_1)v_{be}(-s_2) + g_m v_{be_3}(s_1 + s_1 - s_2) \tag{5.13}$$

where :

$$\epsilon(s_a, s_b, s_c) = K_{3g_m} - \frac{2}{3}K_{2g_m}^2 \left[B(s_a, s_b) + B(s_a, s_c) + B(s_b, s_c)\right] \tag{5.14}$$

Note that this time, contrary to what was done in the Out-of-band analysis of Chapter 3, we do not disregard the term $g_m v_{be_3}(s_1 + s_1 - s_2)$. This is because now we are not looking for the point where $i_{cIM3L} = 0$, but we are searching for its maxima and minima as a function of g_m. Therefore this term becomes important as the 3$^{\text{rd}}$ order voltage v_{be_3} is not zero. The two functions which relate the source voltage to the output IM3 current are:

- the feedback impedance function $B(s) = v_{be}/i_c$, that is present in the equation both at baseband and 2$^{\text{nd}}$-harmonic band.
- the linear transfer function $H_{be}(s) = v_{be}/v_s$ from the source to the base-emitter voltage, present in the equation at the fundamental band.

When the device parameters that introduce memory effects are neglected, the expressions of $B(s)$ and $H_{be}(s)$ become

$$B(s) = \frac{\frac{R_b}{\beta_f} + R_e}{1 + g_m\left(\frac{R_b}{\beta_f} + R_e\right)} \tag{5.15}$$

$$H_{be}(s) = \frac{1}{1 + g_m\left(\frac{R_b}{\beta_f} + R_e\right)} \tag{5.16}$$

The term $\frac{R_b}{\beta_f}$ in equations 5.15 and 5.16 represents the contribution of the base current. If we assume $\frac{R_b}{\beta_f} \ll R_e$, then equation 5.13 becomes:

$$i_{cIM3L} = \epsilon_{DC}\left(1 - \frac{g_m R_e}{1 + g_m R_e}\right) v_{be}^3 \tag{5.17}$$

Here the additional term $\frac{g_m R_e}{1+g_m R_e}$ comes from the linear amplification of the IM3 voltage v_{be_3} generated by the IM3 collector current which are fed back to the input of the device. Expanding the expression of the collector IM3 current yields:

$$i_{cIM3L} = \frac{g_m(1 - 2g_m R_e)}{6V_T^2(1 + g_m R_e)^5} v_s^3 = K_{3deg} v_s^3 \tag{5.18}$$

This is again the result we found by using the power series expansion of the feedback network in the beginning of section 5.2. This leads to the completion of step 1. Now we need to accomplish step 2 and 3: in step 2 we aim to find the biasing point, and thus the value of g_m, where the maximum $K_{3deg,MAX}$ and the minimum $K_{3deg,min}$ of this function are present; and in step 3 to derive the value of F that gives: $|K_{3deg,MAX}| = |K_{3deg,min}|$. In order to complete step 2 of the analysis, we rewrite K_{3deg} as a function of the feedback factor F:

$$K_{3deg} = \frac{g_m(1-2F)}{6V_T^2(1+F)^5} \tag{5.19}$$

and take the derivative with respect to g_m, obtaining:

$$\frac{\partial K_{3deg}}{\partial g_m} = \frac{6(F)^2 - 8F + 1}{(1+F)^{10}} = 0 \tag{5.20}$$

This equation has two real solutions:

$$F_1 = g_{m_1} R_{e_1} = 0.14 \tag{5.21}$$

$$F_2 = g_{m_2} R_{e_2} = 1.2 \tag{5.22}$$

Which give the values of $g_m R_e$ for which the K_{3deg} is maximum and minimum respectively. Finally, to complete step 3, we replace the found values into equation 5.19 and impose that $|K_{3deg}(F_1)| = |K_{3deg}(F_2)|$, yielding :

$$\frac{g_{m_2}}{g_{m_1}} = 13.77 \tag{5.23}$$

where g_{m_2} is the value of g_m for which $K_{3deg}(F)$ is minimum and g_{m_1} is the value of g_m for which $K_{3deg}(F)$ is maximum. Equations 5.21, 5.22 and 5.23 give the requirements for the biasing and for the choice of the degeneration resistors of the branches A and B in the circuit topology of figure 5.4. The cancellation holds for any combination of $g_{m,A}$, $g_{m,B}$, $R_{e,A}$, $R_{e,B}$ that satisfies these equations. This degree of freedom can be exploited to optimize other important aspects of the amplifier such as gain and efficiency. In order to test the derived solution, the circuit of figure 5.6 has been built. It consists of a CE stage made of two branches, which are decoupled at the input through DC-block capacitors, and are connected at the output node. The $Z_{b,shunt}$ impedance is an equation-defined impedance and it is used to short circuit the common base node for the out-of-band frequencies, in order to avoid indirect mixing. For the degeneration of the two branches, the resistance values $R_{e,A} = 2\Omega$ and $R_{e,A} = 3\Omega$ have been chosen. For these values, the K_{3deg} curves of the two transistors are shown in figure 5.7. From this plot we can derive the optimum value of the collector quiescent current I_{cq} at which transistors Q_A ans Q_B must be biased to achieve the condition $K_{3deg,A} = -K_{3deg,B}$. To see the linearity performance over bias, we set a fixed offset between the biasing

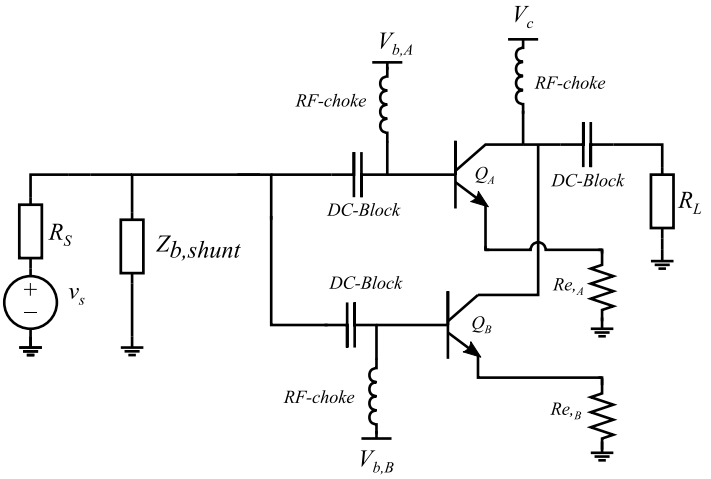


FIGURE 5.6: Test bench circuit used to verify the derived ohmic solution for the DS IM3 cancellation.

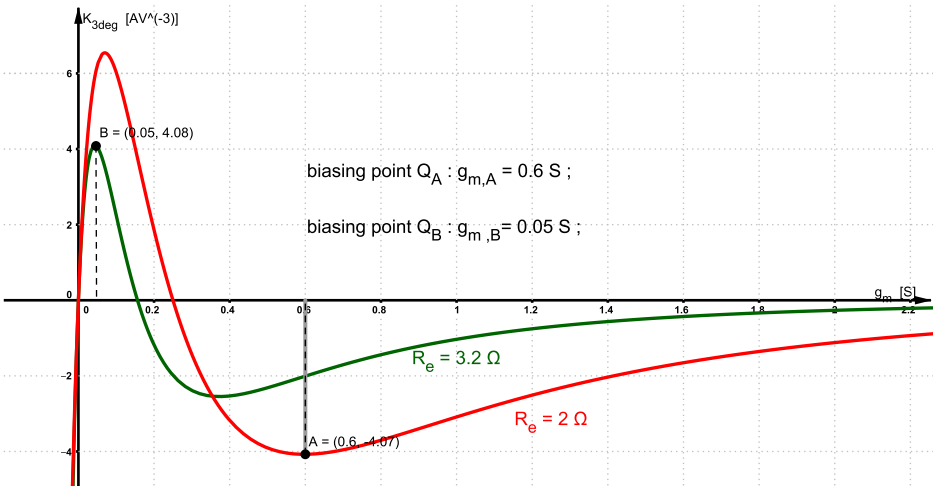


FIGURE 5.7: The third order taylor coefficient plotted versus the linear transconductance g_m for the two used values of the degeneration resistance.

voltages of the two base nodes $V_{b,A}$ and $V_{b,B}$, and perform a 2-tone simulation sweep of the base biasing voltage. The value for this offset which satisfy the optimum biasing conditions for the branches A and B depicted in figure 5.7 was found to be $\Delta V_b = 66$ mV. A reference circuit which makes use of the emitter-tuning Out-of-Band linearization technique is used as means of comparison. In order to make sure that the DS and the out-of-band IM3 cancellation occur for the same DC current budget, a degeneration resistance $R_e = 0.85\Omega$ was used for the emitter-tuned CE stage. For both circuits, a GP model for the BJT is used. Table 5.1 lists the transistor parameters used to characterize the GP model. Since we aim to test the validity of the ohmic solution, we removed from the transistor model those parameters which limit the frequency behavior of the device, namely C_{je}, C_{jc} and τ_f. The simulation details are reported in table 5.2. The resulting plot is shown in figure 5.8, If we look at the results of the DS circuit, we see that 3 OIP3 peaks (or optimum points for linearity) occur at three different biasing

Parameter	**Value**	**Dimension**
I_s	$1.2 \cdot 10^{-15}$	A
β_f	2000	-
C_{je}	0	pF/mult
V_{je}	0.7	V
m_{je}	1/3	-
C_{jc}	0	pF/mult
Vjc	0.7	V
m_{jc}	1/3	-
τ_f	0	ps

TABLE 5.1: List of GP model parameters used for the simulation of the DS-based circuit without memory effects.

f_c	2	GHz
Δf	1	MHz
P_{avs}	-40	dBm (per tone)
V_c	2.5	V
R_S	50	Ω
R_L	50	Ω

TABLE 5.2: List of parameters used for the simulation of the DS-based circuit without memory effects.

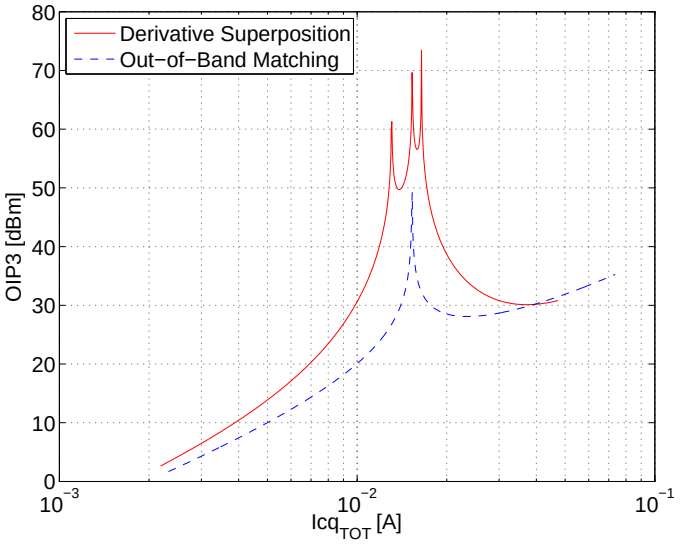


FIGURE 5.8: The OIP3 figure for the Derivative Superposition and the Out-of-Band Matched CE stages, plotted over the total quiescent collector current.

points. In general, the presence of these peaks is due to a (almost) perfect cancellation of the IM3 A and B currents. This occurs when their magnitudes are equal and their phases perfectly aligned. Such a condition is, in practical circuits, very unlikely to be achieved and maintained in different operation conditions, which is the same reason why alternatives to the Out-of-Band technique are being investigated. Therefore, we should use as a figure of merit the range of biasing where the OIP3 is high, rather than the

peak OIP3 value. Using this metric, we can easily see the advantage of the DS method over the Out-of-Band matching.

5.2.2 Solution With Memory Effects

We now include in the circuit those elements which introduce memory effects. This introduction makes the network frequency dependent, and a Volterra Series analysis is necessary to account for the different responses in the involved frequency bands. Again we write the overall expression for the IM3 current as a function of the fundamental voltage components:

$$i_{cIM3L} = \epsilon(s_1, s_1, -s_2)v_{be}(s_1)v_{be}(s_1)v_{be}(-s_2) + g_m v_{be_3}(s_1 + s_1 - s_2) \tag{5.24}$$

This time, since memory effects are included, the expressions of $B(s)$ and $H_{be}(s)$ are frequency dependent, and can introduce phase shifts in the value of the output IM collector current. Let us first focus on the expression of B(s):

$$B(s) = \frac{Z_b/\beta_f + Z_e + s\tau_f(Z_b + Z_e)}{1 + g_m(Z_b/\beta_f + Z_e) + sC_\pi(Z_b + Z_e)} \tag{5.25}$$

The nonlinear current generated by the diffusion capacitance $C_{de} = g_m\tau_f$ introduces a zero, while the interaction between the overall nonlinear current and the total base-emitter capacitance $C_\pi = C_{je} + C_{de}$ introduces a pole. If we impose the frequencies of these two singularities to be the same $\omega_z = \omega_p$, the function $B(s)$ will show a flat phase response, and thus no shift will be introduced to the phase of the IM3 current. If we make the assumption $Z_b/\beta_f \ll Z_e$, the frequency of the zero and of the pole are respectively:

$$\omega_z = \frac{Z_e}{\tau_f(Z_b + Z_e)} \tag{5.26}$$

$$\omega_p = \frac{1 + g_m Z_e}{C_\pi(Z_b + Z_e)} \tag{5.27}$$

setting $\omega_p = \omega_z$ yields:

$$Z_e = \frac{\tau_f}{C_{je}} \tag{5.28}$$

This result is very interesting since it shows the condition for Z_e for which the IM3 currents phase of a degenerated CE stage is flat and independent on the bias current; and it only depends on device technology parameters. We may notice that when $Z_e = 1/2g_m$, we find back the high frequency condition for out-of-band emitter-compensation, reported in Chapter 3: $g_m = C_{je}/2\tau_f$ [8]. This condition ensures therefore the alignment of the IM3 collector currents phases $\phi\{i_{c,IM3}\}$ of transistors Q_A and Q_B, even when

these are biased at two very different current densities, which is required to satisfy condition 5.23. Since the base-emitter junction capacitance C_{je} is directly proportional to the device size, the additional condition 5.28 for the solution of the imaginary part introduces a limitation in the design freedom mentioned in the previous paragraph.
We now look at the frequency dependency of the function $H_{be}(s)$. Since the second order non-linear currents, which interact with the out-of-band impedances defined by $B(s)$, are proportional to the fundamental voltages, to have the phases of the IM3 collector currents of Q_A and Q_B aligned we require that:

$$\phi\left\{v_{be,A_{f0}}\right\} = \phi\left\{v_{be,B_{f0}}\right\} \tag{5.29}$$

This is ensured when 5.28 is satisfied in both branches. The condition 5.29 is not a general requirement for the total IM3 current cancellation; however, when this is guaranteed, we can make use of condition 5.28 to align the phases of the IM3 collector currents of branches A and B. As we did for the ohmic case, we test the validity of the derived solution by simulating a test circuit. This time we include the device parameters

Parameter	**Value**	**Dimension**
I_s	$1.2 \cdot 10^{-15}$	A
β_f	2000	-
C_{je}	0	pF/mult
V_{je}	0.7	V
m_{je}	1/3	-
C_{jc}	0	pF/mult
V_{jc}	0.7	V
m_{jc}	1/3	-
τ_f	2	ps

TABLE 5.3: The GP parameters used for the 2-tone simulation of the DS-based circuit with memory effects.

which cause delay to correctly simulate its frequency behavior. Table 5.3 lists the GP device parameters. To include the effect of the base-emitter depletion capacitance, external components were added between the base and the emitter node of branches A and B, as shown in figure 5.9. Their values are respectively $C_{je,A} = 1.0$ pF and $C_{je,B} = 0.625$ pF, which were found using the condition 5.28. We perform a sweep of the biasing base voltage, and plot the results in figure 5.10 As in the ohmic circuit, also in this case we can observe the advantages of the DS-based CE stage over the out-of-band matched solution.

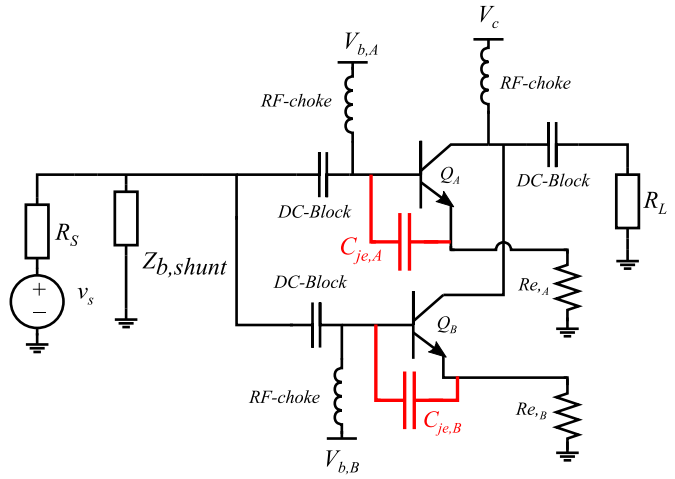


FIGURE 5.9: The position of the added base-emitter capacitors in the derivative superposition circuit schematic.

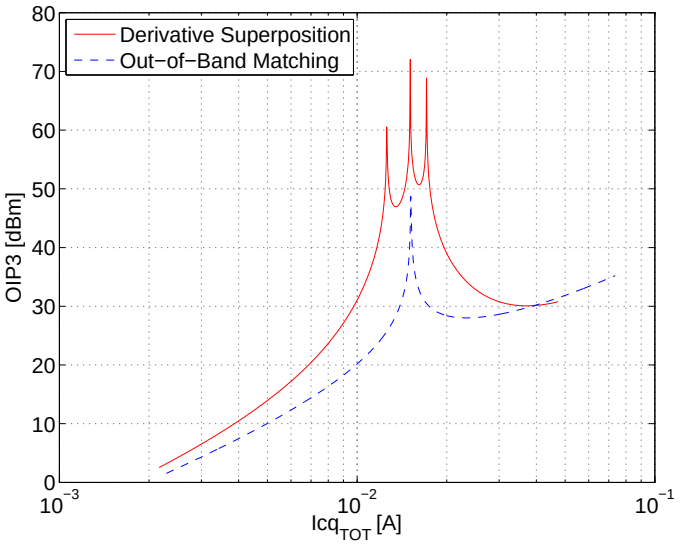


FIGURE 5.10: OIP3 figure plotted versus the total quiescent current for the DS-based and the Out-of-band matched amplifiers, when memory effects are included

5.2.3 High Power Considerations

Up to now, IM3 products have been considered to be generated only by mixing mechanisms of the 3rd order. We have also been assuming that the exponential distortion dominates the overall linearity with its contribution. Nevertheless, for practical applications, we need to take into account those effects that start to appear at low back-off power levels. In first instance we must include the 5th order mixing in our analysis. This type of intermodulation distortion starts to dominate at higher input power levels because it is proportional to the 5th power of the input signal. We can indeed write the

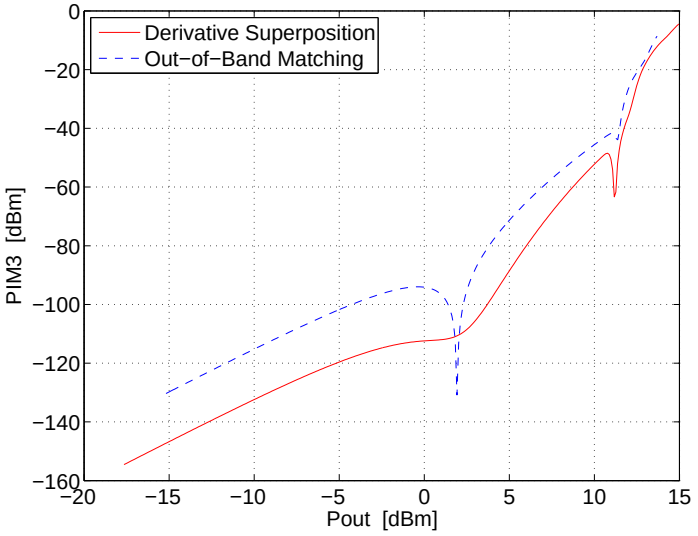


FIGURE 5.11: The IM3 vs fundamental output power comparison between the DS ad the conventional Out-of-Band amplifiers.

IM3 collector current for high power levels in the following way [8]:

$$i_{cIM3} = \frac{3}{4} H_3(s_a, s_b, s_c) v_s^3 + \frac{25}{8} H_5(s_a, s_b, s_c, s_d, s_e) v_s^5 \tag{5.30}$$

A 5^{th} order Volterra Series analysis is needed to completely describe the interaction between all the non-linear elements and the terminations that the circuit provides for the different frequency bands. Because of lack of time, such analysis has not been performed during this project. Another important effect when the input power increases is the consequent increase of the C_{bc} distortion contribution. In fact, when working in class AB, power amplifiers show an increase of the DC current as a function of power due to the self-biasing effect. The increase of the current density makes the base-collector junction capacitance operate in a more non-linear region introducing therefore additional distortion. To show how linearity behaves at different power levels, we make a sweep of the input power and plot the IM3 output distortion. Figure 5.11 compares the performance of the DS and the reference Out-of-Band matched amplifiers. These have been biased in order to show an IM3 "sweet spot" at the same level of fundamental output power. We can see from this plot that the DS shows a more linear IM3 distortion over power. The exact condition that ensures this improvement has not been derived yet. It is believed that the two IM3 and IM5 currents of branches A and B have a similar behaviour over power, allowing the cancellation of the total IM3 output current for a wide range of input power. For the DS method, the cancellation of the IM3 and IM5 components cannot be explained as done in [8] for the Out-of-band technique. In fact, the DS topology is made of two separate CE branches, which interact with each other and have different combinations of operating points for which IP3 sweet spots can be

generated. The analysis of this cancellation mechanisms has not been done during this project because of time limitations, but represents a topic of major interest for future investigations.

5.3 Conclusions

On the basis of what has been reported in Chapter 5, we can draw some important conclusions. We saw in section 5.1 that the characteristic function of a degenerated CE stage has the requirements to be used to implement the DS linearization technique, as a biasing region exists where the third order Taylor coefficient of the voltage-to-current transfer function K_{3deg} is negative. We also mentioned that to ensure the correct operation of the technique it is essential to short-circuit the amplifier driving voltage at BB and 2$^{\text{nd}}$-harmonic band in order to avoid indirect mixing. In section 5.2 the solutions for the Ohmic case and for the circuit including memory effects have been derived. In the former case, the solution consists of a combination of the biasing point and degeneration resistance of the two branches. The device size represents an additional degree of freedom for the designer that can be exploited to boost other performance. In the latter case, an additional condition on the relation between the degeneration resistance Z_e, the forward transit time τ_f and the base-emitter depletion capacitance C_{je} of each branch separately has to be satisfied to align the phases of the two IM3 collector currents. This additional condition puts some limitations on the choice of the device size, as the base-emitter depletion capacitance C_{je} is proportional to the transistor area. The results of simulations performed on the test circuits using GP model show that the DS method provides a high linearity operation for a wider range of biasing currents, when compared to the Out-of-band matching, also when memory effects are included in the device model.

5.4 Future Work

This work represents a first formulation of the circuit solution for IM3 cancellation in bipolar amplifiers through derivative superposition. Future research on this topic is needed to clarify several points which, because of time limitations, where not fully developed in this project. Among them, the effect of the base-collector capacitance on the operation needs further investigation; in particular on the way this element feeds back the IM3 currents coming from both branches, and how this effect makes the two transistors interdependent. One more, important aspect is represented by the high current density at which one of the two branches needs to be biased, in order to

operate in the negative K_3 region. A study on the possible limitations introduced by this condition is suggested as future research on the DS topic. Finally, the behaviour and interaction of the IM3 and IM5 distortion components at low back-off levels of power needs to be further studied to optimize the operation of the DS amplifier with respect to efficiency.

Chapter 6

A Linear Medium Power Amplifier

In this chapter we will describe the design of the realized medium power amplifier, based on the DS linearization technique. During this project, several MPA versions have been designed. The choice of the circuit topology and transistor dimensions are explained in the first part of the chapter. In the second part we discuss in more detail the amplifier version which was chosen for tape-out. We show there the amplifier stages and the biasing blocks, explaining the various design choices. The design of a reference circuit for comparison purposes is also reported. Eventually the simulations of both circuits are shown and some conclusions on their performance are given. All the plots which are presented in this chapter are obtained using the Mextram model of the SiGe HBT. in the QUBiC4Xi process technology used in this work, several SiGe HBT device styles are available. In this design, low voltage (LV) and high voltage (HV) *bnpa* devices are used.

6.1 Circuit Architecture

In view of achieving the original specifications, the following design flow was followed: first a unit-cell version of the MPA circuit has been designed; when this was accomplished, a scaled version of this circuit has been created to satisfy the required levels of output power and OIP3 linearity. Both the unit-cell and the scaled circuits have been diversified in 2 versions, namely the single CE stage and the Cascode topology. This resulted in the overall design of 4 versions, which are listed below:

1. **Unit-Cell CE topology**
2. **Unit-Cell Cascode topology**

3. **Scaled CE topology**

4. **Scaled Cascode topology**

Figure 6.1 shows the topologies of the CE and the cascode versions in a schematic representation of the RF circuitry. We now discuss the advantages and disadvantages of

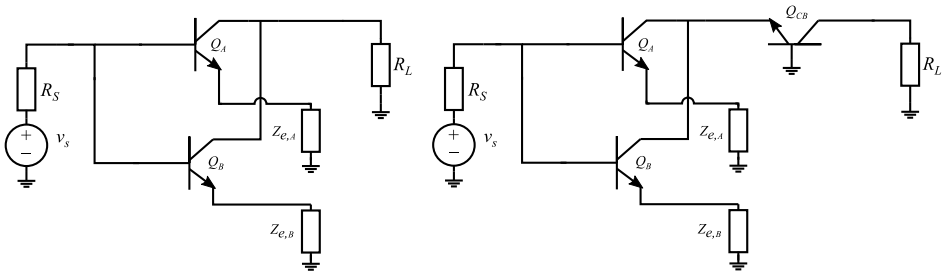


FIGURE 6.1: A schematic representation of the RF signal path of the DS CE and cascode topologies.

these variants grouping them by categories:

Unit-cell designs are characterised by a lower amount of DC and RF current flowing through the transistors and their terminations, which allows to have high on-chip impedance levels. This is preferable for two reasons: one is that there is usually a minimum value for a resistor that can be reliably implemented on chip. In both the out-of-band and the DS techniques the emitter degeneration resistance R_e is inversely proportional to the quiescent collector current, thus a low value of I_{cq} means a higher and more accurate value of R_e. Second, the optimum source and load impedance values for maximum output power are close to 50Ω, reducing the need for matching networks which can be lossy and limit the operating bandwidth. However the unit-cell design does not reach the given output power specification.

To achieve the latter, a 6 times *Scaled* version of the unit-cell has been designed. This version can indeed provide the P_{1dB} required by the specification, but the cost is the need for 6 times lower impedances, including the out-of-band BB and 2^{nd}H base-emitter impedances. Such a requirement can be very limiting in actual implementations, due to parasitics in the circuit layout. We will see in section 6.5 that this represents a limitation for the applied linearization techniques which led to the final choice to only tape-out a unit-cell design to circumvent the problem.

If we instead categorise the versions by topology, we can say that:

The *Single CE Stage* is a simple topology which can result in a very compact layout. Moreover, it only requires biasing circuitry for the CE stage. The drawback is that, as previously shown, its linearity is limited by the C_{bc} generated distortion.

The *Cascode* represents an improvement in terms of unilateral design (reduced S_{12}) as

explained for example in [20], and most important in terms of C_{bc} distortion suppression. We mentioned indeed that the low input impedance of the CB stage reduces the voltage swing over the CE collector node, consequently lowering the influence of the base-collector capacitance.
For the final tape-out, a unit-cell circuit based on a cascode topology (version 2) was chosen. The decision was made based on the goal of creating a test chip which can demonstrate the effectiveness of the developed linearization technique in the current domain, even when the original output power specifications are not achieved.

6.2 DS Circuit Design

In this section, the design of the Unit-Cell Cascode topology version of the MPA will be presented. The DS technique for IM3 current cancellation is used to linearise the

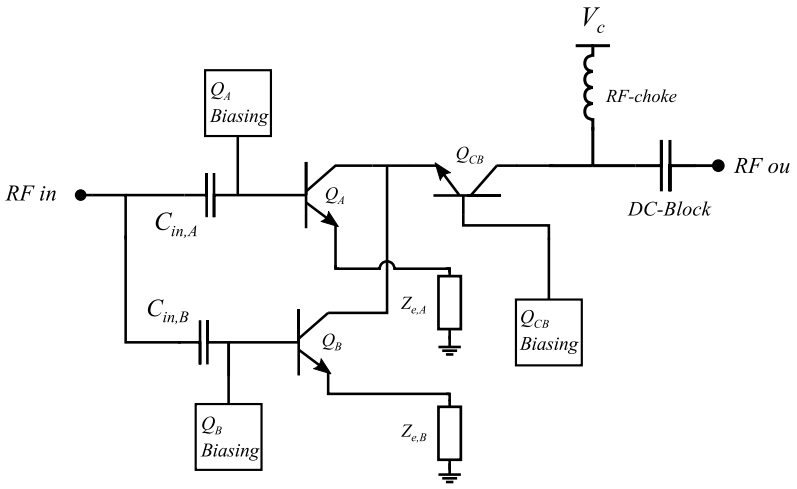


FIGURE 6.2: A schematic representation of the unit-cell cascode topology used for the design of the MPA.

exponential distortion introduced by the CE stage, and the CB stage has the double function of neutralizing the Cbc distortion of the CE stage and making the amplifier more unilateral [20]. All the transistors are biased by on-chip bias circuitry. The latter also plays a crucial role in the linearization due to the out-of-band impedances that they present to the RF transistors. A schematic representation of the cascode amplifier is shown in figure 6.2.

6.2.1 CE Stage

The CE stage is where the linearization technique is implemented. The topology is made of two parallel amplifying branches (A and B). The devices are scaled and biased in such

a way that they generate IM3 collector currents which have the same magnitude but opposite phase. Branch A is the main amplifying path for the RF signal, while branch B is committed to generate the opposite IM3 components of the collector current, which cancel at the output the ones coming from branch A. In general, to achieve the conditions derived in Chapter 5 for the IM3 cancellation on the A and B transconductances ratio, there are 2 different viable approaches:

1. Scaling the transistor of one of the branches with respect to the other, in order to account for the large current difference, while sharing the same base biasing voltage.

2. Introducing a voltage offset $\Delta V_b = V_{b,A} - V_{b,B}$ in the biasing of the two base nodes, that serves to set the proper g_m which results in a positive or negative value of K_{3g_m} depending on the branch.

Method 1 has several advantages: a common base node means that only 1 biasing voltage (and thus circuit) is needed. Moreover, the two branches see the same source impedance at BB frequencies, provided that the input impedance of each branch is high enough in this band. Finally and most important, an LC-resonator used as a 2^{nd} harmonic short, can be connected directly between the common base node and the common node in the emitter path. In this way, an impedance very close to an ideal short can be provided in the wanted band at the input of the amplifying stage. On the other hand, method 2 allows to have comparable size of the two transistors and thus also of the parasitic junction capacitances. It needs nevertheless an additional biasing circuit and one more, large capacitor to decouple the two base DC voltages from each other and from the RF source.
In this design, the choice was to use a compromise between the two methods. Method 2 is limited by constraints in terms of maximum current density, while method 1 is limited by the size of the parasitic capacitance, which becomes too large when only reciprocal scaling is utilized. As a result, the emitter area ratio between branch A and B is 3, and the voltage offset is $\Delta V_b = 61\ mV$. The degeneration impedance is made of a simple resistor in branch A while the parallel combination of a resistor and a capacitor is used for branch B. The capacitor is placed to align the phases of the A and B collector IM3 currents. At the input, two very large capacitors $C_{in,A}$ and $C_{in,B}$ are used to decouple the DC bias from the RF source and from one another. They are scaled proportionally to the input impedance of the two transistors in order to maintain the right power division among the branches. This requirement is very important for the linearization technique to be effective: the IM3 collector current is proportional to the cube of the fundamental base emitter voltage, which in turn is determined by this division. For

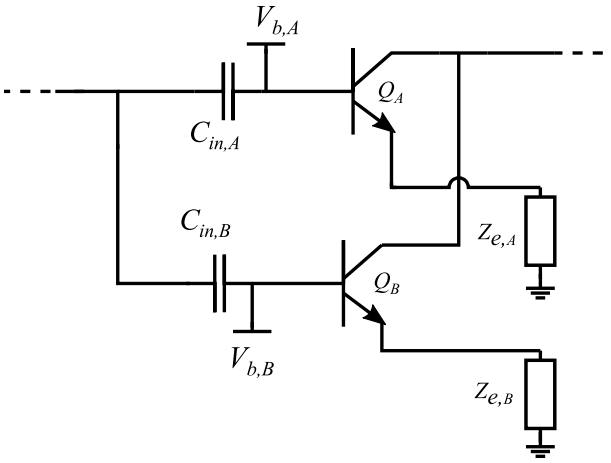


FIGURE 6.3: A schematic representation of the CE stage topology used for the design of the MPA

the CE stage, the low voltage style of the *bnpa* SiGe HBTs has been chosen, with a dimension of 0.5x10.3x2μm^2. This choice is justified by the need for a low base-emitter junction capacitance, in order to fulfil the DS cancellation condition for the imaginary part. The introduction of high voltage devices for the CB stage make it possible to still achieve high output voltage swing. Figure 6.3 shows the schematic of the CE stage. Below we make a list of the active and passive components size and values for the 2 branches of the CE stage:

	Branch A	**Branch B**	
Mult	3	1	-
C_{in}	15	10	pF
R_{deg}	2	2.7	Ω
C_{deg}	0	2	pF

TABLE 6.1: List of the GP model and circuit component parameters for the CE stage of the designed MPA.

The base biasing voltages are provided by on-chip circuitry, which will be discussed in paragraph 6.2.3, and are respectively $V_{b,A} = 0.794\ V$ and $V_{b,B} = 0.733\ V$. The offset between these two values, together with the ratio of the devices area, was chosen to set the transistors operation in the proper region of K_{3deg}.

An LC-resonator is used to provide the 2$^{\text{nd}}$-harmonic short for the driving nodes of the combined transistor. This is placed on one end to the common base node and on the other to the common node in the emitter path, as figure 6.4 shows. The value of the inductance is $L_{res} = 1.2\ nH$ and the capacitance is $C_{res} = 1.3\ pF$. The choice of these values was guided on one side by the need for a very small impedance over the whole 2$^{\text{nd}}$-H band (wideband behaviour), and on the other by the degradation of the

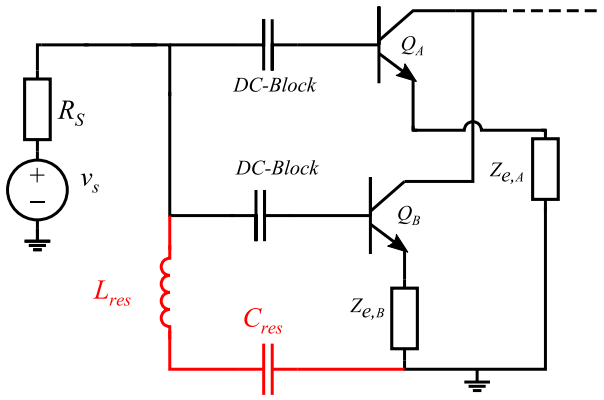


FIGURE 6.4: Position of the LC-resonator in the DS circuit schematic.

S_{21} parameter in the fundamental band. The quality factor of this resonator greatly influences the cancellation, as will be explained in more detail in Chapter 7.

6.2.2 CB Stage

The CB stage is made of a single branch, which serves as a current-controlled current source in series to the linearised current coming out of the CE stage. Its very low input impedance reduces the voltage swing at the collector node of the CE stage, limiting the distortion introduced by the C_{bc} of devices Q_A and Q_B. For the higher output power to be accomplished, high voltage (HV) devices are used in this stage, whose dimensions are 0.5x20.7x2μm^2: they are characterised by an higher breakdown voltage BV, which allows a larger output voltage swing. Nevertheless, the CB collector had to be biased at $V_c = 4\ V$ instead of the standard 5 V to ensure a safer operation and avoid avalanche effects. Four HV devices in parallel are used for the CB transistor, resulting in a total emitter area 2 times larger than the one of the (summed) CE transistors. The base node

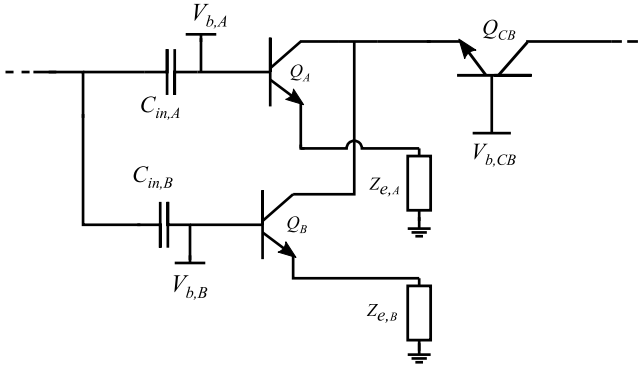


FIGURE 6.5: A schematic representation of the CE and CB stages used for the designed MPA.

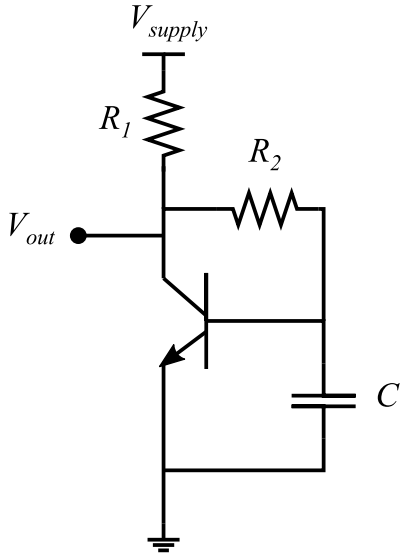
of the CB stage is biased by on-chip circuitry at $V_{b,CB} = 1.9\ V$. To decouple the CB stage base at RF, a large capacitance C_{dec} is placed between this node and the emitter

of the combined CE transistor. In this way, secondary mixing caused by out-of-band base currents in the CB stage is suppressed.

6.2.3 Bias Circuitry

The bias for the CE and CB transistors is provided by on-chip circuitry. The most important requirement for these circuits is to provide the right output impedance in the wanted frequency band. There are in total three biasing blocks: one for the branch A of the CE stage (Block A), one for the branch B of the CE stage (Block B), and one for the biasing of the CB stage (Block CB). We can group these blocks according to the requirements they need to fulfil:

- **Blocks A & B** need to provide the DC voltage for the base nodes of the CE stage, therefore a single forward biased NPN transistor can be used to accomplish this requirement. The output impedance presented to the RF circuit should be as



	Block A	**Block B**	
$Mult$	2	4	-
R_1	190	415	Ω
R_2	800	500	Ω
C	16	8.4	pF
V_{supply}	3.5	2.3	V

FIGURE 6.6: A schematic representation of the circuit used for biasing the base nodes of the CE transistors

low as possible for DC and baseband, while it should resemble an open circuit for the fundamental and 2nd harmonic bands. This is because these blocks provide the BB termination to the RF transistor, which has to be low to avoid indirect mixing; while at the fundamental an 2nd Harmonic bands they should not interfere with the RF signal path. The two blocks A and B make use of the same topology, which is shown in figure 6.6 together with the components value. This topology[1] implements a gyrator: for DC and baseband it acts like a diode-connected NPN

[1]The circuit topology has been proposed by the RF IC designer from NXP dr.ing. M.P. van der Heijden

transistor, while at RF it gyrates the capacitor placed between the base and the emitter nodes into an inductance whose value is $L = \frac{R_2 C}{g_m}$, presenting the wanted high impedance values. In figure 6.7 the impedance offered by blocks A and B are plotted over frequency. We can see that the real part is low for DC and

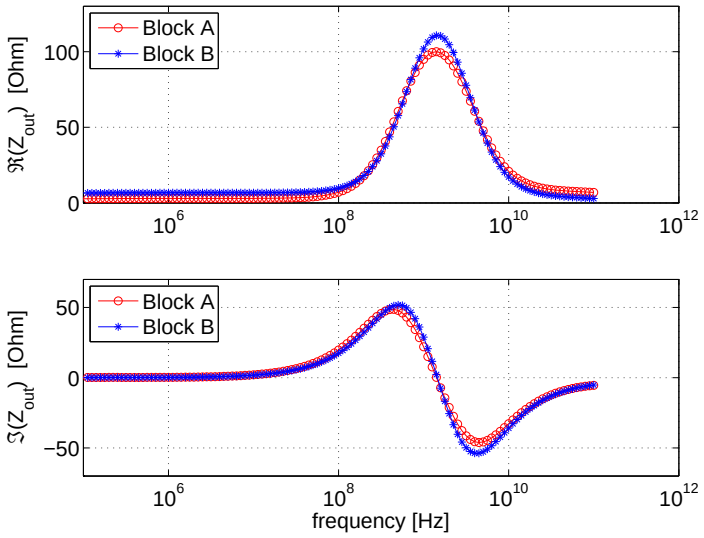
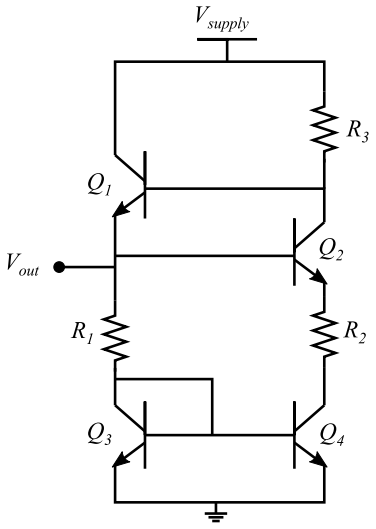


FIGURE 6.7: The real and imaginary part of the output impedance offered by the biasing blocks A & B to the RF circuit.

Baseband, while it rises and reaches a peak at about 1.4 GHz. The impedance starts decreasing at higher frequency due to transistors parasitic capacitances.

- **Block CB** is used for the biasing of the base node of the CB transistor. This block



$Mult_1$	2	-
$Mult_2$	2	-
$Mult_3$	1	-
$Mult_4$	1	-
R_1	30	Ω
R_2	30	Ω
R_3	80	Ω
V_{supply}	3	V

FIGURE 6.8: The on-chip circuit block used for the CB stage transistor biasing

needs to provide a DC output voltage of 1.9 V, which means that the bias voltage of about 0.7 V offered by a single forward-biased junction is too low. Another important necessity of this circuit is to have a very low output impedance in the

whole frequency range involved, which include baseband, fundamental and 2nd harmonic bands. In order to achieve this goal, the circuit of figure 6.8 has been built. The circuit makes use of two feedback loops to lower its output impedance:

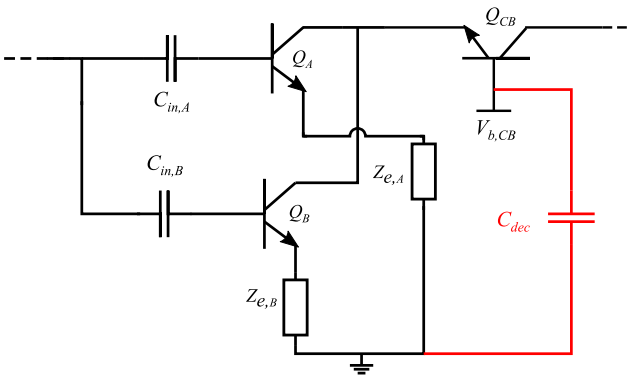


FIGURE 6.9: The position of the DC decoupling capacitor in the schematic representation of the DS amplifier.

transistors Q_1 and Q_2 on top create a feedback loop which reduces the 'cold' impedance seen at the output node, and a current mirror formed by Q_3 and Q_4 doubles the current at the bias node, further reducing the impedance by a factor 2. To achieve a low output impedance Z_{out} at high frequencies, a decoupling on-chip capacitor $C_{dec} = 15\ pF$ is used to short the CB base node to the combined emitter node of the CE stage. Figure 6.9 shows the placement of the decoupling capacitor. In this way, the length of the CB base current loop is minimized, as will be described in section 6.5. We plot in figure 6.10 the real and imaginary part of the output impedance of the designed circuit, comparing the results with and without the decoupling capacitor. For both cases the low frequency output

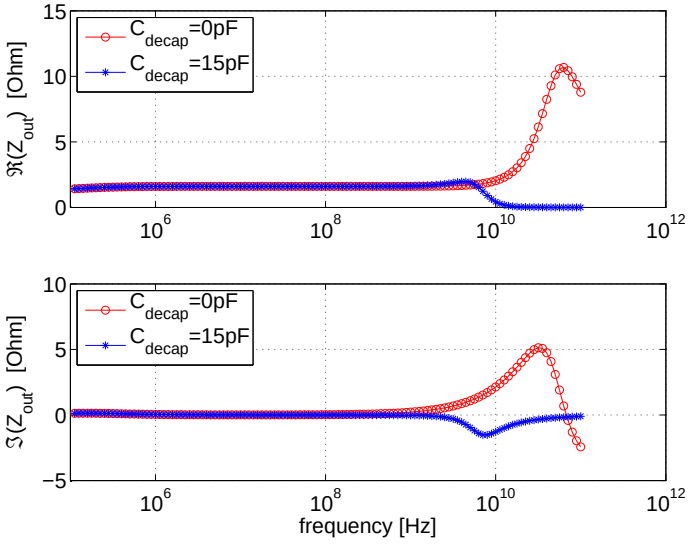


FIGURE 6.10: The real and imaginary part of the output impedance offered by the biasing blocks CB to the RF circuit.

impedance is $Z_{out} = 1.6\ \Omega$. At frequencies higher than 5.6 GHz we note that the presence of the decoupling capacitance lowers the impedance seen at the output terminal.

6.3 Out-of-band Reference Circuit Design

In order to create a valid comparison for the DS based amplifier, a circuit based on the emitter-compensated Out-of-Band linearization technique, which we will from now on call the *Reference circuit*, has been designed. Figure 6.11 shows a schematic drawing of

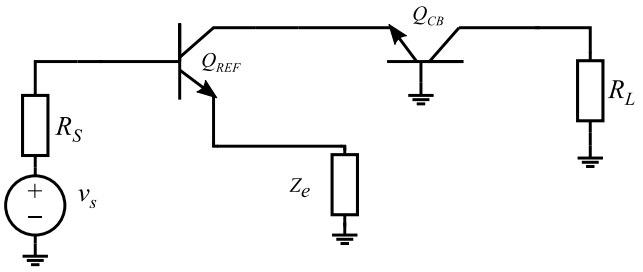


FIGURE 6.11: Schematic representation of the RF signal path in the reference circuit.

the RF signal path of the reference circuit. This circuit has been built such that the peak output power and DC power budget are as close as possible to the ones of the designed DS MPA. To realize this, also the reference circuit is based on a cascode topology. The

$Mult$	3	-
C_{in}	20	pF
R_{deg}	0.55	Ω
C_{deg}	0	pF

TABLE 6.2: List of component values for the RF circuitry of the Reference amplifier.

CE stage is made of a single degenerated transistor, which is biased at the a quiescent current close to the one of the combined CE stage of the DS circuit. The total emitter area of the CE stage of the Reference circuit is (0.5x10.3x2)x3 = $30.9\mu m^2$ and is thus 3/4 of the one of the DS based circuit. For the LC-resonator the values $L_{res} = 0.9\ nH$ and $C_{res} = 1.76\ pF$ have been used. The emitter degeneration resistance is chosen accordingly to the condition for out-of-band IM3 cancellation, and consequently adjusted to account for the intrinsic emitter series resistance of the device. Table 6.2 shows the component values for the CE stage of the reference circuit. The same topology for the CE biasing circuit, as depicted in figure 6.6, is here reused with the proper adjustments. In particular, we want to have approximately the same quiescent collector current for both amplifiers. To achieve this, the values of table 6.3 are used to bias the reference circuit CE stage:

$Mult$	2	-
R_1	280	Ω
R_2	800	Ω
C	4	pF
V_{supply}	3.5	V

TABLE 6.3: List of components values for the CE biasing block of the reference amplifier.

In figure 6.12 we can observe the output impedance offered by the Reference CE stage biasing circuit. The CB stage of the reference circuit is the same as the one designed

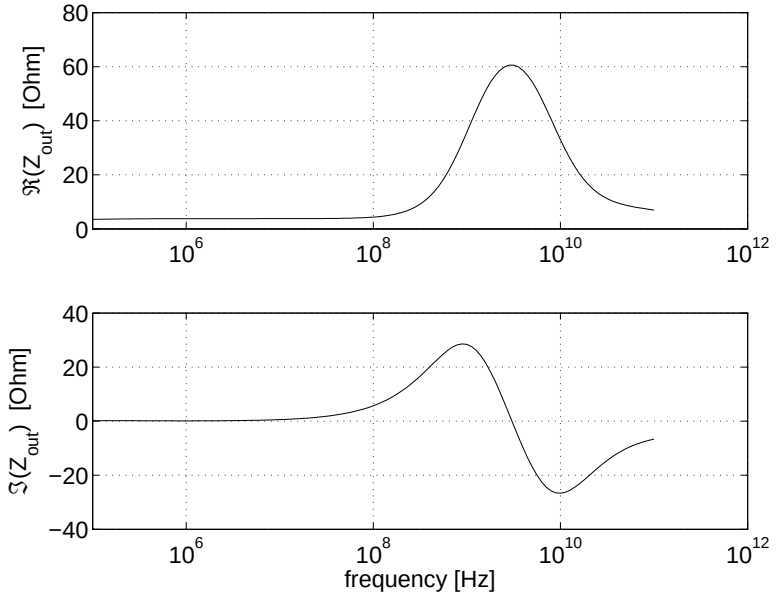


FIGURE 6.12: The real and imaginary part of the output impedance offered by the biasing block for the CE stage of the reference circuit.

for the DS amplifier, in order to provide a similar amount of output power and thus comparable IP3 levels. Also the same CB biasing block is reused.

6.4 Schematic Simulation

In this section we compare the simulations results of the two designed amplifiers. As mentioned, in order to include all the second-order effects that characterize the operation of SiGe HBTs, we use the Mextram transistor model in our schematic. This model allows to switch on or off the influence of several physical mechanism inside the transistor. In particular one can choose between "weak" or "strong" modeling for the avalanche effect in the base-collector junction, and to include or not the effects of self-heating. For this simulation we choose to use "strong" avalanche modelling and to include self-heating

effects. As mentioned in paragraphs 6.2.1 and 6.2.2, we make use of LV devices for the CE stage, and of HV devices for the CB stage.

6.4.1 S-Parameters and Single-Tone Simulation

In order to check whether IP3 linearity levels of the reference and the DS based MPA are comparable, we first perform S-parameters and single-tone simulations. In table 6.4 the

f_c	2	GHz
V_{cc}	4	V
R_S	50	Ω
R_L	50	Ω

TABLE 6.4: List of the parameters for the 2-tone simulation performed on the DS and reference circuits.

simulation parameters are listed. Figure 6.13 shows the Power Gain, the output power and the PAE for the designed DS based amplifier: From the plot of the output current

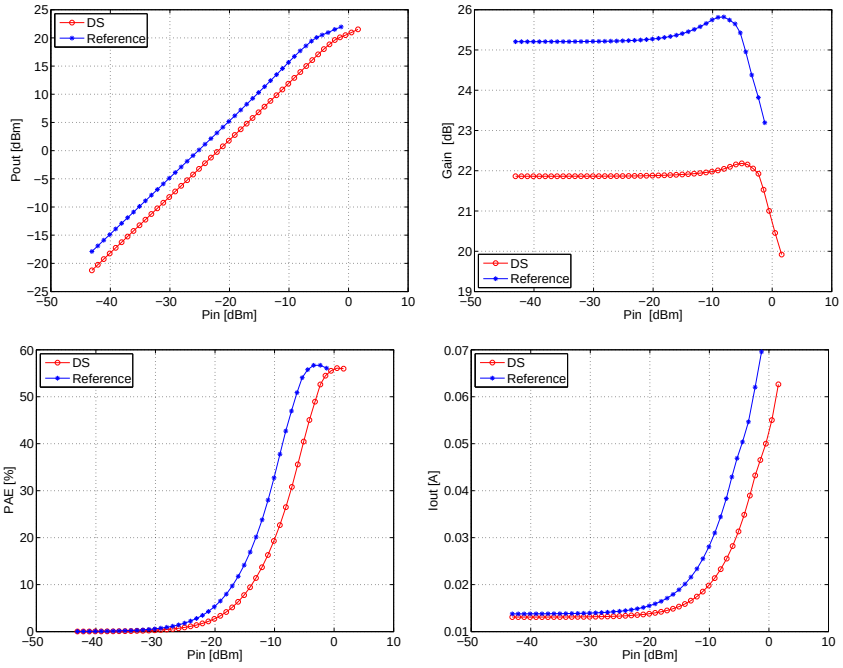


FIGURE 6.13: Comparison of the performance of the DS and reference amplifiers obtained by single-tone simulations.

we can see that the two quiescent collector currents are similar and respectively equal to $I_{cq,Ref} = 13.77\ mA$ and $I_{cq,DS} = 13.09\ mA$. Overall, the two amplifiers have similar peak output power, DC collector current and efficiency performance. The reference circuit shows a linear power gain that is about $3dB$ higher. This can be explained by comparing the feedback factors, defined in Chapter 5 as $F = g_m R_e$, for the reference

and for the branch A of the DS circuit. They are respectively:

$$F_{Ref} \approx 0.5 \tag{6.1}$$

$$F_{DS,A} \approx 1.2 \tag{6.2}$$

The DS circuit is therefore more heavily degenerated than the reference, yielding a lower power gain. We now compare the S_{21} parameter of the two amplifiers to check whether the resonance caused by the LC circuit is centered at the right frequency. From

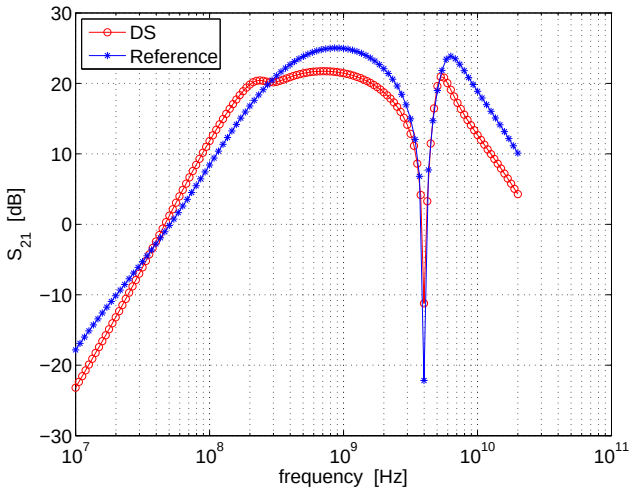


FIGURE 6.14: The magnitude of the S_{21} parameter in dB for the DS and the reference amplifiers.

figure 6.14 we can see that the resonance peak occurs at two times the nominal carrier frequency $2f_c = 4\,GHz$ for both amplifiers.

6.4.2 Two-Tone Simulation

In this paragraph the results from two-tone simulations performed on the designed circuits are compared. First we make a sweep of the quiescent current to show the behavior of the OIP3 figure at different biasing levels. In Table 6.5 the parameters used for the

f_c	2	GHz
Δf	10	MHz
V_{cc}	4	V
P_{avs}	-40	dBm (per tone)
R_S	50	Ω
R_L	50	Ω

TABLE 6.5: List of the parameters for the 2-tone simulation performed on the DS and reference circuits.

2-tone simulation are shown. Figure 6.15 compares the OIP3 linearity measure of the DS

based and the reference amplifier. What emerges from this plot is the much wider bias-

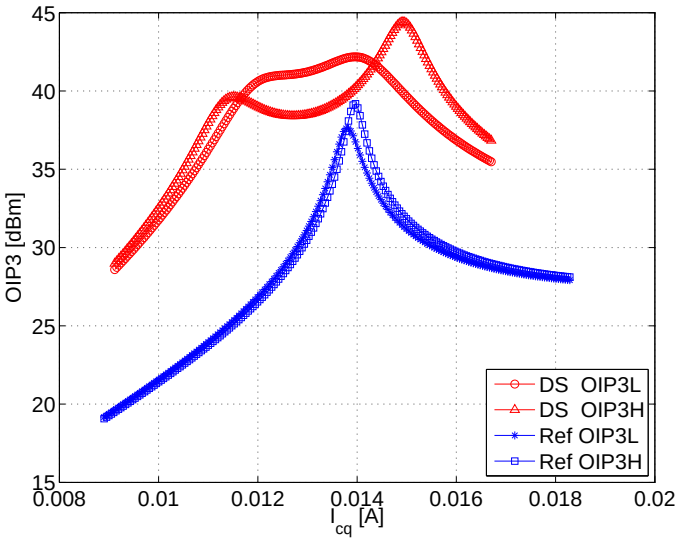


FIGURE 6.15: The compared OIP3 figures of the DS and the Reference circuits plotted versus the biasing current.

ing range for the DS based MPA for which the OIP3 figure is higher than 35 dBm. Now we bias the amplifiers at their nominal points: $I_{cq,DS} = 13.1\ mA$ and $I_{cq,Ref} = 13.8\ mA$ and perform a sweep of the input power to see the behavior of the IP3 figure in the wanted operating region of high efficiency. The results of this simulation are shown in figure 6.16. We can observe that the DS technique improves the linearity level of the

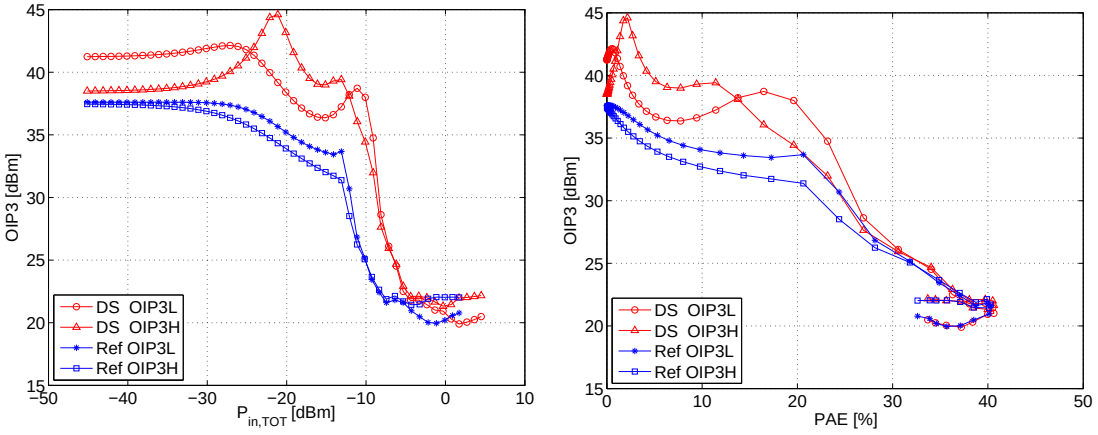


FIGURE 6.16: Comparison of the IP3 linearity performance between the DS-based and the reference amplifiers for a sweep of the input power.

DS based amplifier is higher up to a level of input power of about 0 dBm, where the efficiency peaks. As shown in Chapter 3 for the reference, also for the DS circuit its is possible to bias the amplifier at a slightly different quiescent current to increase the linearity at lower levels of back-off power. A sweet spot can be generated by the mutual interaction of 3rd and 5th order mixing components, which partially cancel each other for

a determined level of input power. Figure 6.17 shows this effect by plotting the output power at the IM3 frequencies versus the total input power, for the DS based amplifier. From this plot we can see that by lowering the quiescent current to $I_{cq} = 12.5\ mA$, a

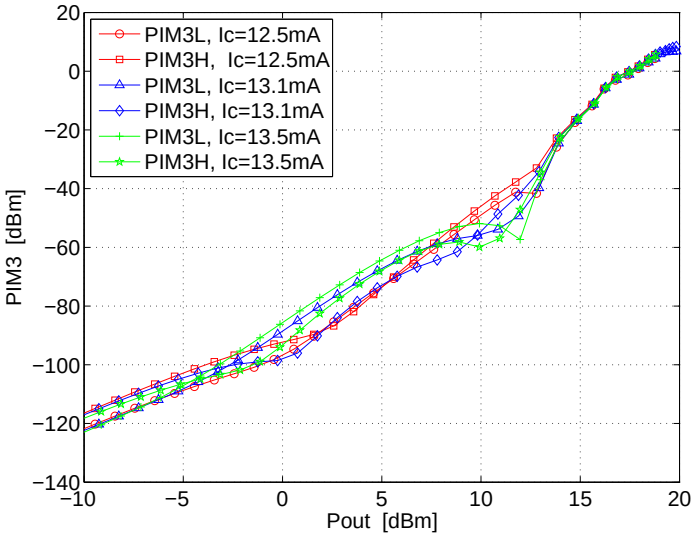


FIGURE 6.17: The power at the IM3 low and high frequencies of the DS amplifier for different biasing points.

sweet spot is generated for an output power of $P_{out} = 4$ dBm, while increasing it to $I_{cq} = 13.5\ mA$, the sweet spots are generated above $P_{out} = 10$ dBm. This suggests that the level of output power at which the sweet spot occurs increases with increasing biasing current.

6.5 Chip Implementation

In this section we discuss the steps followed to implement the test chips based on the described designs. The first part is dedicated to study how the parasitics introduced in the layout implementation affect the linearization technique. We analyse here these effects at a schematic level, by including extra lumped components in the schematic and by using equation defined impedances, which can describe the electrical effects of the geometry and physical parameters. In the second part, we describe the most relevant choices in the layout design, according to the analysis made in the first part. A Momentum simulation of the final layout configuration is performed and the results are presented. To conclude, the stability of the circuit is analysed, and some measures are taken to reduce the possibility of oscillation events.

6.5.1 DS Circuit Sensitivity Analysis

In view of preserving the IM3 cancellation, the major concern is to avoid indirect mixing due to feedback of the IM2 components. In the designed circuit topology, there are several nodes which, when affected by unwanted parasitics (resistive, capacitive or inductive), result in secondary mixing and degrade the cancellation effectiveness. These are:

- **The emitter lead of the (combined) CE stage:**
  This is a very sensitive part because it feeds the collector current content back to the input of the amplifier, and every series impedance in this path weights a factor β_f more than any series impedance in the base lead. One of the most harmful parasitics at RF is the self-inductance of the emitter track. When this inductance is in series with the collector current loop, a significant undesired voltage drop can be created across its terminals. We test this effect by placing in the schematic a lumped inductor L_e in series with the degeneration resistors of branch A and B, as shown in figure 6.18. We then perform the same 2-tone simulation for increasing

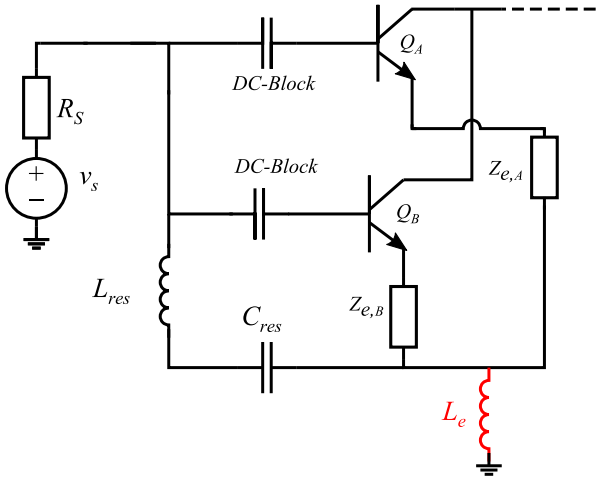


FIGURE 6.18: The position in the schematic of the parasitic inductance L_e.

values of the parasitic inductance L_e. The results are plotted in figure 6.19. A parasitic inductance in the emitter lead affects the cancellation in two ways: first it changes the fundamental power division between the two branches, making the two base-emitter voltages more dependent on each other; in second place, if the 2nd Harmonic short is not perfect (e.g the LC resonator presents a finite quality factor) it generates indirect mixing through the 2nd Harmonic band and thus IM3 distortion. To show this phenomenon, we compare the OIP3 figure of the amplifier with a fixed value of the emitter parasitic inductance $L_e = 30\ pH$ in two cases: in the first the 2nd Harmonic resonator has no series resistance; in the second case

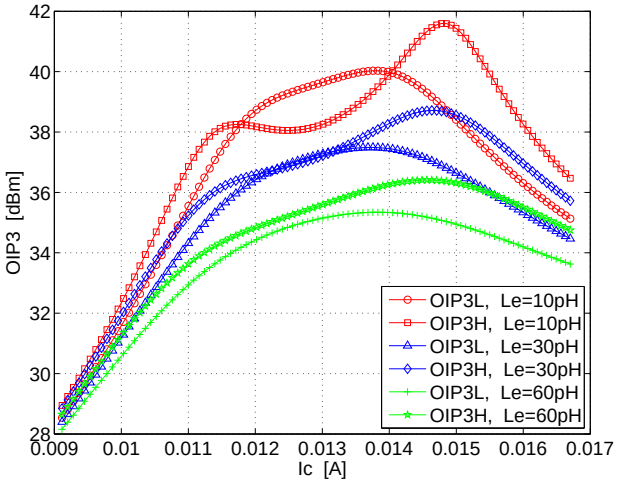


FIGURE 6.19: The OIP3 figure plotted against the collector quiescent current for different values of the emitter parasitic inductance.

it presents a series resistance of $R_{series} = 3\Omega$. We can see from figure 6.20 that

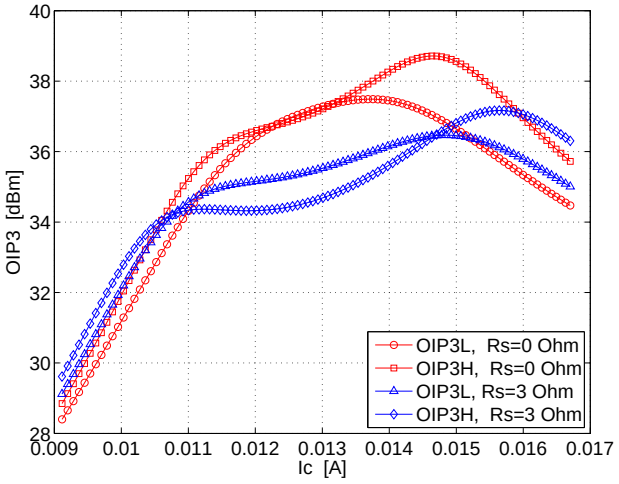


FIGURE 6.20: The OIP3 figure plotted against the collector quiescent current with for different values of the resonance inductor series resistance.

in the first case, the OIP3 level stays high, because the inductance only affects the fundamental power division; while in the second case the OIP3 level drops significantly due to the introduced secondary mixing.

- **The CE Stage Input BB Termination:**
  Another very important aspect is represented by the impedance provided by the biasing blocks A and B. In particular, they provide the BB termination seen by the CE stage transistors base, and are therefore directly involved in secondary mixing mechanisms. Moreover, if the impedance offered by the biasing blocks at RF is not high enough, they also influence the fundamental power transfer from

the source to the base-emitter voltages of the two transistors. As mentioned, this effect directly affects the IM3 collector current cancellation.

- **CB Base Termination**:
  Another requirement of major impact is to keep the impedance in the loop of the CB stage base current very low in all the involved frequency bands. Also in this case we can compare the simulation results in the ideal case, when a voltage source with zero output impedance is used to bias this node, and in a more practical condition by introducing the designed biasing circuit.

These three aspects need to be carefully implemented in the layout in order to avoid unwanted parasitics to degrade the effectiveness of the IM3 cancellation.

6.5.2 Layout Design

The designed circuit has been implemented in the QUBiC4Xi BiCMOS process technology of NXP. The chip layout[2] can be divided in two main parts: The "core", which

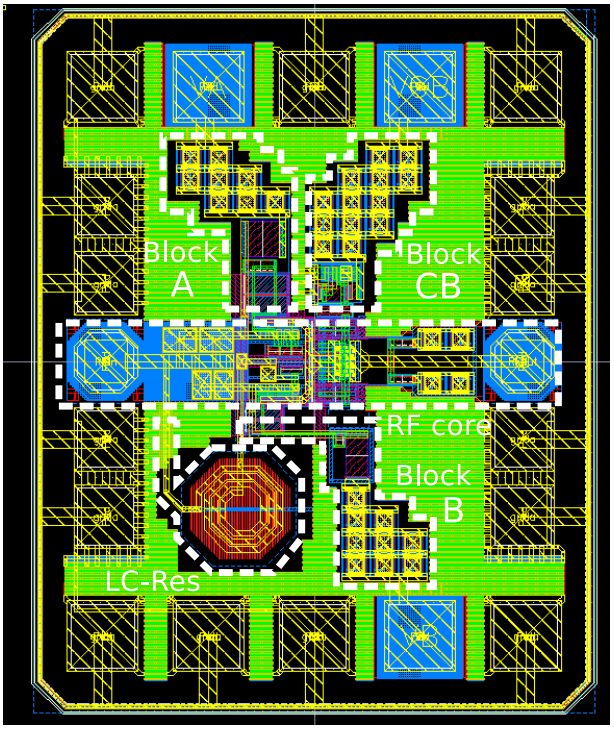


FIGURE 6.21: The die layout of the implemented DS amplifier. On the figure the "core" area, which includes the RF transistors and signal paths, and the other circuit blocks are highlighted.

[2]The Layout has been done in collaboration with the Ph.D. candidates E.S.Malotaux and J.M.M van der Meulen, and the layout designers from NXP J. Baltazar and G. Cunanan.

includes the fundamental RF signal path; and the surrounding circuitry, consisting of the biasing blocks, the LC resonator for the 2nd harmonic short and the decoupling capacitors for the on-chip supply lines. Figure 6.21 shows these areas in the layout. The analysis made in paragraph 6.5.1 directly translates into important considerations to be accounted for in the layout design. To suppress the effect of a parasitic inductance in the emitter path at the 2nd harmonic band, the LC resonator is placed between the base and the combined emitter nodes to achieve the short condition. In this way, any parasitic in the ground path will result in parallel to the harmonic short, and therefore will have no influence on the operation in the frequency band where the LC circuit is resonating. The self-inductance of every additional length in the LC structure was absorbed in the overall value of L_{res}, and the capacitor is placed as close as possible to the combined CE stage emitter node.

For what concerns the impedance offered by the biasing circuits, the following measures have been taken: for the blocks A and B, the capacitor that is meant to short the base-emitter junction of the biasing transistors is placed very close to the latter, such that no additional length can affect the circuit operation at RF introducing inductive effects. To reduce the impedance of the CB base node, CE and CB stages are placed very close together and a large capacitor between them couples the CB base node to the combined CE emitter at RF, keeping the loop of the CB base current very short. To avoid the

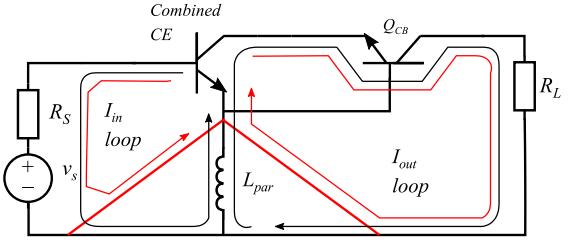


FIGURE 6.22: A schematic representation of the division between the input and output current loops.

output current content to be fed back to the input, the shared path between the input and output current loops needs to be minimized, as shown in the schematic of figure 6.22. In this representation, we can see in black the conventional grounding scheme, in which the parasitic ground inductance is shared between the two current loops. When the configuration in red is adopted, the output current does not affect any more the input voltage. In order to do this, two separate planes have been used for the input and the output ground, which only connect in the center of the layout. This configuration is shown in figure 6.23, and will be referred to as *Star Ground* configuration. Because of time limitations, no momentum view has been created to show the effectiveness of this ground topology. For this reason, both alternatives have been designed and taped-out, such that a comparison could be done in the measurement stage. As no evidence of a

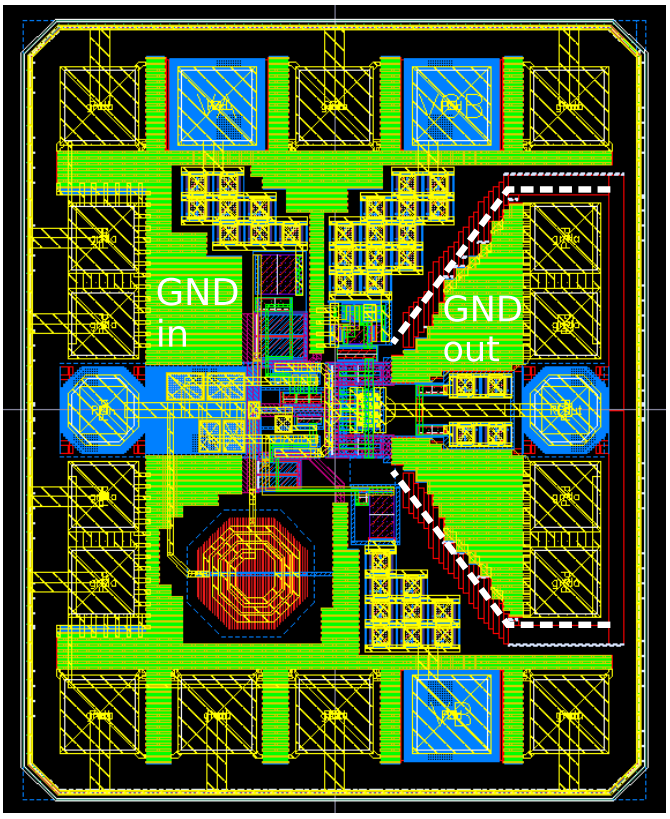


FIGURE 6.23: The chip layout version with separate input and output ground configuration.

difference between the measured results of the two ground configuration was found, it is believed that both achieve the wanted separation of the input and output current loops.

6.6 Momentum Simulation

The implementation of the layout has been done in parallel with momentum simulations, which were used to check the effect of the layout design choices on the circuit operation. Here we present the results of the simulation of the previously introduced schematic, this time including the effect of interconnects and components sizes in general, accounted by the momentum simulation. In figure 6.24 a representation of the momentum view[3] is shown. The actual layout has been simplified to reduce the simulation time of the Momentum algorithm. Nevertheless, several important elements, such as the inductor L_{res} and the RF tracks lengths, have been incorporated in detail to properly verify their influence. Now we compare first the momentum and the schematic simulation, discussing the effects of the layout geometry and physical parameters on the operation of the amplifier. Next we compare the results of Momentum simulation of the DS and

[3]The momentum view has been done by the TU Delft Ph.D. candidate J.M.M. van der Meulen

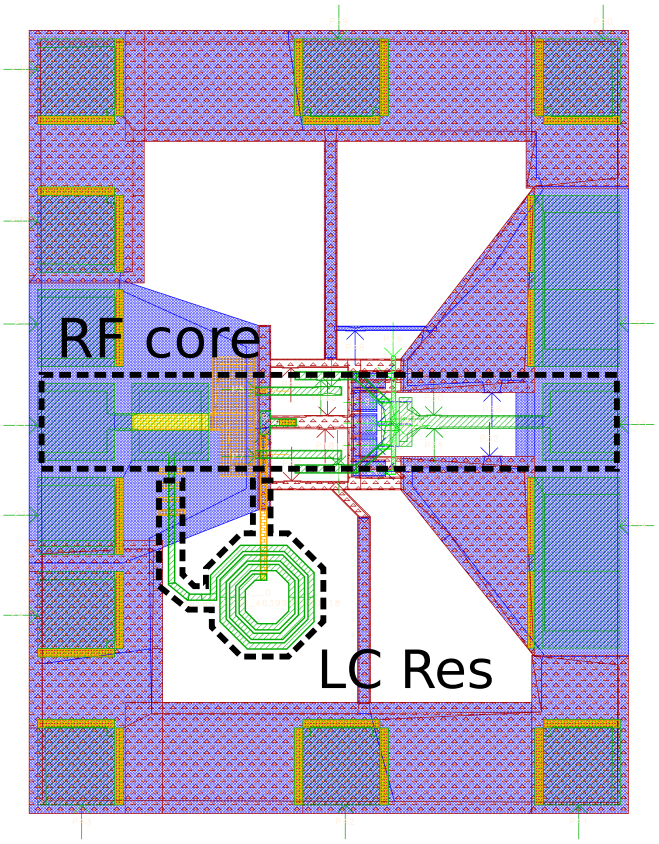


FIGURE 6.24: The Momentum view used to simulate the effect of the layout geometry on the circuit electrical properties.

the Reference amplifiers. In table 6.6, the new component list for the DS circuit that includes the momentum view is shown. The value of the components have been adjusted

	Branch A	**Branch B**	
Mult	3	1	-
C_{in}	15	10	pF
R_{deg}	2	2.3	Ω
C_{deg}	0	2	pF

TABLE 6.6: The new component values used in the simulation of the amplifier including the Momentum view.

to account for the effects of layout. In particular, different values for the degeneration resistance and the base biasing voltage of branch B have been used to properly set the magnitude and phase of the $i_{cB,IM3}$ current. In order to be measured, the chip will have connections with external circuitry through bond-wires. For a more complete and accurate simulation, the effect of bond-wires self inductance has been accounted for by placing lumped inductors in series with each supply and ground line. In particular, for

the downbonds, a value of $L_{db} = 1\ nH$ has been used, while for the other bondwires we have used $L_{bw} = 2\ nH$. The input and output RF ports are floating, as this is the actual condition provided by the system utilized for measurements, as will be described in Chapter 7. These adjustments have very small effect on the other performance of the amplifier, such that the P_{1dB}, Gain and efficiency parameters are maintained. Figure

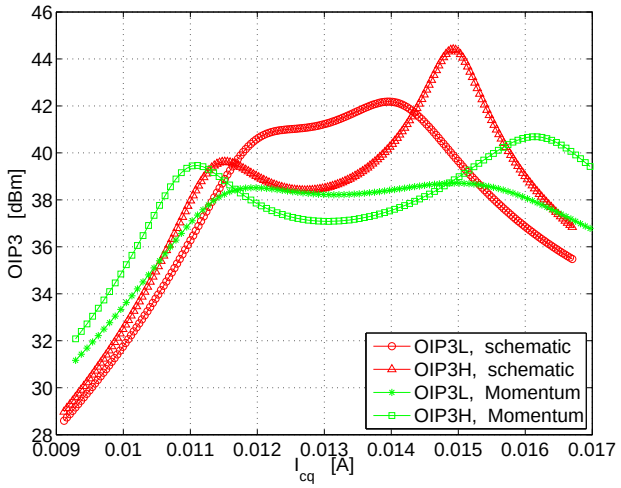


FIGURE 6.25: The OIP3 figure resulting from momentum and schematic simulation of the DS based cascode amplifier.

6.25 shows the OIP3 versus the total quiescent current. If we compare this result to the simulation performed on the original schematic we observe that the peak OIP3 level is lowered, but the wide biasing range for high linearity is maintained.

6.6.1 Stability Analysis

The stability of the circuit over the whole frequency spectrum has to be ensured to avoid any possibility of oscillations. The circuit stability was first analysed using the Rollet stability factor k. When no stabilization circuitry is added, this parameter drops

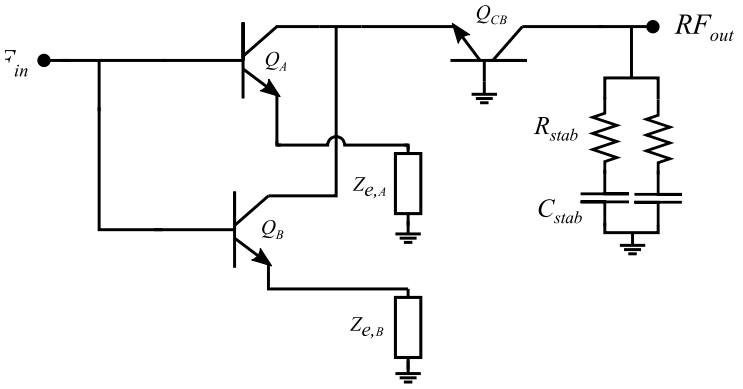


FIGURE 6.26: A schematic representation of the RC-network used for stabilization purposes.

below the inconditional stability level $k = 1$ for certain frequency ranges. To improve the stability in the frequency range where $k < 1$, an RC network in parallel to the load impedance is used to act on the S_{22} parameter. In particular, two branches (in order to keep the layout symmetric) consisting of a series RC combination are used, as shown in figrue 6.26. The value of the resistance is $R_{stab} = 1\ k\Omega$ and the value of the capacitor is $C_{stab} = 2\ pF$. We plot in figure 6.27 the stability factor before and after the stabilization network has been added: We can see that with the addition of this network, the Rollet

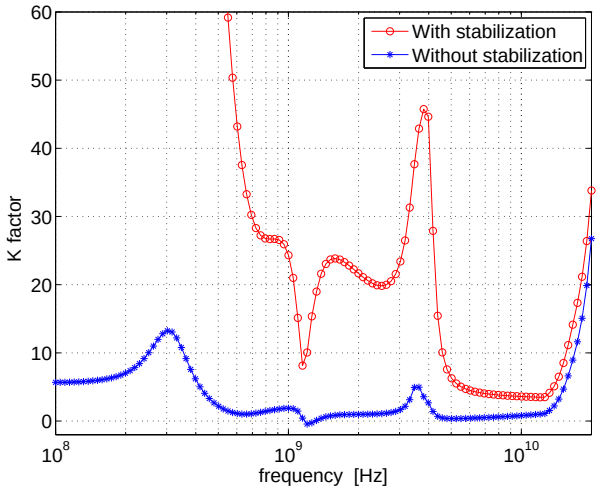


FIGURE 6.27: The Rollet stability factor value over frequency for the designed amplifier.

stability factor is $k > 1$ in the whole frequency range. A final transient test has been performed to make sure that there are no hidden effects in the circuit which can trigger oscillation: a voltage step function is used to excite the circuit with a signal that covers the whole frequency range. The result of this simulation is that, after a small transient, all the nodes steadily settle back to their previous value.

6.6.2 Final Results

Now we present the simulation results of the final circuit, including the stabilization network. In doing it, we compare the performance to the reference circuit. First, we

f_c	2	GHz
Δf	10	MHz
R_S	50	Ω
R_L	50	Ω

TABLE 6.7: List of parameters used for the 2-tone simulation of the amplifier schematic including the momentum view.

compare the linearity levels of the two amplifiers at different biasing points, as we have

done in paragraph 6.4.2. Figure 6.28 shows the OIP3 versus collector quiescent current for the circuits in exam. The results have been obtained using the parameters of table 6.7. One aspect that we can note from this graph is that the peak OIP3 value for

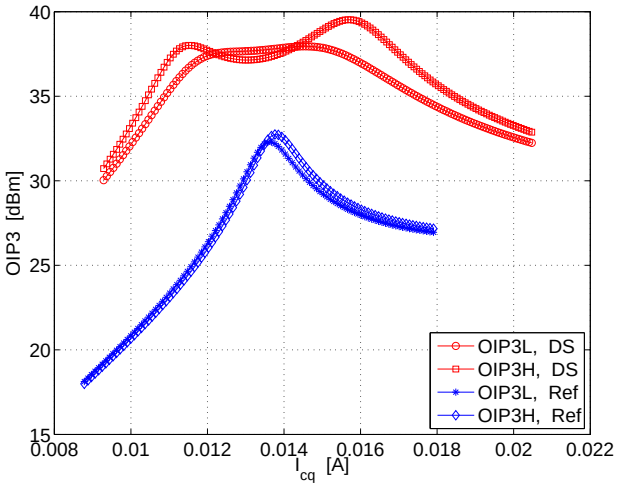


FIGURE 6.28: Comparison of the OIP3 figure achieved with the DS and reference circuit including the momentum view in the simulation.

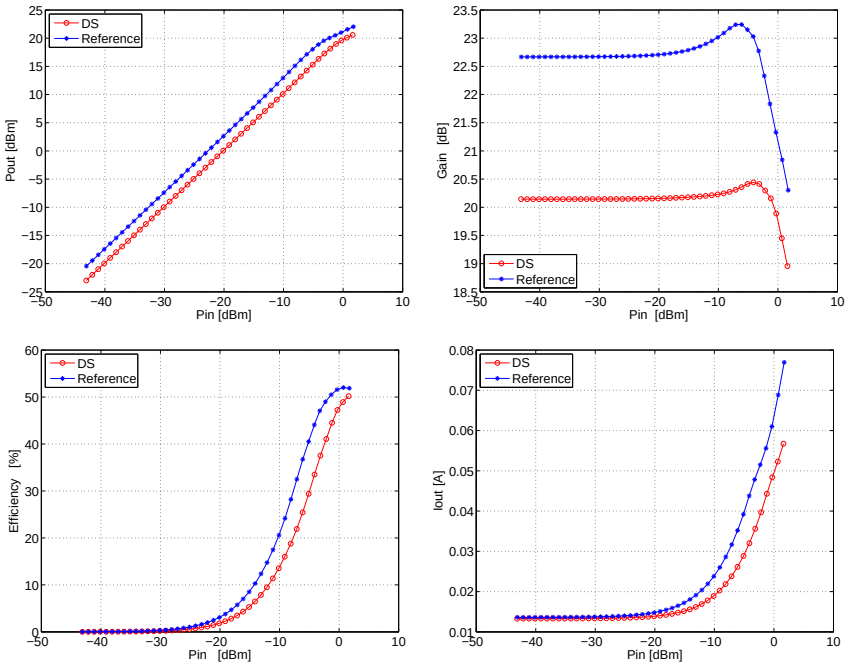


FIGURE 6.29: Comparison between the single-tone performance of the DS and reference amplifiers, with the inclusion of the momentum view.

the reference circuit has significantly degraded in comparison to the simulation of the "pure" schematic circuit. This is because, as mentioned several times, the amplifier operation can shift from the optimum out-of-band condition for cancellation due to layout parasitics. Based on the OIP3 results of figure 6.28, we bias the two circuits at the following current levels $I_{cq,Ref} = 13.6\ mA$ and $I_{cq,DS} = 13.3\ mA$; and run a

single-tone simulation to check the other performance of the amplifier. From the results of figure 6.29 we observe that the power Gain for both configurations has lowered, when compared to the values of the schematic simulations. This due partially to the addition of the stabilization network and partially to the losses introduced by the momentum view.

6.7 Conclusions

Here, the conclusions upon the designed circuits are discussed. In section 6.1 we have said that a unit-cell cascode amplifier topology presents the best requisites to show the effectiveness of the developed DS technique, when implemented in a test chip. This is thanks to the C_{bc} distortion suppression in the CE stage, the improved unilaterality of the amplifier and the more relaxed requirements on the impedance levels. For the fulfilment of the DS IM3 cancellation condition, the use of both transistor scaling and biasing voltage offset methods allows to have reduced size of parasitic capacitor and similar current densities. In section 6.5 the importance of the layout design to avoid secondary mixing is emphasized: the LC-resonator has been implemented such that every additional track length is absorbed in the overall value of the inductance, and the biasing transistors are placed very close to the RF ones, to avoid additional series inductance. Table 6.8 compares the results obtained in simulation with the designed DS and reference MPAs: Here we define $\Delta I_{cq,OIP3}$ as the range of biasing current for

Performance	**DS MPA**	**Ref MPA**	**Unit**
$DCPowerBudget$	13.3@4	13.6@4	mA@V
P_{1dB}	20.6	20.5	dBm
$OIP3$(L/H)	37.6/39.5	32.4/32.1	dBm
$\Delta I_{cq,OIP3}$	42.2	13.8	%
G_P	20.1	22.7	dB
$Eff_{@P1dB}$	50.2	50.5	%

TABLE 6.8: Comparison between the simulated performance of the DS-based and the Reference Out-of-band based amplifiers.

which $OIP3_{DS} > 35$ dBm and $OIP3_{Ref} > 30$ dBm, expressed in percentage of the total quiescent current I_{cq}. From these results, we can conclude that the DS technique ensures a larger range for the biasing current I_{cq} where the linearity is high. This makes the DS technique more robust than the out-of-band linearization over variations of the biasing point.

6.8 Future Work

The application of the Derivative Superposition linearization technique to bipolar amplifiers is at the beginning of its development, and there are still many aspects that need to be further investigated for an optimal implementation of this method in power amplifiers. Here, we report the aspects that we believe need to be studied in future research to complete the findings of this thesis work.
In this project, a high power scaled version of the DS based MPA has been designed, but not implemented in a test chip. This represents an interesting research goal which presents several challenges. The main one is to lower the out-of-band impedance of-

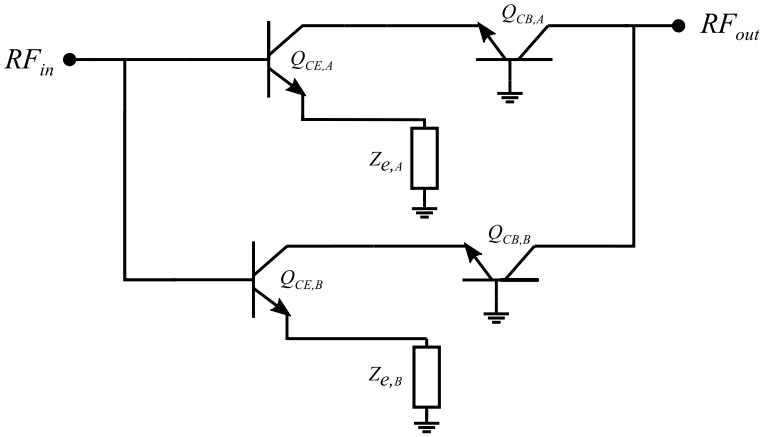


FIGURE 6.30: A representation of the RF signal path for the topology using two parallel cascode branches.

fered to the input current loop, in order to minimize indirect mixing effects. This can be accomplished combining the proper component choices for the biasing blocks at a schematic level, and a careful layout design. Specifically, the positioning of the input LC-resonator and the on-chip ground connection are of major importance in this view. New configurations of the CE and the CB stages can also introduce benefits to the amplifier operation. An example consists of the use of more than two branches for the CE stage. Another alternative to the topology of choice in this design is a CB stage made of two branches, in which the transistors are scaled to operate at the same current density and therefore have similar f_t. This solution, depicted in the schematic of figure 6.30 has not been chosen because in this design the two CB branches are shifting the phases of the separate IM3 currents by a different amount, resulting in deviation from the cancellation point and consequently in a larger total IM3 current. However, time restrictions limited the investigation of this alternative, which represents an interesting subject for future research.

Chapter 7

Measurements

In this chapter, the results of measurements performed on the implemented chips are reported. In total, four different MPA chip versions have been fabricated and tested. Two of them implement the DS based amplifier while the other two implement the Reference amplifier. Within these categories, there are in turn two chip versions which are differentiated by the ground layout configuration. Since the two different grounding configuration gave similar results, in this chapter we will not distinguish among them, and focus on the comparison between the designed amplifier implementing the DS technique, and the Reference based instead on the Out-of-Band matching technique. The chapter is structured as follows: first, the design of the printed circuit board (PCB) where the chip has been mounted is described. A second section is dedicated to explain the measurement setup utilized for the different measurements. Finally the results of the performed measurements are shown, and conclusions are drawn upon the comparison of the two designed chips and with the simulated performance.

7.1 Printed Circuit Board

The designed chip layout presents ground-signal-ground (GSG) pads for the input (RF) and output (RF and DC) signals; while differential ground-signal-ground-signal-ground (GSGSG) pads on the top side and on the bottom side for biasing purposes. To excite the circuit, GSG RF probes were used at the input and at the output, while a PCB connected to the IC via bondwires is committed to provide the wanted levels of supply power for the on-chip biasing blocks, making use of the top and bottom pads. A picture of this configuration is shown in figure 7.1. The layout of this PCB [1] is depicted in figure 7.2. It consists of four bias lines which are decoupled at high frequencies to the

[1]The PCB layout is based on a previous work of the TU Delft Ph.D. candidate E.S. Malotaux

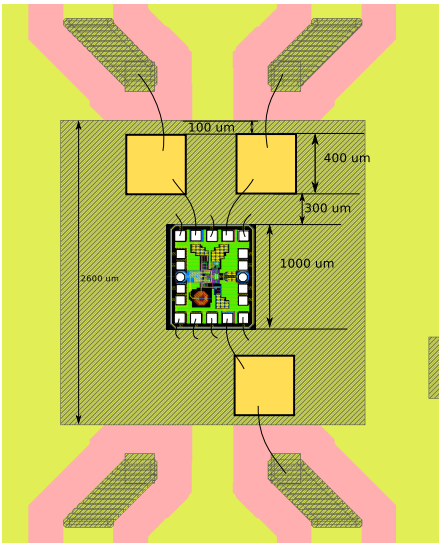


FIGURE 7.1: A graphical representation of the chip bonding to the PCB.

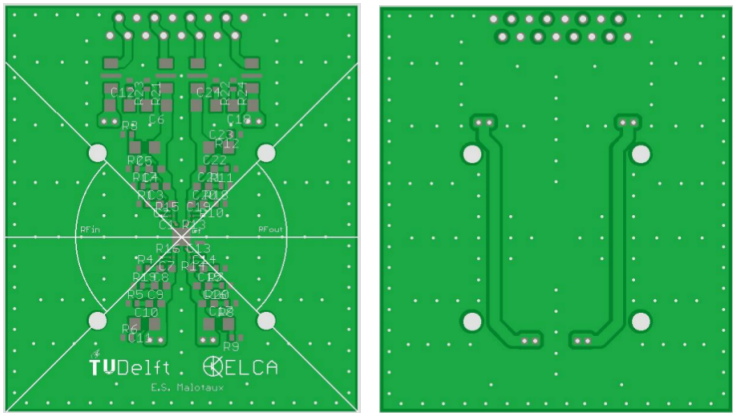
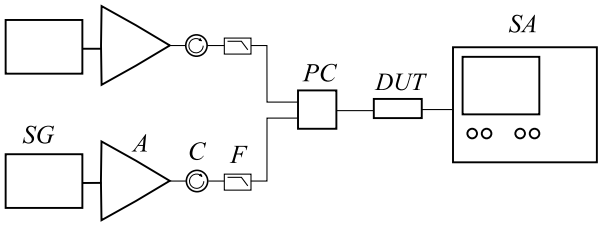


FIGURE 7.2: The top and bottom views of the used PCB.

ground plane using large capacitors. The four lines converge in the centre pad where the chip is placed and connected via bondwires. On the same pad, single layer bondwireable capacitors are used to provide a very short path to ground to the leaking RF signals.

7.2 Measurements Setup

The first setup used to measure the performance of the prototyped chip consists of an active source and load-pull system, shown in the picture below. The possibility of performing source and load-pull is very useful to see how and how much these impedances influence the linearization technique and the MPA performance. Since the load-pull system is made to measure high levels of power, another setup had to be used to check the circuit linearity level in the low input power range, and characterize the OIP3 figure of the amplifiers. Figure 7.3 depicts a block diagram of this second setup. It consists of



SG : Signal Generator - A : Amplifier - C: Circulator
F: Filter - PC: Power Combiner
DUT: Device Under Test - SA : Spectrum Analyzer

FIGURE 7.3: A block diagram representation of the setup used to measure low power points.

a simple two-tone signal source, which is connected to the input of the amplifier. The output is then measured using a Spectrum Analyzer.

7.3 Measurements Results

In this section, the results of the measurements performed on the test chip are reported. Initially, the results of single tone and S-parameters measurements are presented. From these results we can see and compare the gain and output power capability performance of the two designed amplifiers. Next, we report the linearity parameters obtained by performing 2-tone measurements. For the DS based and the reference amplifiers we show the results obtained biasing them at the optimum point for linearity. For this reason, the collector quiescent currents have slightly different values, but the IP3 levels can still be fairly compared.

7.3.1 Single-Tone and S-Parameters

In this paragraph, Single-Tone and S-parameters measurements performed on the test chips are presented. First the results of a single-tone load-pull measurement on the DS amplifier are shown. Next, using the same load condition we compare the DS and the Reference amplifiers single-tone performance to see if the linearity comparison of these circuits in terms of OIP3 levels is fair. Eventually, the measured S_{21} parameter for the DS chip is plotted, to check whether the resonance of the LC-circuit occurs at the expected frequency.

Here we show the results of the load-pull measurement on the DS amplifier. The used parameters are listed in table 7.1. Figure 7.4 shows the fundamental output power, the Power Gain and the PAE for the DS chip, for different values of the load impedance. In the performed load-pull measurements, the load impedance conditions reported in the

f_0	2	GHz
V_c	4	V
R_S	50	Ω

TABLE 7.1: Parameters used for the single-tone measurement

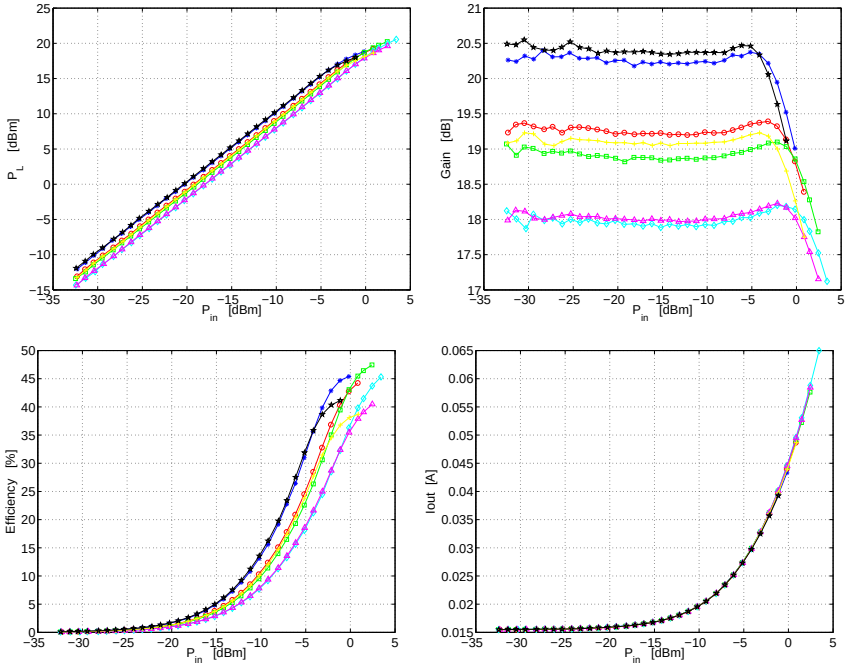


FIGURE 7.4: The performance resulting from a load-pull on a single-tone measurement of the DS chip.

Smith chart of figure 7.5 have been utilized. For this amplifier, the load which gives

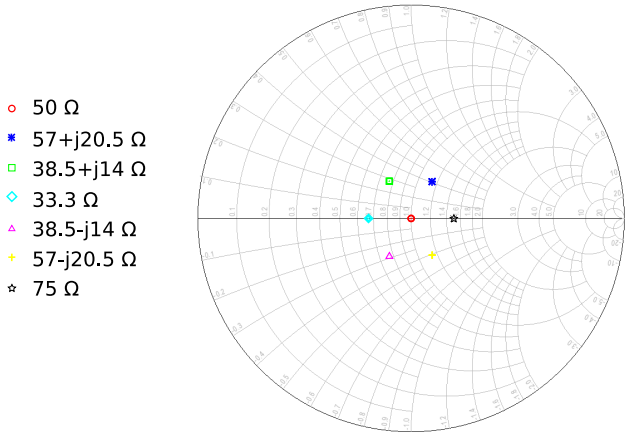


FIGURE 7.5: The values of the load impedance used for the single-tone load-pull measurement

the highest output P_{1dB} is $Z_L = 33.3\ \Omega$, the one that results in the highest Power Gain is $Z_L = 75\ \Omega$ and the one for maximum peak efficieny is $Z_L = 38.5 + j14\ \Omega$.

Now we set the load impedance to 50Ω and compare the results obtained from single-tone measurements of the DS and the Reference circuits. Figure 7.6 plots the output

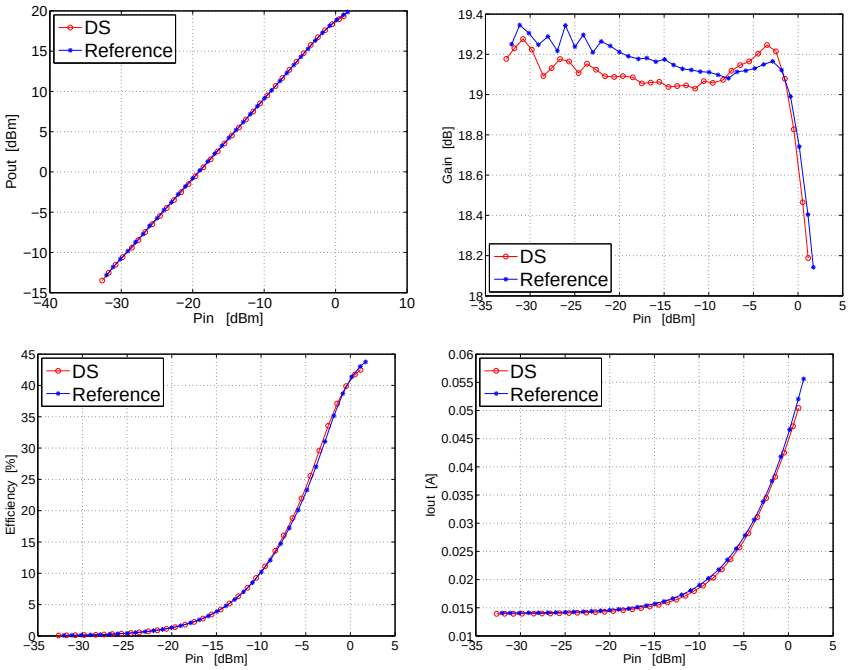


FIGURE 7.6: Comparison between the performance of DS and the Reference chips, obtained through single-tone measurement.

fundamental power, power gain, efficiency and DC output current for the amplifiers in exam. We observe that the linear gain of the Reference is slightly higher than the one of the DS amplifier. Moreover, we can see from the gain shape that the Reference is biased closer to a class A operation. This is explained by observing that the two amplifiers have the same quiescent current, while, as mentioned in Chapter 6, the reference chip has a total emitter area that is 3/4 of the DS one. As expected from simulations, all the

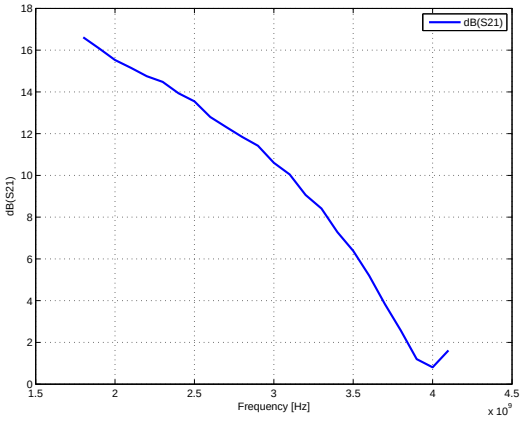


FIGURE 7.7: The S_{21} parameter plotted in dB over frequency for the DS chip version.

single-tone performance are very similar, including the P_{1dB} and the quiescent collector

current. Thus, in the next paragraph, we can fairly compare the IP3 linearity figure of the DS and reference amplifiers, obtained through two-tone measurements. Finally, we plot the S_{21} parameter for the DS amplifier in figure 7.7. These results are obtained biasing the amplifier at a slightly lower quiescent current $I_{cq} = 12.7\ mA$. It can be seen that the resonance occurs at the nominal design frequency of $2f_c = 4$ GHz. Therefore, we will assume that two-tone measurements performed at 2 GHz benefit from the effect of the 2nd harmonic short. In theory, for a correct operation of the linearization technique, also the output termination must be shorted at BB and 2nd harmonic band. For these measurements, no actions were taken to control the load impedance in these frequency bands. The value of the load impedance is thus approximately 50Ω at 2nd harmonic while for BB it is not well defined, as it is offered by the output biasing current loop.

7.3.2 Two-Tone Measurements

In this paragraph, two-tone measurements results are reported and discussed. These measurements have been performed using the active load-pull system for higher power level, and the Spectrum Analyser setup to measure lower power levels for the IM3 components. The source impedance, load impedance carrier frequency and modulation

f_0	2	GHz
Δf	10	MHz
V_c	4	V
R_S	50	Ω
R_L	50	Ω

TABLE 7.2: Parameters used for the single-tone measurement

frequency are listed in table 7.2. To start, we look for the best biasing point for linearity at low back-off power. Figure 7.8 shows the IM3 ouptut power versus the fundamental

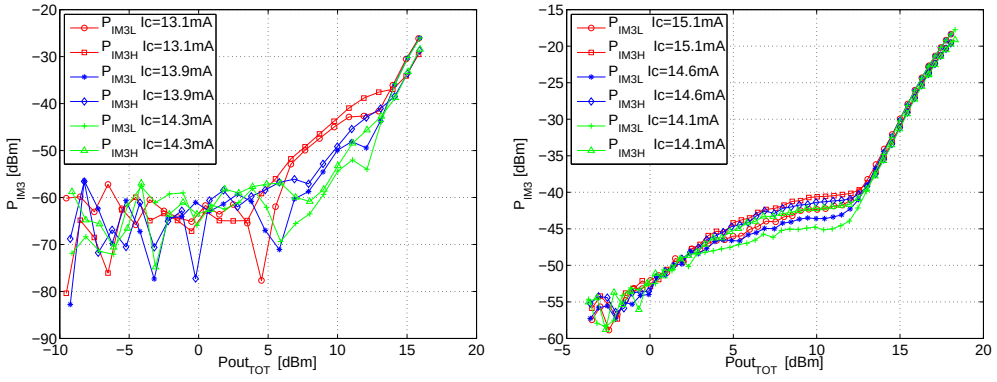


FIGURE 7.8: The IM3 output power plotted versus the total fundamental output power for different levels of biasing of the DS and the Reference chips.

output power for the DS and the Reference chip versions. For these figures, only the

measured point for an output power $P_{out} > 0dBm$ can be considered valid, as for lower power level the measured points correspond to the noise floor of the system. It is possible to notice that, for the DS amplifier, the high power linearity increases with the quiescent current. Instead, for the Reference, a slight improvement of the high power linearity can be seen as the quiescent current is decreased. Following this observation, we bias the two amplifiers at their optimum point for linearity at low back-off power, to compare the obtained performance. For the DS amplifier this occurs at a quiescent current $I_{cq,DS} = 14.7$ mA, while for the reference at $I_{cq,Ref} = 13.7$ mA. We plot in figure 7.9 the IM3 power for the two chips in exam. Also in this case, especially for the

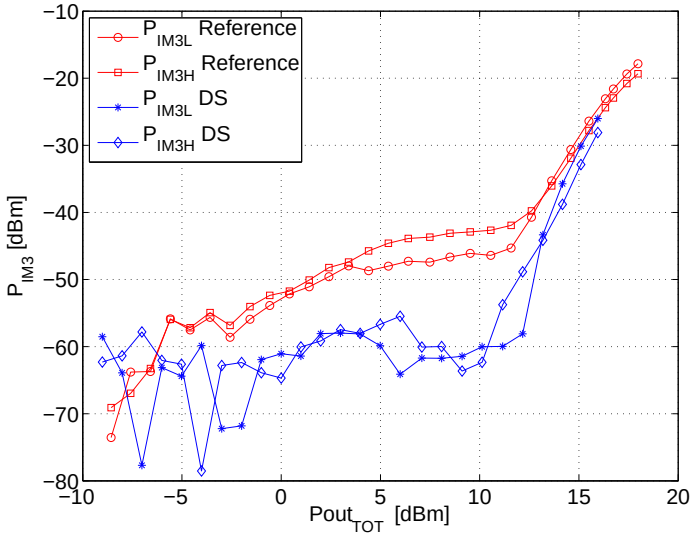


FIGURE 7.9: The comparison of the output low and high IM3 power plotted versus total fundamental output power for the DS and the Reference chips.

DS chip, only the points taken at a total output power above 0 dBm are valid, as the noise floor of the system limits lower power measurements. It can be seen that the DS amplifier shows a lower amount of IM3 distortion than the Reference for the same level of fundamental output power up to 15 dBm, which corresponds to 4 dB back-off from the P_{1dB}.

7.3.3 Measurement vs Simulation Comparison

Here we compare the best measured performance with the best results achieved in simulation for the DS based amplifier. These performance are obtained at slightly different biasing points. The reason of this deviation can be attributed to various causes, and is of difficult identification. Most probably, the motivation is a combination of unaccounted layout parasitic effects and PVT variations. We first compare the performance of the amplifier when this is excited by a single frequency tone. Table 7.3 shows the utilized parameters for both single tone simulation and measurement. From figure 7.10 we can

f_0	2	GHz
R_S	50	Ω
R_L	50	Ω

TABLE 7.3: Parameters used for the single-tone simulation and measurement.

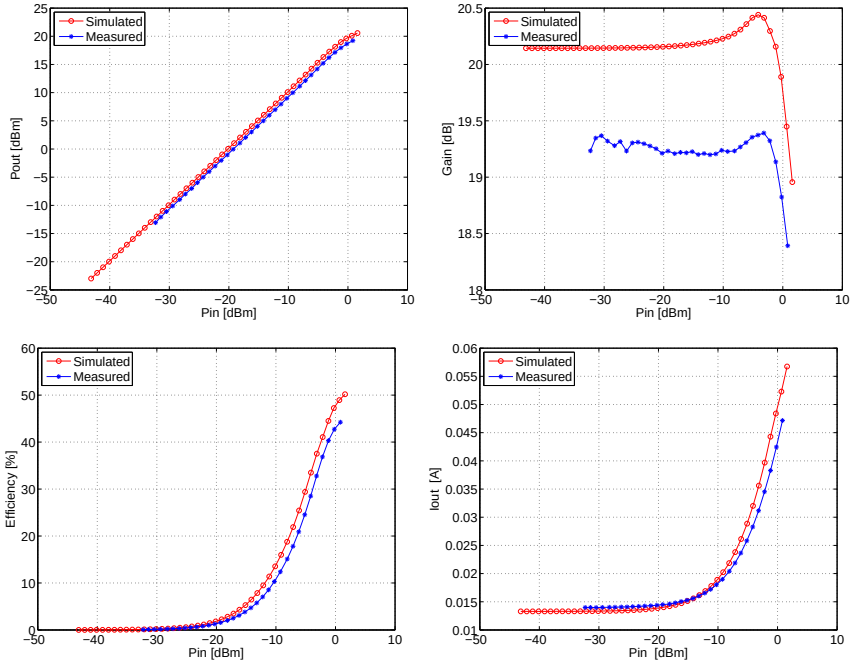


FIGURE 7.10: Comparison of the best measured and best simulated single-tone performance for the DS amplifier.

make an observation: even though the collector quiescent current of the measured chip is higher, its power gain is about 1 dB smaller than the simulated one. This discrepancy is probably caused by additional losses in the actual circuit. We then use a two-tone excitation to see the amount of the output power at the IM3 frequencies, for different levels of input power. Both the simulation and the measurements have been performed with the parameters listed in table 7.4. In this conditions, the simulated and measured

f_c	2	GHz
Δf	10	MHz
R_S	50	Ω
R_L	50	Ω

TABLE 7.4: List of parameters used for the measurement

IM3 power has the behavior shown in figure 7.11: In this figure, we can notice a good agreement between the measured and simulated points in the output power range from 5 to 10 dBm. For lower output power, the measured points are limited by the level of the noise floor of the system. For output power higher than 10 dB, the discrepancy between

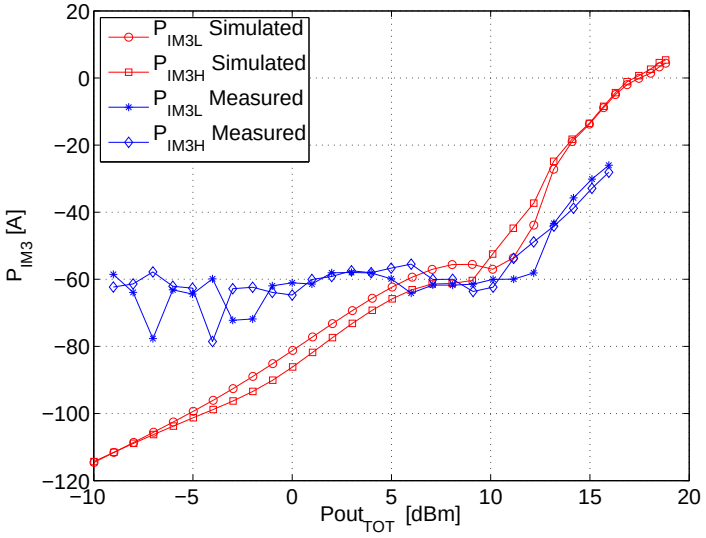


FIGURE 7.11: Comparison between the measured and simulated IM3 output power components for the DS based amplifier with conventional ground configuration

the simulated and the measured points can be due to the limited order of mixing included in the simulation algorithm. Now we compare the low-power measurements with the same simulation. Also in this case we tune the biasing of the amplifier to reach the optimum point for low-power linearity. This is achieved for the DS amplifier at a quies-

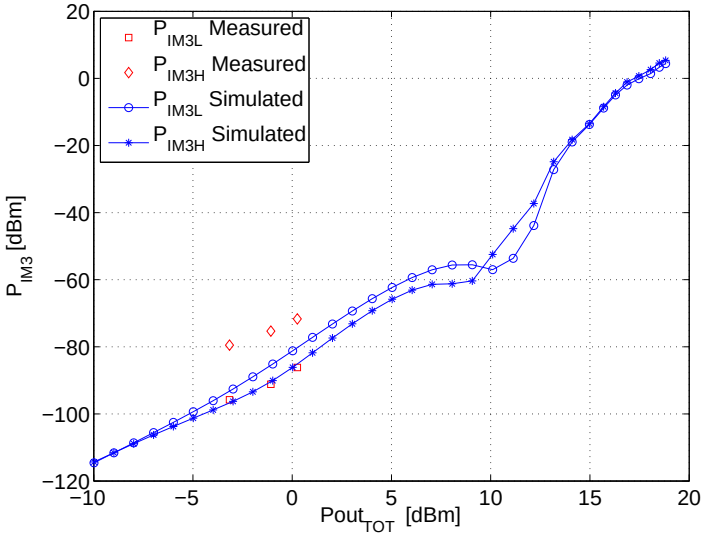


FIGURE 7.12: The measured and simulated IM3 power versus output power for the DS chip version.

cent current of $I_{cq} = 12.2$ mA. from figure 7.12 we can observe that the measured points of the IM3L output power are in line with the simulated ones, while the IM3H power is almost 20 dB higher. This asymmetry between the low and high IM3 is probably caused by an uneven contribution of the BB terminations to the overall IM3 distortion. In this case, the BB impedance offered at the input of the amplifier is controlled by means of

the biasing circuit, while the output BB impedance is provided by the series connection of the bias-T and the V_{CC} supply, and is therefore not well defined. This latter condition at the amplifier output is believed to be the reason for the large IM3 asymmetry.

7.4 Conclusions

From the results of the measurement performed on the test chips we can derive several conclusions, which are here reported. We summarize the performance of the designed and implemented chips in table 7.5. From these results we can conclude that the amount

Performance	**DS MPA**	**Ref MPA**	**Unit**
$DCPowerBudget$	14.7@4	13.7@4	mA@V
P_{1dB}	19.2	19.6	dBm
$IM3_{@BO10dB}$(L/H)	69.7/68	56/52	dBc
$IM3_{@BO20dB}$(L/H)	87/72	-	dBc
$Gain_P$	19.2	19.6	dB
$Eff_{@P1dB}$	44	43	%

TABLE 7.5: Comparison between the simulated performance of the DS-based and the Reference Out-of-band based amplifiers.

of IM3 distortion at a level of back-off power of 10 dB for the DS based MPA is about 15 dB lower than for the Reference MPA. At 20 dB of back-off power, only measurements of the DS MPA were taken, and they show a large asymmetry between the low and the high IM3 components.

7.5 Future Work

The asymmetry in the power level of the low and high IM3 components finds a possible explanation in the baseband modulation of the input and/or output ports of the amplifier. This phenomenon results from an incorrect decoupling of the input or output nodes at the BB frequencies. In order to solve this problem, a new PCB is currently being designed, which can provide BB and second harmonic short condition at the output of the amplifier by means of shunt stubs.

Chapter 8

Conclusions and Recommendations

In this chapter we report the conclusions that have been achieved at the end of this thesis project. First we briefly summarize the content of the report. Next, for each of the investigated linearization techniques we report the main advantages and drawbacks, and give recommendations for future work to be carried out on the topics treated in this report.

As mentioned in the introduction, this project aims to fill the gap in the linearity performance of GaAs and SiGe HBT based RF amplifiers by making use of existing or developing new linearization techniques. In particular, the limitations of the Out-of-Band emitter–tuning method for IM3 cancellation has been used as reference from which the search for a new solution has started. In this thesis work, the following techniques to improve the OIP3 figure of bipolar amplifiers have been investigated and presented:

- **Power Scaling of Out-of-Band Matched Amplifiers**
- **Out-of-Band Active Injection Compensation**
- **Bipolar Derivative Superposition**

In the following sections we summarize their most important advantages and drawbacks, and some suggestions are given on the topics to be further investigated.

8.1 Power Scaling Technique

The power scaling is a straightforward method to achieve high values for the OIP3 figure and, in principle, it can always be applied. The main disadvantage consists of the very small value obtained in this way for the degeneration resistor, which for an emitter compensated design is $R_e = \frac{V_T}{2I_c}$. Above a certain scaling factor m, the value of this component is overwhelmed by the internal emitter series resistance and inductance of the device, limiting the achievable OIP3. Other disadvantages are also related to the minimum resistance that several components are able to offer: the limited Q factor of the LC-resonator and the impedance transformation ratio required to power match the input and output ports are the most relevant of these limitations.

The power scaling technique was judged to be too limited at the beginning of this thesis work for the targeted output power levels due to the severe limitations it encounters when the scaling factor becomes too large. However, this technique can be used in combination with other linearization techniques, as it does not change the operation of the amplifier, when low values of the scaling factor are used.

8.2 Out-of-Band Active Injection Compensation

This linearization technique has the main advantage of providing a compensation for any sort of deviation from the optimum out-of-band matching operating point. We have seen that a symmetric compensation for the low and high IM3 components can only be obtained by injecting the low and high side second harmonic frequencies. Using this method, the in-band characteristics of the amplifier can be fully exploited to achieve high performance such as gain and efficiency, while the active injection is then used to restore the condition for out-of-band IM3 cancellation. The main drawback of the IM2 injection technique is the need to know in advance and with precision how should the compensation signal look like to restore the out-of-band matching conditions.

The problem introduced by this requisite can be solved in two ways: one is to actually introduce the compensation at a post-fabrication stage. In this way, after the chip is tested, the compensation signal can be tuned until the correct values are found. A second option is to make use of a feedback mechanism, which has to adjust the compensation signal according to the amount of IM3 distortion in the output spectrum. The feedback method to sense the output distortion and consequently adjust the signal to be injected represents the most promising method for the effectiveness of this linearization technique.

8.3 Derivative Superposition

The Derivative Superposition method has several advantages, when compared to the conventional Out-of-Band linearization. The most important are the robustness of the OIP3 level over changes of the biasing current and of the input power level. As the simulation results of Chapter 6 showed the DS technique provides a range of biasing for which the output IM3 current is nearly cancelled. Another advantage consists of the larger freedom in the choice of the design variables. It was said in Chapter 5 that an optimum relation exists between the size of the transistors used, the degeneration resistance and the forward transit time. Nevertheless, when this is not or only closely satisfied, a cancellation can still be achieved by shifting the phase of one of the devices. This was done for example by means of a capacitor in parallel to the degeneration resistor in the design of the DS MPA in Chapter 6. As the DS technique functionality is hampered by out-of-band mixing, it needs the amplifier driving nodes to be shorted at the IM2 frequency bands. This requirement, although simple in theory, can be difficult to achieve in practical circuit implementations. In table 8.1 the performance achieved with the designed MPA making use of the DS technique are compared to the project specifications. The first important difference that we can notice in this comparison is

Performance	**Specifications**	**DS MPA**	**Unit**
$DCPowerBudget$	90@5	14.7@4	mA@V
P_{1dB}	27.0	19.2	dBm
$OIP3$(L/H)	45/45	38/33[a]	dBm
$Gain_T$	18 to 20	17.5	dB
$Eff_{@P1dB}$	-	44	%
S_{11}	-10	-	dB
S_{22}	-10	-	dB

TABLE 8.1: Comparison of the performance achieveed with the designed test chip using Derivative Superposition with the original project specifications.

[a]The OIP3 for the DS MPA has been calculated using the low power IM3 measured points

in the DC power budget. This gap exists because the designed MPA consists of a unit-cell circuit, to be scaled 6 times in order to achieve the wanted level of output power. However, several problems have been encountered with the high power version, the most important one being the difficulty of scaling down the impedances provided at BB and 2^{nd}-harmonic at the input of the amplifier.

The main goal of future investigation on the application of the DS linearization technique to Bipolar power amplifiers, should be the design of a scaled version of the amplifier, which can satisfy the high output power specification. In order to accomplish this,

the first problem to solve is represented by lowering the finite impedance offered by the BB and 2nd harmonics input current loops. The requirement on the BB input impedance has been achieved in this work by means of on-chip biasing circuitry. The offered impedance can be in general lowered by placing several of these biasing blocks in parallel. However, this improvement goes at the expense of a larger dissipated DC Power. For what concerns the CB stage, another design possibility consists of using two parallel cascode configurations for the two CE branches, in order to present a proportionally scaled load condition to the CE devices. This option, described already in Chapter 6, was discarded for the different additional phase shift in the IM3 collector currents introduced by the two CB stages, which yielded a misalignment of the IM3 current phases, and therefore degraded the cancellation. Because of time limitations, this alternative was not further investigated, but it represents a point to be studied in future works. For what concerns the design of the active devices in the utilized QUBiC technology, a suggestion is given on the evaluation of the base-emitter junction capacitance. The condition derived in Chapter 5 for the alignment of the IM3 collector current phase wants that $R_e = \frac{\tau_f}{C_{je}}$. When C_{je} is too large, a very small value of R_e has to be used which is not preferable for several reasons, the most important one being the very large value of g_m needed to satisfy the ohmic condition, which leads to unpractical values of the collector current density. Therefore the research for new active devices should be oriented towards the reduction of the base-emitter junction capacitance C_{je}. To conclude, the influence of the base-collector capacitance C_{bc} on the operation of this linearization technique, and in general on the overall amplifier IM3 distortion, needs to be analysed and evaluated. This work is currently in progress within a project of the RF group in TU Delft and might result in very interesting combinations with the work presented in this thesis report.

Appendix A

Out-of-Band Base-Emitter Voltage Conditions

In this appendix we derive the condition for the in-band and out-of-band emitter voltages reported in Chapter 4, to achieve the IM3 collector current cancellation. To find this condition, we can again consider the equation:

$$\begin{aligned} & i_{c,NL3} = \\ & K_{3gm} v_{be}(s_{1,2}) v_{be}(s_{1,2}) v_{be}(-s_{2,1}) + \\ & + \frac{2}{3} K_{2gm} \left[2 v_{be2}(s_{1,2} - s_{2,1}) v_{be}(s_{1,2}) + v_{be2}(2s_{1,2}) v_{be}(-s_{2,1}) \right] = 0 \end{aligned} \tag{A.1}$$

Expressing the voltages in the complex notation $v_{be}(j\omega) = |v_{be}(j\omega)| \, e^{j(\phi)}$, and using that $\phi_{s_{1,2}} = \phi\{v_{be}(s_{1,2})\}$ and $\phi_{2s_{1,2}} = \phi\{v_{be}(2s_{1,2})\}$, we can write :

$$\begin{aligned} 0 = & K_{3gm} \left| v_{be}(s_{1,2}) \right|^2 \left| v_{be}(-s_{2,1}) \right| e^{j(2\phi_{s_{1,2}} - \phi_{-s_{2,1}})} + \\ & + \frac{2}{3} K_{2gm} \left[2 \left| v_{be2}(s_{1,2} - s_{2,1}) \right| \left| v_{be}(s_{1,2}) \right| e^{j(\phi_{s_{1,2}} + \pi)} \right] \\ & + \frac{2}{3} K_{2gm} \left[\left| v_{be2}(2s_{1,2}) \right| \left| v_{be}(-s_{2,1}) \right| e^{j(\phi_{2s_{1,2}} + \phi_{-s_{2,1}})} \right] \end{aligned} \tag{A.2}$$

Making use of the assumptions

$$\phi_{s_{1,2}} = -\phi_{-s_{1,2}} \tag{A.3}$$

$$|v_{be}(\pm s_1)| = |v_{be}(\pm s_2)| \tag{A.4}$$

$$\phi_{s_{1,2} - s_{2,1}} \simeq \pi \tag{A.5}$$

We can rearrange eq A.2 as:

$$\begin{aligned} 0 = {} & K_{3gm} \left|v_{be}(s_{1,2})\right|^2 e^{j(\phi_{s_{1,2}})} + \\ & + \frac{2}{3} K_{2gm} \left[2 \left|v_{be2}(s_{1,2} - s_{2,1})\right| e^{j(\phi_{s_{1,2}} + \pi)}\right] \\ & + \frac{2}{3} K_{2gm} \left[\left|v_{be2}(2s_{1,2})\right| e^{j(\phi_{2s_{1,2}} - \phi_{s_{2,1}})}\right] \end{aligned} \tag{A.6}$$

Since the first and the second term of the right hand part of the equation are opposite in phase, the only way for the total sum to be equal to zero is that the last term is in-phase or out-of-phase with the first one, depending on the magnitude ratio of the first two terms. Introducing for convenience the notations: $v_{be_{f0}} = v_{be}(s_{1,2})$, $v_{be_{BB}} = v_{be}(s_{1,2} - s_{2,1})$ and $v_{be_{2F}} = v_{be}(2s_{1,2})$, we write this condition in formulas:

$$\phi_{2s_{1,2}} = \begin{cases} 2\phi_{s_{1,2}} + \pi, & \text{if } K_{3g_m} \left|v_{be_{f0}}\right|^2 > \frac{2}{3} K_{2gm}(2 \left|v_{be2_{BB}}\right|) \\ 2\phi_{s_{1,2}}, & \text{if } K_{3g_m} \left|v_{be_{f0}}\right|^2 < \frac{2}{3} K_{2gm}(2 \left|v_{be2_{BB}}\right|) \end{cases} \tag{A.7}$$

In this demonstration we consider to be the first of the two inequalities to be satisfied. When this is true, to set the total nonlinear current equal to zero the following conditions have to be satisfied:

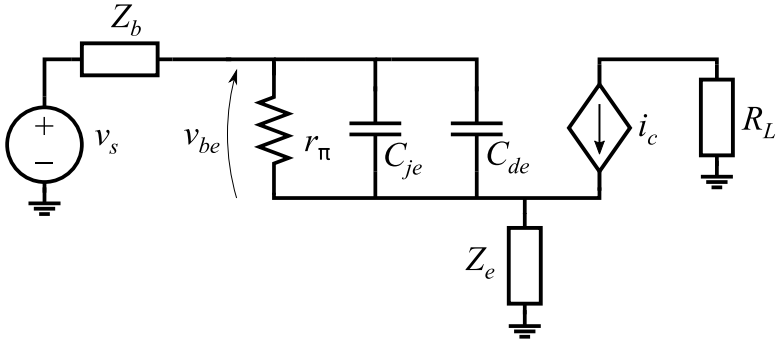
$$\phi_{2s_{1,2}} = 2\phi_{s_{1,2}} + \pi \tag{A.8}$$

$$\frac{|v_{be,f0}|^2}{|v_{be,BB}| + |v_{be,2F}|} = \frac{2}{3} \frac{K_{2g_m}}{K_{3g_m}} = V_T \tag{A.9}$$

Appendix B

Out-of-Band Signal Injection Calculation

In this appendix the derivation of the signal magnitude and phase for the out-of-band signal injection compensation is reported. We start considering the circuit below:



For this circuit we can write the cancellation condition $i_{c,NL3} = 0$ as:

$$K_{3gm} v_{be}(s_a) v_{be}(s_b) v_{be}(s_c) = -\frac{2}{3} K_{2gm} \left[v_{be2}(s_a, s_b) v_{be}(s_c) + v_{be2}(s_a, s_c) v_{be}(s_b) + v_{be2}(s_b, s_c) v_{be}(s_a) \right] \tag{B.1}$$

In this derivation, the fundamental terms are fixed, and we want to use the second order terms $v_{be}(s_i, s_j)$ to satisfy the equality.

B.1 Baseband Injection

For the injection of the BB signal, we isolate the baseband term of equation B.1, obtaining :

$$\begin{aligned} v_{be}(s_1,-s_2) &= -\frac{1}{2}v_{be}(s_1,s_1)\frac{v_{be}(-s_2)}{v_{be}(s_1)} - \frac{3}{4}\frac{K_{3g_m}}{K_{2g_m}}v_{be}(s_1)v_{be}(-s_2) \\ &= \frac{1}{2}i_{NL2}B(2s_1)\frac{v_{be}(-s_2)}{v_{be}(s_1)} - \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}}v_{be}(s_1)v_{be}(-s_2) \\ &= \frac{1}{2}K_{2g_m}v_{be}(s_1)v_{be}(-s_2)B(s_1-s_2) - \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}}v_{be}(s_1)v_{be}(-s_2) \end{aligned} \tag{B.2}$$

The baseband base-emitter voltage component $v_{be}(s_1,-s_2)$ can be expressed as a sum of the internally generated nonlinear current i_{NL2} and the injected current i_{inj} as:

$$v_{be}(s_1,-s_2) = -i_{NL2}B(s_1-s_2) - i_{inj}H_{inj}(s_1-s_2) \tag{B.3}$$

where $H_{inj}(s)$ is the transfer function from the injected current to the base-emitter voltage. In the case that the current is injected in the emitter node, than $H_{inj}(s) = B(s)$ and the expression of the current to be injected for the compensation of the IM3L component becomes:

$$i_{inj,BB} = v_{be}(s_1)v_{be}(-s_2)K_{2g_m}\left[\frac{3}{4}\frac{K_{3g_m}}{K_{2g_m}^2}\frac{1}{B(s_1-s_2)} - \frac{1}{2}\frac{B(2s_1)}{B(s_1-s_2)} - 1\right] \tag{B.4}$$

With the same procedure we can derive the expression of the current to be injected for the compensation of the IM3H component:

$$i_{inj,BB} = v_{be}(s_2)v_{be}(-s_1)K_{2g_m}\left[\frac{3}{4}\frac{K_{3g_m}}{K_{2g_m}^2}\frac{1}{B(s_2-s_1)} - \frac{1}{2}\frac{B(2s_2)}{B(s_2-s_1)} - 1\right] \tag{B.5}$$

Equations B.4 and B.5 have in general different values. In particular, the magnitude of the injected current is the same, while its phase is opposite. For this reason it is not possible to simultaneously compensate the IM3 low and high components through baseband signal injection.

B.2 2nd Harmonic Injection

For the injection of the 2nd Harmonic signal, we isolate the second harmonic term of equation B.1, obtaining :

$$\begin{aligned} v_{be}(s_1, s_1) &= -2v_{be}(s_1, -s_2)\frac{v_{be}(s_1)}{v_{be}(-s_2)} - \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}}v_{be}^2(s_1) \\ &= 2i_{NL2}B(s_1 - s_2)\frac{v_{be}(s_1)}{v_{be}(-s_2)} - \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}}v_{be}^2(s_1) \\ &= 2K_{2g_m}v_{be}^2(s_1)B(s_1 - s_2) - \frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}}v_{be}^2(s_1) \end{aligned} \tag{B.6}$$

The second harmonic base-emitter voltage component $v_{be}(s_1, s_1)$ can be expressed as a sum of the internally generated nonlinear current i_{NL2} and the injected current i_{inj} as:

$$v_{be}(s_1, s_1) = -i_{NL2}B(2s_1) - i_{inj}H_{inj}(2s_1) \tag{B.7}$$

where $H_{inj}(s)$ is the transfer function from the injected current to the base-emitter voltage. In the case that the current is injected in the emitter node, than $H_{inj}(s) = B(s)$ and the expression of the injected current becomes:

$$i_{inj,2f_{01}} = v_{be}^2(s_1)K_{2g_m}\left[\frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}^2}\frac{1}{B(2s_1)} - 2\frac{B(s_1 - s_2)}{B(2s_1)} - 1\right] \tag{B.8}$$

With the same procedure we can derive the expression of the current to be injected at the frequency $2f_{02}$:

$$i_{inj,2f_{02}} = v_{be}^2(s_2)K_{2g_m}\left[\frac{3}{2}\frac{K_{3g_m}}{K_{2g_m}^2}\frac{1}{B(2s_2)} - 2\frac{B(s_2 - s_1)}{B(2s_2)} - 1\right] \tag{B.9}$$

In general, the terms $B(s_2 - s_1)$ and $B(s_1 - s_2)$ give opposite phase contribution. For this reason we have to allow the injection of two different signals at the frequencies $2f_{01}$ and $2f_{02}$ in order to be able to independently compensate the IM3 low and high side components.

Appendix C

Chip Layouts

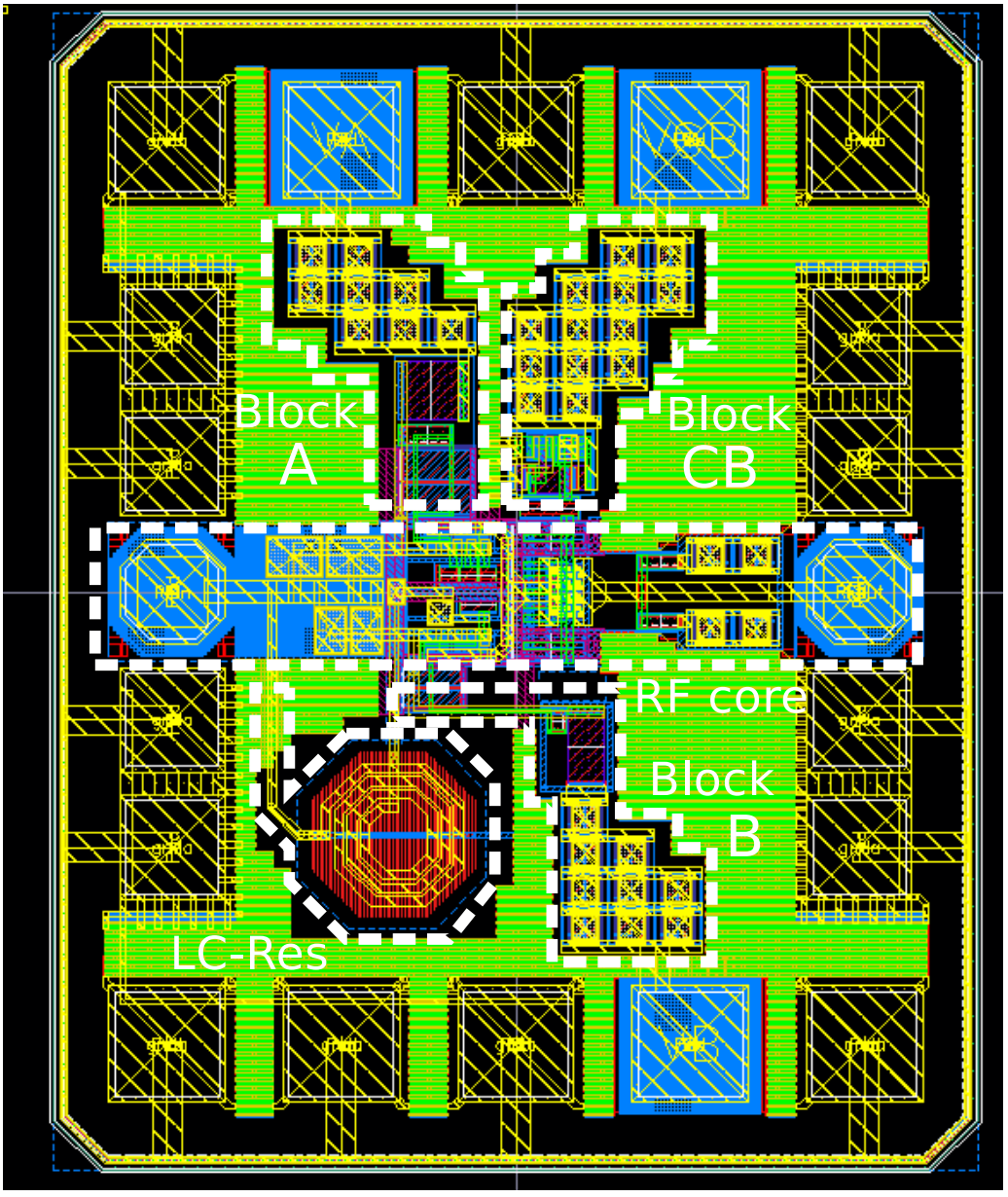


FIGURE C.1: Layout of the DS MPA chip with conventional ground configuration

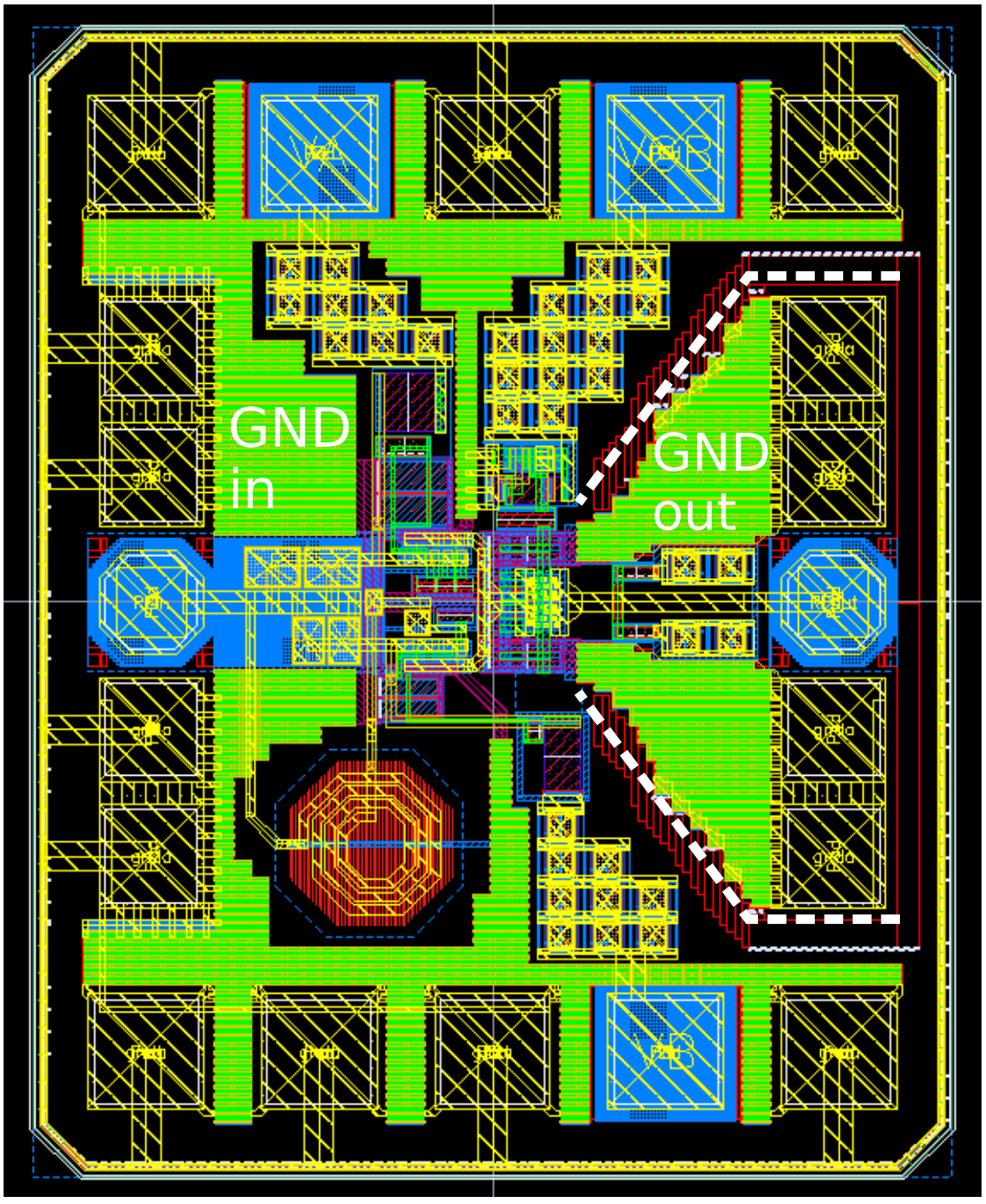


FIGURE C.2: Layout of the DS MPA chip with star ground configuration

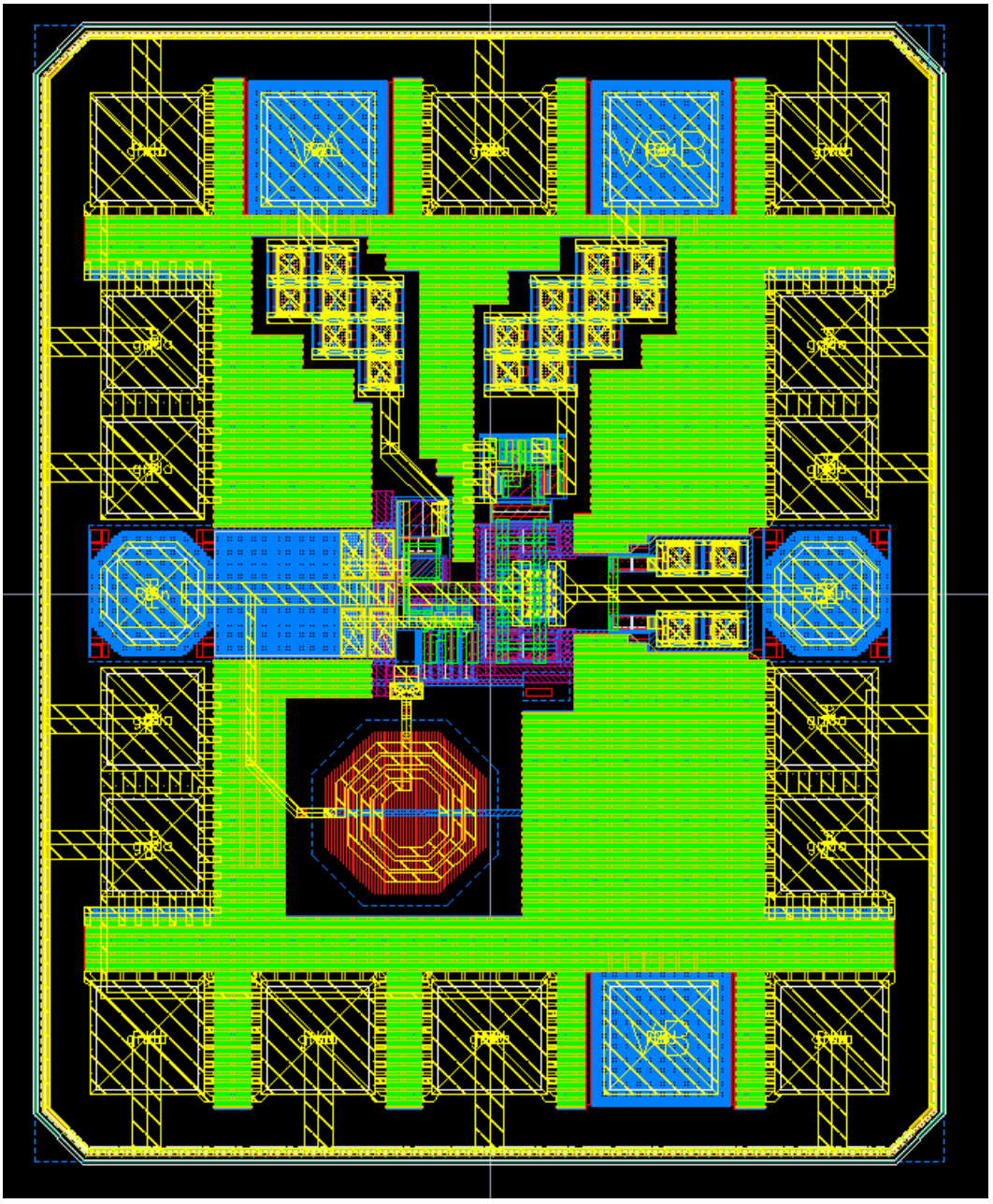


FIGURE C.3: Layout of the Reference MPA chip with conventional ground configuration

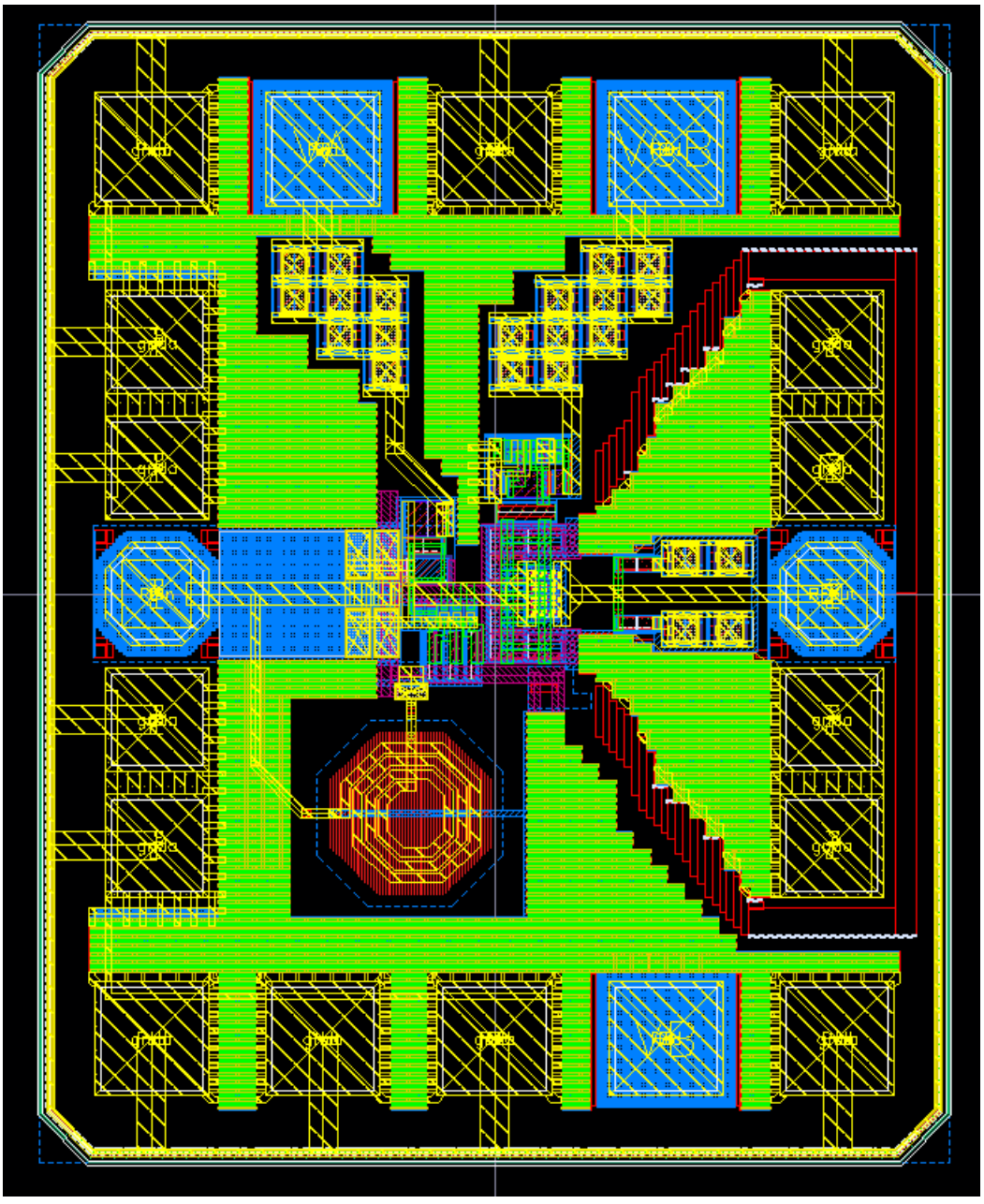


FIGURE C.4: Layout of the Reference MPA chip with star ground configuration

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