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Single-Switch Soft-Switched High Voltage Gain Converter With Low Voltage Stress and Continuous Input Current

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ABSTRACT This paper introduces a soft-switched high step-up converter applicable to photovoltaic systems. In the proposed topology, to further improve the voltage gain and reduce the components voltage stress, coupled inductors and voltage multiplier cell (VMC) techniques are integrated with the conventional boost converter. Hence, it addresses challenges in traditional boost converter when operating at near unity duty cycle and enables it to utilize high-quality components that lead to decreased conduction losses in high-output voltage applications. Furthermore, the converter achieves soft switching operation by incorporating a lossless snubber cell, which consists of just two diodes and requires no additional switches and magnetic cores. These features contribute to enhancing the converter efficiency. Notably, the energy stored in the snubber circuit is effectively recovered to the output without any circulating current, making it a beneficial characteristic among the lossless snubber structures. The proposed topology also offers a common ground between the input and output terminals, as well as the switch which simplifies the converter control circuit. Additionally, it maintains continuous input current, which makes the proposed converter more suitable for photovoltaic system applications. To validate the converter benefits, a 150 W laboratory prototype converter is implemented.

INDEX TERMS High gain converter, low voltage stress, soft-switching, single switch, continuous input current.

I. INTRODUCTION

Nowadays, renewable energy sources (RESs) like fuel cells and photovoltaic (PV) panels have captured significant attention. This heightened interest stems from their potential to reduce reliance on finite fossil fuels, which are a leading contributor to environmental issues like global warming and air pollution [1], [2]. Among RESs, photovoltaic systems are embraced due to the abundant availability of solar radiation and the straightforward installation process for PV panels. However, PV panels typically generate low output voltages; consequently, there is a pressing need to employ high-efficiency DC-DC voltage-boosting converters to supply grid-connected inverters in these systems. Moreover, ensuring a continuous input current can significantly enhance the performance of these systems [3]. The conventional boost topology is a viable candidate for these applications, mainly because of its straightforward structure and control circuit and its ability to maintain a continuous input current [4], [5]. However, when a substantial voltage gain is required, the boost duty cycle (D) approaches unity, which increases conduction losses and decreases overall efficiency. Additionally, the boost converter suffers from hard switching operation and high voltage stress on its semiconductor components [6].

Incorporating switched capacitor/inductor (SC/SI) units [7], voltage multiplier cells (VMC), and coupled inductors (CIs) techniques [8] in the conventional boost topology are common strategies for increasing the boost converter voltage gain, addressing issues related to approaching near-unity duty cycle, and reducing voltage stress on semiconductor

components [9]. The voltage gain of CIs-based converters depends on the CIs turns ratio and duty cycle. However, they often suffer from high voltage spikes across the switch because of the stored energy in the CIs leakage inductance. Additionally, the input current in these converters commonly exhibits discontinuous behavior due to the series connection of the CIs with the input source. Consequently, to resolve these problems, it is necessary to incorporate an input filter and a clamp circuit. Integrating SC and VMC methods involves adding a significant number of components, resulting in higher conduction losses and increased cost which degrade the power density [9], [10].

Achieving soft-switching conditions at Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS), is crucial for minimizing switching losses in high-frequency applications to improve efficiency [11], [12], [13], [14], [15], [16], [17], [18]. Additionally, the increased switching frequency leads to passive components size reduction, thereby enhancing power density. Popular strategies for establishing soft-switching conditions involve the utilization of active clamp units [11], [12], Zero Voltage Transient (ZVT) and Zero Current Transient (ZCT) cells, along with lossless snubber circuits [13], [14]. ZVT and ZCT cells, as well as active clamp circuits utilize an auxiliary switch which complicates the converter structure since each switch contains a driver and control circuit. Among the mentioned soft-switching techniques, passive lossless snubber circuits are very attractive due to their simple structure and not requiring extra switch. However, this technique is usually unable to eliminate the switch capacitive turn on loss.

Voltage-boosting methods and soft-switching approaches are combined at various studies to tackle the challenges faced by boost topology in high voltage gain applications. When integrating different techniques, minimizing the number of switches and magnetic cores is very important to reduce control circuit complexity and enhance power density [11], [12], [13], [14], [15], [16], [17], [18]. In [11], an active clamp circuit is integrated with CIs, and in [12], it is integrated with SC, resulting in the proposal of two soft-switched high step-up converters. The voltage stress on the semiconductor devices in these converters is a fraction of the output voltage. However, both converters employ two switches, complicating their structure, and fully soft-switching conditions are not provided in [11]. A VMC is incorporated into a two-phase CIs-based boost topology, resulting in the proposal of a high step-up topology in [14]. However, this topology establishes only ZCS turn on condition for switches while turn off switching loss is maintained and the use of two switches adds to the converter complexity. Another high step-up topology is developed in [14], and then a lossless snubber circuit is applied to the converter, featuring ZVS turn-off for the switches. Nevertheless, the second version involves a high number of components, including two switches, eight diodes, and two CIs, leading to a degradation in power density and increases the complexity.

Soft-switching conditions in the converters presented in [11], [12], [13] are achieved through the use of an auxiliary switch, and the topology in [14] employs two main switches. Utilizing more than one switch increases structural complexity due to the additional gate drive and control circuits required for each switch. In contrast, the converters in [15], [16], [17], [18] incorporate only a single switch in their structures, achieving soft-switching without adding any extra switches, thereby reducing complexity compared to those in [11], [12], [13], [14]. Converter in [15] incorporates CIs with SEPIC topology and a resonant circuit, while the topology in [16] integrates CIs with VMC techniques. Although both converters improve voltage gain, their switches turn off under hard-switching conditions, requiring additional components to achieve fully soft-switching. A lossless passive snubber circuit is merged with the CIs-based Cuk converter, and a high step-up converter with soft-switching operation is introduced [17]. However, the converter input current is discontinuous, and the common ground is lost in this structure. A fully soft-switched high step-up converter is presented in [18], developed using CIs, and two SCs, along with two passive clamping circuits. However, it suffers from high input current ripple, and its number of components is also high.

In this paper, CIs and VMC methods are integrated and incorporated into the conventional boost topology, resulting in the proposal of a high step-up converter, in which the semiconductor devices voltage stress is a fraction of the output voltage. To ensure fully soft-switching circumstance, an appropriate snubber circuit with only two additional diodes is utilized. Likewise, the energy stored in the snubber circuit is efficiently recovered to the output without generating any circulating current, marking it as an advantageous characteristic among lossless snubber circuits. Furthermore, capacitive turn on loss is considerably reduced in the proposed converter. These attributes, including the reduction of the components voltage stress and the provision of soft-switching without circulating current, have contributed to improve the overall efficiency. The proposed converter also offers a common ground shared between the input and output terminals, as well as the switch, simplifying its control circuit. Additionally, continuous input current has made the proposed topology more suitable for photovoltaic system applications.

II. PROPOSED TOPOLOGY CONFIGURATION AND OPERATIONAL PRINCIPLES

The proposed soft-switched high step-up topology is shown in Fig. 1, in which the boost structure is formed by the input inductor L_{in}, switch S, diode D_1, and capacitor C_1. Meanwhile, the VMC cell incorporates the coupled inductors with primary windings N_1 and secondary windings N_2, capacitors C_2, C_3, and C_4, and diodes D_2 and D_3. Furthermore, the snubber capacitor C_S and the lossless snubber circuit include diodes D_4 and D_5, along with the CIs tertiary winding having N_3 turns. Remarkably, this arrangement ensures that no extra magnetizing core needs to be added to the proposed structure.

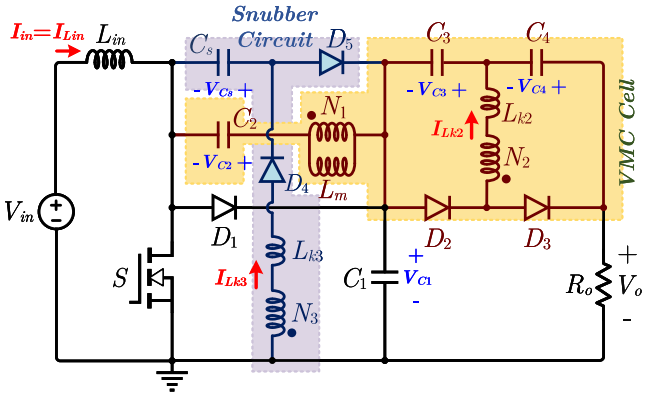

FIGURE 1. Proposed high step-up converter.

As illustrated in Fig. 1, the three coupled inductors are modelled by an ideal transformer with three windings, each having winding turns N_1, N_2, and N_3, a magnetizing inductance L_m, and two leakage inductances (L_{k_2} and L_{k_3}). The turns ratios of the CIs are defined as $n_1 = N_2/N_1$ and $n_2 = N_3/N_1$.

To facilitate the analysis of the operational principles, the following assumptions are considered. The converter operates under continuous conduction mode (CCM), and all components except the CIs, are supposed ideal. Additionally, capacitors C_1, C_2, and C_3, along with the input inductor L_{in}, are assumed to be sufficiently large; consequently, the capacitor voltages and the input inductor current remain constant within a switching cycle.

In a switching period, the proposed topology exhibits seven operating modes. The equivalent circuits of each operating mode, along with the converter key theoretical waveforms are illustrated in figs. 2 and 3, respectively. Prior to the first mode, all the semiconductor components are OFF, and the L_{in} current flows through L_m.

Mode 1 (t_0-t_1), see Fig. 2(a): At the beginning of the first mode, S is turned on under ZCS condition since L_m current (I_{L_m}) and L_{in} current ($I_{L_{in}}$) are equal which makes the current in S to rise gradually. V_{in} and $-(V_{C_1} - V_{C_2})$ are applied across L_{in} and L_m, respectively; thus, $I_{L_{in}}$ and I_{L_m} start to increase and decrease, respectively. Also, $-n_2(V_{C_1} - V_{C_2})$ is applied across N_3 causing D_4 to turn on and thus, a resonant occurs between L_{k_3} and C_S, resulting in N_1 current (I_{N_1}) and $I_{L_{k_3}}$ to increase while V_{C_S} raises resonantly to reach its maximum value. D_2 starts conducting but its current is negligible. The important equations of this mode are as follows:

$$I_{L_{k_3}}(t) = {}^{1}/_{Z_0}\left(n_2\left(V_{C_1} - V_{C_2}\right)\mathrm{Sin}\left(\omega\left(t - t_0\right)\right)\right) \tag{1}$$

$$V_{C_S}(t) = n_2\left(V_{C_1} - V_{C_2}\right)\left(1 - \mathrm{Cos}\left(\omega\left(t - t_0\right)\right)\right) \tag{2}$$

where ω and Z_0 are defined as $1/\sqrt{L_{k_3}C_S}$ and $\sqrt{L_{k_3}/C_S}$, respectively. At the end of this mode, V_{C_S} clamps to V_{C_1} and D_5 turns on.

Mode 2 (t_1-t_2), see Fig. 2(b): At t_1, D_5 turns on and $I_{L_{k_3}}$ start to decrease while $I_{L_{k_2}}$ increases. This mode terminates when $I_{L_{k_3}}$ reaches zero and D_4 and D_5 turn off under ZCS condition.

$$I_{L_{k_2}}(t) = -\left(\frac{n_1\left(V_{C_2} - V_{C_1}\right) + V_{C_3}}{L_{k_2}}\right)(t - t_1) \tag{3}$$

$$I_{L_{in}}(t) = I_{L_{in}}(t_1) + \frac{V_{in}}{L_{in}}(t - t_1) \tag{4}$$

Mode 3 (t_2-t_3), see Fig. 2(c): During this mode, S and D_2 are ON, and similar to the previous modes, L_{in} and L_m are being charged and discharged, respectively. Throughout this mode, C_1, C_2, and C_4 undergo discharge, while C_3 undergoes charging which persists until the switch is turned off at ZVS. In this mode the switch voltage reduces, resulting in low C_{oss} losses. Important equations of this mode are the same as the previous mode.

Mode 4 (t_3-t_4), see Fig. 2(d): This mode initiates when S is turned off under ZVS condition due to the capacitor loop around it (C_S and C_1). The polarity of voltage changes across L_m and turns on D_5 and thus, V_{C_S} decreases to zero while V_S increases to V_{C_1}. In this mode, I_{N_1} and consequently $I_{L_{k_2}}$ are decreasing. At the end of this mode, V_S reaches V_{C_1} while D_5 turns off under ZCS condition. Also, I_{N_1} changes direction; therefore, the D_2 current reaches zero and turns off under ZCS condition.

$$V_{C_S}(t) = V_{C_1} - \frac{I_{C_S}}{C_S}(t - t_3) \tag{5}$$

$$I_{L_{k_2}}(t) = \left(\frac{n_1 V_{C_1} - n_1 V_{C_2} - V_{C_3}}{L_{k_2}}\right)(t - t_3) \tag{6}$$

$$I_{C_S(max)} = 2I_{L_{in}(avg)} + \frac{nD}{f_s}\left(\frac{n_1\left(V_{C_1} - V_{C_2}\right) - V_{C_3}}{L_{k_2}}\right) \tag{7}$$

Mode 5 (t_4-t_5), see Fig. 2(e): Throughout this mode, V_{C_S} has reached zero and V_S is clamped to V_{C_1}, D_1 is on and C_1 is being charged while $I_{L_{k_2}}$ direction changes and flows through D_3. In the continuation of this mode, $I_{N_1} + I_{L_m}$ is increasing until it reaches $I_{L_{in}}$, and then D_1 turns off under ZCS condition. During this mode, C_3 and C_4 start to discharge and charge, respectively, while, C_1 and C_4 are charged.

$$V_{C_4}(t) = n_1 V_{C_2} - \left(\frac{\pi I_o}{2d_1}\sqrt{\frac{L_{k_2}}{C_4}}\right)\mathrm{Cos}\left(\omega\left(t - t_4\right)\right) \tag{8}$$

$$I_{L_{k_2}}(t) = \left(\frac{\pi I_o}{2d_1}\right)\mathrm{Sin}\left(\omega\left(t - t_4\right)\right) \tag{9}$$

where d_1 represents the duration of the fifth and sixth modes, equating to half the resonant period of C_4 and L_{k_2} during these modes.

Mode 6 (t_5-t_6), see Fig. 2(f): In this mode, I_{N_1} and consequently $I_{L_{k_2}}$ are decreasing, until their currents reach zero, simultaneously. At the end of this mode, $I_{L_{in}}$ and I_{L_m} become equal.

Mode 7 (t_6-t_7), see Fig. 2(g): At t_6, $I_{L_{in}}$ and I_{L_m} are equal and thus, S can be turned on under ZCS condition, where the minimum of $I_{L_{in}}$ is equal to the maximum of I_{L_m}.

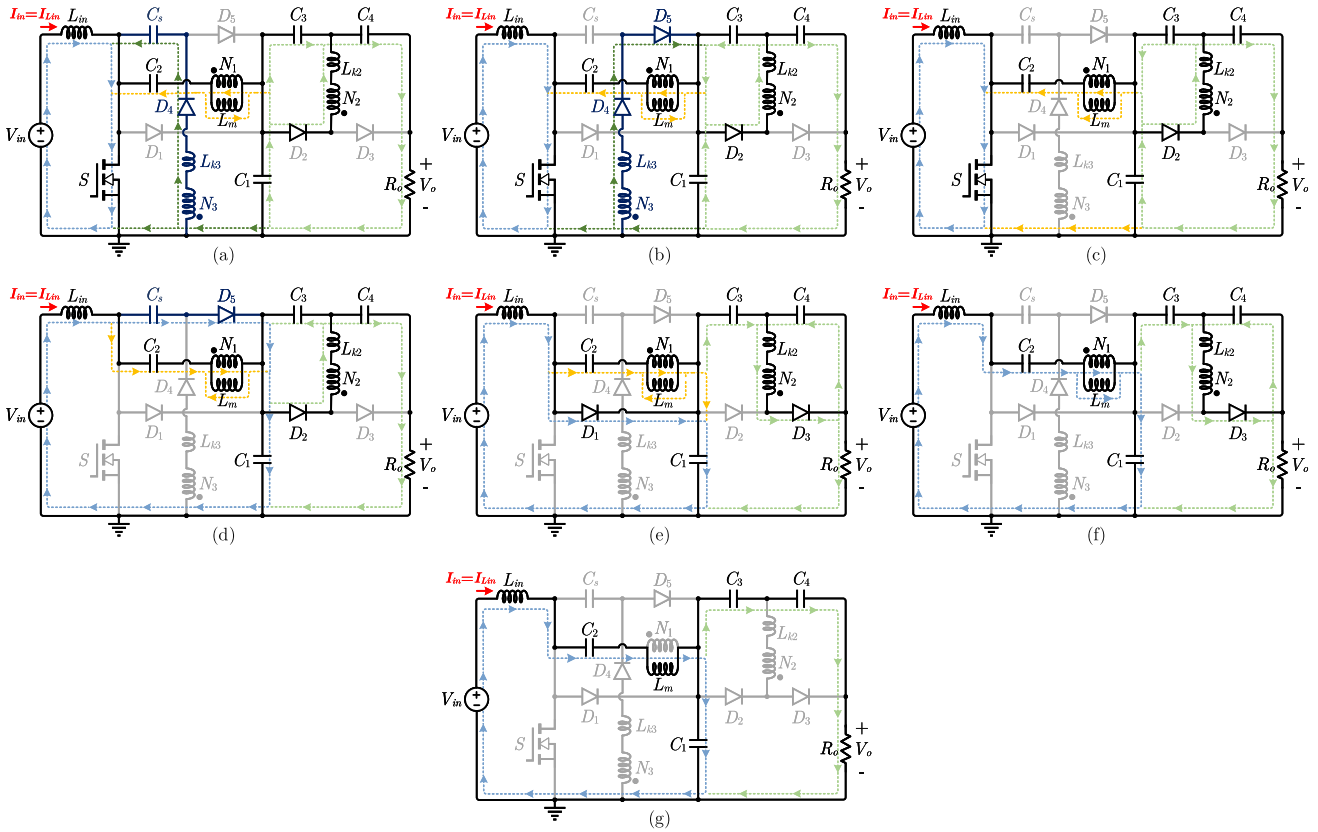

FIGURE 2. Equivalent circuits of the converter modes; (a) Mode 1 (t_0-t_1), (b) Mode 2 (t_1-t_2), (c) Mode 3 (t_2-t_3), (d) Mode 4 (t_3-t_4), (e) Mode 5 (t_4-t_5), (f) Mode 6 (t_5-t_6), and (g) Mode 7 (t_6-t_7).

III. STEADY-STATE ANALYSIS

This section outlines the steady-state analysis, encompassing calculations of the converter voltage gain, assessment of voltage stress on semiconductor devices, and the design of passive components. To streamline the steady-state analysis, the first, fourth, sixth, and seventh modes are overlooked due to their short durations.

A. VOLTAGE GAIN

By applying volte-second balance on L_{in} and L_m, V_{C_1} and V_{C_2} are calculated as follows:

$$V_{C_1} = \left(\frac{D+d_1}{d_1}\right) V_{in}, V_{C_2} = \left(\frac{D}{D+d_1}\right) V_{C_1} \tag{10}$$

At DT, I_o is equal to the average current of L_{k_2}, thus:

$$I_o = \left(\frac{D}{2}\right) I_{L_{k_2}(max)} \tag{11}$$

By employing (3), $I_{L_{k_2}(max)}$ is calculated as follows:

$$I_{L_{k_2}(max)} = -\left(\frac{n_1\left(V_{C_2} - V_{C_1}\right) + V_{C_3}}{L_{k_2}}\right) DT \tag{12}$$

By substituting (11) into (12), V_{C_3} is obtained as below:

$$V_{C_3} = n_1\left(V_{C_1} - V_{C_2}\right) - \frac{2V_o L_{k_2} f_s}{R_o D^2} \tag{13}$$

where D represents the duty cycle of the converter, f_s stands for the switching frequency, and R_o denotes the load resistance. By employing the equation $V_o = V_{C_1} + V_{C_3} + V_{C_4}$ and substituting (10) and (13), the voltage gain of the proposed topology is derived as follows:

$$\frac{V_o}{V_{in}} = (1+n_1)\left(\frac{D+d_1}{d_1}\right)\left(\frac{R_o D^2}{R_o D^2 + 2L_{k_2} f_s}\right) \tag{14}$$

Since the average current of L_m is zero, d_1 is derived as follows:

$$d_1 = \frac{2I_{in} L_{in} L_m}{V_{in}(L_{in}+L_m)DT} - D \tag{15}$$

As the term $(R_o D^2)$ is significantly larger than $(2L_{k_2} f_s)$, the effect of leakage inductance can be ignored. Therefore, the ideal voltage gain along with the capacitor voltages are derived as follows:

$$\frac{V_o}{V_{in}} = (1+n_1)\left(\frac{D+d_1}{d_1}\right) \tag{16}$$

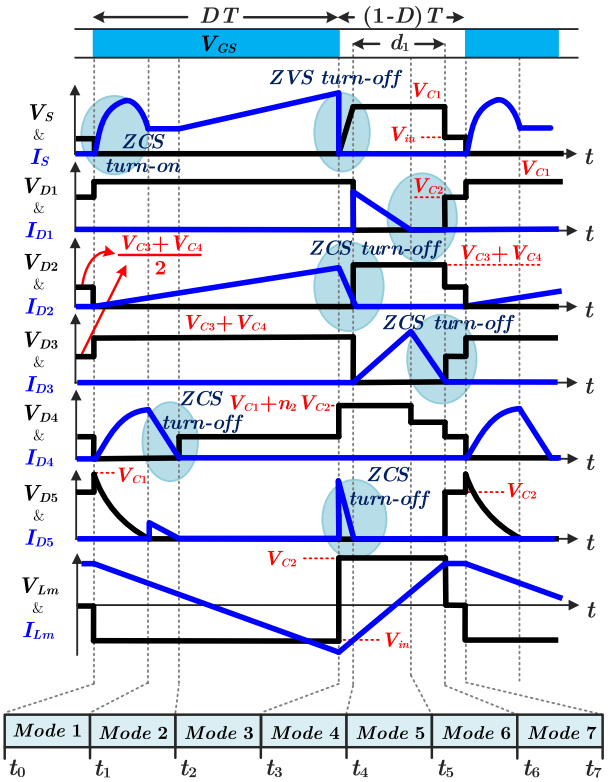

FIGURE 3. Key theoretical waveforms.

$$V_{C_1} = \left(\frac{D+d_1}{d_1}\right) V_{in}, V_{C_2} = \left(\frac{D}{d_1}\right) V_{in}$$

$$V_{C_3} = n_1 V_{in}, V_{C_4} = n_1 \left(\frac{D}{d_1}\right) V_{in} \tag{17}$$

Equation (16) demonstrates that the converter voltage gain is improved compared to the conventional boost topology, and the problems associated with the unity duty cycle are resolved. Also, the voltage gain is adjustable, and by increasing the CIs turns ratio (n_1), the converter voltage gain can be enhanced. It is noteworthy that, the duration of d_1 is smaller than $(1-D)$, presented in other step-up converters.

B. SEMICONDUCTOR COMPONENTS VOLTAGE AND CURRENT STRESS

Applying Kirchhoff's Voltage Law (KVL) principle within the fourth mode yields the voltage stress across the switch as follows:

$$V_S = V_{C_1} = \frac{V_o}{n_1+1} \tag{18}$$

Furthermore, the voltage stress across the diodes is determined by applying KVL in the converter loops.

$$V_{D_1} = V_{D_5} = V_{C_1} = \frac{V_o}{n_1+1}$$

$$V_{D_2} = V_{D_3} = \frac{n_1 V_o}{n_1+1}$$

$$V_{D_4} = V_{C_1} + n_2 V_{C_2} = \left(\frac{D(n_2+1)+d_1}{(n_1+1)(D+d_1)}\right) V_o \tag{19}$$

Equations (18) and (19) demonstrate a reduction in voltage stress across the semiconductor components. When $n_1 = 1$, the voltage stress on the semiconductor components is reduced to half of the output voltage, allowing the use of semiconductors with half the voltage rating compared to those in the conventional boost converter. This reduction in voltage stress enables the use of faster switches with low on-state resistance, as well as fast diodes with minimal forward voltage drop, which together result in lower conduction and switching losses, thereby improving overall efficiency.

The switch current stress equals the maximum value of the snubber capacitor current, as follows

$$I_{S(max)} = 2I_{L_{in}(avg)} + \frac{2n_1 I_o}{D} \tag{20}$$

Moreover, the diodes average current is obtained as:

$$I_{D_1(avg)} = I_{D_2(avg)} = I_{D_3(avg)} = I_{o(avg)}$$

$$I_{D_4(avg)} = I_{D_5(avg)} = \frac{2C_S f_s V_o}{n_1+1} \tag{21}$$

C. PASSIVE COMPONENTS DESIGN

The input inductor is designed similar to the boost input inductor [5], and the magnetizing inductance (L_m) is calculated as below:

$$L_m = \frac{V_{in} DT}{2I_{in}} \tag{22}$$

The average current of C_1 and C_4 when the switch is ON is equal to the output average current. Similarly, the average current of C_3 when the switch is OFF matches the output average current, while the average current of C_2 during the switch off-period is I_{in}. As a result, the capacitors values are determined as:

$$C_1 = \frac{I_o D}{\Delta V_{C_1} f_s}, C_2 = \frac{I_{in}(1-D)}{\Delta V_{C_2} f_s}, C_3 = \frac{I_o(1-D)}{\Delta V_{C_3} f_s} \tag{23}$$

where ΔV_{C_1}, ΔV_{C_2}, and ΔV_{C_3} are the capacitors voltage ripple. In order to establish soft switching condition at ZCS when the switch is turned on, half a resonance period of L_{k_2} and C_4 should be less than the duration of switching off-time, therefore:

$$\frac{T_{res}}{2} \le d_1 T \rightarrow \pi\sqrt{C_4 L_{k_2}} \le d_1 T \rightarrow C_4 \le \frac{\left(d_1 T/\pi\right)^2}{L_{k_2}} \tag{24}$$

The snubber capacitor is designed as follows:

$$C_S \ge \frac{I_S t_f}{2\Delta V_S} \tag{25}$$

As described in prior literature [19], I_S represents the maximum switch current prior to turn-off, t_f denotes the switch current fall time, and ΔV_S represents the switch voltage when the switch current reaches zero.

D. SOFT-SWITCHING REALISATION

In the proposed converter, before the switch turns on in the seventh mode, the L_{in} current flows through the L_m. At the beginning of the first mode, when the switch is activated, the switch current remains zero due to the series connection of L_{in} and L_m, which prevents any sudden change in the switch current. After the switch is turned on, the leakage inductance causes the switch current to rise gradually, enabling almost ZCS condition. The switch current increment rate should be limited at turn on. By writing the switch current expression, and calculating its increment rate the following equation is achieved

$$\frac{1}{\sqrt{L_{k_3}C_s}} \leq \frac{\gamma_i}{t_r} \tag{26}$$

where γ_i represents the ratio of the current slope in soft-switching to that in hard-switching, and t_r is the switch rise time.

When the switch is turned off at the start of the fourth mode, the capacitors C_S and C_1 around the switch prevent any abrupt voltage change, allowing for ZVS. To achieve this, the voltage across C_S must reach V_{C_1} ($V_{C_S}(t_1) \geq V_{C_1}$), which is facilitated by the resonance between C_S and L_{k_3} during the first mode, and V_{C_S} is clamped to V_{C_1} by D_5. Moreover, to fully charge C_S, half a resonance period $(T_{res}/2)_{L_{k_3}\&C_S}$ must be shorter than the duration of DT.

IV. RESULTS

In order to justify the converter performance and the analysis performed in the previous sections, a 150 W laboratory prototype converter with input voltage between 40 V to 52 V and 400 V output voltage, operating at 100 kHz switching frequency is implemented. The implemented prototype converter uses a Pulse-Width Modulation (PWM) control method. This control system integrates an SG3526 PWM controller IC for generating precise PWM signals and an HCPL3120 optocoupler IC to drive the gate with electrical isolation, ensuring safe and efficient operation.

A. DESIGN GUIDELINES

To select a high-efficiency switch according to (18), n_1 is chosen as 1.5, resulting in the switch voltage stress of 160 V. This makes the $IRFP4668PbF$ an appropriate and efficient choice for the converter. Additionally, as discussed in Section III-D, to ensure ZVS turn-off for the switch, the voltage across C_S must reach V_{C_1}. Therefore, n_2 is calculated to be 2. To further ensure soft-switching conditions, n_2 is selected as 2.5, providing greater confidence in achieving the desired switching performance. Using the prototype input and output voltages and applying (16), the duty cycle (D) is calculated to be 0.6, while d_1 is set at 0.2 to allow sufficient time for the switch to establish soft-switching condition during turn-on. From (19), the voltage stresses for D_1 and D_5 are calculated to be 160 V, while the voltage stresses for D_2 and D_3 are determined to be 240 V. Additionally, the voltage stress for D_4 is found to be $460V$. Consequently, $V30202C$ can be utilized for D_1 and D_5, while $SBR10U300$ is suitable for D_2, and D_3, and $1N5406$ is implemented for D_4. The average current for L_{in} equals the average input current, which is 3.75A. Consequently, L_{in} is computed to be 320 μH. In contrast, the average current for L_m is zero, but the current ripple for L_m is twice the input current, totaling 7.5A; hence, according to (22), L_m should have a value lower than 32 μH, and it is determined as 28 μH. Using (26), by considering a value of 0.2 for γ_i and substituting t_r from the switch datasheet, L_{k_3} is calculated to be greater than 10.3 μH, and in the experimental prototype, it is considered as 14 μH. As a result, the coupling coefficient $k = L_m/(L_m + \frac{L_{k_3}}{n_2^2})$ for the experimental laboratory prototype converter is determined to be 0.93. Based on (23), the values of C_1, C_2, and C_3 are derived as 3.3 μF, 10 μF, and 3.3 μF, respectively, and applying (24), C_4 is designed as 390 nF. Using (25), C_S is designed as 4.7 nF. The specifications of the implemented prototype converter are presented in Table 1.

TABLE 1. Implemented Prototype Topology Specifications

Parameters	Symbol	Specification
Capacitors	C_1	$3.3\mu F - 250\,V$ (Polyester)
	C_2	$10\mu F - 250\,V$ (Polyester)
	C_3	$3.3\mu F - 250\,V$ (Polyester)
	C_4	$390nF - 250\,V$ (Polyester)
	C_s	$4.7nF - 250\,V$ (Polyester)
Input inductor	L_{in}	$320\mu H$
Magnetizing inductance	L_m	$28\mu H$
Leakage inductances	L_{k2}	$5\mu H$
	L_{k3}	$14\mu H$
Switch	S	$IRFP4668PbF$
Diodes	D_1 & D_5	$V30202C$
	D_2 & D_3	$SBR10U300$
	D_4	$1N5405$

B. EXPERIMENTAL RESULTS

The implemented prototype topology, along with the voltage and current waveforms of the components, are shown in figs. 4 and 5, respectively. The waveforms for the switch and diodes D_1, D_3, D_4, and D_5 are depicted in figures 5(a)–(e), demonstrating the soft-switching behavior and reduced voltage stress. Fig. 5(f) presents the input inductor current and output voltage, while Fig. 5(g) shows the input current and voltage, confirming the voltage-boosting capability and continuous input current in the proposed topology. The zoom-out waveforms of S, D_1, and D_3 are illustrated in fig. 5(h)–(j).

V. COMPARISON

Table 2 provides a comparison between the proposed topology and other related counterpart converters. The highlighted

TABLE 2. Comparison Between the Proposed Topology and Other Counterpart Converters

Converter	Voltage Gain	Switch Voltage Stress	Number of Components S/D/M/C/T[1]	ICR[2]	CG[3]	Switching Condition Switches (on/off)		CTL[4]	Soft-Switching Technique
Ref. [7]	$\frac{3}{1-D}$	$\frac{V_o}{3}$	2/3/3/4/12	Low	Yes	Hard	Hard	High	—
Ref. [8]	$\frac{nD+D+1}{1-D}$	$\frac{V_o}{1+D+nD}$	1/2/2/3/8	Low	Yes	Hard	Hard	High	—
Ref. [10]	$\frac{2n+2}{1-D}$	$\frac{V_o}{2n+2}$	1/5/2/6/13	Low	No	ZCS	Hard	High	—
Ref. [11]	$\frac{n+2}{1-D}$	$\frac{V_o}{n+2}$	2/2/2/4/10	Low	Yes	ZVS	Hard	Zero	Active Clamp
Ref. [12]	$\frac{3-D}{1-D}$	$\frac{2V_o}{3-D}$	2/5/3/4/14	Medium	Yes	ZVS	ZVS	Zero	Active Clamp
Ref. [14](a)	$\frac{nD+2}{1-D}$	$\frac{V_o}{nD+2}$	2/6/3/2/13	High	Yes	ZCS	Hard	High	Passive Snubber
Ref. [14](b)	$\frac{nD+2}{1-D}$	$\frac{V_o}{nD+2}$	2/8/5/2/17	High	Yes	ZCS	ZVS	High	Passive Snubber
Ref. [15]	$\frac{2+n(1+D)}{1-D}$	$\frac{V_o}{2+n(1+D)}$	1/4/2/5/12	Low	Yes	ZCS	Hard	High	Quasi Resonant
Ref. [16]	$\frac{n+2}{1-D}$	$\frac{V_o}{n+2}$	1/3/2/4/10	Low	Yes	ZCS	Hard	High	Quasi Resonant
Ref. [17]	$\frac{1+(n_2+n_3)D}{1-D}$	$\frac{V_o}{1+(n_2+n_3)D}$	1/4/1/4/10	Medium	No	ZCS	ZVS	High	Passive Snubber
Ref. [18]	$\frac{1+n(1+D)}{1-D}$	$\frac{V_o}{1+n(1+D)}$	1/6/3/6/16	Medium	Yes	ZCS	ZVS	High	Passive Snubber
HSPC[5]	$\frac{(D+d_1)(n_1+1)}{1-D}$	$\frac{V_o}{n_1+1}$	1/3/2/4/10	Low	Yes	ZCS	Hard	Low	—
SSPC[6]	$\frac{(D+d_1)(n_1+1)}{1-D}$	$\frac{V_o}{n_1+1}$	1/5/2/5/13	Low	Yes	ZCS	ZVS	Low	Passive Snubber

[1] S: Switch(es)/ D: Diodes/ M: Magnetic Core(s)/ C: Capacitors/ T: Total number of components, [2] ICR: Input Current Ripple, [3] CG: Common Ground, [4] CTL: Capacitive Turn-on Loss, [5] HSPC: Hard-Switched Proposed Converter, [6] SSPC: Soft-Switched Proposed Converter.

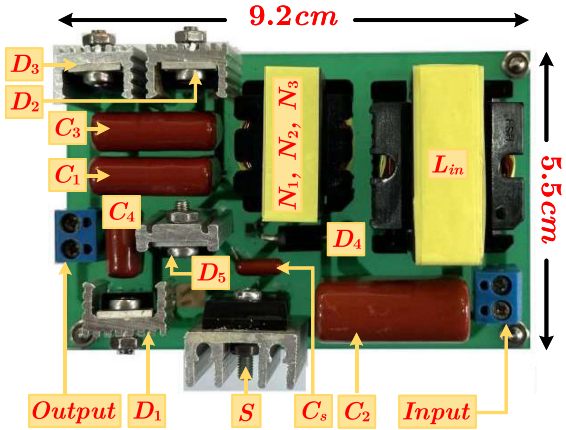

FIGURE 4. Converter laboratory prototype.

features of the proposed topology include improved voltage gain, reduced voltage stress on semiconductor components, fully soft-switching operation, continuous input current, and a shared common ground between the input and output terminals. All the counterpart converters listed in Table 2 are developed using various voltage-boosting methods to enhance their voltage gain and reduce the semiconductor components voltage stress. However, the converters in [7], [8] operate under hard-switching conditions, resulting in reduced efficiency. Additionally, fully soft-switching conditions are not provided for the converters of [10], [11], [14], [15], [16], and they require more components to achieve full soft-switching functionality. In contrast, the proposed topology, along with the topologies introduced in [17], [18] offer fully soft-switching operation; consequently, the switching frequency of these converters is not restricted and can be increased to reduce the size of passive devices and enhance power density. The topologies in [7], [11], [12], [14] incorporate two switches in their structures, and as each switch includes a gate driver and control circuitry, leads to increased structural complexity. Unlike the presented converters in [12], [14], [17], [18], the proposed topology, along with those in [7], [8], [10], [11], [15], [16], maintains continuous input current, eliminating the need for an input filter in solar system applications. Moreover, the proposed topology and the topologies in [7], [8], [11], [12], [14], [15], [18] share a common ground between the input and output terminals, simplifying system integration.

Fig. 6 compares the voltage gain of the proposed topology and counterpart converters as a function of duty cycle, with a coupled-inductors turns ratio of 1.5. The results highlight the superior voltage gain capability of the proposed topology, especially at a duty cycle of 0.65. Additionally, Fig. 7 presents the voltage stress comparison for the switch and output diode(s), showing that the proposed topology effectively reduces voltage stress on both components to below the output voltage. This reduction in voltage stress helps minimize converter losses and enhance overall efficiency.

VI. LOSS BREAKDOWN ANALYSIS AND EFFICIENCY

To validate the proposed converter efficiency improvement, a comprehensive loss analysis is conducted in this section. By ensuring fully soft-switching conditions for all semiconductor components, switching losses in both the switch and diodes are effectively eliminated. The remaining losses are classified into five categories. The first category is the parasitic capacitive turn-on loss, calculated as $P_{C_{oss}} = 1/2 C_{oss} V_{DS}^2 f_s = 0.09$ W, where C_{oss} represents the switch output capacitance. Notably, the parasitic capacitive turn-on loss is significantly

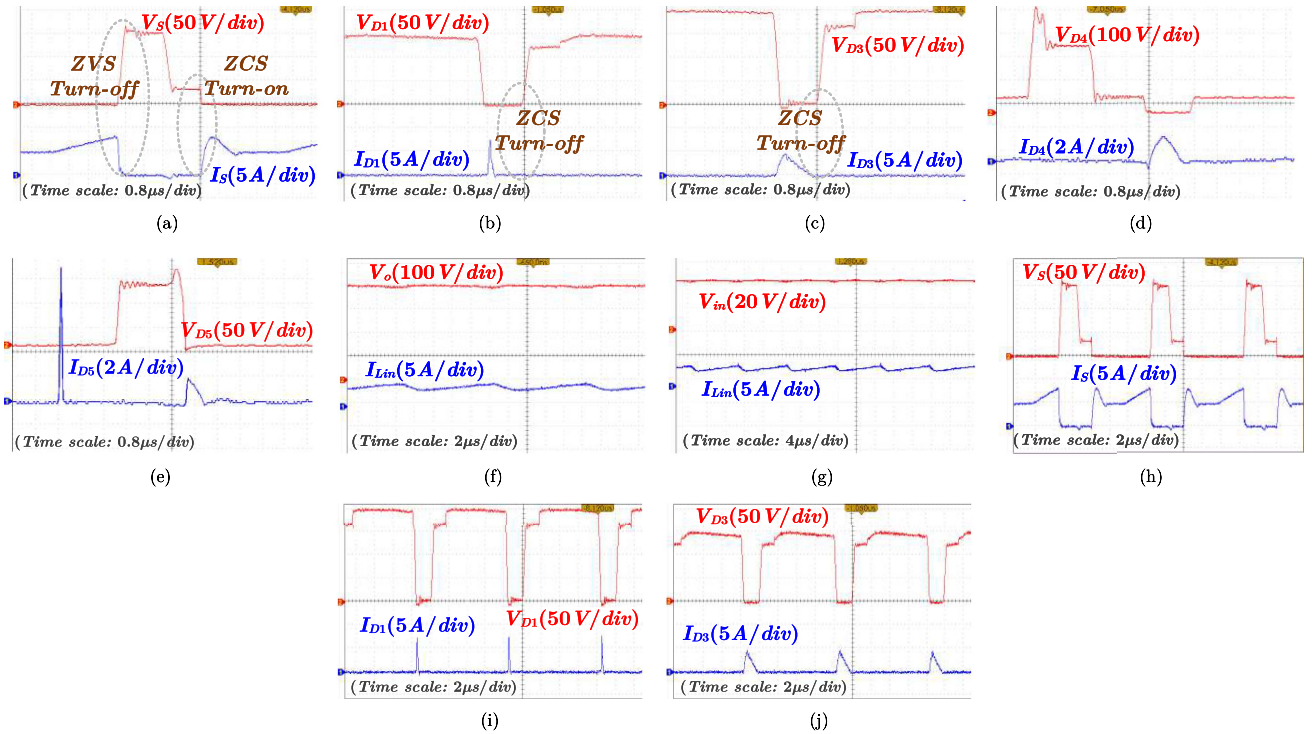

FIGURE 5. Experimental results of the proposed converter; the voltage and current waveforms of (a) S, (b) D_1, (c) D_3, (d) D_4, (e) D_5, (f) the input inductor current and output voltage, and (g) the input current and voltage; Zoom-out waveforms of (h) S, (i) D_1, and (j) D_3.

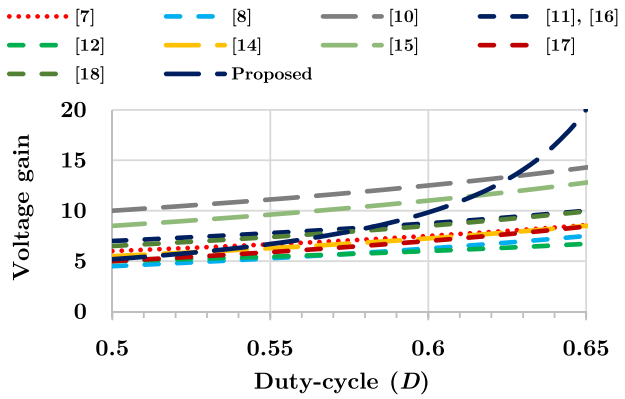

FIGURE 6. Voltage gain comparison between the proposed topology and counterpart converters versus duty cycle with a coupled-inductors turns ratio of 1.5.

mitigated due to the substantial reduction in switch voltage stress before the switch turns on in the first mode. The second category encompasses the switch conduction loss, derived as $P_{cond\_S} = R_{DS(on)} I^2_{rms\_S} = 0.17\,\text{W}$, with $R_{DS(on)}$ representing static drain-to-source on resistance. The third category involves diode conduction loss, determined by $P_{cond\_D} = V_F I_{avg\_D} = 0.8\,\text{W}$, where V_F is the instantaneous forward voltage. Conduction losses in the switch and diodes are minimized as a result of the reduced voltage stress, leading to an overall improvement in the converter efficiency.

Utilizing equation $P_{cond\_L} = R_{DC} I^2_{DC\_L} + R_{ac} I^2_{ac\_L}$, the conduction losses in the inductor are calculated. Due to employing Litz wires, R_{ac} and R_{DC} are nearly equal. Using $I^2_{rms\_L} = I^2_{DC\_L} + I^2_{ac\_L}$, the inductor conduction losses are determined as $P_{cond\_L} = R_{DC} I^2_{rms\_L} = 0.55\,\text{W}$. The final category of losses is the core losses, calculated as $P_{Core} = P_{CL} V_e = 1.09\,\text{W}$, where P_{CL} is the core loss, and V_e is the effective volume of the core.

Utilizing the results from the loss analysis, the theoretical efficiency of the proposed soft-switched topology and hard-switched converter (without the lossless snubber) are calculated to be 98% and 95%, respectively. The loss distribution of the both converters are illustrated in Fig. 8. These theoretical results are further validated through experimental and simulation results. It is important to note that the incorporation of soft switching and the reduction in semiconductor components voltage stress contribute to the elimination of switching losses. Additionally, the parasitic capacitive turn-on loss, as well as switch and diode conduction losses, are significantly mitigated, leading to an overall improvement in the converter efficiency.

The proposed converter efficiency versus the output power for input voltages of 40 V, 48 V, and 52 V is shown in Fig. 9. Typically, the components conduction losses decrease at lower powers, while the switch capacitive turn-on losses and core losses remain relatively constant. In the proposed converter, the voltage across the switch is substantially

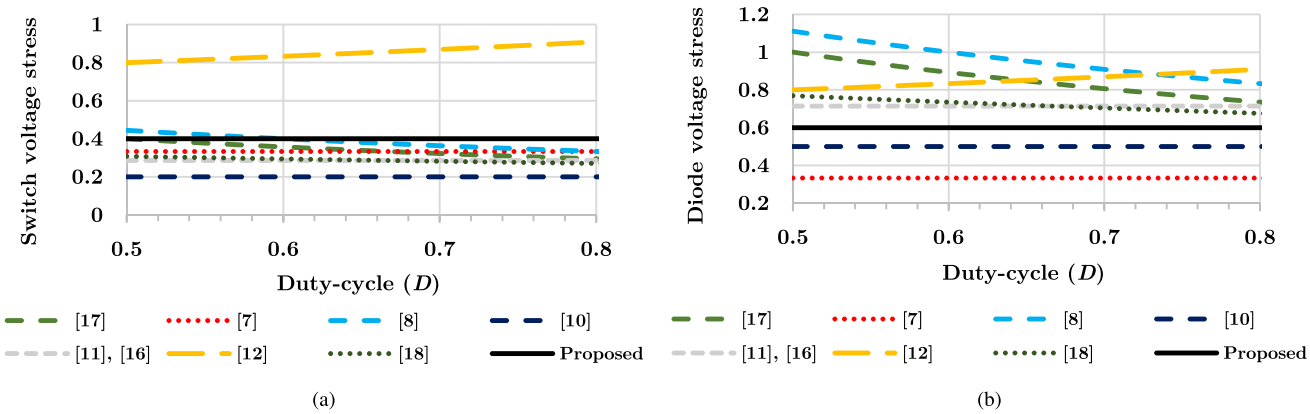

FIGURE 7. Voltage stress comparison for (a) the switch and (b) the output diode(s) between the proposed topology and counterpart converters versus duty cycle, with coupled-inductors turns ratio of 1.5.

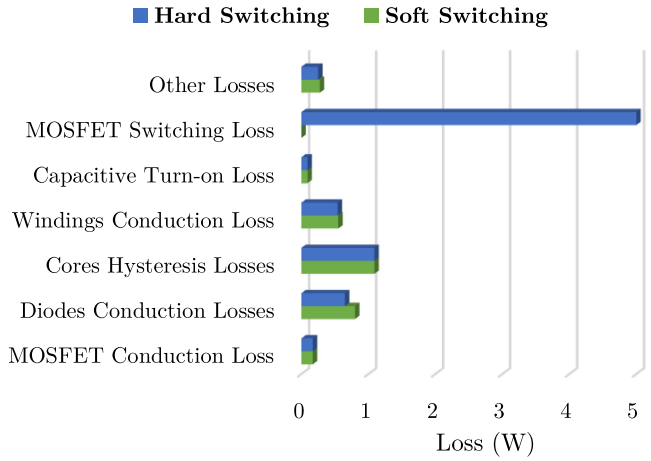

FIGURE 8. Loss distribution of the proposed hard-switched and soft-switched converters.

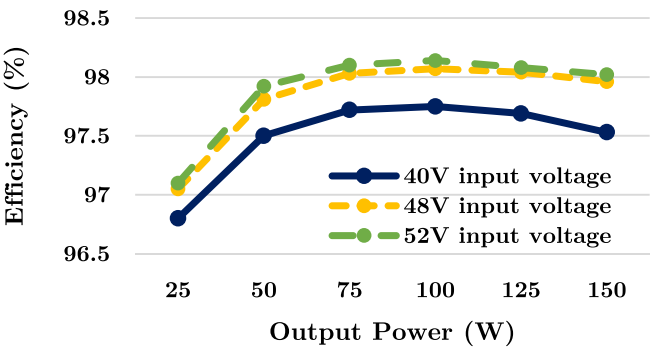

FIGURE 9. Proposed converter efficiency versus output power for input voltages of 40*V*, 48*V*, and 52*V*.

reduced before turn-on, significantly lowering the capacitive turn-on loss, which remain consistent across different power levels. Additionally, the input inductor undergoes minimal current variation, resulting in negligible core losses, as core losses are mainly driven by current changes. In the CIs, variations in I_{L_m} contribute to notable core losses. However,

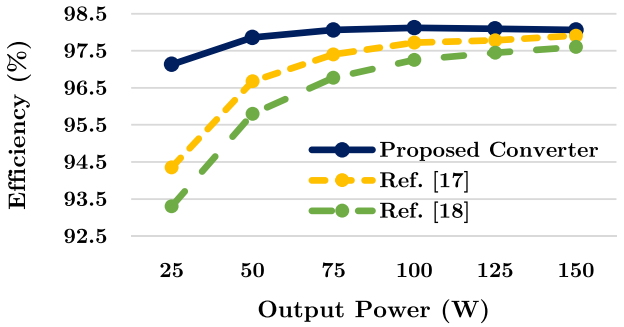

FIGURE 10. Efficiency comparison between the proposed converter and the presented topologies in [17] and [18].

these variations are directly tied to the input current, so as power decreases, the input current also reduces, leading to smaller fluctuations in I_{L_m} and thereby the CIs core losses decrease. As a result, the proposed converter maintains high efficiency even under light load conditions, as the overall efficiency is minimally affected by reduced power.

Fig. 10 compares the proposed soft-switched converter efficiency with similar counterpart converters listed in Table 2. The selected converters are all fully soft-switched, single switch with lossless passive snubber similar to the presented converter. To ensure a fair comparison, the efficiencies of all converters are evaluated under identical conditions (input/output voltages, switching frequency, and output power), using similar technology elements. At full load condition, the proposed converter as well as the topologies in [17] and [18] have almost similar efficiency. However, under light load condition, the capacitive turn-on and core losses in the proposed converter are almost negligible due to the voltage across the switch is substantially reduced before turn-on, significantly lowering the capacitive turn-on loss, which remain consistent across different power levels. Additionally, the input inductor undergoes minimal current variation, resulting in negligible core losses. Whereas the converters in [17] and [18] experience substantial losses. This difference leads to a decrease in their overall efficiency.

VII. CONCLUSION

In this paper, a fully soft-switched high step-up topology is developed by incorporating coupled inductors and a voltage multiplier cell into the conventional boost converter. This modification further improved the voltage gain and reduced the components voltage stress. Additionally, a suitable lossless snubber circuit comprising of only two diodes, requiring no additional switches or magnetic cores, is utilized to establish soft switching and zero-voltage switching (ZVS) for the switch, thereby enhancing the converter efficiency compared to the hard-switched version of the proposed topology. A $150W$ laboratory prototype topology with input and output voltages ranging from 40 to $400V$ is implemented, and the results demonstrate the superior performance of the proposed converter compared to other related counterpart converters. A comprehensive loss analysis is conducted for the proposed topology in both hard switching and soft switching operations, confirming the improvement in the efficiency of the soft-switched proposed converter. Furthermore, the proposed topology offers common ground shared between the input and output terminals, as well as the switch, and also continuous input current, simplifying its control circuit structure.

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