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DOI
10.1109/PVSC57443.2024.10749399

Publication date
2024

Document Version
Final published version

Published in
2024 IEEE 52nd Photovoltaic Specialist Conference, PVSC 2024

Citation (APA)
Van Dyck, R., Van Nijen, D., Muttillo, M., Manganiello, P., Bakovasilis, A., Borgers, T., Onda, K., Zulhidza, R., Isabella, O., & More Authors (2024). Photovoltaic Module-Integrated Capacitors to Facilitate Embedded Power Electronics. In *2024 IEEE 52nd Photovoltaic Specialist Conference, PVSC 2024* (pp. 356-358). (Conference Record of the IEEE Photovoltaic Specialists Conference). IEEE. https://doi.org/10.1109/PVSC57443.2024.10749399

Photovoltaic Module-Integrated Capacitors to Facilitate Embedded Power Electronics

Rik Van Dyck[1,2,3,4], David van Nijen[5], Mirco Muttillo[5], Patrizio Manganiello[5], Apostolos Bakovasilis[1,2,3,4], Tom Borgers[2,3,4], Kinichi Onda[6], Restu Zulhidza[6], Wilmar Martinez[1,4], Hariharsudan Sivaramakrishnan Radhakrishnan[2,3,4], Olindo Isabella[5], Aart Willem van Vuure[1], Jef Poortmans[1,2,3,4]

1. KU Leuven, Leuven, Belgium,
2. Hasselt University, imo-imomec, Hasselt, Belgium
3. imec, Leuven, Belgium
4. EnergyVille, Genk, Belgium
5. Delft University of Technology, Delft, The Netherlands
6. Nippon Chemi-Con, Fukushima, Japan

2024 IEEE 52nd Photovoltaic Specialist Conference (PVSC) | 978-1-6654-6426-0/24/$31.00 ©2024 IEEE | DOI: 10.1109/PVSC57443.2024.10749399

I. INTRODUCTION

An important part of modern photovoltaic (PV) systems is the so-called power electronics. Its two main goals are to convert the power output of a PV module to the desired voltage, current, and frequency, and to control the operation point of the PV modules for maximum power harvesting. The power electronics and their behavior within a hybrid, smart AC-DC system is currently being studied within the emerging field of *photovoltatronics* [1]. This coincided with (sub-) module-level power electronics being one of the fastest-growing market segments in the solar industry, namely power converters designed to be used for (a part within) one single PV module. It comes with advantages, such as increased shade tolerance, energy yield, module reliability, safety, and design flexibility. However, module-level converters are nowadays both bulky and expensive, with most of the volume being occupied by passive devices such as inductors and capacitors. These passives also represent a significant share of the converter cost. On top of this, power converters are still the least reliable part of a PV system [2]. To increase the lifetime and performance of power converters while reducing their cost and size, power electronics research is focusing on the integration of power converters, and there are two ways of doing so [3]:

- Wafer integration: all system components, including passive devices such as capacitors and inductors, integrated into one single chip. This solution is also called Power System-on-Chip (PwrSoC).
- Package integration: integrated circuits and passive components bundled in a package. Such a solution is also called Power System-in-Package (PwrSiP).

In both cases, the major bottleneck is again represented by passive components. Size reduction of both capacitors and inductors can be obtained through high converter's switching frequency. However, this size reduction has two main disadvantages: higher switching frequency leads to higher electromagnetic interference since this is directly proportional to the square of the frequency; and fabrication of small inductors for PwrSiP or PwrSoC is complex and expensive, thus increasing the overall cost of the converter [4].

This work explores another approach, which keeps only the active components in the converter, and shifts the passive components to other parts of the PV system: the PV module. A first step would be to employ the intrinsic capacitance of the solar cell by using a smart cell interconnection design. Chang et al. previously reported on the idea of distributed power electronics using the cell junction capacitor [5]. This might become even more relevant with the ever-increasing capacitance of modern, high-efficient solar cells. In previous work, the impedance of single solar cells was studied using an in-house designed impedance spectroscopy setup for solar cells [6]. Also, a fitting procedure to find the PN junction capacitance (C_j) of different solar cell architectures was described. As expected, it was found that C_j is dependent on the applied bias voltages; hence it will also vary under different illumination intensities. As a next step, custom-built capacitors are integrated into modules containing IBC solar cells to achieve a less variable module impedance and further study the feasibility of passive-free power electronics. This work focuses on the integration of add-on capacitors into a module and investigates the influence of these additional capacitors on the module's impedance.

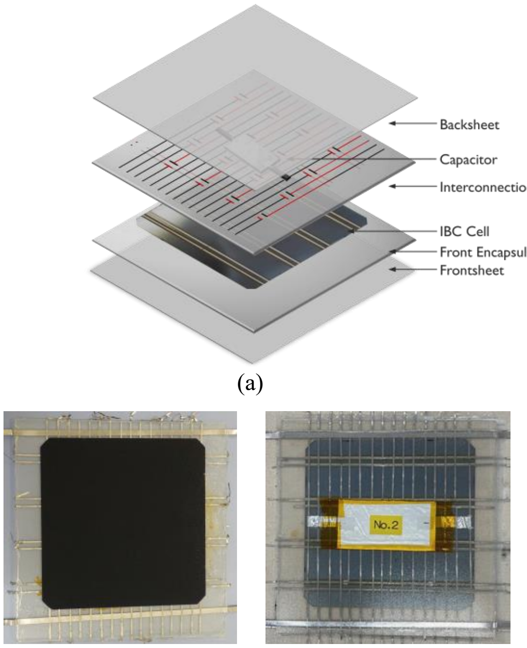
II. MATERIALS AND METHODS

A. *Sample preparation*

Module integration poses additional size limitations for the passive components. For this work, electrolytic plate-plate capacitors – as shown in Fig. 1 – having aluminum leads and a thickness of 120 µm are provided by Nippon Chemi-Con.

Fig. 1. Photo of an electrolytic plate-plate capacitor.

Two functional laminates, each containing one zebra interdigitated back-contact (IBC) solar cell are made using a three-dimensional (3D) interconnection. The technology is based on a 3D woven interconnection fabric into which components can be integrated, thus potentially facilitating module integration on an industrial scale. In this work, a capacitor is integrated in the connection fabric using an electrically conductive adhesive. Laminate fabrication happens in a two-step cycle. First, a layup is made, of which an exploded view is shown in Fig.2 (a). Then this layup is laminated to form the one-cell laminates, with or without integrated capacitor. A more elaborate discussion of the principles, advantages and fabrication procedures of this novel 3D interconnection concept is beyond the scope of this abstract but can be found in previous publications [7].



(a)

(b)

Fig. 2. **(a)** Exploded view of the module layup; **(b)** Front and rear side of a one-cell laminate with zebra IBC cell and integrated capacitor.

B. *Impedance characterization*

The non-linearity and high operating currents of solar cells bring additional challenges to the impedance measurement procedure. In this work, impedance measurements are performed in the frequency domain in dark conditions at different DC bias voltages. A custom-built setup is used, and a schematic diagram is shown in Fig. 3. It uses power supplies (PS1 and PS2) and a function generator (FG) to provide a DC bias voltage and an AC signal input, and two lock-in amplifiers (LA1 and LA2) for current and voltage output signal detection. An in-depth description can be found in a previous publication [6]. The in- and output signals are used for electrical model fitting using MATLAB.

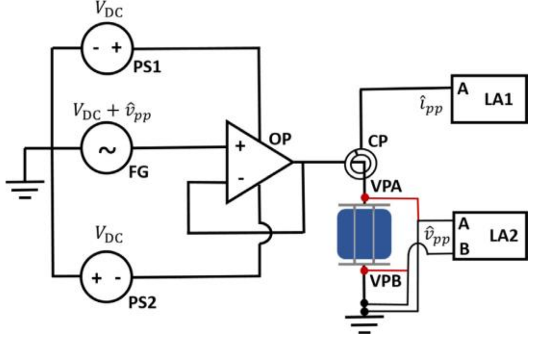


Fig. 3. Schematic diagram of the impedance spectroscopy setup for mini modules [6].

III. RESULTS AND DISCUSSION

This section discusses the results of the impedance characterization and modeling of three samples: a custom-made capacitor, a laminate with zebra IBC cell (IBC) and a laminate with zebra IBC cell and integrated capacitor (IBC+C).

A. *Capacitor model*

The electrolytic plate capacitor used in this study can be modeled as an RCL-loop as shown in Fig. 4. After performing impedance spectroscopy, the best fitting values for this circuit are 0.103 Ω, 198 µF and 102 nH for R_c, C and L_c respectively.

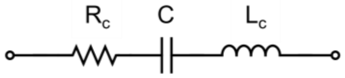


Fig. 4. Equivalent model of the capacitor.

B. *Zebra IBC cell model (IBC)*

The used equivalent model of a one-cell laminate is shown in Fig. 5, where the combination of R_j and C_j are attributed to the PN-junction, the R_{LH} and C_{LH} to the low-high junction and R_s and L_s mainly to the metallization and interconnection.

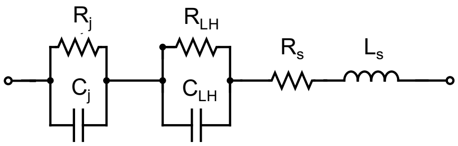


Fig. 5. Equivalent model of a one-cell laminate.

In previous research, it was found that the IBC cell junction capacitance increases with an increase in the applied bias voltage [6]. The results on zebra IBC cells with a three-dimensional interconnection yield similar results, of which some can be found in Table 1.

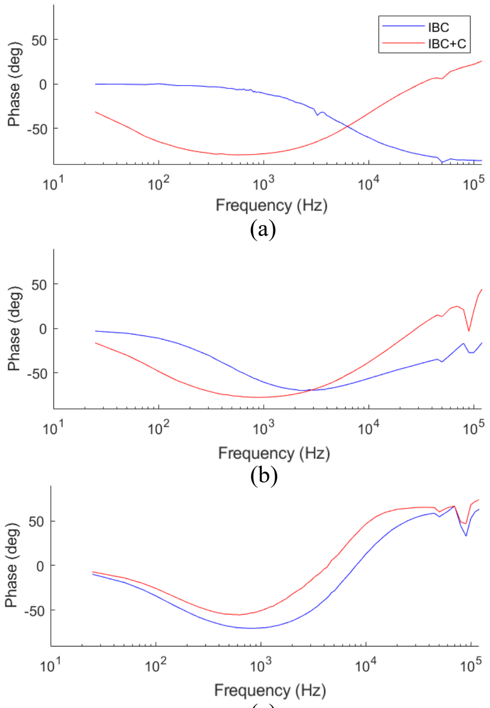
TABLE I

FITTED RESULTS OF THE IBC CELL LAMINATE MODEL

Bias Voltage (mV)	C_j (µF)	R_j (Ω)	C_{LH} (µF)	R_{LH} (Ω)	R_s (mΩ)	L_s (nH)
0	2.326	13.06	-	-	0.72	85.83
300	5.824	9.03	8.65	0.803	2.42	90.02
450	44.8	1.94	38.7	0.034	2.08	86.00
550	2192	0.439	463	0.013	2.42	85.80
600	9574	0.086	750	0.010	2.05	97.71

C. Combined zebra IBC cell and capacitor model (IBC+C)

Impedance characterization on the one-cell laminate with integrated capacitor (IBC+C) was performed using the same measurement procedure as for the laminate without capacitor (IBC). Fig. 6 shows the impedance phase of the IBC and IBC+C samples at three different DC bias voltages. Note that the impedance behavior of the integrated capacitor is independent of the bias voltage. It can be observed that the effect of the capacitor on the laminate impedance is large at low bias voltages and becomes less at higher bias voltages. Indeed, the capacitor had a fixed capacitance of around 200 µF, while the junction capacitance of the solar cell is small (a few µF) at low bias voltages and increases to 44.8 uF and 2192 uF when increasing the bias voltage to 450 mV and 550 mV respectively.



(a)

(b)

(c)

Fig. 6. Phase of the impedance of the IBC cell (IBC) and IBC cell and capacitor (IBC+C) laminate as a function of the frequency at a DC bias voltage of **(a)** 0 mV, **(b)** 450 mV, and **(c)** 550 mV.

Since the capacitor is integrated into the metal interconnection and connected in parallel with the solar cell, an equivalent model can be established as shown in Fig. 7. In this model, the R_s and L_s from the metallization and interconnection are divided between R_{s1} and R_{s2}, and L_{s1} and L_{s2}.

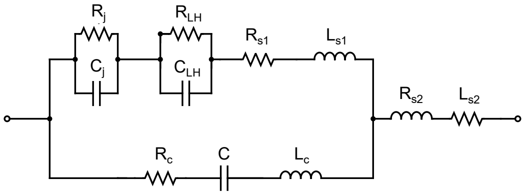


Fig. 7. Equivalent model of a one-cell laminate with integrated capacitor.

This model has been simulated using the software LTspice, where Rs and Ls are split equally as a first approximation ($R_{s1} = R_{s2}$ and $L_{s1} = L_{s2}$). The impedance magnitude and phase of the measured and simulated model of the IBC+C laminate operating at 300 mV are shown in Fig. 8, showing a good match between simulation and measurement.

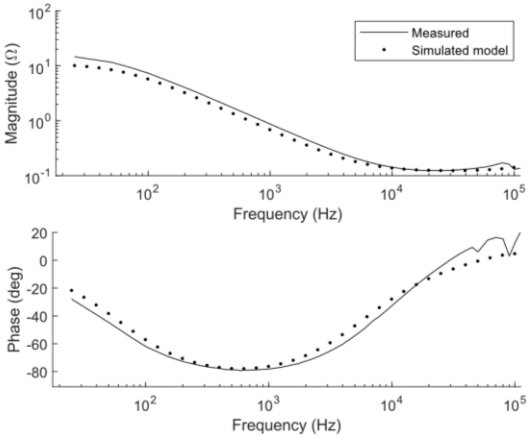


Fig. 8. The impedance magnitude and phase of the IBC+C laminate, and the simulated equivalent model at a DC bias voltage of 300 mV.

IV. CONCLUSIONS AND OUTLOOK

A functional one-cell laminate with integrated capacitor is fabricated and analyzed using a custom impedance characterization setup. First attempts in modeling the electrical behavior of the solar cell and capacitor have been performed.

One important aspect is the scale-up of these experiments to larger samples. Modules containing 4 IBC cells and add-on capacitors are currently being fabricated. We aim to perform impedance characterization on the modules and build a custom-designed power converter to assess the potential benefit of a simplified design.

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