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Design of a High-Voltage Arbitrary Waveform Generator Using a Modular Cascaded H-Bridge Topology

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Abstract: As the integration of renewable energy sources into the grid increases, the insulation systems of grid components such as transformers and switchgear encounter significant challenges due to the transients and harmonics generated by power-electronic-based converters. A test generator capable of replicating these component stresses is essential to accurately evaluate these insulation systems under real-grid conditions. This paper proposes a modular cascaded H-bridge-based high-voltage arbitrary waveform generator, prototyped with three stages to generate customized waveforms (triangular, sawtooth, pulse, and complex) up to 8 kV. The H-bridge modules are designed using Si MOSFETs with a maximum blocking voltage of 4.5 kV. The input to the HV H-bridge module is provided by a 10 kV medium-frequency transformer, whose design is described with a focus on the insulation system and winding configuration. This transformer is driven by a zero-voltage switching driver. This arbitrary waveform generator excels in several aspects, including a straightforward design procedure, compact size, high voltage capability, ease of integration, and cost.

Keywords: high-voltage H-bridge; medium-frequency transformer; zero-voltage switching driver; high-voltage arbitrary waveform generator

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1. Introduction

As a large number of renewable energy sources are integrated into various levels of the power grid, there will be substantial growth in the use of power-electronic (PE)-based converters for electric power conversion such as DC-to-AC and AC-to-DC, which will gradually dominate the power grid. However, due to the fast switching and high dv/dt and di/dt, PE-based modules generate high-frequency (HF) harmonics, transients, steep current spikes, and voltage overshoots, creating new electric field stresses on HV insulation systems. Therefore, the HV equipment insulation can degrade faster and jeopardize the reliability of grid assets.

It is widely known that the mitigation of these harmonics, transients, spikes, and oscillations is complicated because of the unavoidable parasitic parameters present in the PE-based converters, which can rapidly charge or discharge due to the solid-state switching and HF circulating current harmonics. The most economical and practical solution is to improve the insulation quality of the HV grid components. Before installation, these HV components should be tested under specific and customized HV and HF field strength, similar to the actual power grid. A reliable HV arbitrary waveform generator (HV-AWG) that can generate such HV test signals is required for insulation testing. Typically, insulation materials are characterized using (quasi-)sinusoidal signals produced by various pulse transformers.

In addition to power grids, railway systems operate under similar HV conditions where the accurate measurement of system impedance is required [1,2]. The impedance

characteristics of the railway system, especially in double-sided feeding systems, need to be measured by injecting harmonic signals into the system. For instance, railway traction power supply systems, which operate at voltages as high as 25 kV, experience harmonic resonance that can affect system stability. The injection of high-order harmonic signals, up to 5 kHz, is necessary to evaluate the system's impedance and stability [3,4]. Thus, the HV-AWG capable of producing customized waveforms, including harmonics and other transient signals, is essential for both grid and railway applications.

1.1. State of the Art

Several effective approaches to an HV-AWG for insulation testing have already been presented in the literature. An overview of these approaches is given:

- Commercially available linear HV amplifier (e.g., Trek).
- Modular multilevel converter (MMC) [5].
- Modular cascaded H-bridge (CHB).
  - With flyback supply [6].
  - With boost supply [7].

The function generator combined with the HV Trek amplifier can easily generate arbitrary waveforms, but its output waveform is limited to a low bandwidth ($\leq$2.5 kHz). MMCs have high efficiency and scalability and offer excellent harmonic performance. However, they are complex in terms of control and design. Additionally, the large number of components makes maintenance and fault detection more challenging and time-consuming. The submodule of the CHB-based HV-AWG with boost supply has low voltage capability due to the absence of the transformer. Achieving a certain level of HV output requires more submodules, resulting in a more complicated control algorithm. Furthermore, the flyback supply requires a complicated transformer insulation system. Consequently, an HV-AWG with a higher submodule output voltage capability ($\approx$3 kV_{pk}), simple design and control algorithm, compact size, high scalability, and low manufacturing cost is desired.

1.2. Proposed Topology

The general architecture of the envisioned modular CHB-based HV-AWG with multiple stages is illustrated in Figure 1, highlighting two critical components: the isolated DC/DC supply and the HV H-bridge.

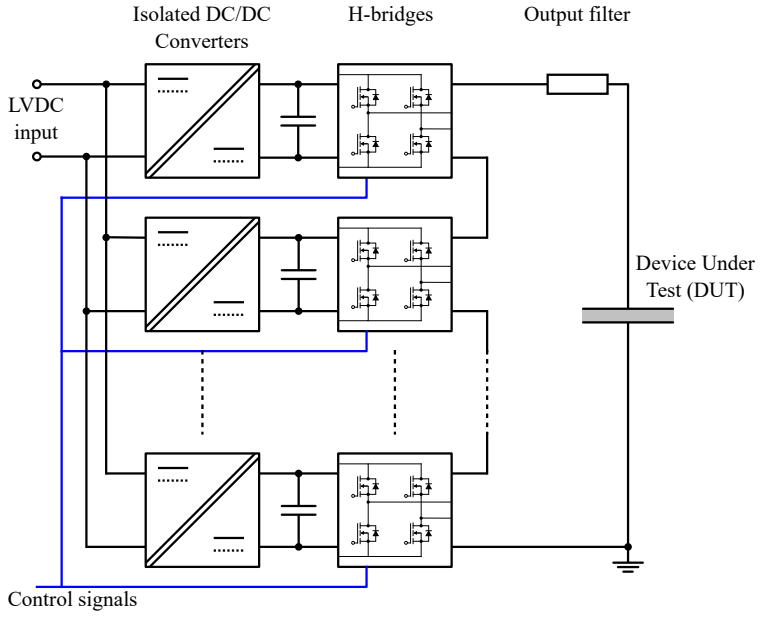


Figure 1. Modular cascaded H-bridge topology for HV AWG showing three cascaded stages.

The low-voltage (LV) DC input, supplied by a commercial DC source, will be converted into either HF AC pulses (hard-switching) or sinusoidal waveforms (soft-switching) to drive a medium-frequency transformer (MFT) operating at frequencies above 25 kHz. The transformer is designed to provide a galvanic isolation of at least 10 kV between the primary and secondary sides, requiring careful insulation and winding design. The MFT's output voltage is rectified into a high DC voltage and supplied to the HV H-bridge module. By precisely controlling multiple high-voltage H-bridge modules, the output waveform of this modular CHB-based HV-AWG can be customized.

1.3. Outline

In Section 2, the design process of the HV H-bridge is elaborated on, focusing on the selection of semiconductor devices and gate driver design. Section 3 explains the design of the isolated DC/DC converter comprising a zero-voltage switching (ZVS) driving circuit and MFT. The transformer, designed in a split winding configuration and insulated with silicone rubber, can easily provide isolation voltages above 8 kV. Section 4 presents the experimental results of the three-stage HV-AWG prototype, demonstrating the achievement of customized waveforms with a peak voltage of 8 kV. Finally, Sections 5 and 6 discuss the enhancements to the AWG submodules to improve their high voltage capability and scalability.

2. H-Bridge Design

The number of output voltage levels N_{level} can be calculated from (1) by considering that each H-bridge stage has three states ($+V_{DC}$, 0, and $-V_{DC}$). The number of cascaded H-bridge submodules is N.

$$N_{level} = 2N + 1 \tag{1}$$

The number of cascaded H-bridge stages depends on generator output voltage, circuit complexity, and cost. With a low number of stages, to fulfill a desired output voltage, the voltage per stage is high, adding cost and complexity to the semiconductor devices. Additionally, the output waveform will have a smaller number of levels. On the other hand, with a large number of stages, more isolated DC/DC converters and control circuits are required. The number of stages is related to the maximum output voltage U_{out}^{max} by (2), where U_{stage}^{max} is the maximum stage voltage.

$$N = \frac{U_{out}^{max}}{U_{stage}^{max}} \tag{2}$$

The limited number of N_{level} in the HV-AWG restricts its ability to accurately approximate arbitrary waveforms, resulting in relatively coarse and rough approximations. Increasing the number of stages would enhance resolution and produce smoother waveforms, particularly important for generating complex shapes such as impulse waveforms. However, adding stages increases the HV-AWG system's complexity, requiring more auxiliary circuitry. This design demonstrates the feasibility of a cascaded H-bridge-based HV-AWG with three H-bridge modules. U_{out}^{max} is limited to 8 kV due to the insulation level of the components integrated into H-bridges (e.g., optocouplers). The scalability of the system also depends on the control architecture; for example, the Typhoon HIL 604 controller could support up to 32 digital outputs. Future work will explore further scalability through fiber-optic connections to increase the number of cascaded H-bridges.

2.1. Semiconductor Device Selection

In the semiconductor device selection, a trade-off must be made between its breakdown voltage and current capacity (or on-resistance $R_{DS,on}$). In general, the on-resistance increases more than quadratically with increasing breakdown voltage due to the required die thickness [8]. Silicon carbide (SiC) devices with voltage ratings up to 3.3 kV and excel-

lent current ratings are available. However, this restricts the maximum voltage per stage to about 2 kV (considering a 40 % safety factor). Placing multiple low-voltage (e.g., 1.2 kV) devices in series is possible, but this introduces additional complexity to maintain equal voltage sharing across the devices [9]. Silicon (Si) devices with higher voltage ratings are commercially available because the technology is more mature than SiC, resulting in a low price. However, they typically have much larger on-resistances than an equivalent SiC MOSFET would have.

The current rating of the applied switches can be divided into repetitive peak current $I_{d,pk}$ (during switching transients) and the RMS current $I_{d,rms}$, which determines the thermal performance. For the proposed HV-AWG, the generator drives an *RC* load, and a considerable amount of current will only be drawn during the switching transients. To accurately replicate the fast transient overvoltages that insulation materials might encounter in real applications, the waveform generated by the HV-AWG must have a relatively short rise time t_r. The peak current through the HV H-bridge module is given by (3). Considering the HV-AWG stage output U_{stage}^{max} of 3 kV, for a rise time of about 0.6 µs and a maximum load C_{DUT}^{max} of 60 pF (extra 20 pF for parasitics C_{par}), the permissible pulsed drain current I_{DM} of the selected MOSFET should be larger than 0.4 A ($I_{d,pk}^{max}$).

$$I_{d,pk}^{max} = (C_{DUT} + C_{par})\frac{dU}{dt} \approx (C_{DUT}^{max} + C_{par})\frac{U_{stage}^{max}}{t_r} \tag{3}$$

$$I_{d,rms}^{max} \approx 2\pi f_s^{max} \cdot U_{stage}^{max} \cdot (C_{DUT}^{max} + C_{par}) \tag{4}$$

If the HV-AWG device is used to perform sample breakdown tests, to obtain the required t_r, the total resistance in the circuit (MOSFET $R_{DS,on}$ and external resistance R_{ext}) should be limited. For an RC output circuit, the 10–90% rise time can be approximated by 2.2τ, where τ stands for RC time constant. For the prototype HV-AWG, the value of R_{tot} is selected as 14 kΩ, resulting in a maximum fault current of 0.57 A when the maximum sample voltage U_{out}^{max} 8 kV is applied. Owing to the low capacitive load application, for an AWG output frequency f_s of 1–10 kHz, the permissible continuous current of the selected MOSFET should be above $I_{d,rms}^{max}$ (0.04 A), which is easily achievable.

Considering the component's price and availability, the Si MOSFET of type IXTT02N-450 HV is selected, which has a continuous current capability of 0.2 A (0.6 A for I_{DM}) and a voltage limitation of 4.5 kV, with an $R_{DS,on}$ of around 625 Ω. Thus, U_{stage}^{max} is decided as 2.7 kV, considering a 40% safety margin, and the number of stages N should be 3. During the HV testing, if the insulation sample breaks down, the HV-AWG output is momentarily short-circuited, causing a large current pulse to be drawn either once or multiple times in quick succession. This short-circuit current can be limited by the resistance in the three-stage CHB circuit, which includes (i) the Si MOSFET $R_{DS,on}$ multiplied by two times the number of stages N, and (ii) an external current limiting resistor R_{ext} with a value of 10.25 kΩ, calculated by (5).

$$R_{ext} = R_{tot} - 2NR_{DS,on} \tag{5}$$

For breakdown testing of insulation samples, a smaller t_r and faster switching performance can be ensured by selecting a smaller external resistance R_{ext}, particularly when the HV H-bridge utilizes the semiconductor devices with higher current ratings or when the required output voltage U_{out} for sample breakdown is lower. Additionally, if the current measurement sensor exhibits extremely high sensitivity, R_{ext} can potentially be eliminated. In cases where the arbitrary waveform generator is employed solely for aging insulation samples over a fixed duration, rather than for breakdown testing, R_{ext} can also be omitted, allowing the generation of waveforms with exceptionally short t_r values. As R_{ext} can be significantly reduced in these scenarios, the achievable t_r can be improved, thus expanding the applicable range of sample loads C_{DUT} for testing.

2.2. Gate Driver Circuit

Because the HV H-bridge circuits' reference potentials are switching with the output voltage, high isolation is required between the H-bridge and the control circuit. This isolation concerns the gate signals, gate driver supply voltages, and optional feedback signals such as measurements or status signals. Optical signal isolation is one of the feasible choices for the considered output voltage levels, either using a high-isolation optocoupler or fiber optics. The rest of the gate drive circuitry must only withstand the voltages inside one H-bridge stage. This concept is shown schematically in Figure 2, where the non-isolated gate driver circled by red is implemented using a BJT push–pull stage with a split output and the isolation barrier is shifted towards the optocoupler and isolated DC/DC converter. Compared to the core-isolation method [10,11], the optical-isolation method excels in its superior high-voltage performance, faster signal transmission and response, reduced electromagnetic interface, and enhanced safety and reliability.

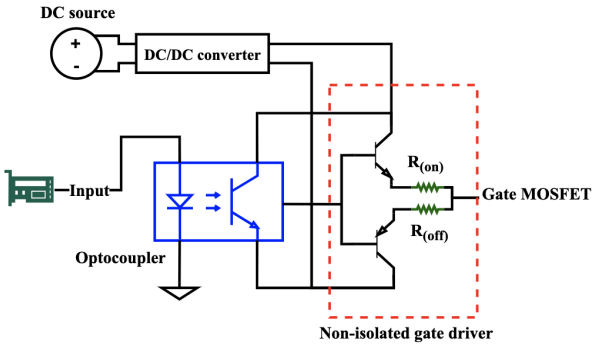


Figure 2. High-voltage gate driver using a high-isolation optocoupler & DC/DC converter, and a non-isolated driver circuit.

The isolated DC/DC converter generating the gate drive voltages has a limited isolation voltage. In HV converters, the auxiliary power supply is usually derived from the submodule voltage, eliminating the need for full isolation to earth [12]. It is also possible to add a tertiary winding to the transformer secondary to power the PE-based components integrated on the HV H-bridge PCB, described in Section 5.

2.3. Over-Current Protection

Typically, during insulation testing, the fast switching capability of the HV-AWG is crucial due to noise reduction, improved thermal management, and accurate simulation of field strength. Using an R_{ext} with approximately 10 kΩ would significantly slow down the t_r of the generated arbitrary waveform. An over-current protection circuit is implemented to prevent the breakdown of HV H-bridge components caused by the high dv/dt and current spikes during sample failure.

The current measurement sensor of the H-bridges and protection circuitry are integrated and used to address the issue of over-current. If the selected current sensor has a wide measurement range (e.g., −20 to +20 A), the measured signal will be noisy, with an inaccuracy of several 100 mA. Since the current rating of the designed HV H-bridge is only 0.2 A, a current sensor with a lower measurement range should be selected. Moreover, the current sensor must provide enough space for the connection cable to pass through and have sufficient sensitivity to detect the over-current pulses. Consequently, the current sensor of type LEM CTSR 0.6-P has been selected, which features a low measurement range of −0.85 A to 0.85 A and a relatively fast response time of 3.5 µs (0 to 90 % response time).

3. Isolated DC/DC Design

3.1. Transformer ZVS Driving Circuit

The ZVS driver was selected for the transformer driving circuit to address the issues of power losses and operational instability associated with hard switching. In hard-switching circuits, MOSFETs switch at high voltage and current levels, leading to significant switching losses and electromagnetic interference (EMI). These losses can degrade performance, especially under varying load conditions. ZVS, on the other hand, ensures that the MOSFETs switch at zero voltage, which reduces the di/dt during the transient period, minimizing EMI and power losses. This contributes to better thermal management and overall system stability. Therefore, the transformer driving circuit should employ a ZVS driver that generates a sinusoidal waveform. This significantly reduces the di/dt during the transient period, thereby decreasing the disturbances on the voltage waveform, which is crucial for accurate HV waveform generation. Additionally, the ZVS driver offers a voltage amplification factor of π.

The ZVS driver is self-oscillating if sufficient input voltage is applied. As the driving circuit starts, one of the MOSFETs is turned on first due to the resistance tolerance range variation in the divider resistors and the difference in MOSFET gate threshold voltages. According to Figure 3, if $V_{GS(1)}$ rises faster than $V_{GS(2)}$, Q_1 reaches its threshold voltage earlier and is triggered faster. Then, $V_{DS(1)}$ reduces and the charges flow through the Schottky diode D_2 instead of the gate of MOSFET Q_2. As a result, $V_{GS(2)}$ is pulled low and $V_{DS(2)}$ becomes larger. Therefore, Q_2 remains off. Due to the LCR resonant circuit shown in Figure 4, at a particular instant, $V_{DS(2)}$ will also be pulled low. The charges will then flow through D_1. Conversely, $V_{GS(1)}$ will be pulled low and Q_1 will be switched off, resulting in an increase in $V_{DS(1)}$. D_2 will be switched off and the charges will be added to the gate of Q_2 through the voltage divider. Thus, $V_{GS(2)}$ rises and Q_2 will be triggered, and the oscillation continues.

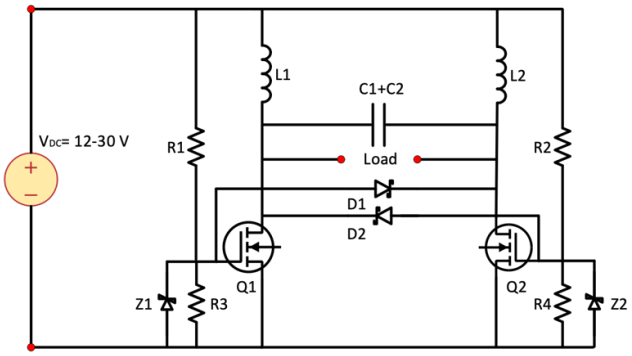


Figure 3. Schematic of the ZVS driver before self-oscillation.

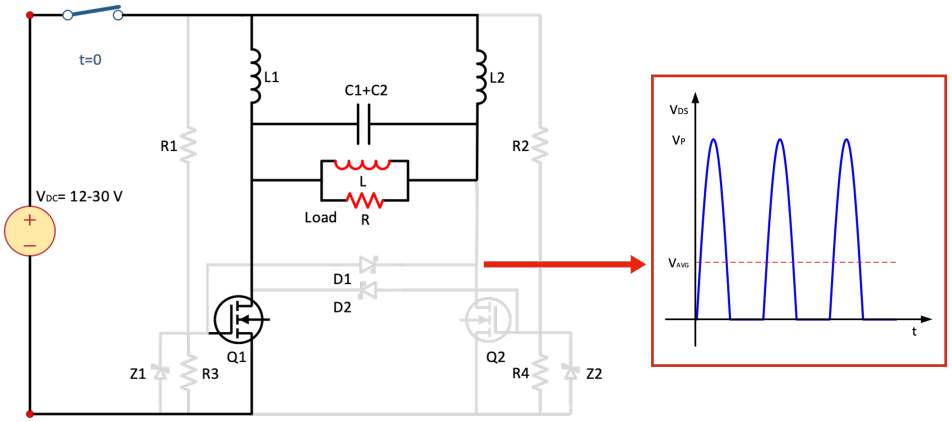


Figure 4. (**Left**): Schematic of the ZVS driver while MOSFET Q_1 is ON and Q_2 is OFF. (**Right**): Drain-source V_{DS} waveform of MOSFET Q_2.

In Figure 4, the driver capacitors C_1 and C_2 have a value of 0.3 µF, leading to a total capacitance C of 0.6 µF. The internal inductances L_1 and L_2 are approximated at 98 µH. When Q_1 is ON and Q_2 is OFF, the resonant circuit can be simplified as shown in Figure 5, assuming the load resistance R is negligible. Its resonant frequency f_o can be derived as follows (7):

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} \cdot \frac{V_{DC}}{s} = \frac{\frac{1}{L_1 C}}{\left(s + \frac{1}{2RC}\right)^2 + \frac{1}{L_{load}C} + \frac{1}{L_1 C} - \frac{1}{4R^2C^2}} \cdot \frac{V_{DC}}{s} \tag{6}$$

$$\omega_o^2 = \frac{1}{L_{load}C} + \frac{1}{L_1 C} - \frac{1}{4R^2C^2} \tag{7}$$

In this study, the input voltage of the ZVS circuit is V_{in}, limited by 35 V_{rms}. The waveform polarity of $V_{DS(1)}$ and $V_{DS(2)}$ is complementary. The average value V_{avg} of the obtained $V_{DS(i)}$ (half-sine waveform) is V_{in}, resulting a peak value of πV_{in}. The voltage applied to the inductive load (transformer primary winding) is a complete sinusoidal waveform. For continuous operation, the input voltage of the ZVS driver should be limited to within 80% of $V_{in(max)}$. As a result, the peak value of the driver output U_p should be 28π.

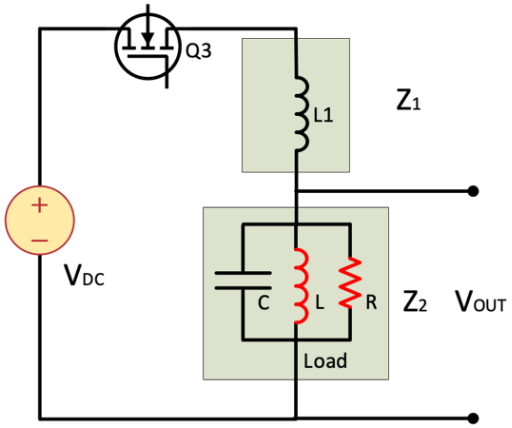


Figure 5. Schematic of the simplified resonant circuit of the ZVS driver while $Q_{1(on)}$ and $Q_{2(off)}$.

3.2. Medium-Frequency Transformer Design

A medium-frequency (MF) transformer is used to step up the voltage generated by the ZVS driver and provide high isolation between the H-bridge stages and the LV driving circuitry. The output of the transformer is rectified to generate the DC link voltage. The target output voltage is 10 kV, which is higher than $N \cdot U_{stage}^{max}$. The working frequency of the transformer is determined by the ZVS driver, which is tuned to operate above the audible threshold at 25 kHz. The specifications of the medium-frequency transformer are provided in Table 1.

Table 1. MF transformer requirements.

Parameter	Value	Unit
Working frequency f_s	≥25	kHz
Secondary voltage U_{sec}	2.7	kV
Isolation voltage U_{iso}	≥10	kV

3.2.1. Transformer Winding Configuration and Core Selection

A split winding configuration (with the windings on two legs of a U-U core) creates sufficient creepage and clearance between the two windings. More insulation material can be placed between the windings to achieve a required isolation level U_{iso}. This configuration has a large leakage inductance, so the secondary voltage drop ΔV is significant. The transformer core should have a large window area but small outer dimensions. According

to Table 2, two Ferroxcube U100/57/25 core halves of material 3C90 ($\mu_i \approx 1900$) are used due to their relatively large window area, compact size, and low price.

Table 2. MF transformer ferrite-core comparison.

Core Shape	Ferroxcube UU100/114/25	TDK UU93/152/30	EPCOS UU126/182/20	
Core size	100 × 114	93 × 152	126 × 182	mm^2
Window area A_w	52 × 68	34.6 × 96	63 × 140	mm^2
Price	33	51	62	EUR/pc

3.2.2. Transformer Primary Number Selection

After selecting the core, the primary number of turns N_p can be selected based on the effective area A_e and saturation flux density B_{sat} of the magnetic core, and the primary voltage $U_{p(max)}$ using (8) and (9). The parameters chosen for the prototype are shown in Table 3.

Table 3. MF transformer prototype parameters.

Parameter	Value	Unit
Source maximum current I_{source}^{max}	≤10	A
H-bridge maximum current I_B^{max}	160	mA
Transformer maximum primary voltage U_p^{max}	$28 \cdot \pi$	V
Minimum saturation flux density B_{sat}^{min}	320	mT

An HV-insulated cable is selected as the primary winding for robust transformer isolation to avoid winding-to-winding and winding-to-core discharges. The cable diameter D_{cable} is 3 mm and the core inner height H_{inner} is measured as 68 mm. As a result, N_p should be larger than 3 but lower than 22. Therefore, N_p is set to 5.

$$N_p \geq \frac{U_p^{max}}{2\pi f_s A_e B_{sat}^{min}} = 3 \tag{8}$$

$$N_p \leq \frac{H_{inner}}{D_{cable}} = 22 \tag{9}$$

The measured inductance of the primary winding is 106 µH with core (L_{load}). The internal capacitance and inductance of the ZVS driver are 0.6 µF (C) and 98 µH (L_1), resulting in a transformer working frequency of around 28 kHz according to (7).

3.2.3. Transformer Turn Ratio Selection

To achieve the desired secondary output voltage from a ZVS driver with limited input voltage, a minimum turns ratio n is required. On the other hand, the transformer secondary current is reflected back to the primary, leading to a maximum n for a current-limited source. From (10), n can be selected as 50. Thus, the number of secondary turns N_s is 250. Referring to (11), the core remains unsaturated with N_s of 250 turns, and the resulting flux density is only 96 mT.

$$\frac{U_{sec}\,[\mathrm{kV_{pk}}]}{U_p\,[\mathrm{kV_{pk}}]} \leq n \leq \frac{I_{source(max)}}{I_{s(max)}} \tag{10}$$

$$\hat{B}_{sec} = \frac{\hat{U}_{sec}}{2\pi f_s \cdot N_s A_e} < B_{sat(min)} \tag{11}$$

3.2.4. Transformer Secondary Winding (Bobbin) Design

To simulate the breakdown performance of the MFT's insulated winding, insulated twisted-wire samples are selected. According to [13], the minimum breakdown voltage of

a single insulated wire layer is approximately 3.5 kV_{pk}, with a testing frequency of around 33 kHz. Considering that the maximum required U_{sec} is only 2.7 kV_{pk}, and assuming a derated permissible breakdown voltage of a single wire layer at 1.5 kV_{pk}, a winding comprising more than two layers can safely withstand the desired voltage. As a result, both the disc-type and layer-type windings are viable options. The disc-type winding is favored due to its superior high voltage capabilities.

For the MFT secondary winding, every disc segment is expected to handle around 1.5 kV. In total, six discs should be provided (to satisfy the desired U_{iso}). Moreover, as seen in Figure 6, an isolation turn is introduced between adjacent winding discs to avoid disc-to-disc discharges. By wrapping this isolation turn around the bobbin, it separates the adjacent discs and makes sure that the last turn of the upper disc segment does not touch all the other layers of the adjacent lower disc segment. The designed bobbin has rounded corners and sufficient disc-to-disc creepage distance to prevent flashovers.

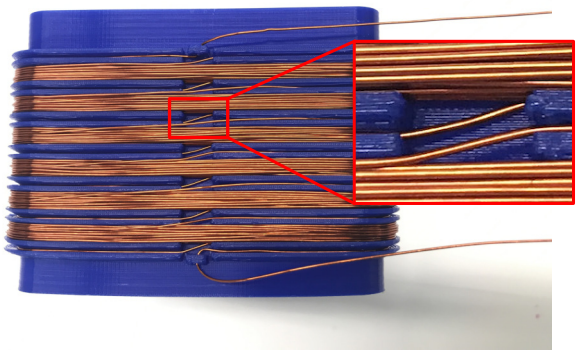


Figure 6. Medium-frequency transformer secondary winding with isolation turns.

3.2.5. MF Transformer Insulation Selection

Typically, transformer insulation system design involves two types of dielectrics: liquid (e.g., transformer or silicone oil) and solid (e.g., epoxy or silicone rubber). While liquid dielectrics offer lower loss and efficient cooling, solid dielectrics present advantages such as allowing for compact insulation systems, resistance to environmental factors (e.g., moisture and contaminants), cleanliness, and eco-friendliness, along with higher thermal conductivity κ.

Based on the Steinmetz Equation (12), the loss of the transformer core of type 3C90 can be calculated. The values of the parameters ($k = 5.69$, $\alpha = 1.46$, and $\beta = 2.75$) are all obtained from the manufacturer. The obtained maximum core loss at room temperature 25 °C is around 7 W.

$$P_{l(core)} = k f_s^{\alpha} B_{sec}^{\beta} V_e \tag{12}$$

$$P_{l(winding)} = R_{AC} I_{s(max)}^2 \approx 0.4\,W \tag{13}$$

The total transformer winding loss can be calculated by (13). It can be noted that R_{AC} is measured from Bode-100 with a value of 15 Ω and the obtained winding loss is around 0.4 W. Since the total power rating of the designed transformer is around 7.4 W, the considerations regarding loss and heat dissipation cannot be simply disregarded. According to the findings shown in Table 4, if solid-type dielectrics are favored, silicone rubber emerges as the preferred choice owing to its comparable lower loss $\tan\delta$ [13], superior thermal conductivity, and ease of preparation and casting. These properties make it an ideal choice for the MFT used in the arbitrary waveform generator. In HV applications, ensuring sufficient creepage and clearance distances between the windings is crucial, and silicone rubber's flexibility and ease of preparation allow for compact insulation systems while still providing the necessary dielectric strength.

Table 4. MF transformer insulation properties obtained from Novo-control measurement [13].

Material	ϵ_r	**tan** δ $[10^{-4}]$ **@ 10 kHz**	κ **[W/(mK)]**
Epoxy CY225	2.8	100	0.21
Silicone rubber	3.1	25	0.30

In [13], the twisted-wire samples insulated with silicone rubber are verified to exhibit higher breakdown voltages compared to those cast in epoxy resin. This result substantiates the appropriateness of silicone rubber as the preferred insulation material. The twisted-wire samples are employed to simulate transformer disc wires, which have multiple points of contact, thereby simulating real-world operational conditions.

3.2.6. Transformer Bobbin Cup and Bushings

The transformer secondary winding is positioned within the bobbin cup, illustrated in Figure 7, which features grooves to accommodate the secondary turns and guides for the connection cables and secondary wire terminals. The bobbin cup geometry incorporates an inner cavity designed to accommodate the core. Additionally, an air gap of 17 mm is maintained between the core and the main compartment, which houses the secondary windings. According to the findings in [14], the breakdown voltage of air at 57 kHz is reduced to 66% of the standard air breakdown voltage of 3 kV/mm. Under the assumption of worst-case operating conditions, the air breakdown voltage is conservatively set at 0.6 kV/mm. The designated air gap is sufficient to sustain the insulation requirement of 10 kV, when the core is grounded. This gap plays a critical role in minimizing the risk of discharge between the windings and the core. The output terminals of the secondary windings are attached with the connection cables, going through the extended part of the bobbin cup. The main compartment is filled with silicone rubber to generate the required isolation.

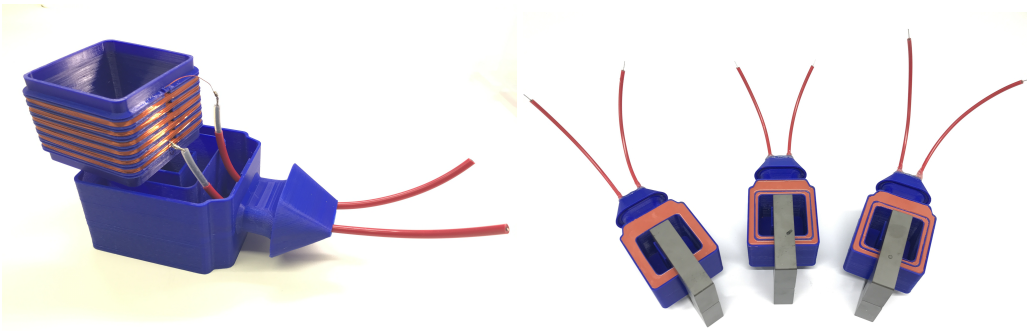


Figure 7. MFT secondary winding before silicon rubber casting (**left**) and after casting (**right**).

4. Experimental Results

Figure 8 illustrates the non-breakdown experimental configuration of the three-stage CHB-based HV-AWG. The setup includes a 10 kV MFT that provides galvanic isolation between primary and secondary sides. The output voltage from the MFT is subsequently rectified by the 6 kV, 1 A rectifiers and then stabilized using a 3 kV, 1.0 µF capacitor. This stabilized voltage is then supplied to a series of cascaded HV H-bridge modules, which are responsible for synthesizing the desired arbitrary waveforms.

In this configuration, the medium-frequency transformers ensure safety and isolation by preventing direct electrical connection between the high-voltage output and the low-voltage control circuitry, thereby protecting sensitive components. The rectification and stabilization process involving the capacitor smooths out voltage fluctuations, ensuring a consistent HV output for subsequent stages. The cascaded HV H-bridge modules

then modulate this HVDC into complex AC waveforms as required for the application, leveraging the high switching speed.

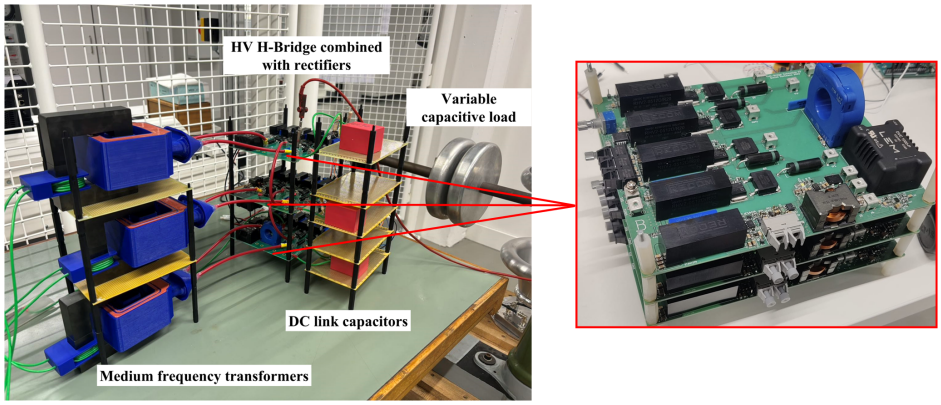


Figure 8. The experimental set-up of the 3-stage modular CHB-based HV-AWG.

As illustrated in Figure 9, the customized waveforms—namely stair (triangle), saw-tooth, pulse, and complex shapes—are generated with a peak voltage of around 8.1 kV and frequency f_{sw} of 1.5 kHz. The output waveforms exhibit up to seven distinct voltage levels. According to Figure 10, achieving an output voltage range from 0 to 8.1 kV with a load of 40 pF (plus an additional 20 pF for the measuring probe) results in a t_r of approximately 1.2 µs. In contrast, under no-load conditions, the t_r is reduced to approximately 800 ns. By modifying the input signals, it is possible to obtain the desired high-voltage waveforms with specific shapes.

Switching and conduction power loss analysis: The output waveform of this three-stage CHB-based HV-AWG is determined as centro-symmetric and repetitive. The total switching energy loss per half cycle $E_{tot,0.5pt}$ can be computed using Formula (14), where K represents the number of switching transients per half cycle. V_i denotes a specific step voltage in the HV-AWG output waveform, while $V_{(i+1)}$ stands for the adjacent step voltage following V_i.

$$E_{tot,0.5pt} = \frac{1}{2} * (C_{DUT} + C_{par}) * \sum_{i=1}^{K} |V_{(i+1)}^2 - V_i^2| \tag{14}$$

The total switching power loss of the Si MOSFETs $P_{tot(sw,MOS)}$ can be calculated using Formula (15), where $E_{tot,pt}$ denotes the total switching energy loss per cycle.

$$P_{tot(sw,MOS)} = E_{tot,pt} * f_{sw} = 2 * E_{tot,0.5pt} * f_{sw} \tag{15}$$

$$P_{tot(cd,MOS)}^{max} = 2N * R_{DS,on} * \left[2\pi * f_{sw} * (C_{DUT} + C_{par}) * U_{out}^{max}\right]^2; N = 3 \tag{16}$$

The maximum total conduction power loss $P_{tot(cd,MOS)}^{max}$ can be calculated according to Formula (16), where N is the number of stages within HV-AWG. Based on the obtained experimental results, the value of $P_{tot(cd,MOS)}^{max}$ is computed as 79 mW.

During the half-switching cycle, if the output waveform of the HV-AWG is designed to rise from 0 V, reach its peak value U_{out}^{max}, and then return to 0 V, as illustrated in cases (a–c) of Figure 9, these configurations result in a lower $P_{tot(sw,MOS)}$ compared to case (d). The $P_{tot(sw,MOS)}$ for cases (a–c) is calculated to be 11.8 W. However, that for case (d) is 18.37 W. Consequently, the conduction loss in the Si MOSFETs is negligible in comparison to the switching loss. To prevent thermal breakdown during switching, it is critical to employ a heat sink with low thermal resistance to ensure effective heat dissipation.

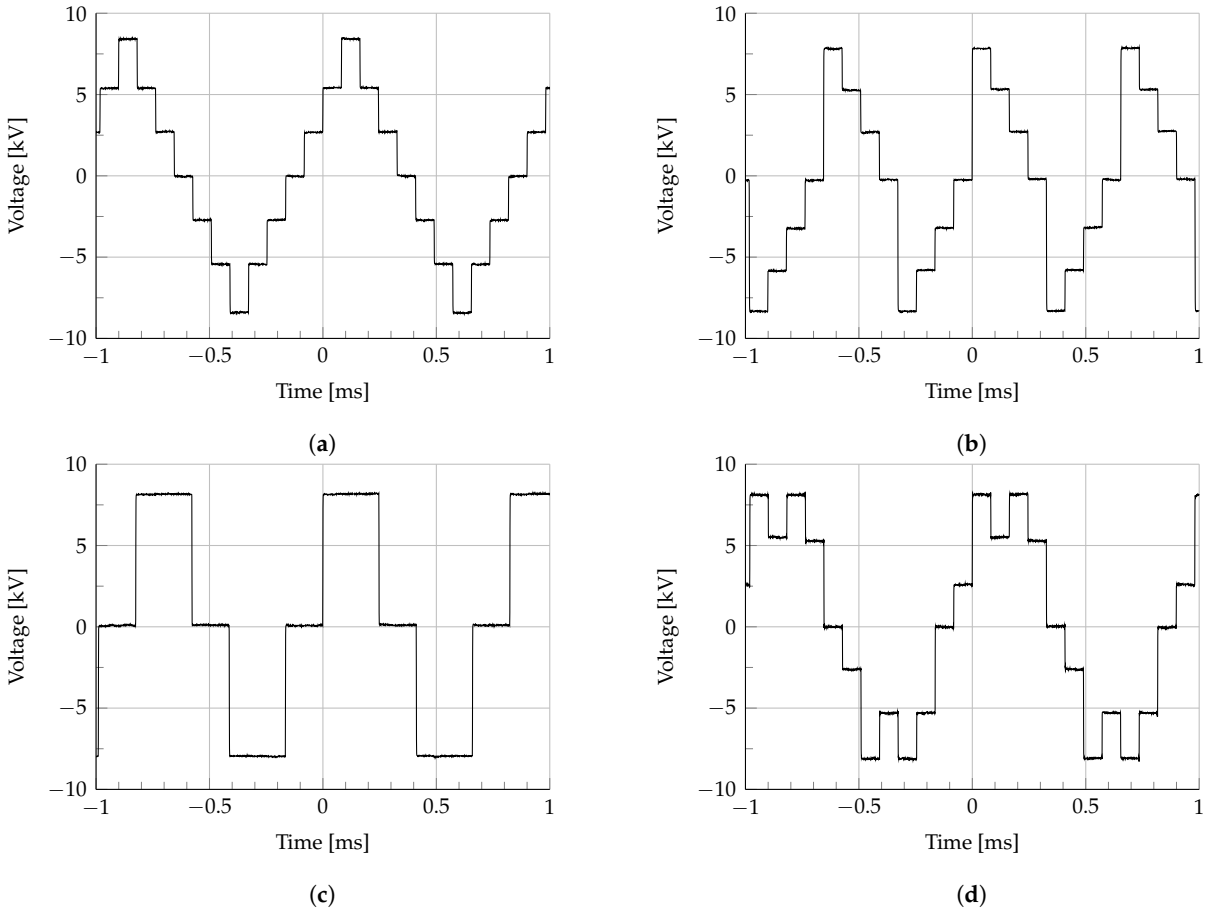


Figure 9. Customized output waveforms of the 3-stage modular CHB-based HV-AWG. For waveform (**c**), three H-bridge stages are controlled as a single stage. (**a**) Triangular staircase waveform. (**b**) Sawtooth-shape staircase waveform. (**c**) Three-level square waveform. (**d**) Complex-shape staircase waveform.

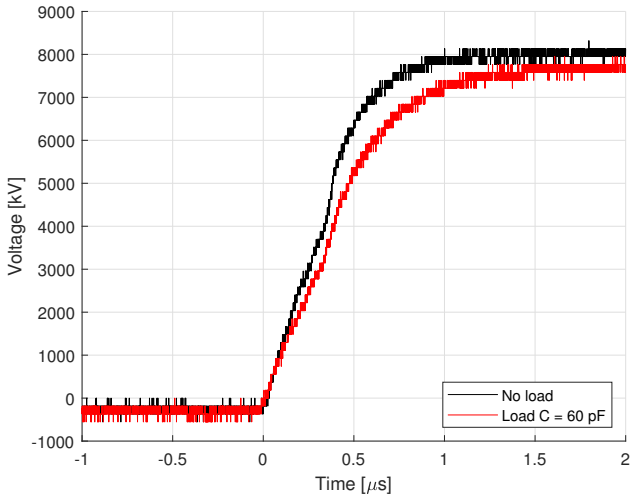
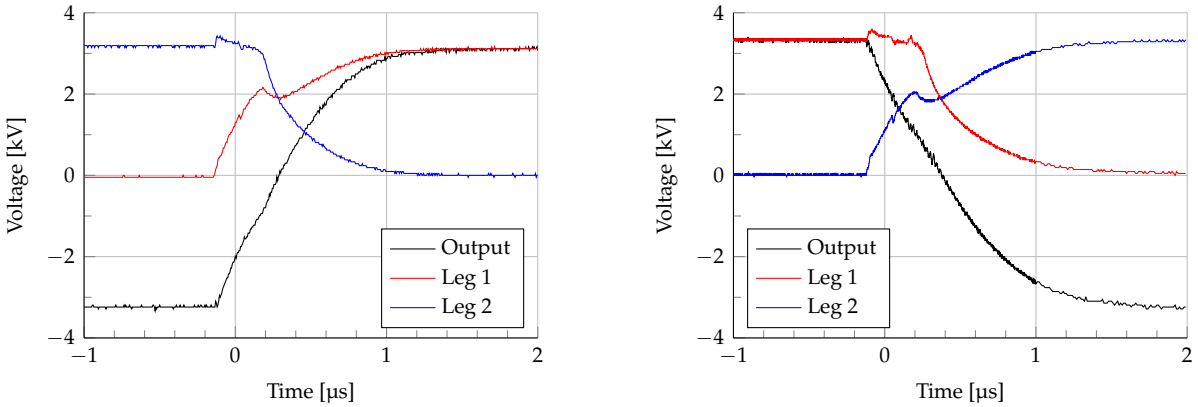


Figure 10. Comparison of the case in Figure 9b,c without load and with 60 pF load.

5. Discussion

For each individual HV H-bridge module, with a total load C_{DUT} of 60 pF (including 20 pF for the measuring probe), the voltage applied to the test object can be increased to ± 3.2 kV. As shown in Figure 11, the rise and fall times of the HV H-bridge are approximately 800 ns (without R_{ext}), resulting in a maximum current peak adjacent to, but less than

0.6 A. Therefore, the H-bridge validation voltage is limited to 3.2 kV. Exceeding this voltage during switching transients causes the current to surpass the I_{DM}^{max}, potentially damaging the MOSFET layout.



(**a**) (**b**)

Figure 11. Output and phase leg waveforms for one H-bridge with 3.2 kV DC voltage and 80 pF load (60 pF for C_{DUT} and 20 pF for C_{par}). (**a**) HV H-bridge output voltage rise duration; (**b**) HV H-bridge output voltage fall duration.

Output voltage scalability: In the prototype design, the optocouplers and auxiliary DC/DC converters are subjected to the entire output voltage U_{out}, if the H-Bridge module is positioned near the HV output and the submodules are all connected with copper wires to a controller. Typically, the selected DC/DC converters of type RHV2-0512D and optocouplers of type OPI1268S provide isolation up to 12.5 kV AC for only 1 minute. For extended insulation testing periods, the U_{out}^{max} of the HV-AWG should be around 7.5–8 kV, considering a 40 % safety factor. Therefore, even though the HV-AWG submodule has been validated to achieve a higher output voltage (3.2 kV per submodule, corresponding to an output voltage of almost 10 kV), it is not yet possible to run it at this voltage for prolonged periods.

To achieve a higher HV-AWG output voltage, isolated DC/DC converters and optocouplers with higher isolation ratings are required. However, such components are expensive and bulky. To enhance the control system and scalability of the CHB-based HV-AWG, fiber-optic communication can be adopted to improve signal integrity and electromagnetic interference immunity, while enabling distributed control across modules. This approach also offers galvanic isolation between the HV H-bridge modules and the LV control system, eliminating the need for optocouplers capable of withstanding high voltages. By using a Typhoon HIL to control all H-bridge modules, system complexity and risk are further reduced. Addressing thermal management, signal attenuation, and insulation reliability challenges ensures that the generator can meet the demanding requirements of high-voltage applications more effectively.

Additionally, a tertiary winding can be incorporated on the secondary side of the MFT and encapsulated in silicone rubber. When combined with a rectifier and a buck converter or linear regulator, this tertiary winding provides power to the control circuitry of the H-bridge. This modification eliminates the need for an auxiliary DC/DC converter with a higher insulation level (the selected DC/DC converter only needs to handle the maximum stage voltage U_{stage}^{max}). As a result, the scalability of the CHB-based HV-AWG system can be significantly improved. But all the MFTs should be able to handle the full output voltage U_{out}.

Semiconductor device selection: Choosing another type of HV MOSFET with larger pulsed and continuous drain current ratings is advisable. This choice accommodates a broader range of the testing load C_{DUT}^{max}. Additionally, it allows for achieving lower values of R_{tot} and t_r. For the lifetime considerations of the HV-AWG, the MOSFETs with lower $R_{DS,on}$

are recommended. Higher $R_{DS,on}$ values result in large losses within the semiconductor device, making heat dissipation more challenging. An external current limiting resistor R_{ext} is recommended to limit the t_r and current since this can be cooled more effectively. For example, the Si MOSFETs of type IXTT1N450HV with $I_{D25}^{max} = 1$ A, $I_{DM}^{max} = 3$ A, and $R_{DS,on} = 85\,\Omega$ could be selected.

Current sensor selection and protection circuit design: Faulty operation of the protection circuitry can be prevented by selecting a current sensor with reduced sensitivity, particularly when the maximum allowable current of the H-bridge protection circuit (I_{HB}^{max}) is less than the peak drain current of the H-bridge during switching transient ($I_{d,pk}^{max}$). However, with the availability of a Si MOSFET that possesses a higher maximum drain current (I_{DM}), the I_{HB}^{max} can be increased. Consequently, this adjustment mitigates the risk of mis-operation, provided that the maximum capacitance (C_{DUT}^{max}) and maximum output voltage (U_{out}^{max}) remain unchanged. It is advisable to select a current sensor with greater sensitivity to enhance fault detection speed and prevent thermal breakdown of the H-bridge components.

6. Conclusions

A three-stage CHB-based HV-AWG has been designed and validated to generate customized arbitrary waveforms (sawtooth, triangular, pulse, and complex) with peak voltages of around 8 kV. The prototype stands out for its simple design, low manufacturing cost, excellent HV performance, and potential for extending the number of stages. Silicon MOSFETs with a maximum blocking voltage of 4.5 kV are used to simplify the design of the HV H-bridge module and reduce cost. Optocouplers and non-isolated gate drivers are utilized to create the corresponding HV gate drivers. A transformer with a split winding configuration, insulated with silicon rubber, creates the isolated DC link voltage of the CHB modules. An isolation turn is placed between adjacent transformer secondary discs to prevent disc-to-disc discharges, effectively mitigating discharges and allowing the transformer to withstand more than 10 kV. A commercially available ZVS driver is also selected to drive the transformer properly. PD-free measurement equipment is necessary to achieve a non-distorted and stable HV output. Measurements show rise times on the order of 0.8 µs when switching all CHBs in a single stage. Switching waveforms are smooth and without overshoot, allowing accurate waveform reconstruction.

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Abbreviations

The following abbreviations are used in this manuscript:

HV	High voltage
PE	Power electronics
MF	Medium frequency
HF	High frequency
MMC	Modular multilevel converter
CHB	Cascaded H-bridge
AWG	Arbitrary waveform generator
ZVS	Zero-voltage switching
MFT	Medium-frequency transformer
LV	Low voltage
HP	High power
OC	Over-current

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