Data acquisition system for sub-sea instrumentation

Designing and testing a high-pressure-tolerant precision data acquisition system

Bachelor graduation project electrical engineering

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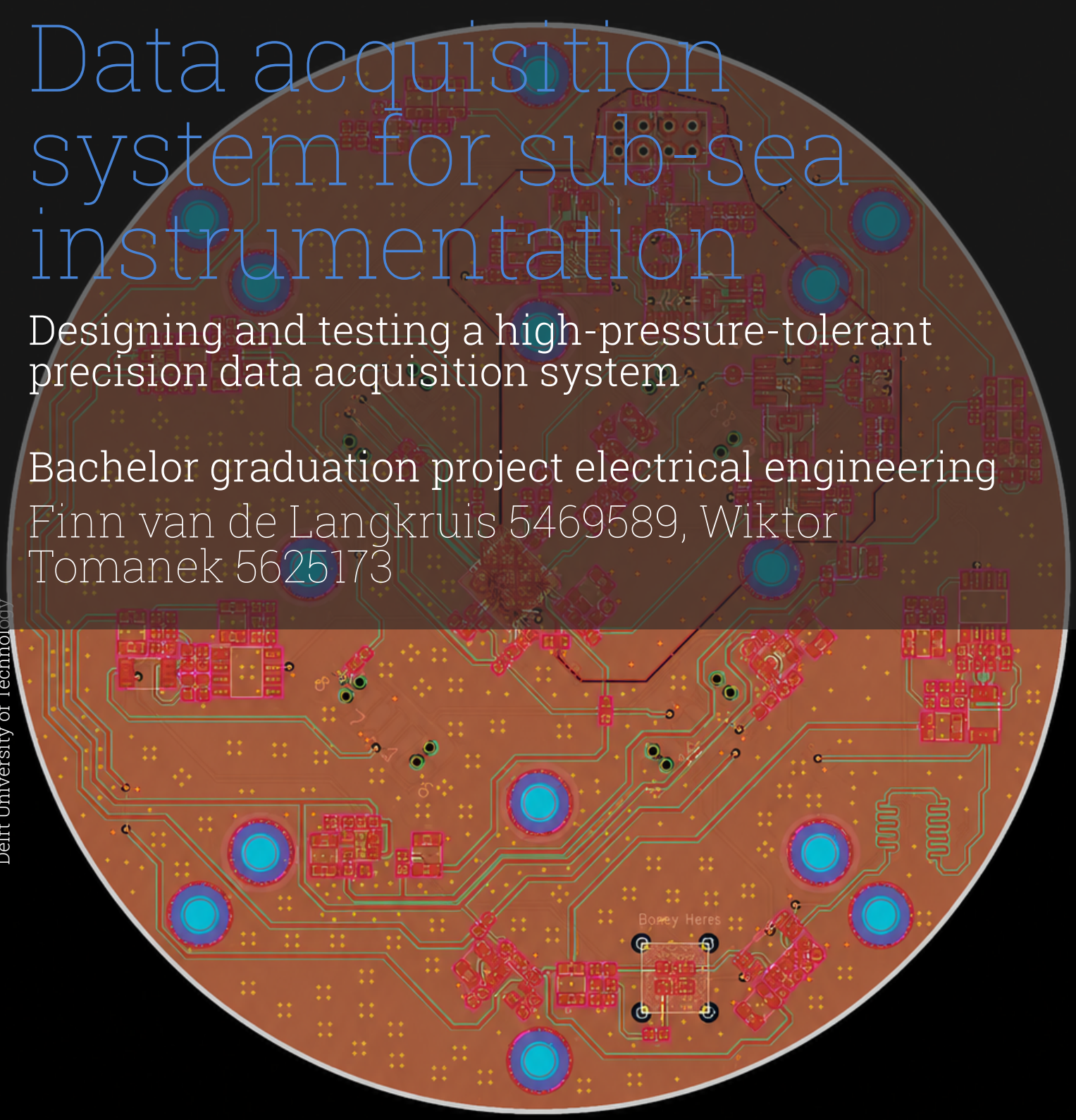

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Abstract

This report describes the design, building and testing of a high precision data acquisition system that is able to function in high pressure environments. The system uses an FPGA as its controller sending and receiving information to and from a data conversion device with the AD4630 as its ADC and the DAC8811 as its DAC. The system is tested in a pressure chamber which was pressurised up to 500 bars of pressure and the performance difference was found to be negligible. The system had to be proven to be scalable to 16 channels and these 16 channels had to fit inside a volume of $100cm^3$.

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Part I

Problem Definition

1

Introduction

1.1. Background

Precision data acquisition systems are a critical component in a wide range of industrial and scientific applications. In many of these applications, performance alone is insufficient — the system must also operate reliably under demanding physical conditions. Harsh environments such as high-temperature industrial processes, aerospace deployments, and subsea installations impose constraints that go far beyond what standard laboratory instrumentation is designed to handle. Meeting the performance specification is only half the challenge; doing so under the operating environment is the other.

Subsea deployment presents a particularly demanding set of constraints. Hydrostatic pressure increases with depth, subjecting all electronics to mechanical stress that can shift component parameters and degrade signal integrity. Existing high-precision DAQ[1] systems capable of meeting stringent distortion and dynamic range requirements are predominantly designed for laboratory use and have not been characterized under hydrostatic pressure. Where pressure protection is applied, it typically requires bulky sealed enclosures that are incompatible with compact, weight-constrained platforms. There is no compact DAQ system that combines this level of signal quality with verified performance under subsea pressure conditions.

1.2. State-of-the-art analysis

Several commercial DAQ systems address parts of the problem. Spectrum Instrumentation offers the hybridNETBOX, a combined DAC and ADC solution with Ethernet connectivity, as well as PCIe variants for high-throughput applications[1]. Scopefun provides an open-source platform with a USB 3.0 interface, though it is limited to acquisition only with no signal generation capability[2]. SIRIUS offers a 24-bit ADC solution targeting precision measurement[3], and National Instruments provides a multi-channel solution combining a 20-bit ADC at 250 kSps with a 16-bit DAC[4]. Hybrid systems that combine both generation and acquisition in a single platform are relatively uncommon; the market is largely served by separate oscilloscope and arbitrary waveform generator products. Despite their differences, these solutions share a common architectural pattern. An FPGA acts as the central controller, managing the converter interfaces and handling communication to the host PC over Ethernet, PCIe, or USB. This architecture is well-established and forms the basis of the design presented in this report. None of the listed solutions, however, satisfies the full set of requirements. The signal quality and sample rate targets of this project are at the boundary of what currently available converter ICs can achieve according to email contact with Analog devices. More importantly, none of these systems has been characterised under hydrostatic pressure, and their physical form factors are too large for compact subsea platforms. A system that combines the required performance, compact form factor, and verified behaviour under pressure does not yet exist.

[1] Data Acquisition

1.3. Project Objective

The objective of this project is to design a compact, high-precision data acquisition system capable of both signal generation and acquisition, and to characterise its performance under hydrostatic pressure.

The system must meet the signal quality requirements identified as missing from existing solutions, achieving sample rates of at least 2 MSps, distortion levels below -100 dB, and a dynamic range exceeding 160 dB/Hz, all within a single unified system. The full set of system requirements is defined in Chapter 2.

To evaluate its behaviour under realistic operating conditions, the system was tested inside a pressure chamber, providing a controlled environment that replicates the hydrostatic conditions of subsea deployment. The result is a fully characterised DAQ system whose performance under pressure is documented and verified against its specifications.

1.4. System Overview

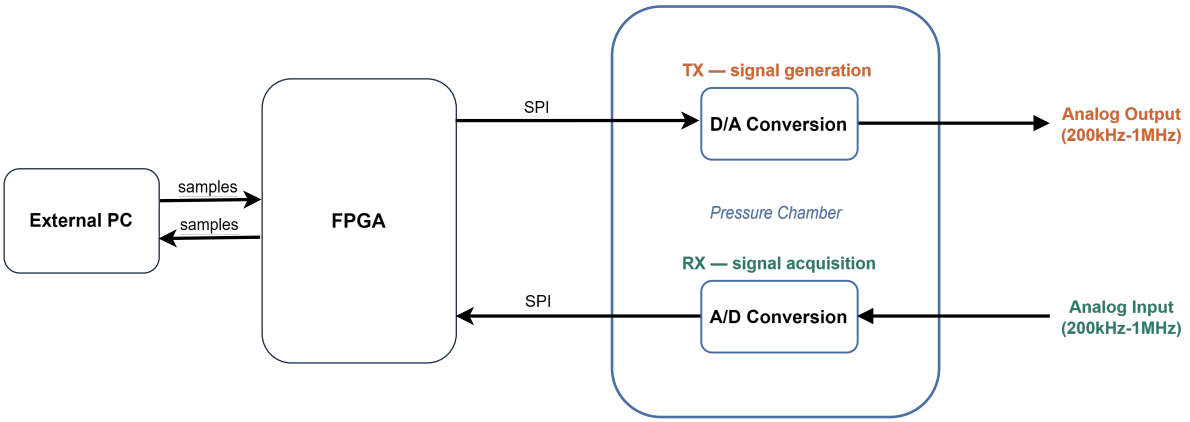


Figure 1.1: High-level DAQ system overview.

The system consists of two physically separated parts, as shown in figure 1.1. The first is a PCB containing the converter ICs and their surrounding circuitry, which is placed inside the pressure chamber and subjected to hydrostatic pressure during testing. The second is the communications and control side, comprising an FPGA and an external PC, which remain outside the chamber. The FPGA drives the converters and manages the data flow between the PC and the converter ICs.

The system operates in two directions. In the transmit path, digital samples are generated by the PC, sent to the FPGA, and converted to an analog signal by the DAC. In the receive path, an analog signal is sampled by the ADC, and the resulting digital data is sent back through the FPGA to the PC.

1.5. Project Structure

The task of this project is divided across three subgroups:

- **The control group** is responsible for the communication link between the external PC and the FPGA, including Ethernet protocol handling and data buffering
- **The circuit design group** handles the analog front-end, including the converter circuitry, voltage references, and PCB layout
- **The interface group** designs the digital interface between the FPGA and the converter ICs, covering the SPI masters, clock architecture, and synchronisation

The work of each subgroup is documented in a separate thesis, which together provide a complete account of the full system design.

2

Program of requirements

In this chapter the program of requirements will be discussed. First the functional requirements will be given. This is what the product must do if the product is finished. Then the non-functional requirements will be given. These are the bounds which the product should comply to. At last the constraints of the project will be discussed.

2.1. Functional requirements

These are the functional requirements of the system:

- The system is able to convert a digital data stream to an analog signal;
- The system is able to convert an analog signal to a digital data stream;
- The system is able to do digital-to-analog conversion and analog-to-digital conversion at the same time;
- The system is able to stream the data or have a one-second buffer;
- The system should have at least 2 different channels working and have an architecture that is scalable to up to 16 channels;
- The system is able to be tested under high pressure.

2.2. Non-functional requirements

Table 2.1: Non-Functional Requirements

ID	Requirement	Target / Description
R1	Sample rate	≥ 2 MS/s
R2	Dynamic range	≥ 160 dB/Hz
R3	Bandwidth	≥ 1 MHz
R4	Total harmonic distortion	$\text{THD}_{BW} < -100$ dB
R5	Data handling	Stream data or provide a 1-second buffer
R6	Number of channels	At least 2 channels
R7	Channel scalability	Scalable up to 16 channels
R8	User interface	Python or C(++) script

2.3. Project constraints

Table 2.2: Constraints

ID	Constraint	Limit / Condition
C1	Physical volume	$\leq 100\ \text{cm}^3$
C2	Development time	10 weeks
C3	Pressure rating	500 bar
C4	Operating temperature range	−20°C to +85°C

Part II

Design

3

Design Methodology

The development of the DCD and external breakout boards was originally intended to follow a rapid prototyping approach. In such a workflow, the design is implemented in several iterative cycles, where each version of the hardware is used to verify functionality, identify problems, and refine the next revision before reaching a final design. This method is especially useful in hardware development, because it allows the designer to detect issues in schematic choices, PCB layout, grounding, noise performance, connector placement, and assembly before committing to a final implementation.

For this project, rapid prototyping would have meant building an initial prototype of the circuit, testing the most critical functions, and then incorporating the results into a revised second or third prototype. In particular, this would have been useful for validating the analog performance of the DAC and ADC sections, the power supply rails, the signal integrity across the pressure-chamber connection, and the interaction between the FPGA and the DCD board. By iterating in this way, weaknesses in the design could have been corrected early, reducing the risk of problems in the final system.

However, due to the time constraints of the project, the development process was adapted to a more compressed approach. Instead of producing multiple prototype revisions, the design was moved directly toward one final prototype that combined the most important requirements from the beginning of the project. This final prototype was therefore designed to be as complete and representative as possible, so that it could function both as a proof of concept and as the basis for testing the system's performance. In practice, this meant that more effort had to be invested in upfront design decisions, simulation, component selection, and PCB layout, since there would be less opportunity to correct mistakes in later iterations.

Because only one prototype revision was feasible, several design choices were made conservatively. Components were selected based not only on performance, but also on availability, robustness, and implementation simplicity. For example, ready-made integrated circuits were preferred over custom solutions when they met the required specifications sufficiently well. This reduced development time and avoided unnecessary complexity in the analog and digital interface sections. Likewise, the PCB layout was designed with extra attention to grounding, decoupling, and connector compatibility, since layout errors would be difficult to correct after fabrication.

The decision to proceed directly to a final prototype did reduce the flexibility typically provided by rapid prototyping, but it also reflects a realistic constraint in hardware development. Unlike software, where changes can often be made late in the process, hardware revisions require new boards, new assembly, and new verification cycles, which are costly in both time and resources. For that reason, a large part of the development effort in this project was spent on minimizing design uncertainty before fabrication. The result was a final prototype that was intended to be sufficiently mature for testing

without requiring intermediate validation boards.

Even though the process did not include multiple hardware iterations, the design still benefited from the rapid prototyping mindset. The project remained focused on early validation of the most critical technical risks, especially analog performance, pressure-chamber compatibility, and interfacing between subsystems. The main difference was that these risks had to be addressed through analysis, calculations, and careful design decisions rather than through successive physical prototype revisions. As a result, the final prototype represents the outcome of a compressed development cycle in which rapid prototyping principles were applied conceptually, but implemented in a single hardware revision.

4

Circuit Design

As mentioned previously in the introduction, the prototype system was implemented in a way to be able to verify its performance with the use of the pressure chamber provided by the company for which the data acquisition system was made. Therefore, a decision was made to implement the circuit using the printed circuit board (PCB) templates provided by the host, which allow for mounting of the whole system on the pressure chamber.

The circuit was designed so that all of the specifications could be tested using the loopback method, thus feeding the ADC with a signal generated by the DAC, or, if possible, using external measurement tools. Figure 4.1 shows the top-level ideological overview of the circuit board that will be tested inside the pressure chamber, from this point called the Data Conversion Device (DCD) board. It can be noted that this overview follows the top hierarchical level of the detailed schematic diagram in the appendix B

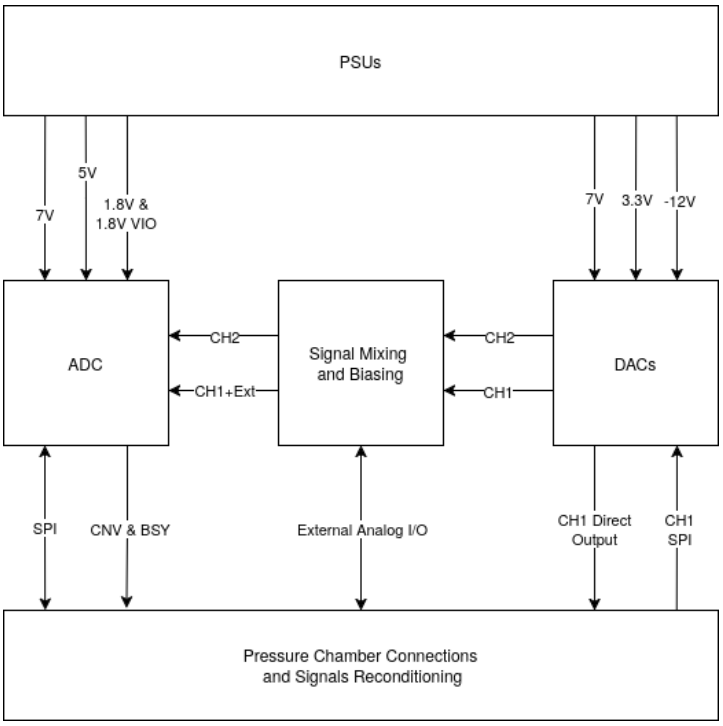


Figure 4.1

Both the ADC and DAC were placed on the same DCD circuit with the intention of testing them

simultaneously in the pressure chamber. The decision to proceed with this approach and skip potential subrevisions was made due to the time constraints of the project, as described in the design methodology section. By moving directly to a single final prototype, the development process was compressed, but this also required that all critical design decisions be made early and that the board be as complete and testable as possible from the first fabrication.

The signal mixing and biasing section was implemented as a simple summing node using resistors. This design choice allowed the circuit to accept either an external signal or the stimulus from the DAC, thereby enabling a loopback test of the ADC without requiring very high-precision external signal sources. The loopback approach significantly reduces the need for advanced measurement equipment, since the DAC itself provides a known test signal that can be used to characterize the ADC's performance. However, to achieve more accurate and detailed characterization, a spectrum analyzer will still be used. The model of the spectrum analyzer is the Siglent SSA3021X, which has a frequency range from 9 kHz up to 2.1 GHz. This range is well within the bandwidth requirements of our system, ensuring that the analyzer can capture the relevant spectral content for THD+N, dynamic range, and harmonic distortion measurements.

Channel 2 is only accessible on a separate header on the board. This header was included to allow testing of the system with two channels running simultaneously, which would be useful for validating multi-channel behavior during development. However, running two channels simultaneously is not necessary for testing in the pressure chamber. Furthermore, the pressure chamber only has 16 connections going out of it, and it was not possible to route both channels through these limited connections. Therefore, only channel 1 will be used for the pressure chamber tests, which is sufficient to verify the performance of the system under high-pressure conditions.

Components chosen for circuit design in this chapter if not mentioned specifically in the text of this chapter can be found in Appendix I.

4.1. DCD

4.1.1. ADC

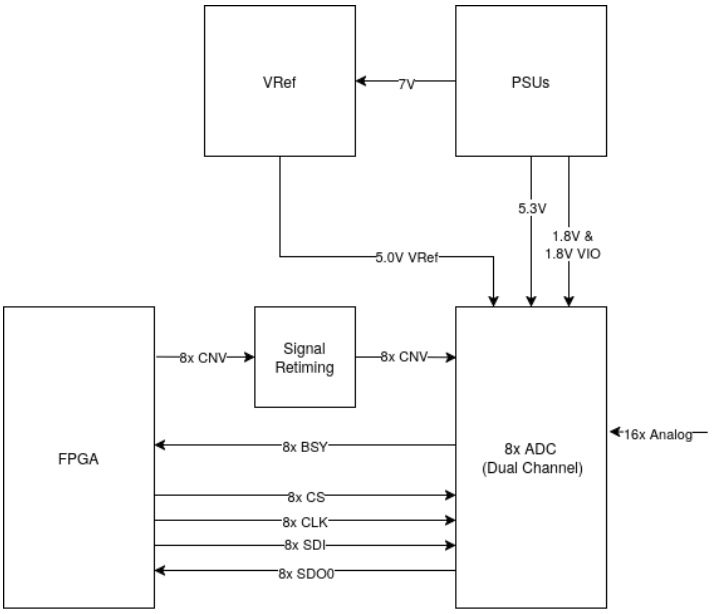


Figure 4.2: ADC subsystem

The ADC section of the DCD board is shown in Figure 4.2. It was designed for all 16 channels in the full system, but for the DCD prototype, the design was scaled down by a factor of 8 so that only 2 channels

were implemented. This allowed the same architecture to be tested in a reduced form while keeping the prototype practical in terms of board space, routing complexity, assembly effort, and price.

A key part of this section is the signal retiming circuit. Its purpose is to synchronize the conversion (CNV) signal, which triggers sampling, with the clock source on the DCD board. That same clock is also distributed to the DAC and out to the FPGA, so that all parts of the system operate from a common timing reference. This was done to achieve very low jitter, on the order of X ps, and to ensure that the ADC and DAC can be synchronized so they sample and update at the same time. The circuit itself was designed in detail by the interfacing group, while our group implemented it on the circuit board; the detailed explanation is therefore given in their report.

The ADC was implemented using the AD4630, which was chosen because it is a top-end converter from Analog Devices and outperforms the alternative parts that were considered. It also includes built-in bypass capacitors, which simplified the surrounding implementation significantly. As a result, the external circuitry mainly consisted of input filtering using first-order low-pass filters, which can also be implemented digitally if needed, and ferrite beads on the digital lines to keep EMI low. The detailed circuit design is shown in the appendix B.

An important design consideration for this chip was the separation of the digital and analog grounds. These were kept separate throughout the board and connected at a single point through a ferrite bead to reduce noise coupling between the two domains. This is especially important in a mixed-signal converter design, where digital switching noise can directly affect analog performance if the return paths are not controlled properly.

The AD4630 was selected not only because it meets the required specifications, but because it significantly exceeds them in several respects. A detailed comparison between this chip and the other converters that were considered is included in the appendix C, where the relevant specifications can be found side by side. This comparison was important in the selection process, since it justified using a higher-performance part than the bare minimum required by the design.

One of the main reasons this ADC section was considered critical for pressure testing is the complexity of the device itself. The AD4630 uses a BGA package and integrates internal capacitors, which makes it more mechanically and thermally complex than a simpler packaged part. That combination means it could be vulnerable to pressure-related failure, either through package stress, solder joint failure, or internal damage. For that reason, the ADC section was one of the most important parts of the DCD board to validate in the pressure chamber. The risk of damaging this chip was also accepted since the raster of its BGA package is relatively big and equal to 0.8 mm, so it has a high chance of surviving the pressure.

4.1.2. DAC

The schematic for two channels of the DAC part of the DCD is shown in Appendix E Figure E.1.

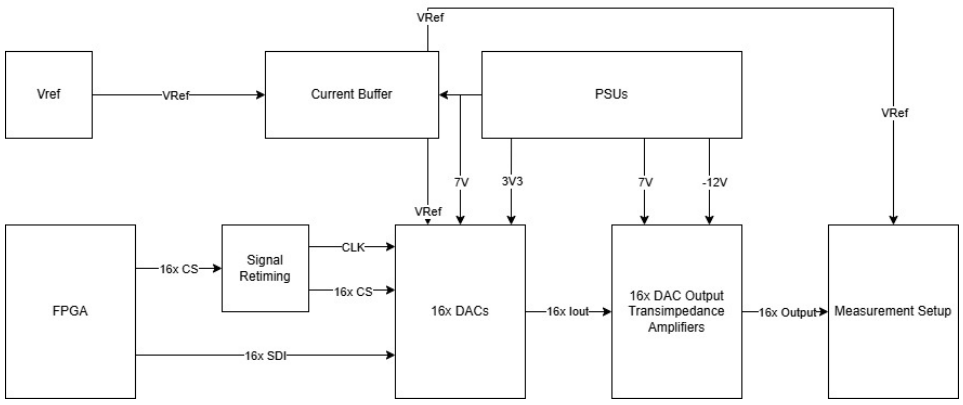


Figure 4.3: DAC circuit layout

Figure 4.3 shows the general layout for the DAC circuit for all 16 channels. For the testing, however, only

two channels are used, but Figure 4.3 shows which parts of the DAC circuit should be scaled when the number of channels is increased to 16.

The DAC used in this design is the DAC8811 from Texas Instruments [5]. Other DACs were considered as shown in Appendix C, but this specific DAC was chosen because of its high dynamic range density, which is close to the required 160 dB/Hz, and its THD of around -100 dB, while meeting the other required specs. These specs are in the datasheet, evaluated at 1kHz instead of 1 MHz, but since this is one of the best ready-made DACs within the required specs range for the data acquisition system, it was deemed sufficient. There were some DACs with comparable specs, but they were far more complex, requiring a JESD204 [6] serial interface instead of SPI, which would compromise other specs and constraints of this project, as the space limitation of the system scaled to 16 channels and the time constraint of the project. The dynamic range density was calculated to be 175.4dB/Hz, and the dynamic range was calculated to be 145.4 dB at 1MHz, both at a full-scale reference voltage of $V_{ref} = 10V$, which, given the rest of the specs needed for the DAC was chosen to be sufficient as designing and building a DAC would have taken too much time for this project. The actual calculations for the dynamic range are as follows: the output spot noise voltage is $e_n = 12nV/\sqrt{Hz}$ at 1 kHz, as can be found in the datasheet [5]. In dB this becomes $e_n = 20 \cdot log_{10}(12 \cdot 10^{-9}) = -158.4dBV/\sqrt{Hz}$. The full scale output voltage with $V_{ref} = 10V$ is $V_{FS} = 10V$ which gives the rms voltage $V_{FSrms} = 10/\sqrt{2} = 7.071V$ rms, which in dB is $V_{FSrms} = 20 \cdot log_{10}(7.071) = 17.0dBV$. The dynamic range density now becomes:

$$DR = V_{FSrms}(dBV) - e_n(dBV/\sqrt{Hz}) = 17.0 - (-158.4) = 175.4dB/Hz \tag{4.1}$$

At 1 MHz, the dynamic range is:

$$DR(1MHz) = DR - 10 \cdot log_{10}(1MHz/1kHz) = 175.4 - 10 \cdot log_{10}(1000) = 175.4 - 30 = 145.4dB \tag{4.2}$$

The DAC in this project uses a reference voltage of $V_{ref} = 5.0V$, which affects the dynamic range. Since $V_{FSrms} = 10.97dBV$ and e_n stays unchanged, the dynamic range density $DR = 10.97 - (-158.4) = 169.4dB/Hz$ which gives a dynamic range of $DR(1MHz) = 139.4dB$. So the dynamic range density is higher than the required 160 dB/Hz.

The THD found in the datasheet is -105 dB, but it is evaluated at 1 kHz using a reference voltage of 5.0 volts. An estimation can be done for evaluating the THD at around 1 MHz instead by using the INL voltage and using a reference voltage of 5.0 volts. The INL voltage is 1 times the LSB voltage step as found in the datasheet [5]. The voltage step for 1 LSB or when the CODE changes by 1, can be found by rewriting the following formula found in the datasheet:

$$V_{out} = -V_{ref} \cdot (CODE/65536) \tag{4.3}$$

This gives the following formula:

$$V_{LSB} = V_{ref}/2^N = 5/2^16 = 5/65536 = 76.29\mu V \tag{4.4}$$

And this value can be used to approximate the THD as follows:

$$THD = 20 \cdot log_{10}(V_{INL}/V_{FSrms}) = 20 \cdot log_{10}(76.29 \cdot 10^{-6}/3.536) = -93.3dB \tag{4.5}$$

A THD of -93.3 dB at 1 MHz was found acceptably close to -100dB, after a consultation with the project proposer, as this was not the most important spec. This estimation will be verified with the spectrograph of harmonic response; this will be done in the chapter focused on testing chapter 6. Here, this approximation was used, which treats the peak INL error as if it were the distortion voltage. This was done to get an estimation of the actual THD.

The DAC8811 has a current output. Using the OPA277 amplifier [7], this current output can be turned into a voltage output by connecting it to the inverting input of the opamp. This is also suggested in the

DAC8811 datasheet [5]. A 10pF capacitor is added between the internal feedback resistor output of the DAC8811 and the current output going to the OPA277 op-amp for stabilisation.

The offset voltage of the OPA277 can be trimmed to null the offset of the operational amplifier as shown in the datasheet [7] with a 20 kΩ potentiometer. The offsettrim pins of the OPA277 can also be left open. For testing of the DCD circuit, both options were built to get better measurements, but the final version that goes into the pressure chamber has no potentiometers to adjust the voltage offset, because potentiometers would probably not survive high-pressure environments due to air pockets inside them, which could make them break under high pressure.

The DAC8811 needs a 5.0V voltage reference V_{ref}, which is created from a 7.0V voltage at the ADC part of the DCD circuit. The voltage reference is buffered in the DAC part of the DCD circuit by use of a voltage follower using the same type of operational amplifiers, an OPA277, as used at the output of the DAC8811. The buffer ensures a stable 5.0V voltage reference going into the V_{ref} pin of the DAC.

The opamp used as the voltage follower is powered using 7.0V at the V+ input and ground at the V- input. A bypass capacitor of 100nF is placed between the V+ and V- inputs to decouple the noise coming in from the power supply [7]. The DACs are powered by a 3.3V voltage going to the V_{DD} input and the GND pin connected to ground. Three bypass capacitors of 1nF, 100pF, and 1μF are connected between the V_{DD} and GND pins of the DAC for decoupling, as suggested in the datasheet of the DAC [5]. The op-amps at the output of the DACs are powered using 7.0V at the V+ input and -12V at the V- input. Bypass capacitors of 100nF are placed between the V+ input and ground and between the V- input and ground for decoupling.

The DACs use a clock signal, CLK, and a chip select, *CS, in order to input a serial digital input, SDI. The DACs output a current, Iout, which is made into a voltage output, DAC_ext, by using operational amplifiers. In the full system with 16 channels, 16 of the chip select, and serial digital input signals would be used together with one clock signal for all 16 DACs to get 16 signals at the output of the full DAC part of the DCD circuit.

4.1.3. PSUs

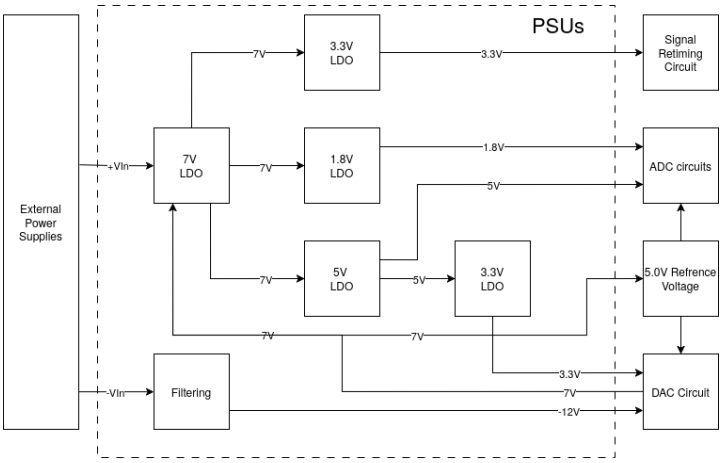


Figure 4.4: PSUs

The PSUs section of the DCD board is shown in Figure 4.4. The design uses LDOs for every voltage stage instead of switching converters. This choice was made because the implementation had to remain simple and compact, while also keeping the supply noise as low as possible. Switching converters were avoided because they create noise through their switching action, which can couple into the analog parts of the circuit and degrade measurement quality.

Each output of every voltage stage is followed by its own filtering network based on a ferrite bead and high-performance ceramic capacitors, as seen in the detailed circuit design in the Appendix B. This was done to suppress supply noise as much as possible before the rails reach the sensitive ADC, DAC,

and signal-conditioning circuits. Later in the development process, it was also found that this was the recommended configuration in the DAC datasheet [5], which confirmed the suitability of the chosen layout.

The reference voltage for the ADC and DAC sections is generated by the ADR4550BRZ, which is a high-performance voltage reference recommended in the ADC datasheet .... Since the current consumption of this reference source is marginal, the reference output was filtered using a ferrite bead, a relatively large ceramic capacitor, and a 100Ω resistor in the reference path. This helped isolate the reference source from load disturbances and reduce residual noise coupling into the analog conversion stages, while keeping the noise introduced by the resistor low.

In several places, combinations of small and large ceramic capacitors were used in parallel. This was done to obtain a broader filtering effect over different frequency ranges, since capacitors with different values also have different equivalent series resistances (ESR) and equivalent series inductances (ESL). Using a mix of capacitor values, therefore, helps suppress noise across a wider spectral range than a single capacitor value would provide. This is particularly important in mixed-signal designs, where noise can appear both at low frequencies and at higher-frequency switching or harmonic components.

The resulting power architecture provides the required supply rails of 3.3V, 1.8V, 5V, 7V, and -12 V for the different parts of the DCD system while keeping the analog supply paths as clean as possible. The combination of linear regulation, local filtering, and a dedicated reference source was chosen to support stable and low-noise operation of the full converter chain. The stacked topology of the power supplies was selected because it distributes the heat dissipation across multiple stages, which becomes increasingly important when all 16 channels are used in the future. This helps avoid concentrating the thermal load in a single regulator stage and improves the long-term scalability of the design. Detailed calculations of the power dissipation are included in the schematics in the appendix B.

4.1.4. Communication interfaces

4.2. External Breakout

The external breakout board functions as a connection between the DCD board, inside or outside the pressure chamber, and the FPGA development board. It has connections for the external power supply that the PSUs on the DCD board need and connections for measuring outputs of the FPGA and DCD.

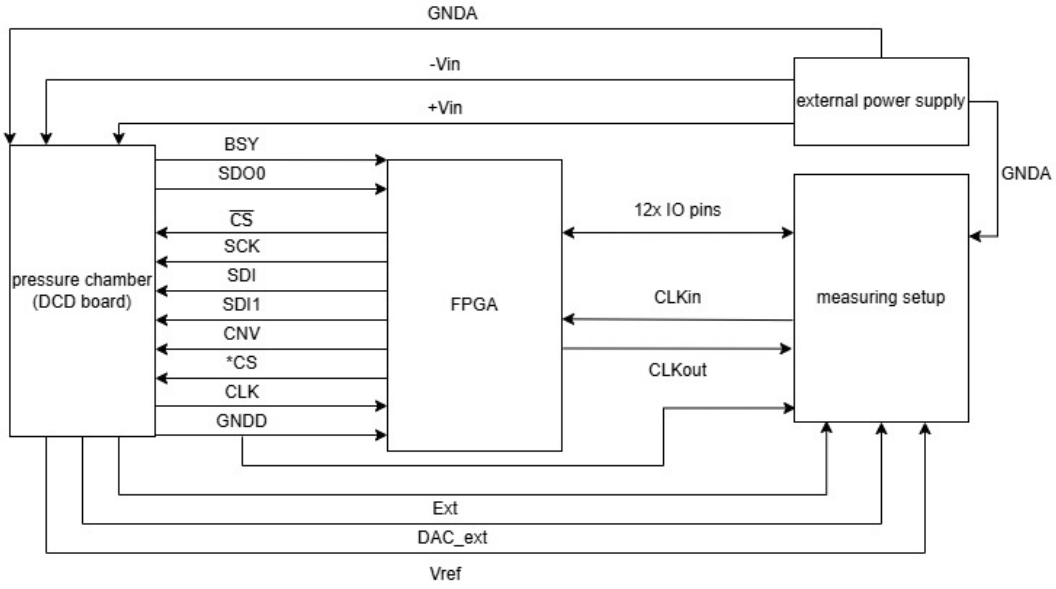


Figure 4.5: External breakout board

Figure 4.5 shows the connections that run via the external breakout board to the DCD board, FPGA, external power supply and measuring equipment. Figure E.2 in Appendix E shows the schematic of the

external breakout board in more detail.

external power supply
The external power supply is needed for the PSUs on the DCD board to generate the appropriate power that the components, like the ADCs and DACs, need to function properly. The external power supply delivers a positive, +Vin, and a negative, -Vin, voltage, where the voltage Vin is chosen to be 12V. An SS34 [8] schottky diode is placed in series with the power rails for reverse polarity protection. This specific diode was chosen for its low voltage drop of only 500mV at 3A. It also has a high maximum surge current of 100A and fast switching speed, making it perform well in high-frequency applications. The power supply also gives an analog ground connection for the DCD and measuring setup.

measuring setup
The external breakout board has some pins and coaxial connections for cables that can go to a measuring setup. The measuring setup used for testing will be discussed in chapter 6. The breakout board has SMA connectors for measuring the reference voltage, Vref, used in the DCD circuit, the output of the DAC, DAC_ext, and the output after the ADC, Ext, which is the output of the full system. These signals come directly from inside the pressure chamber. The external breakout board can also deliver a clock to the FPGA or read out a clock of the FPGA via pin headers. Although this will not be needed for this setup, the pins are there in case they are needed for future implementations. There are 12 more pin headers on the board that go to the IO pins of the FPGA, which can be used as extra inputs or outputs if that is needed for writing or reading data to or from the FPGA. The measuring setup can also connect to the digital, GNDD, and analog ground, GNDA, which it receives from the DCD board and external power supply, respectively.

DCD board connections
The UMPT-04-01.5-G-VT-SM-WT connectors are chosen because they were already in use on other boards developed by the company for which this board was made, and these connectors make connecting to those boards that are a part of the pressure chamber used in testing easier. There are four of these connectors on the external breakout board, which provide 16 connections to the DCD board.

FPGA
The FPGA development board is connected to the external breakout board via pin sockets, which connect the FPGA to the connections to the DCD. The signals that come from the DCD or inside the pressure chamber to the FPGA via the external breakout board are BSY, SDO0, and CLK, which go to the IO pins of the FPGA. The FPGA also sends the signals $\overline{CS}$, SCK, SDI, SDI1, CNV, and *CS from IO pins to the DCD board. The FPGA also receives the digital ground GNDD from the DCD.

5

PCB Layout

Below stands the explanation of the approach taken during implementing the circuit designs from the chapter 4 as a PCB, and explanation of the pressure chamber connections to the measurement setup during testing.

5.1. DCD

The PCB layout was developed with standard EMI mitigation practices in mind to preserve signal integrity and reduce unwanted coupling between the analog and digital parts of the system. One of the main layout rules applied was that every signal via was accompanied by a nearby pair of ground vias. This allowed the return current to transition cleanly to the other internal layer and reduced discontinuities in the current path, which is important for minimizing parasitic inductance and electromagnetic emissions.

In addition, ground stitching was used throughout the board to provide a low-impedance return network and to improve shielding between different sections of the circuit. The power delivery traces were also thickened to reduce resistance and voltage drop, especially for rails carrying higher current or feeding sensitive subsystems. This helped ensure that the supply voltages remained stable and that power routing did not become a limiting factor in the performance of the board.

A clear separation was maintained between the digital and analog ground regions. These ground domains were kept apart across most of the board and connected at a single point using a ferrite bead. This arrangement helps prevent high-frequency digital return currents from flowing through the analog ground region, which would otherwise increase noise coupling into the measurement chain. By controlling the ground connection in this way, the layout supports cleaner analog operation while still maintaining a defined common reference point.

Special care was taken when routing the delicate analog traces. These signals were kept as far away as practical from noisy digital lines, clock traces, and other switching signals to minimize crosstalk. Short, direct routing paths were preferred for the most sensitive nets, and unnecessary loop areas were avoided wherever possible. This was especially important for traces carrying low-level analog signals, where even small amounts of coupled noise could affect measurement accuracy.

All important high-speed traces were designed as coplanar waveguides with a characteristic impedance of 50Ω. This was done to improve signal integrity and to make the routing more predictable across the board. The exact trace widths, spacings, and layer stack parameters required to achieve this impedance are listed in Appendix F. These dimensions were used consistently for the critical nets to ensure controlled impedance routing and to keep reflections and transmission losses within acceptable limits.

The above-mentioned layout practices were based on the following papers:

- Analog Devices: [9]
- IEEE: [10]

- IEEE: [11]
- IEEE: [12]
- IEEE: [13]
- IEEE: [14]
- AllPCB: [15]

5.2. Component Placement for a 16 Channel Implementation

The draft component placement shown in the appendix H demonstrates that a 16-channel implementation is feasible within the physical volume constraint of 100 cm3. The placement study was used as an early check that the full system could be realized without exceeding the available space, before finalizing the mechanical and electrical integration of the board.

The PCB outline used for this draft has dimensions of 126 mm by 79 mm, which gives a board area of approximately 9954 mm2. With a board thickness of 1.6 mm, the base PCB volume is already constrained to a compact form factor. In addition, the tallest components on the board, such as the 1206 capacitors, define a stack height that must be taken into account when estimating the total occupied volume of the assembly.

The height budget was estimated as 2.5 mm above the PCB for the tallest component on each side, plus the 1.6 mm thickness of the PCB itself. This leaves approximately 3.4 mm of remaining vertical space for a second PCB layer stacked on top of the first one. That upper layer would contain the FPGA and its companion circuitry, while the lower layer contains the analog DCD channels. This stacked approach makes efficient use of the available volume and keeps the analog and digital sections physically separated.

This draft, therefore, indicates that the complete 16-channel system can be implemented within the 100 cm3 constraint, provided that the mechanical stacking arrangement is respected. The result is encouraging because it shows that the physical integration of the analog board, FPGA board, and associated support circuitry is possible without exceeding the available enclosure space.

5.3. External Breakout

The external breakout board was made on a 4-layer PCB. The design rules of the manufacturer [16] were used as constraints for designing the PCB. For the PCB layout design of the external breakout board, two separate ground planes were needed: one analog ground, GNDA, and one digital ground, GNDD. These ground planes were connected on the DCD board but were kept separated on the External Breakout Board to protect the analog signal from the noisy digital signals, as shown in the following article about PCB layout design [17]. The analog and digital ground planes are connected via a ferrite bead. The same trace width and distances as on the DCD layout were used. The renders and layout views of both the External Breakout and DCD boards are visible in the Appendix G. Appendix G shows the layout of the PCB of the external breakout board.

5.4. Chamber connection

For testing of the boards without the pressure chamber, everything is connected analogously as when the pressure chamber is used. A schematic of the connection without the chamber is shown in Figure E.3 in Appendix E. The external breakout board with the FPGA development board attached to it is connected directly to the internal breakout board with the DCD on it. Both boards are the same boards that will be used when testing with the pressure chamber. In Figure E.4 in Appendix E, it is shown how these same boards are connected when the pressure chamber is used. The previously discussed external breakout board is here connected to an external interposer board whose purpose is to connect the backside of the breakout board to 16 cables, which pass through the pressure chamber lid to an internal interposer board with the same purpose as the external interposer board. The interposer boards and the cables are a part of the pressure chamber used in testing. The internal interposer board then connects to the internal breakout board with the DCD circuit on it.

Part III

Evaluation

6

Testing of the system and Validation of its Performance

6.1. Production and bring-up of the PCBs

6.1.1. Production

The production and bring-up of the PCBs formed a critical step in the verification of the DCD system. After the schematic and PCB layouts were completed, the manufacturing data were exported and sent to the production house Aisler using ODB+ files. This format was chosen because it contains all information required for PCB fabrication and assembly in a structured way, reducing the chance of interpretation errors during production.

The components used for the boards were sourced in advance from Mouser, Farnell, and directly from SiTime. This allowed the required parts to be available when assembly started and reduced the risk of delays caused by long lead times. The full bill of materials is included in the appendix, which also makes it easier to reproduce the design and to track component choices during later revisions or maintenance.

The boards were assembled using vapor phase soldering, which provided a controlled and uniform reflow process for the solder joints. Because the design included a mixture of small surface-mount components and more delicate ICs, this method was suitable for achieving reliable soldering. In addition to the reflow process, pick-and-place was performed manually. Although this required more time than automated placement, it didn't require coordinating the process with a production house and was simply performed by our team.

After assembly, the boards were visually inspected to check solder quality, component orientation, and overall assembly accuracy. This inspection step was important for detecting obvious defects such as misaligned components, missing parts, poor solder joints, or accidental bridges before the boards were powered. A visual inspection at this stage reduced the risk of introducing avoidable damage during bring-up.

A special mechanical design consideration was made for the MEMS oscillator. A custom plastic bracket was designed to cover the oscillator so that it could later be encapsulated in epoxy. This was done to protect the oscillator from mechanical stress and to improve its suitability for use in the pressure environment. The bracket helped create a stable shape for the epoxy layer and ensured that the oscillator would remain covered in a controlled way.

6.1.2. Bring-up

Before powering the complete board, one PCB was assembled with only the power supply sections populated. This bring-up step was used to verify that the supply rails functioned correctly and that the power connections to the various ICs were properly routed. Testing the power supplies separately was important because it allowed any mistakes in the power distribution network to be identified before

applying power to the full board. This reduced the risk of damaging expensive components during the initial power-up of the complete assembly.

During bring-up, the board was carefully checked for correct voltages, continuity, and proper connection to all chips before the remaining circuitry was powered. This approach made it possible to identify several required modifications, or bodges, before full operation. A list of all bodges applied to the boards is included in the appendix and can be found in Appendix X. Some of these corrections were necessary because the initial design would have caused damage if the board had been powered without modification. In particular, it was discovered that the DAC outputs a negative voltage, which would have damaged the ADC section if connected directly. To prevent this, the DAC output was biased using VRef so that the signal remained within a safe operating range for the ADC.

This staged bring-up process was therefore an essential part of validating the hardware before full system testing. It provided an opportunity to detect design issues early, apply practical corrections, and ensure that the boards could be powered safely before proceeding to functional measurements.

6.2. Validation of the performance of the system without pressure

The goal of all measurements in this chapter is to determine whether the system can meet the required specifications at all. These tests were performed outside the pressure chamber to establish a baseline performance before any high-pressure operation is attempted. The analog performance is very much dependent on the digital performance, because glitches in the digital domain essentially create nonlinearities, which change the harmonic content of the signal and result in distortions in the analog output. If such glitches occur, the analysis would focus on the periods of time when they are not present so that the intrinsic analog behavior can still be evaluated.

All tests described in this chapter are performed using the spectrum analyzer and the ADC output. The output of the ADC is post-processed in Python using Fourier transforms and other spectral analysis methods so that quantities such as THD, THD+N, dynamic range, and ENOB can be calculated from the measured data. The testing methods follow standard procedures for data converters as described in chapter 5 of the Analog Devices data conversion handbook [18].

6.2.1. Initial tests

The initial tests outside the pressure chamber focused on offset error, gain error, noise floor, and other basic functional parameters. These measurements were used to confirm that the system was operating within a reasonable range and that the analog signal path was correctly biased and scaled. The offset error is defined as:

$$\text{Offset error} = V_{\text{out, measured}}(0) - V_{\text{out, ideal}}(0) \tag{6.1}$$

The gain error is defined as:

$$\text{Gain error} = \frac{V_{\text{out, measured}}(V_{\text{FS}}) - V_{\text{out, measured}}(0)}{V_{\text{FS}}} - \text{Gain}_{\text{ideal}} \tag{6.2}$$

where VFS is the full-scale input voltage. The noise floor was measured from the power spectral density of the output when no signal was applied.

During testing, a frequency sweep was also performed to check the bandwidth performance of the output stage. This revealed that the op-amp selected for the DAC output stage had a too-low slew rate of 0.8 V/μs. At a 1 MHz triangle wave, the output would be limited to approximately 0.2 V, which made meaningful high-frequency characterization impossible. For this reason, all testing was limited to lower frequencies.

6.2.2. THD+N

The total harmonic distortion plus noise, THD+N, was measured using sine-wave inputs at 1 kHz and 10 kHz. These frequencies were selected to evaluate both low-frequency and moderately higher-frequency behavior while remaining within the reliable operating range of the output stage. The signal spectrum

was analyzed in Python after acquisition, using Fourier analysis to separate the fundamental component from the harmonic and noise contributions. This test provided a direct view of how much the system distorted a clean sinusoidal input and how much additional noise was present in the output.

THD+N is defined as the ratio of the RMS sum of all harmonic and noise components to the RMS value of the fundamental, expressed as a percentage or in dB:

$$\text{THD+N} = \frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_N^2 + V_{\text{noise}}^2}}{V_1} \tag{6.3}$$

where V1 is the RMS voltage of the fundamental, and V2, V3, ..., VN are the RMS voltages of the harmonic components up to the NN-th harmonic, and Vnoise is the RMS noise voltage outside the fundamental band.

$$(\text{THD+N})_{\text{dB}} = 20 \log_{10} \left(\frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_N^2 + V_{\text{noise}}^2}}{V_1} \right) \tag{6.4}$$

6.2.3. Dynamic range

Dynamic range was also measured using sine-wave excitation at 1 kHz and 10 kHz. The Nyquist bandwidth for a sampling rate fs is:

$$f_{\text{BW}} = \frac{f_s}{2} \quad \text{(Nyquist bandwidth)} \tag{6.5}$$

The dynamic range is:

$$\text{Dynamic range} = 20 \log_{10} \left(\frac{V_{\text{FS, rms}}}{V_{\text{noise, rms}}} \right) \tag{6.6}$$

The dynamic range density in dB/Hz is:

$$\text{DR}_{\text{dB/Hz}} = \text{SNR}_{\text{dB}} + 10 \log_{10}(f_{\text{BW}}) \tag{6.7}$$

6.2.4. INL, DNL, and linearity

INL, DNL, and linearity were evaluated using a ramp input, which is the standard method for observing the transfer function deviation. The DNL for code kk is:

$$\text{DNL}(k) = \frac{\Delta V_k}{V_{\text{LSB, ideal}}} - 1 \tag{6.8}$$

where ΔVk is the measured voltage difference between code transitions kk and k+1k+1, and VLSB, idealVLSB is the ideal LSB voltage step.

The INL for code kk is:

$$\text{INL}(k) = \sum_{i=0}^{k} \text{DNL}(i) \tag{6.9}$$

or in voltage form:

$$\text{INL}(k) = \frac{V_{\text{measured}}(k) - V_{\text{ideal}}(k)}{V_{\text{LSB, ideal}}} \tag{6.10}$$

6.3. Validation of the performance of the system with pressure

The same measurements described in Section 6.2 are intended to be performed inside the pressure chamber at 500 bar. However, the first objective under pressure is to verify that the circuit survives the 500-bar environment at all. Only after this basic survivability is confirmed can the full performance characterization be carried out. The intention is to repeat all tests at 500 bar and compare the results

with the ambient-pressure measurements. If discrepancies are observed, the goal will be to determine the dependency of those deviations on the pressure level.

Every test below will be described using the spectrum analyzer and the ADC output, with the same Python-based post-processing (Fourier transform, spectral analysis) used as in the unpressurized case. These comparisons will reveal whether pressure affects monotonicity, code transitions, or cumulative nonlinearity.

7

Test Results

This chapter will show and explain the results of the tests done on the DCD system inside and outside the pressure chamber. It will also show the resulting 16 channel system and explain if and how it meets the given system specifications.

7.0.1. Test results without pressure

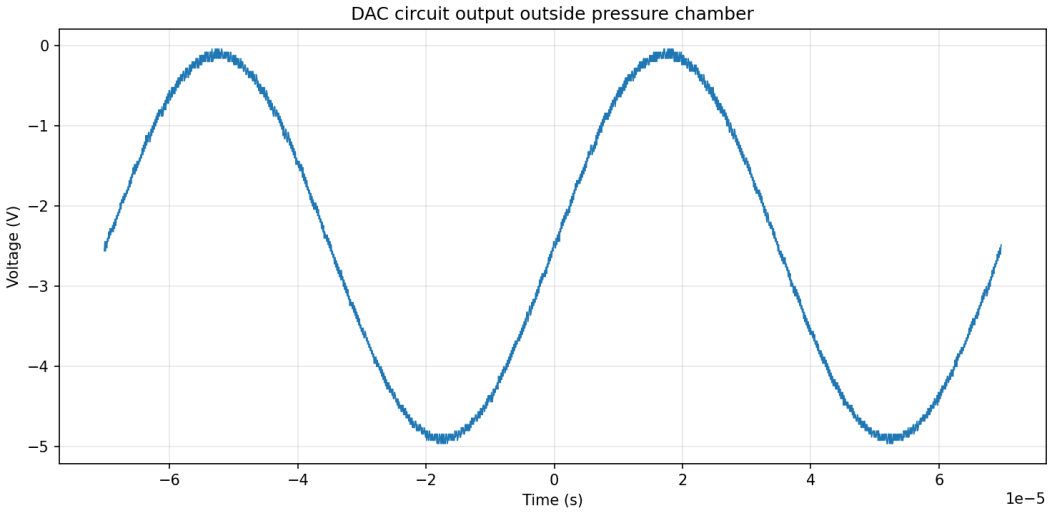


Figure 7.1: DAC circuit output without pressure chamber

Figure 7.1 shows the output signal of the DAC circuit when the FPGA sends data to the DAC to output a sine wave.

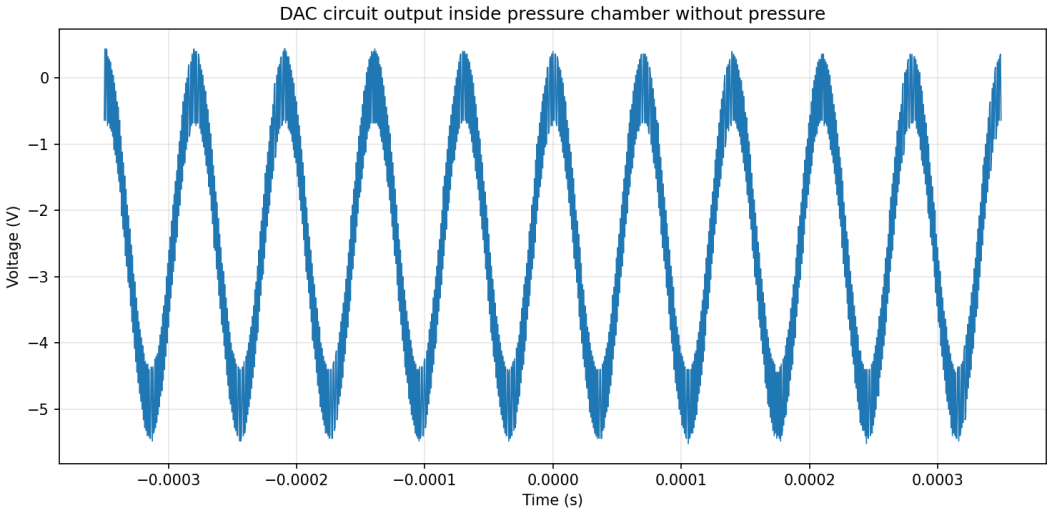


Figure 7.2: DAC circuit output in the pressure chamber and measured by the oscilloscope

Figure 7.2 shows the output of the DAC circuit when it is asked to output the same signal as in Figure 7.1. This signal is a null measurement for the pressure test since the system is placed inside the pressure chamber while still at atmospheric pressure. This signal has more noise than the signal without the pressure chamber. This is probably due to the lid of the pressure chamber used. To read out the DAC circuit output on the oscilloscope, the analog signal has to pass through this metal chamber lid.

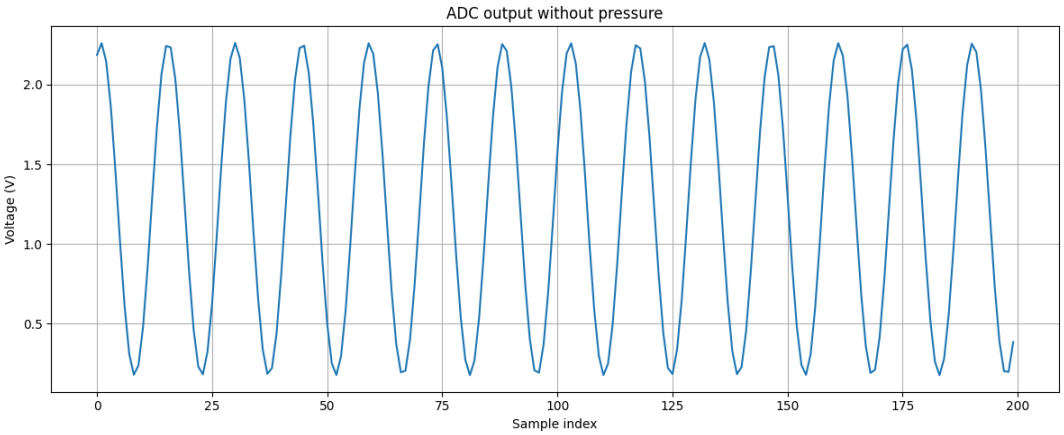


Figure 7.3: DAC output measured by the ADC inside the pressure chamber without pressure

Figure 7.3 shows the signal that is outputted by the ADC on the DCD circuit when the system is inside the pressure chamber at atmospheric pressure, when the ADC receives the sine wave signal from the DAC circuit shown in Figure 7.2. This signal is not noisy, which leads to the assumption that the chamber lid used for the pressure chamber testing is the source that introduces noise to the sine wave signal. The readout of the digital ADC signal is done via the FPGA and Ethernet cables.

7.0.2. Test results with pressure

For pressure testing, the pressure in the pressure chamber was increased from 0 to 500 bars of pressure. This was done in steps of 50 bars.

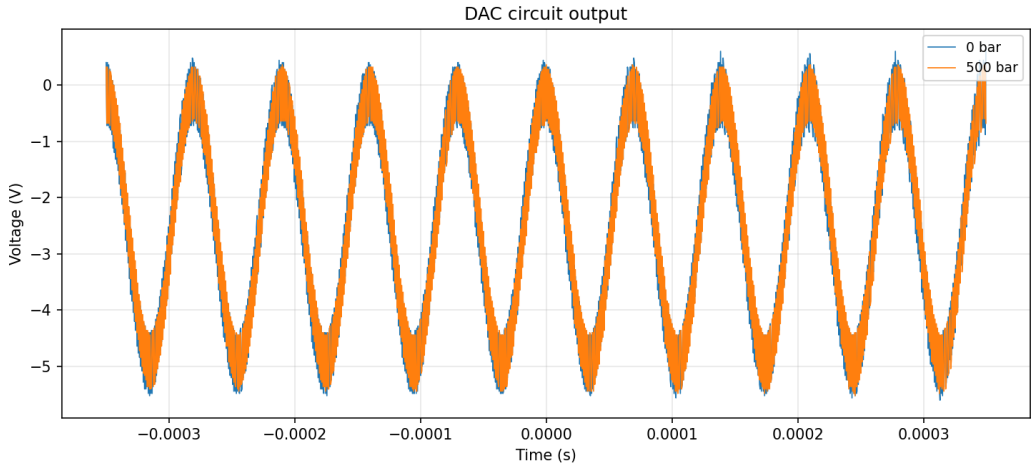


Figure 7.4: comparison between null measurement and 500 bars pressure test

As can be seen in Figure 7.4 the output signal of the DAC circuit is almost the same at 500 bars of pressure as at 0 bars of pressure; the difference here is negligible.

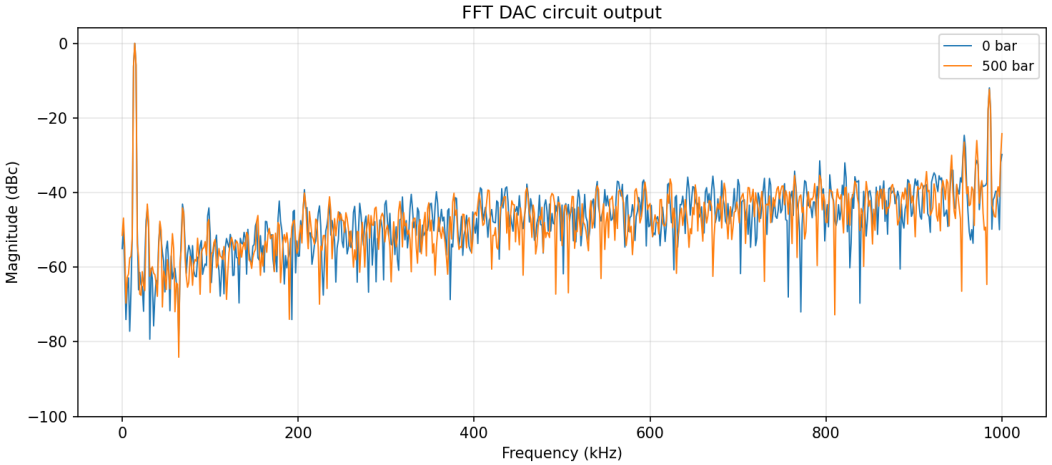


Figure 7.5: FFT comparison between null measurement and 500 bars pressure test

The FFTs of the signals in Figure 7.4 are shown in Figure 7.5. Due to the noisy signal in Figure 7.4, the FFTs are also very noisy and it is not possible to see clear harmonics to read out for the dynamic range and THD+N calculations, but since the signals under pressure and without pressure were found to be almost the same and the noise floor for both FFTs are almost the same and to high due to noise, it is not really possible to calculate the dynamic range and THD+N here.

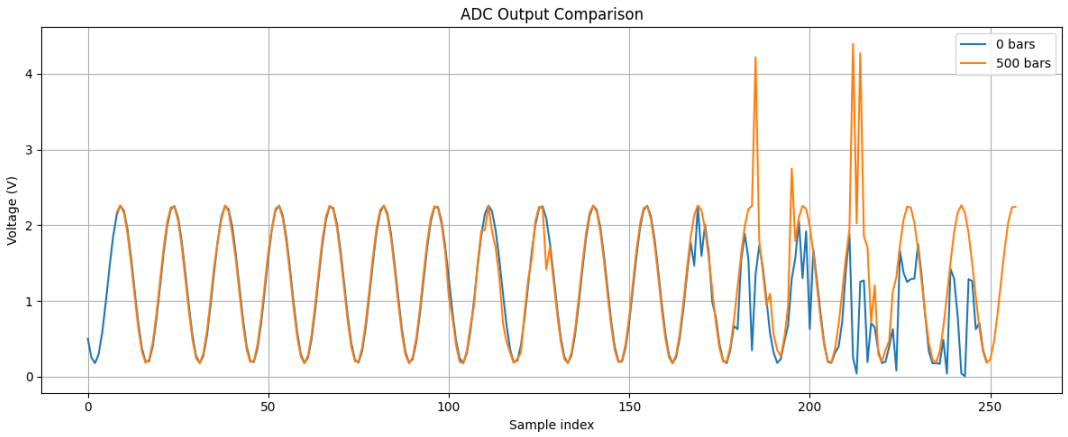


Figure 7.6: ADC output comparison between null measurement and 500 bars pressure test

Figure 7.6 shows the comparison between the signals outputted by the ADC under atmospheric pressure and 500 bars of pressure. The signal seems to be unaffected by the increase in pressure; however, due to the bodge mentioned in the Appendix D that required 1k resistors to be added to reduce the output voltage of the FPGA to match the levels expected by the ADC, and due to the parasitic capacitance of the traces going to the ADC, which was about 2pF, the timings required to operate that chip with its full performance could not be met, consequently resulting in missing bits. This phenomenon can be visible as occasional bursts of distortions, as seen in the figure 7.6.

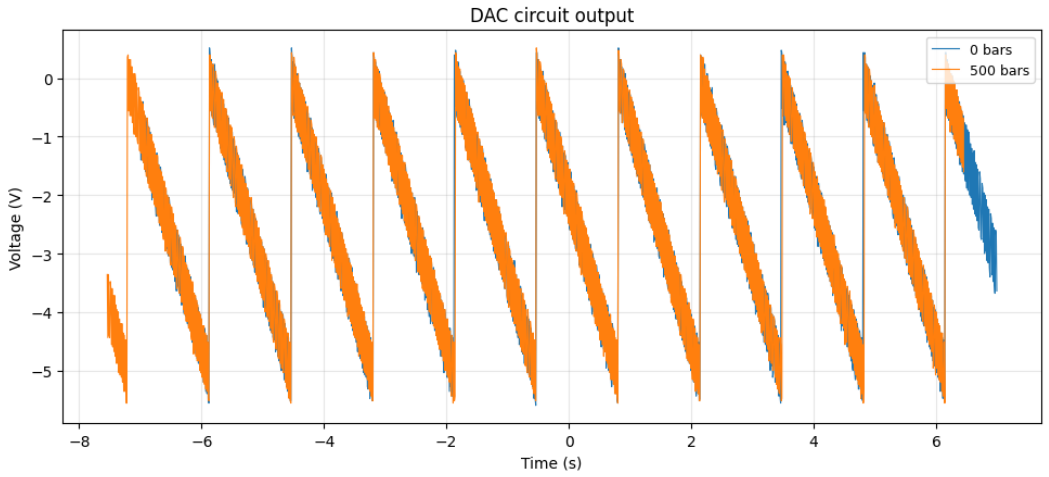


Figure 7.7: DAC circuit output ramp signal

Figure 7.7 shows the DAC circuit output signal when the DAC is instructed to output a ramp function. The ramp signal is almost the same at 0 bars of pressure as it is at 500 bars of pressure.

8

Discussion

Although the project did not allow us to verify every performance aspect of the chip and complete all intended tests, the overall result is still positive. The main limitations came from the available equipment, the time available for development, and the fact that several quick fixes had to be introduced during bring-up to make the system operate safely. In addition, a few design mistakes became apparent only after hardware assembly, which is normal in a project of this complexity, but still affected the completeness of the validation.

One of the most important issues was the output stage of the DAC. The selected opamp did not have a sufficiently high slew rate for the intended signal bandwidth. With a slew rate of only 0.8 V/µs, the amplifier could not reproduce fast-changing waveforms properly, especially at higher frequencies.

Several of the bring-up corrections were also necessary to make the board functional in the first place. For example, the FPGA outputs 3.3 V logic levels, and these signals were temporarily adapted using voltage dividers. While this allowed the board to operate during bring-up, the dividers introduced additional propagation delay with the parasitic capacitance of the traces, which caused timing issues in the digital interface. This kind of correction is acceptable as a quick hardware fix during prototyping, but it also shows that the signal chain would benefit from a proper level-shifting solution in a future revision. Dedicated level shifters would provide cleaner edge translation, better timing performance, and a more robust interface than the resistor-based workaround, especially when the board is intended to operate in a demanding, noisy environment, such as a robot.

Despite these limitations, the system did work, and a large part of the required functionality was successfully demonstrated. The power supplies were brought up, the digital and analog sections were connected correctly, and the loopback concept allowed the system to be tested without relying on external ultra-high-precision stimulus sources for every measurement. This confirmed that the basic architecture is sound and that the chosen approach is viable. It also showed that the board is capable of supporting the intended measurement workflow, at least for the frequency range and operating conditions that were practically accessible during the project.

The performance results also indicate that many of the original requirements are achievable with further development. Some specifications were already close to target, while others were constrained more by implementation details than by the underlying architecture. This is an important distinction because it suggests that the design itself is not fundamentally flawed. Rather, it needs refinement in a few key areas, such as the output stage, signal conditioning, and some of the temporary fixes used during bring-up.

Overall, the project can be considered a successful prototype demonstration. It was not possible to complete every planned validation step, but it was possible to show that the system is able to output a signal and that most of the required behavior can be obtained. With more time, more careful component selection, and proper redesign of the quick fixes, the remaining specifications should be reachable. In particular, replacing workaround solutions such as voltage dividers with proper level shifters and selecting an opamp with adequate slew rate and bandwidth would significantly improve the robustness

and completeness of the design.

9

Conclusion

The project resulted in a DAQ prototype that was designed to satisfy the full set of non-functional requirements, but only a subset of them could be verified experimentally within the available project time. In particular, the system was tested and demonstrated to meet the requirements for data handling, number of channels, channel scalability, and pressure rating, corresponding to R5, R6, R7, and C3, in the chapter 2.

The data handling requirement, R5, was validated by the implemented system architecture, which is capable of streaming data or providing a one-second buffer. The design was structured in a way that remains scalable toward 16 channels. In addition, the complete system was tested successfully at the required pressure level of 500 bar, confirming compliance with C3.

Although the full specification set was not experimentally verified, the remaining requirements were met by design. This includes the sample rate, dynamic range, bandwidth, THD performance, and user interface requirements. These were addressed through component selection, circuit architecture, and the overall system implementation, but they could not all be fully validated under test conditions within the project scope.

The main reason for limiting the verification scope was the development-time constraint, C2, which had the highest priority in practice and was enforced by TU Delft. Given the available 10 weeks, the project had to focus on the most critical requirements and on getting a working prototype completed in time. As a result, the validation effort was concentrated on the requirements that were most essential to demonstrate system functionality and pressure survivability.

Overall, the project achieved its main goal: a working prototype was built, key requirements were demonstrated, and the design approach proved feasible for further development. With more time, the remaining design targets could be tested and refined, but the results already show that the proposed architecture is a solid basis for a more complete future implementation.

A

Ethical implications

This appendix provides an ethical analysis about the data acquisition system discussed in this report.

Societal impacts (product)
If fully implemented this data acquisition system could be used for research purposes and have a positive impact in that area because it allows for high precision gathering of data in high pressure environments where it would otherwise be hard to gather that data or at such high precision. the main stakeholders affected here would be researchers working with high pressure environments like sub-sea who would want to gather data about fish populations or the bottom of the sea, or environments in space, mainly on planets where gravity is higher than on earth. The data acquisition system could in these cases give a positive impact. Other stakeholders involved could be people developing spyware or developing weapons, where a high precision data acquisition system could have negative impacts. The system could be used in high pressure environments like sub-sea to build targeting systems for torpedos or other missiles in normal environments since they would need a high precision system like this one. It could be used in spyware to illegally gather data if the system falls into the wrong hands which would have a negative impact.

Ethical aspects of development (process)
To make the system, components and substances like solder and cleaning materials were used. These materials contain substances which are bad for human health and the environment. These products were therefore handled with care and ventilation systems with filters were used so that these substances could not harm the environment or the health of the ones building the PCBs of the data acquisition system.

Ethical evaluation
The most significant ethical concern raised by the product is its potential for dual use. While the system was designed for scientific research, the same precision and environmental robustness that make it valuable for subsea data collection could be exploited for weapons development or surveillance. Therefore the development of a product like this could have negative ethical impact. The fact that the system is a concept demonstrator rather than a finished product offers some mitigation, but does not eliminate the concern that technologies at early stages can still be used for unethical purposes. Publishing the design of the high precision data acquistition system is ethically valuable if used for research, supporting others with their scientific research, but it also enables misuse by parties with malicious intent. This is a trade-off between openness and security.

On the process side, the handling of hazardous materials such as solder and chemical cleaning agents represents a real, but manageable, ethical concern. The people most directly affected are the engineers building the system, whose health could be harmed by improper exposure. The use of ventilated workspaces and filtered extraction systems is ethically praiseworthy: the harm was anticipated, and concrete precautions were taken rather than ignored. The environmental impact of these substances, if improperly disposed of, would extend beyond the lab, affecting third parties who have no stake in the

project and no ability to consent to that risk. Proper disposal therefore carries a moral ethical weight beyond the legal obligations.

Reflection on design choices

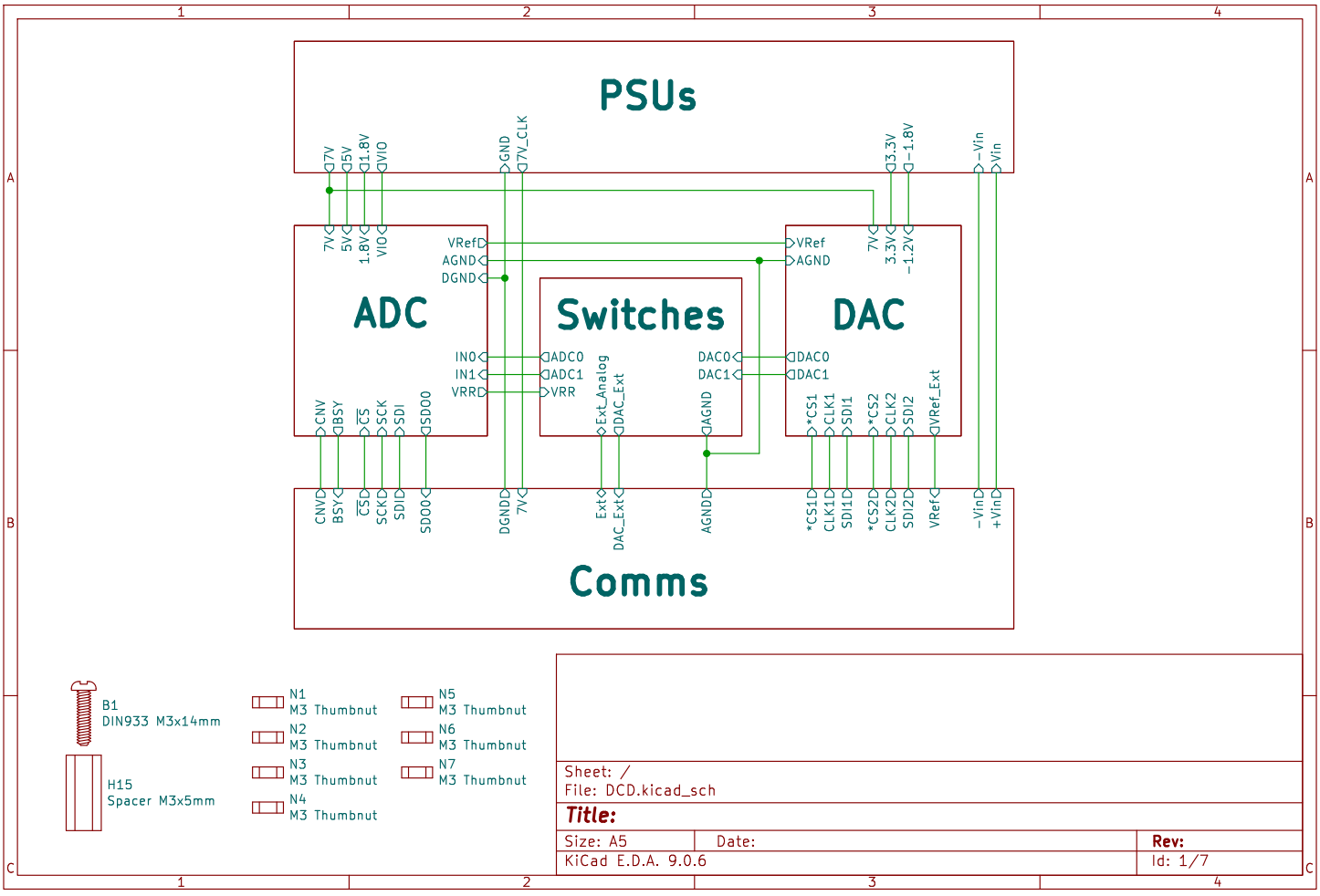
Ethical considerations had a limited influence on the engineering process. The most direct example was the handling of environmentally harmfull materials during PCB assembly, the decision to use ventilated workstations with filtered extraction was a deliberate choice to protect both the people involved and the surrounding environment, rather than treating safety precautions as optional. Foreseeable harms to those involved in a project should be prevented when possible. However, the dual-use potential of the system was not explicitly addressed during the design phase. The focus remained on optimising technical performance such as precision, dynamic range, and high pressure environment suitability. The steps that could have been considered more to better address the ethical issues are things like deciding in advance which technical details to keep internal and which to publish openly.

Forward-looking responsibility

If developed into a real-world application, access to the system and its full design documentation should be restricted to research institutions, with clear contractual limits on permitted use. An export control review would be advisable given the subsea and high-pressure capabilities. On the process side, any scaling of production should comply with european RoHS regulations to minimise hazardous material use, and proper disposal procedures for chemical waste should be formalised. A brief ethics review at each major development milestone would help ensure that dual-use risks are reassessed as the system's capabilities grow.

B

Detailed Circuit Design



B1
DIN933 M3x14mm

H15
Spacer M3x5mm

N1
M3 Thumbnut

N2
M3 Thumbnut

N3
M3 Thumbnut

N4
M3 Thumbnut

N5
M3 Thumbnut

N6
M3 Thumbnut

N7
M3 Thumbnut

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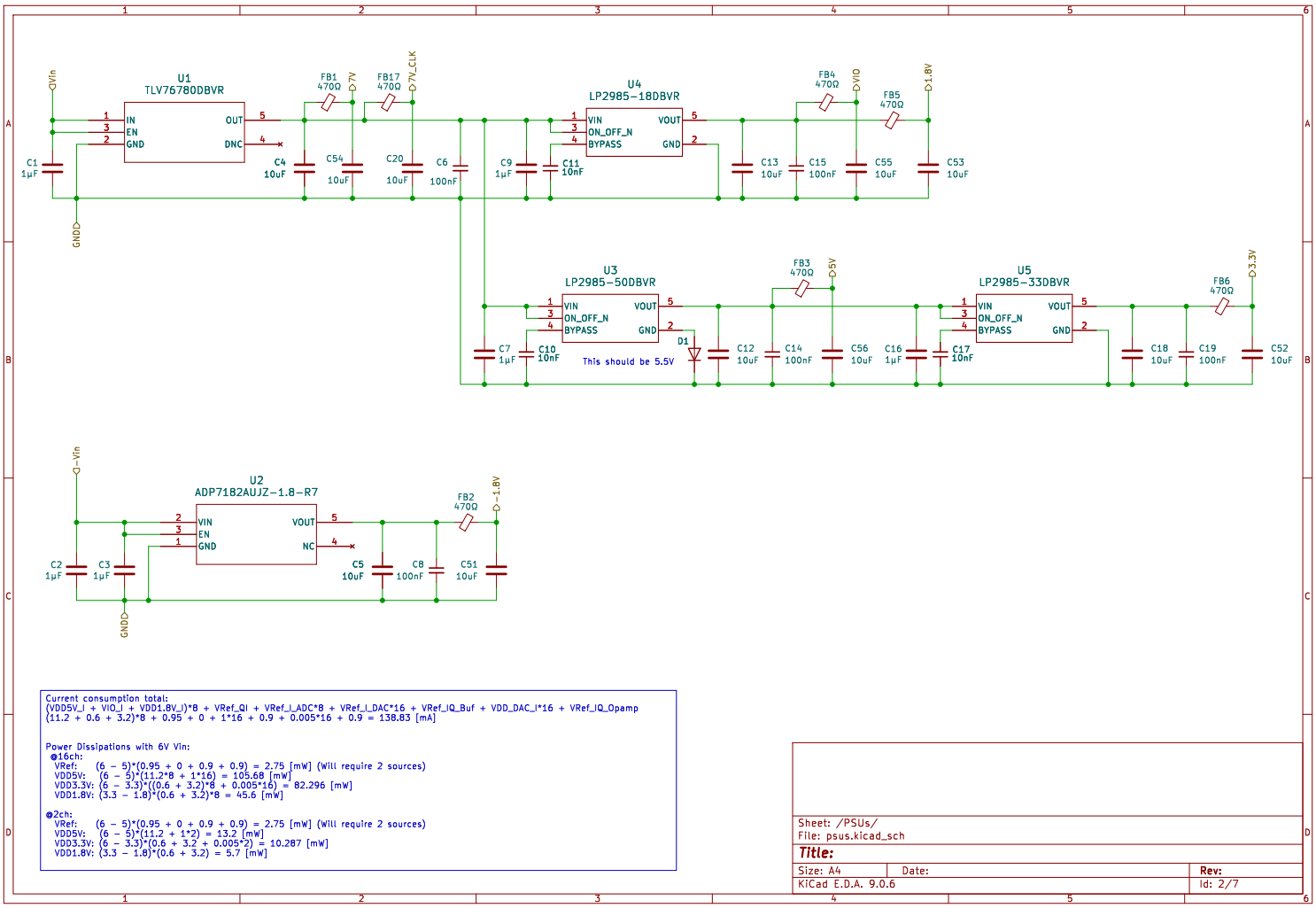

Current consumption total:
(VDD5V_I + VIO_I + VDD1.8V_I)*8 + VRef_QI + VRef_I_ADC*8 + VRef_I_DAC*16 + VRef_IQ_Buf + VDD_DAC_I*16 + VRef_IQ_Opamp
(11.2 + 0.6 + 3.2)*8 + 0.95 + 0 + 1*16 + 0.9 + 0.005*16 + 0.9 = 138.83 [mA]

Power Dissipations with 6V Vin:
@16ch:
VRef: (6 - 5)*(0.95 + 0 + 0.9 + 0.9) = 2.75 [mW] (Will require 2 sources)
VDD5V: (6 - 5)*(11.2*8 + 1*16) = 105.68 [mW]
VDD3.3V: (6 - 3.3)*((0.6 + 3.2)*8 + 0.005*16) = 82.296 [mW]
VDD1.8V: (3.3 - 1.8)*(0.6 + 3.2)*8 = 45.6 [mW]

@2ch:
VRef: (6 - 5)*(0.95 + 0 + 0.9 + 0.9) = 2.75 [mW] (Will require 2 sources)
VDD5V: (6 - 5)*(11.2 + 1*2) = 13.2 [mW]
VDD3.3V: (6 - 3.3)*(0.6 + 3.2 + 0.005*2) = 10.287 [mW]
VDD1.8V: (3.3 - 1.8)*(0.6 + 3.2) = 5.7 [mW]

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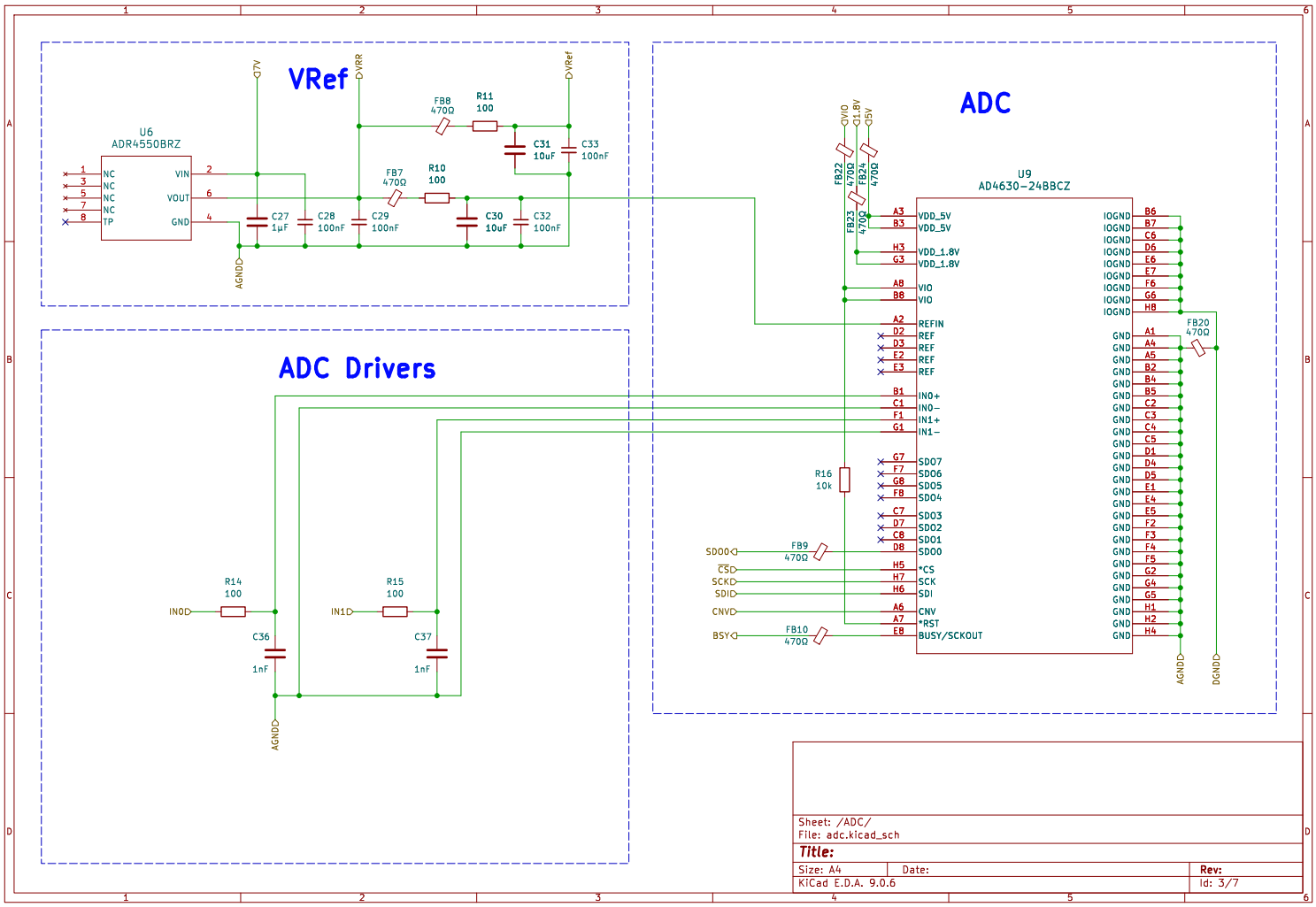
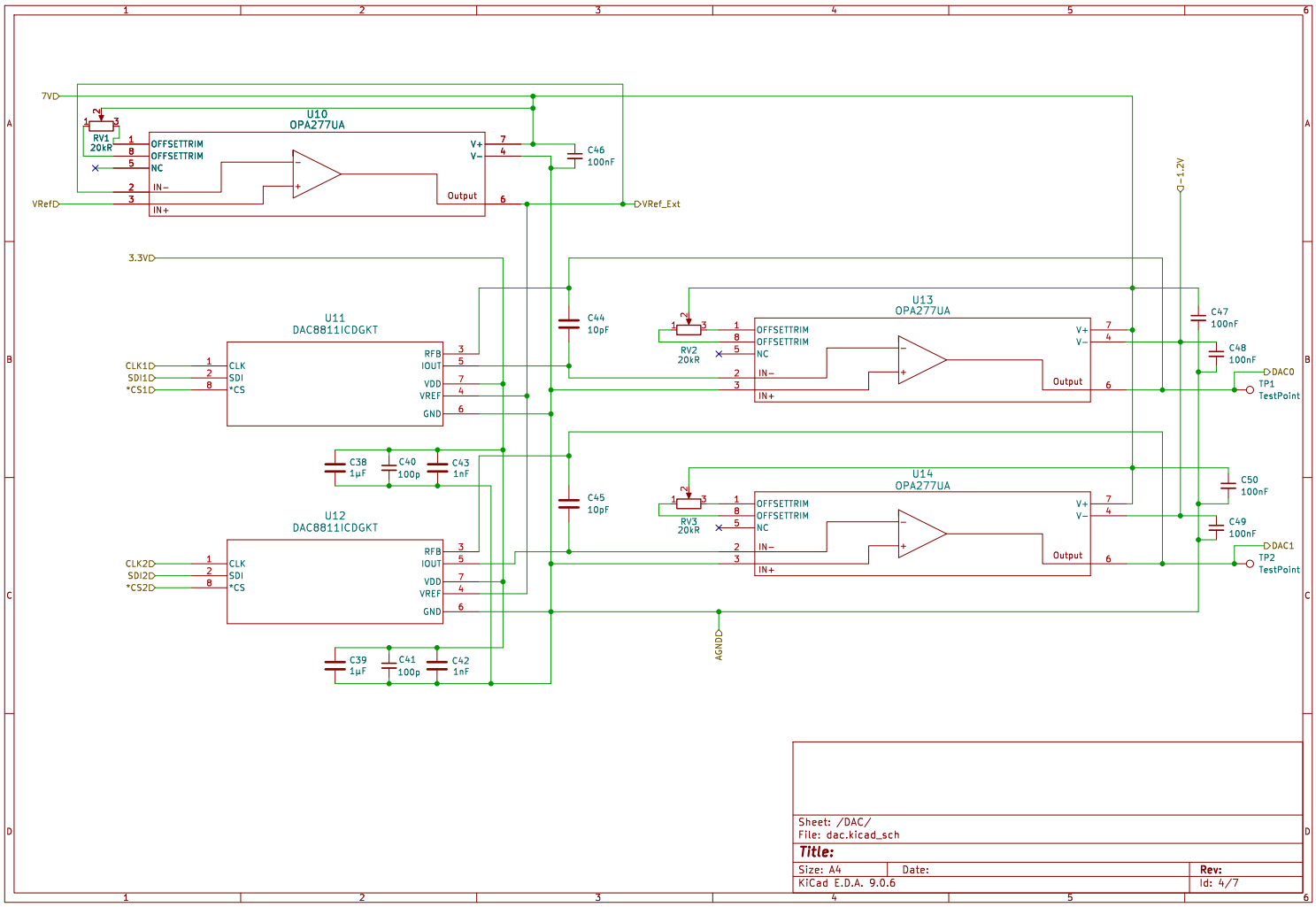
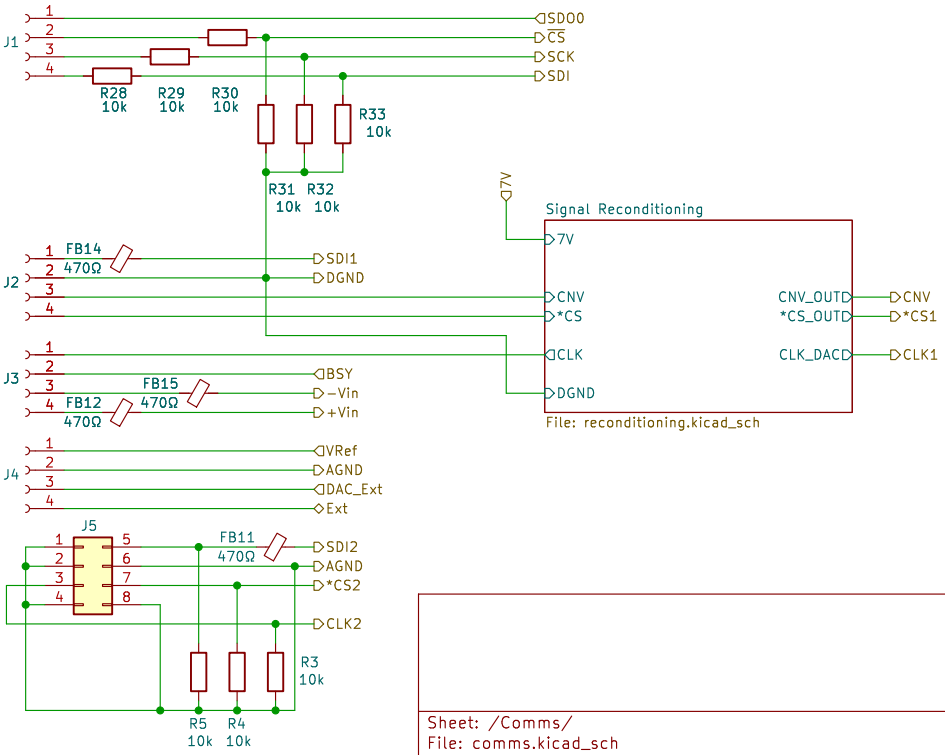


Sheet: /ADC/	
File: adc.kicad_sch	
Title:	
Size: A4	Date:
KiCad E.D.A. 9.0.6	Id: 3/7



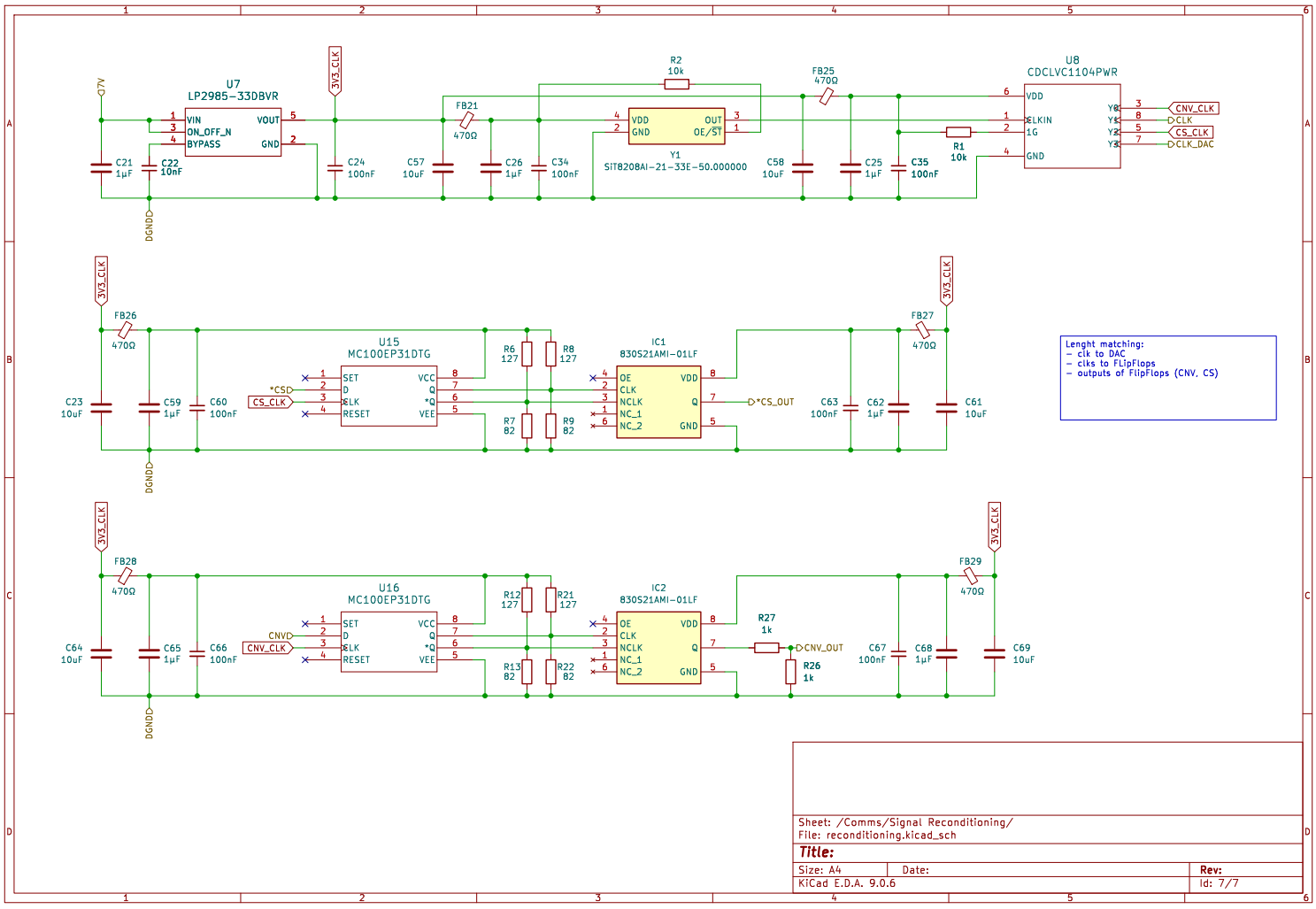
Sheet: /DAC/		
File: dac.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 4/7



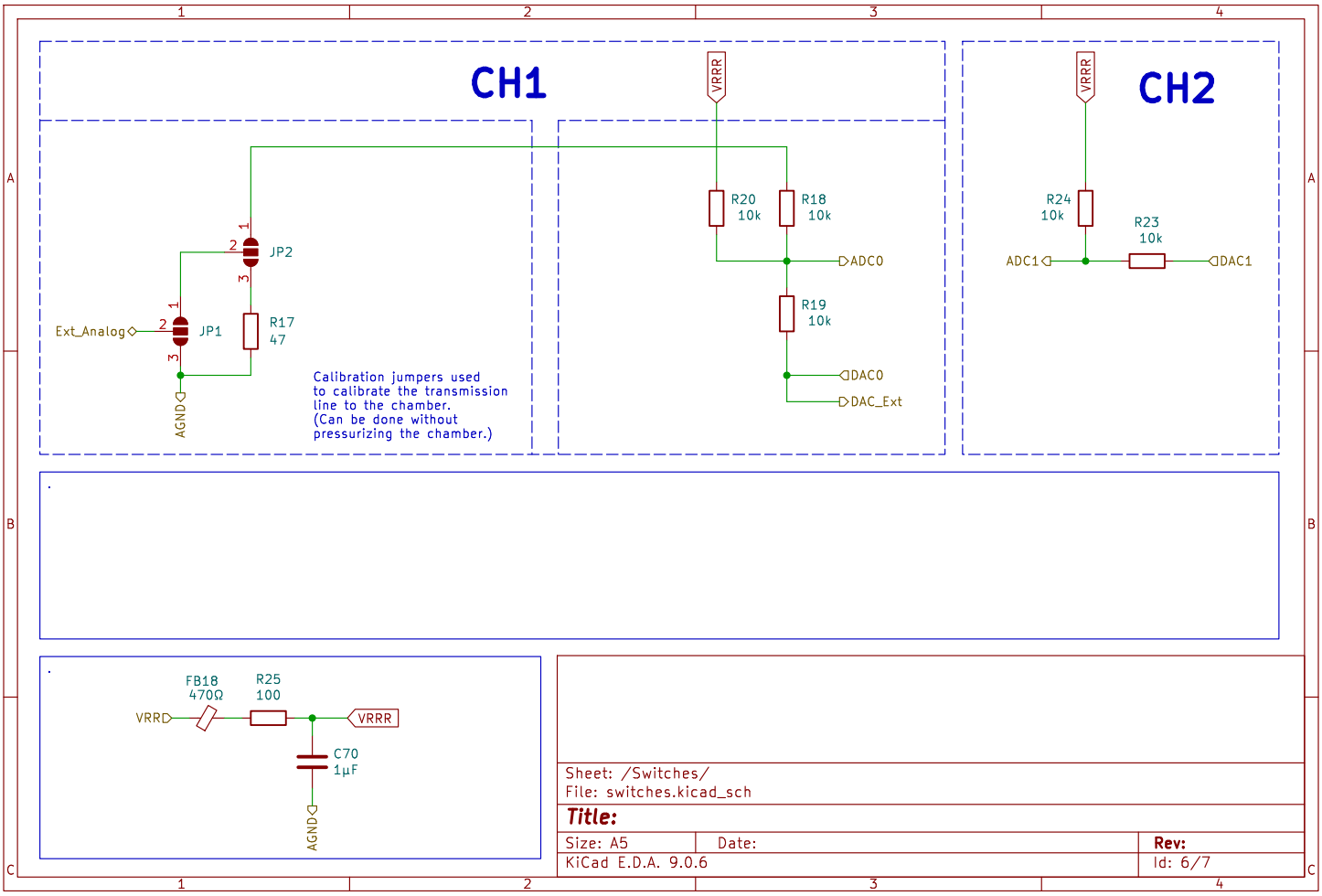
Sheet: /Comms/
File: comms.kicad_sch

Title:

Size: A5	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 5/7



Sheet: /Comms/Signal Reconditioning/		
File: reconditioning.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 9.0.6		Id: 7/7


CH1
CH2
VRRR
VRRR
R20
10k
R18
10k
ADC0
R19
10k
DAC0
DAC_Ext
R24
10k
R23
10k
ADC1
DAC1
JP2
JP1
Ext_Analog
R17
47
AGND
Calibration jumpers used
to calibrate the transmission
line to the chamber.
(Can be done without
pressurizing the chamber.)
FB18
470Ω
R25
100
VRRD
VRRR
C70
1µF
AGND
Sheet: /Switches/
File: switches.kicad_sch
Title:
Size: A5
Date:
Rev:
KiCad E.D.A. 9.0.6
Id: 6/7

C

DAC and ADC Selection

C.1. DAC Candidate Comparison

Table C.1 lists the specifications of the DAC candidates evaluated during the selection process described in chapter 4. Eight candidates were considered across a range of manufacturers and interface types. The key selection criteria were serial interface compatibility, sample rate, resolution, dynamic range, and THD performance.

The majority of high-speed candidates (MAX5888, AD9726, AD9783, AD9144, AD9747), use parallel or high-speed differential interfaces (LVDS, JESD204B) that are incompatible with the 16-wire bulkhead constraint. The AD3552R offers a serial QSPI interface at 33 MSps, but its THD degrades to −84 dB at 100 kHz, falling short of the −100 dB system requirement. The DAC8811 is the only candidate that combines a serial SPI interface, 16-bit resolution, and a THD of −105 dB, while fitting within the wire count constraint. It was therefore selected as the DAC for this design.

Table C.1: DAC Specifications referenced from `DAC specs.xlsx`

Specification	MAX5888	MAX5195	AD9726	AD9783	AD9144	AD9747	DAC8811	AD3552R
Dynamic Range	155dB/Hz	160dB/Hz	160dB/Hz	157dB/Hz	162dB/Hz	160dB/Hz	169.4dB/Hz	158 dB/Hz
THD and Noise	-107dB	–	-95dB	–	-80/-85dB	-80dB	-105 @ 1kHz	-105 dB @1 kHz / -84 dB @100 kHz
Footprint	10mm x 10mm	–	–	–	–	–	very low	5×5 mm
Sampling Rate	500MS/s	260MS/s	400MS/s	500MS/s	2.8GS/s	250MS/s	2MS/s	33 MUPS (fast) / 22 MUPS (precision)
Power Consumption	250mW	–	575mW	315mW	2W	340mW	–	~200 mW est.
Power Rails	3.3V	–	2.5V, 3.3V	1.8V, 3.3V	3.3V, 1.8V	3.3V	–	5V, 1.8V
No. Bits	16	14	16	16 (dual)	16	16	16	16
No. Channels	1	1	1 (4 after demux)	2 (I & Q)	4	2	1	2
Package	68 QFN-EP	–	80 TQF-EP	72 LFCSP	72-pin LGA	48-pin LQFP	–	20-pin LFCSP
Thermal Range	-40 to +85	-40 to +85	-40 to +85	-40 to +85	-40 to +85	-40 to +85	-40 to +125	-40 to +105
Evaluation Board	yes	–	yes	yes	yes	yes	yes	Yes
Stocking Options	–	–	–	–	–	–	–	–
Interface	–	–	LVDS	LVDS	JESD204B	LVCMOS	SPI	QSPI (1/2/4-wire / SDR/DDR)

C.2. ADC Candidate Comparison

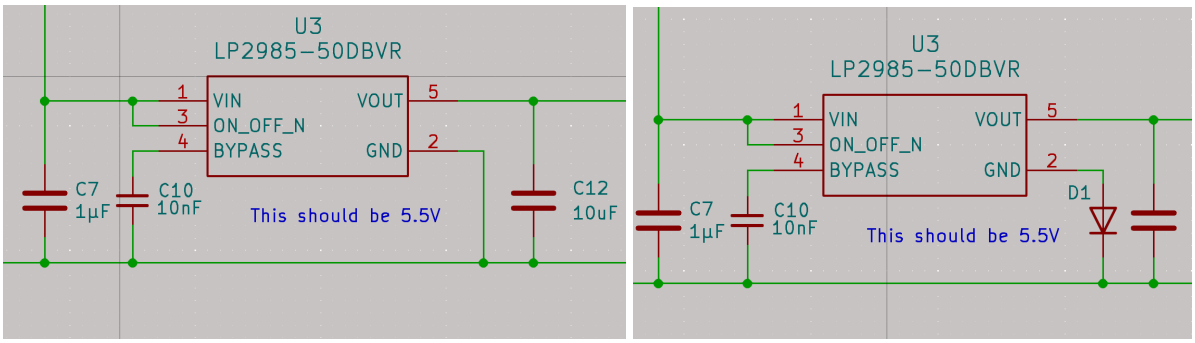
	ADS1675	AD7760	AD4630	AD4081
Dynamic Range	103dB	100dB	107dB	105 (164 dB/Hz)
THD and Noise	-107dB	-105dB	-127dB	−103.7dB at 1MHz
Footprint	1.2cm x 1.2cm	1.2cm x 1.2cm	7mm x 7mm	5mm x 5mm
Sampling Rate	4MSPS	2.5MSPS	2MSPS	20MSPS
Power Consumption	575mW	1W	30mW	68.6mW
Power Rails	5V, 3.3V	2.5V, 3.3V, 5V	5V, 1.8V	3.3V
No. Bits	24bit	24bit	24bit	20bit
No, Channels	1ch	1ch	2ch	1ch
Package	64 TQFP	64 TQFP	64 BGA 0.8mm	49 BGA 0.65mm
Thermal Range	-40 to 85	-40 to 85	-40 to 125	-40 to 85
Evaluation Board	Not really	Yes	Yes!	Yes
Stocking Options	775 (DigiKey)	706 (DigiKey)	1600 (DigiKey)	954 (DigiKey)
Communication Interfaces and Bandwith	LVDS or SPI (96Mbps)	16bit Parallel (5Mbps)	SPI (96Mbps, 1 - 4 SPI data lanes)	LVDS, QSPI (200Mbits), SPI (50Mbits)
Link	Link	Link	Link	Link
Notes		Built-in input filters		

D

Circuit Fixes and Post-production Adjustments

03-06-2026 - ADC chip requiring 5.3V at the VDD pin instead 5V

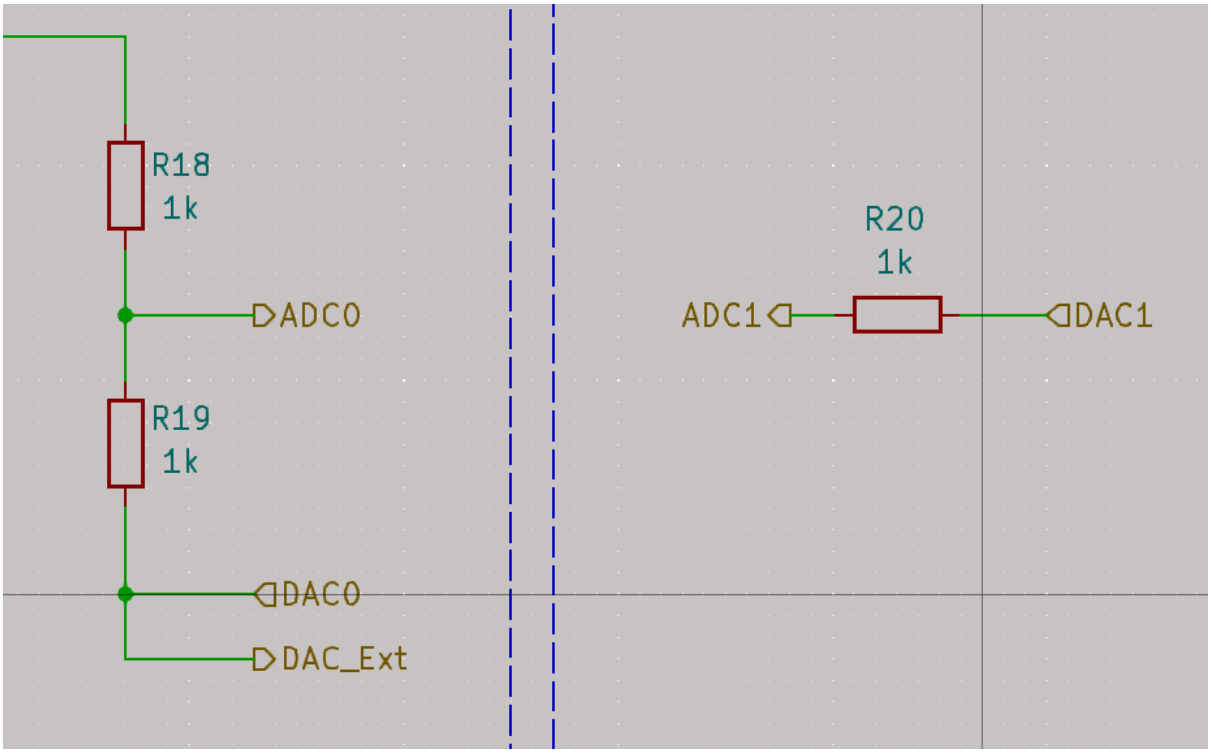
ADC chip requires the voltage at its VDD pin to be 5.3V to 5.5V for a 5V voltage reference source. The linear regulator for this supply was chosen to be 5V. The solution to boost its voltage to 5.3V is to use a diode between the ground connection of that chip and ground. The circuit below on the left is before, and the circuit on the right is after.



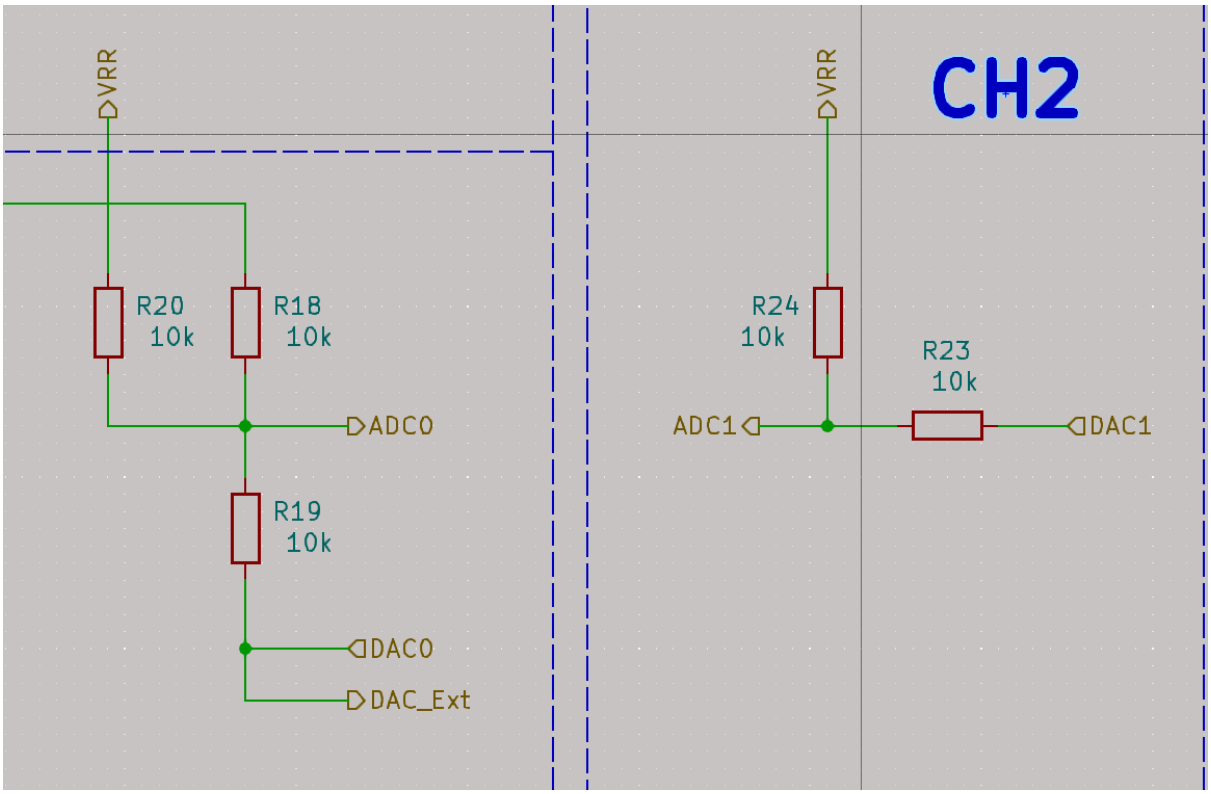
03-06-2026 - DAC outputs a negative voltage that the ADC can’t take

In the design of the DAC circuit, it was not noticed that the operational amplifier would output a negative voltage that the ADC wouldn’t tolerate, thus they cannot be connected together. The solution is to boost the resistances on the summing node and add one more resistor connected to the VRef. This way, the output of the DAC will be summed with VRef and biased up, allowing the summing node to swing between VRef/2 and 0V, instead of 0V to -VRef that the DAC produces. Halving the swing of the signal is acceptable because the resolution of the ADC is significantly higher than the resolution of the DAC (24bits vs 16bits).

Before:



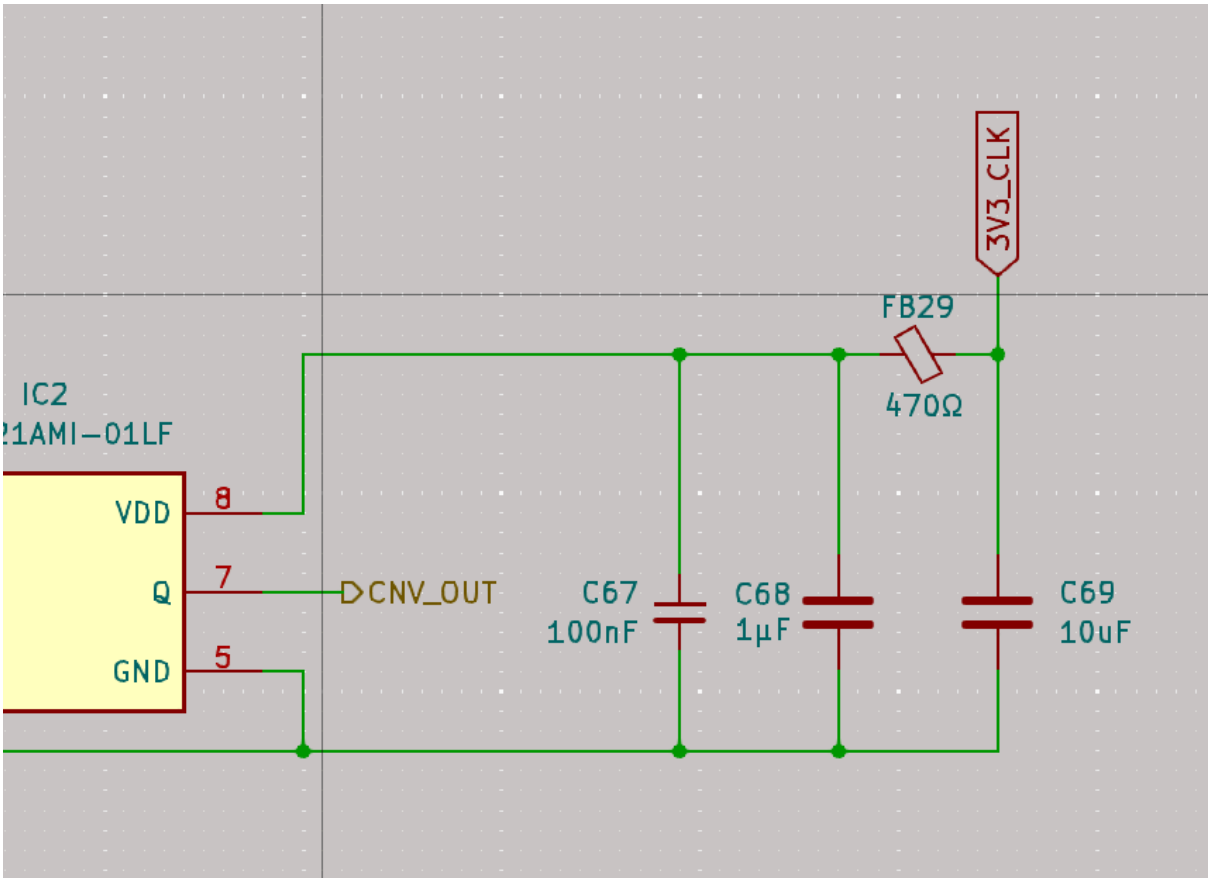
After:



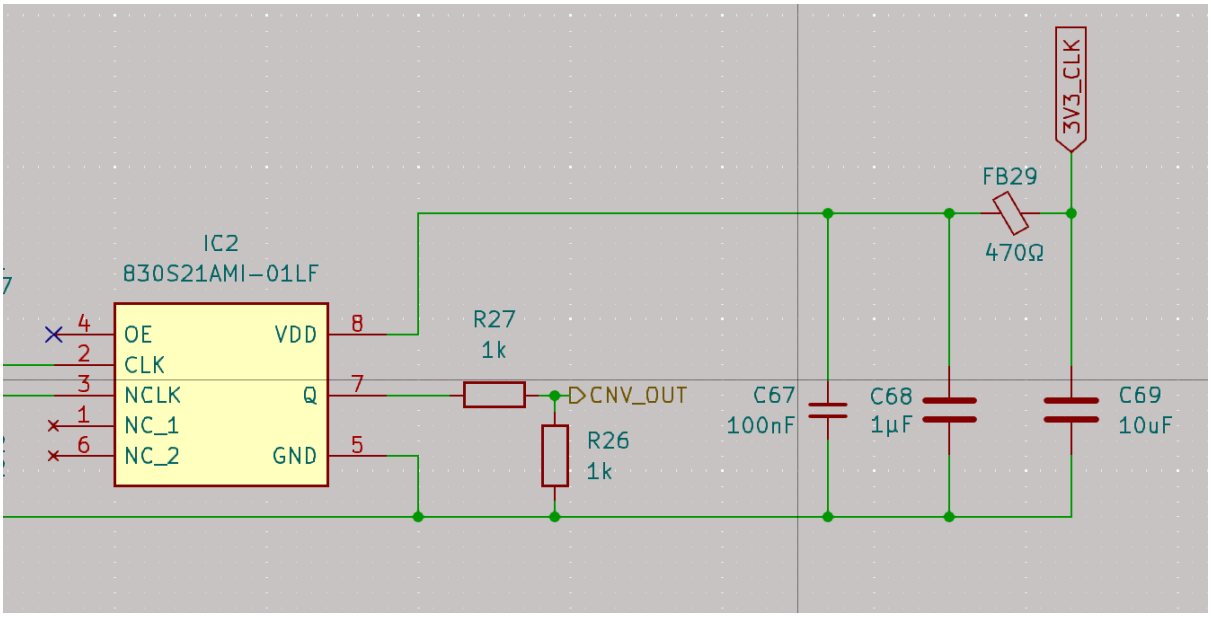
10-06-2026 Output of the media converter for the CNV signal is 3.3V, while the ADC can only take 1.8V

Adding a voltage divider will fix that.

Before:



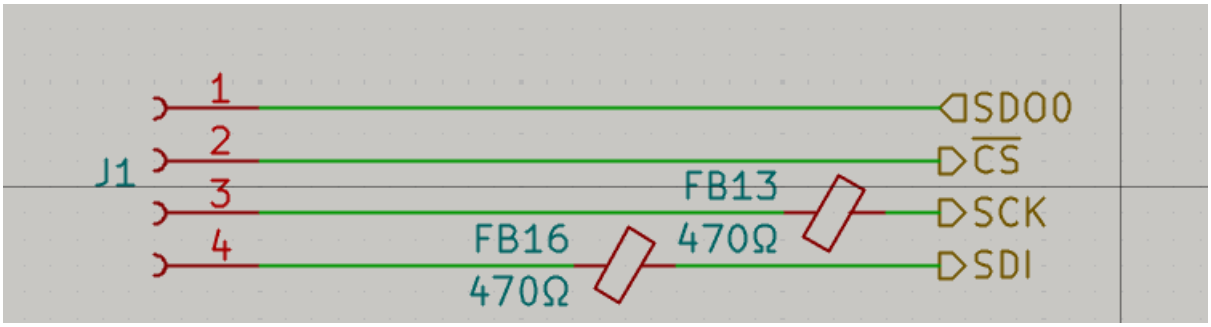
After:



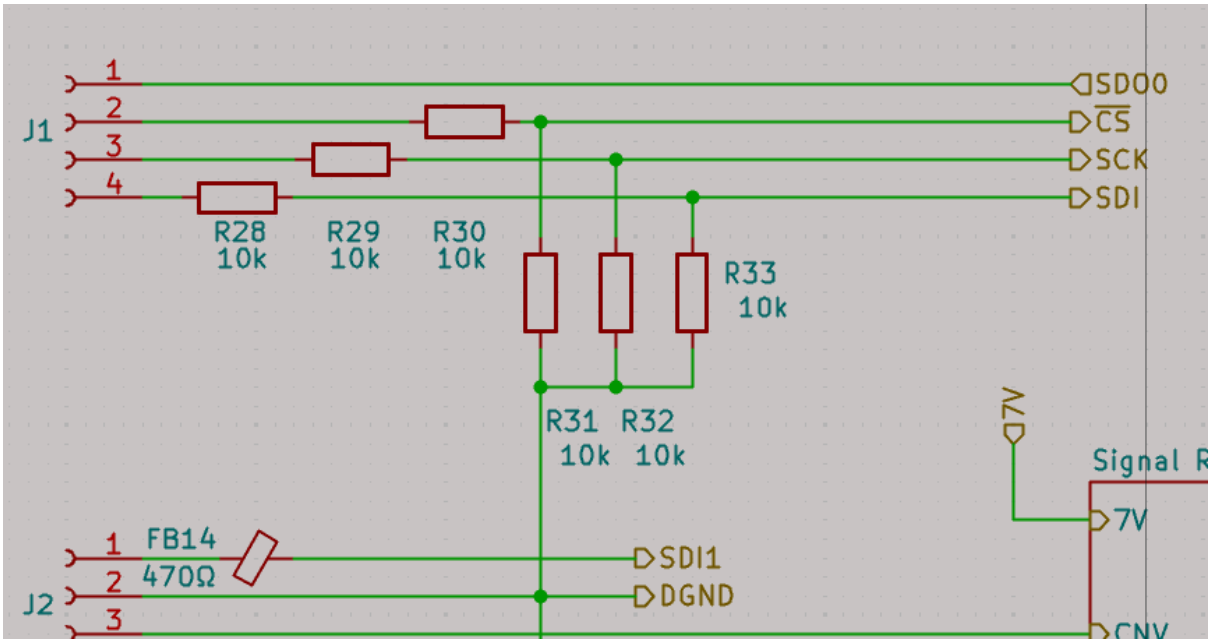
11-06-2026 Output of the FPGA can’t be set to 1.8V so it’s 3.3V, while the ADC can only take 1.8V

Calculated the parasitic capacitance of the traces as coplanar waveguides. It turned out to be about 2pF, so added 10k resistors in series, as the delays were deemed to be manageable.

Before:



After:



E

Schematics and Figures

E.1. Schematics

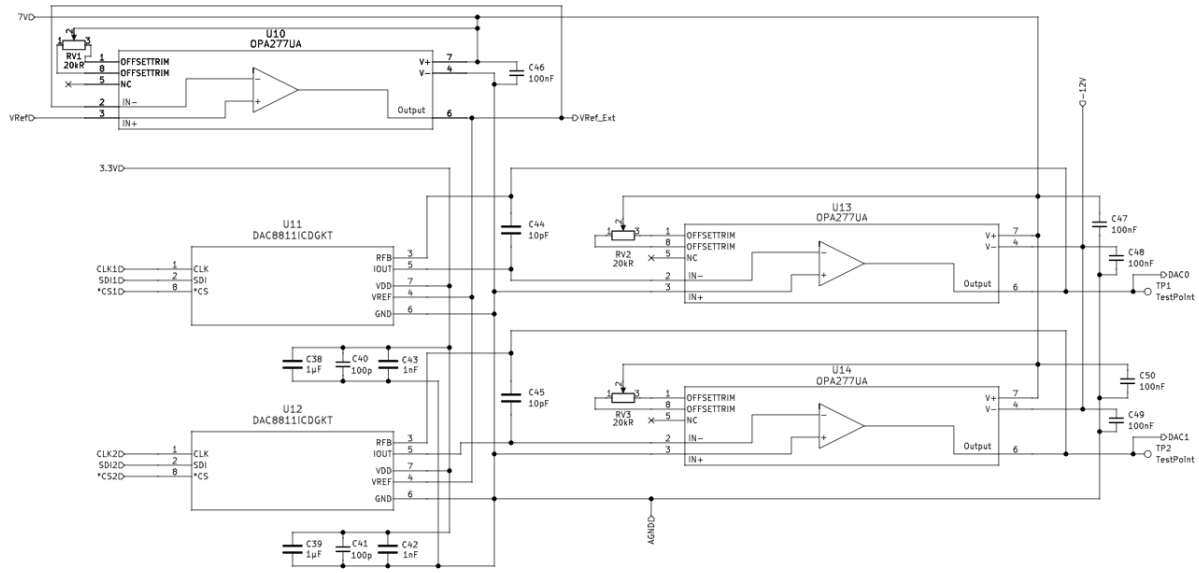


Figure E.1: Schematic DAC circuit

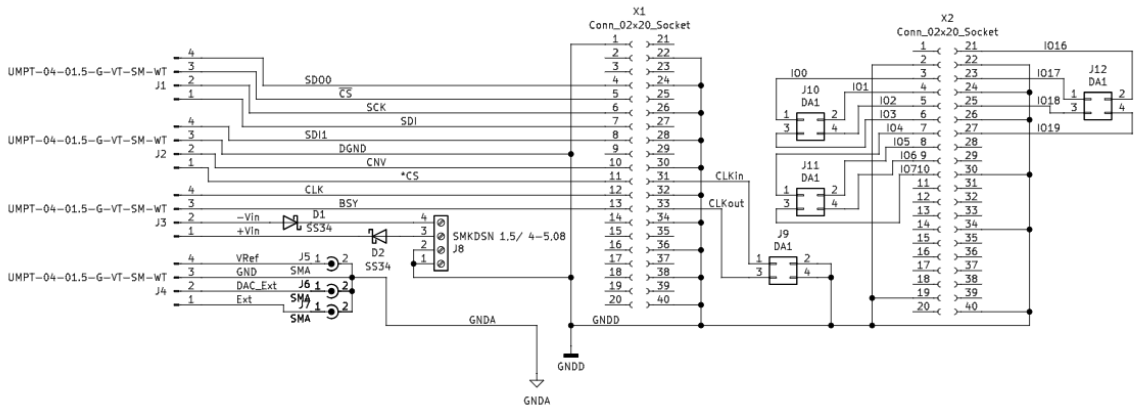


Figure E.2: Schematic breakout board

E.2. Figures

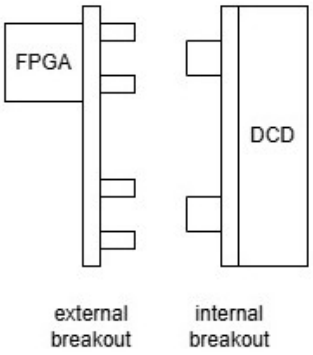


Figure E.3: connection for testing

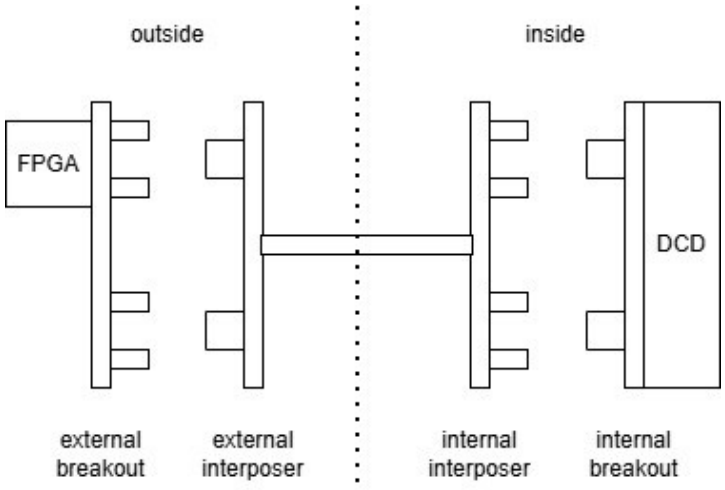


Figure E.4: connection for testing with pressure chamber

F

PCB Parameters

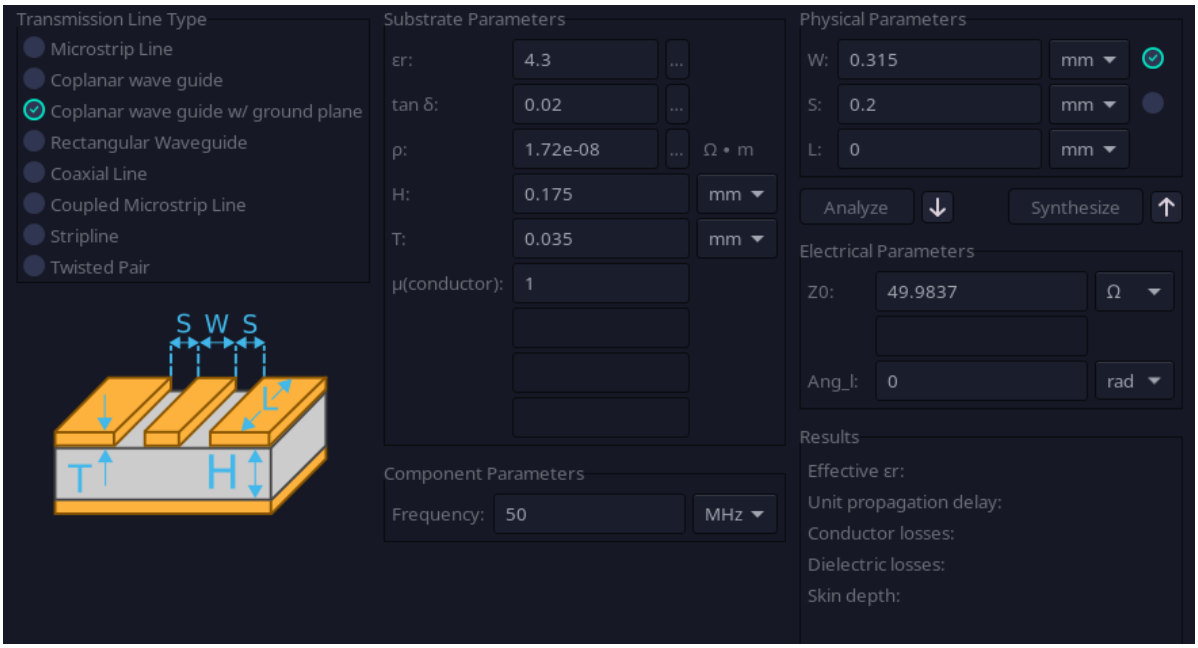


Figure F.1: calculated trace sizes

G

PCBs Layout and Render

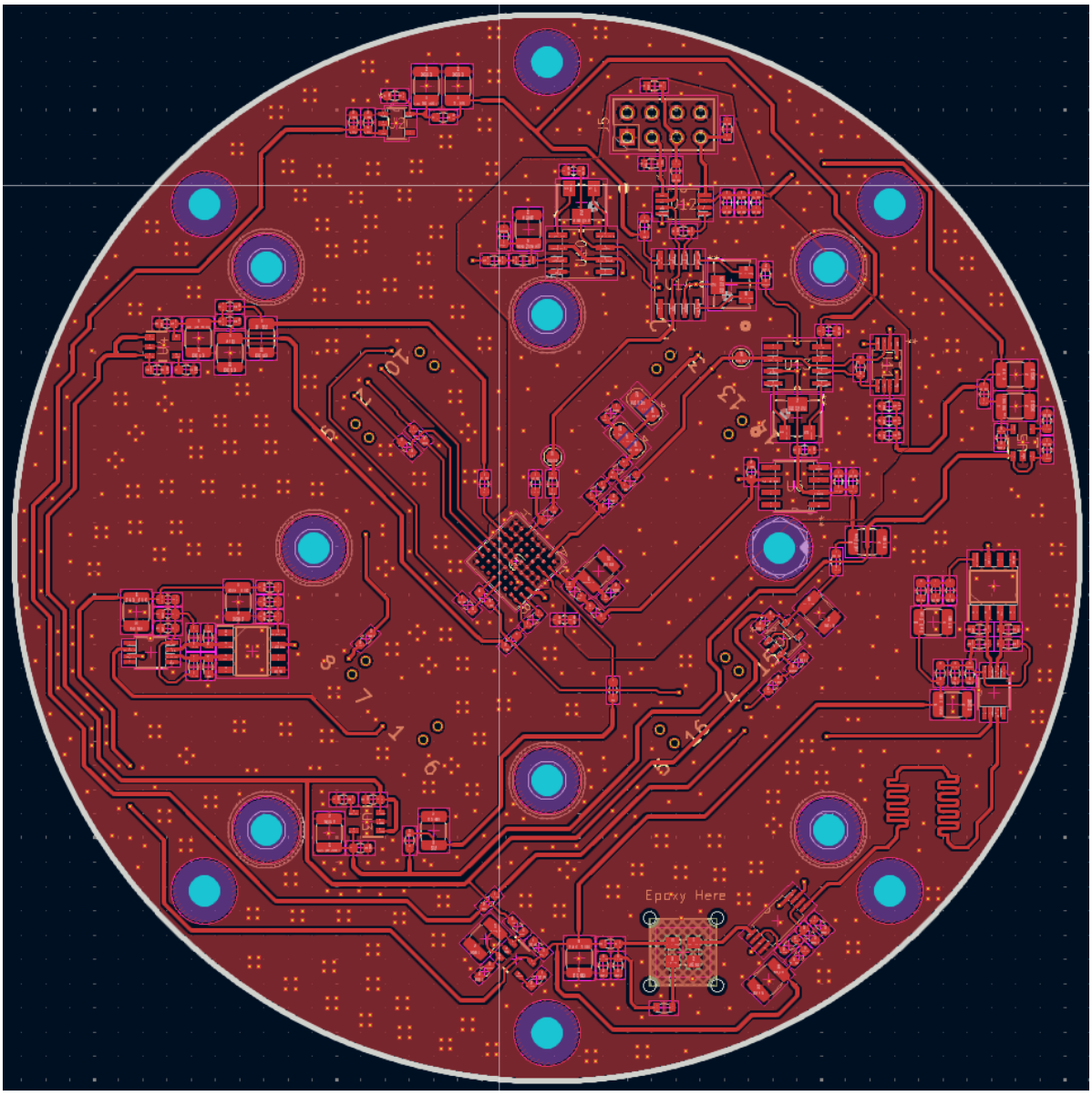


Figure G.1: DCD Layout Front

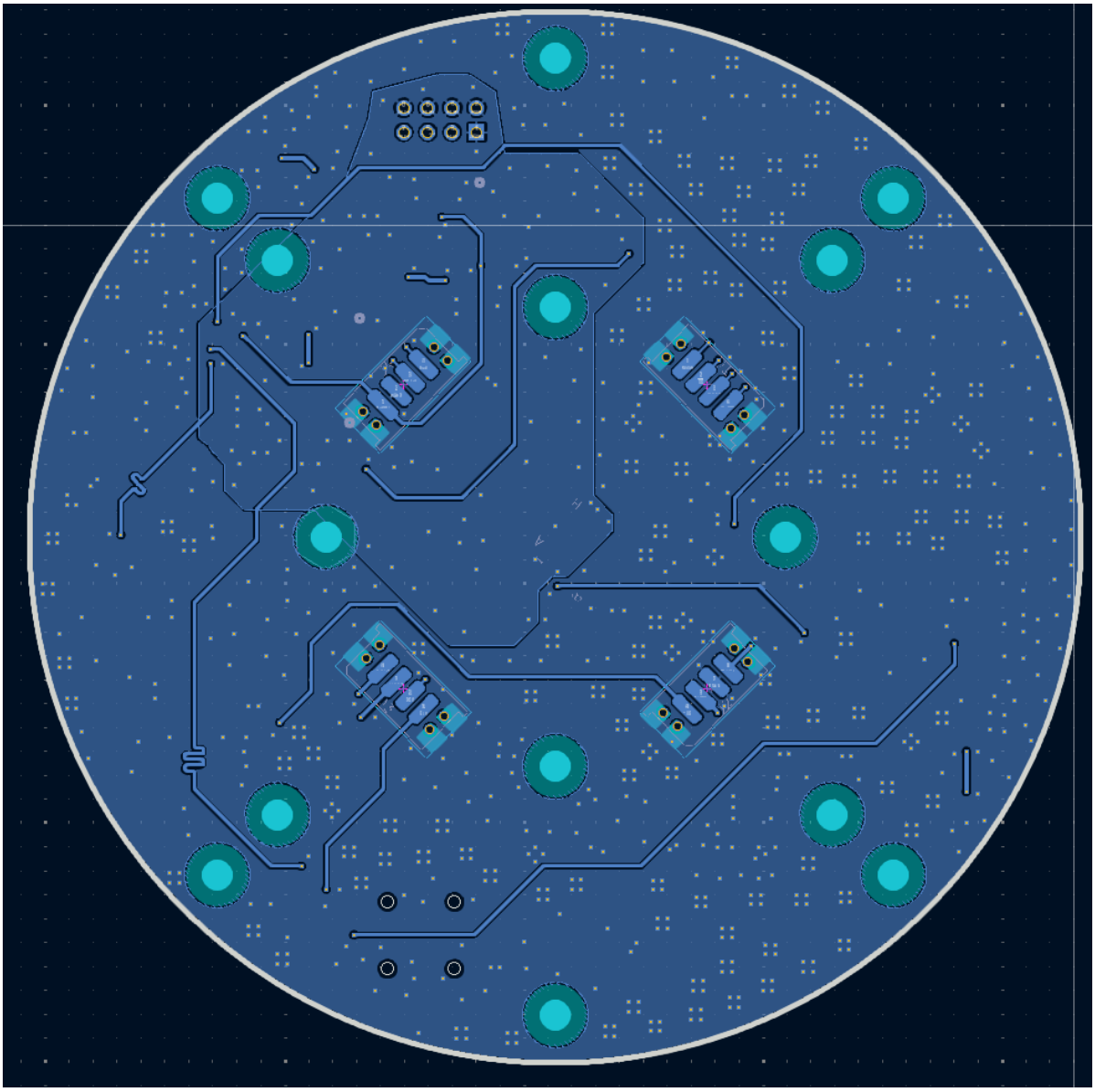


Figure G.2: DCD Layout Back

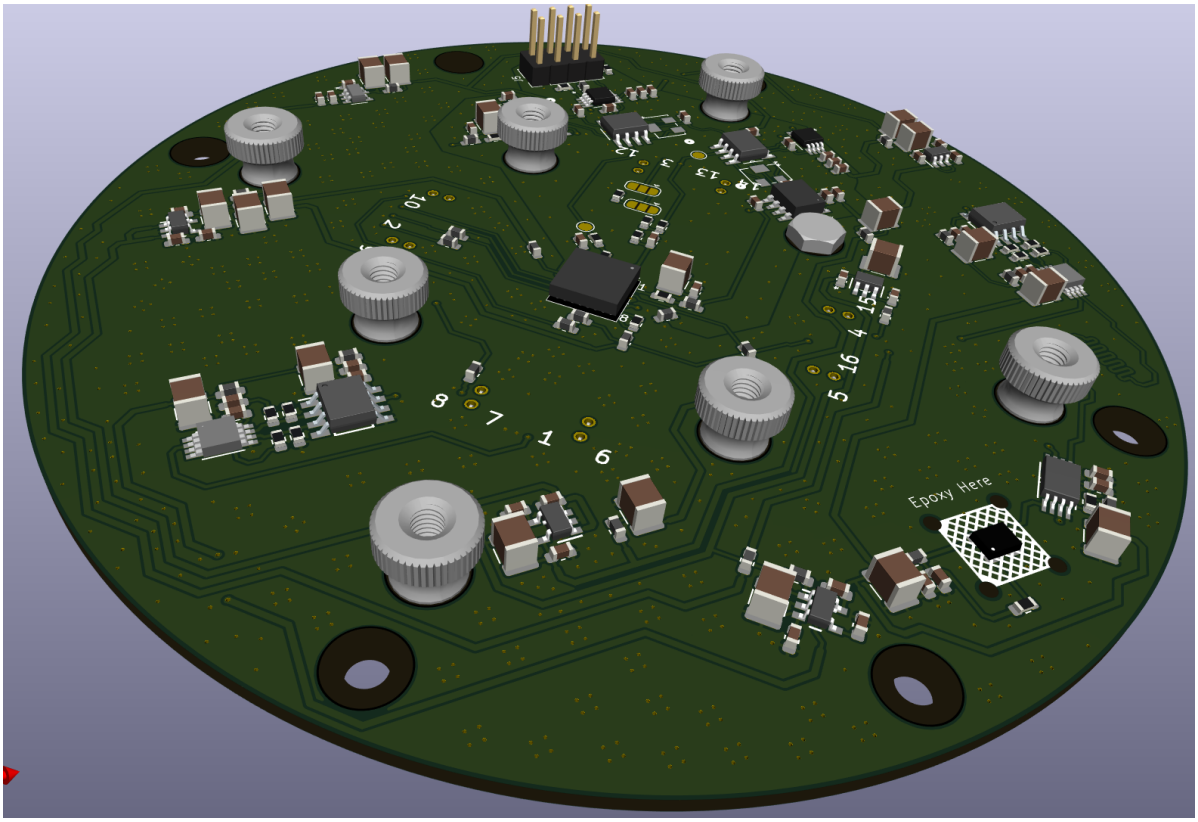


Figure G.3: DCD Render Front

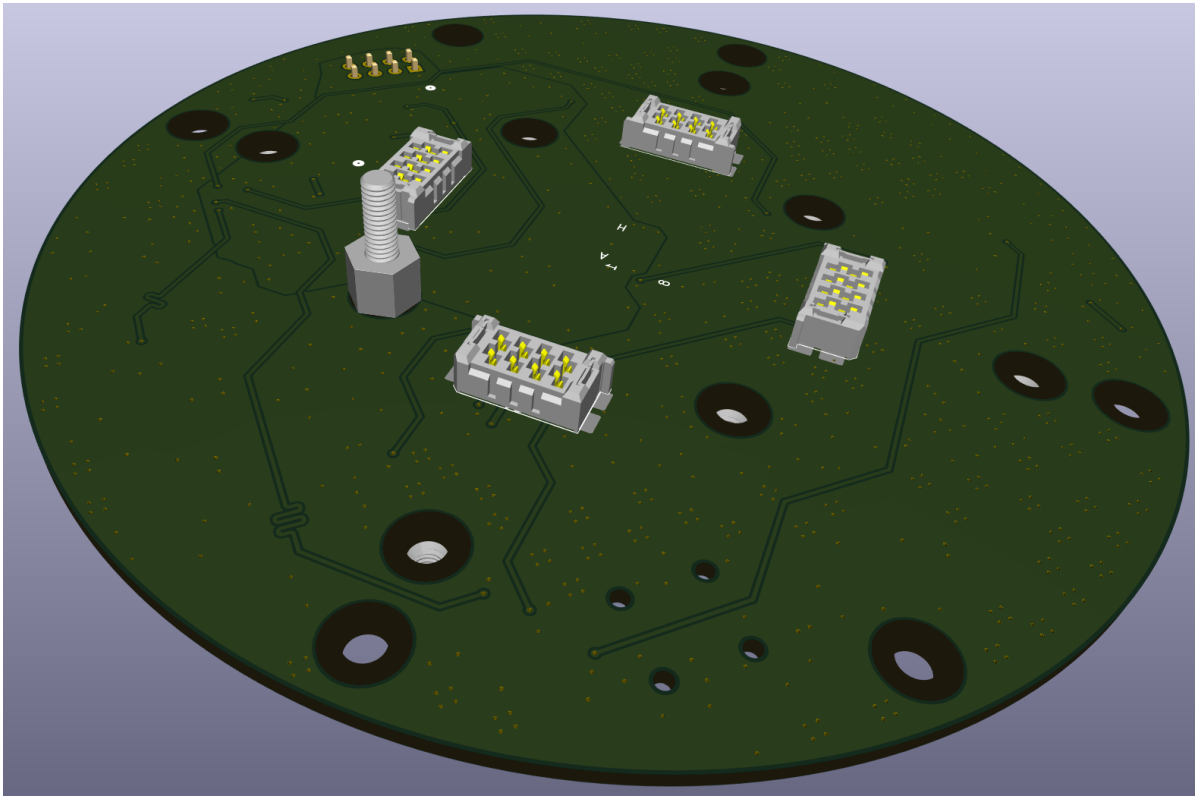


Figure G.4: DCD Render Back

G.1. external breakout board

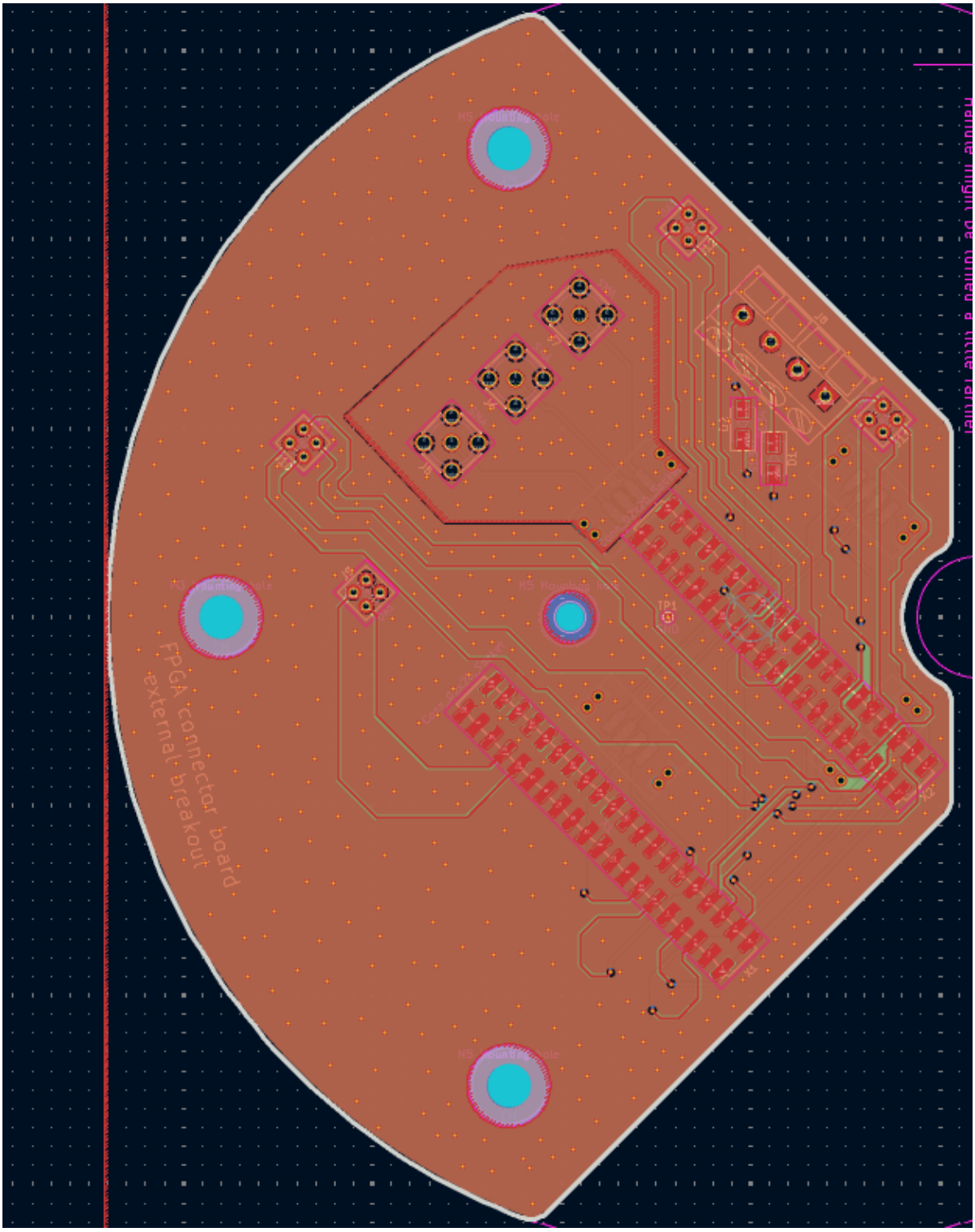


Figure G.5: external breakout layout front

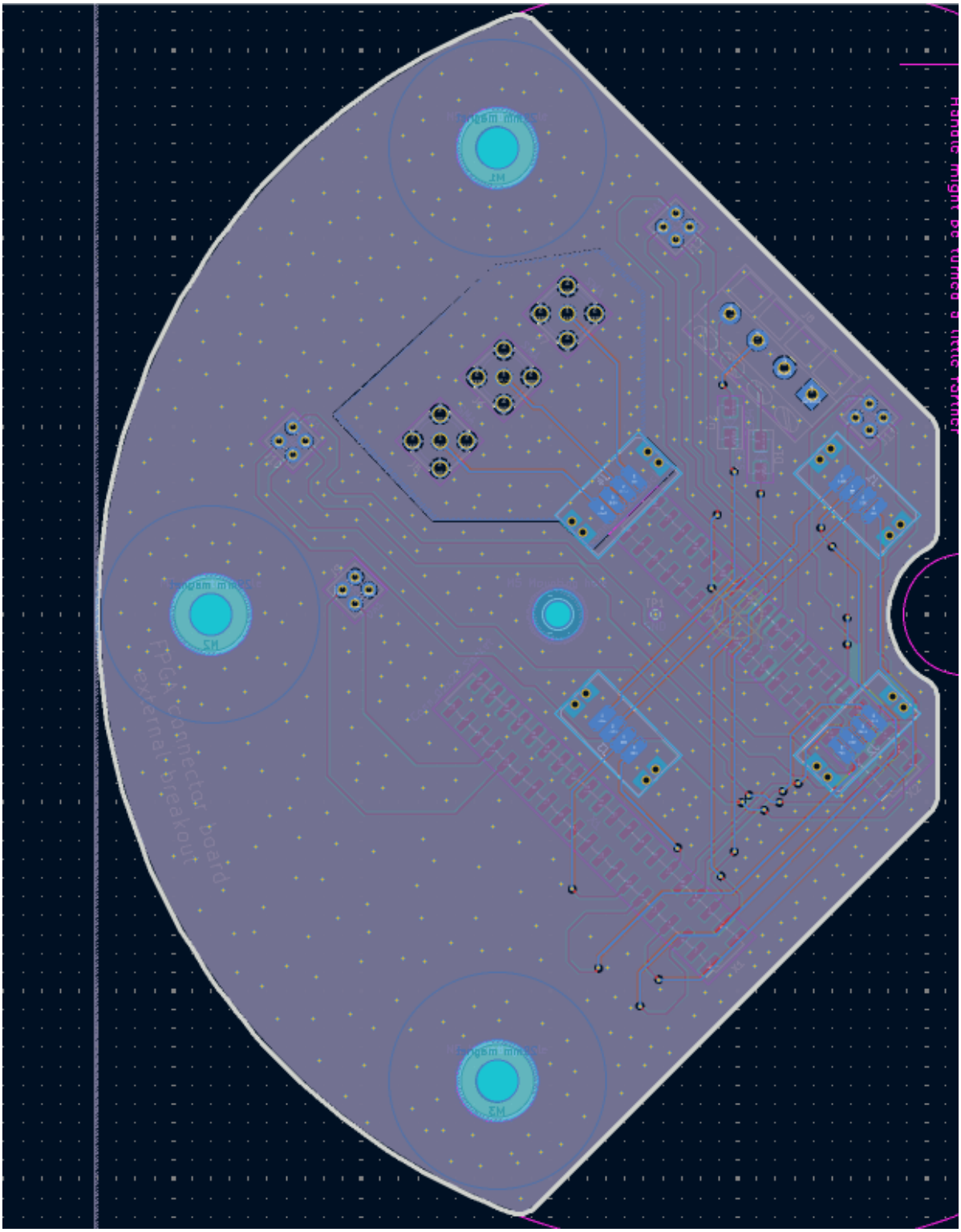


Figure G.6: external breakout layout back

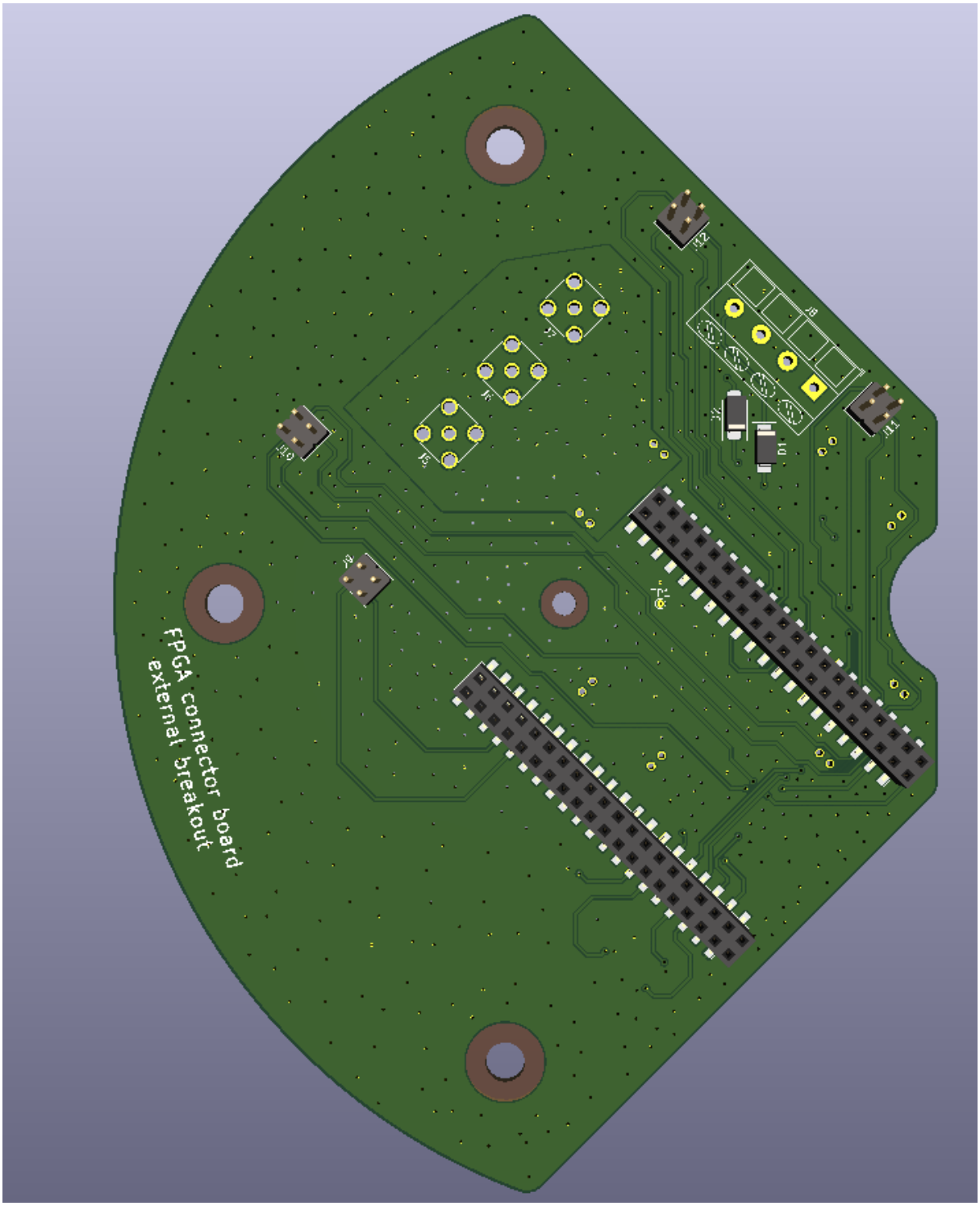


Figure G.7: external breakout render front

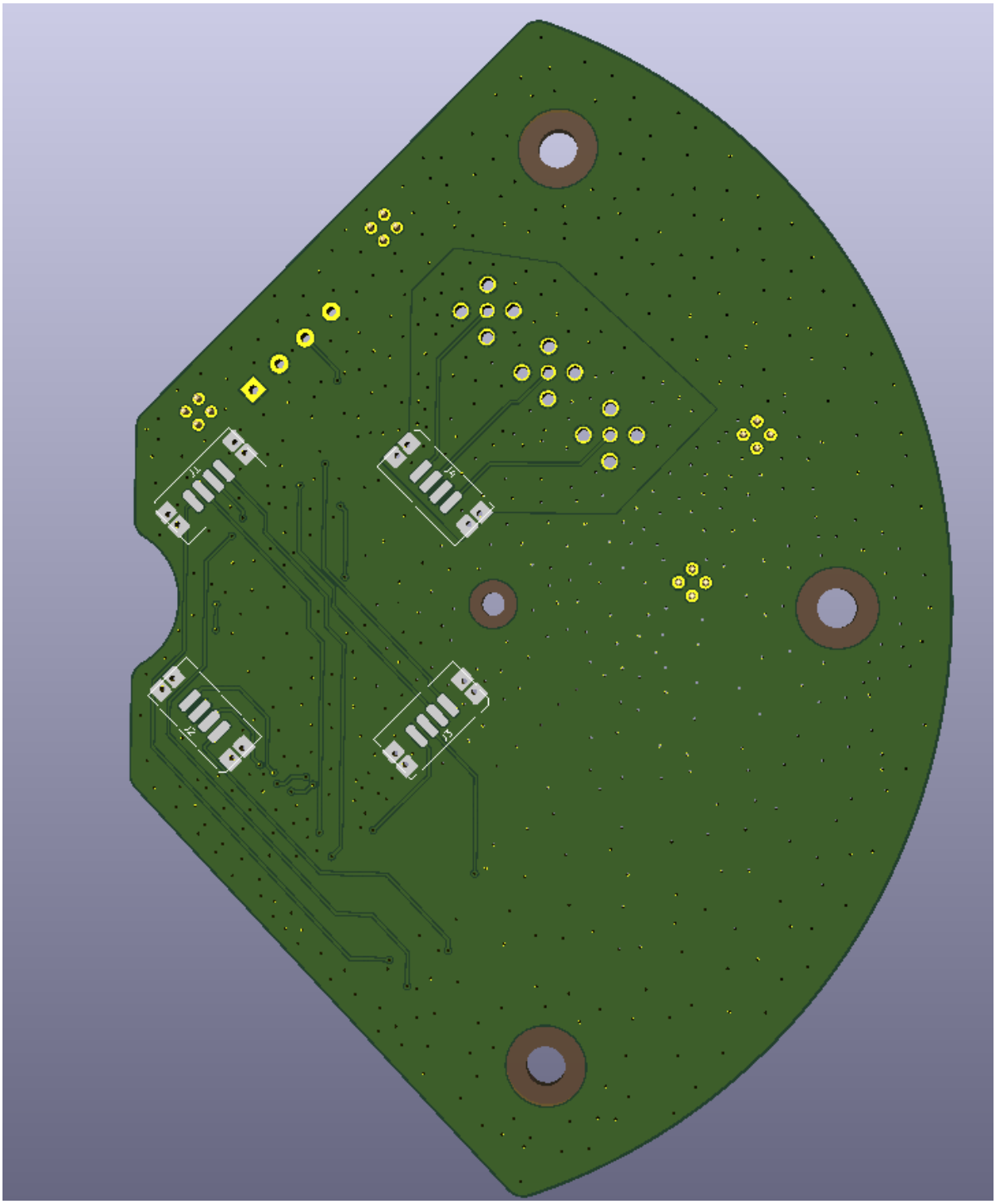


Figure G.8: external breakout render back

H

Draft of component placement of a 16-channel board

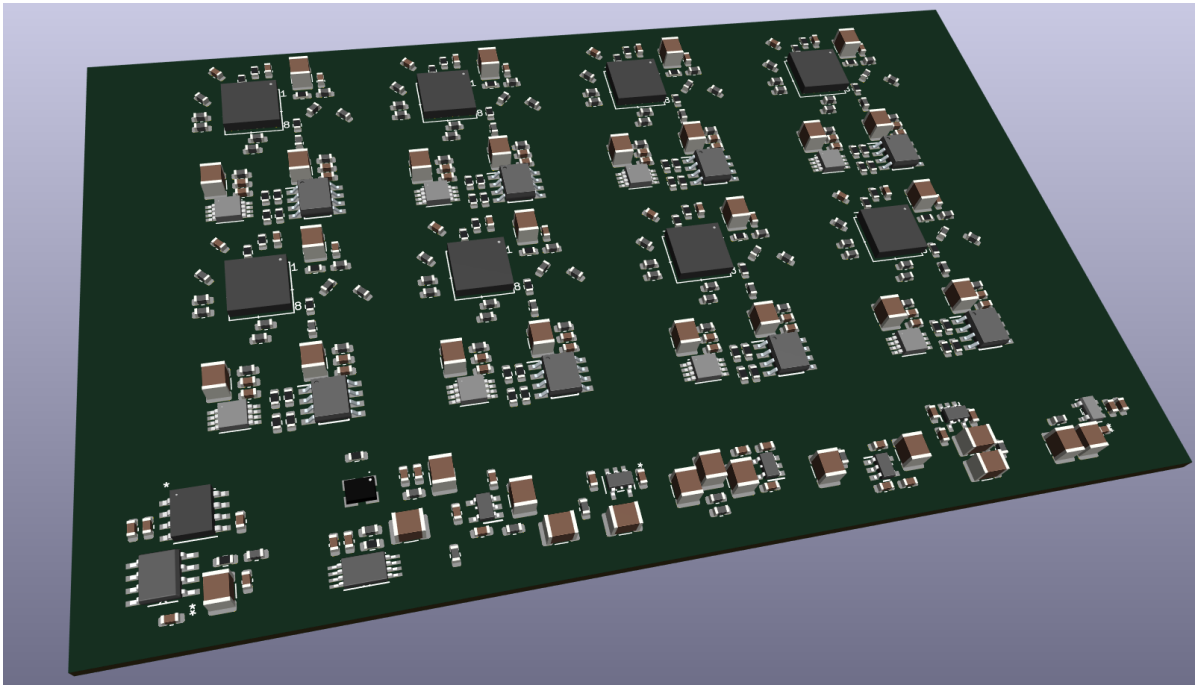


Figure H.1: Component placement front

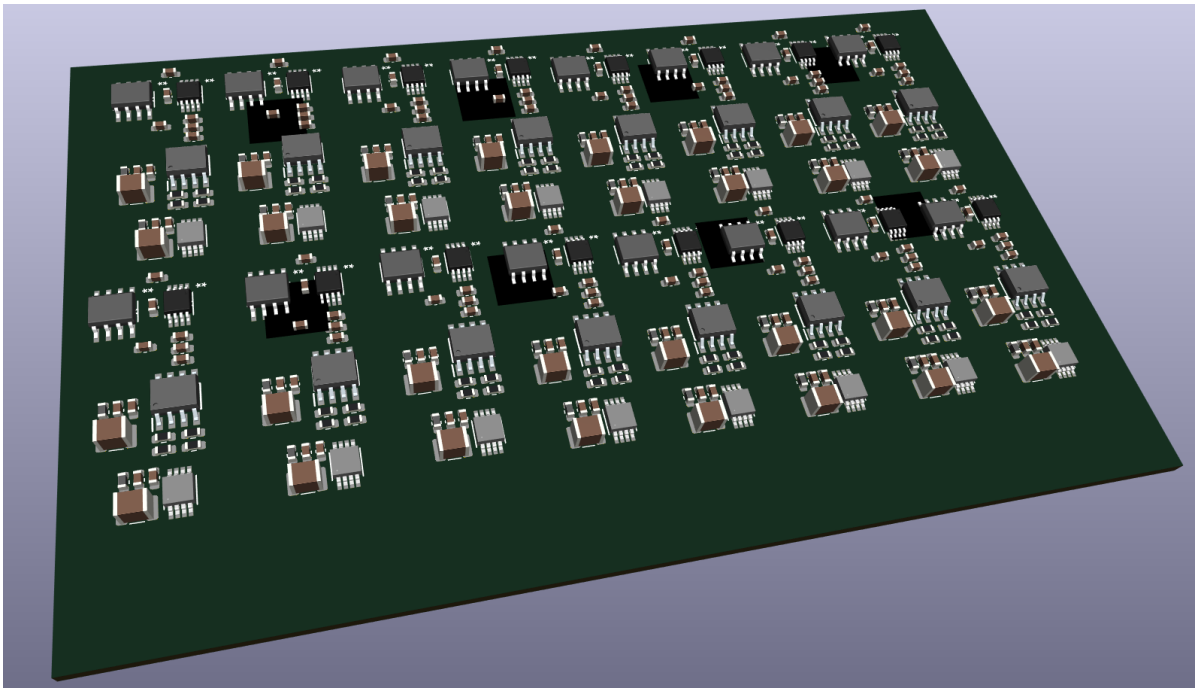


Figure H.2: Component placement back

I

Bill of Materials for the DCD board

Table I.1: Bill of materials with bibliography references

Ref.	Qty	Value
B1	1	DIN933 M3x14mm
C1–C3,C7,C9,C16,C21,C25,C26,C27,C38,C39,C59,C62,C65,C68,C70	17	1 μF
C4,C5,C12,C13,C18,C20,C23,C30,C31,C51,C52,C53,C54,C55,C56,C57,C58,C61,C64,C69	20	10 μF
C6,C8,C14,C15,C19,C24,C28,C29,C32,C33,C34,C35,C46,C47,C48,C49,C50,C60,C63,C66,C67	21	100 nF
C10,C11,C17,C22	4	10 nF
C36,C37,C42,C43	4	1 nF
C40,C41	2	100 pF
C44,C45	2	10 pF
D1	1	1N4148WT
FB1–FB12,FB14,FB15,FB17–FB29	26	470 Ω
H15	1	Spacer M3x5mm
IC1,IC2	2	830S21AMI-01LF
J1–J4	4	UMPS-04-03.5-G-VT-SM-WT
J5	1	Conn_02x04_Top_Bottom
JP1,JP2	2	SolderJumper_3_Open
N1–N7	7	M3 Thumbnut
R1–R5,R16,R18–R20,R23–R24,R28–R33	17	10 kΩ
R6,R8,R12,R21	4	127Ω
R7,R9,R13,R22	4	82Ω
R10,R11,R14,R15,R25	5	100Ω
R17	1	47Ω
R26,R27	2	1 kΩ
RV1–RV3	3	20 kΩ
TP1,TP2	2	TestPoint
U1	1	TLV76780DBVR
U2	1	ADP7182AUJZ-1.8-R7
U3	1	LP2985-50DBVR
U4	1	LP2985-18DBVR
U5,U7	2	LP2985-33DBVR
U6	1	ADR4550BRZ
U8	1	CDCLVC1104PWR
U9	1	AD4630-24BBCZ
U10,U13,U14	3	OPA277UA
U11,U12	2	DAC8811ICDGKT
U15,U16	2	MC100EP31DTG
Y1	1	SiT8208AI-21-33E-50.000000

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