# A Capacitively-Coupled Autozeroed and Chopped Operational Amplifier

By

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## Abstract

This thesis describes the design and simulation of a capacitively-coupled autozeroed and chopped operational amplifier in the TSMC high-voltage BCD 0.18 µm 5 V technology. It uses chopping and autozeroing to achieve high precision (10 µV offset and 50 nV/√Hz noise density) and a capacitively-coupled input stage to safely handle beyond-the-rails 50 V input voltages. The amplifier employs a pseudo-continuous time architecture that periodically autozeroes a single signal path, which is also chopped. Compared to amplifiers with ripple-reduction loops, this approach should potentially result in area and power savings. However, it also means that the signal path is periodically broken during a short deadtime, during which the signal path is autozeroed. Since the presence of the deadtime comes with a noise penalty, the amplifier's clocking scheme has been optimized to reduce the length of the deadtime relative to the length of the two amplification phases. The simulated performance of the resulting amplifier is comparable with that of other precision amplifiers, while its chip area should be lower, resulting in lower production costs.

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# 1. Introduction

## 1.1. Operational Amplifiers

Electronic amplifiers are used in many applications to convert small electrical signals into larger versions that are easier to process and convert into digital signals. Several applications, such as medical devices, electric cars, and smart homes, are depicted in Figure 1.1. In these applications, precision amplifiers are often used to boost the tiny signals output by typical sensors. Since no practical amplifier can be ideal, many distinct types of amplifiers have been designed to address the specific challenges of particular applications. Semiconductor manufacturers such as Analog Devices and Texas Instruments boast device catalogs of thousands of amplifiers [1] [2].

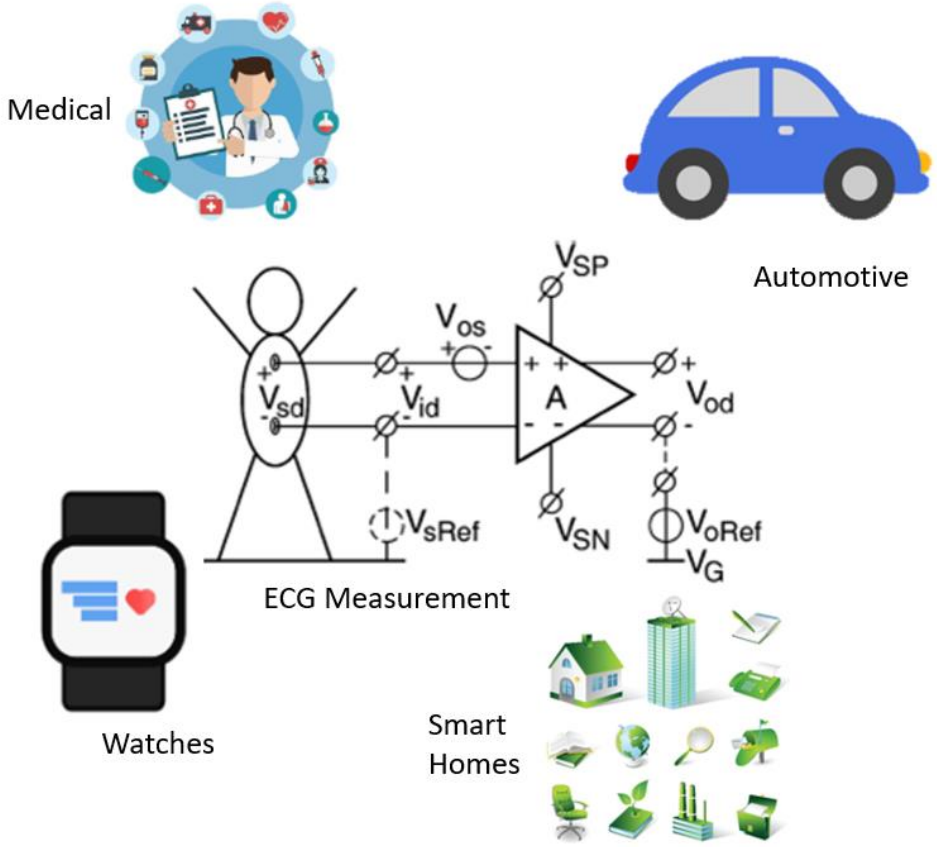


*Figure 1.1 Amplifiers and their broad reach [3]*

One of the first and probably the most well-known monolithic amplifiers is the 741 op-amp. It was designed in 1968 by David Fullagar of Fairchild Semiconductor. Since then, tens of millions of 741 amplifiers have been sold [4] [5].

Amplifiers can be categorized into many sub-groups with different characteristics. A differential amplifier has differential input signals. A fully differential amplifier has differential inputs and outputs. An instrumentation amplifier is a differential amplifier with a high input impedance and a well-defined gain. An isolation amplifier is a differential amplifier with a high common-mode voltage functionality. An operational amplifier is a differential amplifier with an extremely high gain.

Operational amplifiers are usually used as general-purpose gain blocks. Combined with feedback, their high open-loop gain results in an accurately defined closed-loop gain. Operational amplifiers are widely used in noisy environments to get an accurate and precise reading of sensor data. They are designed to be robust to common-mode interference, such as 50/60 Hz pickup from the mains. They are often packaged in plastic for low cost in mass production, as shown in Figure 1.2.

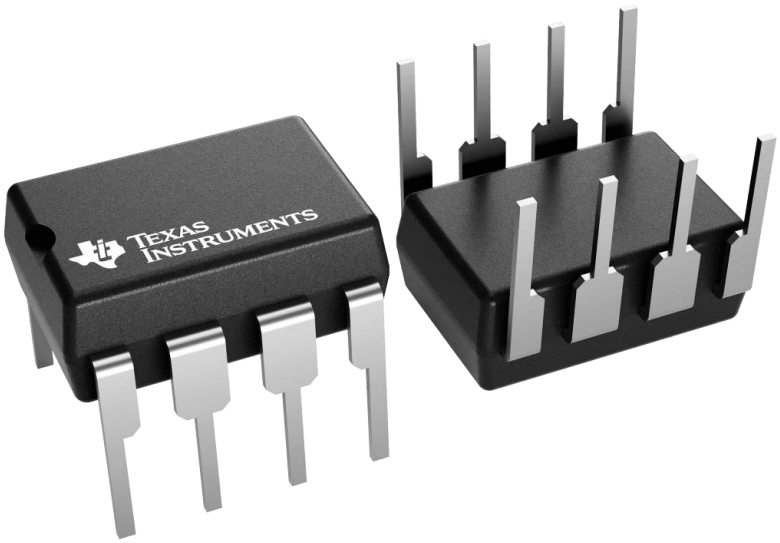


*Figure 1.2 Operational Amplifier Package [6]*

This thesis describes the design of an operational amplifier that addresses the challenge of amplifying input signals that can range outside the supply rail voltages with an offset of a few microvolts.

## 1.2. Amplifier Specs

The operational amplifier architecture described in this thesis must be simple, general purpose, low noise, low power, have isolated inputs, and have a small chip area, and therefore be low cost. The following subsections discuss some of the resulting amplifier's characteristics in more detail [7] [8].

### 1.2.1. Gain

The closed-loop gain of an amplifier with a finite open-loop gain depends on the loop gain (Aβ), open-loop gain (A), and the feedback factor (β). If the open-loop gain (A) is infinite, then the closed-loop gain is equal to the inverse of the feedback factor (1/β). The closed-loop gain is $A/(1+A\beta) \approx 1/\beta$. An operational amplifier (op-amp) has high gain and is usually used with feedback, as shown in Figure 1.3 [9].

The proposed amplifier should have enough open-loop gain to sustain a well-defined closed-loop gain of 100 or 40 dB. In addition, the amplifier's residual offset should be in the µV range. Assuming a 1 V output voltage, achieving a 1 µV overdrive voltage needs a gain of 120 dB. Together, these two constraints result in a minimum open-loop gain of 160 dB. However, to take manufacturing spread into account, a nominal gain of 180 dB is targeted. This very high gain can be achieved in two ways: by implementing a single stage with a very high gain or by cascading a number of stages with lower individual gains.

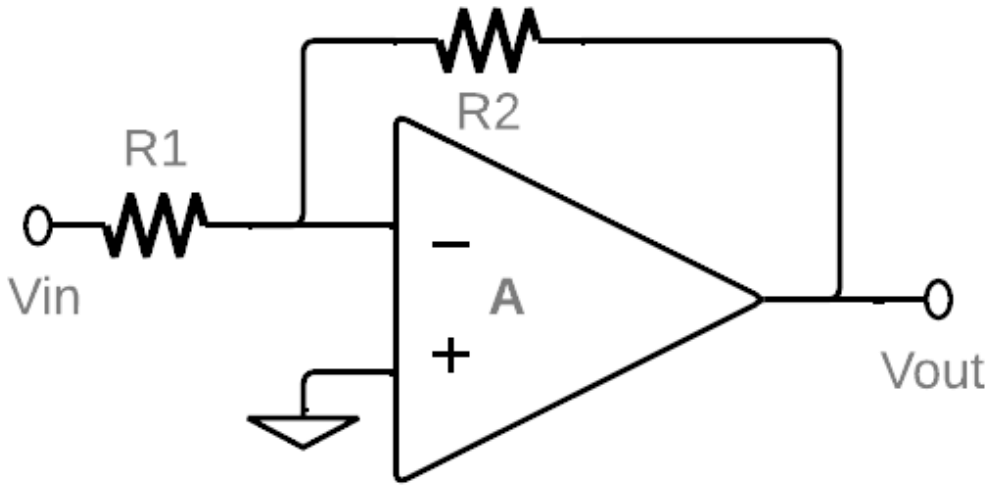


*Figure 1.3 Op-Amp with Negative Feedback*

### 1.2.2. Input Impedance

The higher the input impedance of an op-amp is, the less loading there is on the input source and the feedback network. A common-mode input impedance of more than 1 GΩ is often required. In real op-amps, a small common-mode biasing current flows into both inputs. These input currents are never precisely matched, and their difference combined with high source or feedback impedances creates an extra error voltage [7]. This can be a problem when targeting low offset. Therefore, a low input bias current of less than 100 pA is targeted to be competitive with the state of the art [10].

### 1.2.3. Input and Output Range

An ideal op-amp can handle any input voltage and deliver any output voltage. However, real op-amps have limits to both. Usually, their input and output ranges are limited by the supply rails. Rail-to-rail op-amps can swing close to the supply rails for their input and output without degrading the linearity. The proposed amplifier should process rail-to-rail input and output signals that range from ground to the supply voltage (VDD).

In advanced CMOS processes, supply voltages may be lower than 1 Volt. This development benefits low-power systems, but it limits the input voltage range. Despite the small input signals, the input common-mode voltage can be beyond the supply voltage in many applications, such as battery monitoring. To overcome this issue, a rail-to-rail or beyond-the-rail input stage can be designed to alleviate the supply rail limit on the common-mode input voltage range. The proposed amplifier should have rail-to-rail input and output stages.

### 1.2.4. Noise

Noise is the name given to undesired random variations in the magnitude of an electric signal. It is commonly expressed as a spectral density in Volts per root Hertz (V/√Hz) or Amps per root Hertz (A/√Hz). The three relevant types of noise for this operational amplifier are thermal noise, flicker noise, and sampling noise.

Thermal noise, often called white noise, is caused by charge carriers moving around with thermal energy in a resistor. It has a flat spectrum and extends (in principle) over an infinite bandwidth.

Flicker, 1/*f*, or pink noise is usually caused by non-ideal material properties and device fabrication. It has a 1/*f* noise spectrum, meaning its noise power increases as frequency decreases.

Capacitors themselves do not exhibit thermal noise, but every conductor does, and so sampling a voltage on a capacitor will also store this noise on the capacitor [7] [8] [11]. The total noise power is given by kT/C. This amplifier aims for a low noise spectral density of less than 50 nV/√Hz.

#### 1.2.5. Offset

Ideally, applying zero input to an op-amp should result in zero output. However, due to its imperfections, this is not the case for a real amplifier. A non-zero input voltage is required to get a zero-output voltage. This input voltage is referred to as offset. An operational amplifier with offset cannot be used in an open-loop configuration because its output will usually clip due to its high open-loop gain. To avoid this, negative feedback is necessary, but the offset will still be present. This can be problematic if the input signal is small compared to the offset or if an accurate output is desired. Typical offset values can be as large as a few millivolts, whereas input signals can be as small as a few microvolts. This amplifier design targets a worst-case offset of less than 10 µV.

### 1.3. Low Offset Techniques

In precision applications, it is crucial to compensate for an amplifier's offset. There are two general approaches. The first approach, trimming, is a static offset cancelation technique. The second, known as dynamic offset cancelation (DOC), involves chopping and autozeroing to periodically correct amplifier offset.

DOC techniques are implemented on-chip and therefore do not need external measurement equipment. They compensate for offset changes due to amplifier aging and temperature variations. They also help mitigate the amplifier's low-frequency noise and improve its common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). The trade-off is an increase in circuit and design complexity [12].

#### 1.3.1. Trimming

Trimming involves modifying an electronic component after fabrication to adjust its value. Resistances, capacitances, and threshold voltages can all be trimmed. Unlike DOC, trimming requires external equipment. It needs trimming procedures to be designed and implemented in fabs (production facilities) so that chips can be trimmed in mass production. It therefore increases production times and costs. This makes trimming an expensive technique. Trimming can be used to reduce the native offset of an amplifier. However, trimming cannot decrease offset drift caused by temperature or aging. Some off-the-shelf amplifier designs using laser trimming achieve 25-µV (max) offset voltage and 0.8-µV/°C (max) drift [13].

#### 1.3.2. Chopping

Chopping is a modulation technique [7] [12] [14]. Figure 1.4 shows the block diagram of a chopper amplifier. A DC input voltage at point A is applied to a polarity reversing switch known as a chopper. This up-modulates the DC signal, resulting in a square wave at point B. The amplifier's native offset (in red) is then added to the result at point C, and amplified (by two

times in the example), resulting in the signal at point D. The second chopper then down-modulates the signal back to DC while simultaneously up-modulating native offset up to chopping frequency. The resulting output waveform is a DC voltage with a superimposed square wave, as shown in point E. This ripple, also called chopping ripple, does not cause any offset as the average value of the waveform is zero, therefore, the signal is now offset-free. Although, depending on the application, the ripple can be detrimental and is undesired. Several ways of reducing ripple are discussed in section 1.3.2.1.

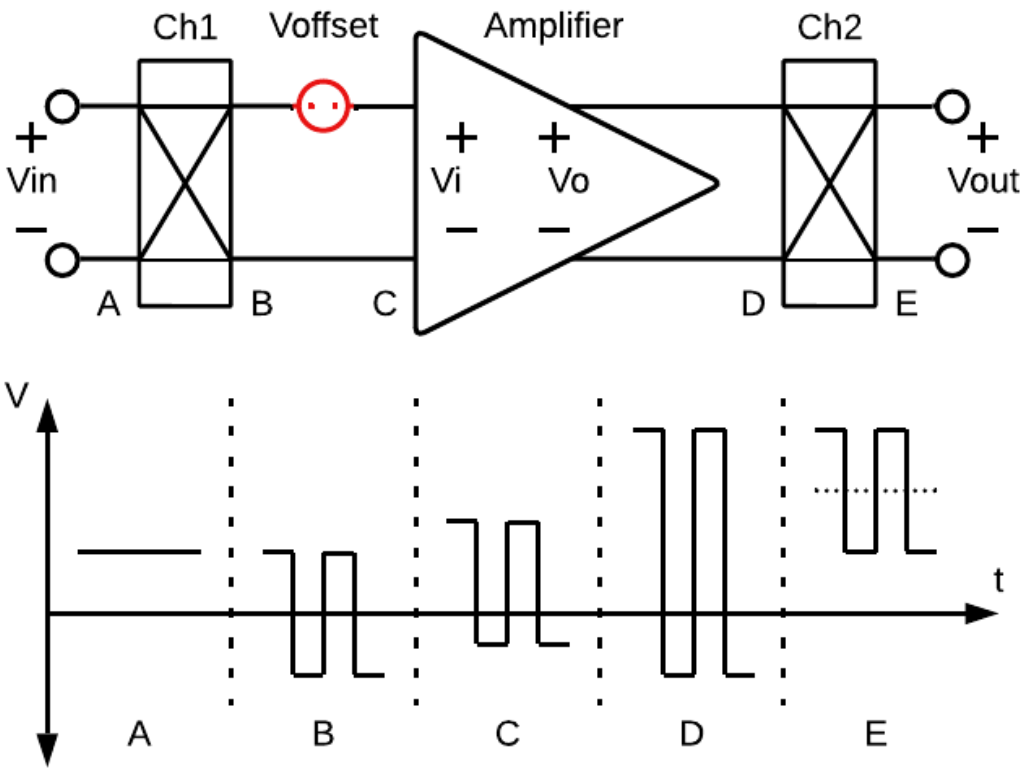


*Figure 1.4 Chopping Explained*

Another important non-ideality is clock skew: a non-fifty % duty cycle of the chopper clock. This results in a residual offset because an equal voltage is averaged over unequal intervals, and so does not exactly cancel out [7]. Furthermore, chopping transistors contribute on-resistance related noise and charge injection mismatch. The chopping frequency is chosen above the noise corner frequency of the amplifier to up-modulate 1/*f* noise away from low-frequency and to not alias with its images [15].

#### *1.3.2.1. Techniques to Decrease Chopper Ripple*

Precision amplifiers require a ripple in the order of a few µV, not mV. Increased circuit complexity is needed to bring the ripple down. Some solutions are low-pass filters, ripple reduction loops, trimming, and autozeroing.

##### *1.3.2.1.1. Low-pass Filter*

Using an ideal brick wall filter at the chopping frequency would eliminate any ripple, as the ripple is also at the chopping frequency. In practical applications, ripple suppression is limited and depends on filter design. Therefore, there is a residual ripple after the filter. A low-pass

filter also causes a loss of bandwidth as the filter also suppresses in-band signals. It is only suitable for amplifiers where the chopping frequency is higher than the amplifier's bandwidth.

#### *1.3.2.1.2. Notch Filter*

Instead of a low-pass filter, a notch filter centered around the chopping frequency can suppress the ripple while achieving wideband output [16].

One implementation of a notch filter is the ripple reduction loop (RRL) [16]. An example of RRL is shown in Figure 1.5. The RRL converts the ripple into a current (Iac), chops this current to generate a demodulated current (Idc), and integrates it into Vo. This integration generates a voltage input to a transconductor (Gm5). This transconductor sums a current to the output of the input stage (Gm3) to compensate for the offset. At the same summation node, feedback transconductor (Gm4) is used to generate a feedback current from the feedback voltage. This completes the feedback loop.

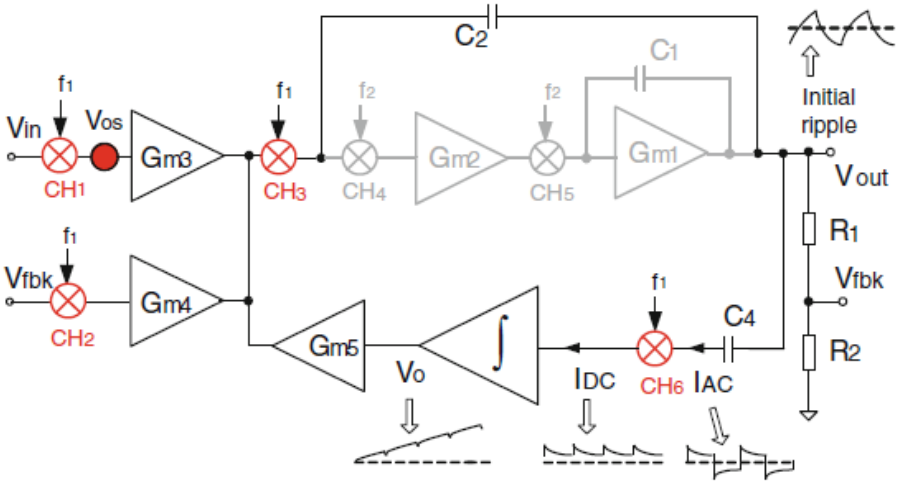


*Figure 1.5 Ripple Reduction Loop (RRL) [16]*

#### *1.3.2.1.3. Trimming*

Trimming, as explained in section 1.3.1 can reduce the native offset. Chopping ripple can therefore be reduced by trimming the native offset of an amplifier.

#### *1.3.2.1.4. Autozeroing*

The last technique considered to reduce the chopping ripple is autozeroing. With the autozeroing technique explained in section 1.3.3, the native offset of an amplifier can be lowered to a few µV. The amplifier has an offset with only autozeroing. The combination of autozeroing and chopping is offset free and results in a few µV chopping ripple.

### 1.3.3. Autozeroing

Autozeroing is a sampling method, and the working principle includes two phases of operation and switches to alternate between them [12]. Two autozeroing loops are evaluated in Figure 1.6 or Figure 1.7.

One option is putting the amplifier in a unity gain loop and storing offset at input capacitors, also called closed-loop offset cancelation [17]. A possible implementation is shown in Figure

1.6. During the sampling phase, the amplifier is in a closed loop with S3, S4, and S5 closed. The amplifier works to have an output voltage of zero, and as the amplifier is in a loop with a gain of one, its offset is stored on the capacitors (C1 and C2) at its input. During the signal phase S1 and S2 are closed, and the amplifier's native offset is compensated with the stored value on the capacitors.

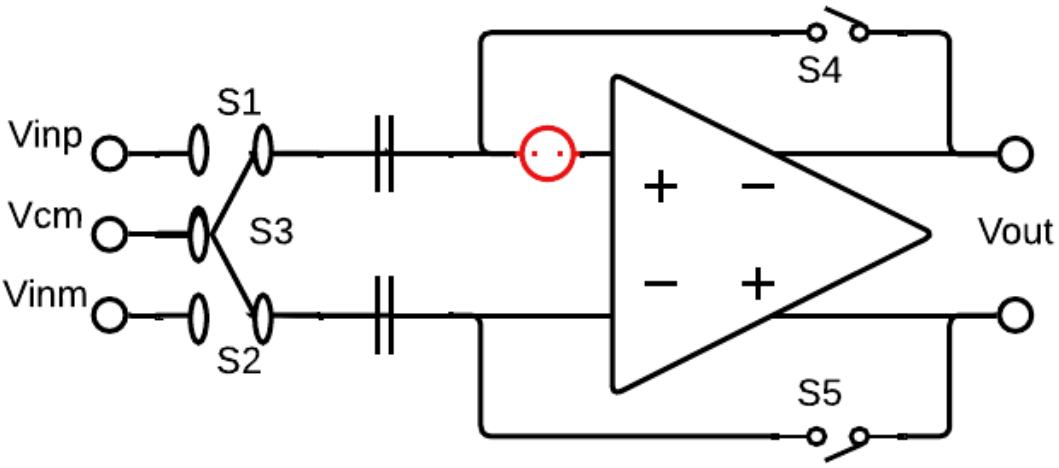


*Figure 1.6 Closed-Loop Offset Cancelation*

Another alternative uses an auxiliary amplifier, with one implementation shown in Figure 1.7. In the sampling phase S3, S5, and S7 are closed. S3 shorts the amplifier's input. Its offset, represented in red, causes an output current at the amplifier output. This amplifier current (Iamp) integrates on the autozeroing capacitors (C1 and C2) at the input of the auxiliary amplifier. The extra amplifier generates an offset compensating current (Iaux), and both currents sum to zero (Iout) at the output of the amplifier (Vout). Then in the signal phase S1, S2, S4, and S6 are closed, and the circuit uses the auxiliary current to compensate for native offset and errors resulting from this offset. Speed and limited loop gain reduce the compensation accuracy [17].

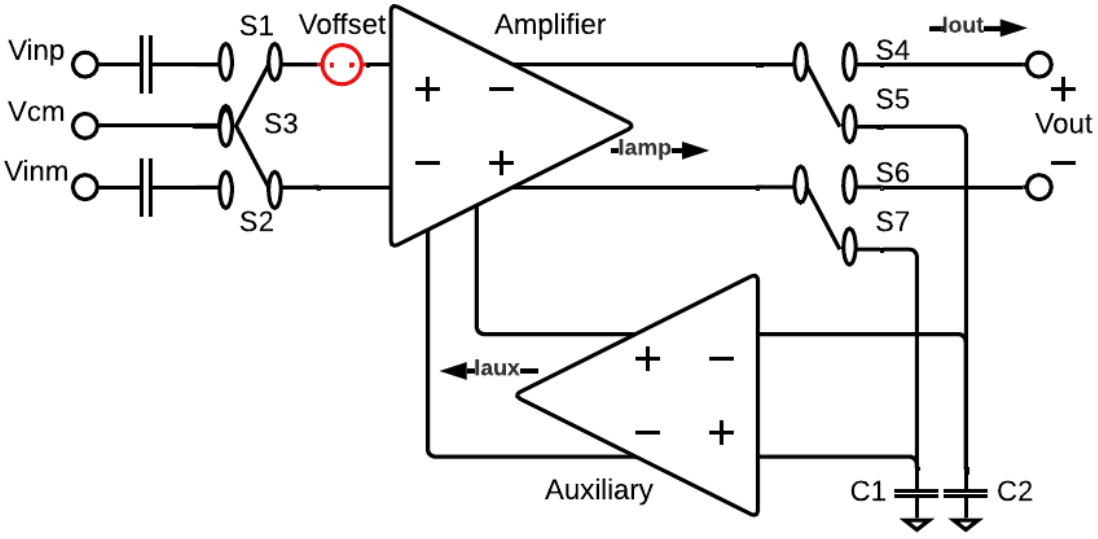


*Figure 1.7 Auxiliary Amplifier Autozeroing*

### 1.3.4. Low Offset Technique Trade-offs

#### *1.3.4.1. Noise with DOC*

The noise spectral density of a CMOS amplifier over a wide band is shown in Figure 1.8. Autozeroing is a sampling technique that folds wide-band noise back to lower frequencies. The resulting noise spectrum increases significantly at lower frequencies. Chopping is a modulation technique that up-modulates an amplifier's $1/f$ noise to the chopping frequency [12]. The use of both techniques has a combined effect. Autozeroing folds noise down and chopping up-modulates folded noise to the chopping frequency [16]. This amplifier design limits the autozeroing noise penalty at low frequencies. The average of ripple is zero, however if ripple cannot be averaged then noise may be preferred.

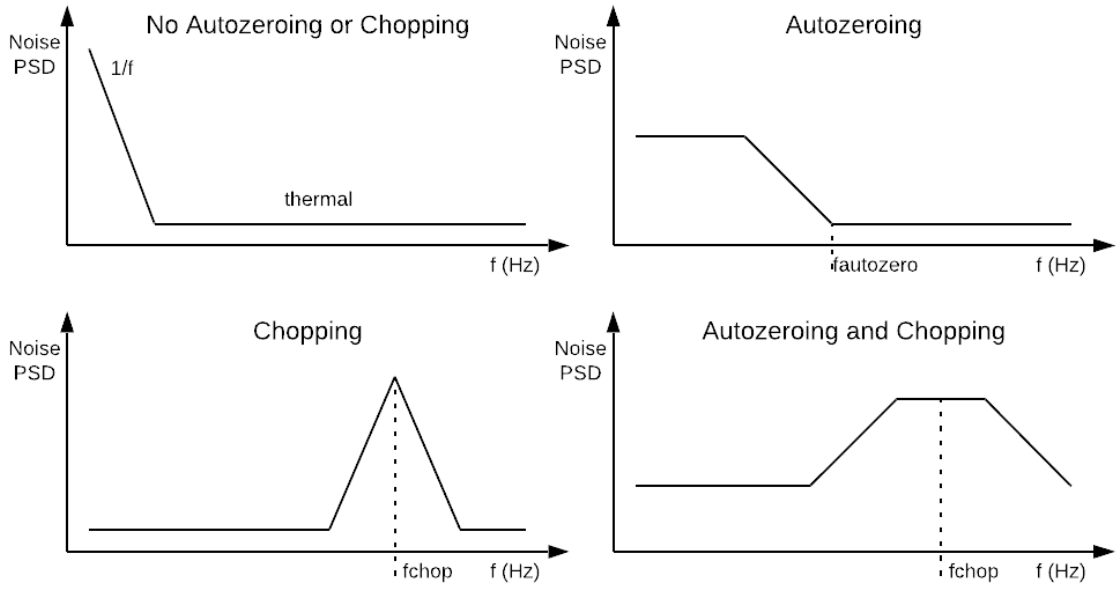


*Figure 1.8 Noise Spectrums with Autozeroing and Chopping*

#### *1.3.4.1. Spikes and Glitches*

An analog switch turning on or off injects different quantities of charge into the drain and source of the transistors. Turning off an N-channel switch causes a negative voltage spike. In contrast, turning off a P-channel switch causes a positive voltage spike. This phenomenon of voltage spikes and changing capacitance voltages is called charge injection. It happens to load capacitance, such as C1 and C2 in Figure 1.7, and gate capacitance. Charge injection spikes are shown in the output waveform in Figure 1.9. The larger the capacitance the smaller the voltage jump and the less detrimental the charge injection, as evidenced by $\Delta Q = C\Delta V$ [18].

Complementary switches (transmission gates) help decrease charge injection as the PMOS and NMOS devices inject opposite charges. Another compensation method is using differential circuits. In this case, charge injection becomes a common-mode effect [16]. Ideally, the two voltage spikes are equal when using a differential circuit and compensate for each other. In practice, the two are different in amplitude. This leaves a smaller charge injection mismatch which still causes an error.

Furthermore, there is a non-overlapping time delay between the falling edge of one chopping clock (ChopA) and the rising edge of the successive chopping clock (ChopB). This causes a glitch

in the output for every non-overlapping time moment in the clocking scheme [19]. Output spikes and glitches are depicted in Figure 1.9. This amplifier aims to have low voltage spikes and glitches as the two harm the overall accuracy. The goal is to limit transient errors to less than a microsecond (µs) and make them smaller than a few hundred microvolts (µV).

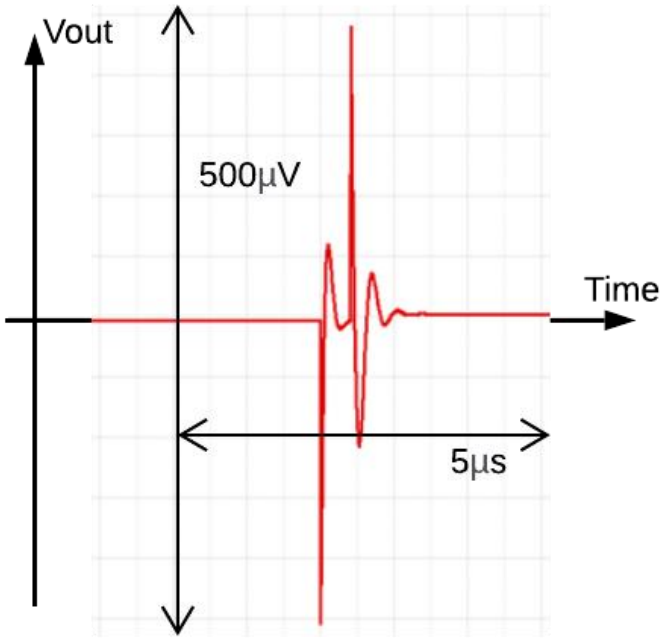


*Figure 1.9 Output Spikes and Glitches*

## 1.4. Beyond-the-rail Input Stages

Many operational amplifiers employ input stages that consist of folded cascode amplifiers with PMOS differential pairs, as will be described in section 3.1. However, these can only handle input voltages near the negative supply rail. One way of handling input voltages near both rails is by combining PMOS and NMOS differential input pairs [20]. Alternatively, a charge-pump boosted input stage can be used. Here an on-chip charge pump creates a higher tail voltage for a folded cascode amplifier. This allows a single input differential pair to handle rail-to-rail inputs [21]. A third alternative involves the use of a capacitively coupled input stage. Capacitors in series with the input path isolate the DC bias voltages of the input stage from external DC voltages. AC signals are not blocked, and the amplifier achieves beyond-rail functionality [22].

### 1.4.1. Capacitive coupling

Capacitors block DC voltages. So, they can isolate internal nodes from large external DC voltages. This protects internal transistors and ensures that overvoltage conditions are circumvented. This also allows the circuit to be connected to a common-mode voltage that may exceed the supply rails [22] [23] [24] [25] [26]. When using such capacitors and isolating the input CM voltage the circuit cannot sense DC signals. DC signals must then be modulated to a higher frequency to pass through a capacitor. Therefore, circuit techniques such as chopping are needed.

As shown in Figure 1.10 (A), capacitive coupling can be implemented with two floating capacitors (C1 and C2). However, large transients at the inputs (Vin) will be coupled to the internal output voltages (Vcmgm). This may result in overvoltage conditions for the input

devices. To prevent this, the internal voltages (Vcmgm) can be maintained at a safe voltage by the resistors (RB1 and RB2), as shown in (B). The capacitors then function as floating batteries that shift the input voltages to the DC bias voltages of the input transconductor. The input capacitors are thus charged to the level shifting voltage, i.e., the voltage difference between the input voltage (Vin) and the Vcmgm [27] [28]. The diodes are added for protection as described in more detail in section 2.7.

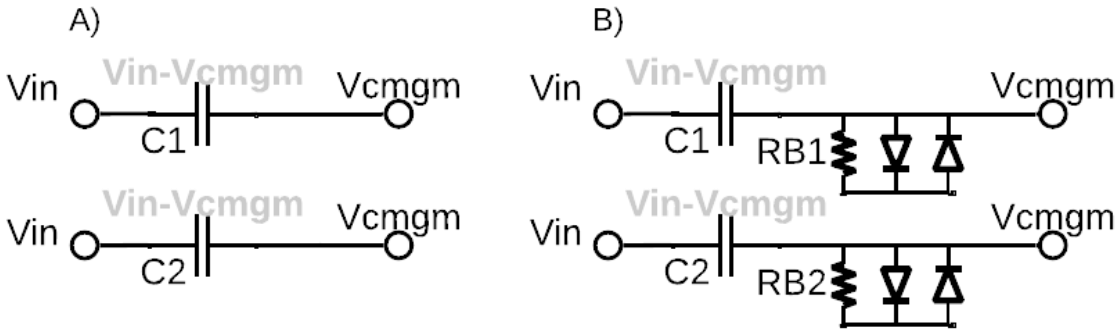


*Figure 1.10 Capacitive Coupling A) with only Capacitors B) with Resistors and Diodes*

## 1.5. Amplifier Topologies

The section discusses the use of some relevant topologies in detail, after which it is determined whether the proposed amplifier would benefit from their use.

### 1.5.1. Multi-path Amplifier

The multi-path topology involves designing amplifiers with multiple paths for the signal to propagate through. Figure 1.11 shows a four-stage amplifier with two paths. It has a low-frequency and a high-frequency path. All stages are present in the low-frequency path and are compensated. The signal passes through fewer stages in the supplemental path and is less compensated. The low-frequency path has higher gain through more stages, while the high-frequency path has a faster response and increases bandwidth. If the crossover frequency between the two paths is low, the ripple and glitches through the low-frequency path can be suppressed by the high-frequency path [29].

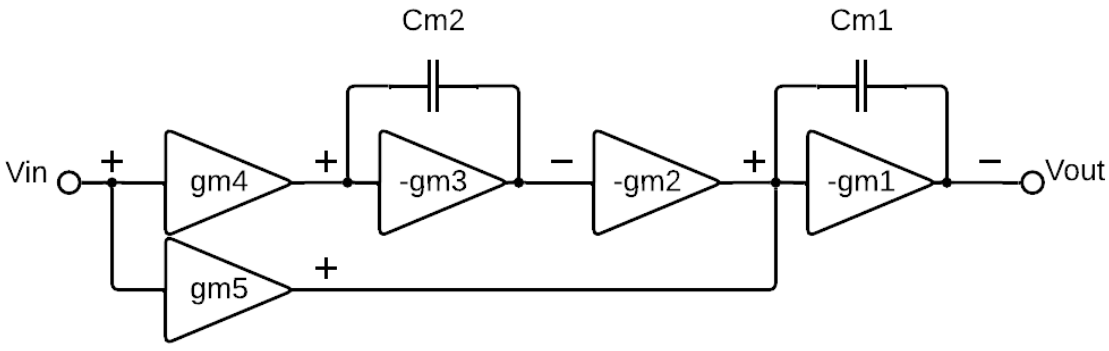


*Figure 1.11 A four-stage conditionally stable amplifier with multiple paths [29]*

### 1.5.2. Ping-Pong Amplifier

As described in section 1.3.3, autozeroing relies on two phases. During the sampling phase the signal path is broken and then it is reconnected during the signal phase. Therefore, it does not

provide continuous-time amplification. A quasi-continuous-time solution is shown in Figure 1.12. This topology uses two copies of the input stage (Ping and Pong), where each copy has its own auxiliary amplifier to cancel its offset. These two copies alternate their operating phases with opposing clock phases. One phase is sampling, while another is amplifying and vice-versa. The output stages and compensation networks are not doubled; they are shared between the two input stages. The downside of the ping-pong topology is the increased area and power consumption of adding the extra input stage [30].

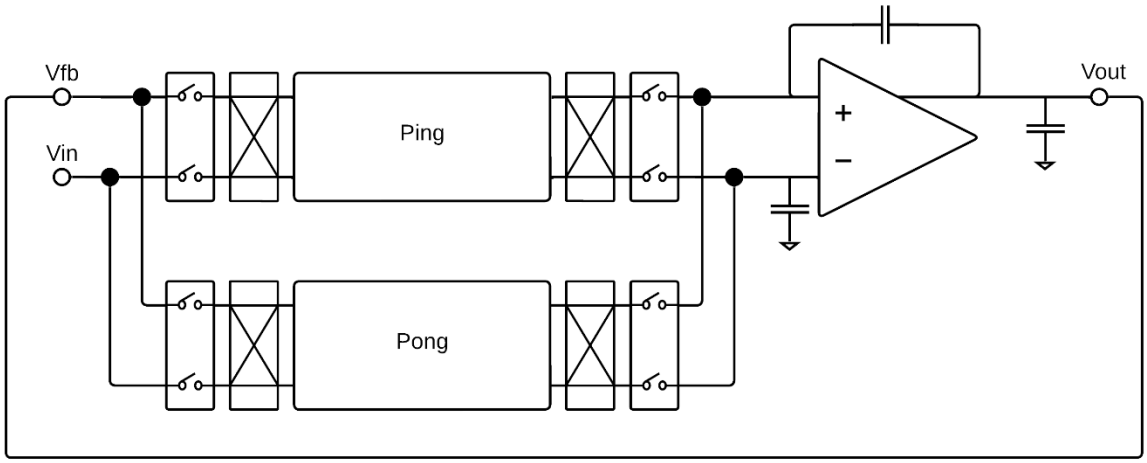


*Figure 1.12 Ping-pong Amplifier*

### 1.5.3. Capacitively-Coupled Operational Amplifier

In recent years, publications have focused on capacitive coupling combined with chopping to design amplifiers capable of sensing beyond-the-rails. One example of this is the Capacitively-Coupled Operational Amplifier (CCOPA) in Figure 1.13 [23]. The CCOPA has capacitive coupling to block input common-mode voltages and uses chopping to up-modulate and pass signals through the capacitors. The CCOPA uses a ripple reduction loop (RRL) to reduce the chopping ripple. The RRL deteriorates the frequency spectrum by introducing a notch at the chopping frequency. To fill the notch at the chopping frequency, the design uses a multi-path amplifier with chopping in the low-frequency path and an additional high-frequency path. The CCOPA has a few drawbacks. These include the need for an RRL and the multi-path implementation to get a flat frequency, which increases the area and power consumption. In particular, the total capacitance of CinH and CinL can be tens of Picofarads, which is larger than what is usually needed for autozeroing capacitors [31]. Furthermore, the CCOPA has a relatively slow response to input transients as the biasing resistors (Rb1) and coupling capacitors (Cin1) settle slowly at the input of Gm1.

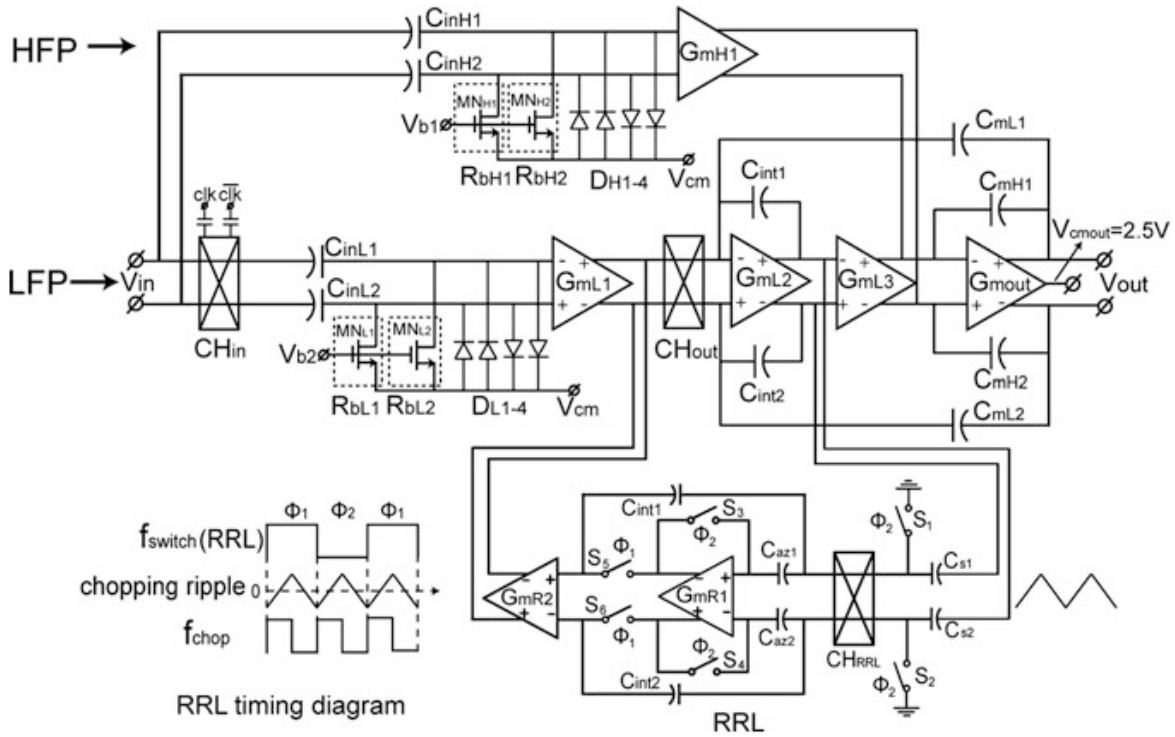


*Figure 1.13 CCOPA [23]*

### 1.5.4. Auto-Chop Amplifier

Apart from extending input common mode voltage ranges, various amplifiers that combine autozeroing and chopping to achieve low noise, low offset, low drift, low area, and low power have also been proposed [32]. As explained in section 1.5.1, ping-pong amplifiers combine autozeroing and chopping and achieve low noise, -offset, and -drift. However, ping-pong amplifiers require a relatively large area and high-power consumption. Therefore, the recent trend has been to avoid using ping-pong architectures, as this halves the area and power needed for the input stage. An example of this is the auto-chop amplifier in Figure 1.14 [33]. It employs autozeroing between two choppers. The amplifier's signal path is periodically broken during autozeroing; it causes a short deadband, which introduces a noise penalty.

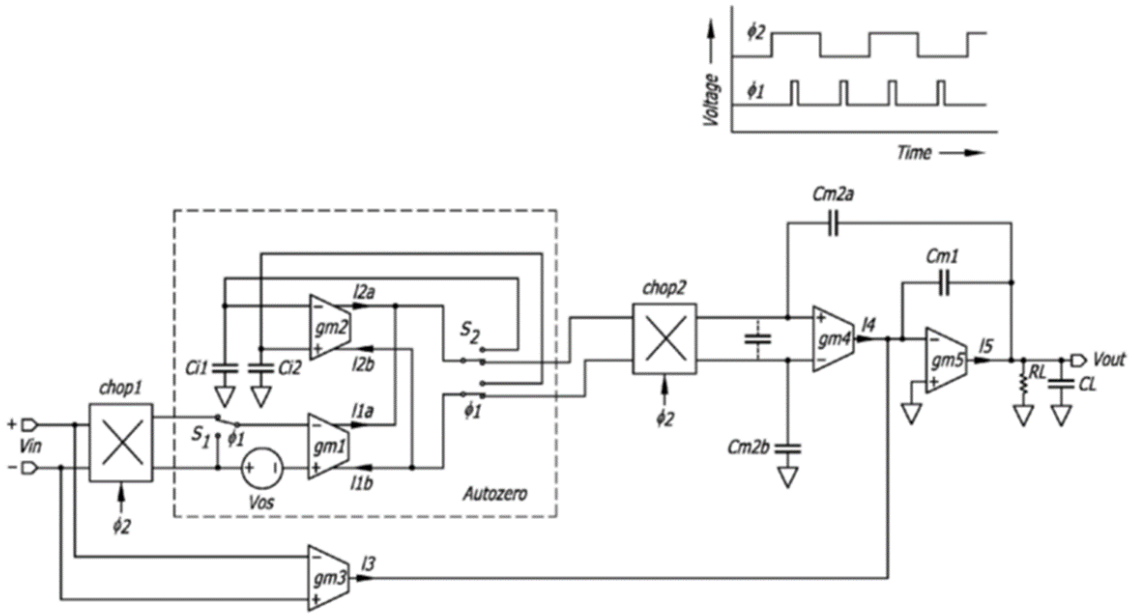


*Figure 1.14 Auto-Chop Amplifier [33]*

## 1.6. Key Idea / Specifications

The use of capacitive coupling to achieve beyond-the-rail input voltage ranges, and the use of chopping and auto-zeroing in the main signal path to realize low noise, -offset, and -area amplifiers have not been combined before. The key objective of this thesis is to combine these methods and solve the problems that arise in the process.

This thesis aims to achieve the same or better performance levels as the CCOPA and Auto-chop architectures. The critical performance parameters are the required total area, power consumption, response to large transients, and noise penalty due to deadtime. A list of target specifications is included below in Table 1.1. The table details CCOPA and Auto-chop amplifiers and how their combination is expected to produce a unique amplifier.

*Table 1.1 Specifications*

| Specs | Combination | CCOPA [23] | Auto-Chop [33] |
|---|---|---|---|
| Input Impedance | High >1 GΩ | High | High |
| Input Current | Low <100 pA | Low | Low |
| Output Range | Rail-to-Rail | Rail-to-Rail | Limited |
| Input Range | Beyond-the-Rail | Beyond-the-Rail | Limited |
| Gain | >160 dB | High | High |
| Offset | <10 µV | Low | Low |
| Noise | <50 nV/√Hz | Low | Low |
| Noise Penalty | Low | None | Low |
| Power | <1.5 mW (300 µA) | Higher | Similar |
| UGB | >1 MHz | Similar | Similar |
| Area | Small | Large | Small |
| CM Tran. Resp. | Fast | Slow | Fast |

## 1.7. Thesis Organization

This thesis has been divided into five chapters. This introductory chapter explains general background concepts, recent techniques and state-of-the-art, and thesis design goals. Following this introduction, Chapter 2 describes the relevant circuit techniques, presents the design of a 3-stage multi-path amplifier, and explains the clocking scheme for the switching between different amplifier states in the periodic steady state operation. Chapter 3 describes the transistor-level design. Chapter 4 describes the simulation results, and the thesis ends in Chapter 5 with conclusions and future work.

# 2. System Design

This chapter discusses the amplifier's system-level design. Additionally, its high gain, frequency compensation, unity-gain-bandwidth (UGB), stability, phase margin, and gain margin are considered. Then its operational phases and a simple switching scheme which combines chopping and autozeroing are detailed. Lastly, the chapter concludes with an analysis of the operational amplifier as a whole.

## 2.1. Loop Gain

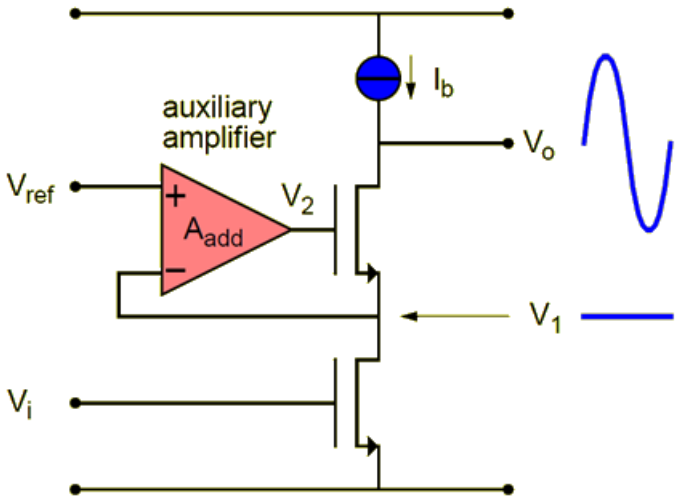


*Figure 2.1 Auxiliary Amplifier Helps Cascode Transistor in Gain Boosting [34]*

As discussed in section 1.2.1, the amplifier should be designed for an open-loop gain of 180 dB, which is quite challenging. As shown in Figure 2.1, gain boosting can be used to increase an amplifier's gain by using an auxiliary amplifier to increase its output impedance [34] [35]. However, implementing a single stage with a gain of more than 180 dB is not possible since the required output impedance cannot be realized on chip. Therefore, to achieve a gain of more than 180 dB, a cascaded design must be employed.

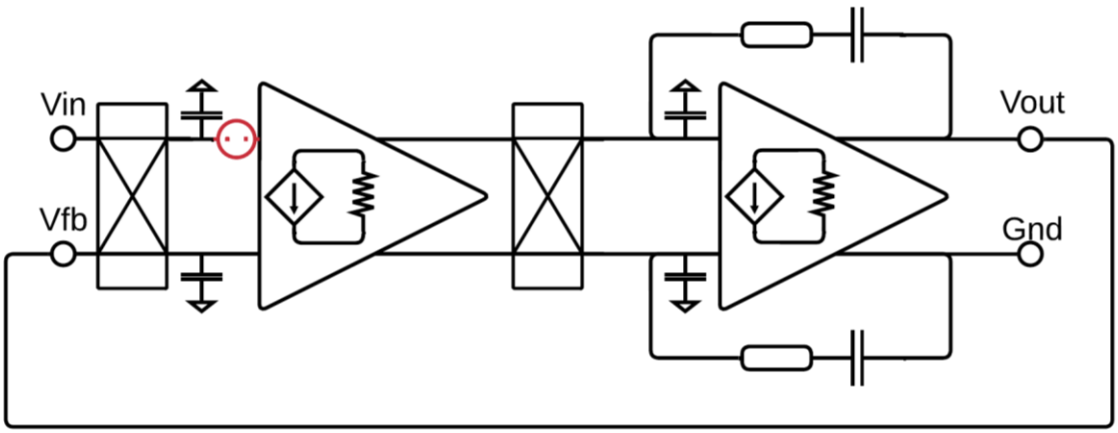


*Figure 2.2 Two-Stage Amplifier Showing Loop Gain and Chopping*

One possible topology is a two-stage amplifier. A two-stage design requires that each stage achieves 90 dB gain. This is not easy to achieve in the selected 180 nm TSMC process. If the

input stage is gain-boosted, then it can be designed to have a gain of 120 dB, allowing the output stage to have a gain of 60 dB. An illustration of such a 2-stage amplifier is shown in Figure 2.2. The amplifier must also have a low-offset, and so the chopping technique, explained in section 1.3.2, is used around the first stage. The input chopper up-modulates input signals to the chopping frequency. These signals are applied to the input of the first stage. The output of the first stage is then demodulated and applied to the output stage. The gain of each stage is a function of its transconductance, output impedance, and capacitance and typically has a low-pass characteristic [34]. The amplifier stage between the choppers should have low delay, to avoid amplitude-dependent distortion, or intermodulation distortion. The stage needs a design with high frequency internal poles.

Another option is a 3-stage amplifier, as depicted in Figure 2.3. For clarity, the equivalent single-ended architecture is shown. The total effective gain of the three stages will be reduced by various non-idealities and parasitic capacitances. Therefore, the amplifier is designed to have a higher gain of 200 dB to compensate for the expected gain loss. The first, second, and third stages are designed to have a gain of 70 dB, 70 dB, and 60 dB respectively. The first stage can be optimized for low noise and high CMRR, the second for coupling, and the third for load driving and PSRR [36]. With a 4-stage amplifier, an even higher gain can be achieved, but at the expense of amplifier stability and (probably) the need to decrease bandwidth and increase capacitor sizes, both of which are undesirable [3] [29]. A 3-stage amplifier is chosen over 2-stage and 4-stage alternatives.

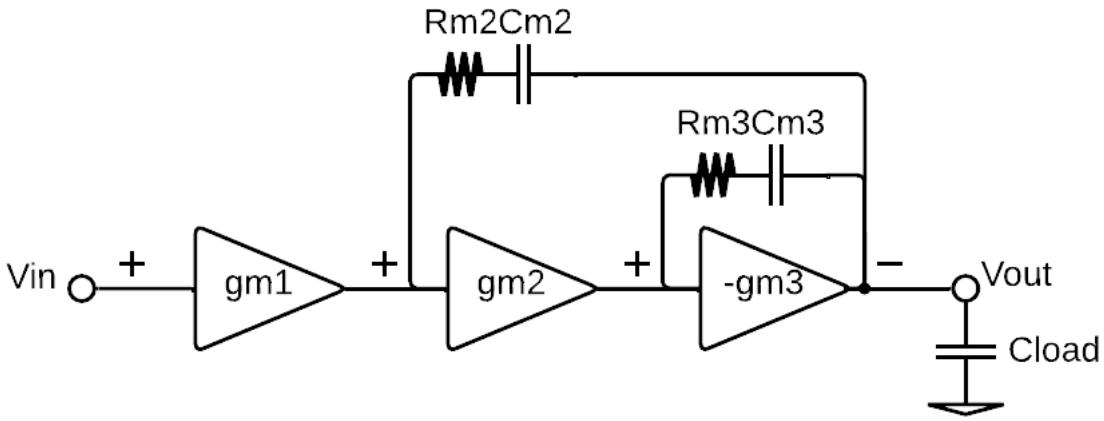


*Figure 2.3 Ideal Three-Stage Amplifier Model with Single-Ended Output*

## 2.2. Frequency Compensation

A single stage amplifier has only one dominant pole and a first-order frequency response. Its Bode plot resembles Figure 2.4b and goes down by 20 dB per decade, while its phase changes by only $90^{o}$. Thus, it is always stable in a feedback loop. The number of poles increases as the stage count increases. An uncompensated 3-stage amplifier has three dominant poles resulting in a $270^{o}$ phase change and a 60 dB per decade roll-off shown in Figure 2.4a. Such an amplifier is not stable with feedback [29].

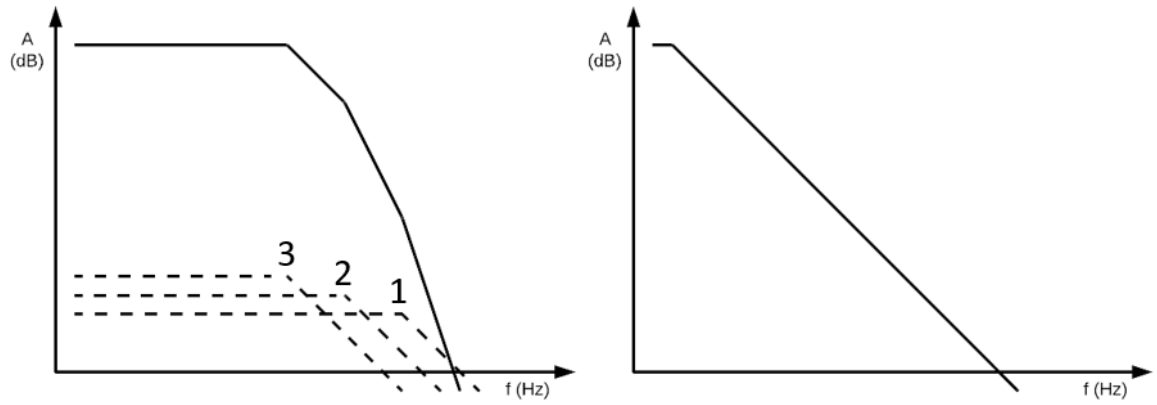


*Figure 2.4 a) Uncompensated 3-Stage Amplifier b) Compensated 3-Stage Amplifier*

Frequency compensation is needed to realize a stable multi-stage feedback amplifier. In [29], five requirements of frequency compensation schemes for integrated amplifiers are:

1. Uses small capacitors only.
2. Robust against process variations.
3. Stable with sufficient phase and gain margin under different load and feedback conditions for universal use.
4. Has high loop gain at low frequencies.
5. Has an open loop Bode-plot with a 20 dB per decade roll-off.

### 2.2.1. Miller Compensation

To realize a stable 3-stage amplifier with feedback, the proposed design uses Miller compensation. This results in small compensation capacitors, inherent robustness against process variations, and good distortion performance. However, an evaluation of Miller compensation reveals that its bandwidth potential is limited, as every added stage reduces the amplifier's bandwidth by a factor of two. A 3-stage amplifier requires two (nested) Miller compensated stages, and thus has a bandwidth loss factor of four [29].

### 2.2.2. Multi-Path Technique and Compensation

The bandwidth loss is undesirable as it decreases the bandwidth-to-power ratio. Furthermore, lower bandwidth requires larger Miller capacitors. Capacitor size doubles as bandwidth halves. This requires more chip area, which is costly and is not desired. Some bandwidth loss can be recovered using the multi-path technique [29].

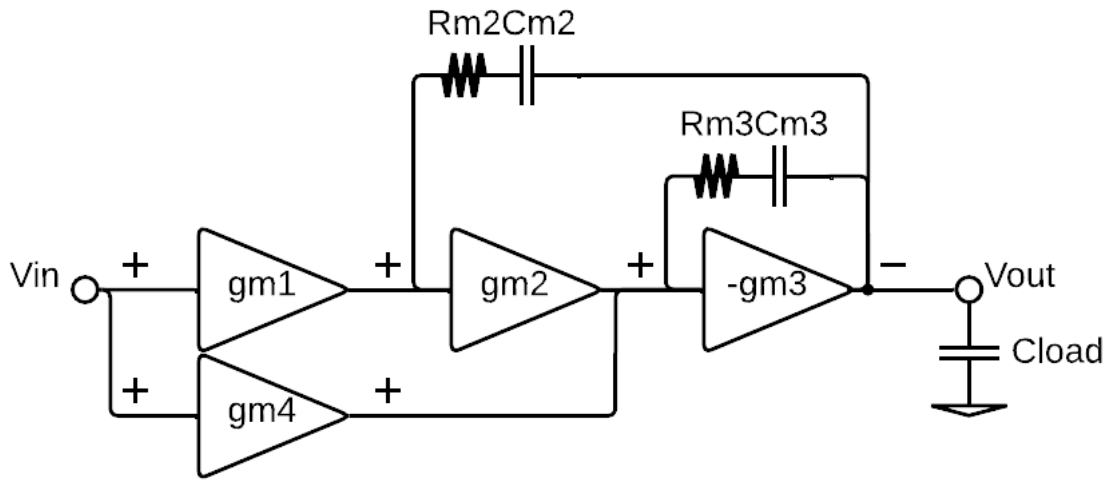


*Figure 2.5 Multi-Path Nested Miller Compensated Three-Stage Amplifier*

Figure 2.5 shows a multi-path amplifier. It has a 3-stage low-frequency path and a 2-stage high-frequency path. It also has two nested Miller-compensated Gm stages [29]. Due to the feedforward path through the Miller capacitors, these stages have right-hand-plane (RHP) zeros that deteriorate their phase margin. The conventional solution is to add a resistor Rm3 in series with Cm3. $Rm3 = 1/Gmout$, where Gmout is the transconductance of the output stage. This places the RHP zero at infinity and mitigates phase margin loss [3] [29].

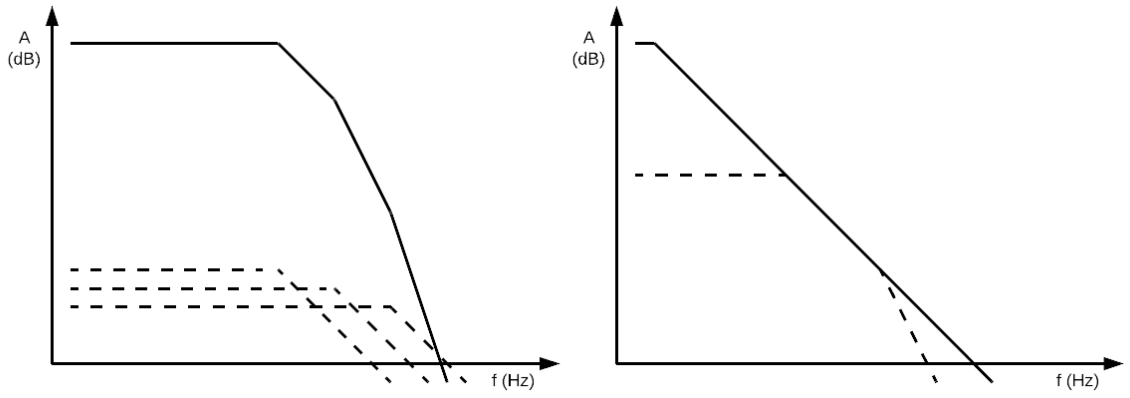


*Figure 2.6 a) Uncompensated 3-Stage Amplifier b) Compensated Multi-Path 3-Stage Amplifier*

Three dominant poles result in a 60 dB per decade roll-off, as shown in Figure 2.6a, which corresponds to a $270^{o}$ phase shift at high frequencies. The multi-path solution shown in Figure 2.5 approximates a one dominant pole system at low frequencies. It achieves high DC gain in the magnitude of 180 dB. The low-frequency path (gm1, gm2, and gm3) has a second pole at a non-zero gain. This is the crossover frequency. After the crossover, the low-frequency path has a 40 dB per decade roll-off and the high frequency path (gm3 and gm4) takes over the amplifier response. The high-frequency path of two stages is limited to a maximum phase shift of 180 degrees. Therefore, the amplifier phase change is also limited to a reduced value of 180 degrees. For stability, the amplifier phase change is limited even further using compensation capacitors [29]. Thus, the amplifier has a 20 dB per decade roll-off and is stable, as depicted in Figure 2.6 (b).

## 2.3. Implementing a Multi-Path Amplifier

The multi-path capacitively-coupled and chopped operational amplifier with a precision LF and a fast HF path is implemented as shown in Figure 2.7 [37] [38]. This amplifier has a precision LF path that employs chopping and capacitive coupling. The input chopper (Up-Mod) up-modulates LF input signals to the chopping frequency. These signals are coupled capacitively to the input of LFGm. The output of LFGm is then demodulated (Down-Mod) and applied to the two output stages. The LF and HF paths are connected together by a chopper linking both signal paths after the floating capacitors. The so-called cross-modulator (Cross-Mod) demodulates the signal at the input of LFGm back to DC, so that it can be applied to the HFGm [3]. The cross-modulator is placed at the input of HFGm rather than at its output because this ensures that HFGm has a higher effective gain and lower power consumption. As shown in Figure 2.5, the output of HFGm is then applied to the third stage.

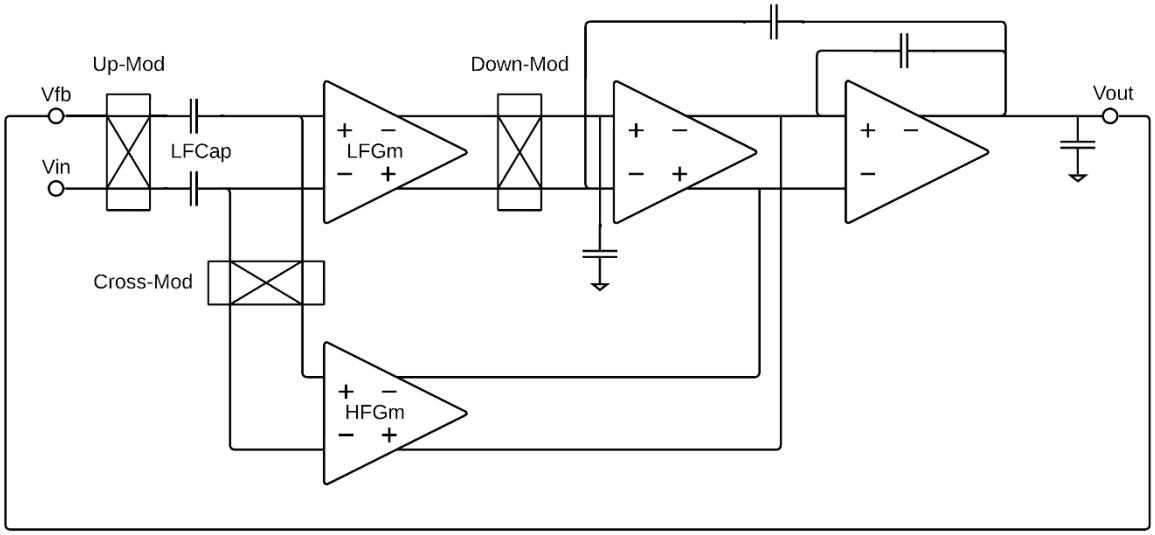


*Figure 2.7 Multi-Path Amplifier combining an HF path with a precision DC path*

## 2.4. Notch at the chopping frequency

The capacitive coupling capacitors and the large biasing resistors (not shown) at the input of the LFGm have a high-pass filter characteristic. The corner frequency of the filter can be expressed as $1/2\pi RC$. Since the biasing resistors are large, the corner frequency will be low, but DC signals will still be blocked.

As explained in section 1.3.2, chopping is mixing in the frequency domain: a chopper up-modulates or down-modulates signals [12]. An input signal around the chopping frequency will be down-converted to DC by the input chopper (Up-Mod). This DC signal will then be blocked by the high pass filter. This means the amplifier will have a notch in its frequency spectrum at the chopping frequency, as shown in Figure 2.8 (b) [3] [23]. As a result, the amplifier will settle slowly in response to a step at its input [3] [39].

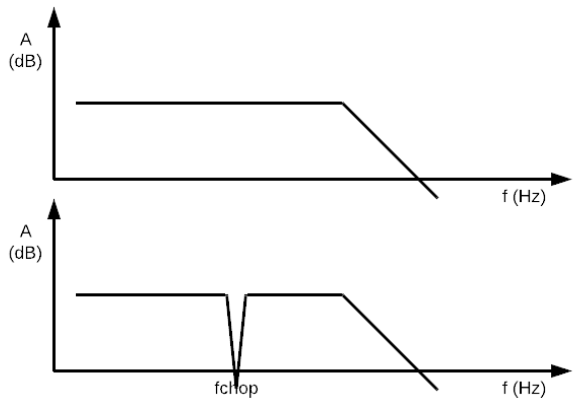


*Figure 2.8 a) Flat Frequency Spectrum b) Frequency Spectrum with Notch at Chopping Frequency*

Multipath amplifiers can have a flat frequency response since the HF path bypasses the notch [23] [25] [39] [40]. The final result is a flat frequency response as shown in Figure 2.8 (a). In Figure 2.7, however, the notch filter precedes both the LFGm and HFGm. The problem of the notch is solved by the Input Refresh described next.

## 2.5. Input Refresh

The level shift voltage across the coupling capacitors is periodically refreshed. This periodical refresh turns the capacitors into a battery by recharging them to the input voltage and the internal common-mode voltage on their terminals. As shown in Figure 2.9, the level-shift voltage across the coupling capacitors (C1 and C2) is set by closing the S2 and S3 switches. The S2 switches connect the same input voltage on one side and the two different coupling capacitors on the other side. At the same time, the S3 switches set the input common-mode voltage at the inputs of the first stage. The high pass filter is eliminated. Therefore, the notch filter is eliminated, and this makes an all-pass filter. The input refresh achieves a flat frequency spectrum at the expense of creating a deadtime in the signal path.

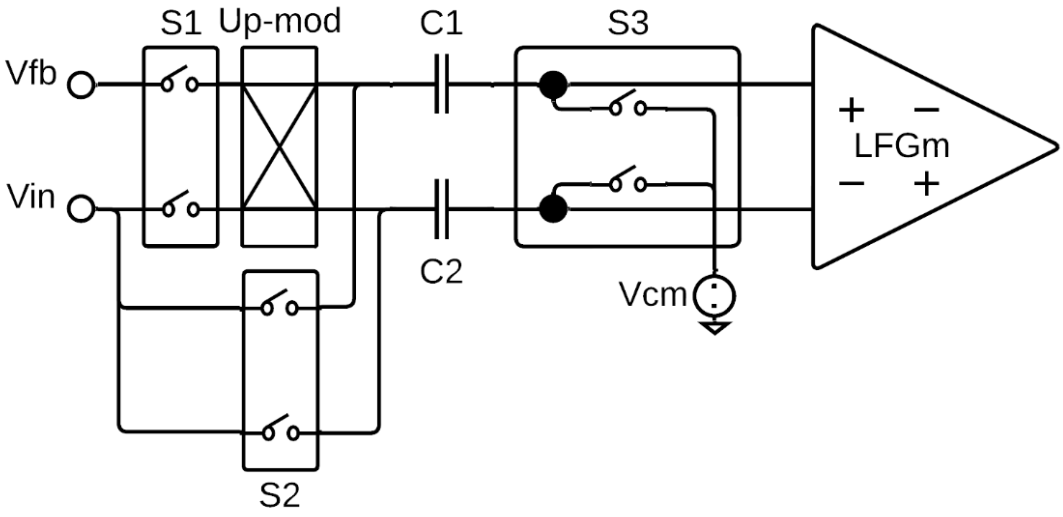


*Figure 2.9 Input Structure Showing Level Shifting and Input Refresh Switches*

Simple clock signals for the input structure are shown in Figure 2.10. In one phase, S1 switches are closed while S2 and S3 switches are open. This phase performs chopping. In the next phase,

S1 switches are open while S2 and S3 switches are closed. This phase performs the input refresh.

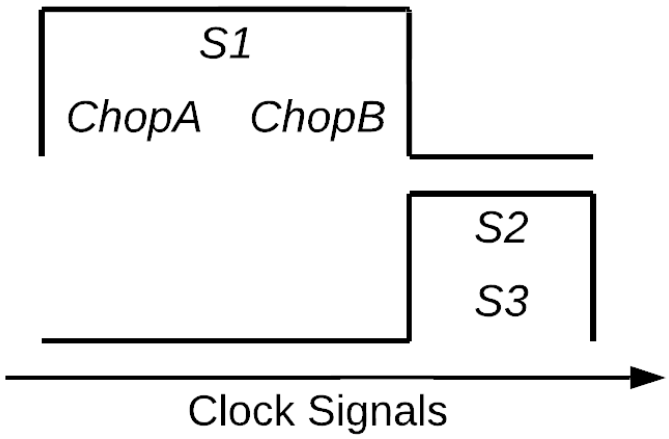


*Figure 2.10 Simple Clock Signals for Input Structure Switches*

## 2.6. Autozeroing

The input common-mode switches have an added benefit. The closing of S3 switches in Figure 2.9 not only sets the input common-mode voltage but also autozeroes the LFGm. The inputs of LFGm are shorted together as shown in Figure 2.11. The offset is autozeroed by an auxiliary amplifier as described in section 1.3.3. The offset of LFGm is sensed on the autozero capacitors at the input of AZGm and is auto-zeroed by AZGm in the next phase of operation. A smaller residual offset remains. This residual offset gives rise to the ripple of the chopped amplifier at the chopping frequency.

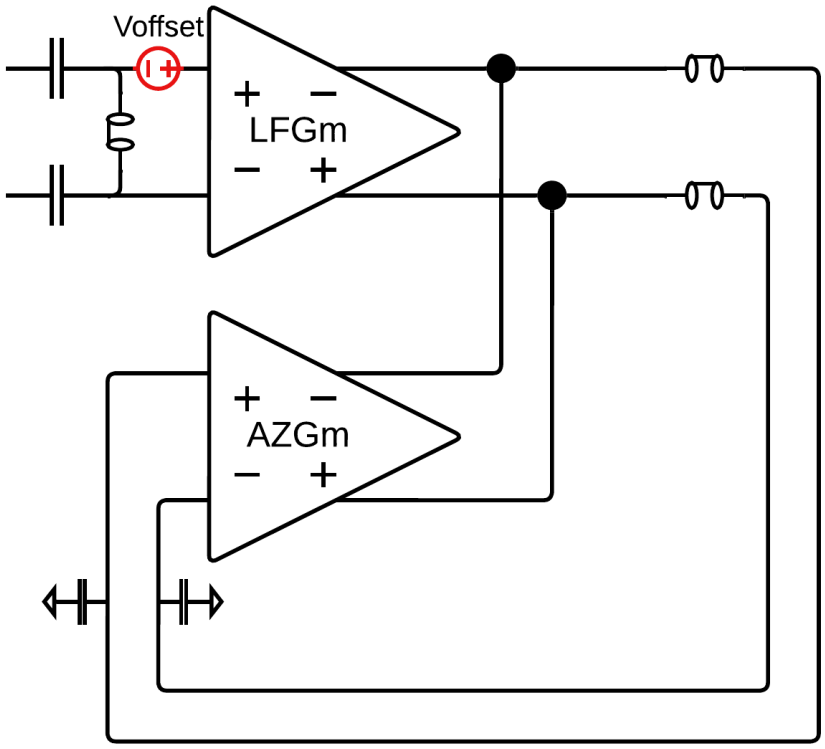


*Figure 2.11 Low-Frequency Path First Stage and Autozeroing Circuitry*

## 2.7. Protection Diodes

The inputs of the first stage will swing in response to large input signal transients. As shown in Figure 2.12, two sets of parallel back-to-back protection diodes (D1 and D2) are connected to both inputs of LFGm. The protection is one diode (~600 mV) above and below the common-mode (2.4 V). This ensures that over voltage stress conditions are prevented. As a result, the transistors do not blow up or age extensively.

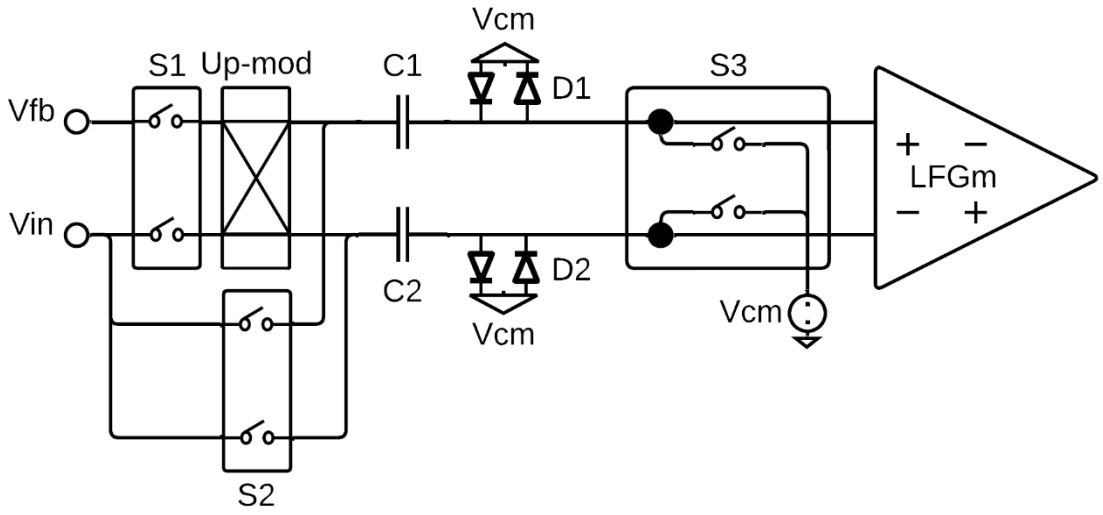


*Figure 2.12 Coupling-Capacitors and Protection Diodes for Input Structure*

## 2.8. Phases of Operation

The multi-path capacitively-coupled autozeroed and chopped operational amplifier and its phases of operation are described in this section. Since the chopping and autozeroing techniques mainly affect the low-frequency path, the high-frequency path is omitted in most of the schematics.

### 2.8.1. Phase 1 – Chopping

The chopping phase of the operational amplifier is implemented as shown in Figure 2.13. The autozeroing and level-shifting and input setting switches are open and not shown. The input chopper can be in both chopping states. The up-modulated input signals at its output are coupled capacitively to the input of the LFGm stage. This stage is autozeroed by AZGm in conjunction with the autozeroing capacitors at the inputs of AZGm. The output of LFGm is then demodulated and applied to the output stages.

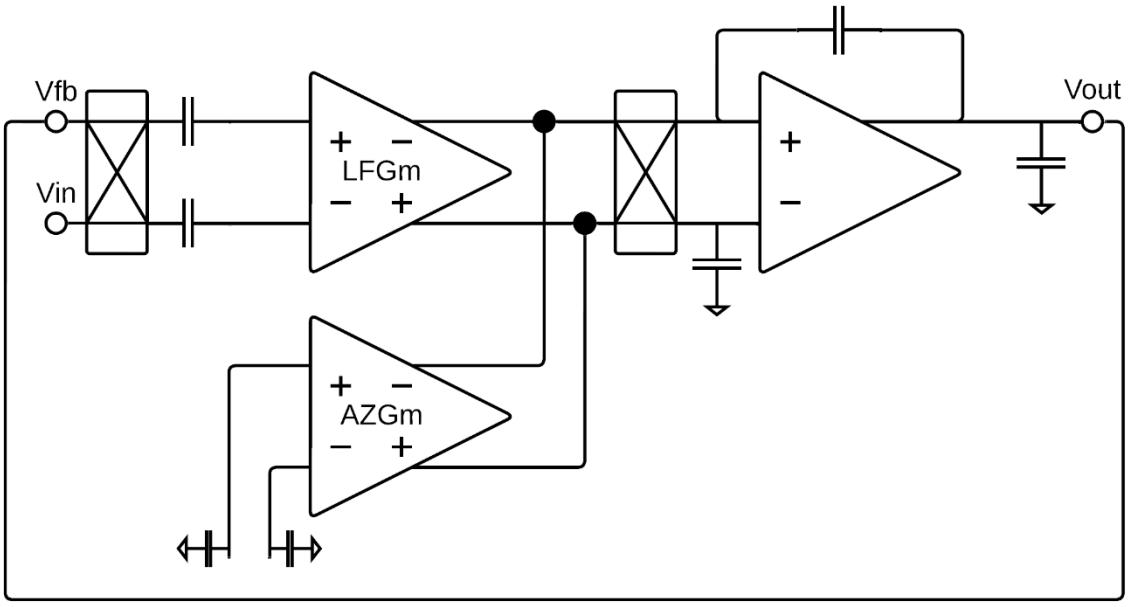


*Figure 2.13 Chopping Phase*

The chopped amplifier has an output ripple. Without global feedback, the resulting differential offset currents will be integrated on the Miller capacitors, resulting in a triangle wave as shown in Figure 2.14 (a). However, feedback around the amplifier limits the output ripple. The output ripple is not a triangle wave but rather a settling ripple as shown in Figure 2.14 (b). The ripple amplitude is determined by the amplifier's input offset. The Miller capacitors remember the output voltage and thus the state of the amplifier [19].

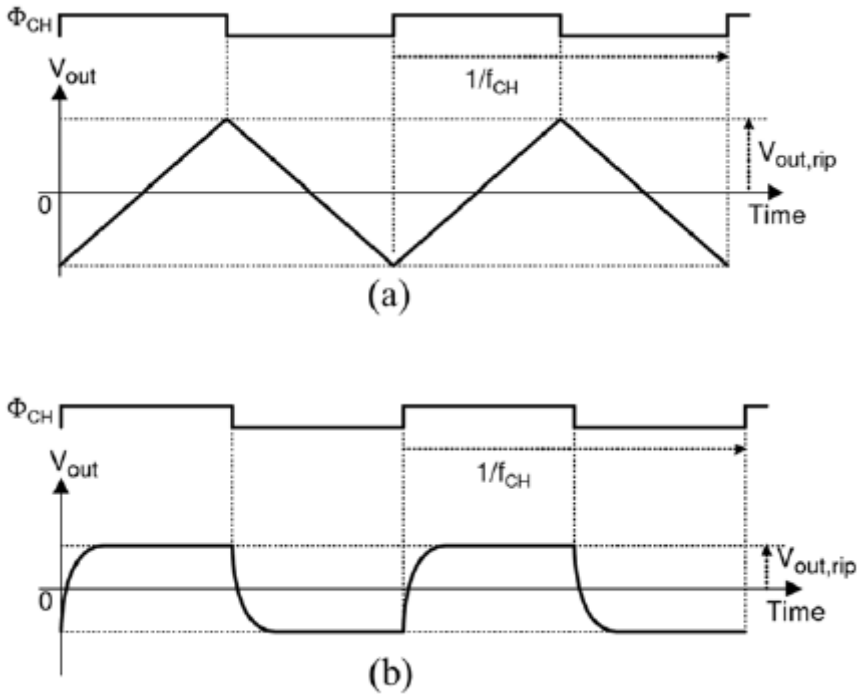


*Figure 2.14 Chopped Amplifier Output Ripple a) without Feedback b) with Feedback [19]*

### 2.8.2. Phase 2 – Autozeroing

The autozero phase of the operational amplifier is implemented as shown in Figure 2.15. The S1 and S4 switches in series with both choppers are open. During this phase, the input common-mode voltage at the inputs of LFGm and the level-shift voltage across the coupling capacitors are set by closing the S2 and S3 switches. Simultaneously, the offset voltage of LFGm is stored on the autozeroing capacitors at the inputs of AZGm using the S3 and S5 switches. This ensures that the offset of LFGm is cancelled during the chopping phase [17]. During this phase, the output stages and the Miller capacitors hold the output voltage. To minimize output distortion, this phase is brief, but long enough to settle the autozero loop [27] [28] [33].

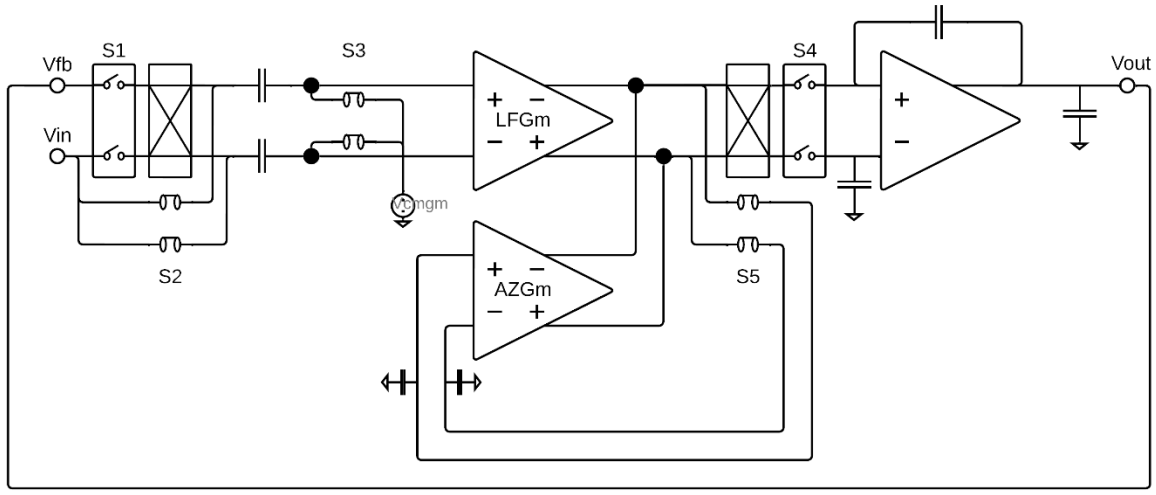


*Figure 2.15 Autozeroing Phase*

## 2.9. Simple Clock Scheme

This is a pseudo-continuous time amplifier that combines chopping and autozeroing. A simple clock scheme for this pseudo-continuous time amplifier is shown in Figure 2.16. The amplifier has a single signal path which is chopped. As shown in Figure 2.16, ChopA and ChopB clock phases select the two states of the single signal path. The amplifier periodically autozeroes the signal path. Autozeroing borrows time from the two equal chop phases [27] [33].

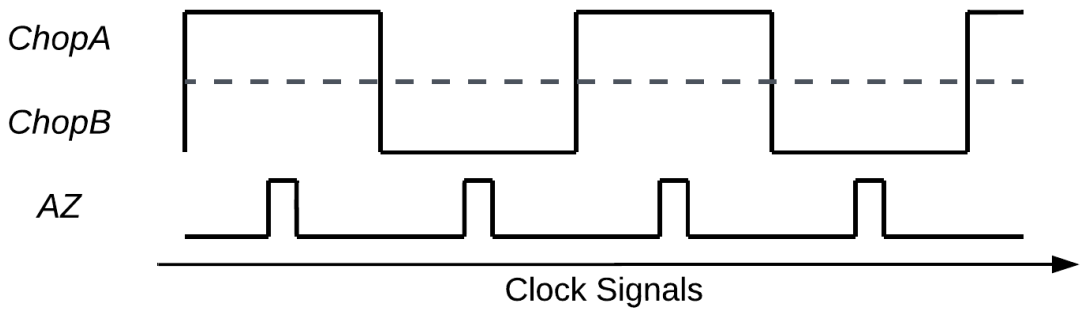


*Figure 2.16 Simple Clock Scheme for Pseudo-Continuous Time Chopping and Autozeroing*

## 2.10. Operational Amplifier

The resulting operational amplifier is implemented as shown in Figure 2.17 [9]. It has a pseudo-continuous time architecture that periodically autozeroes a single signal path, which is also chopped. The chopped input signals are coupled capacitively to the inputs of LFGm [40] [41]. Switches set the common-mode voltage at the inputs of LFGm. Switches also set the level-shift voltage on the coupling capacitors, thereby eliminating the notch filter. AZGm autozeroes LFGm [17]. The output of LFGm is then demodulated by the succeeding chopper and applied to the output stages. The high-frequency path is omitted to simplify the schematic.

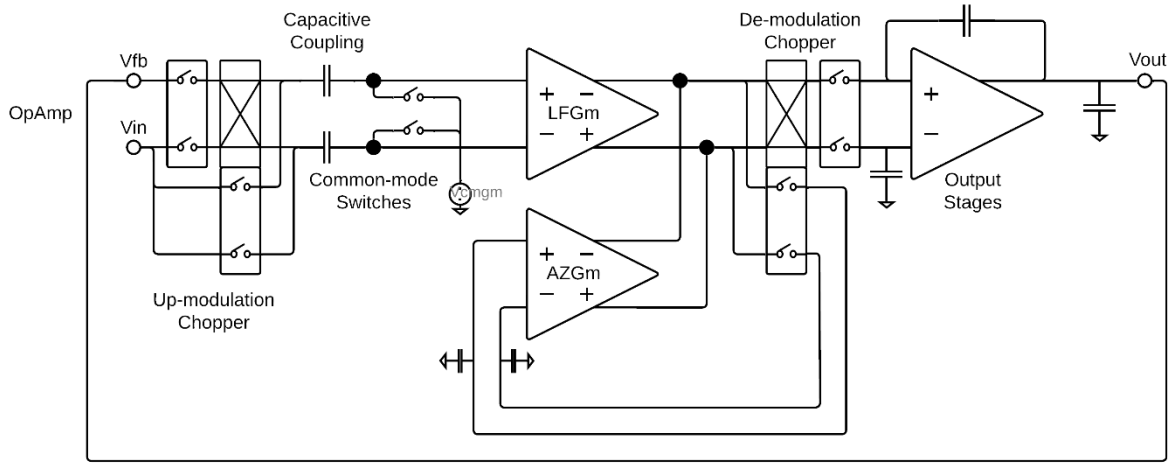


*Figure 2.17 Simplified Operational Amplifier Design*

The multi-path operational amplifier including the high-frequency path is implemented as shown in Figure 2.18. The cross-modulator demodulates the signal at the input of LFGm back to DC and applies it to the HFGm. The output of HFGm then bypasses the second stage and is applied to the third stage. Compared to a nested Miller compensation, the use of multi-path compensation limits the loss of bandwidth from a factor of four to a factor of two [29].

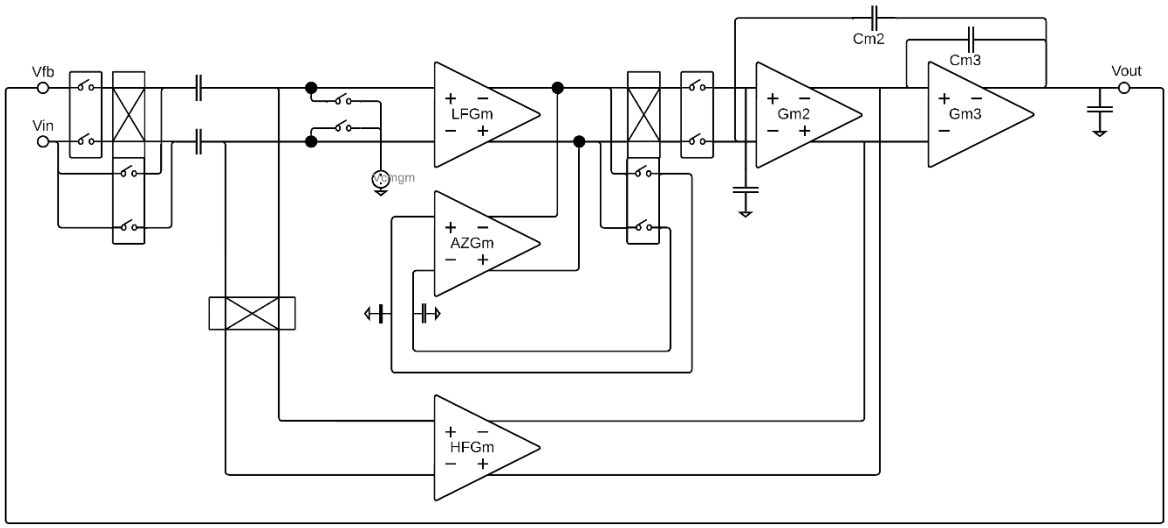


*Figure 2.18 High-Level Operational Amplifier Design*

The amplifier as shown in Figure 2.18 should have a low noise spectral density and uses chopping, autozeroing, and power consumption to achieve this. Thus, Gm1 (LFGm) is set to 120 µS to meet the noise spec of the amplifier of less than 50 nV/√Hz noise spectral density. Gm4 (HFGm) is also set to 120 µS to achieve a flat noise spectrum. The amplifier should also be stable and have a high unity gain bandwidth. Therefore, Gm3 is set to 500 µS, so that while driving a 20-pF load capacitor a unity gain bandwidth of 4 MHz can be achieved. The remaining transconductances and capacitances are then determined as described in *Section 6.2.3 Three-GA-Stage Frequency Compensation* of [3], which describes the optimal ratios of $Gm3/Cload$, $Gm4/Cm3$, $Gm2/Cm3$, and $Gm1/Cm2$. Gm2 is chosen to have a value of 40 µS. Cm2 is sized as 10 pF and Cm3 as 5 pF. This results in a multi-path operation with a crossover between the low and high frequency paths and a phase margin of approximately 60 degrees.

# 3. Design Implementation

This chapter continues the high-level system design. The amplifier design continues with transistor-level implementation details using the TSMC 180 nm process. The switching blocks of the operational amplifier use the clock scheme described in this chapter. The clock scheme interleaves the two techniques of chopping and autozeroing. The clock scheme is motivated with a comparative analysis of various clocking effects.

## 3.1. Transistor-level Design

The op-amp is drawn in buffer configuration with its output connected to its input with negative feedback. Figure 3.1 shows the block schematic of the operational amplifier design which will be discussed in the following sections. Its main parts are: the LF input stage OTA Gm1 (LFGm), the second stage OTA Gm2, the output stage OTA Gm3, the autozeroing OTA GmAZ or AZGm, the autozeroing storage capacitors for auxiliary amplifier inputs (AZCAPS), the HF input stage OTA Gm4 (HFGm), the coupling capacitors for level shifting the input common-mode voltage (LVLSHFT), the autozeroing switches and up-modulating chopper (AZCP1), the autozeroing switches and de-modulating chopper (AZCP2), the high-frequency multi-path chopper so called a cross-modulating chopper (HFCP), and the input common-mode voltage clamp for setting the common-mode voltage at the inputs of the first stage (CMVC). Additionally, the common-mode feedback amplifier and the biasing are also discussed.

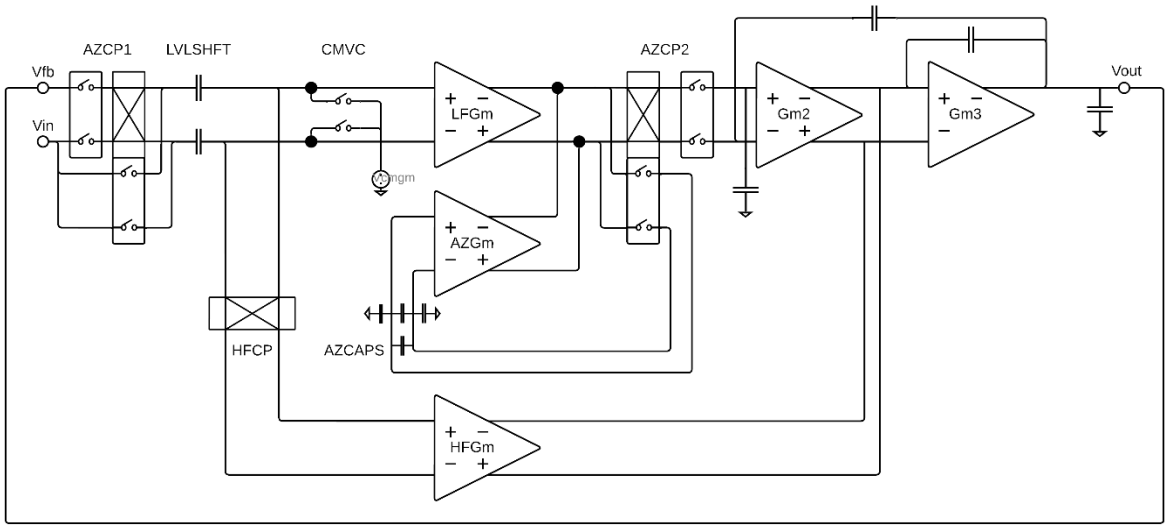


*Figure 3.1 High-Level Operational Amplifier with Callouts*

### 3.1.1. Gm1 (LFGm)

Gm1 (LFGm) is the LF input stage OTA. It is a folded cascode amplifier, as shown in Figure 3.2. This simplifies the design and eases implementation, which are valuable considerations. Furthermore, the cascodes of the output branch provide an excellent summation node for the offset-correcting current provided by AZGm. Also, the folded cascode has a wide input voltage range. However, this is not needed as the amplifier is capacitively coupled. Thus, the input voltage range of the overall amplifier is decoupled from that of the first stage. The amplifier can thus have input voltages beyond the supply rails. However, the folded cascode has limited linearity. This is tolerated as the high gain and the periodic refreshing of the level-shifting

voltage on the coupling capacitors ensure a small swing. It also has a limited output current. This is also not an issue as this is a 3-stage amplifier with a dedicated output stage. Lastly, the noise efficiency is decreased due to the extra noise contributors of the current sources and sinks in the output branch of the folded cascode [34]. These can be tolerated at the cost of slightly increased power consumption.

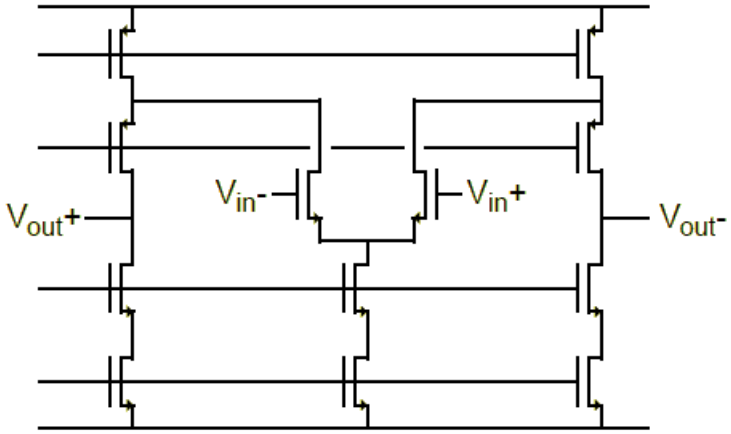


*Figure 3.2 Differential Folded Cascode Amplifier [34]*

The folded cascode design is depicted in Figure 3.3. The differential pair (DifPair) is chosen to have a transconductance of 120 µS to meet the speed and noise requirements of the amplifier [3] [36]. The input transistors are sized for noise performance and native offset optimizations. The current sinks (NSink) are split into two blocks, one for common-mode feedback, and resistive degeneration is used to minimize their noise contributions further [34]. The main noise contributor with ~50 % is the signal differential pair (DifPair). Next, there is considerable noise of ~18 % from PMOS current sources (PSource) and ~16 % from NMOS current sinks (NSink). Finally, adding an autozeroing differential pair (to 1.5 µA nodes) adds further noise to the circuit. This is a twofold effect. The noise from autozeroing differential pair transistors (~12 %) deteriorates overall noise and NMOS current sinks (NSink) have more current and therefore introduce noise (~4 %). The noise of the cascodes (PCasc & NCasc) in a folded cascode barely contributes to the circuit noise. This is because the transfer function from the cascodes to the output node is practically zero [8]. Offset depends on differential pairs (DifPair), current sources (PSource), and current sinks (NSink). Thus, proper sizing of the transistors is essential to minimize the native offset of the amplifier. The 3-sigma offset of the amplifier is approximately 2.5 mV.

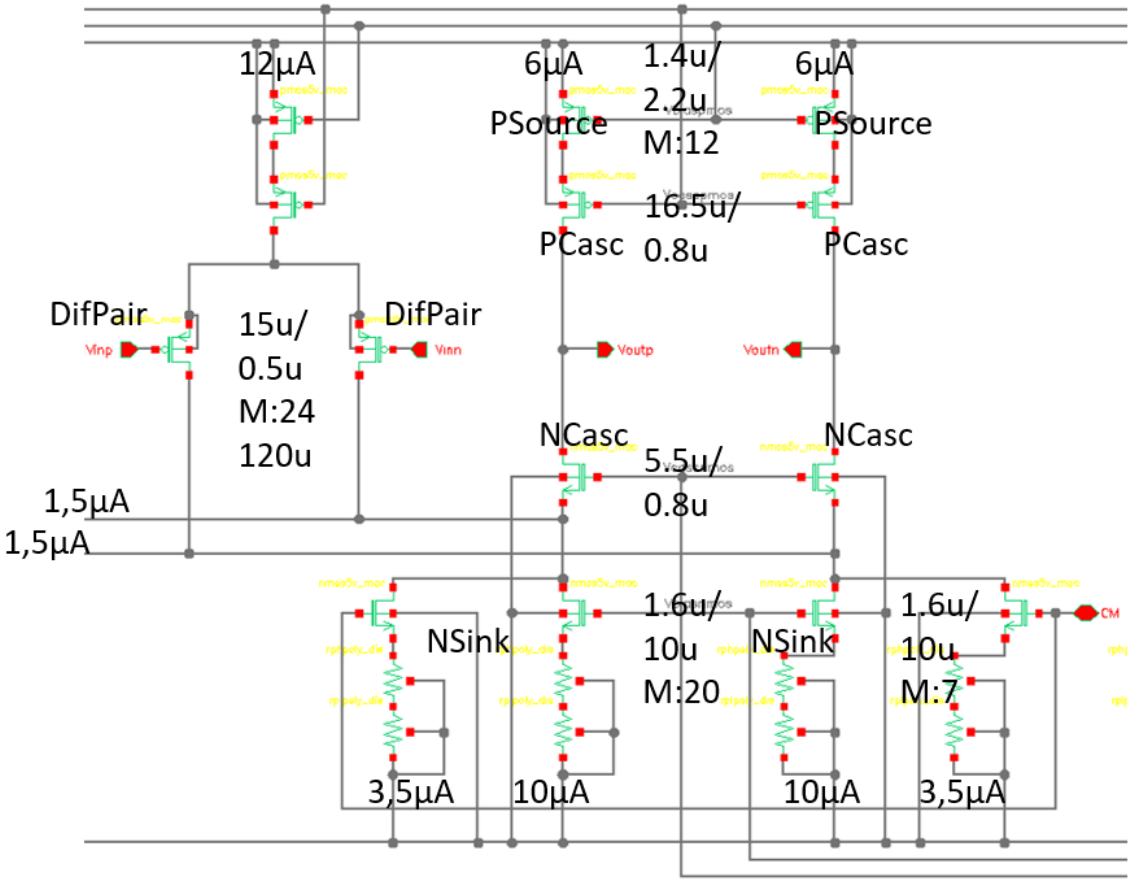


*Figure 3.3 Gm1 First Stage Folded Cascode Amplifier*

### 3.1.2. Gm2

Gm2 is also designed as a folded cascode amplifier [34]. Gm2 is shown in Figure 3.4. The cascodes (NCasc) of the secondary branches provide a low-impedance node at their source. The low-frequency (LF) and high-frequency (HF) paths of the multi-path amplifier sum at the low-impedance node. The transconductance of Gm2 determines the crossover frequency [29]. The transconductance is chosen as 40 µS. Therefore, the LF and HF paths have a crossover frequency of approximately 500 kHz. The gain of the first stage attenuates the offset and noise of the second stage [17]. Therefore, some transistors of Gm2 are sized smaller than those of Gm1. The DifPair transistors are sized the same as 15/0.5, the PSource are sized the same as 1.4/2.2, the PCasc are sized smaller as 16.5/0.8 vs. 8.1/0.6, the NCasc are smaller as 5.5/0.8 vs. 2.7/0.6, and the NSink are smaller as 1.6/10 vs. 0.8/5. Furthermore, trans-linear control transistors (Ctrl) are added between the right branch of the output currents. These are used to drive the class-AB output stage [3] [36] [42]. A replica transistor (Copy) is then added to the left branch of the output currents to improve the matching between the two branches.

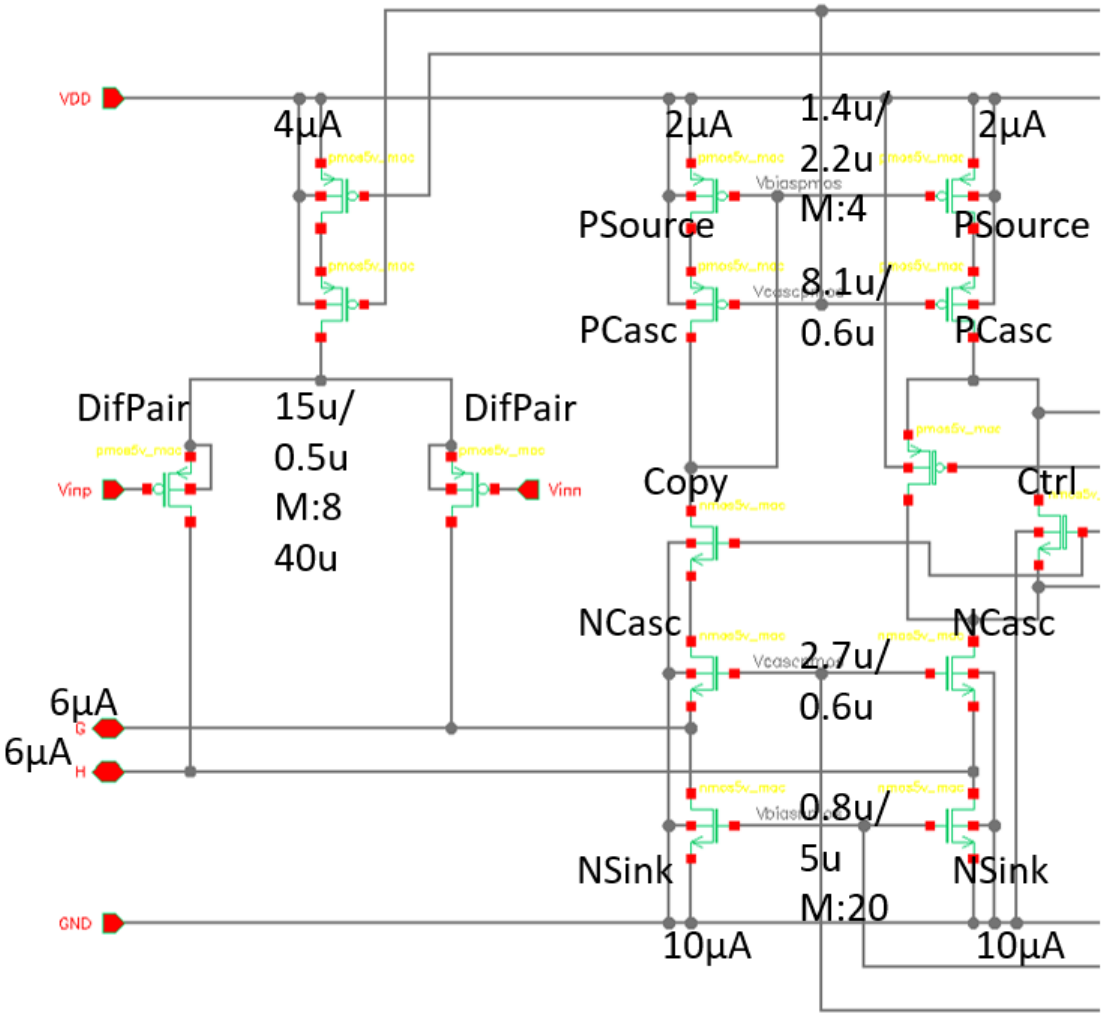


*Figure 3.4 Gm2 Second Stage Folded Cascode Amplifier*

### 3.1.3. Gm3

Gm3 depicted in Figure 3.5 is the third and output stage. It is a class-AB stage general common source amplifier with high efficiency, good linearity, and almost rail-to-rail output range [3] [36] [42]. It also has Miller capacitors (not shown) and thus negative feedback across both output transistors (POut and NOut). The output transistors are very robust due to the trans-linear loop biasing. Each loop is made up of four (PMOS or NMOS) transistors. The loop goes down through the diode-connected PMOS transistors (PDiode1 and PDiode2) and their gate-to-source voltages. It then goes up two gate-to-source voltages with the PMOS transistor (PCtrl) within the folded branch and the output transistor (POut). The other loop has four NMOS transistors (NDiode1, NDiode2, NCtrl, and NOut). The class-AB output stage drives the load impedance, which is a 20-pF capacitance. The output stage has a high transconductance of 500 µS and a low distortion. Additionally, class-AB biasing delivers output currents with high efficiency. Furthermore, the output voltage range of the circuit is almost rail-to-rail, with only saturation voltages missing from both sides of the rails, which are approximately 200 mV. The last design consideration is sizing the output transistors with a low W/L ratio and a large length

to ensure transistors have low sensitivity to process variations and supply variations and thus have a high power-supply-rejection ratio [3] [43].

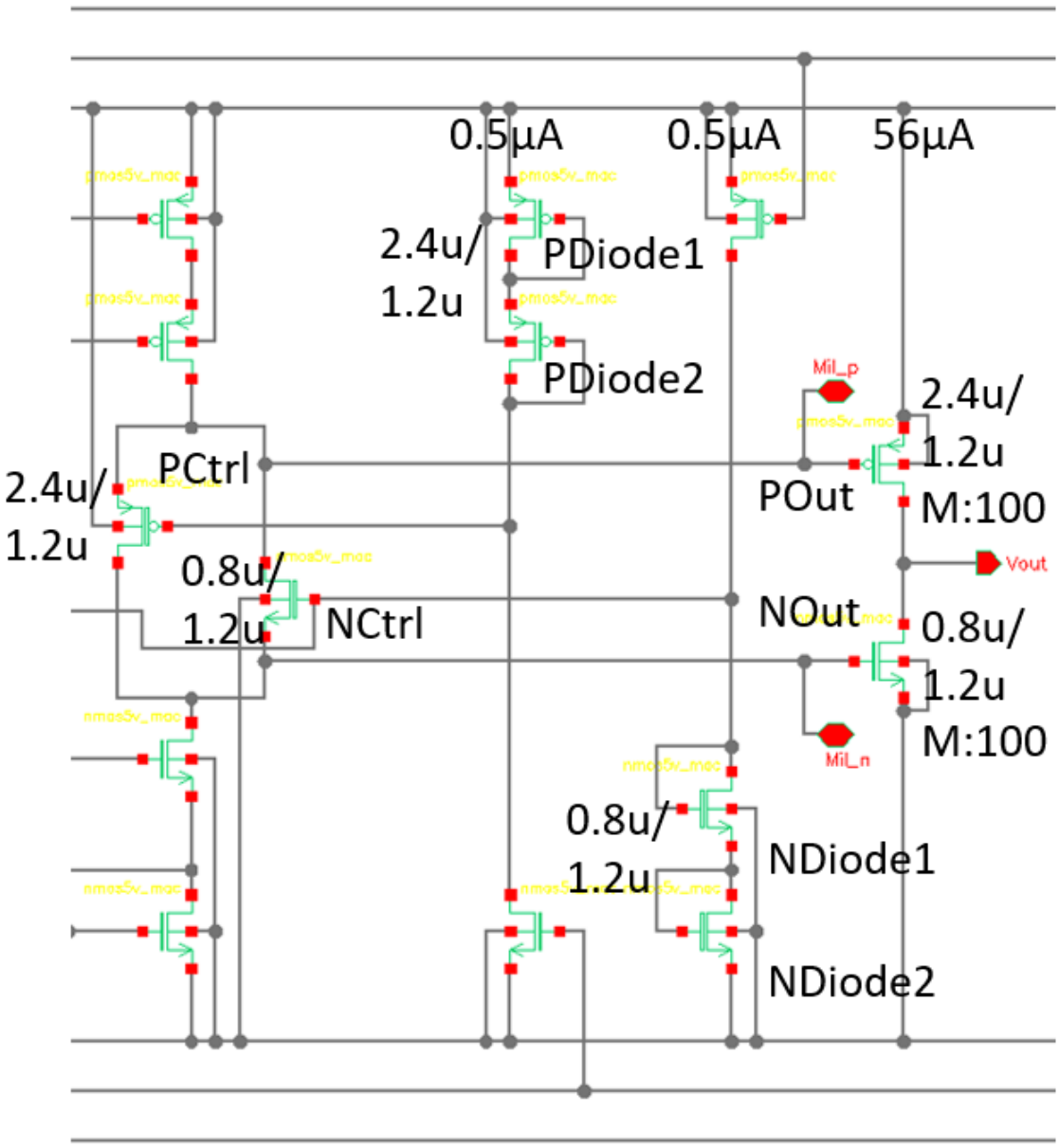


*Figure 3.5 Gm3 Class-AB Output Stage with Trans-linear Control*

### 3.1.4. GmAZ (AZGm)

An auxiliary amplifier, GmAZ (AZGm), is used to perform auto-zeroing [17]. It employs a differential pair, which, like Gm1, has a 3-sigma native offset in the 2.5 mV range. A smaller GmAZ requires a larger differential voltage to deliver the same correction current, which will be limited by the linear input range of the differential pair [34]. Therefore, the effective autozeroing range decreases with lower GmAZ transconductances. As explained in section 1.3.2.1.3, this problem can be mitigated by trimming the native offset down to the linear range of GmAZ. However, this is costly. Another potential solution is to degenerate GmAZ. The

linearity of the source degenerated transconductor improves and therefore, degeneration increases the linear range of GmAZ.

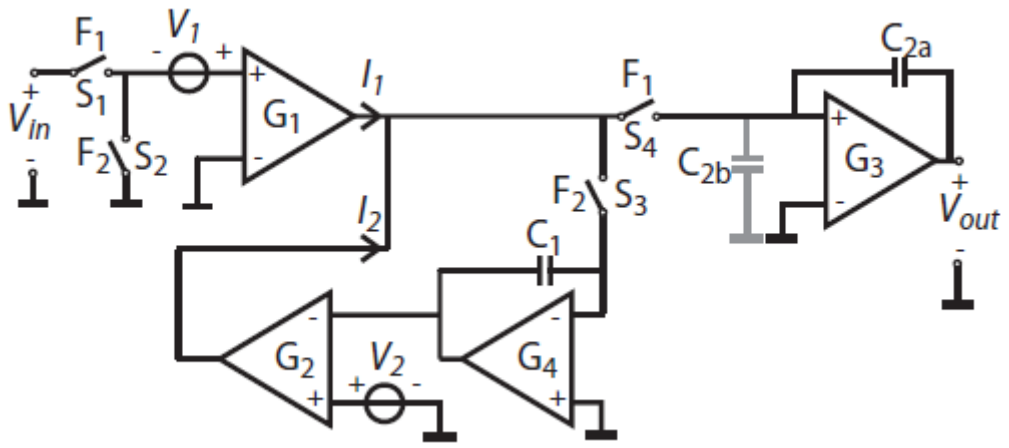


*Figure 3.6 Autozeroing with an auxiliary amplifier and an active integrator [16]*

The relationship between the transconductance of GmAZ and its relative ratio to the transconductance of Gm1 (120 µS) and the residual offset and therefore the ripple of the chopped amplifier is analyzed with a testbench using ideal transconductances, as shown in Table 3.1. The periodic steady state analysis of Cadence is used. The analysis is independent of the settling time constants and computes the steady-state response of the autozeroing circuit at the clock frequency of 50 kHz. The autozeroing pulse length is a control variable and Gm1/GmAZ ratio is limited for the linearity of the differential pair. A smaller GmAZ (larger Gm1/GmAZ ratio), minimizes the extra noise contributions resulting in lower noise. It also decreases sensitivity to charge injection from the switches. The autozeroing loop has decreased gain with smaller GmAZ, resulting in an increased residual offset and worsened ripple. A potential solution is to use a two-stage amplifier with an active integrator, as shown in Figure 3.6. The active integrator increases the loop gain and therefore decreases residual offset and ripple. Furthermore, the active integrator mitigates voltage steps [17]. This thesis elects to use a Gm1/GmAZ of 120 µS/30 µS. This is cheaper than trimming and simpler than a two-stage amplifier [33].

*Table 3.1 Gm1/GmAZ and Autozeroing Analysis Summary*

| AZ Pulse (ns) | Gm1/GmAZ | Noise (nV/√Hz) | Ripple (µV) |
|---|---|---|---|
| 400 | 3 | 24.8 | 5.0 |
| 400 | 4 | 24.1 | 7.3 |
| 400 | 5 | 23.7 | 9.7 |

### 3.1.5. Autozeroing Capacitors

This design uses a low-frequency path amplifier (LFGm) and an auxiliary autozeroing amplifier (AZGm), as shown in Figure 3.7. During the autozeroing phase, the input switches (CMVC) short the input of LFGm, and the autozeroing loop switches (AZCP2) complete the autozeroing loop.

The offset is integrated on the autozeroing capacitors (AZCAPS) until the resulting differential current from this voltage difference cancels at the summation node. For the autozeroing capacitors one possible implementation is to use two differential capacitors from both AZGm inputs to the ground. But this does not have any common-mode memory. A better implementation uses an arrangement of four capacitors with both common-mode and differential components, as shown in Figure 3.7. The bandwidth of the autozeroing loop decreases with increasing autozeroing capacitors. This reduces the noise in the loop that can fold back down to lower frequencies [30]. At the same time, charge injection also decreases. Given infinite time to settle and provided it has enough loop gain, the autozeroing loop would eventually converge to zero offset. However, with limited time, the time constant (tau) of the loop determines the settling accuracy. Decrease in bandwidth results in slower settling of the offset cancelation loop. The time constant (tau) of the loop decreases, and the loop settles less given the same time to settle. The residual offset from autozeroing increases and therefore the ripple after chopping increases. An autozeroing capacitance of 2 pF is chosen.

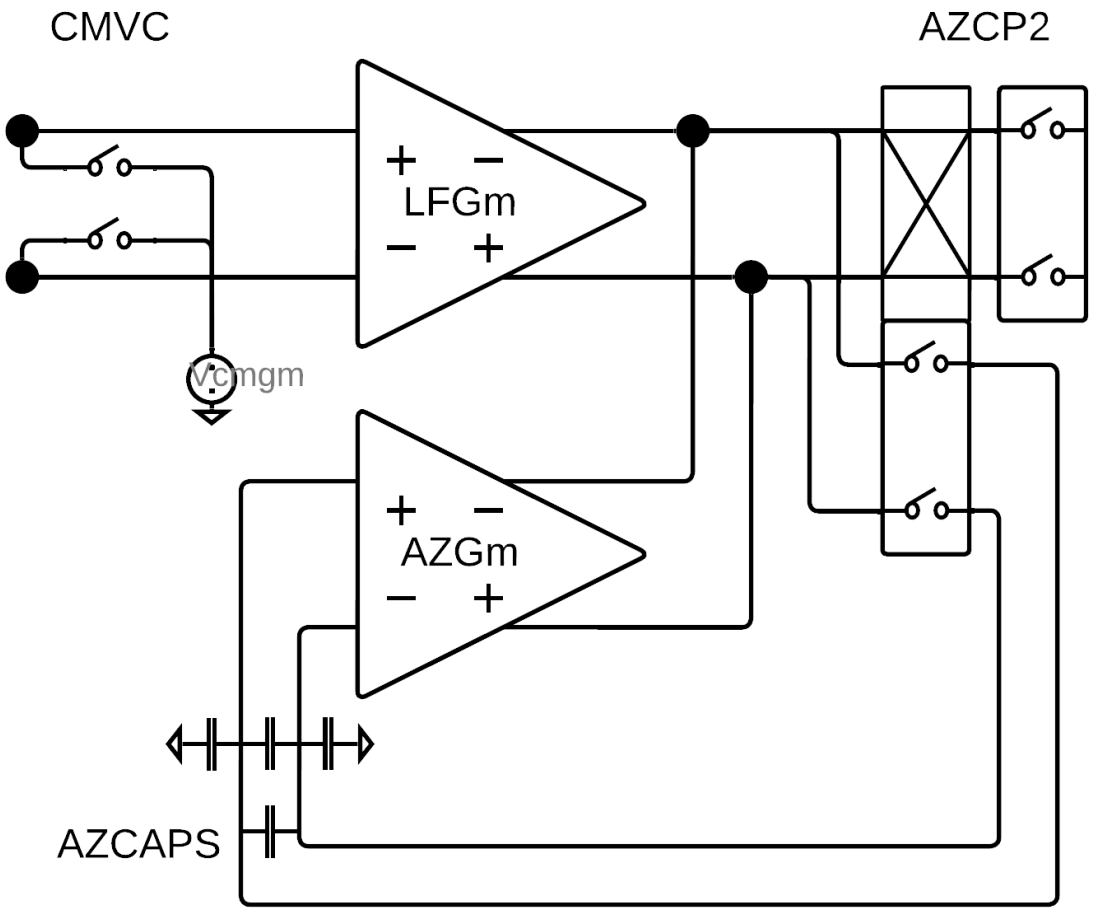


*Figure 3.7 Autozeroing Loop and Input Offset Cancelation*

### 3.1.6. Common-Mode Feedback (CMFB) Amplifier

The differential common-mode feedback amplifier in Figure 3.8 is used at the output of the signal (LFGm) and autozeroing (AZGm) amplifiers, shown in Figure 3.7. The CMFB senses both

outputs of the first stage (LFGm) as inputs (In1 and In2) and sums up two currents (Sum1) proportional to gate voltages. Another two currents are generated using a reference (Ref) and summed up (Sum2) for comparison. The implementation uses long transistors (0.22/18) to generate this reference voltage of 2.5 V. The comparison currents (Sum2) are fed to a diode-connected current sink. This is fed back to the common-mode tracking of Gm1 current sinks, completing the feedback loop [44] [45] [46].

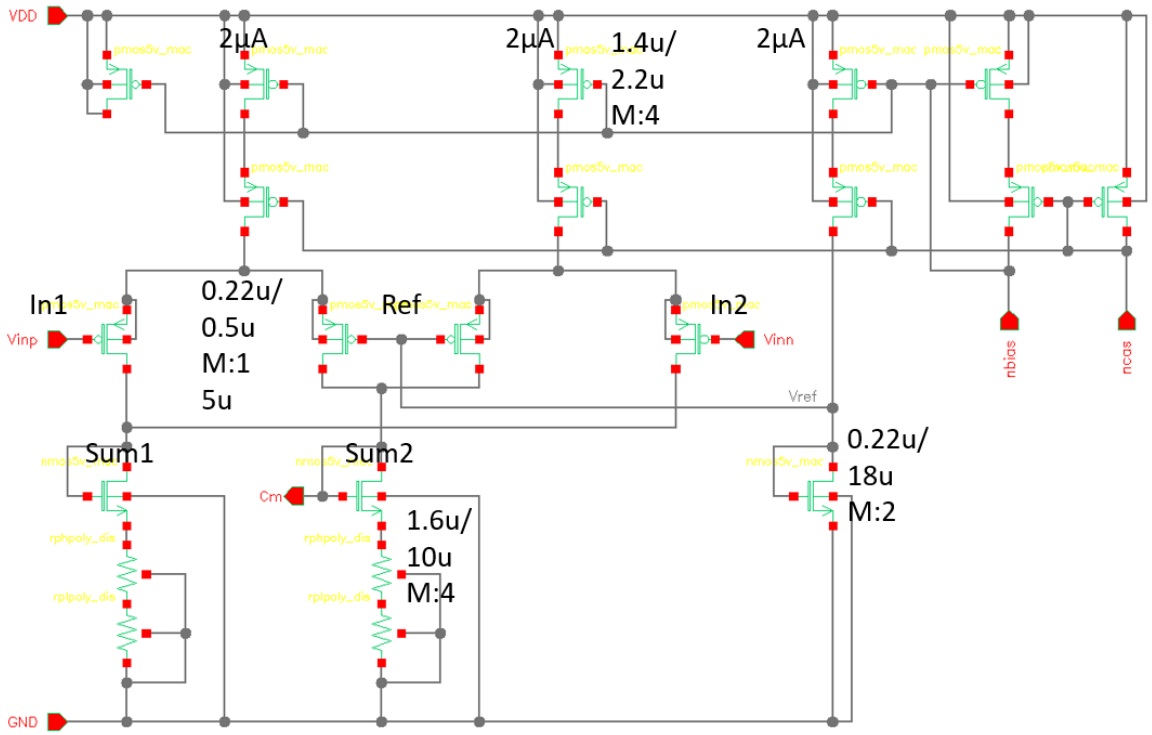


*Figure 3.8 Common-Mode Feedback (CMFB) Amplifier*

### 3.1.7. Gm4 (HFGm)

Gm4 (HFGm) is the HF input stage OTA. It uses the same differential pair as Gm1 [34]. This is for matching. The cascodes of Gm2 provide a suitable summation node for the currents of Gm4 to inject into the output stage. The gain of the low-frequency path makes the offset of Gm4 trivial. However, noise is not affected similarly. After the crossover frequency, the dominant noise source changes from Gm1 to Gm4. Thus, Gm4 is chosen to have a transconductance of 120 µS to match Gm1. This ensures a flat noise spectrum over frequency [3].

### 3.1.8. Coupling Capacitors with Level Shift

The input structure is shown in Figure 3.9. The coupling-capacitors (C1 and C2) are charged to the level-shifting voltage (LVLSHFT). They separate the input voltage of the capacitively coupled amplifier from the common-mode voltage at the input of Gm1 (LFGm) [23] [26].

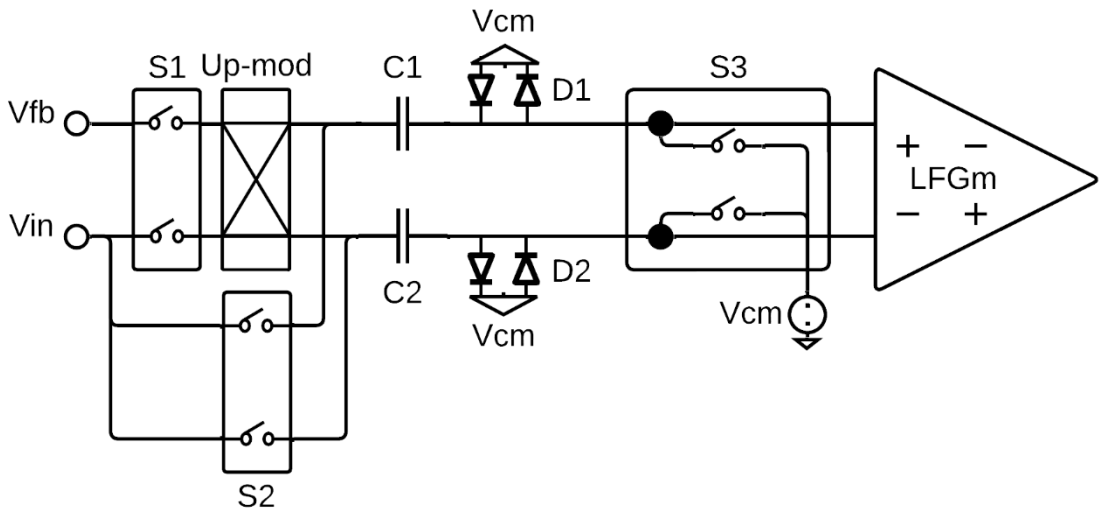


*Figure 3.9 Coupling Capacitors with Level Shift and Input Stage*

The coupling capacitors are sized with a few design considerations. The noise benefits from larger capacitances since the $kT/C$ noise, as explained in section 1.2.4, is reduced. The DC gain and phase margin of the circuit also benefit from larger capacitance. The main limitation to increasing capacitance is the associated capacitor area. The capacitance analysis is summarized in Table 3.2 below. The performance improvements due to increasing capacitance have diminishing returns. Therefore, a value of 15 pF is chosen for the coupling capacitors.

*Table 3.2 Coupling Capacitor with Level Shift Analysis Summary*

| Coupling Capacitor (F) | 1p | 5p | 10p | 15p | 20p |
|---|---|---|---|---|---|
| Phase Margin (°) | 79 | 68 | 66 | 65 | 64 |
| Gain Margin (dB) | 20 | 15 | 13 | 13 | 13 |
| UGB (MHz) | 0,9 | 1,5 | 1,8 | 1,8 | 1,9 |
| DC Gain (dB) | 177 | 182 | 182 | 182 | 183 |
| Residual Offset (nV) | 860 | 120 | 30 | 10 | 20 |
| Output Spikes (µV) | 360 | 360 | 360 | 360 | 360 |
| Noise Level (nV/√Hz) | 100 | 34,2 | 28,7 | 27,4 | 26,8 |
| Ripple (µV) | 20 | 9 | 7,5 | 7,1 | 6,9 |

### 3.1.9. Biasing

Eight identical long tail 1 µA currents are mirrored from a main biasing current as shown in Figure 3.10. Transconductance blocks of this amplifier use current mirrors that source 1 µA from these eight current sinks [34].

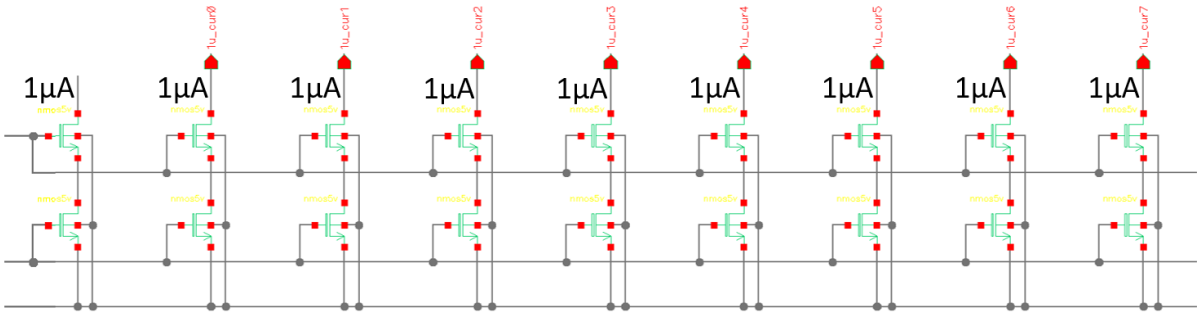


*Figure 3.10 Current Sinks*

The main biasing current is generated with start-up and temperature compensation, as shown in Figure 3.11. The current mirrors are connected along the dotted arrows. The biasing uses 12 µA, this is negligible compared to the total current consumption of 256 µA.

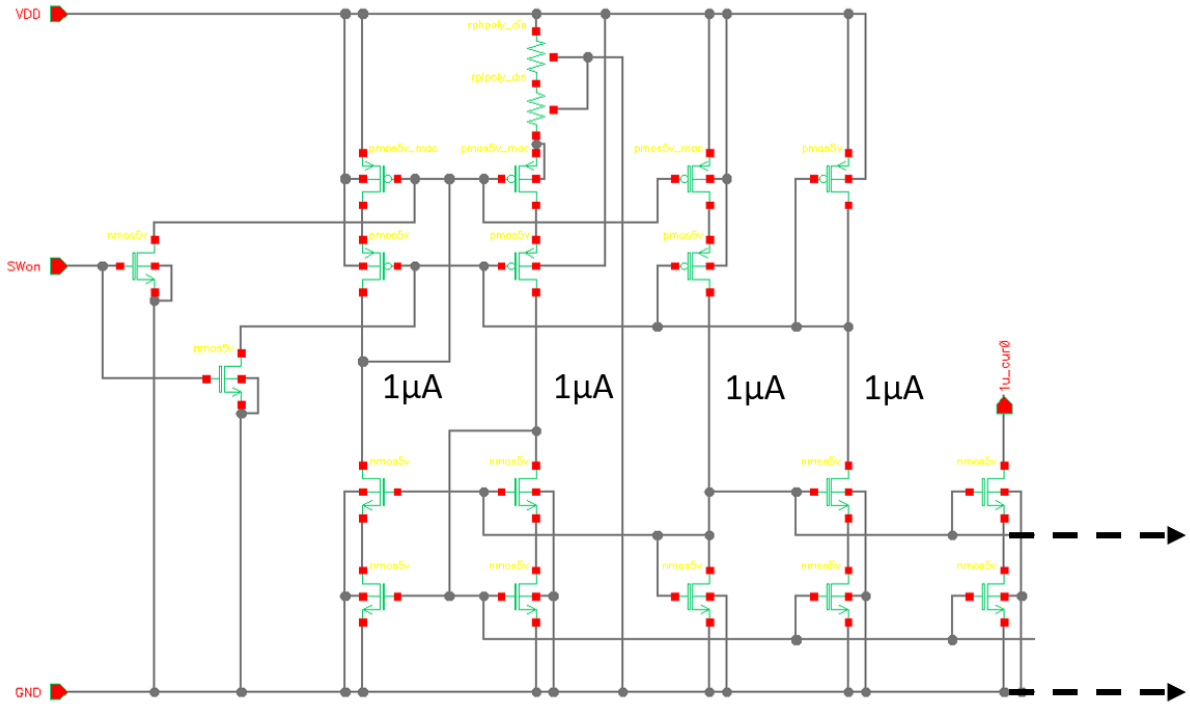


*Figure 3.11 Biasing Block*

### 3.1.10. Autozeroing Switches and Up-Modulation Chopper (AZCP1)

The simple implementation of the autozeroing switches and up-modulating chopper (AZCP1) is shown in Figure 3.12. AZCP1 up-modulates signals and passes them through the coupling capacitors. Chopping is performed by the four polarity reversing switches, two transistors for each state. The level shifting voltage is refreshed by another two switches. These are transistors with autozeroing phase (AZ) on their gates connecting the input voltage to both coupling capacitors.

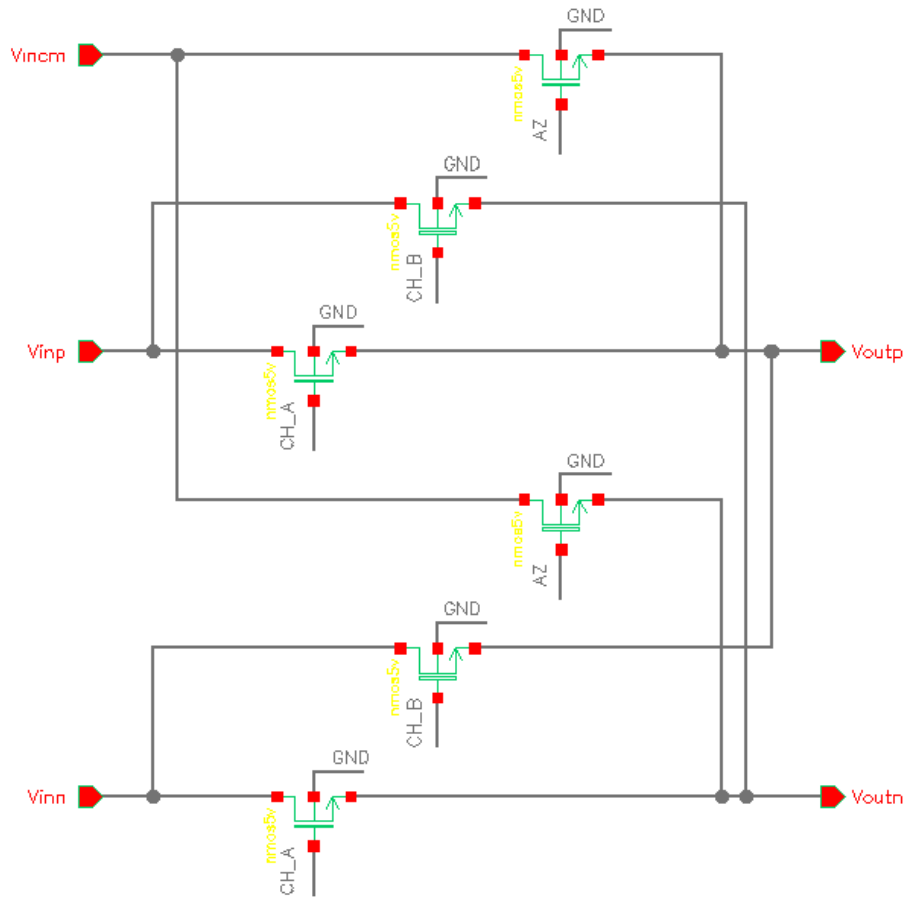


*Figure 3.12 Autozeroing Switches and Up-Modulation Chopper (AZCP1) Simple Implementation*

This amplifier senses beyond-the-rail common-mode voltages. However, AZCP1 of Figure 3.12 only works with limited input common-mode ranges and does not work with this amplifier's desired beyond-the-rail input range. Floating input choppers are necessary to sense beyond-the-rails [23] [40] [41]. Floating input choppers in [23] [40] [41] use boosted gate voltages to turn on the transistors. The choppers are controlled using a floating latch. The latch of [23] [40] [41] is only suited to applications with chopping and lacks autozeroing. The new control latch design in Figure 3.13 expands upon the latch and has both chopping and autozeroing phases.

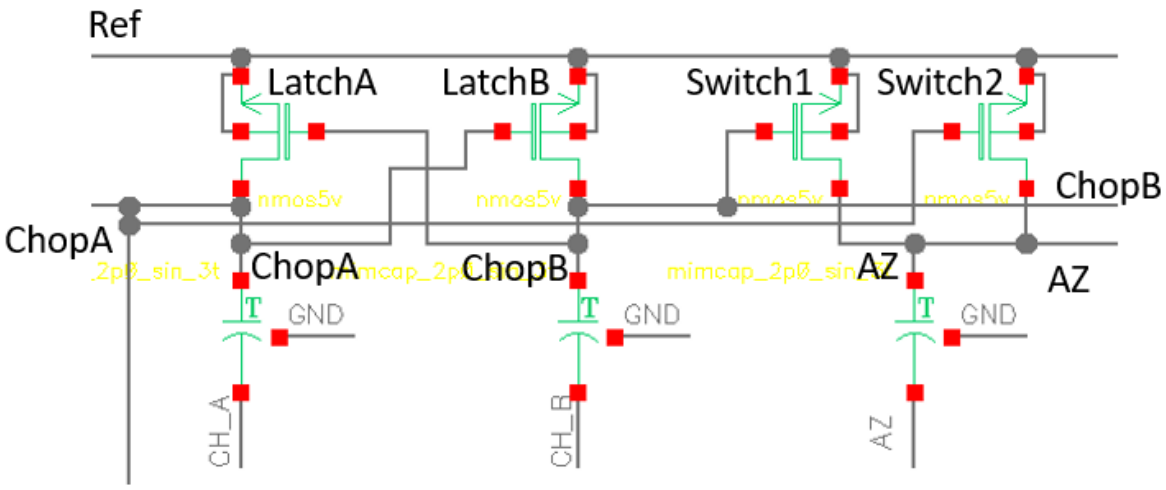


*Figure 3.13 Modified Floating Latch*

The modified floating latch consists of a latch and two outer switch transistors. The latch holds the data with the cross-coupling feedback of the latch transistors (LatchA and LatchB). The truth table of the modified floating latch is shown in Table 3.3. Two of its outputs (Chop A and ChopB) go to the chopper switches. Chopping puts the amplifier in either state of its chopping phase. The latch cannot be in both chopping states simultaneously. The third output (AZ) goes to the autozeroing switches. Switches (Switch1 and Switch2) force their drain voltage to their source voltage if either of their gates is high in response to a high voltage in the latch. Autozeroing can happen if both chopping signals are low. When all controls are low, the amplifier is neither chopping nor autozeroing.

*Table 3.3 Modified Floating Latch Truth Table*

| AZ | CH_A | CH_B | Phase |
|---|---|---|---|
| 0 | 0 | 0 | Neither |
| 0 | 0 | 1 | Chopping (B) |
| 0 | 1 | 0 | Chopping (A) |
| 0 | 1 | 1 | Chopping (Previous) |
| 1 | 0 | 0 | Autozeroing |
| 1 | 0 | 1 | Chopping (B) |
| 1 | 1 | 0 | Chopping (A) |
| 1 | 1 | 1 | Chopping (Previous) |

The floating input choppers in [23] with floating bulk voltages are used. The bulk voltage needs to be defined. Either of the inputs can be used for the bulk connection. Alternatively, a minimum selector as shown in Figure 3.14 can be used. It selects the lower input voltage of

the two (Input1 or Input2) as the cross-connection of gates turns on the opposing transistor. The bulk voltage (Bulk) is then connected to the minimum. This minimum bulk voltage ensures that all switches can be turned off. Additionally, back-to-back diodes are added to limit the voltage difference between the two input terminals for increased circuit protection [23].

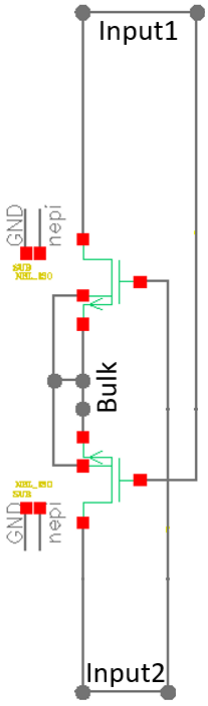


*Figure 3.14 Minimum Selector*

The switch transistors are 5 Volt devices. The voltage across the transistors cannot be larger. The voltages of the floating choppers vary with a wide range. Additionally, the chopping and autozeroing clock is added to turn on the switches. This risks the overall voltage to reach an amplitude larger than 5 Volts. Therefore, the clock amplitude is scaled down to 2.4 Volts, to ensure that overvoltage conditions are avoided, and devices are protected against damage. The switches are sized for low on resistance (Ron). The resulting autozeroing switches and up-modulation chopper is shown in Figure 3.15. This capacitively coupled floating input chopper is a new modification with both chopping and autozeroing phases, based on the [23] design.

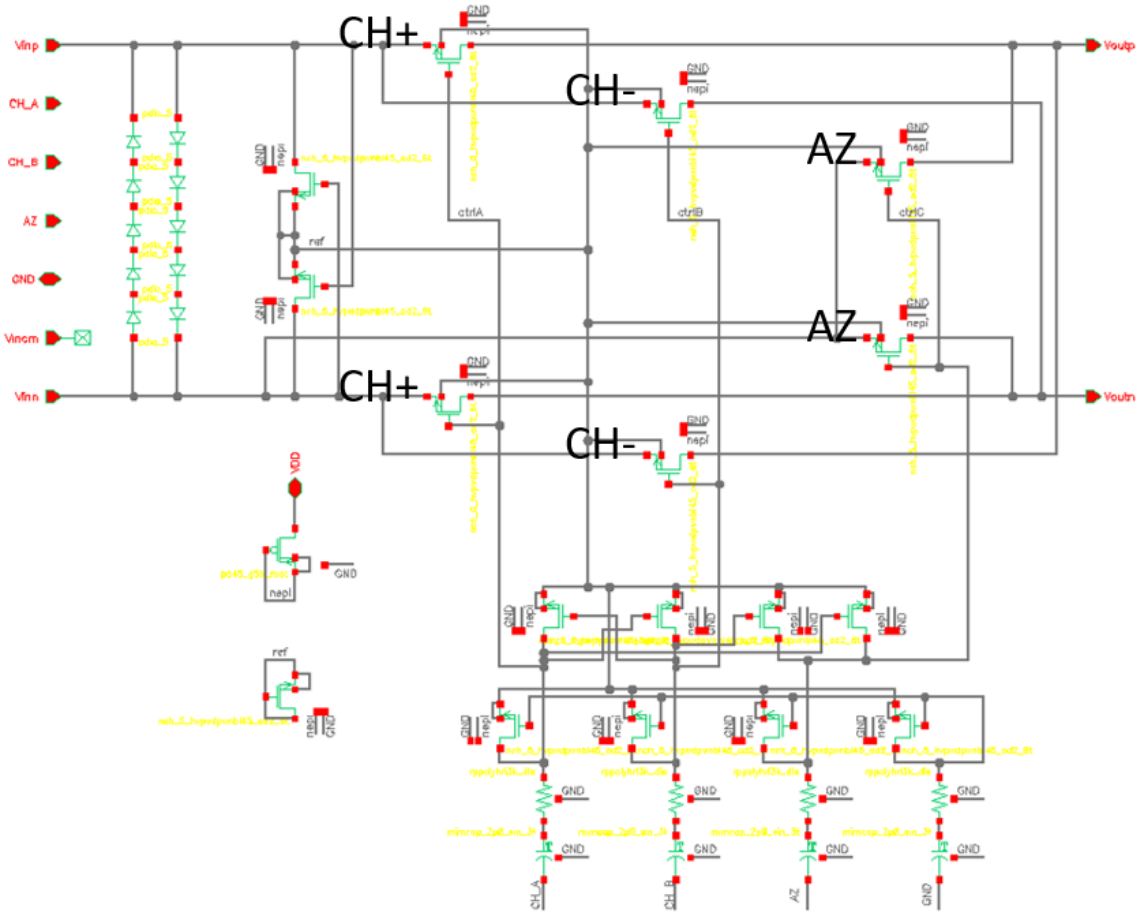


*Figure 3.15 Autozeroing Switches and Up-Modulation Chopper (AZCP1) Final Implementation*

### 3.1.11. Autozeroing Switches and De-Modulation Chopper (AZCP2)

The autozeroing switches and de-modulation chopper (AZCP2) is shown in Figure 3.16. It demodulates signals back to their initial frequency band with chopping. Chopping uses four polarity reversing switches. It closes the autozero loop for offset cancelation with another two extra switches (AZ). The drains and sources of AZCP2 switches are at the CMFB reference voltage of approximately VDD/2.

This design uses one digital block to limit digital power consumption. However, the previously chosen clock amplitude of 2.4 Volts does not turn on the switches of the AZCP2 on its own. It needs higher gate voltages to operate correctly from a low amplitude clock. Therefore, the modified floating latch generates voltages needed to operate the six switches. One latch is used in combination with a minimum selector. This guarantees that the gate voltages track the lower of the two inputs, that there is no performance deterioration, that no switches turn on backward, and that there are no overvoltage conditions. The final AZCP2 implementation shown in Figure 3.16 is used.

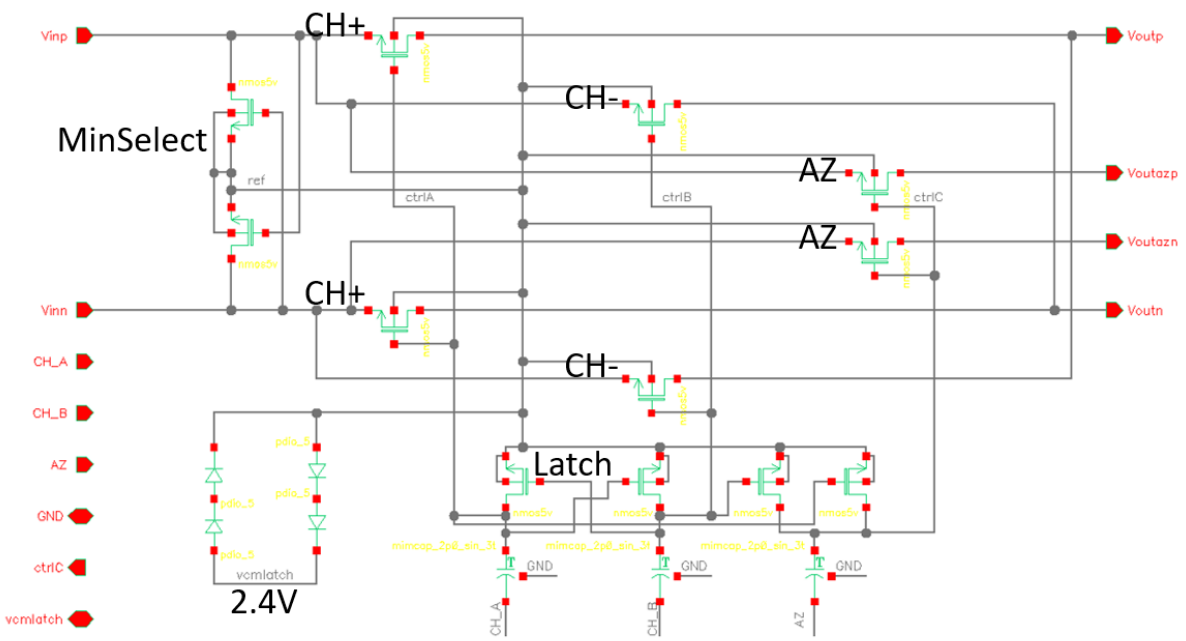


*Figure 3.16 Autozeroing Switches and De-Modulation Chopper (AZCP2) Final Implementation*

### 3.1.12. High-Frequency Multi-Path Cross-Modulation Chopper (HFCP)

The high-frequency multi-path chopper so called a cross-modulation chopper (HFCP) modulates signals back to their initial frequency band at the inputs of the high-frequency path HFGm [3]. As shown in Figure 3.17, it is a chopper with four polarity reversing switches. The clock amplitude is 2.4 Volts, and the drains and sources of the switches are also at 2.4 Volts. Therefore, HFCP has the same voltage problem. The HFCP is only involved in chopping and is not involved with autozeroing. The floating latch is used with a minimum selector. A simple latch is enough, and extra autozeroing controls are unnecessary. The final HFCP implementation shown in Figure 3.17 is used.

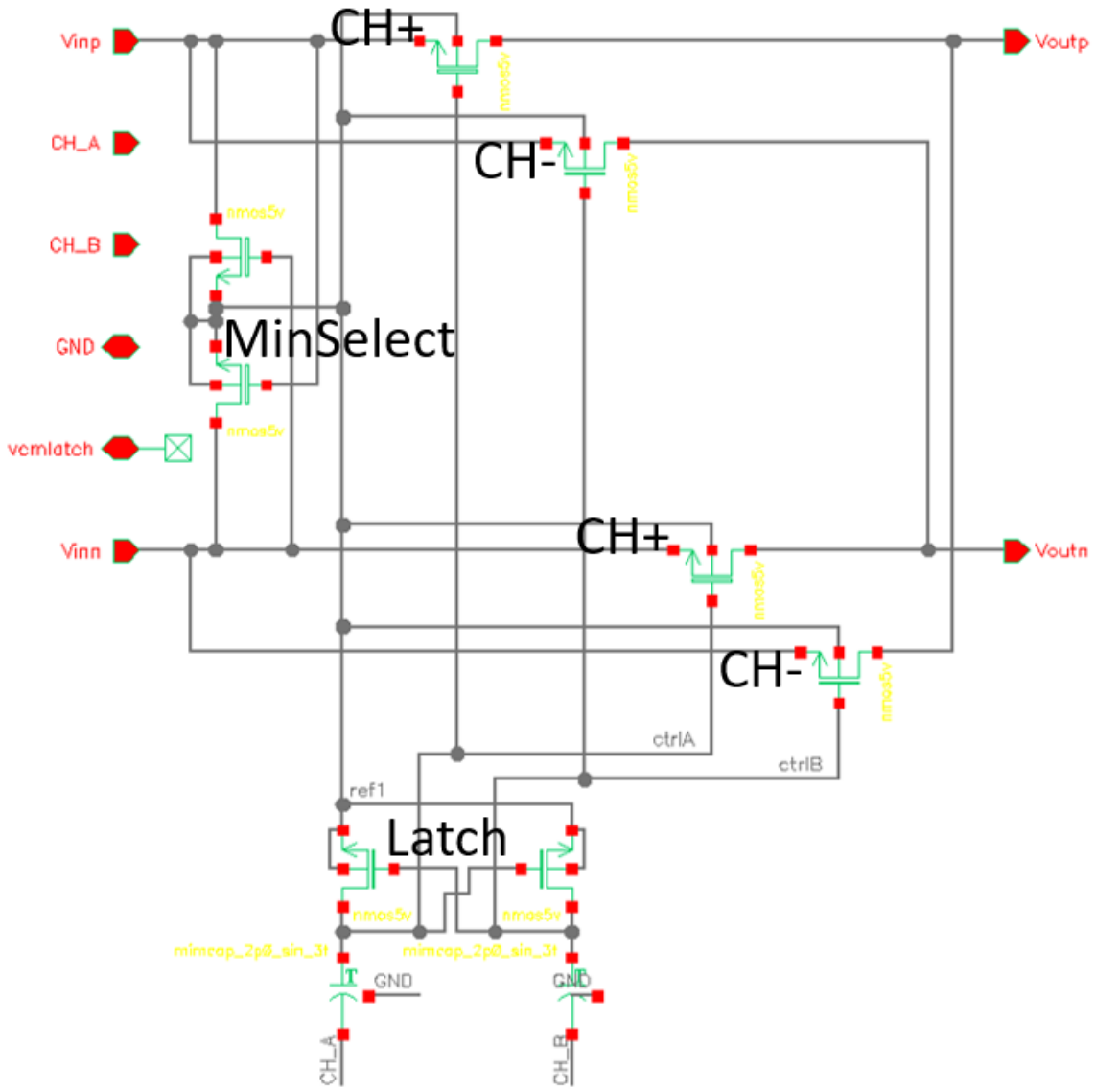


*Figure 3.17 High-Frequency Multi-Path Cross-Modulation Chopper (HFCP) Final Implementation*

### 3.1.13. Input Common-Mode Voltage Clamp (CMVC)

The input common-mode voltage clamp (CMVC) for setting the common-mode voltage at the inputs of the first stage is shown in Figure 3.18. It sets the first stage input common-mode voltages and shorts the input stage to autozero with the auxiliary amplifier and refreshes the level shifting voltage on the coupling capacitors. Setting input voltages is done by shorting a voltage source to both inputs. The voltage source is not designed as part of the thesis. The voltage source is 2.4 Volts. The two switches also short the two inputs. The native offset of the amplifier is then autozeroed with the auxiliary amplifier. These switches with the help of the external switches also refresh the level shifting voltage.

CMVC runs from a 2.4 Volt clock. Modified floating latches (Latch1 and Latch2) are needed to generate voltages to operate the two switches (Switch1 and Switch2). Using one floating latch for both switches is possible. However, a voltage difference caused by a signal swing limits the floating voltage of the latch thereby limiting the operation of the switches. Therefore, two

separate latches are used. Two minimum selectors (MinSelect) are added. This ensures that the floating voltage of the latch tracks the lower of the drain or source voltages, and so do the gate voltages. Thus, switches do not turn on when they are not supposed to. The final CMVC implementation shown in Figure 3.18 is used.

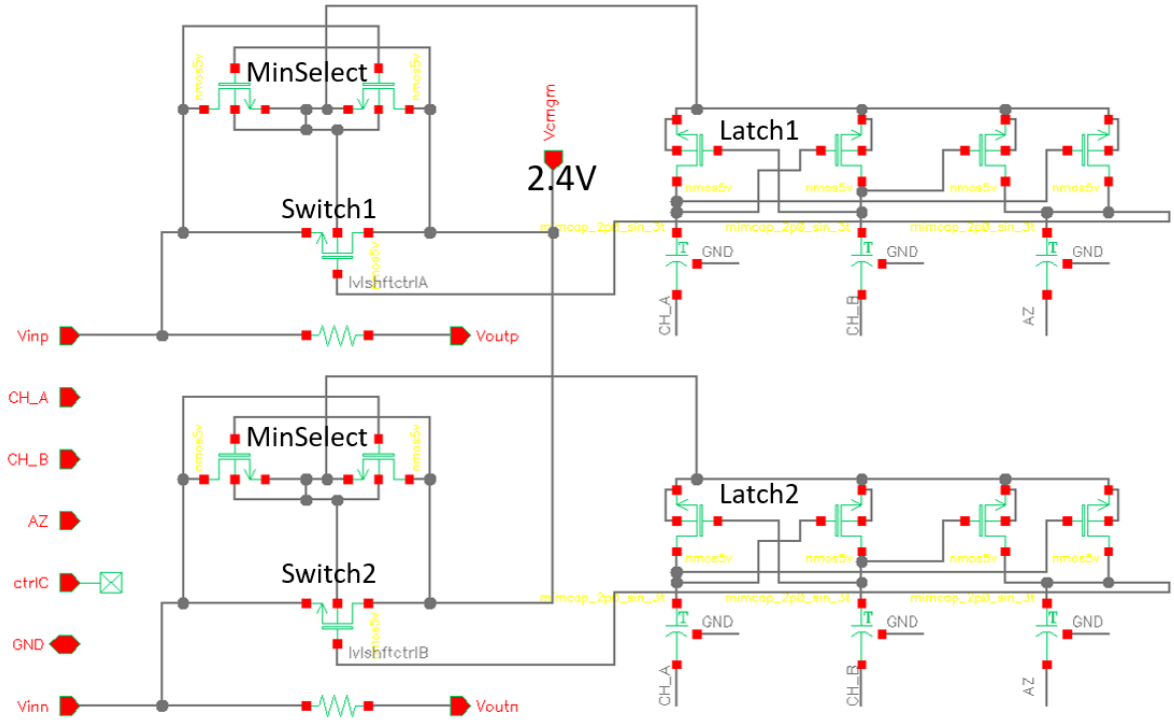


*Figure 3.18 Input Common-Mode Voltage Clamp (CMVC) Final Implementation*

## 3.2. Clock Scheme Design

Alternative clock schemes for chopping and autozeroing the amplifier have been created. For memorability and distinguishability, the clocks are named after titans from mythology. The clocks are Atlas, Themis, Iapetus, Rhea, and Hyperion. Circuit parameters including glitches, phase margin, gain margin, UGB, DC gain, ripple, offset, and noise vary depending on the clocks. The autozeroing offset cancelation accuracy and therefore settling is decided as a control variable. The autozeroing pulse length is set to 400 ns. The chopping frequency is selected as 50 kHz or a total period of 20 µs. The ratio of the autozeroing pulse to the period is 2 %. The effects of different clock schemes are compared. An in-depth analysis of ripple, offset and noise is performed.

### 3.2.1. Switches

The implementation of the switches interleaves the chopping and autozeroing phases. One implementation shown in Figure 3.19 (a0) uses S1 and Up-mod switches in series. The S1 and S2 switches have autozero (AZ) and not-autozero ($\overline{AZ}$) states. The up-mod switches have two equal chopping states. The circuit is not autozeroing and is chopping while the S1 switches are closed, and the up-mod switches are chopping (a1). The circuit is autozeroing when the S2 switches are closed (a2). The downside is that more switches have more noise. The alternative implementation shown in Figure 3.19 (b0) changes the idea of what a chopper is. The chopper

is unlike conventional choppers. These Up-mod chopping switches have three states: both chopping states and open [33]. The S2 switches have two states: autozero (AZ) and not-autozero ($\overline{AZ}$). The S2 switches are open when chopping (b1) and the Up-mod chopping switches are open when the S2 switches are closed during autozeroing (b2).

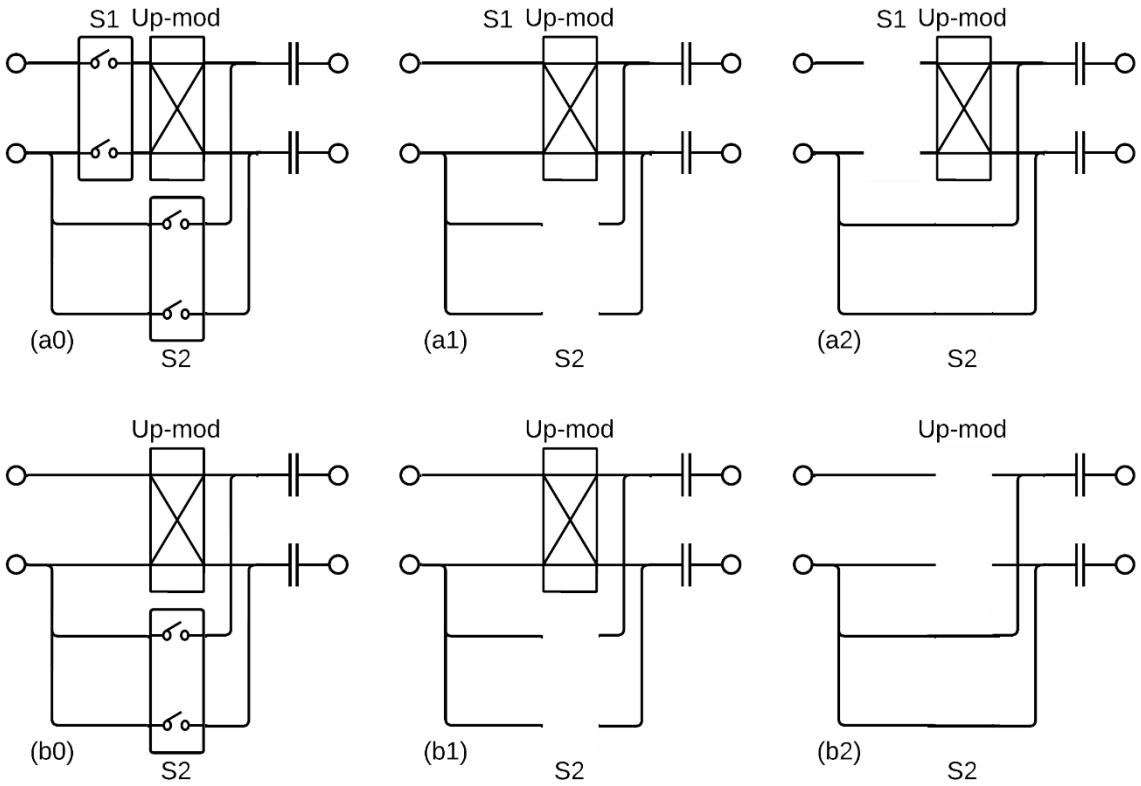


*Figure 3.19 Switch Alternatives a) Series Switches b) Combined Switches*

The clocks need to be recreated as in Figure 3.20 [27]. There are three control clocks operating the switches and these are ChopA, ChopB, and Autozero. The phases are all non-overlapping. Autozeroing borrows time from chopping when both chopping clocks are low. Therefore, the two chopping states are not 50 %.

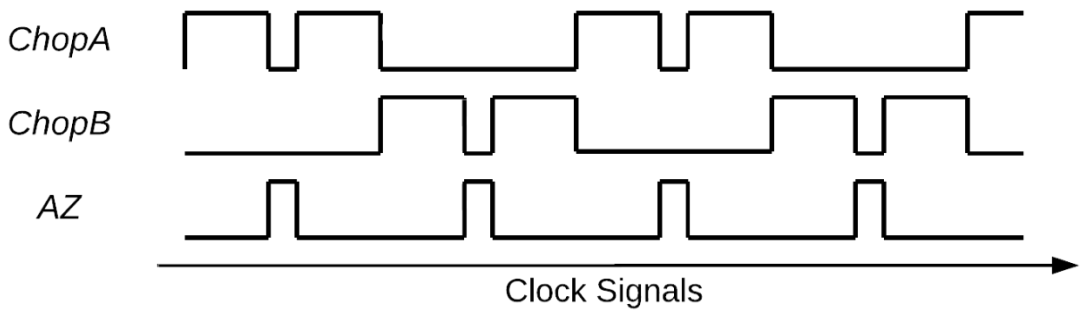


*Figure 3.20 Timing Diagram for Non-Overlapping Phase Control*

### 3.2.2. Clock One – Atlas

The first test clock is shown in Figure 3.21. It is named the Atlas Clock. This clock has a 2 % autozeroing pulse. The remaining duty cycle is split into two equal chopping states of 49 % duty cycles. The Atlas clock has two drawbacks. It has an inherent offset. The offset is due to the extension of the second chopping phase due to the sample and hold action of the Miller capacitors. This is shown in green. It also suffers from noise sampling at the end of autozeroing phase. This sampled noise is chopped unequally, as shown in navy, resulting in an increased noise floor.

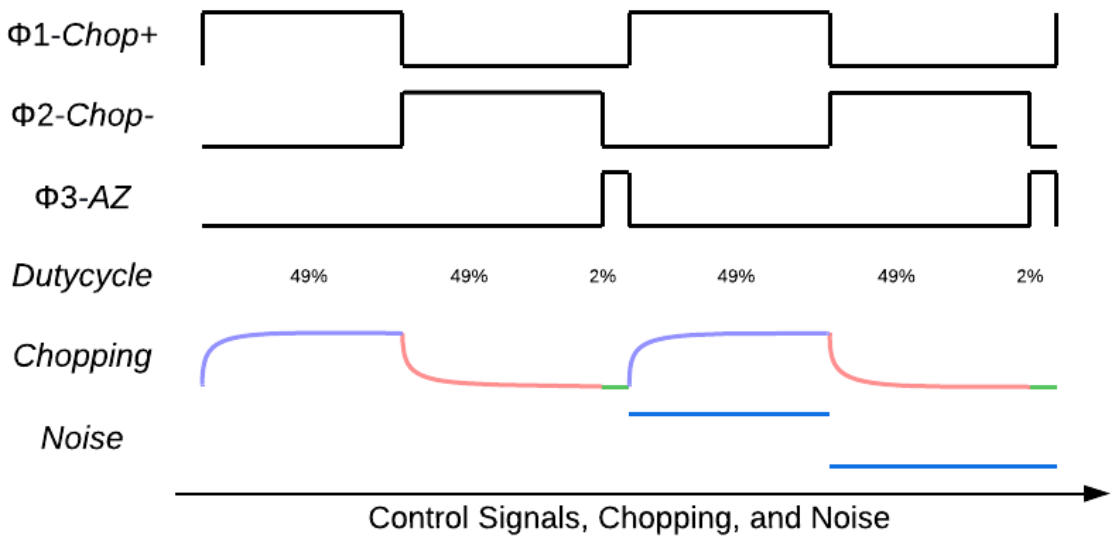


*Figure 3.21 Clock One – Atlas*

The autozeroing part of the duty cycle extends the second chopping phase and thus causes an offset. The autozero duty cycle is exaggerated to ease the description of this problem in Figure 3.22. It has half duty cycle for chopping and another half for autozeroing. The circuit is an integrator without feedback. The output voltage is a triangle wave with a pause due to autozeroing. However, with feedback the chopped amplifier settles to the ripple [19]. The Miller capacitors store the ripple during autozeroing. Thus, the autozeroing essentially causes clock skew, which introduces residual offset. The clock skew of the Atlas clock is the autozeroing pulse length of 400 ns. The resulting skew is 2 percent, with the chopping frequency of 50 kHz, which is large for a chopper amplifier. A realistic native offset value for this amplifier is 2.5 mV as a 3-sigma value. The offset is reduced by approximately 350 times due to autozeroing. This reduces the resulting ripple. The ripple is assumed to be 7 µV. The residual offset of the autozeroed and chopped amplifier is therefore estimated as $400e-9 * 50e3 * 7e-6 = 1.4e-7V$ [15]. This value is a systematic error and should be avoided.

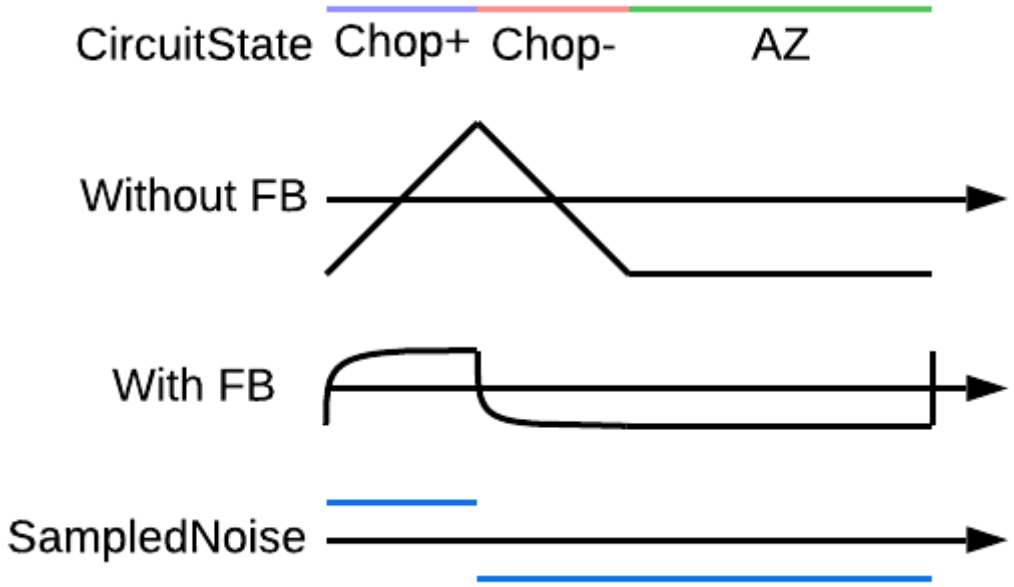


*Figure 3.22 Visualizing Inherent Offset*

As mentioned in Figure 3.21, the Atlas clock causes a noise increase by chopping the sampled noise unequally. To ease the description of the problem, an exaggerated clocking case where autozeroing has half the duty cycle of chopping is shown in Figure 3.23. Autozeroing samples the instantaneous noise (navy) on the autozeroing capacitors. This noise is random and varies in time. The sampling is then repeated (magenta) with the next autozeroing. This clock holds the sampled noise for different durations. There is unequal noise chopping as depicted with navy and magenta [27]. Therefore, the Atlas clock increases the noise floor and the noise peak at and around $fchop$. More clocks are generated and tried to mitigate the noise problem.

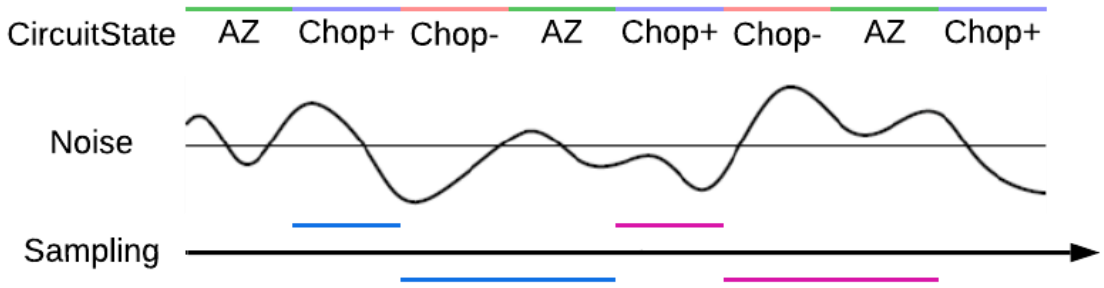


*Figure 3.23 Unequal Noise Chopping*

### 3.2.3. Clock Two - Themis

The inherent offset problem can be solved by autozeroing twice in one period. Then, one autozeroing phase and the offset due to its ripple is matched by another. However, this would result in worse noise as autozeroing again would sample another instantaneous value. Alternatively, the inherent offset problem can be solved by chopping and autozeroing in an alternating sequence. This clock is the Themis Clock. The second test clock is shown in Figure 3.24. It has duty cycles of 48 % chopping and 2 % autozeroing in an alternating sequence. The offset is not cancelled by chopping and autozeroing once. However, the alternating order

cancels the offset. The Themis clock's fundamental frequency is 50 kHz, but it is autozeroing at 100 kHz as it has two autozeroing pulses. This is good for noise folding as folded noise is spread over a wider bandwidth. It has more switching and therefore increased charge injection. This causes an increase of the residual offset. The autozeroing phase samples noise and holds it through the chopping phase. As shown in navy, dark orange, and dark green, the noise is chopped with a repeating pattern of 24 % and 26 % duty cycles. The Themis clock suffers from unequal noise chopping. This results in a noise increase.

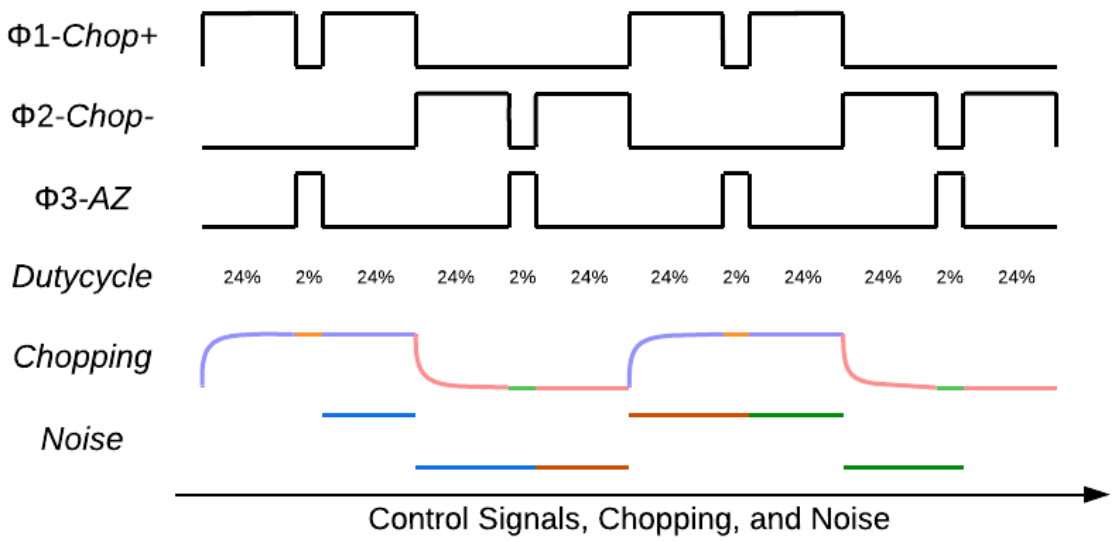


*Figure 3.24 Clock Two – Themis*

### 3.2.4. Additional Phase – Deadtime

Adding an extra deadtime phase is an idea to cancel out the offset and decrease the noise. The deadtime phase of the operational amplifier is implemented as shown in Figure 3.25. Deadtime is a brief transition state between the other phases. All switches are open. The signal path is broken. The deadtime phase extends the first chopping phase as the autozeroing phase extends the second chopping phase. Thus, both chopping phases are extended equally due to the sample and hold action of the Miller capacitors.

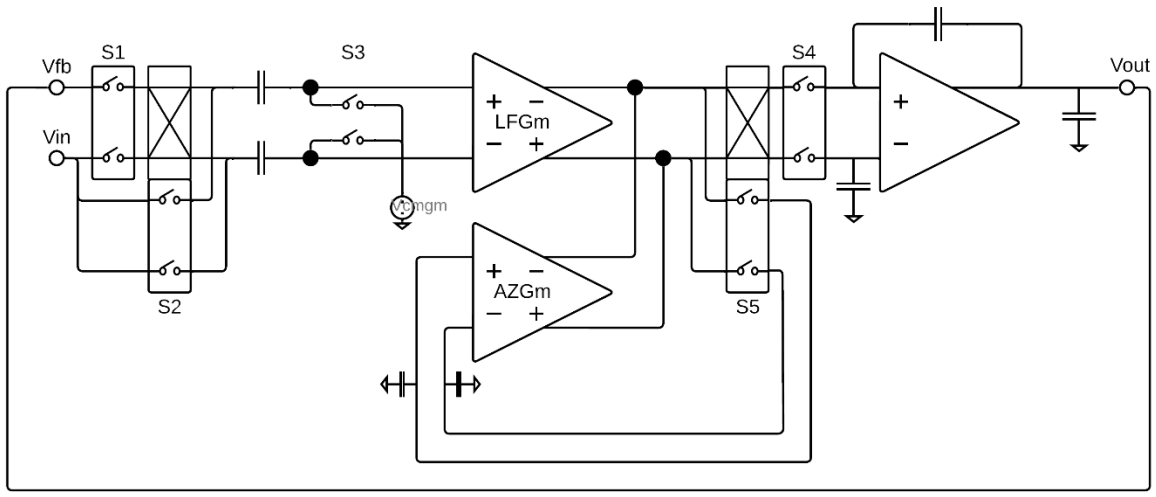


*Figure 3.25 Deadtime Phase*

### 3.2.5. Clock Three – Iapetus

The deadtime phase is used with the third test clock. This is the Iapetus Clock shown in Figure 3.26. It combines chopping with autozeroing and deadtime and then repeats with an alternating sequence. The duty cycles repeat as 23 %, 2 %, 23 %, and 2% and repeat once more. This clock solves the offset problem as autozeroing is matched with deadtime. Iapetus samples noise during autozeroing and then chops with two states of 25 % to 25 %. Iapetus then alternates its chopping sequence and completes one period. The Iapetus clock mitigates unequal noise chopping. However, it has additional deadtime noise. Opening switches samples further noise. Overall, it has increased noise compared to the Themis clock.

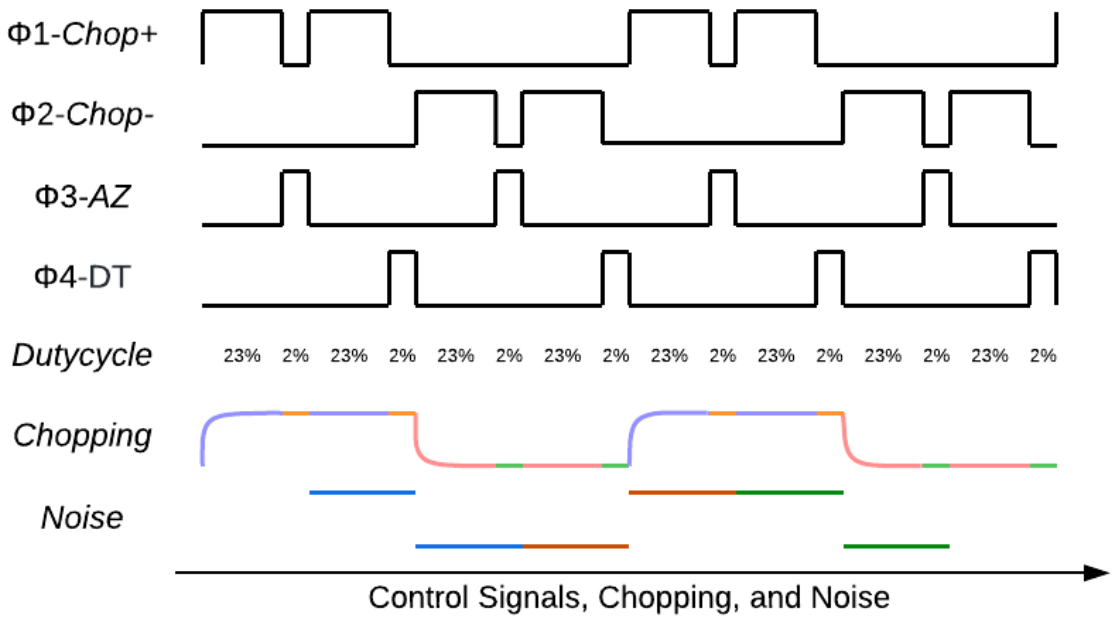


*Figure 3.26 Clock Three – Iapetus*

### 3.2.6. Clock Four – Rhea

The Rhea Clock is the fourth test clock. It is shown in Figure 3.27. This clock does not have a deadtime phase. It solves the offset problem by shifting autozeroing pulses within chopping phases. It has two 48 % duty cycles of chopping phases and two 2 % autozeroing pulses cut out from the chopping phases. It has an alternating order of chopping following the autozeroing pulse. Rhea clocks' fundamental frequency is 50 kHz, and its autozeroing frequency is 100 kHz. Like Themis's clock, folded noise is spread over a wider bandwidth, and more switching events have more charge injection. Autozeroing samples noise. This clock holds the sampled noise for equal durations of 25 % duty cycles. Therefore, the noise is chopped equally, and this clock has better noise than the Themis clock.

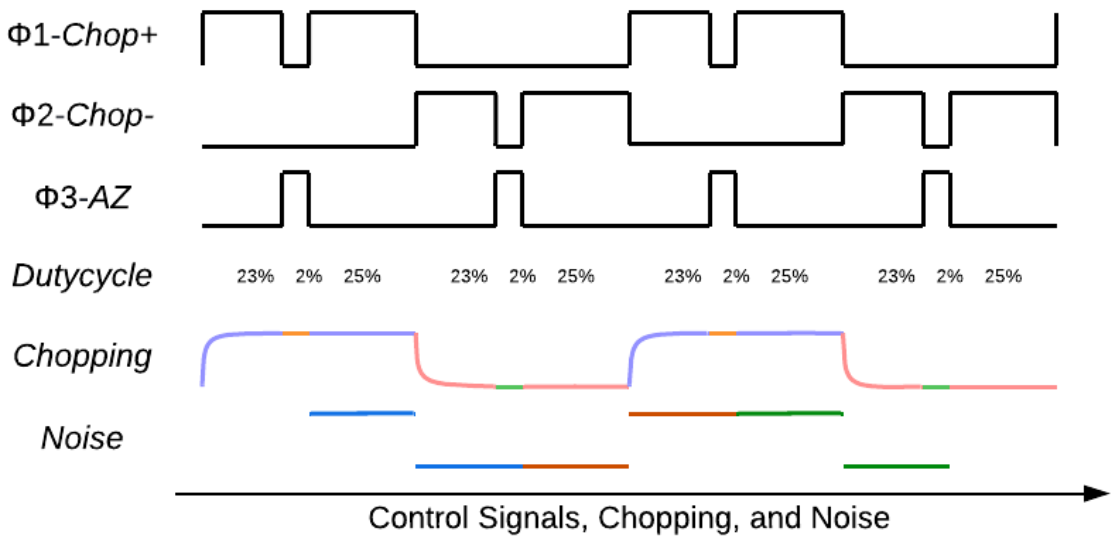


*Figure 3.27 Clock Four – Rhea*

### 3.2.7. Clock Five – Hyperion

The fifth and last test clock is the Hyperion Clock. It is shown in Figure 3.28. This clocking scheme uses findings from all previous clocks. It does not alternate the phase order of chopping as it solves the offset problem by shifting the autozeroing phase. It does not have equal duty cycles of chopping. It has pseudo 50 % chopping cycles where the shorter chopping phase and a 2 % autozeroing phase match the longer chopping phase. It has a fundamental frequency as well as an autozeroing frequency of 50 kHz. The folded noise is spread over a narrower bandwidth and increases the noise compared to Rhea Clock. At the same time, it has fewer switching events and less charge injection. Furthermore, shifting the autozeroing phase results in a decrease in noise. The Atlas clock, the starting point, has its noise chopped with duty cycles of 49 % to 51 %. Whereas, with Hyperion the noise is chopped equally. The amplifier has less noise with Hyperion clocking.

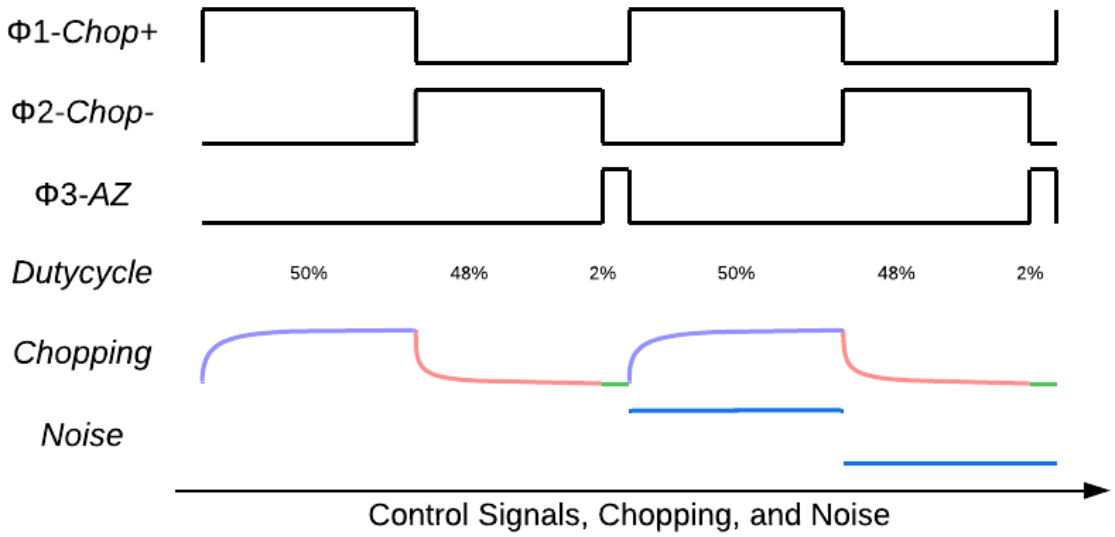


*Figure 3.28 Clock Five – Hyperion*

The amplifier is simulated as a buffer with a gain of one and an input voltage of 2.4 Volts. The amplifier is modeled with a 2-mV offset at its inputs. The periodic steady state analysis of Cadence is used to characterize the output voltage of the amplifier with the Hyperion clock. The output voltage is shown in Figure 3.29. The chopping phase and the autozeroing phase of the amplifier are distinguishable in the output waveform. The ripple of the amplifier separates the chopping phase. The chopping phase is split as 10 µs or 50 % duty cycle and 9.6 µs or 48 % duty cycle. The autozeroing phase of 400 ns or 2 % duty cycle mitigates the offset of the amplifier. The amplifier has pseudo 50 % chopping cycles where the shorter chopping and a 2 % autozeroing phase equal the longer chopping.

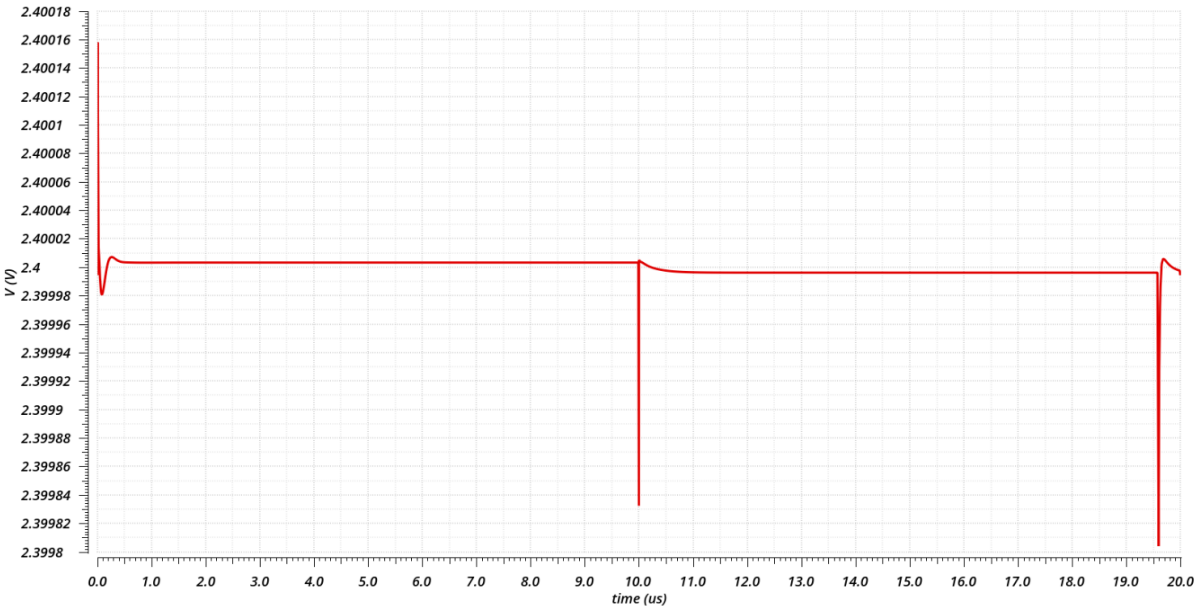


*Figure 3.29 Output Voltage of Amplifier with Hyperion Clock*

The noise analysis of Cadence is also used to characterize the output noise of the amplifier with Hyperion clock. The output noise is shown in Figure 3.30. Autozeroing folds noise down to low frequencies and creates a flat noise floor. Chopping up-modulates low frequency noise and causes the noise peak at the chopping frequency. Some low frequency flicker noise remains after chopping. The increase to the noise floor depends on the autozeroing bandwidth and chopping timing, and therefore depends on the clocking of the amplifier.

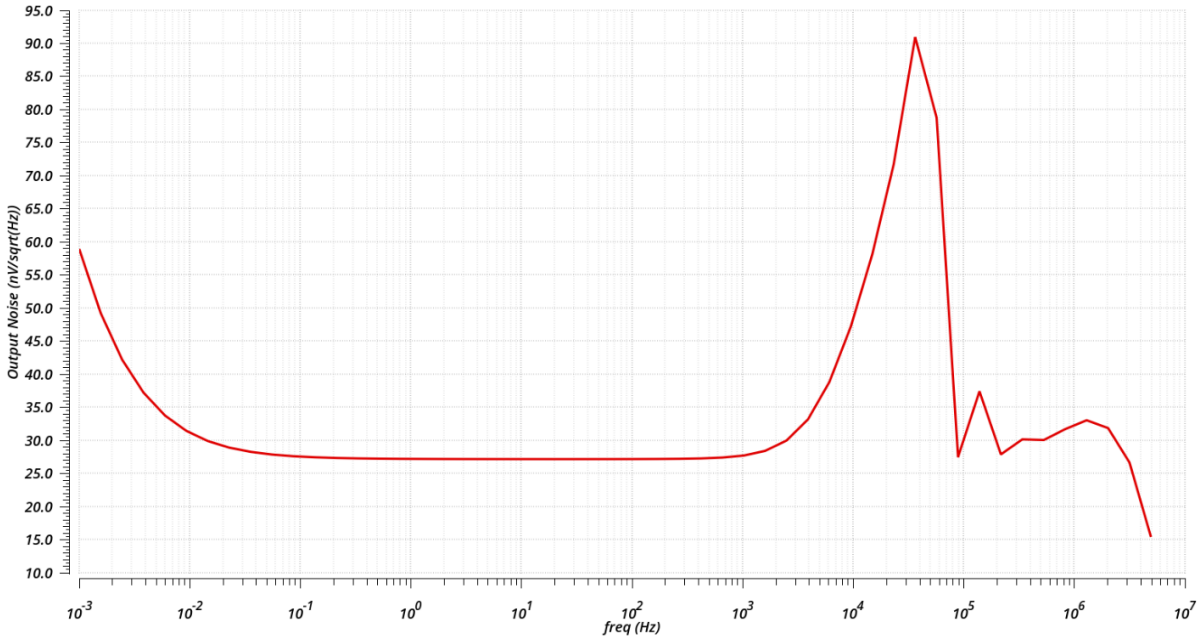


*Figure 3.30 Output Noise of Amplifier with Hyperion Clock*

## 3.3. Amplifier Analysis with Various Clocks

The performance of the amplifier design in Figure 3.1 is characterized and compared with all five clocks. The amplifier is a buffer. The test bench has an input voltage of 2.4 Volts. The amplifier has a 2-mV input offset modeled to the inputs of the first stage. The autozeroing phase reduces the offset of the amplifier. The chopping phase results in a ripple. The amplifier has an offset due to clock skew. The output voltage and noise of the amplifier differ with all five clocks: Atlas, Themis, Iapetus, Rhea, and Hyperion. The test bench uses the transistor implementations as described earlier in this chapter. The components are designed with the Taiwan Semiconductor Manufacturing Company (TSMC) process design kit (PDK).

Amplifier performance with all the various clocks is summarized in Table 3.4 for quantitative comparison of offset, ripple, and noise. Autozeroing is a control variable and the autozeroing phase is always the same duration. Therefore, the autozeroing accuracy and the resulting ripple variations are negligible. The Rhea and Hyperion clocks have lower noise than the Atlas, Themis, and Iapetus clocks. The Hyperion clock has the best offset, and the Themis and Rhea clocks also have low offset.

*Table 3.4 Offset, Ripple, and Noise of Amplifier with Various Clocks*

| Clocks | Atlas | Themis | Iapetus | Rhea | Hyperion |
|---|---|---|---|---|---|
| Offset (nV) | 70 | 50 | 250 | 50 | 10 |
| Ripple (µV) | 7.1 | 7.0 | 7.0 | 7.0 | 7.1 |
| Noise (nV/√Hz) | 27.8 | 27.8 | 29.6 | 27.2 | 27.4 |

The effect of clocking on noise is analyzed in detail in Table 3.5. The noise of the amplifier without any clocking is simulated. This noise is a DC simulation that includes the switches and the thermal noise of the switches. The amplifier is characterized in its one signal path. The amplifier has a thermal noise floor of 26.0 nV/√Hz. The noise of the amplifier without any of the switches is also calculated. It does not include any chopping or autozeroing switch transistors and does not have their associated noise. The noise is 23.5 nV/√Hz. The thermal noise of the switches represents a noise increase of 11 % for the amplifier design.

Noise with clocking is the noise of the amplifier with chopping and autozeroing phases. The reported switching noise is the low-frequency flat noise floor of the amplifier. The switching noises of all five clocks are different. Hyperion and Rhea Clocks have lower noise than other clocks. Rhea Clock is autozeroing at 100 kHz whereas Hyperion Clock is autozeroing at 50 kHz. Rhea clock folds noise down to a wider bandwidth than Hyperion Clock. Rhea Clock achieves a noise level of 27.2 nV/√Hz in comparison to 27.4 nV/√Hz achieved by Hyperion Clock. The Rhea and Hyperion clocks both achieve a noise increase of only 5 %, which is low.

*Table 3.5 Detailed Noise Analysis and Comparison*

| Clocks | Atlas | Themis | Iapetus | Rhea | Hyperion |
|---|---|---|---|---|---|
| Noise without Clocking (nV/√Hz) | 26.0 | 26.0 | 26.0 | 26.0 | 26.0 |
| Noise with Clocking (nV/√Hz) | 27.8 | 27.8 | 29.6 | 27.2 | 27.4 |
| Noise Increase with Clocking | +7 % | +7 % | +14 % | +5 % | +5 % |

Rhea and Hyperion Clocks are studied further in Table 3.6. The two are characterized by their chopping and autozeroing frequency, count of glitches due to clock scheme, charge injection of these transient glitches, clock skew caused residual offset without circuit mismatch, phase margin, gain margin, UGB, DC Gain, noise, and ripple. From the results, Hyperion Clock is chosen as it has lower transition count and, therefore, lower charge injection. It has the best offset, UGB, and DC gain. Its noise and ripple are comparable.

*Table 3.6 Detailed Comparison of Rhea and Hyperion Clocks*

| Clocks | Rhea | Hyperion |
|---|---|---|
| Chopping Freq (kHz) | 50 | 50 |
| Autozeroing Freq (kHz) | 100 | 50 |
| Glitch (µV) | 360 | 360 |
| Glitch Count | 6 | 3 |
| Offset (nV) | 45 | 10 |
| Phase M (°) | 66 | 65 |
| Gain M (dB) | 13.7 | 13.5 |
| UGB (MHz) | 1.81 | 1.88 |
| DC Gain (dB) | 173 | 182 |
| Noise (nV/√Hz) | 27.22 | 27.36 |
| Ripple (µV) | 6.96 | 7.08 |

# 4. Results

The operational amplifier shown in Figure 4.1 is simulated as a buffer and as an amplifier with gain and negative feedback. The amplifier's performance parameters are characterized. The power consumption is 256 µA at 5 V. The total capacitance is approximately 90 pF.

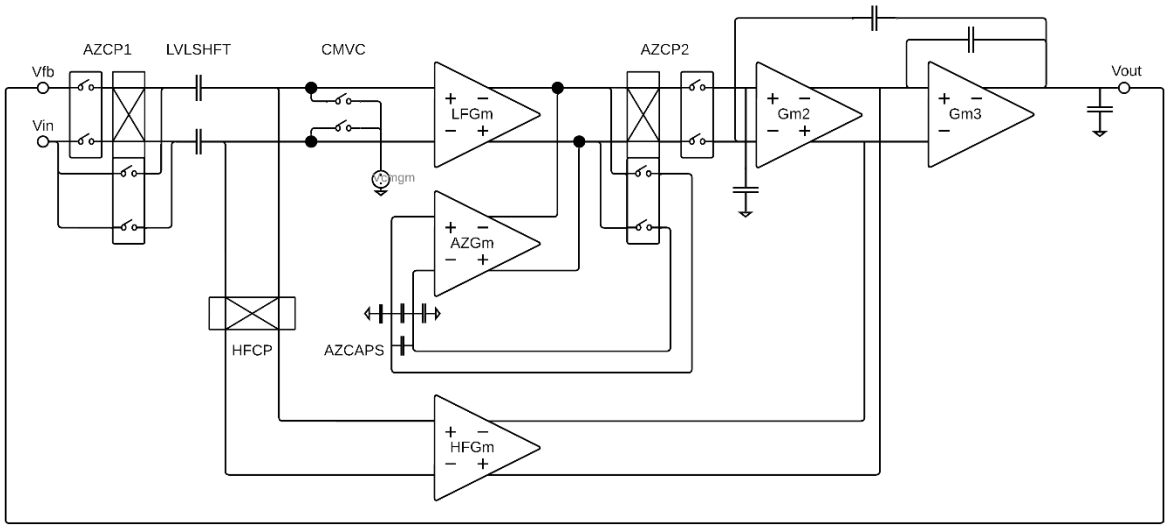


*Figure 4.1 Circuit of the Operational Amplifier in Buffer Configuration*

## 4.1. Amplifier Output Voltage

The operational amplifier employs a pseudo-continuous time architecture. It has a single signal path which is chopped and autozeroed. Hyperion clock controls the switching of its chopping and autozeroing phases. The phases of the amplifier and the settling of the amplifier in these phases are analyzed using the periodically steady state (PSS) analysis of Cadence. The amplifier is put in a buffer configuration with a 2-mV offset at its inputs and an input voltage of 2.4 V. It is simulated with five process variations and four temperatures generating twenty corner cases. The results estimate the performance spread. The amplifier output voltage in all twenty corners is shown in Figure 4.2. The two voltage levels recognized in the outputs are due to chopping. The short pulse is the autozeroing. The output has glitches. The output voltage is 2.4 V in all cases. Ripple variations resulting from the 2-mV native offset are minor. The nominal ripple is 7 µV, the minimum ripple is 3.2 µV, and the maximum ripple is 11.3 µV.

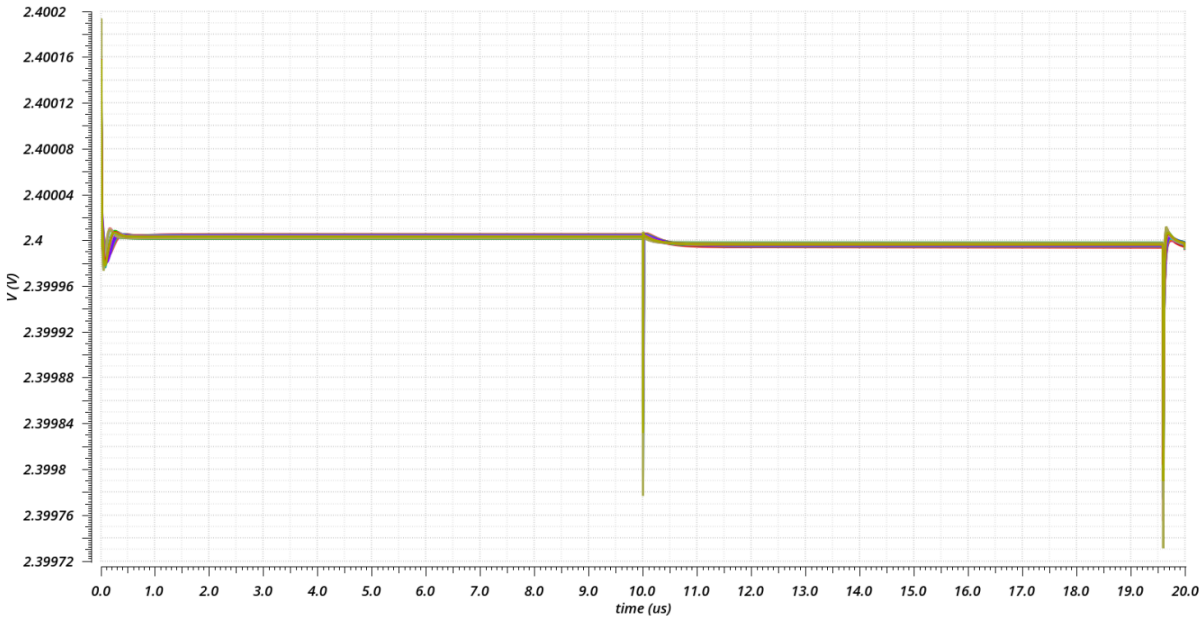


*Figure 4.2 Amplifier Output Voltage Spread with Temperature and Process*

## 4.2. Amplifier Output Noise

The amplifier output noise in twenty corners is shown in Figure 4.3. Autozeroing folds noise down to low frequencies, then chopping up-modulates noise at and around the chopping frequency. There is residual $1/f$ noise at very low frequencies with a noise corner around 10 mHz. The high-frequency noise of the amplifier is a combination of the low-frequency and high-frequency paths as there is a crossover between the two paths. A lower cross-over frequency achieved with a 4-stage amplifier would provide lower noise at high frequencies. The up-modulated noise peak is at the chopping frequency of 50 kHz. All simulations result in a noise floor of less than 50 nV/√Hz. The output noise averages a value of ~30 nV/√Hz across all cases. Noise variations are minor. The nominal noise floor level is simulated as 27.36 nV/√Hz. The minimum output noise floor for the low frequencies is 21.2 nV/√Hz, and the maximum is 39.3 nV/√Hz. The noise breakdown using Hyperion Clock is simulated. The differential pair of the first stage (LF input OTA) is the main noise contributor. Other considerable noise contributors are the PMOS current sources of the first stage, the autozeroing differential pair of the auxiliary amplifier, main NMOS current sinks of the first stage, the common-mode feedback NMOS current sinks of the first stage, and the chopping switches in that order.

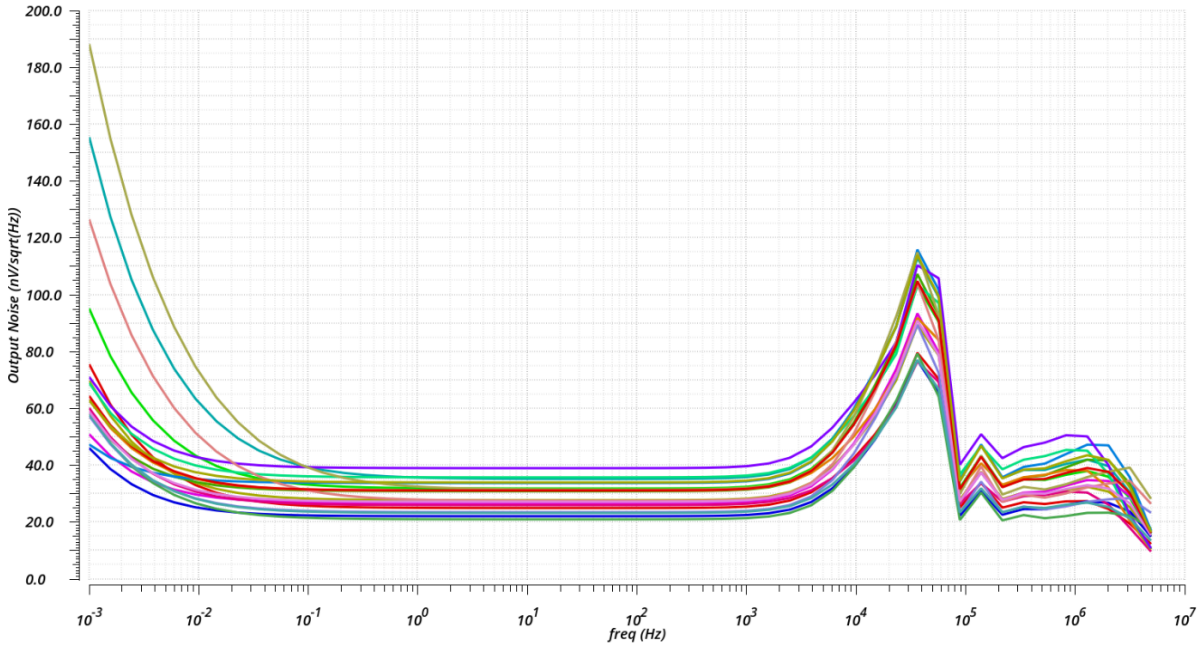


*Figure 4.3 Amplifier Output Noise Spread with Temperature and Process*

## 4.3. Amplifier Gain and Phase

The amplifier gain and phase in twenty corners are shown in Figure 4.4 and Figure 4.5 respectively. The crossover frequency between the high-frequency and low-frequency paths is visible and around 100 kHz. The fundamental chopping and autozeroing artifacts at 50 kHz are not suppressed, and higher-order harmonics are suppressed. The nominal amplifier has a DC gain of 182 dB, a gain margin of 14 dB, and a UGB of 1.86 MHz. There are significant variations to gain. The average DC gain is 180 dB, the maximum is 199 dB, and the minimum is 137 dB. The minimum gain is an important constraint. The minimum fails to meet the design target. This is because operational amplifier performance deteriorates at cold temperatures due to operating point changes. The phase is shown starting from 1 Hz and up. Phase Margin variations are small, with an average phase margin of approximately 65°. The nominal phase margin is 67°, the maximum is 70,4°, and the minimum is 59,0°. This is a good result as a worst-case phase margin of 60° was targeted.

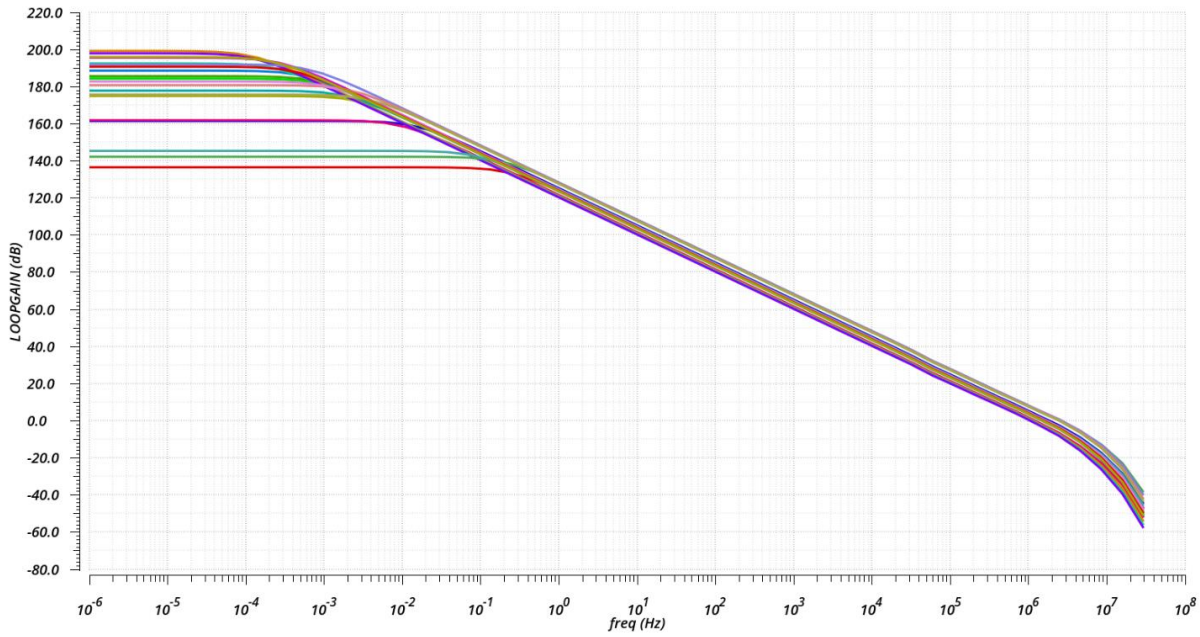


*Figure 4.4 Amplifier Gain Spread with Temperature and Process*

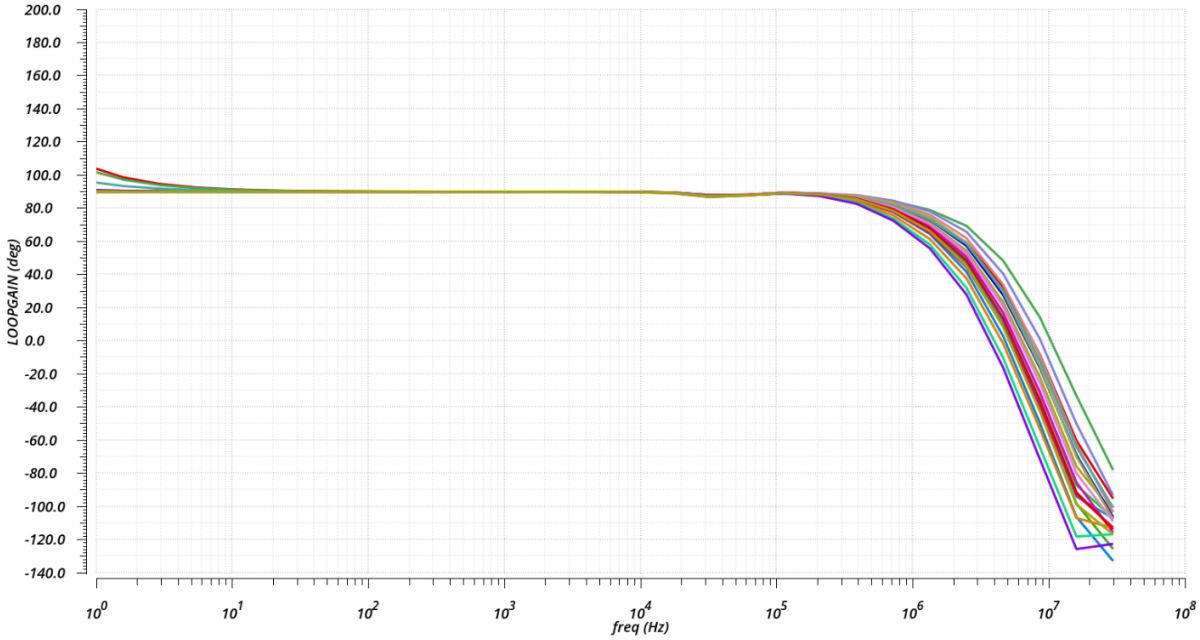


*Figure 4.5 Amplifier Phase Spread with Temperature and Process*

The slewing of the amplifier in response to a 0.5 V voltage step at its input is shown in Figure 4.6. The slew rate varies depending on the temperature and whether the process corner is fast or slow. The average slew rate is approximately 0.5 V/µs, the same as the nominal case. Faster corners have faster slewing, and hotter conditions also have faster slewing. Therefore, the quickest case is the fast corner (FF) with the hot temperature (125˚C) slewing at 0.820 V/µs, and the slowest is the slow corner (SS) with cold temperature (-40˚C) slewing at 0.380 V/µs.

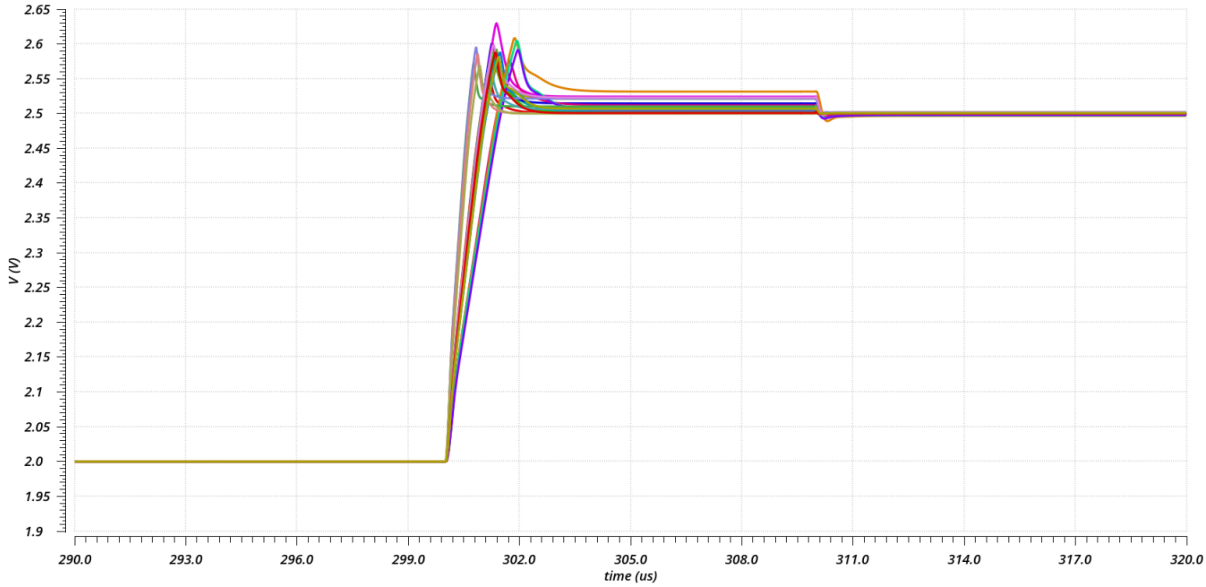


*Figure 4.6 Amplifier Output Slew Spread with Temperature and Process*

## 4.4. Amplifier Performance Spread Summary

The operational amplifier is characterized across five process variation corners and four temperatures and cross-tested across their combinations in twenty cases. The results with the process variations of the nominal (TT), fast corner (FF), slow-fast corner (SF), fast-slow corner (FS), and slow corner (SS) at room temperature are summarized in Table 4.1. The variations are within reasonable limits.

*Table 4.1 Amplifier Performance with Process Variations at 27˚C*

| Process | TT | FF | SF | FS | SS |
|---|---|---|---|---|---|
| Fundamental Freq (kHz) | 50 | 50 | 50 | 50 | 50 |
| Glitch (µV) | 360 | 440 | 340 | 370 | 290 |
| Offset (nV) | 10 | 10 | 10 | 10 | 20 |
| Phase M (°) | 65 | 63 | 63 | 66 | 65 |
| Gain M (dB) | 13 | 13 | 12 | 14 | 14 |
| UGB (MHz) | 1.8 | 2.8 | 1.9 | 1.8 | 1.2 |
| DC Gain (dB) | 182 | 192 | 195 | 175 | 199 |
| Noise (nV/√Hz) | 27.4 | 23.9 | 27 | 28 | 31.4 |
| Ripple (µV) | 7.1 | 4.7 | 6.4 | 7.9 | 9.9 |
| Slew Rate (V/µs) | 0.45 | 0.73 | 0.44 | 0.47 | 0.32 |

The amplifier is tested at varying operating temperatures. These are cold temperature (-40˚C), room temperature (27˚C), heated temperature (85˚C), and hot temperature (125˚C). The results with the nominal (TT) and all four temperatures are summarized in Table 4.2. Most variations are within reasonable limits except for the cold temperature DC gain. The threshold voltages increase with decreasing temperature. The operating points change, and the overhead voltages of transistors decrease. Thus, not all transistors are in saturation. The DC gain decreases.

*Table 4.2 Amplifier Performance with Temperature Variations*

| Temperature (˚C) | -40 | 27 | 85 | 125 |
|---|---|---|---|---|
| Fundamental Freq (kHz) | 50 | 50 | 50 | 50 |
| Glitch (µV) | 370 | 360 | 350 | 340 |
| Offset (nV) | 10 | 10 | 10 | 10 |
| Phase M (º) | 68 | 65 | 63 | 62 |
| Gain M (dB) | 15 | 13 | 12 | 12 |
| UGB (MHz) | 1.9 | 1.8 | 1.7 | 1.7 |
| DC Gain (dB) | 145 | 182 | 190 | 196 |
| Noise (nV/√Hz) | 23.5 | 27.4 | 31.5 | 34.3 |
| Ripple (µV) | 6.9 | 7.1 | 7.7 | 7.8 |
| Slew Rate (V/µs) | 0.43 | 0.45 | 0.47 | 0.49 |

## 4.5. Amplifier Step Response

The operational amplifier is simulated as a buffer. The amplifier is modeled with a 2-mV offset at the inputs of the first stage. The amplifier's step response with various differential input voltage steps of 10 mV, 1 V, 4.6 V, and rail-to-rail are tested. First, the input is connected to 2 Volts and a 10-mV step is excited at the input of the amplifier. The step response is shown in Figure 4.7. The amplifier settles within 10 µs, and the chopping ripple is approximately 5 µV. This means autozeroing reduces offset by a factor of four hundred.

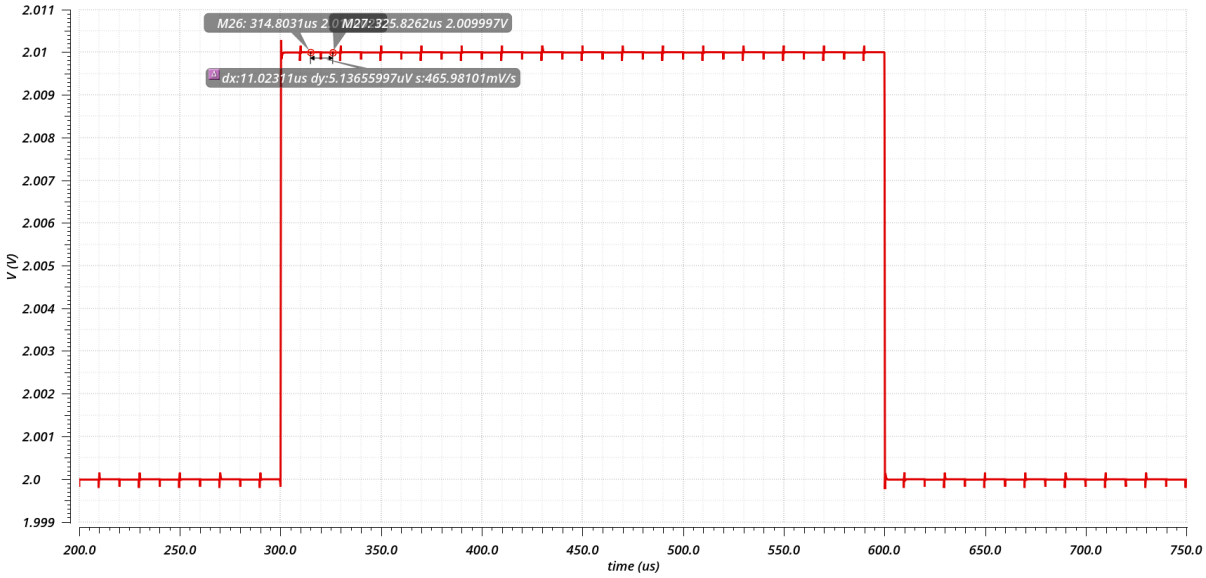


*Figure 4.7 Amplifiers Output Voltage with 10 mV Step*

Next, the amplifier is simulated with a larger 1 V input step from an input voltage of 0.5 Volt to 1.5 Volts. The step response is shown in Figure 4.8. The amplifier slews with a speed of 470 kV/s or 0.47 V/µs. The slewing has a stepping behavior as the protection diodes limit the single-step size to roughly one diode voltage. The ripple reduces quickly within a few clock cycles but fully settles in approximately 200 µs to 4 µV.

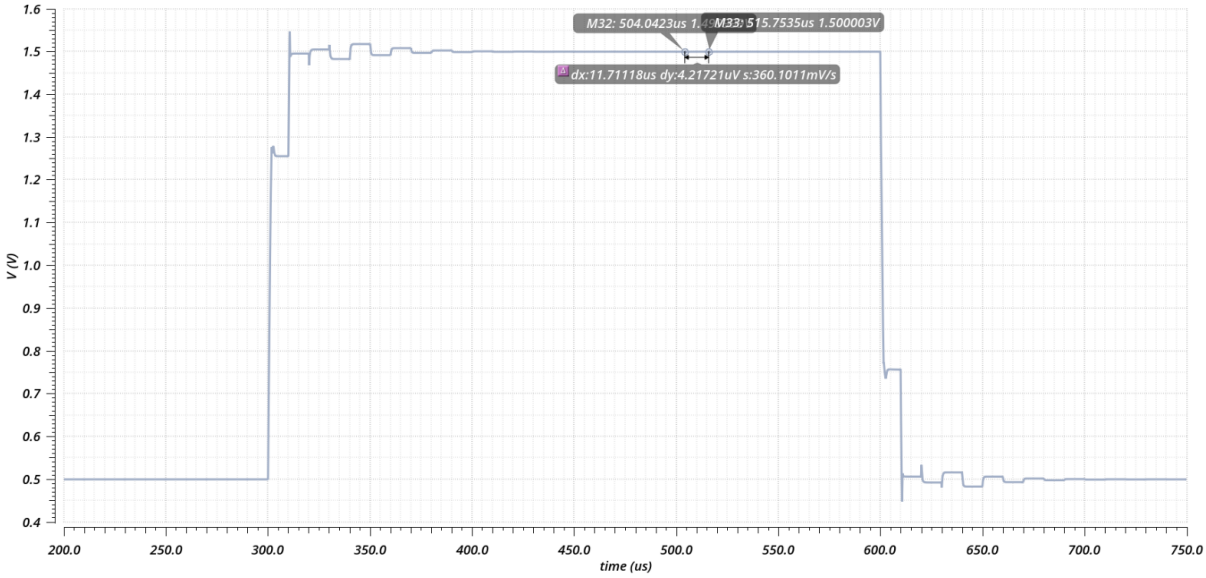


*Figure 4.8 Amplifiers Output Voltage with 1 V Step*

Afterward, the amplifier is simulated with a 4.6 V step. The input voltages are stepped from almost GND (200 mV) to almost VDD (4.8 V). The step response is shown in Figure 4.9. The diode protections of the floating chopper are shorted. The amplifier is not meant to be used with steps larger than one diode voltage. This simulation demonstrates the class-AB output stage's almost rail-to-rail functionality. The ripple gets small quickly within a few clock cycles. The ripple settles in approximately 250 µs to 8 µV.

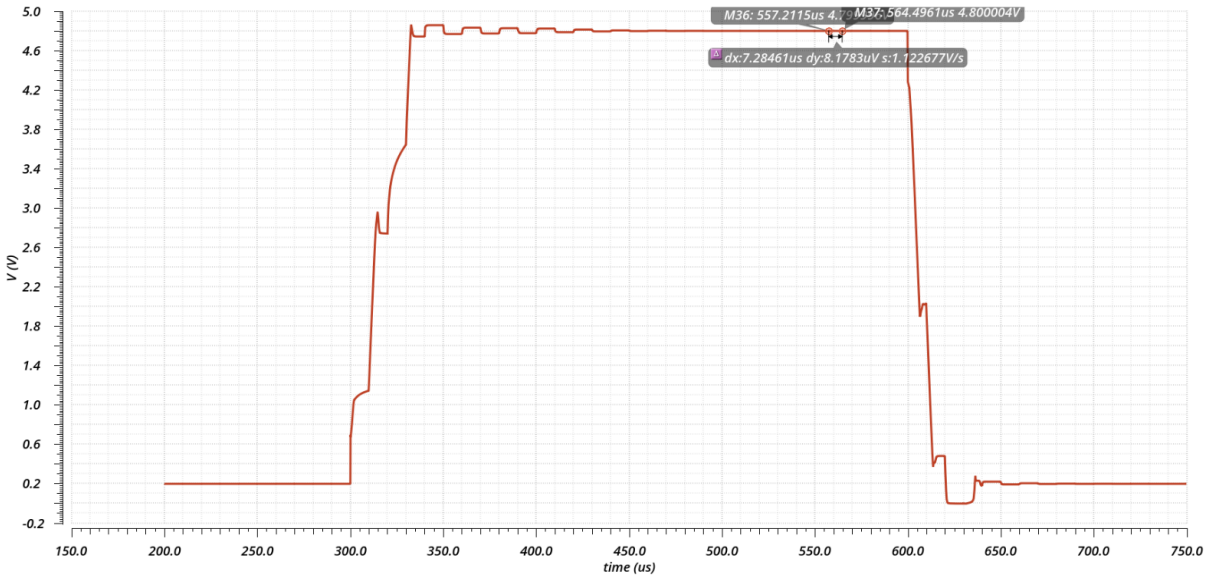


*Figure 4.9 Amplifiers Output Voltage with 4.6 V Step*

Last, the amplifier input is driven into the rails of 0 V and 5 V to see the behavior of the protection circuitry and the output stage. The amplifier output voltage is shown in Figure 4.10. It shows that the amplifier inputs and outputs can reach the supply voltages. There are no overvoltage conditions and no physical failures. The amplifier can go to the supply rails, but it is not an amplifier at these voltages. This is due to the class-AB output stage.

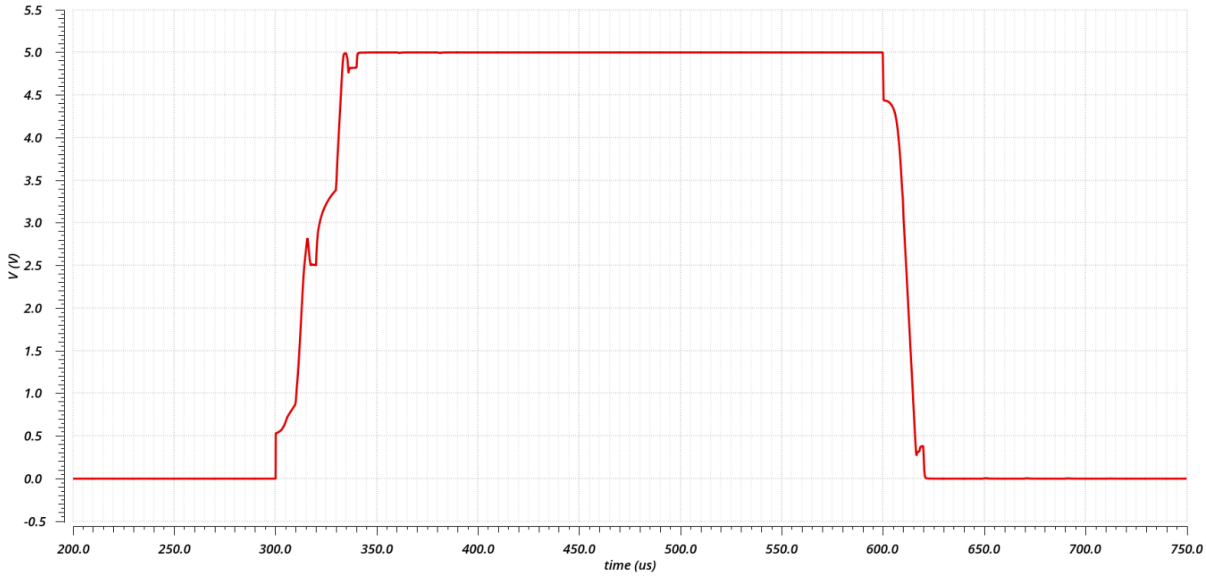


*Figure 4.10 Amplifier Output Voltage if the Input is Driven into the Supply Rails*

## 4.6. Amplifier with Sine Wave Input and Chopper Induced IMD

The amplifier is put in a buffer configuration with a 2-mV offset at its inputs and an input voltage of 2.4 V. The amplifier is simulated with a sine wave with a frequency of 2 kHz. The sine wave amplitude is kept small at 100 mV as larger amplitudes have limitations with passing through the coupling capacitors and the input common-mode refresh. Chopping and autozeroing frequencies are 50 kHz, making the sine wave frequency much smaller than both.

As shown in Figure 4.11, this results in only minor disturbances to the amplifier output waveform as the amplifier is much faster.

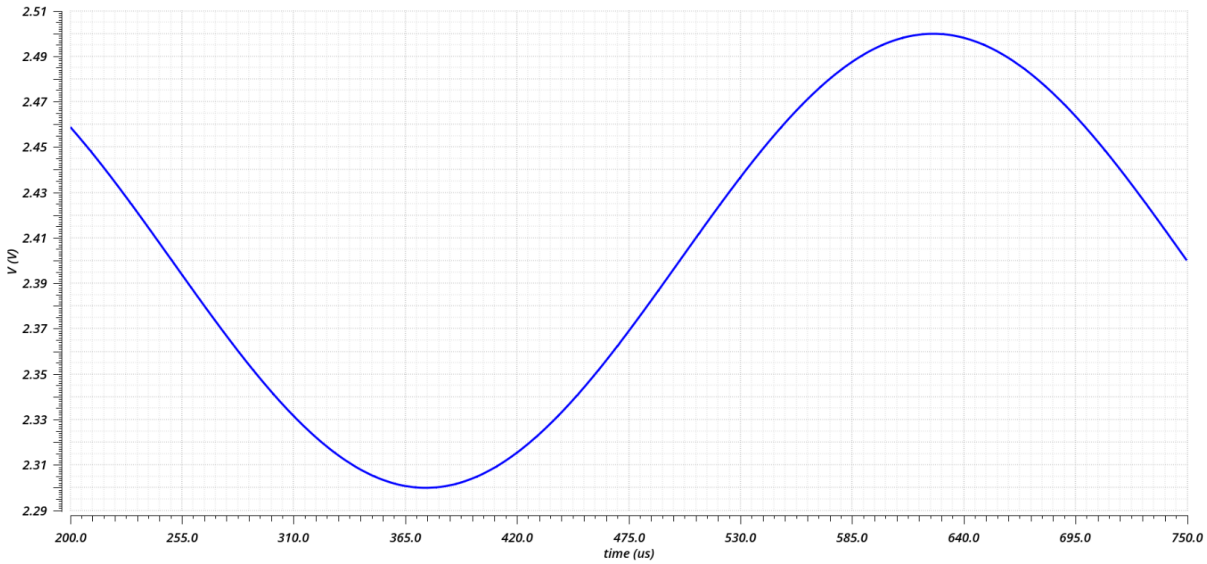


*Figure 4.11 Amplifier Output with 100 mV 2 kHz Sine Wave Input*

Chopper amplifiers suffer from chopper-induced intermodulation distortion (IMD). Typically, IMD is measured with two separate input signals, but with chopper amplifiers, one of the signals can be treated as the chopping clock signal running at the chopping frequency. The chopper-induced IMD is due to the limited bandwidth of the amplifier and the resulting signal delay within the up-modulation and de-modulation choppers. The chopper-induced IMD of the amplifier is simulated for a 100 mV 2 kHz sine wave input as shown in Figure 4.12. The signal at 2 kHz and chopping at 50 kHz results in a 4 µV tone at 48 kHz. The ratio of the input signal to the tone is approximately 25000 or 88 dB.

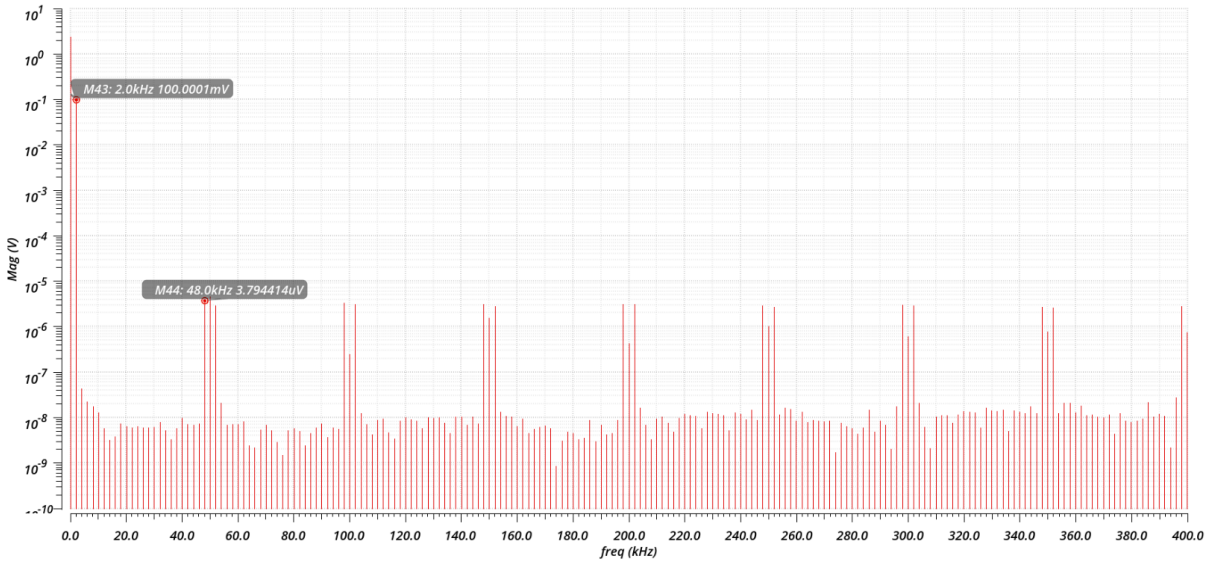


*Figure 4.12 Chopper-Induced IMD of Amplifier with 100 mV 2 kHz Sine Wave Input Signal*

The chopper-induced IMD of the amplifier is simulated for a 100 mV 48 kHz sine wave input as shown in Figure 4.13. The signal at 48 kHz and chopping at 50 kHz results in a tone at 2 kHz.

The tone has a magnitude of 176 µV. This is a much smaller ratio of 570 or 55 dB. The chopper-induced IMD worsens with an input signal frequency closer to the chopping frequency.

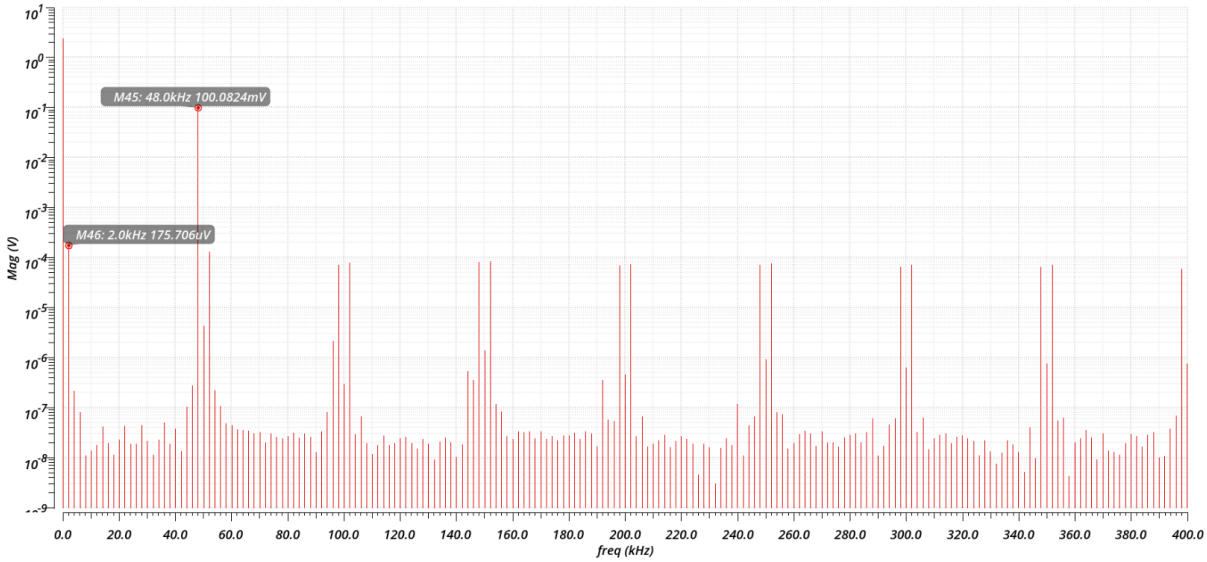


*Figure 4.13 Chopper-Induced IMD of Amplifier with 100 mV 48 kHz Sine Wave Input Signal*

## 4.7. Power Supply Rejection Ratio (PSRR)

The amplifier's PSRR is simulated by injecting an AC signal through the positive supply. In the nominal case, the resulting disturbance to the output is approximately 1 nV. This means 180 dB PSRR for the nominal without mismatch. Mismatch decreases the PSRR of the circuit. One hundred Monte-Carlo simulations are run to characterize the PSRR further. The mean PSRR is 149 dB. The minimum is 136 dB. A worst-case PSRR of 136 dB is within desired specifications.

## 4.8. Common-Mode Rejection Ratio (CMRR)

The amplifier's CMRR is simulated similarly by injecting an AC signal. This is a common-mode signal injected through both inputs of the amplifier. In the nominal case, the result on the output is approximately 1 nV. This is 180 dB CMRR in the nominal case. One hundred Monte-Carlo simulations are run to characterize the CMRR further, and the mismatch decreases the CMRR. The mean CMRR is also 180 dB. This is a minimum CMRR of 176 dB. This amplifier has high CMRR.

## 4.9. Mismatch

Like most processes, the TSMC high-voltage BCD 0.18 µm 5 V technology has minor fabrication deviations or mismatches between components. The mismatch and the slightly different parameters of the amplifier in Figure 4.1 is modeled and simulated using Monte Carlo experiments. First, the amplifier is simulated DC. It does not switch between chopping and autozeroing phases. It is modeled with three hundred randomly generated Monte-Carlo variants different from one another. The amplifiers' parameters such as phase margin, gain margin, UGB, DC gain, offset without chopping, and noise are summarized in Table 4.3. The minimum phase margin is 53˚, the minimum gain margin is 10 dB, the minimum UGB is 2 MHz, the minimum DC gain is 192 dB, and the maximum noise is 27 nV/√Hz. The mean offset is close to zero, and the offset standard deviation is 844 µV. The three-sigma offset varies from negative 2.5 mV to positive 2.5 mV.

*Table 4.3 Amplifiers' Signal Path Parameters with Mismatch*

| Spec | Min | Max | Mean | Std Dev |
|---|---|---|---|---|
| Phase M (º) | 52,9 | 61,7 | 57,7 | 1,5 |
| Gain M (dB) | 10,6 | 13,4 | 12,1 | 0,5 |
| UGB (Hz) | 2,03 M | 2,16 M | 2,09 M | 23 k |
| DC Gain (dB) | 192,8 | 197,8 | 195,4 | 0,8 |
| Offset w/o Chopping (V) | -2,3 m | 2,0 m | -20 µ | 844 µ |
| Noise (V/√Hz) | 25,6 n | 26,8 n | 26,2 n | 0,19 n |

Next, the amplifier is simulated periodically steady state. Hyperion clock is used for chopping and autozeroing the amplifier. The amplifier is simulated with three hundred randomly generated new Monte-Carlo runs. The amplifier's phase margin, gain margin, UGB, DC Gain, residual offset, glitches, noise, and ripple are investigated. The results are shown in Table 4.4. The minimum phase margin is 62˚, minimum gain margin is 12 dB, minimum UGB is 1.8 MHz, and minimum DC gain is 173 dB. The residual offset standard deviation is 560 nV. The glitches are approximately 350 µV. The maximum noise is 28 nV/√Hz. The ripple standard deviation is 3,3 µV. The minimum absolute value of ripple is 3 nV. Residual offset, ripple, and the absolute value of ripple are analyzed further.

*Table 4.4 Switching Circuit Monte Carlo Summary*

| Spec | Min | Max | Mean | Std Dev |
|---|---|---|---|---|
| Phase M (º) | 62,1 | 68,1 | 65,1 | 1,1 |
| Gain M (dB) | 12,4 | 14,9 | 13,5 | 0,5 |
| UGB (Hz) | 1,79 M | 1,95 M | 1,88 M | 29 k |
| DC Gain (dB) | 173,0 | 233,6 | 184,1 | 7,1 |
| Residual Offset (V) | -1,8 µ | 1,5 µ | 25 n | 557 n |
| Glitches (V) | 350 µ | 361 µ | 355 µ | 2 µ |
| Noise (V/√Hz) | 26,7 n | 28,1 n | 27,4 n | 0,21 n |
| Ripple (V) | 3 n | 12 µ | 2,6 µ | 2 µ |

The residual offset is centered around zero. This is as expected from a chopper amplifier. The standard deviation of the residual offset is 557 nV. The residual offset of this amplifier is in the µV scale, and the three-sigma residual offset varies from negative ~1.7 µV to positive ~1.7 µV.

The difference between the amplifier output voltages with chopping phases is expressed as a negative or positive value depending on the sequence in which the amplifier integrates to the higher or lower voltage. Ripple is a scalar quantity and does not have polarity. The absolute value of the difference is ripple. The amplifier has a low ripple.

## 4.10. Gain Amplifier

The operational amplifier with gain and negative feedback is simulated. This is an inverting amplifier as shown in Figure 4.14 where the feedback sets the gain as $-R2/R1$. The amplifier is simulated with gains of one and hundred.

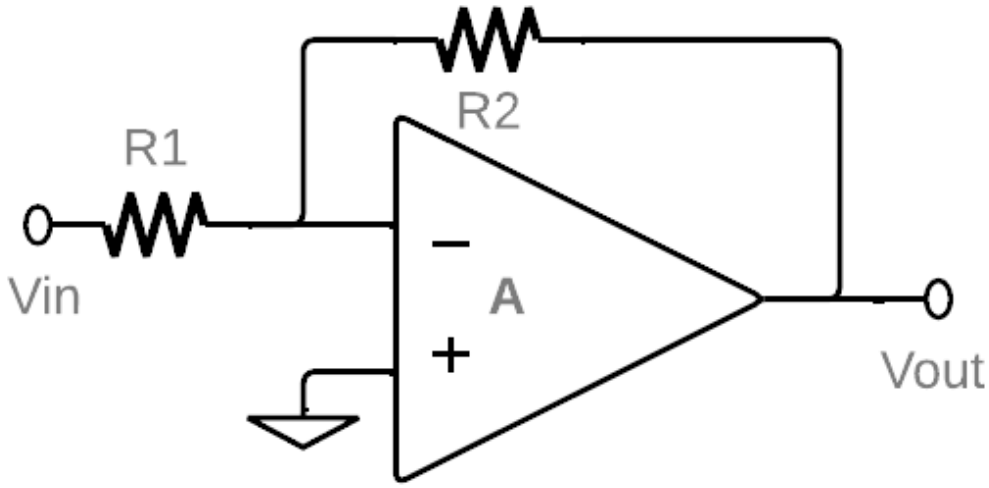


*Figure 4.14 Op-Amp with Gain and Negative Feedback*

First, the amplifier has a gain of -1. The common-mode is set to 2.4 V, and the input signal is 1 mV. The input signal has a magnitude smaller than the offset of the amplifier without chopping. The output is shown in Figure 4.15. The amplifier's output voltage is 2.399 V. The offset is 2.1 µV, and the ripple is 14 µV.

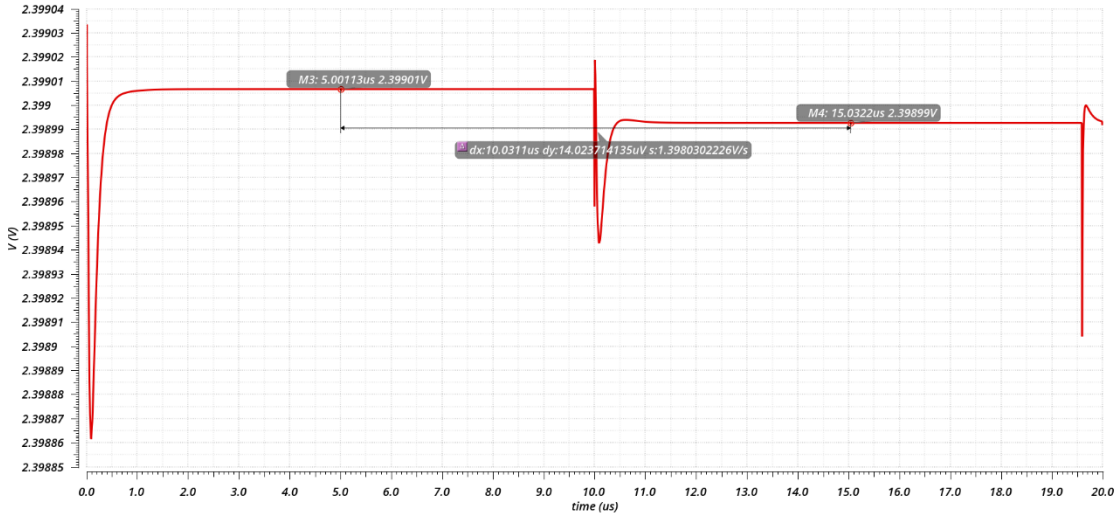


*Figure 4.15 Amplifier Output with Gain of -1*

Next, the amplifier's gain is set to -100. The common-mode is kept at 2.4 V, and the input signal remains 1 mV. The amplifier output is shown in Figure 4.16. The amplifier's output voltage is 2.3 V. The offset at the amplifier output is 190 µV, and the ripple is approximately 500 µV. Both amplifier output voltage offset, and ripple are larger due to the increased gain. The input-referred offset is smaller and is 1.9 µV. Thus, the operational amplifier's correct operation is demonstrated with high gain and negative feedback.

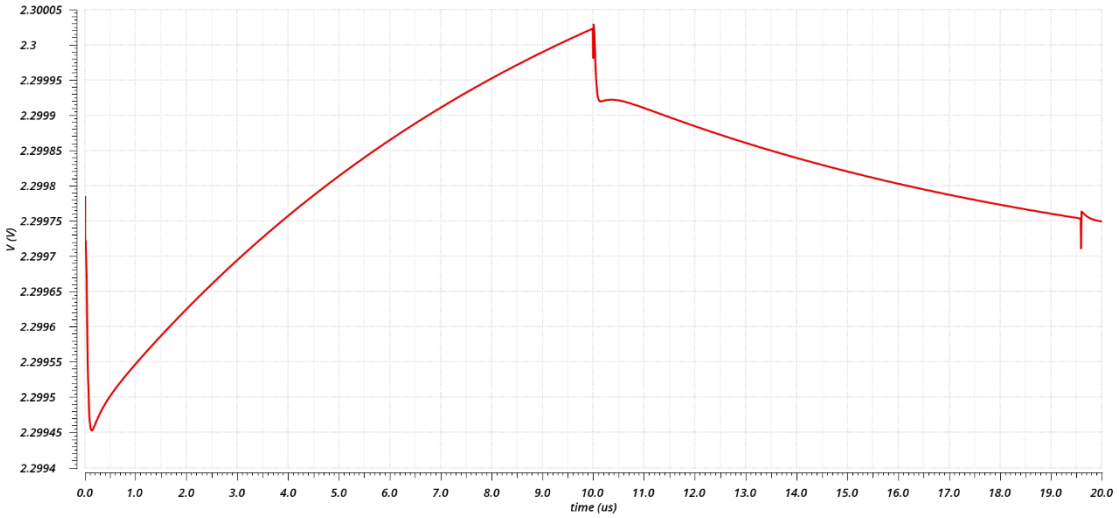


*Figure 4.16 Amplifier Output with Gain of -100*

# 5. Conclusions and Future Work

## 5.1. Conclusions

This thesis presents the design and simulation of a capacitively-coupled autozeroed and chopped operational amplifier in the TSMC high voltage BCD 0.18 µm 5 V technology. The operational amplifier achieves high precision (10 µV offset and 50 nV/√Hz noise density) and safely handles beyond-the-rail (50 V) input voltages. The notch in the frequency spectrum is eliminated with the input common-mode refresh. The floating capacitively coupled chopper is expanded to include autozeroing functionality. The Hyperion Clock improves amplifier performance and lowers amplifier noise. In simulation, the Hyperion clock halves charge injection compared to the Themis clock and improves noise by as much as 9 % compared to the Iapetus clock.

## 5.2. Future Work

In the following section, several changes to the current design are proposed. These changes expand upon the ideas, modify the current reported design, and continue the investigation.

### 5.2.1. A Secondary Digital Block

There is only one digital block in the design. This runs from a supply of 2.4 Volts. The autozeroing switches and de-modulating chopper (AZCP2), the high-frequency multi-path chopper so called cross-modulating chopper (HFCP), and the input common-mode voltage clamp for setting the common-mode voltage at the inputs of the first stage (CMVC) are complicated because of this digital block limitation. The next step can be replicating the digital and running the secondary digital block with a 5 V supply. Alternatively, level shifters can be added to level shift from the low-voltage digital domain to the higher-voltage analog domain. These can generate an extra clock scheme, as shown in Figure 5.1. This additional clock can then control some of the switching blocks.

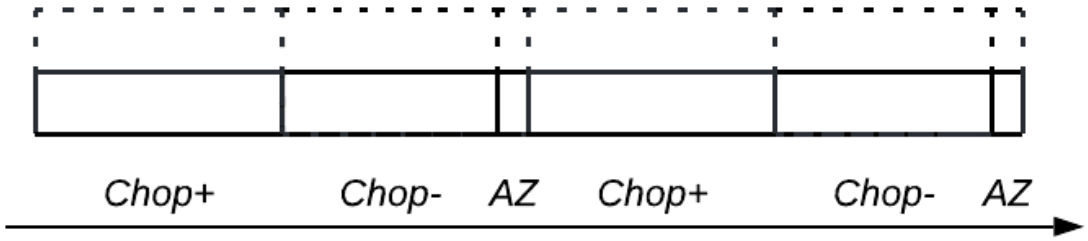


*Figure 5.1 Analog Domain and Digital Domain Clocks*

### 5.2.2. Voltage Reference

The design of the voltage reference is omitted in this thesis. The next steps can include the design of an on-chip voltage reference.

### 5.2.3. Input Stage

The input stage implementation used for this amplifier is a folded cascode with a differential PMOS pair for its inputs. The input stage folded cascode NMOS current sinks are degenerated with resistors to lower their noise contributions and improve the amplifier's noise. This comes with an area tradeoff. The resistive degeneration can be removed for reduced chip area. Therefore, lowering production costs. Alternatively, a different input stage can be further analyzed and used.

### 5.2.4. Layout

The thesis design is at a point where it can be laid out and taped out. Layout and tape-out would enable testing of the fabricated structure and characterizing tradeoffs of this topology compared to other topologies. The chip area is chip cost.

### 5.2.5. 4-Stage Amplifier

The amplifier stage count can be increased to four stages. Adding one more stage complicates the frequency compensation, increases power consumption due to the additional power of the extra stage, and increases capacitor area. At the same time, it increases the gain of the amplifier and allows for using alternative frequency compensation techniques such as Hybrid Nested Miller Compensation (HNMC). An amplifier with four stages and HNMC is shown in Figure 5.2 [29].

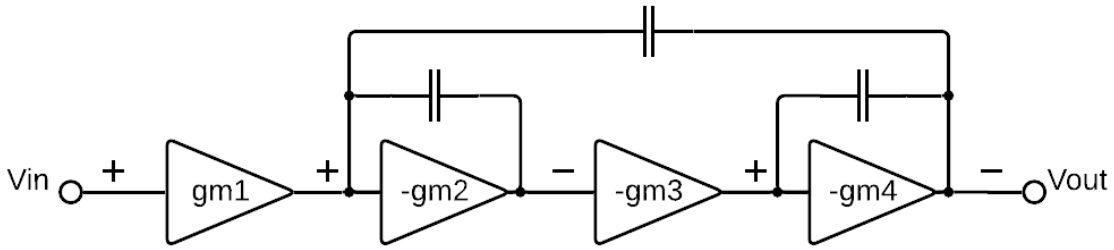


*Figure 5.2 4-Stage Amplifier with HNMC*

A 4-stage amplifier can be multi-path (MP) as well. In a multi-path amplifier, one of the signal paths is a feedforward path that bypasses some of the stages and their frequency compensation. The extra stage count allows for moving the cross-over frequency. It further moves the cross-over frequency to lower frequencies [29]. This reduces the noise peak at and around the chopping frequency and improves the noise spectrum [17]. An amplifier with four stages and MPHNMC is shown in Figure 5.3.

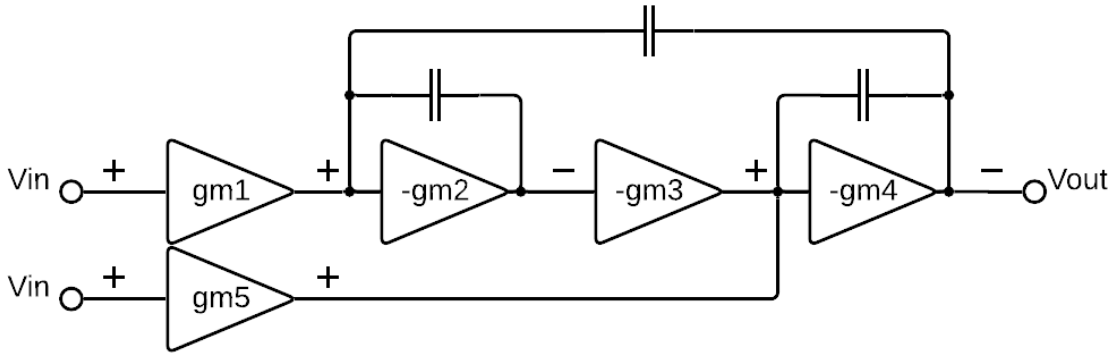


*Figure 5.3 4-Stage Amplifier with MPHNMC*

### 5.2.6. Instrumentation Amplifier

The operational amplifier is a high-gain amplifier that must be used in a loop. It has no decoupling between the input and output voltage ranges. On the other hand, an instrumentation amplifier has a well-defined gain predetermined and implemented into its feedback network. Therefore, the input (Vin) and output (Vout) are decoupled. This can achieve beyond-the-rail input sensing [16] [17].

The design of an instrumentation amplifier (IA) can be future work. A potential IA design is shown in Figure 5.4. The coupling capacitors (Cc1) block high DC voltages and protect internal structures. The first chopper (Ch1) up-modulates input signals and passes DC signals through the capacitors. This achieves beyond-the-rail input specs. The current feedback instrumentation amplifier (CFIA) is the amplifier's core. The CFIA uses the current domain and works with currents summing to zero [47]. This enables matching the differential input voltage with the differential feedback voltage and compensation for the native offset with the auxiliary amplifier [16]. The rerouting network (RN) pairs input and feedback voltages for small differentials at the input of the CFIA [48]. The auxiliary amplifier (GmA) compensates for the native offset of the amplifier and decreases the chopping ripple amplitude [17]. The second chopper (Ch2) demodulates signals. The output stages (Gm3) and their Miller compensation (Cm1/Cm2) couple the input to the output. The amplifier shown as having two stages in the schematic is simplified and has four stages. It is a multi-path implementation and uses hybrid

nested Miller compensation. The feedback network sets the well-defined gain of the instrumentation amplifier. The amplifier's gain accuracy can be improved using gain error correction [16].

The instrumentation amplifier decouples the input voltages from the output voltages. Therefore, the positive supply voltage can be decreased. Then the power consumption is reduced. This can be achieved by recreating the design using different voltage-rated transistors.

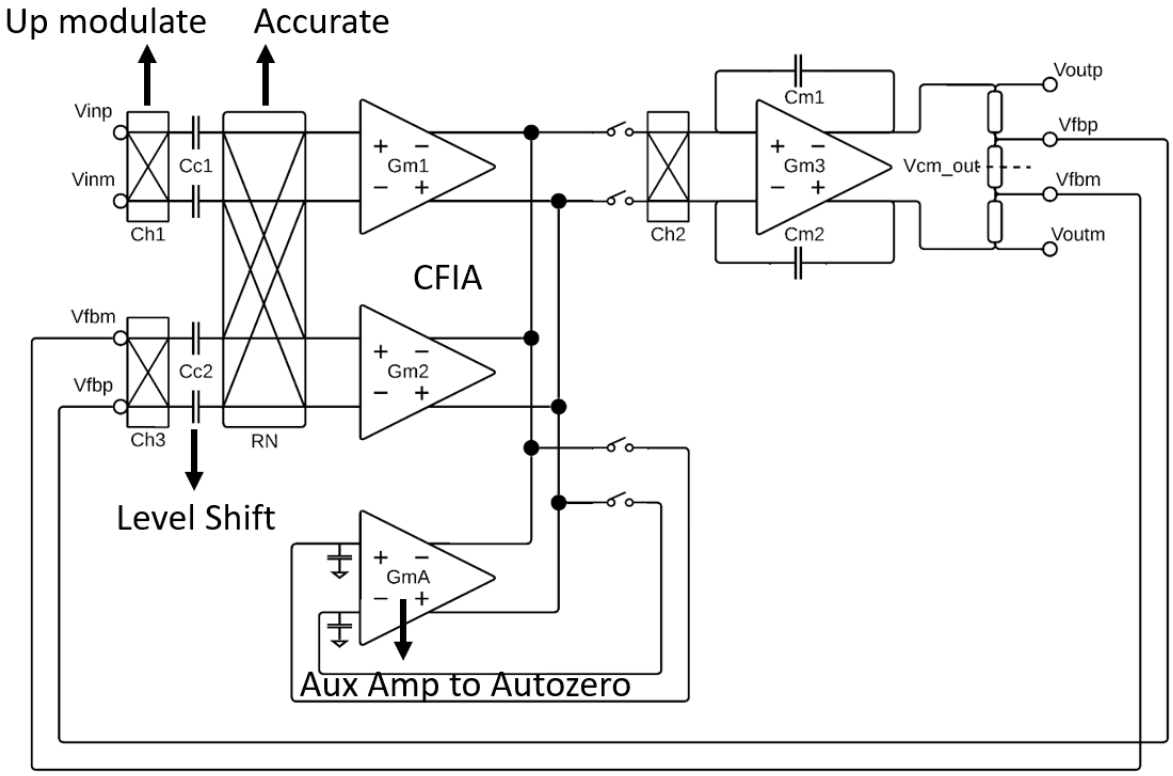


*Figure 5.4 Instrumentation Amplifier*

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