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Superconducting Magnetic Energy Storage-Based DC Circuit Breaker for HVDC Applications

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***Abstract*—Dealing with the fast-rising current of high voltage direct current (HVdc) systems during fault conditions, is one of the most challenging aspects of HVdc system protection. Fast dc circuit breakers (DCCB) have recently been employed as a promising technology and are the subject of many research studies. HVdc circuit breakers (CBs) must meet various requirements to satisfy practical and functional needs, among which fast operation, low voltage stress, and economic issues are the key factors. This article presents the procedure for designing a superconductive reactor-based DCCB (SSR-DCCB) for HVdc applications. In the proposed structure, a full-bridge power electronic configuration controls the superconducting reactor to limit the dc fault current and create a dc zero-crossing; it is connected to the HVdc line by a series transformer. After successfully suppressing the line fault current (current zero current), an ultrafast disconnector isolates the faulty line. The main advantage of the proposed HVdc CB is its ability to interrupt the dc fault current without using the solid-state main breaker and limit the magnitude of the fault current and voltage stress. The proposed SSR-DCCB is investigated in MATLAB/Simulink, and an experimental prototype setup validates the results.**

***Index Terms*—High voltage direct current (HVdc) circuit breaker (CB), HVdc protection, series limiting reactor, superconducting reactor.**

I. Introduction

HIGH voltage direct current (HVdc) system's technology has advanced significantly, considering its ability to enhance the efficiency of long transmission lines [1]. The evolution of the commercialized HVdc systems began in 1954 and has steadily progressed, facing various challenges along the way [2]. Nonetheless, ensuring the protection of the HVdc system remains a vital concern [3].

In the occurrence of a dc fault, the HVdc grid's low impedances cause a significant challenge, leading to a faster and higher fault current increase compared to ac grids [5]. Moreover, the dc fault current does not have a current zero crossing and a high rate of rise [6]. Consequently, HVdc grids require suitable circuit breakers (CBs) to promptly interrupt fault currents that could cause damage [7].

Researchers have recently studied several concepts as potential solutions to address dc fault current interruption in HVdc systems [8]. These solutions, namely fault current limiters (FCLs) [9] and fast HVdc CB [10], have emerged significantly. Within the HVdc system, FCLs operate crucially in enhancing the performance of fast dc breakers by mitigating the magnitude and rate of dc current rise [11].

HVdc CBs are anticipated to have four crucial features: ultrafast breaking action within a period of milliseconds; minimal conduction losses; prevention of excessive overvoltage during breaking operations; and the ability to dissipate energy effectively [12], [4].

Several types of HVdc CBs have been introduced, and are broadly classified as resonance or hybrid CBs. Among the resonance CBs, active and passive resonant CB schemes have been proposed as potential solutions for dc systems [13], [14]. However, their speed is inadequate for effectively safeguarding voltage source converter-based HVdc grids [15].

The hybrid HVdc CB has been introduced as an advanced technology capable of efficiently breaking high dc fault currents safely and reliably [16], [17]. The hybrid CB provides minimal conductive power losses attributed to its utilization of a solid-state load commutation switch (LCS) structure [18]. Notable examples of commercialized HVdc CBs include the ABB hybrid DCCB [19], the Alstom thyristor-based hybrid CB [20], Zhangbei project 500kV HVdc breaker [21], the SciBreak [22], Nan'ao project coupling mechanical HVdc breaker (CM-DCCB) consisting of capacitor storage [23], and air-core HTS pulse transformer for the S-HCB application [24]. Furthermore, various DCCBs are operating based on the hybrid breaker and controllable reactor principles, aiming to improve the performance of well-established hybrid breakers [25], [26]. Primarily, these breakers enhance the current limiter section of DCCB [27], [28].

Although hybrid CB technology offers advanced features, specific areas require improvement to enhance the overall performance. Accordingly, this artic;e aims to introduce a novel concept based on solid-state switches and superconducting magnetic energy storage (SMES), namely the superconducting storage reactor-based DCCB (SSR-DCCB). This configuration operates

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by taking into account the current injection of SMES and a solid-state bridge, offering the following advantages.

1) There is no need to employ a solid-state main breaker.
2) Very low voltage stress across the breaker.
3) Shallow peak of fault current.
4) Relatively fast fault current interruption (less than 1 ms).
5) Limiting the rate of fault current before breaker operation.
6) The decrease of the main breaker dissipated energy.
7) No need to enormous surge arrester.

Moreover, the reasons for selecting SMES technology to develop a new HVdc CB are as follows.

1) Minimal energy loss considering superconducting technology.
2) High transient current excitation capability.
3) Fast response time considering exciting circuit as a current source.
4) providing very fast reverse current to interrupt fault current.
5) Fast recharge capability, which provides swift reclosing.

The rest of this article is organized as follows. Section II demonstrates the SSR-DCCB configuration and its operation and provides an analytical study. Section III presents the simulation results. Section IV introduces the developed control strategy. In Section V, experimental test results are presented. In subsequent Section VI, the comparison study is presented. Finally, Section VII concludes this article.

II. SSR-DCCB Configuration, Operation, and Analysis

This section introduces the components of the proposed SSR-DCCB and discusses its operation principle. As demonstrated in Fig. 1, SSR-DCCB comprises a series transformer (ST), the primary winding of which is connected in series to an ultrafast disconnector (UFD) and the dc line. Its secondary winding is connected to the solid-state bridge switches and SMES reactor. This reactor is created by a high-temperature superconducting wire model, Bi2223, being cooled at a temperature of 77 °K using liquid nitrogen, with a quenching point for the superconducting reactor 2.5 kA. The secondary circuit of the SSR-DCCB includes four solid-state IGBT switches S_1-S_4, which create a bridge, and its middle branch connects to SMES and its charging circuit. Moreover, each IGBT switch is protected against voltage stresses by a parallel surge arrester.

For charging the SMES, we have considered an external circuit comprising a transformer, a rectifier, a resistor, a capacitor, a switch *S*5, and a current sensor. The charge circuit is shown in the Fig. 1(b).

The operation principle of the SSR-DCCB is classified into three statuses: normal steady-state condition, normal dynamic condition, and short-circuit fault condition.

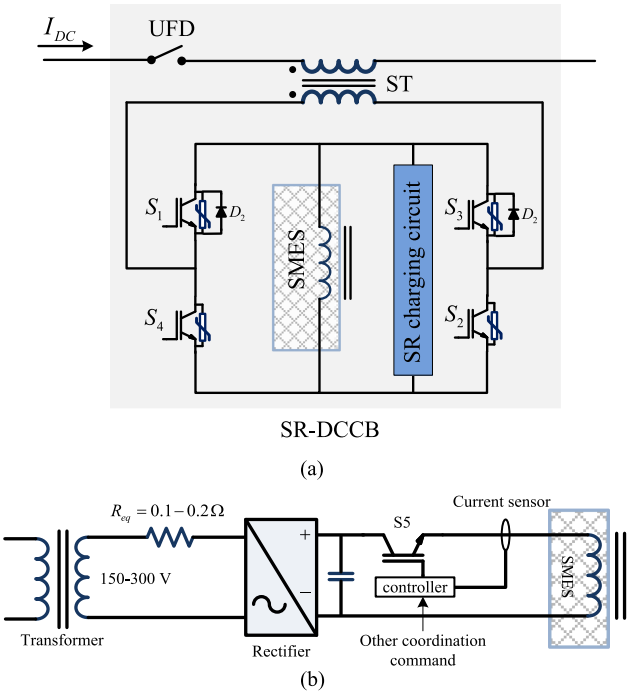

Fig. 1. (a) Superconducting reactor-based DCCB topology. (b) Charger circuit.

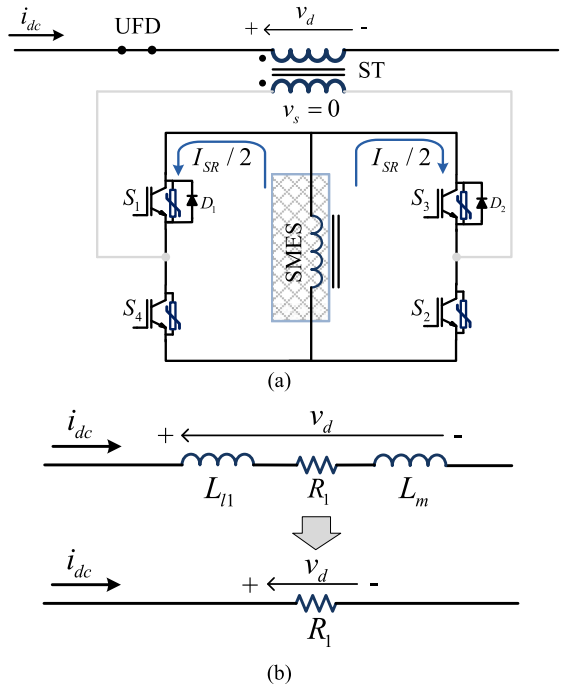

Fig. 2. (a) SSR-DCCB operation during normal steady-state condition. (b) Equivalent circuit for a normal steady-state condition.

A. SSR-DCCB Operation in the Normal Condition (Steady State)

For the first studied condition, it is considered that there is no fault and current variation. In this state, UFD is closed, and all the bridge IGBTs S_1-S_4 are turned ON to circulate the current of the SMES, which is known as I_{SR}. Considering that there is no current variation and voltage v_d in the ST primary winding, the voltage of the secondary winding v_s is almost zero. This operation is shown in Fig. 2(a).

The current circulation in the topology of SMES is provided by an external IGBT bridge. Since this freewheeling current has

its maximum value, the maximum energy of SMES is available to interrupt the fault current.

The equivalent circuit of the SSR-DCCB in this state is shown in Fig. 2(b), where there are three elements in series with the power line as a leakage inductance of ST primary (L_{l1}), the resistance of the primary winding (R_1), and magnetization inductance of ST (L_m). By assuming that there is no current variation, the voltage drop of the inductive term is zero and the only remaining element is R_1. The voltage drop of the SSR-DCCB is expressed by (1), which is extremely small

$$v_d(t) = i_{\mathrm{dc}}(t).R_1. \tag{1}$$

Considering that SSR-DCCB mostly operates in this mode, its power loss during the normal state is calculated as

$$p_{\mathrm{loss}}(t) = {i_{\mathrm{dc}(t)}}^2.R_1. \tag{2}$$

In addition, the current of the SMES is a constant value that is always prepared to operate for fault current interruption.

B. SSR-DCCB Operation in the Normal Condition (Dynamics)

This section focuses on the SSR-DCCB operation when the system dynamic occurs in normal operation. Considering the variation rate (increasing or decreasing of the line current), induced voltage polarity in the secondary winding can be changed where, in each state, D_1 and S_3 or D_2 and S_1 conduct the current of the secondary winding. These two operations for dynamic conditions are illustrated in Fig. 3(a) and (b).

During the dynamic state, the secondary winding is short-circuited by the solid-state switches, and the generated current in the secondary circuit bypasses the ST magnetization inductance. This equivalent circuit is illustrated in Fig. 3(c). In this circuit, leakage inductance L_{l2} and secondary winding resistance R_2 are in parallel with the magnetization inductance of the ST. Considering that the values of R_2 and L_{l2} are much smaller than the magnetization inductance, L_m can be removed from the equivalent circuit. Consequently, the remaining elements in the equivalent circuit are L_{l1}, R_1, L_{l2}, and R_2, which are connected in series to the DC power line. Also, a is the turns ratio of ST. Therefore, the voltage drop of SSR-DCCB can be written by expression as

$$v_d(t) = (R_1 + \alpha^2 R_2) i_{\mathrm{dc}}(t) + (L_{l1} + \alpha^2 L_{l2}) {di_{\mathrm{dc}}(t)}/{dt}. \tag{3}$$

Considering the value of the primary and secondary winding resistance and leakage inductances of both windings are so small, it can be concluded that SSR-DCCB has almost no effect on system dynamics and stability. To sum up, the series impedance of SSR-DCCB is almost equal to zero during system dynamics, and it has no system stability effects

$$p_{\mathrm{loss}}(t) = {i_{\mathrm{dc}(t)}}^2.\left(R_1 + \alpha^2 R_2\right). \tag{4}$$

C. SSR-DCCB Operation in the Fault Condition

This section provides information about the primary operation of the SSR-DCCB and how it can interrupt the dc fault current. Fig. 4(a) and (b) illustrates the operation principle of

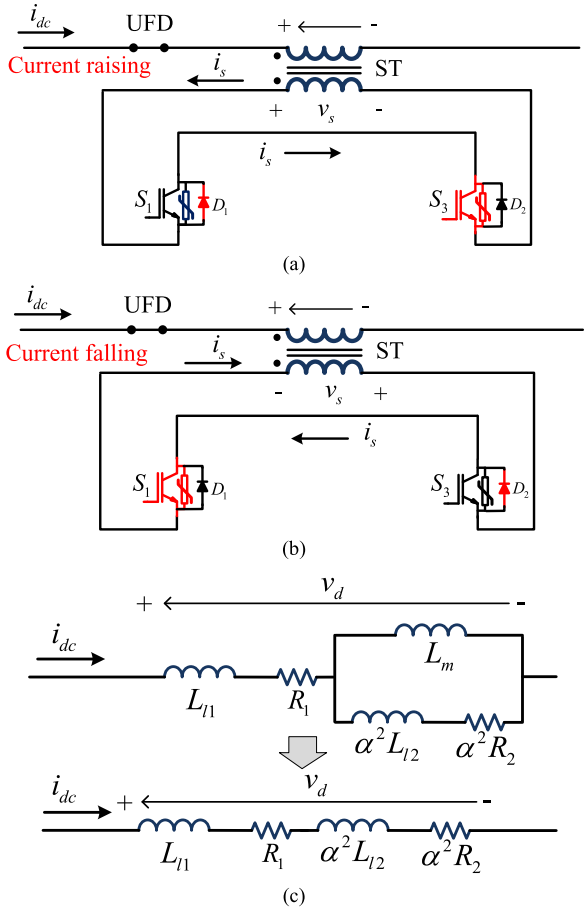

Fig. 3. (a) Operation SSR-DCCB in normal dynamic condition (current raising). (b) Operation SSR-DCCB in normal dynamic condition (current falling). (c) Equivalent circuit in a dynamic.

the SSR-DCCB for both different directions of the fault current (bidirectional operation).

In Fig. 4(a), it is assumed that the fault current passes from the left to right direction where, in this state, to interrupt the fault current, switches S_1 and S_2 will be turned ON, and switches S_3 and S_4 will be turned OFF to redirect the SMES current to the secondary coil of ST. This operation causes an induced transient voltage in the primary winding of the ST, which is in the reverse direction of the grid's voltage, forcing the fault current to decline and reach a current zero. By operating the control system with a current zero-cross detection, the UFD will open the faulty line and interrupt the current permanently. During the operation of UFD, the voltage across this switch is near zero because, in the current zero-crossing occurrence, the ST generates a reverse voltage opposite of the dc system voltage. It means that the voltage across the UFD is low enough to avoid arc formation and provide time for the complete operation of the UFD.

In the reverse fault current direction, as shown in Fig. 4(b), the operation procedure of SSR-DCCB is the same as the previous operation, while the turned-ON switches in the secondary circuit are S_3 and S_4, and switches S_1 and S_2 will be turned OFF. In the second operation, the state current of the secondary winding and

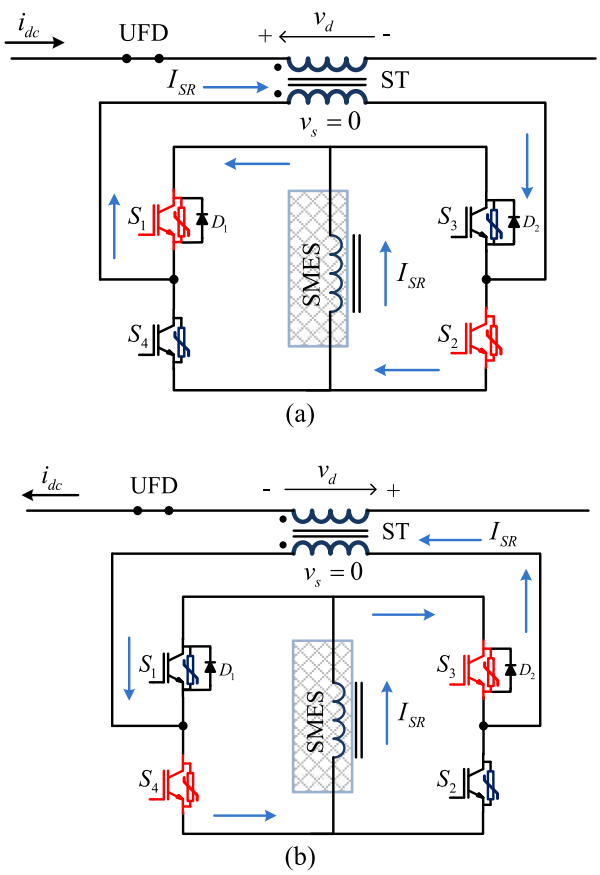

Fig. 4. (a) Operation SSR-DCCB in a direct fault current condition. (b) Operation SSR-DCCB in a reverse fault current condition.

induced voltage to the primary winding are reversed compared to the previous operation.

In this operation state, the SSR-DCCB voltage of the primary winding is computed using (5). In this equation, φ_t is the total linked flux in the ST core. This flux can be calculated by considering (6), where L_1 and L_2 are primary and secondary inductances of ST. Here, N_1 and N_2 are turns of primary and secondary coils, and i_{SR} is the current of SMES, which is this state equal to the secondary current of the ST. Finally, (7) presents the voltage of the primary coil throughout the fault, and the resistive voltage drop of the primary winding is ignored

$$v_d(t) = N_1 {}^{d\varphi_t(t)}/_{dt} + (R_1 + \alpha^2 R_2) i_{\mathrm{dc}}(t) \tag{5}$$

$$\varphi_t(t) = \varphi_1(t) - \varphi_2(t) = (i_{\mathrm{dc}} L_1 / N_1) - (i_{\mathrm{SR}} L_2 / N_2) \tag{6}$$

$$v_d(t) = d\left(L_1 i_{\mathrm{dc}}(t) - \alpha^2 L_2 i_{\mathrm{SR}}(t)\right)/dt. \tag{7}$$

Equation (7) can be used to calculate the required dc current in the SMES to provide the needed reverse voltage on the ST's primary side by considering the condition that the voltage of SSR-DCCB should be slightly higher than the dc system voltage. In this equation, L_1 and L_2 are inductances of ST's primary and secondary sides. α is the turns ratio of ST. φ_1 and φ_2 are magnetic fluxes of the core generated by primary and secondary coils of ST.

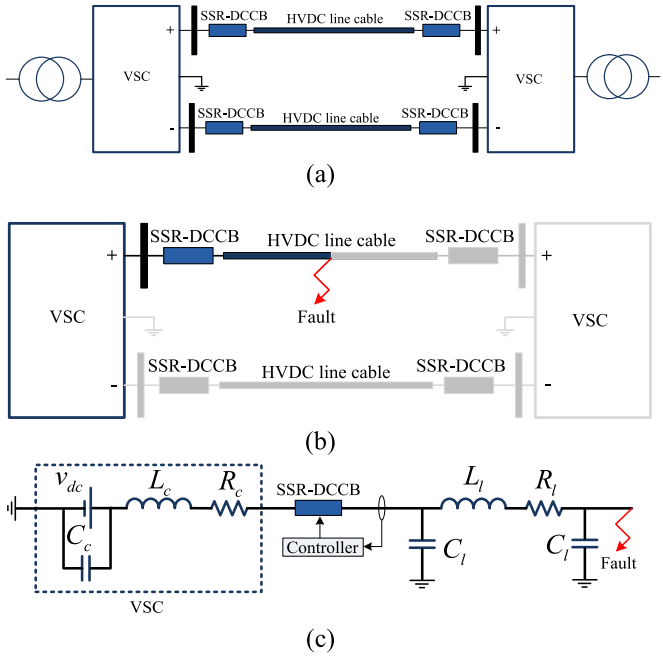

Fig. 5. (a) Illustration of the considered HVdc power system. (b) Simplified diagram to consider SSR-DCCB operation. (c) Simplified model for simulation.

III. Simulation of the SSR-DCCB Operation

To evaluate the main operation of the proposed SSR-DCCB, the simulation is performed for the circuit as shown in Fig. 5, where the fault is located on the point-to-point dc line and SSR-DCCB will operate from a normal state to short-circuit fault state. This simulation is carried out in MATLAB Simulink using the simplified equivalent of a VSC circuit in the fault state, dc power line model, and low impedance short circuit fault. The simulated power system diagram is illustrated in Fig. 5.

In Fig. 5(a), a point-to-point HVdc line is illustrated, where each line end is equipped with an SSR-DCCB. The rationale behind selecting the point-to-point dc line is to simplify the dc system and evaluate the SSR-DCCB features when operating against the dc fault current. Fig. 5(b) demonstrates a fault occurrence in the positive pole line, and the operation of SSR-DCCB will be observed only at the sending end of the HVdc line. In Fig. 5(c), the simplified model of the VSC, including the *RLC* branch and dc source as a charging circuit of the capacitor, is represented [29]. This circuit is connected to SSR-DCCB, HVdc line (a short length of a cable modeled by one PI-section with a fault occurring near the dc terminal), and the fault is shown, which is the practical way to demonstrate the performance of the proposed SSR-DCCB thoroughly. The data of the simulated HVdc power system are given in Table I. The assumptions for the simplified model of VSC during fault transient are the capacitor of VSC is fully charged by a dc source (in reality, by solid-state switches), and the power is injected into the dc line by an RL series impedance.

One important consideration when designing the ST of the proposed SSR-DCCB is the saturation. To avoid ST saturating in both normal and fault conditions, the parameters of the ST given in Table I are calculated according to [30]. In this calculation, a

TABLE I
SIMULATED HVDC POWER SYSTEM SPECIFICATIONS

	Parameter description	value
HVDC system	Series resistance of the VSC (R_c)	50 mΩ
	Series inductance of the VSC (L_c)	30 mH
	Shunt capacitor of the VSC (C_c)	5000 μF
	Voltage of the VSC (v_{dc})	200 kV
	Line equivalent resistance (R_l)	100 mΩ
	Line equivalent inductance (L_l)	0.5 mH
	Line equivalent capacitance (C_l)	0.2 μF
	Fault resistance	0.1 Ω
	DC line normal current	1 kA
SSR-DCCB	Primary coil turns	280 turns
	Primary coil inductance	100 mH
	Permeability of core	0.005
	Primary coil resistance	10 mΩ
	Secondary coil turns	28 turns
	Secondary coil inductance	1 mH
	Core normal magnetic flux density	0.7 T
	Core maximum flux density	1.8 T
	ST core cross section	0.5 m^2
	Secondary coil resistance	0.8 mΩ
	SMES Inductance	500 mH
	SMES Charged current	1400 A
	SMES critical current	2500 A
	IGBTs' turned ON resistance	0.1 mΩ

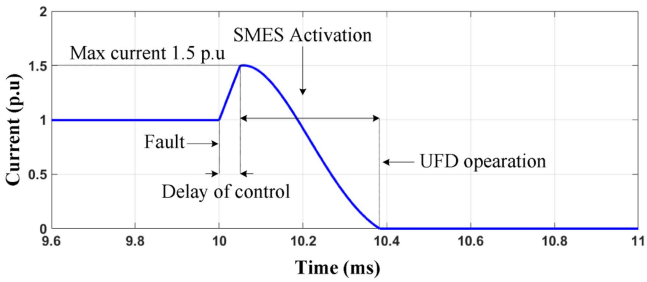

Fig. 6. HVdc line current.

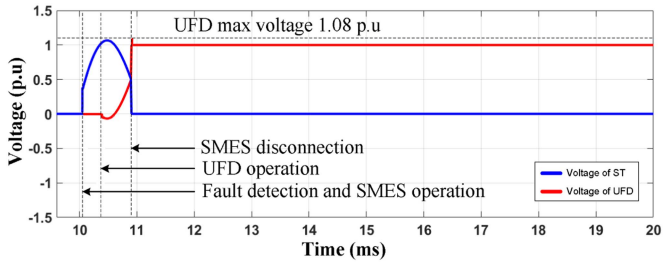

Fig. 7. Voltage across the SSR-DCCB.

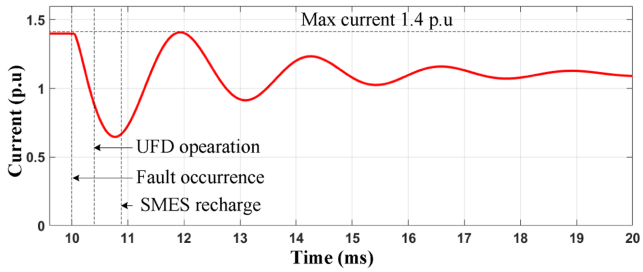

Fig. 8. Current of the SMES.

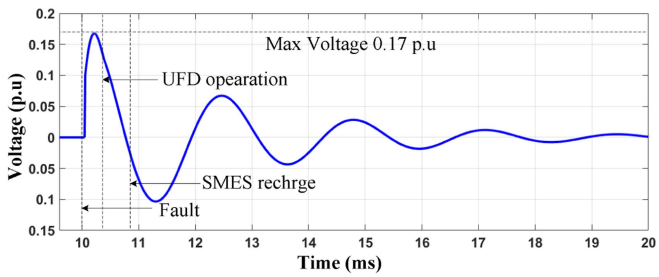

Fig. 9. Voltage across the IGBT arm.

line normal and maximum fault current, core cross-section, and primary turns of ST are considered to be ST operating under the saturation region.

In the simulated model, the VSC voltage is 200 kV (taken as 1 p.u.) the HVdc line's normal current is 1 kA (taken as 1 p.u.), and a fault occurs at $t = 10$ ms. In this simulation, the fault is detected 70 μs after the fault occurrence to activate SSR-DCCB. After the operation of SSR-DCCB, the line current drastically declines toward zero crossing, where the control system sends a command to UFD to disconnect the power line around a very low current. This scenario is clearly shown in Fig. 6 when the fault current maximum magnitude reaches 1.5 p.u. (where 1 kA known as 1 p.u.), and the fault current interruption duration is 0.4 ms. This current can be mathematically calculated using (7).

Considering Fig. 7(a), the UFD starts operating when the current zero is reached at 10.06 ms. At this instant, a current zero-crossing occurs because of the reverse voltage generated by the ST and SMES injected current. This means that the voltage across the UFD is low enough to avoid arc formation, and provides enough time for the operation of the UFD. It is observable that after 0.4 ms from fault inception, the voltage of the UFD rises. The peak magnitude of the voltage across the UFD after this time reaches 1.08 p.u. when the distance between conducts is long enough to withstand the recovery voltage. This voltage jump is suppressed by the ST reverse voltage, which is shown in Fig. 7(b). The duration of the ST primary voltage is nearly 1 ms and its peak magnitude reaches 1.08 p.u., which is in line with (7).

Fig. 8 shows the current of SMES during normal and fault conditions. This curve depicts the oscillating trend of the SMES current; hence, a port of its initial stored energy is used for the HVdc line current interruption after the fault (during 10.06–10.86 ms). After the falling trend of the SMES current, the charger circuit turns on to recharge the superconducting reactor again to reprepare it for the next required switching (if reclosing is needed). This oscillation is because of the connection of the charger to quickly transfer energy to the SMES. This current is finally stabilized for more than 1 p.u. where SMES is recharged by the energy resulting from the charger circuit.

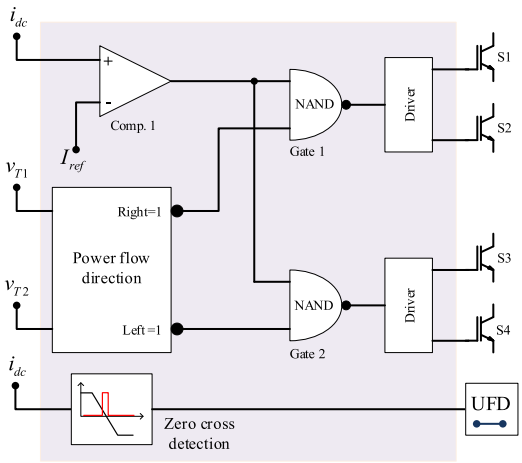

Fig. 10. Control diagram of the SSR-DCCB.

TABLE II
CONTROL LOGIC OF THE SSR-DCCB

Sequences	S_1	S_2	S_3	S_4	D_1	D_2	UFD	S_5
Normal	1	1	1	1	0	0	1	0
Dynamic Current rising	0	0	1	0	1	0	1	0
Dynamic Current falling	1	0	0	0	0	1	1	0
Fault (right side)	1	1	0	0	0	0	1	0
Fault (left side)	0	0	1	1	0	0	1	0
Fault interruption	0	0	0	0	0	0	0	0
SMES recharge	0	0	0	0	0	0	0	1

In Fig. 9, the voltage stress of the turned-OFF IGBT switches ($S3$, $S2$) is illustrated, considering that both voltages are the same for the last arm ($S1$, $S4$). A surge arrester and reverse diodes protect all the IGBT switches. The maximum magnitude of the voltage reaches 0.17 p.u., which can be simply withstood by applying conventional medium voltage (MV) IGBTs.

IV. CONTROL STRATEGY

The control strategy of the proposed SSR-DCCB is based on the current measurement and detection of power flow direction. The control system diagram is demonstrated in Fig. 10. By measuring and comparing the current value with the reference current via Comp. 1, as shown in Fig. 10, the HVdc line fault is first detected. Then, the direction of the power flow regarding the voltage difference between the sending and receiving end of the power line determines which IGBT switches in the bridge configuration must be turned ON or OFF. This decision is made by using two NAND logic gates 1 and 2. Thereafter, generated commands are driven to trigger IGBTs.

In the final stage of the control diagram, the dc line current will experience a zero crossing, and a current zero crossing detection block detects this state. It sends a command to the UFD to disconnect the power line and provide permanent current interruption. Table II gives the logical control of the switches for all operation stages. Furthermore, this table shows whether diodes are ON or OFF.

Considered operation sequences of the SSR-DCCB are likely the operation stages as shown in Section II, encompassing a normal operation, dynamic current rising, dynamic current falling, fault condition on the breaker right side, fault condition on the breaker right side, and fault current interruption.

Additionally, Table III gives the timing of the fault occurrence and SSR-DCCB operation and clarifies the operation time of each component in SSR-DCCB.

TABLE III
CONTROL LOGIC OF THE SSR-DCCB

States	Timing
Normal condition	t<10 ms
Fault occurrence	t=10 ms
Fault detection	t=10.06 ms
SMES activation	t=10.065 ms
UFD activation	t=10.4 ms
SMES Disconnecting and charger activation	t=10.8 ms
UFD reaches the max. gap	t=12.2 ms

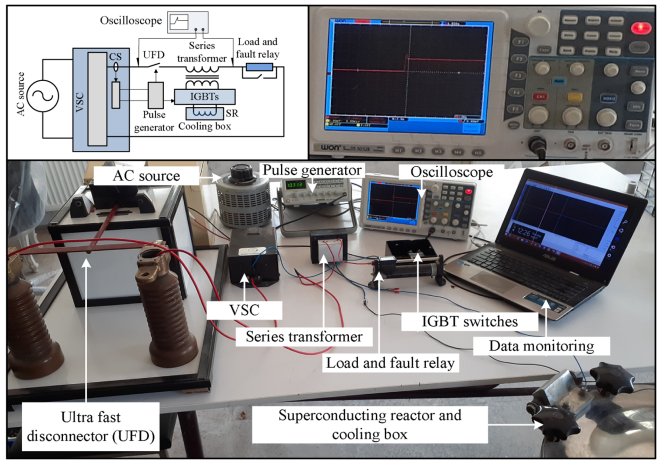

Fig. 11. Experimental laboratory test setup.

V. EXPERIMENTAL STUDY OF THE PROPOSED SSR-DCCB

In this section, the implementation of the prototype scheme of the proposed SSR-DCCB is shown as a laboratory scale-down setup to validate the obtained results from the simulations. Fig. 11 depicts the implemented SSR-DCCB, the laboratory setup, and the diagram of connections and measurement.

The details of the equipment considering the electrical specifications of the devices to carry out the laboratory tests are given in Table IV.

The parameters of the prototype inductance, resistance, and capacitance in the laboratory setup are the same as the presented parameters in Table I.

In the laboratory test procedure, firstly, the system operates in a normal condition where the output voltage of the VSC is 300 V (known as 1 p.u.), and the steady-state current is 1 A (known as 1 p.u.). The fault is applied by providing a short circuit on the dc load connected to the VSC. After the fault

TABLE IV
ELECTRICAL SPECIFICATION OF LABORATORY EQUIPMENT

Device name	Specifications
oscilloscope	Digital oscilloscope, model: WON ds5
UFD	Mechanical magnetic based, 20 kV, 100 A, 1.6 ms
IGBT	Bridge IGBT, 1200 V, 20 A
Deriver	3 A optocoupler IC series: FOD 3184
SMES	500 mH, HTS Bi2223
Cooler	Liquid Nitrogen cooling box at 77 Kelvin degree
VSC	IGBT-based, 500 W, 300 V, voltage source converter
AC source	Variable 1000 W autotransformer

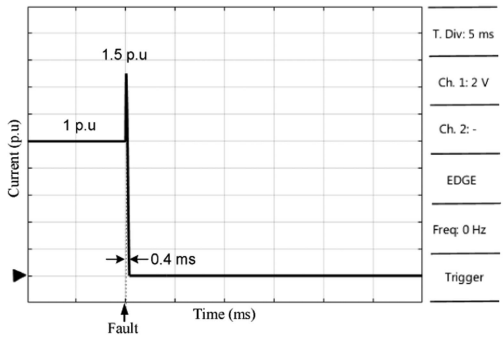

Fig. 12. Tested DC line current.

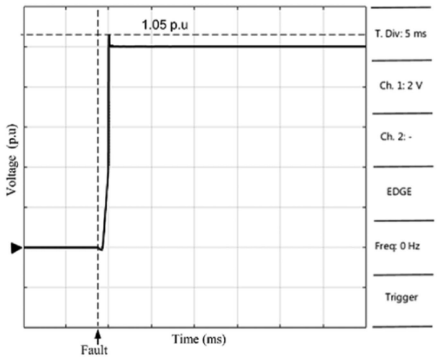

Fig. 13. Voltage across the UFD.

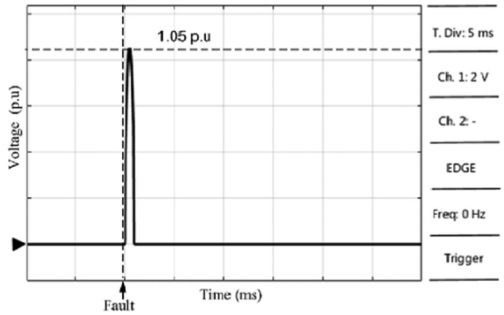

Fig. 14. Voltage of the primary side of ST.

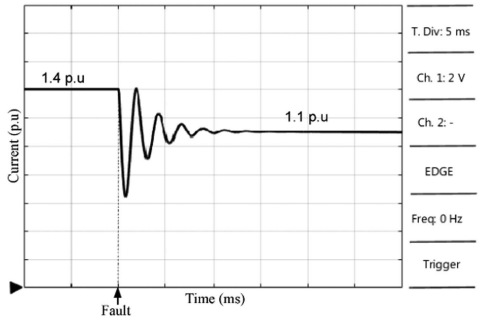

Fig. 15. Current of the laboratory SMES.

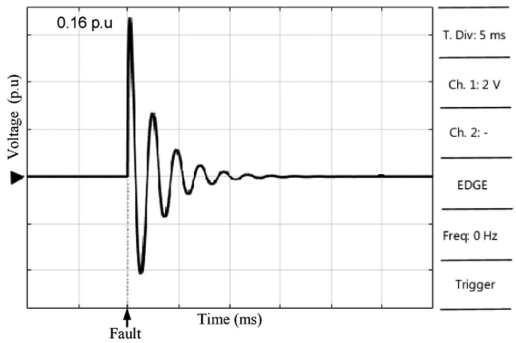

Fig. 16. Voltage across the SMES of the prototype.

inception, the VSC experiences the rising trend of the current until the internal controller of the VSC sends the command to the IGBTs of the SSR-DCCB to decrease the fault current. At the current zero crossing, UFD will operate to disconnect the VSC from the faulty line. The current trend measured in the laboratory setup is depicted in Fig. 12. This figure validates the simulation presented in Fig. 6, where the current variation trend is in good agreement.

Fig. 13 shows the voltage across the UFD of SSR-DCCB. This voltage also validates the simulation results shown in Fig. 7. The peak magnitude of the voltage reaches 1.05 p.u. and then quickly declines toward the voltage of the VSC. Furthermore, after starting the operation of UFD, its voltage for a duration of roughly 0.4 ms is close to zero. It reaches maximum voltage when its contact moves for a distance of 25 cm between terminals.

Fig. 14 shows the primary induced voltage of ST, which is in the reverse direction of VSC voltage to create a current zero-crossing and decline the voltage across the operated UFD to avoid arcing when the contacts of UFD are not far from each other. The peak magnitude of this voltage is 1.05 p.u., and its duration is nearly 1 ms.

Fig. 15 verifies the SMES current curve of the laboratory setup, which is in good agreement with the simulation result in Fig. 8. According to this figure, SMES current declines from 1.4 to 0.45 p.u. during the fault interruption operation, and then its current oscillates, affecting the charging circuit to recharge and stabilizes at 1.1 p.u.

Moreover, according to Fig. 16, the maximum stress voltage of IGBTs ($S1$, $S4$ and $S3$, $S2$) is limited to the safe range, confirming the results obtained in Fig. 9. The peak magnitude is less than 0.2

p.u., and its voltage oscillates and declines to zero after almost 15 ms.

VI. Feasibility of Implementing the Real-Scale SSR-DCCB

Technical justifications are provided to assess the feasibility of implementing the proposed SSR-DCCB in both MV and high voltage (HV) level grids. Here the discussion regarding the feasibility of the SSR-DCCB in MV and HV dc grids is structured around the examination of each of the three main sections comprising the SSR-DCCB design.

Regarding the series reactor, the SSR-DCCB incorporates a series dc reactor with an inductance in the range of 100 mH. This value of the inductance is suitable for both MVdc and HVdc grids, as it aligns with the specifications commonly utilized in the topology of recently designed limiter reactors for dc grids. Employing a 100 mH series reactor is practical for full-scale breakers, offering advantages in terms of stability, power loss, and protection effects. We base our reasoning on the findings of the following state-of-the-art studies referenced in our manuscript [19], [20], [21], [22], [23].

Regarding SMES, in our simulation, the designed SMES has a capacity of 500 kJ and is connected to the secondary circuit of the ST at a voltage level of a maximum of 20 kV in transient states. This SMES design is suitable for real-scale HVdc grids, given its moderate capacity and MV range.

Regarding solid-state switches, the primary challenge in designing HVdc CBs lies in employing multiple series of solid-state switches to withstand the voltage stress during the current interruption. In the designed SSR-DCCB, all solid-state switches are linked to the secondary side of the ST, with a maximum voltage stress of 32 kV, compared to the grid nominal voltage of 200 kV. For practical implementation, only three IGBTs (4.5 kV) modules are required for each arm of the bridge rectifier, presenting a significant advantage over the conventional approach of using numerous IGBTs in series for the main breaker, as often suggested in research studies.

In summary, the feasibility of each key component of the SSR-DCCB offers logical advantages over other types of HVdc CBs.

Regarding the reclosing capability of the SSR-DCCB in practice, it is possible based on the following procedure: First, the UFD closes the line to conduct the current. Second, when the current does not exceed the normal value and voltage takes place as its nominal value, power should flow as its nominal value (fault removed). Third, when the current exceeds the normal value and the dc-protected terminal faces under voltage (fault remains), SMES switches will operate. Finally, the UFD will open the line at the current zero-crossing.

VII. Comparison Study of Proposed SSR-DCCB

In this section, the comparison study is carried out between features of the studied SSR-DCCB and two well-known HVdc CBs to prove the main contributions of the SSR-DCCB concept. Regarding this comparison, the features of the breakers are given in Table V. The comparison is carried out with hybrid breakers [23], which, in practice, utilized HVdc breakers and designed SSR-DCCB. Considering that these breaker properties are presented for different dc voltage levels, for the sake of clear and reasonable comparison, the current and voltage magnitudes are presented in per unit voltage and current. The focused features are the number of used switches for each topology, the transient interruption voltage, the peak magnitude of the interrupted current, the duration of the current interruption, and the dissipated energy.

TABLE V
Comparison of the HVDC Breakers

Sections	Hybrid breaker [19]	CM-DCCB [23]	S-HCB [24]	SSR-DCCB
Peak voltage	1.5 p.u.	2 p.u.	1.8 p.u.	1.05 p.u.
Peak current	9 p.u.	18 p.u.	6 p.u.	1.5 p.u.
Operation time	<5 ms	5 ms	<1 ms	0.4 ms
LCS	1 IGBT, 4.5 kV, 4.8 kA	Four fast mechanical switch	-	-
Main breaker	67 series IGBT,	LC resonance	1 FMB	-
Ultra-fast disconnector	1 UFD	-	-	1 UFD
Limiter DC reactor	one reactor, 100 mH	-	one series transformer	one series transformer, 100 mH
Arresters	MOV voltage 1.5 p.u., 2.75 MJ	MOV voltage 1.5 p.u.	MOV voltage 1.8 6 kA	MOV voltage 0.16 p.u.
Snubber	67 RCD snubber	Four RC snubber and Four shunt resistor	-	-
Reactor switch	-	A SCR	2 IGBTs 12 kV, 200 A	12 IGBT 4.5 kV, 4.8 kA
Storage	-	capacitor bank	Two capacitor banks	One SMES reactor
Normal state power loss	Reactor loss	Limiter reactor loss	ST loss	ST loss

Considering the rating of required equipment for designing a real-scale SSR-DCCB, and the number of required solid-state switches, arresters, capacitors, and mechanical switches, it can be concluded from a cost-performance point of view that the proposed SSR-DCCB has substantial economic benefits.

Considering the comparison provided in Table V, the overall advantages of the SSR-DCCB over the three relevant technologies are as follows.

1) Lower peak magnitude of voltage stress and current.
2) Very fast operation time of less than 0.5 ms.
3) No need for a main breaker, either mechanical or solid-state.
4) No need to use enormous metal oxide surge arrester.

The challenge of SSR-DCCB is as follows.

1) Designing the applicable SMES for an appropriate performance.

VIII. Conclusion

This article proposes the design of a crucial topology aimed at significantly enhancing the performance of currently employed DCCB in HVdc systems. The novel DCCB, referred to as SSR-DCCB, comprises three essential components: controllable reactors; SMES; and an MV IGBT full bridge. Through simulation and experimental scale-down tests, the investigation results in the following outcomes: SSR-DCCB can effectively interrupt dc fault currents without relying on the main breakers and LCSs, leading to a substantial reduction in voltage stress across the breaker, eliminating the use of large surge arresters to dissipate huge amount of energy and limit the fault current peak to an exceptionally low value. Moreover, the operation of this CB is fast, taking less than a millisecond. Notably, the achieved results showcase a pioneering topology that operates distinctively from the well-known hybrid or resonance HVdc breakers, marking a significant advancement in the field.

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