A Bootstrapped ESD Structure for CMOS Amplifiers with femtoampere leakage current

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Challenge the future

A Bootstrapped ESD Structure for CMOS Amplifiers with femtoampere leakage current

by
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TU Delft

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Abstract

Integrated circuits (ICs) are susceptible to damage by Electrostatic Discharge (ESD), which necessitates protection diodes. However, these diodes can cause leakage currents in the range of picoamperes, dominating the input current of CMOS ICs. This thesis presents the implementation of a low leakage bootstrapped ESD protection circuit for amplifier's with low input currents. An auxiliary buffer connected to the input pad is used to drive the voltage across the ESD protection diodes to a near-zero value, thus ensuring leakage currents in the femtoampere range. Two kinds of protection diode structures were designed and characterized. Based on the results, an auxiliary buffer was designed to bootstrap the diodes. Next, the bootstrapped ESD diode structure was taped out and measured. A low leakage test PCB was designed using techniques such as guarding, shielding, and via-fencing, resulting in bare PCB leakage currents well below 20 fA. The ESD protection circuit is fabricated in TSMC 180 nm MS/RF CMOS technology and occupies an area of 0.043mm^2. With this circuit, input leakage currents below 150fA have been measured.

Acknowledgment

Seven years ago, the dream of pursuing a master's in the field of Analog Design seemed only that – a dream, a fantasy. Now that I am defending my thesis after this arduous pursuit of that dream, I can say that the journey has made me strong, fearless, empathetic, and determined. However, my pursuit would not have been fruitful without the assistance and advice of numerous amazing people.

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Last but not least, I would like to thank my parents for their support and understanding.

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1. Introduction

1.1. Motivation

The phenomenon by which two dissimilar objects in physical contact build up static electric charges when separated is called the triboelectric effect [1]. This can often be experienced in day-to-day life. One example is the small electric shock that can sometimes be felt when a door handle is touched after walking on a carpet. This electric shock is due to the discharge of the accumulated charge on our bodies through the door handle, known as electrostatic discharge (ESD). Depending on its magnitude, it is often possible to feel and witness the discharge in the form of a spark or a flash. Although humans can easily handle these small ESD events, not everything can handle this discharge without damage. One example of this is a semiconductor chip. If a semiconductor chip is not handled with care and proper ESD protection, there is a good chance that it will be damaged. This is due to the discharge through the chip and the sensitive structures it comprises. Figure 1-1 shows the magnified view of a metal trace within an SRAM before ESD and its damage after an ESD event [2].

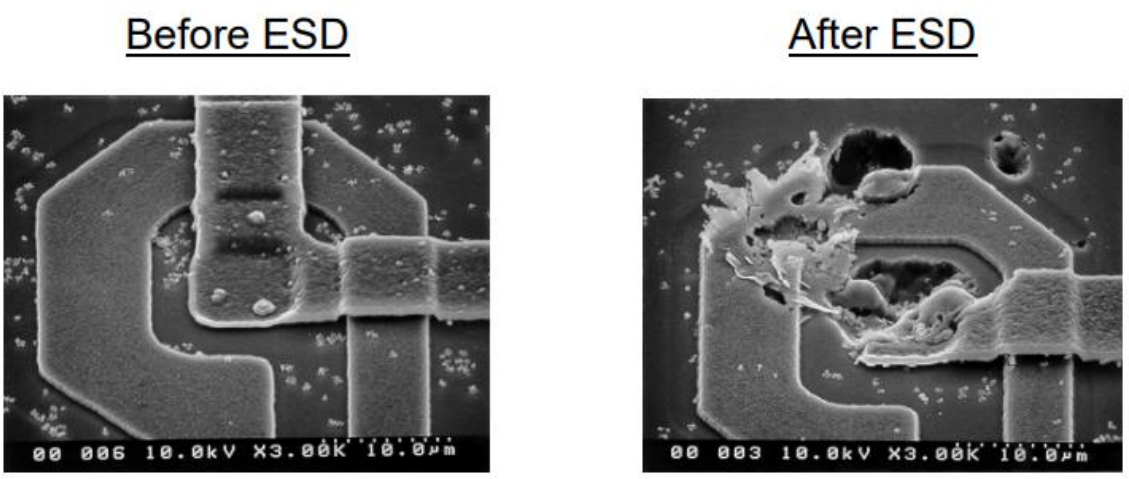


Figure 1-1: Magnified metal trace before ESD and after ESD[2]

With advances in semiconductor technology, the structures inside the chip have become progressively smaller (thinner oxide, shallower junction, etc.) and, consequently, are more susceptible to ESD damage. Since damage to a single component on a chip can render it useless, it is essential to take protective measures to safely handle ESD events that a chip might experience during its installation and operating lifetime.

ESD damage is one of the most critical reliability issues in the semiconductor industry. Statistics indicate that 30% of IC failures are attributed to ESD [1]. To mitigate ESD damage, special measures (e.g., ESD straps or gloves) are often taken in testing and manufacturing environments to neutralize static electricity [3]. Besides such efforts, a typical chip will contain additional circuitry to handle ESD events and protect it from ESD damage. Protection against electrostatic discharge is a well-known concept. An example of this is the lightning rod used to prevent damage to high-rise buildings. Just as a lightning rod shunts the current due to a lightning discharge to the

ground, chips contain protective circuitry that shunts the current due to ESD events safely without damaging the circuitry in the chip.

1.2. Challenges and Solution

Several ESD protection circuits have been proposed in the literature. Based on their behavior, they are broadly classified into two categories: non-snapback and snapback [1], [4]. The non-snapback category includes devices such as p-n junction diodes, zener diodes, and polysilicon diodes. This category is characterized by a critical voltage V_t after which the current tends to increase rapidly while the voltage remains nearly constant, as shown in Figure 1-2.a [1]

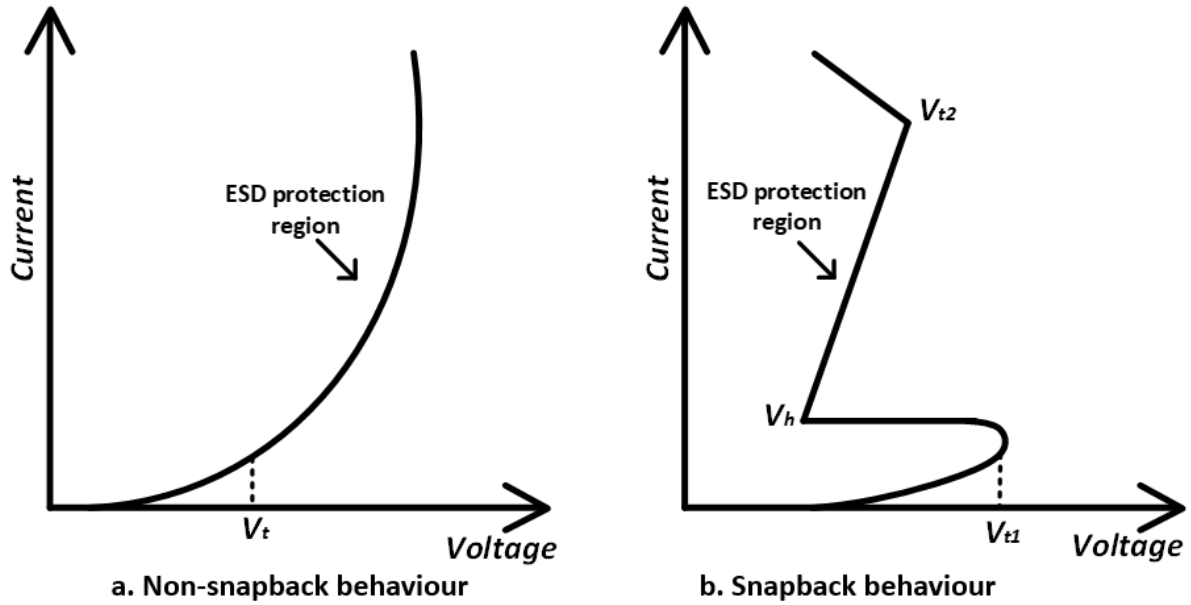


Figure 1-2: I-V curve for ESD Protection design: a.non-snapback b.snapback [1]

The snapback category includes devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and silicon-controlled rectifiers (SCR's). In this category, if the voltage across the device is increased above V_{t1}, it enters the breakdown region. After the breakdown, due to an internal feedback mechanism, the voltage decreases, and the device moves to the holding region, V_h. This creates a discharge path for current. While SCR-based protection circuits offer smaller sizes, lower on-state impedance, and lower capacitance, they have higher triggering voltages and higher turn-on time. Diode-based protection circuits are the simplest of them and are preferred for low voltage and high-speed applications [5]. Compared to other approaches, however, they exhibit higher leakage especially at high temperatures [6].

The leakage of ESD diodes via input pads is a severe drawback in applications where a high input impedance is required or where input bias currents need to be very low, in the range of hundreds of femtoamperes [7]. In such cases, traditional ESD diode structures cannot be used because the associated leakage currents will be very high, around 1pA [7]. For high-impedance readouts, it is desirable to have an ESD structure that is robust and provides less leakage.

For example, an auto-zero (AZ) stabilized voltage amplifier with a trimmed input current of 0.2pA has been designed [7]. Its input current was measured by connecting

the buffer to an on-chip hold capacitor and then observing the resulting voltage drift. In general-purpose applications, the amplifier's input pads need to be protected by ESD diodes. However, the maximum leakage current of the standard ESD diodes was measured to be 1pA at room temperature. This is much higher than the amplifier's input current. Furthermore, diode leakage increases exponentially at high temperatures. Therefore, there is a need to design low leakage ESD diode structures [8].

This thesis aims to design a low-leakage diode structure whose input leakage current is below 50fA at room temperature.

2. Bootstrapped ESD diode structure

2.1. Principle of Operation

The schematic of a standard ESD diode structure is shown in Figure 2-1. It consists of two diodes: D_1 and D_2, connected to an I/O pad, VSS (0V), and VDD (1.8V). In case of an ESD event at the I/O pad, these two diodes prevent excessive input voltages (V_{in}) that could otherwise damage the circuitry connected to the pad.

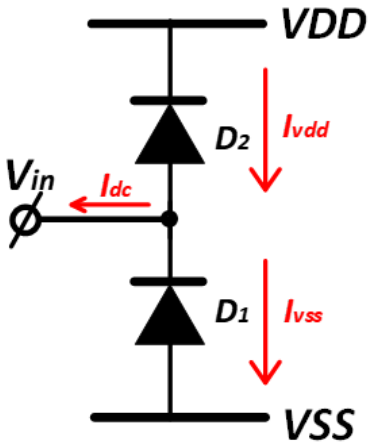


Figure 2-1: Standard ESD Diode structure

This can be understood by looking at the typical I-V characteristics of a diode, shown in Figure 2-2. The current through a diode increases rapidly when the forward voltage V_a, typically 0.7V for silicon diodes, is exceeded. If an ESD event causes the input voltage to exceed the supply voltage VDD (1.8V) plus the forward voltage, diode D_2 will be forward biased and will shunt a large current to VDD. In the same way, if the input voltage is less than VSS (0V) minus the threshold voltage of the diode, then diode D_1 will be forward biased and shunt a large current to VSS. In this way, the ESD diode structure prevents V_{in} from going one forward voltage above or below the supply rails, as long as the shunting current is large enough. During regular operation ($V_{SS}<V_{in}<V_{DD}$), these diodes are reverse biased and will only conduct a small reverse current denoted by I_{vdd} and I_{vss}, as shown in Figure 2-1. The combination of I_{vdd} and I_{vss} gives rise to a leakage current ($I_{dc}=I_{vdd}-I_{vss}$) provided by the input.

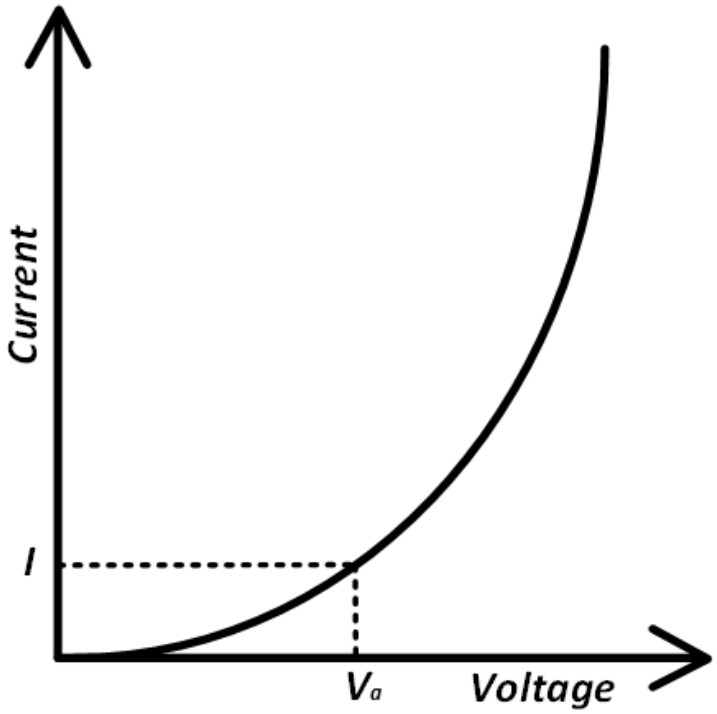


Figure 2-2: Typical I-V curve of the standard TSMC ESD protection diode

Figure 2-3 shows a plot of the measured leakage current (I_{dc}) versus input voltage for the standard ESD diode structure available in a traditional CMOS process (TSMC 180 nm MS/RF CMOS technology) [7].

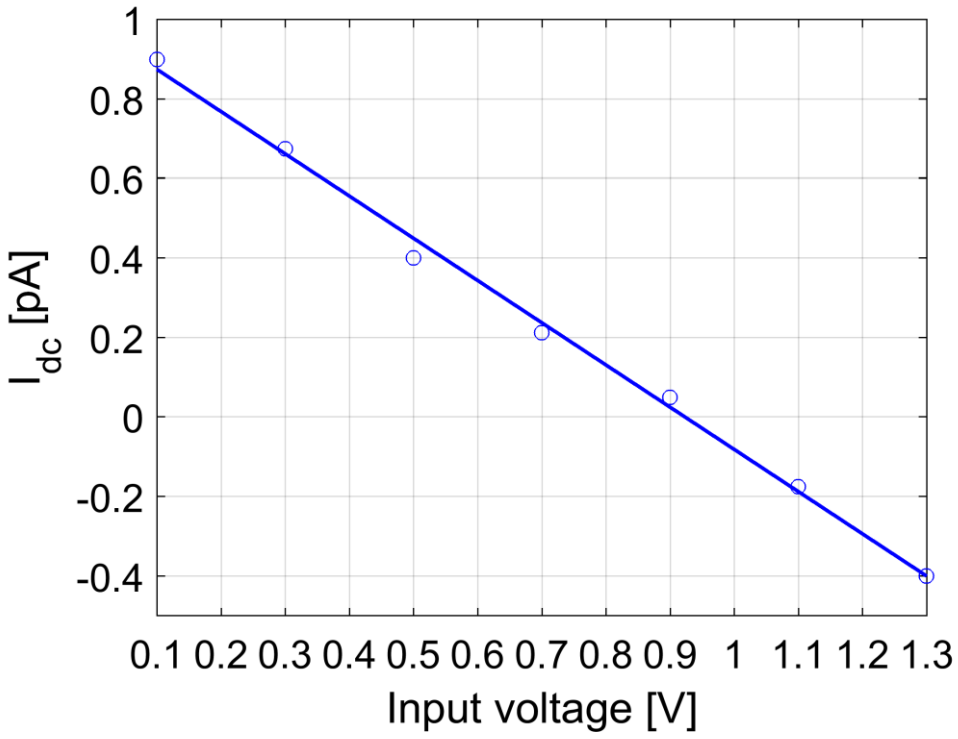


Figure 2-3: Measured input current vs. input voltage plot of standard TSMC ESD diodes

As shown in Figure 2-3, the leakage current is linearly related to the input voltage. At an input voltage of 0.1V, the input current is close to 1pA. In this case, D_2 has a big reverse voltage, while D_1 has a small reverse voltage, which means that I_{vdd} almost entirely determines the leakage current. When the input voltage is halfway between VDD and GND, i.e., equal to 0.9V, the input current is zero for nominally identical diodes because the I_{vdd} and I_{vss} compensate each other. At an input voltage of 1.3V, the input current is dominated by I_{VSS}.

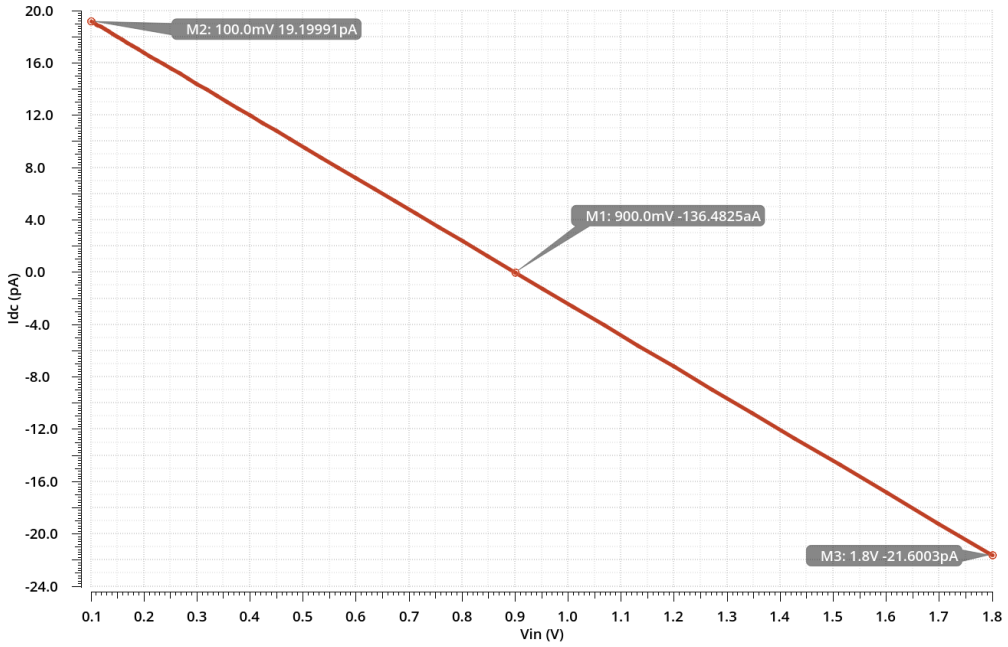


Figure 2-4: Simulated input current vs. input voltage plot of standard TSMC ESD diodes with VDD=1.8V, T=27°C

Figure 2-4 shows the simulated leakage current for the same diode structure as measured in [7]. Despite the same trend, a significant difference (nearly 20×) is observed between the simulated and measured values. This significant difference may be due to the large safety margins used in the TSMC models. From these measurements and simulation, it is clear that for a standard ESD structure, the leakage current is much higher than the targeted 50fA. This leakage is too high for our application, and hence, a better ESD protection circuit is needed.

2.2. Design of bootstrapped diode structure

The current *I* flowing through an ideal p-n junction is given by

$$I = I_s \left[exp\left(\frac{V_a}{V_t}\right) - 1 \right] \tag{2.1}$$

Where I_s is the reverse saturation current
V_a is the applied voltage across the p-n junction diode
V_t is the thermal voltage

For $V_a = 0$, the current *I*=0. At positive values of V_a, the exponential term inside the bracket dominates, and the current-voltage relationship becomes exponential. If the diode is reverse biased, the current exponentially decays to the value of $-I_s$ (reverse

saturation current). So minimizing the p-n junction voltage is critical for reducing its leakage current. This can be achieved using the bootstrapping technique [8]. As shown in Figure 2-5, ESD diodes are stacked, and intermediate nodes: CP and CN are connected to a buffered version of the input voltage. Ideally, this method eliminates the voltage applied on D_2 and D_3 and forces zero diode leakage. In the actual design, the input leakage current through the diode will be determined by the buffer's offset. If the buffer's offset is small, the current through D_2 and D_3 are nearly zero. The currents through D_1 and D_4 would flow into the output terminal of the buffer.

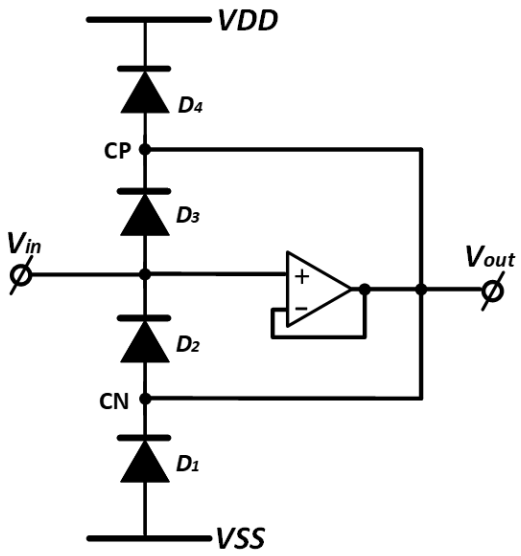


Figure 2-5: Bootstrapped ESD Diode structure

Figure 2-6 shows the simulated leakage current vs. offset voltage of the buffer. For simplicity, the buffer is modeled as an ideal voltage-controlled voltage source (VCVS), where an offset was inserted to simulate the effect on the leakage.

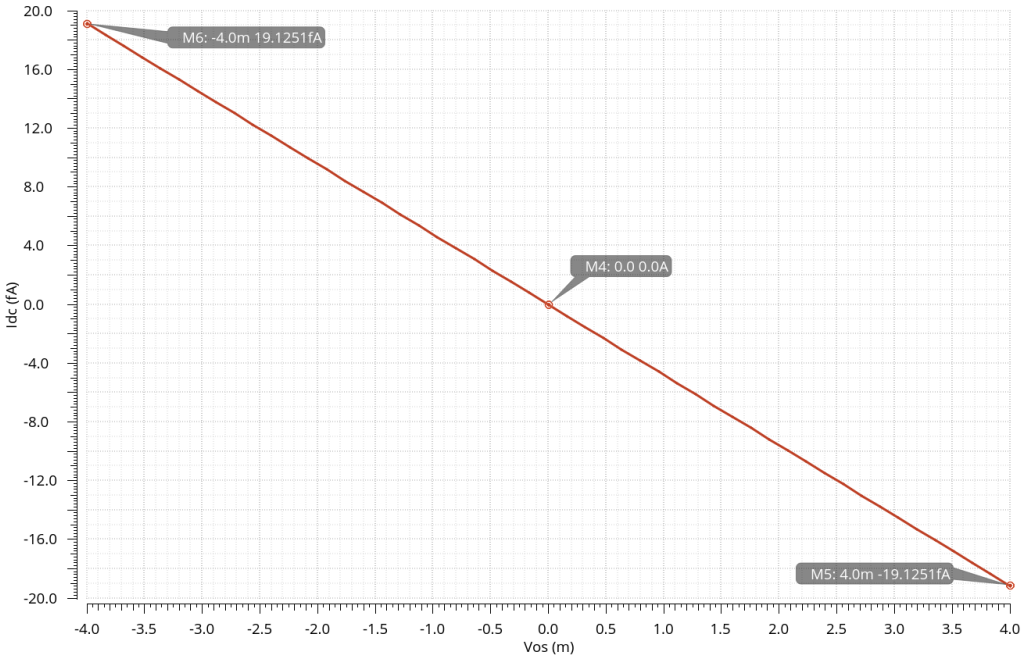


Figure 2-6: Input current for bootstrapped diode structure for different offset values of the buffer

From simulations, the leakage current is around 20fA given a 4mV buffer offset. Since the simulations are rather pessimistic, as explained in section 2.1, the measured results are expected to be about 20× better.

The simulations clearly show that the use of bootstrapped diode structure significantly reduces leakage. The following section deals with the design and fabrication of the bootstrapped diode structure. Two kinds of diodes (i.e., P+/N-well diode and N+/P-well diodes) were designed and taped out in a TSMC 180 nm MS/RF CMOS technology.

2.2.1. P-diode (P+/N-well diode)

The cross-section of the standard ESD Diodes of Figure 2-1 is shown in Figure 2-7. Diode D_1 is formed between the P+ and N+ diffusion areas on a P-Substrate. Diode D_2 is formed between P+ and N+ diffusion areas in an N-well.

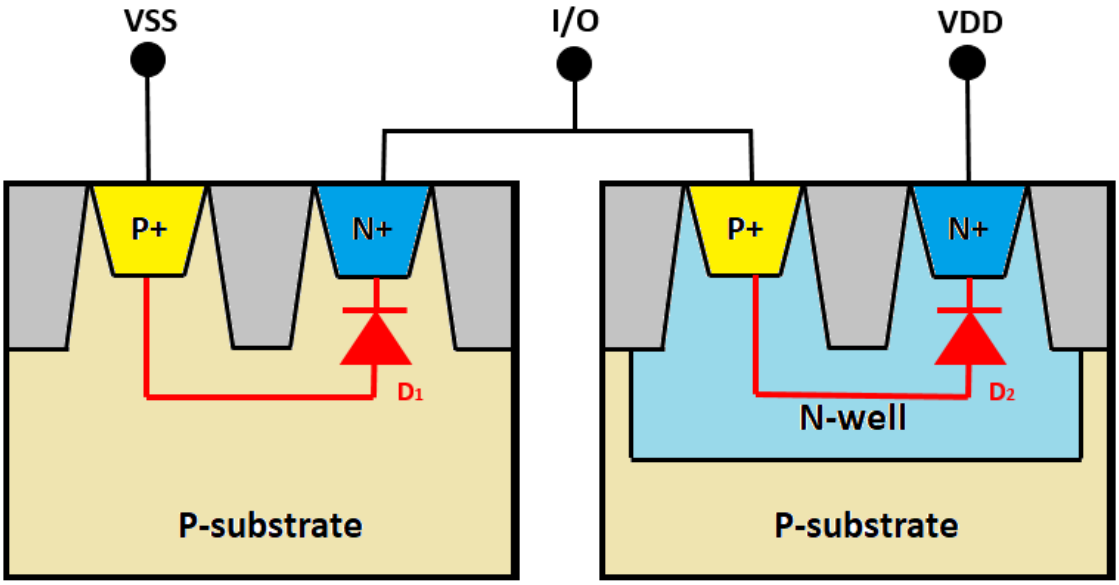


Figure 2-7: Cross Section of a standard ESD Diode

The structure shown in Figure 2-7 cannot be used directly to implement the bootstrapped ESD diodes due to the direct connection of the P+ side of D_1 to the substrate. However, in the bootstrapped ESD diode structure of Figure 2-5, the p+ of diode D_2 needs to be connected to CN. To disconnect the P+ from the substrate, a Deep-N-well is necessary. This results in an increased area with no other added benefits.

The proposed scheme of bootstrapped diode structure would resolve the above problem. It uses four diodes, each in the form of P+/N-well, as shown in Figure 2-8. The layout of the P-diodes has been obtained from Corentin Pochet (Prof. Drew Hall group from UCSD). The P+/N-well structure was already tested for its ESD protection capabilities.

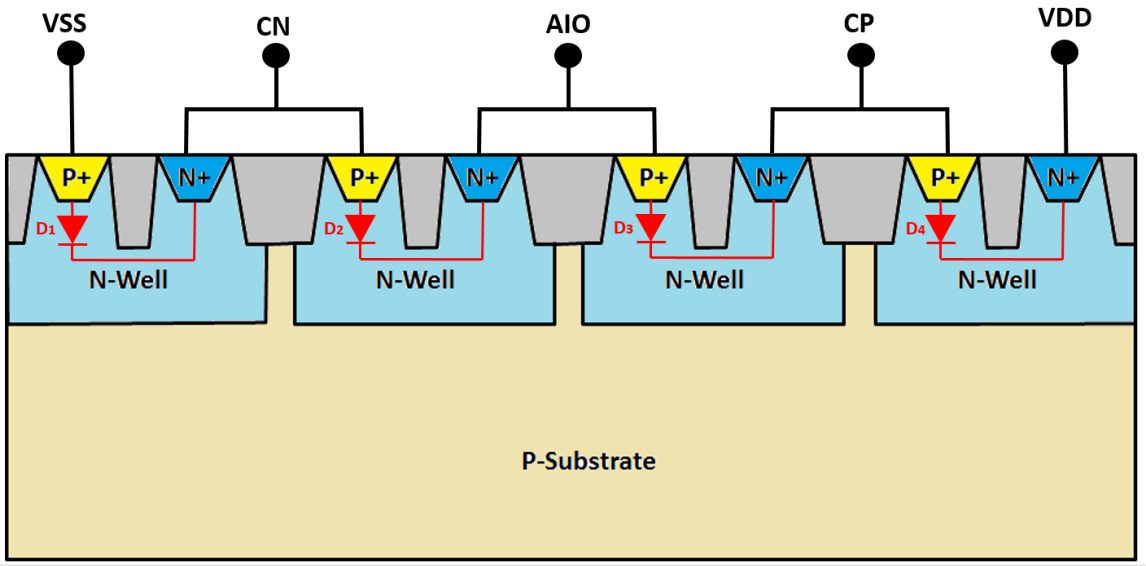


Figure 2-8: Cross Section of a P+/N-well diode

The bootstrapped diode structure consists of a string of four diodes D_1-D_4 connected between VDD and VSS. Each diode is formed between P+ diffusion and

the N-well. These wells are placed in the P-substrate. The diodes were designed and taped out in a TSMC 180 nm MS/RF CMOS technology. The layout area of each diode is $1.6 * 10^{-11} m^2$.

The drawback of this structure is the presence of the parasitic N-well/P-sub diodes shown in Figure 2-9. Since there is always a voltage difference across these diodes, there will always be some leakage current flowing through two of them, D_6 and D_7, drawn through the input pin. Thus, the leakage through the input pin can be substantially significant.

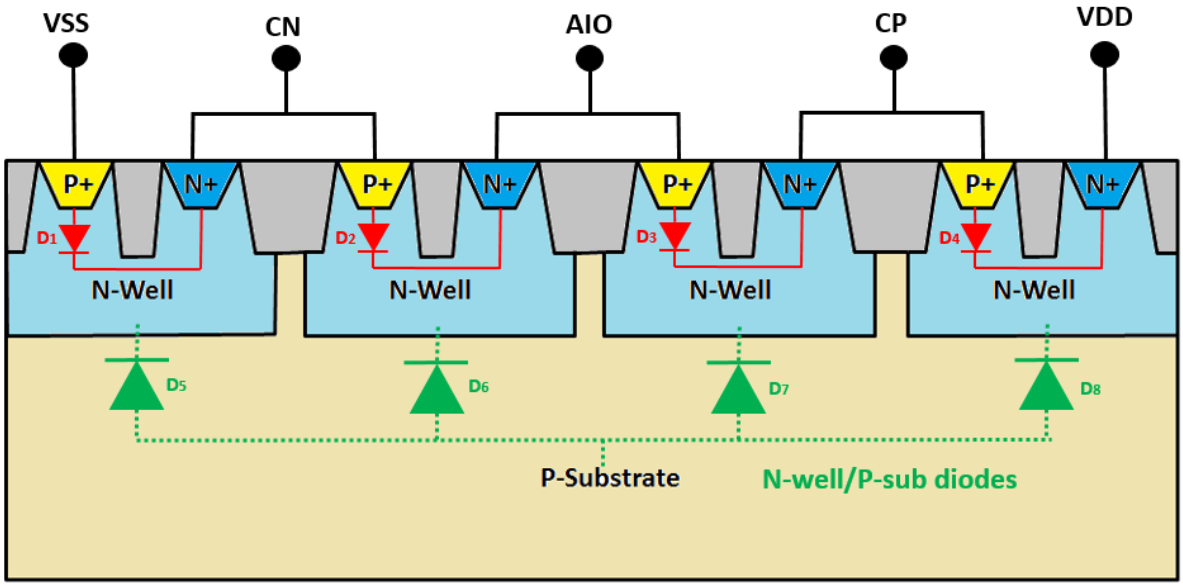


Figure 2-9: N-well/P-sub diode in P-diode

2.2.2. N-diode (N+/P-well diode)

To mitigate the leakage current of the parasitic N-well/P-sub diodes, a structure using N+/P-well diodes is proposed. Figure 2-10 shows the cross-section of a string of four N+/P-well diodes, each sitting in a Deep-N-well to reduce the leakage current.

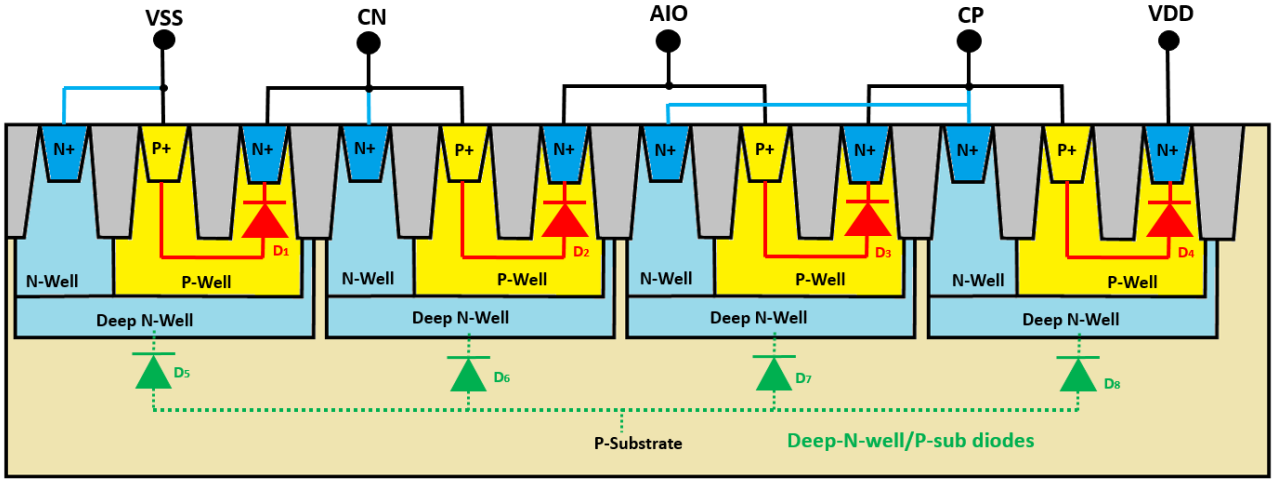


Figure 2-10: Cross Section of an N+/P-well diode

Here, the parasitic N-well/P-sub diode shown in Figure 2-9 doesn't exist. But the parasitic Deep-N-well/P-sub diode still exists. The Deep-N-well is now connected to the CP and CN nodes. Any leakage current due to the parasitic diodes will now be drawn from the CP and CN nodes and not the input node. Moreover, the Deep-N-well layer has a higher doping level than the N-well, the leakage current itself is reduced.

2.3. HBM (Human Body Model) stress test for the ESD diode structure

The human interactions with the chip are a major source of ESD failure. These interactions may include those during fabrication, packaging, and characterization. One method to test the reliability of chips is using the Human Body Model (HBM) [4]. Here, a 1.5kΩ and 100pF RC network is paired up with an ESD gun through which a voltage of 2kV (0.2uC) can be applied. The human, source of charge, is represented by the 100pF capacitor. The fingers of humans, discharge path, is represented by the 1.5kΩ series resistance. The circuit should be able to handle the resulting transient current of 1.3A $\left(\frac{2kV}{1.5k\Omega}\right)$. The equivalent circuit for the HBM model is shown in Figure 2-11 [4]

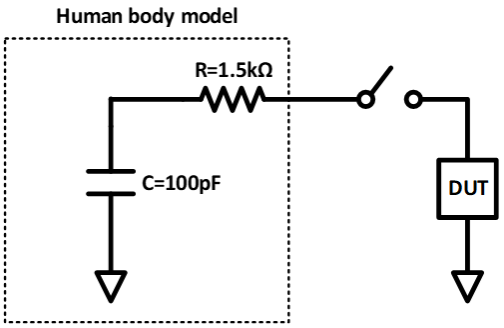


Figure 2-11: RC equivalent circuit for HBM model of ESD

As described by Prof. Drew Hall and his students, the stacked ESD diodes (P+/N-well diodes) went through an ESD stress test, starting at 200V for each pad. These stacked diode structures showed robustness up to 6kV, thus proving that they meet the HBM requirements for IC components.

2.4. Characterization of stacked diode structure using an external buffer

Due to the large safety margins present in the models, the leakage current of bootstrapped ESD diode structure cannot be accurately estimated from simulations. To accurately characterize the diodes' leakage current, the two diode structures were fabricated and connected to an external buffer setup, as shown in Figure 2-12. A low-input-current buffer with trimmable offset was obtained by cascading two buffer stages. The first is the ADA4530-1, an op-amp with a very low input current, maximum 20fA at room temperature [9]. This was combined with the OP27, whose offset can be easily trimmed from -8mV to +8mV using its trimming inputs and a potentiometer. A Keithley 6514 electrometer is used to measure current up to fA level. The electrometer's input is connected to the test PCB through a Triax cable that connects the 'Hi' terminal of the electrometer to the input of the ADA4530-1 op-amp on the PCB.

The main aim of the measurement set up is:

1. Measure the input leakage current of the diode circuit at room temperature for input voltage varying from 0V-1.8V
2. Measure the input leakage current for offset ranging between ± 8mV for input voltages varying from 0V-1.8V

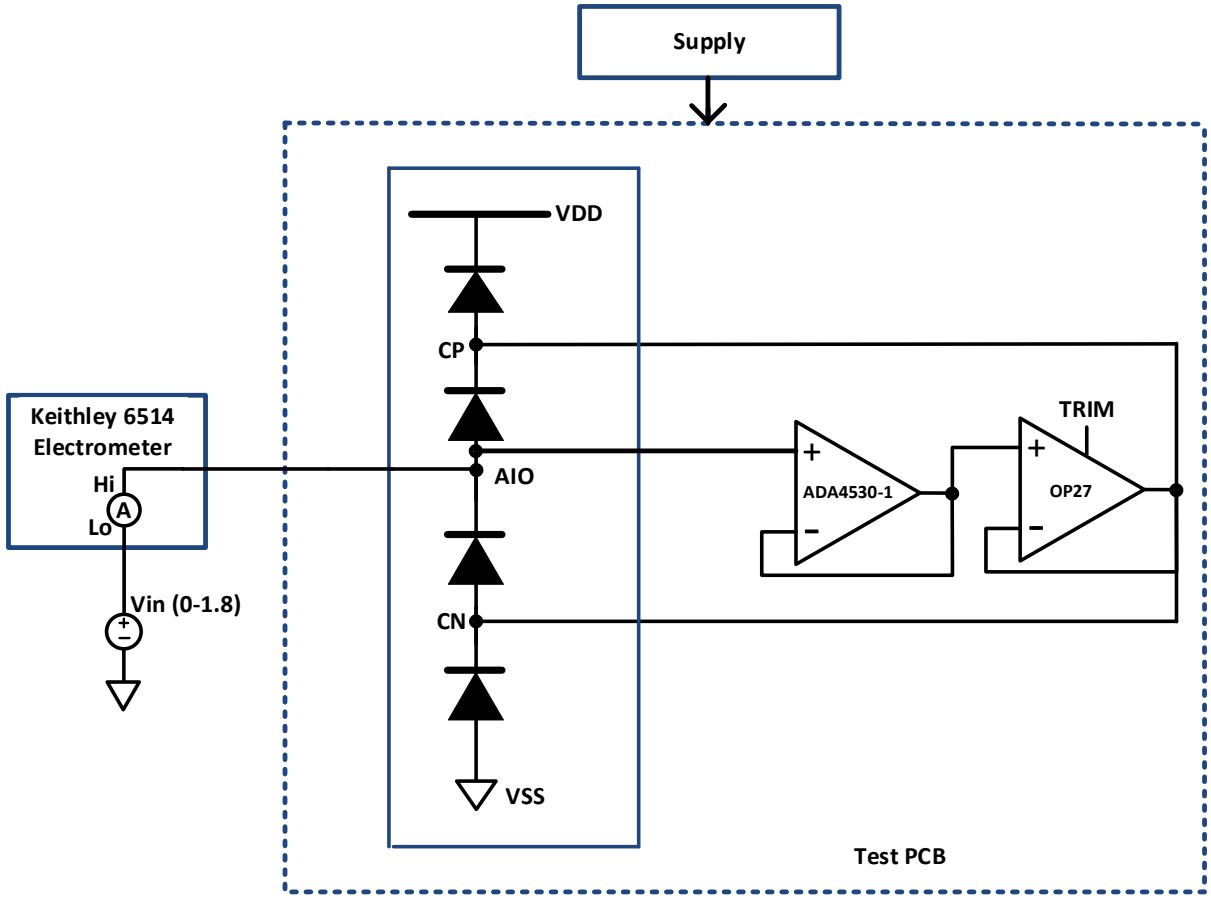


Figure 2-12: Measurement Setup

Figure 2-13 shows the photo of the test PCB with the chip. To avoid leakage from the board, the package's input pin is ‘airlifted’ and connected to a Teflon standoff.

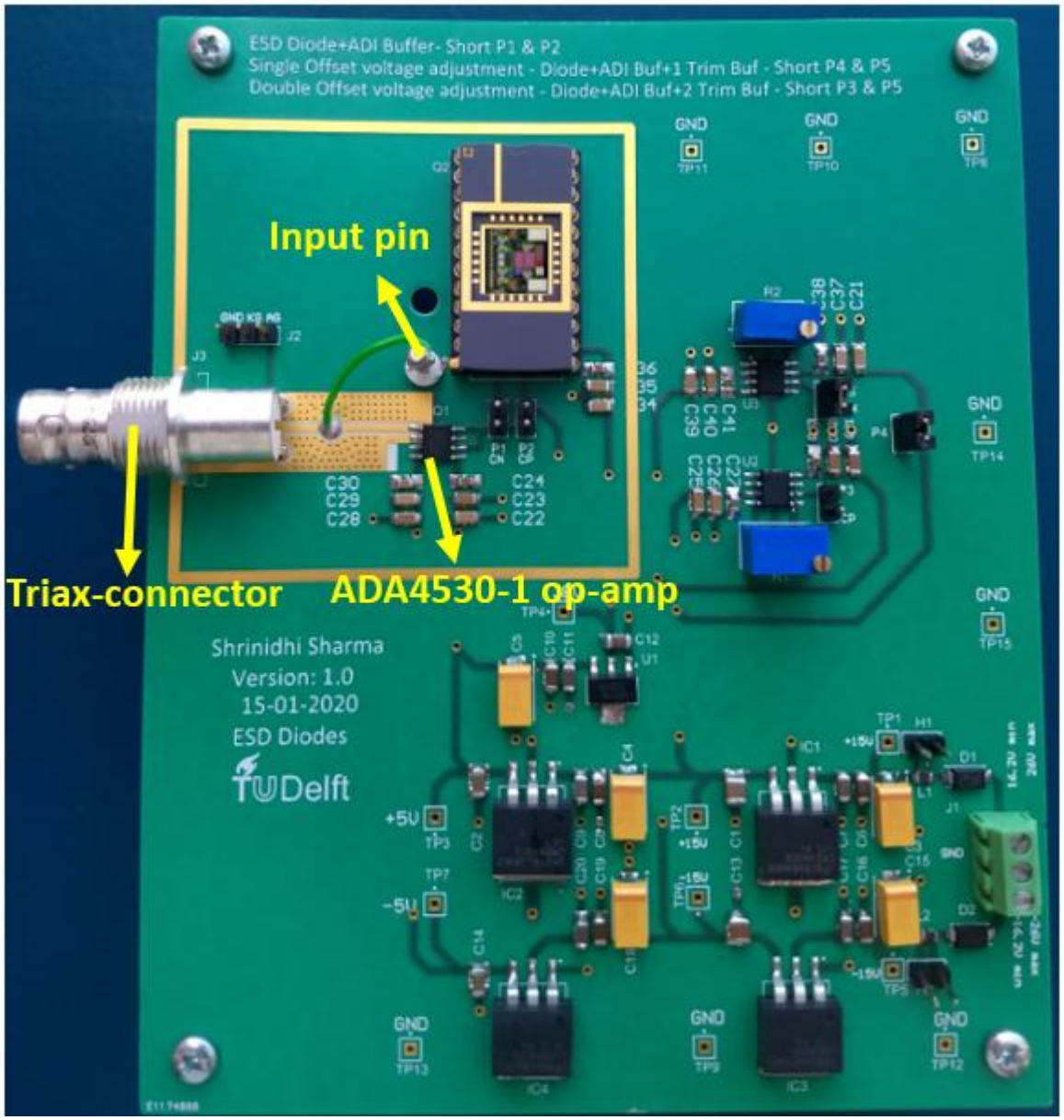


Figure 2-13: Test PCB with the Chip

The connection to the board (input of the ADA4530-1 op-amp) is through a wire. More details regarding the PCB for low leakage measurements are described in Chapter 4.

Procedure for the Measurement Setup:

a. Place the PCB in a metal box and cover it with a lid for shielding
b. The test set up for Keithley 6514 electrometer:
   i. Enable Zero Check
   ii. Perform Zero Correction
   iii. Set the range to 20pA and display resolution to $6\frac{1}{2}$ digits
   iv. Set integration Rate to 5PLC (Power Line Cycles)
   v. Select Repeating Filter
   vi. Enable Digital Filter and guard

c. The measurement data of the input leakage current obtained from Keithley is collected for 180 secs and averaged.

Usually, the input voltage should be varied between 0V-1.8V. However, measurements were made only up to 1.6V due to the limitation of the measurement set up. Here, the input voltage has been varied using a potentiometer connected to a battery. With a single battery, it was possible to vary the input voltage only up to 1.6V.

Measurement results

First, the leakage current was measured without the chip but including all other components present on the PCB. As shown in Figure 2-14, the PCB leakage is low enough that any measured leakage above 20fA can be attributed to the chip with the ESD structure.

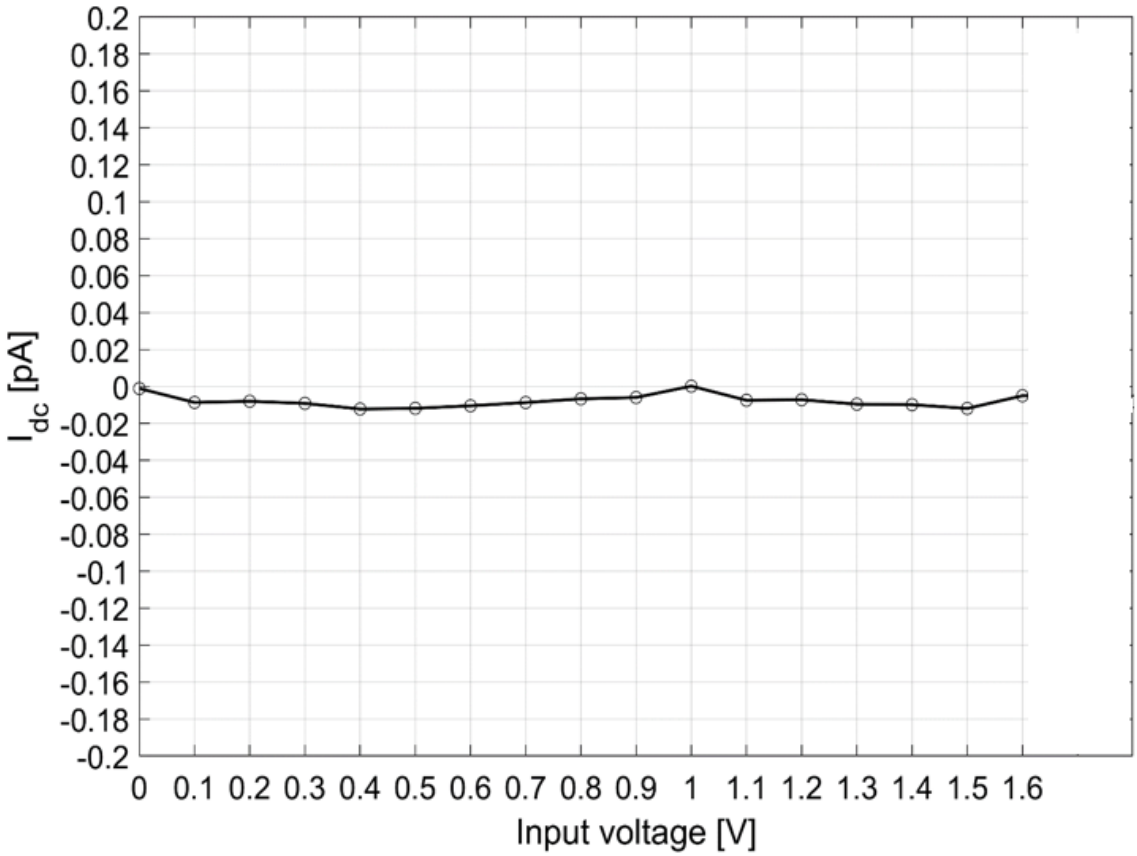


Figure 2-14: Plot of measured leakage current of the PCB with other components and without the chip

Next, the leakage current was measured with the chip present for both P-diodes and N-diodes. The input leakage current was measured for three different offset voltages for the buffer that is bootstrapping the diodes: i.e., 0mV, -8mV, +8mV. Figure 2-15/Figure 2-16 shows the measured graph for three different offset voltages and input voltage varying from 0V to 1.6V for the P-diodes/N-diodes.

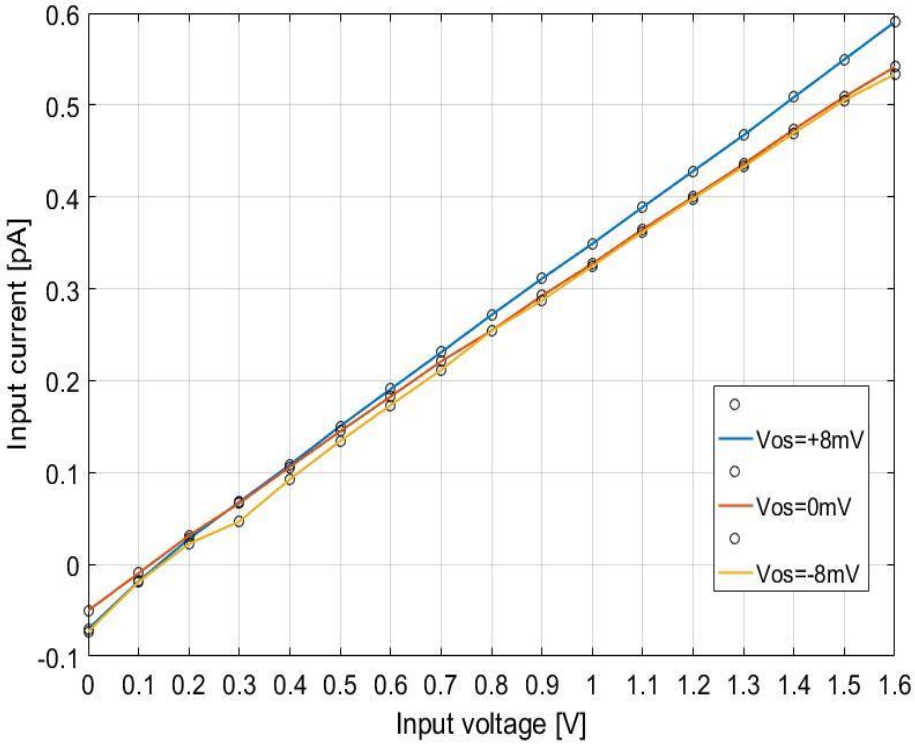


Figure 2-15: Plot of measured input leakage current for three different offset voltages of P-diodes

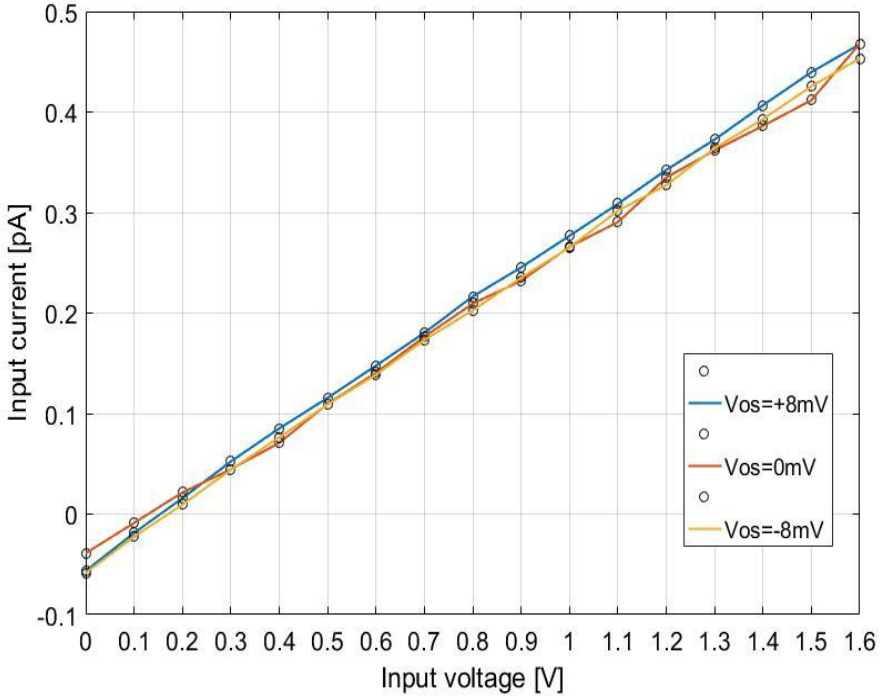


Figure 2-16: Plot of measured input leakage current for three different offset voltages of N-diodes

In both cases, the input current increases with the input voltage, while the buffer offset has an insignificant impact. The maximum difference is approximately 50 fA. At an input voltage of 1.6V, the input current reaches a maximum of 0.6pA, which

corresponds to a resistance of 3TΩ $\left(\frac{1.6V}{0.6pA} = 3T\Omega\right)$, a stray leakage path. Figure 2-17 shows the chip diagram with the PAD connections.

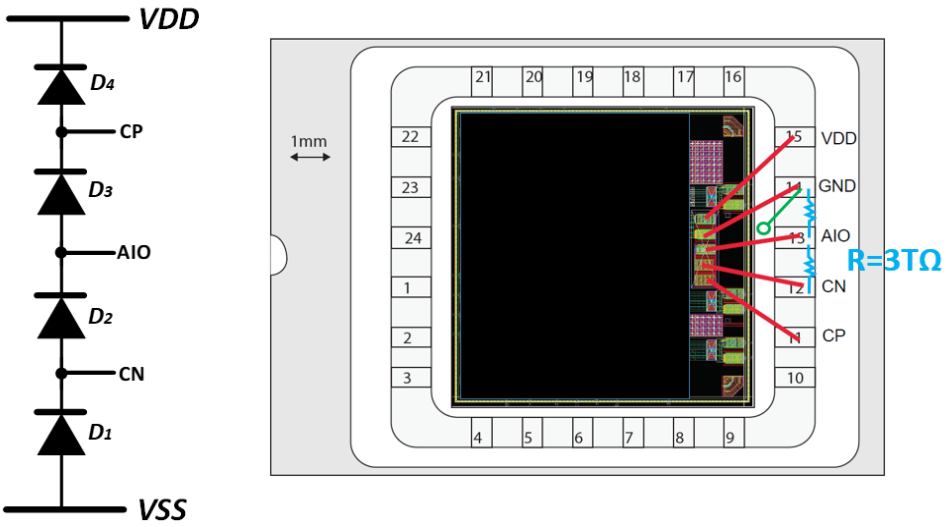


Figure 2-17: Chip Diagram

In the above chip diagram, the input pin AIO is placed next to the GND and CN pins. Therefore, this leakage is suspected to be coming from the parasitic resistance between adjacent pads on a package. To determine the leakage path and check if the leakage is because of the pin's proximity in the package, the measurement was done on the empty packages. This removes the leakage due to the chip and just leaves the package leakage. Figure 2-18 shows the pin configuration of the package with the chip.

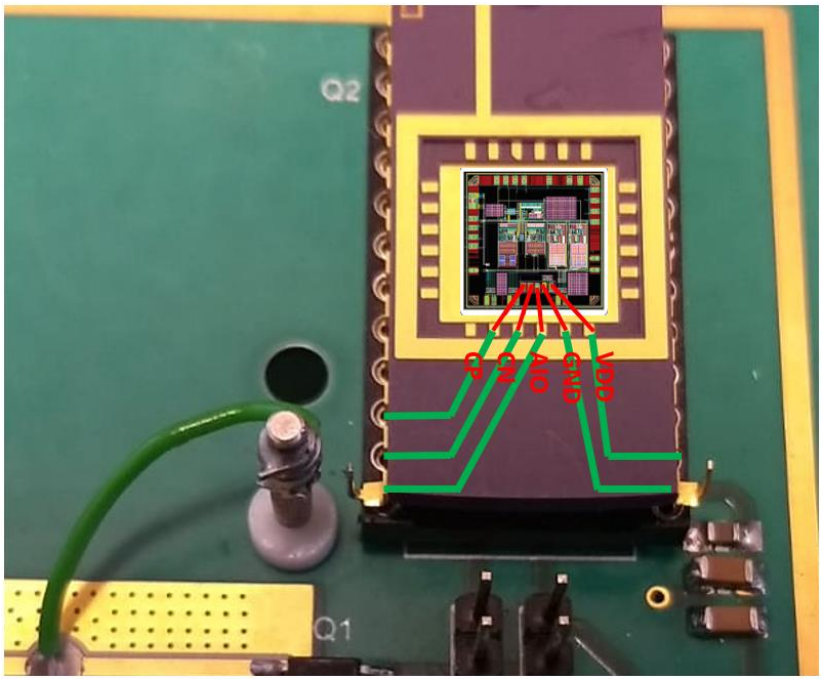


Figure 2-18: Package pin connection with the chip

The same pin configuration was used for the empty package, as shown in Figure 2-18, and the leakage current was measured.

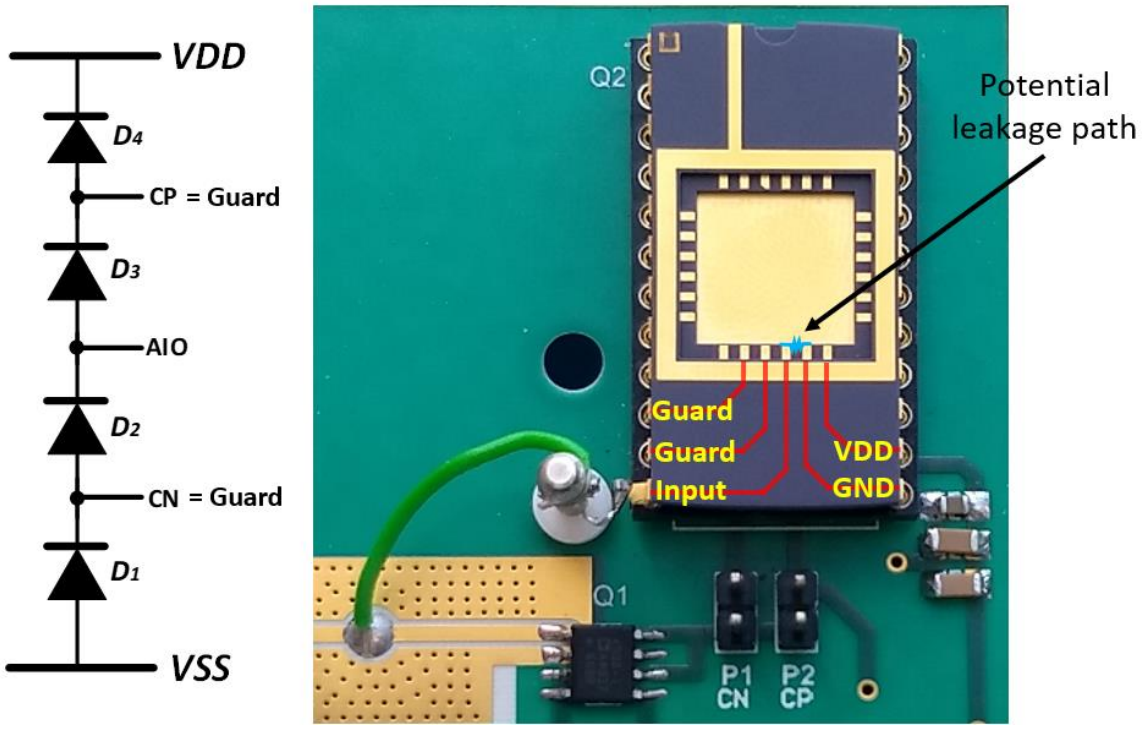


Figure 2-19: Empty package measurements with the same pin configuration

Figure 2-20 shows the graph of the measured leakage current of the empty package vs. input voltage.

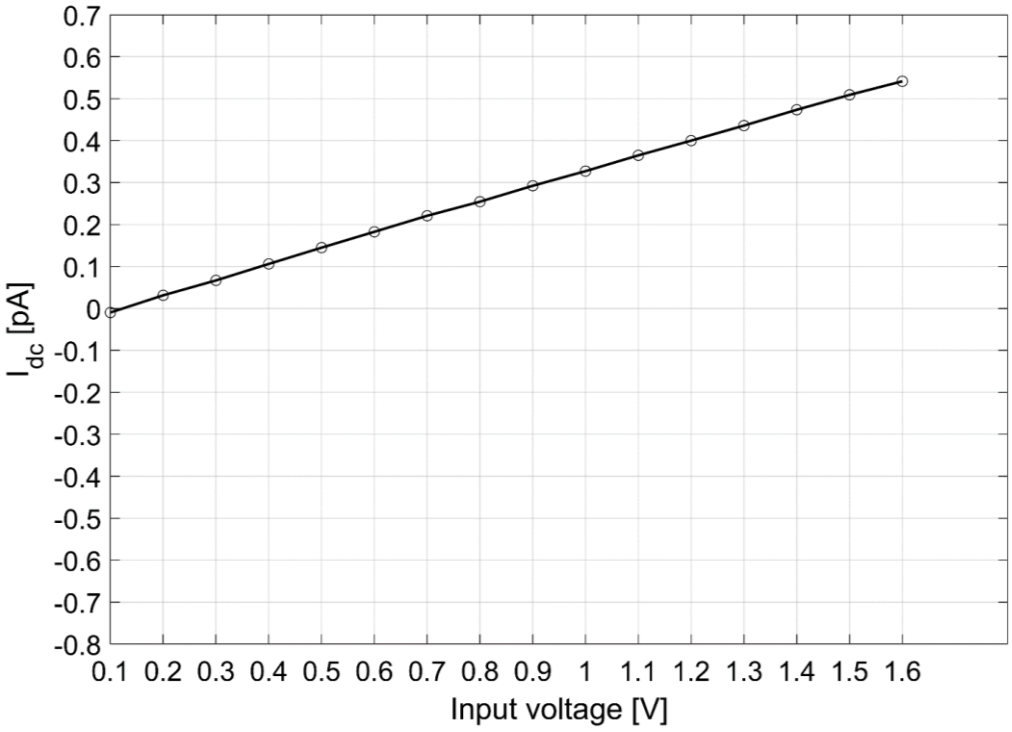


Figure 2-20: Plot of measured input leakage current of the empty package

The graph shows that the input leakage current is input voltage-dependent. This result confirms that the leakage seen in Figure 2-15 and Figure 2-16 is due to the

parasitic resistance. The leakage path between the Input pin and GND within the package at high input common-mode voltages is of the order of 3TΩ resistance (shown in Figure 2-19).

To confirm this result, another experiment was done with an empty package with improved pin configuration. The input pin is surrounded by guard pins (CP and CN) on both sides to minimize leakage, as shown in Figure 2-21. The leakage can be significantly suppressed, as shown in Figure 2-22

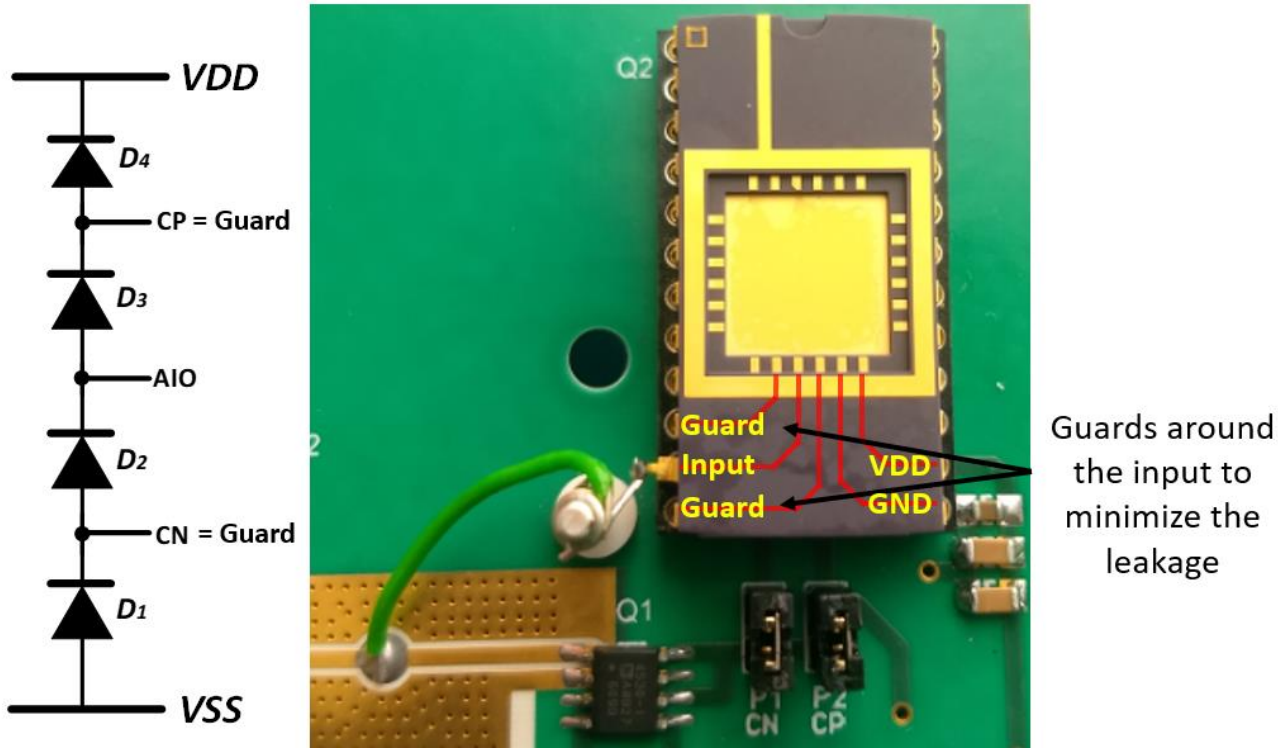


Figure 2-21: Empty package with improved pin configuration

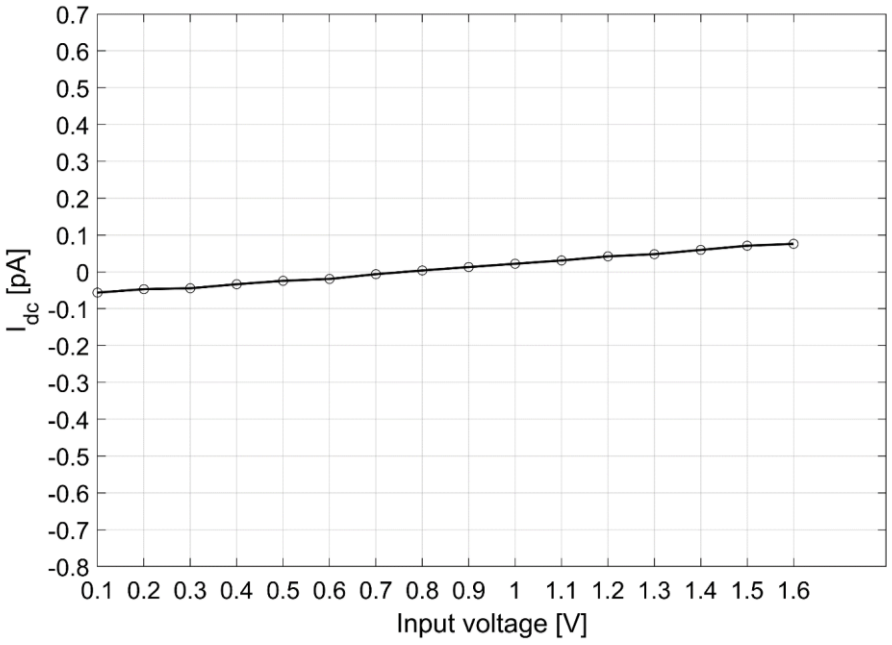


Figure 2-22: Plot of measured input leakage current of the improved pin configuration

As a consequence of guard pins, the input current reduces from 500fA to 100fA. However, the 100fA maximum input current is still high for the targeted application. Expected leakage from stray paths needs to be significantly less than 50fA which is the ESD structure's expected leakage. Further, an experiment was done with double guarding around the input pin, as shown in Figure 2-23. Also, the outer metal ring of the package was connected to the guard pin using a wire. The results are shown in Figure 2-24.

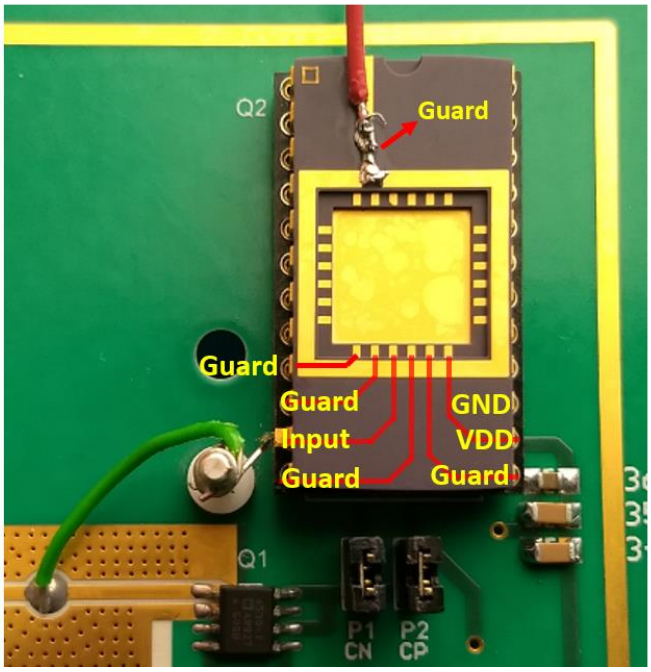


Figure 2-23: Package with double guarding around the input pin and outer metal ring connected to the guard pin

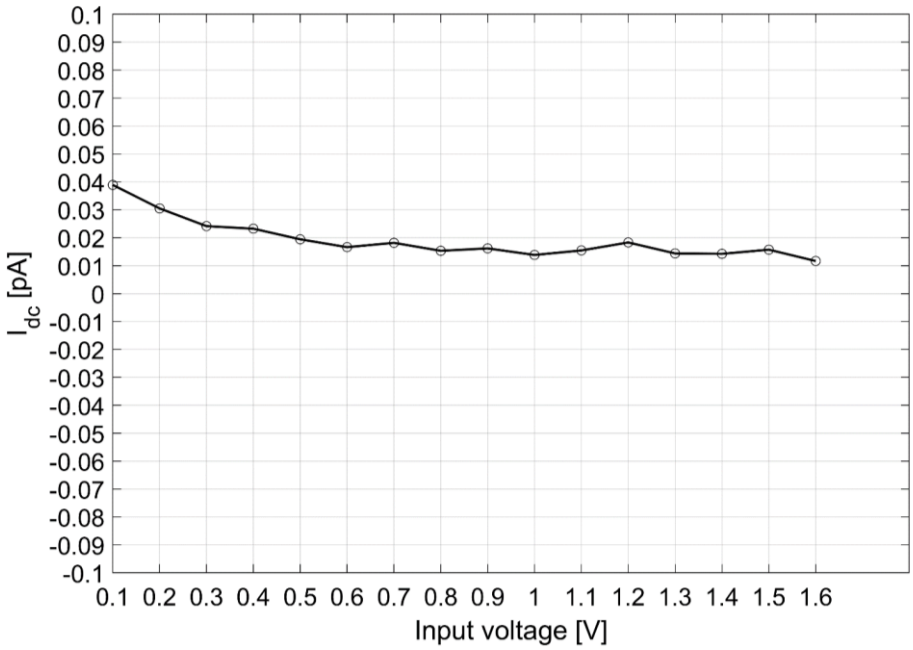


Figure 2-24: Plot of measured input leakage current with double guarding around the input pin and outer metal ring connected to the guard pin

This shows a reduced input leakage current less than 40fA for the Input Common-Mode Range (ICMR) from 0V-1.6V. This is within the acceptable range for the targeted application.

These techniques were implemented in the next tapeout and measurement of the input leakage current of bootstrapped ESD diode described in Chapter 5.

2.5. Specifications for On-Chip Auxiliary Buffer Design

The design requirements for the auxiliary buffer are derived from measurement results presented in Section 2.4 and are described below:

- Since little difference was observed in leakage current for offsets up to 8mV, the limit for the error in the buffered voltage was set to 8mV. With a supply voltage of 1.8V, and an offset of 8mV, this corresponds to a DC gain of 47dB (gain= 20*log (1.8/8m) =20*log (225) =47dB). This error of 8 mV can be equally divided between the acceptable input offset voltage and the limited DC gain. This leads to a specification for the offset voltage of 4mV and a DC gain of 53dB.
- The load capacitor's specification that the auxiliary buffer should drive is set to 10pF, considering 3pF for coaxial cables, 6pF for bonding wires, and 1pF for PCB routings.
- The total current drawn from the supply by the AZ amplifier is 210uA [7]. To have a small effect on the total current consumption, the auxiliary buffer's current budget is set at 1/10th of that of the AZ amplifier. This leads to a specification for the current consumption of 20uA.
- The Unity Gain Bandwidth (UGB) of the AZ amplifier is around 1.4MHz [7], the UGB of the auxiliary buffer is set at 1/10th of that of the AZ amplifier. This leads to a UGB of the auxiliary buffer of 140kHz.

Table 1 below summarizes all the specifications of the Auxiliary buffer.

Table 1: Auxiliary Buffer Specifications

Parameter Name	**Value**
Input Offset Voltage	≤ 4mV
DC Gain	53dB
Input Swing	0V-1,8V
Output Swing	0,1V-1,7V
Load Drive Capability (Capacitive)	10pF
Phase Margin	60° (min) at 140kHz (UGB)
Supply Voltage	1,8 V
Supply Current	20µA
Die area	As low as possible
Temperature range	-40°C to + 85°C

3. On-Chip Buffer Design

This chapter presents the design of a rail-to-rail input-output buffer (auxiliary buffer) based on the specifications shown in Table 1.

3.1. Rail-to-Rail Input Stage

The input stage's main goal is to amplify the differential input signals applied at its inputs while rejecting the common-mode signals. *Rail-to-rail* indicates that the output follows the input even when the input voltage swings from one supply rail to another. The rail-to-rail input stage will maximize SNR and signal range. The rail-to-rail input stage is used in buffer amplifiers shown in Figure 3-1. In buffer amplifiers, if the input is going from rail to rail, e.g., from VSS (0V) to VDD(1.8V), then due to the virtual ground, the output signal should also go from rail to rail[10].

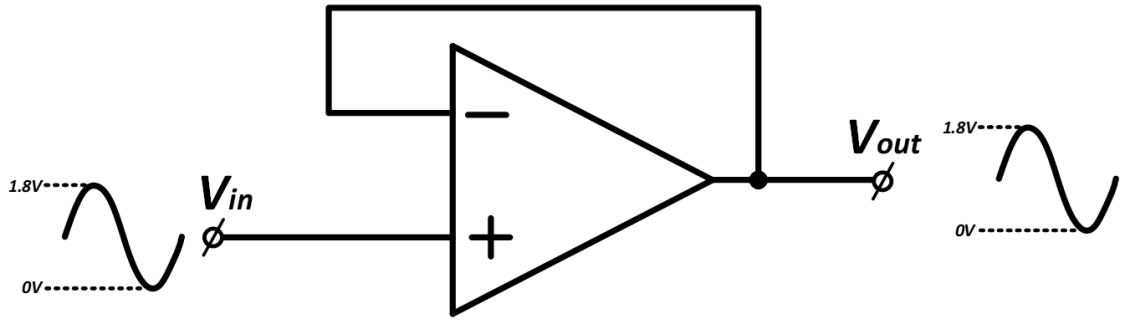


Figure 3-1: Buffer Amplifier

There are different ways to realize rail-to-rail input stages. Some examples are discussed below.

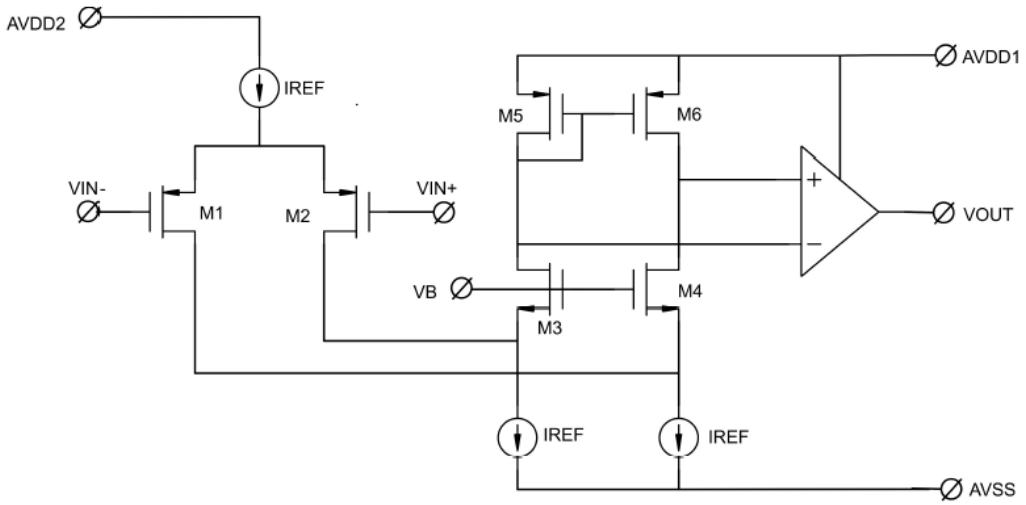


Figure 3-2: Rail-to-Rail input stage using two supply voltages [10]

Figure 3-2 [10] shows a folded-cascode input stage with two supply voltages AVDD1 and AVDD2. The maximum voltage that input common-mode can reach is

limited to AVDD2-$V_{GSP1,\ 2}$-$V_{DSAT,\ IREF}$. Here, $V_{GSP1,\ 2}$ is the gate-source voltage of transistor M_1 and M_2, respectively; $V_{DSAT,\ IREF}$ is the saturation voltage of the current source I_{ref}. When AVDD2 and AVDD1 are equal, the input voltage cannot swing from rail to rail. If AVDD2>AVDD1+$V_{GSP1,2}$-$V_{DSAT,\ IREF}$, the input voltage can go rail to rail with a simple PMOS input differential pair. However, this would require two supply voltages.

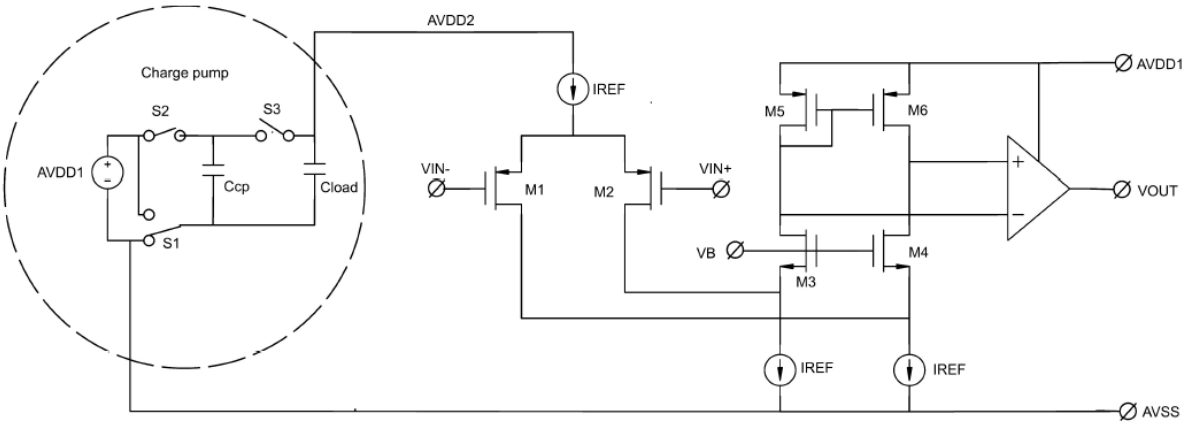


Figure 3-3: Rail-to-Rail input stage using charge pump[10]

A charge pump is often used to generate the boosted supply voltage, as shown in Figure 3-3. However, the drawback of using a charge pump is the increased area and power consumption. The charge pump in [11] consumes an area of 0.1mm^2 , while the op-amp area is 0.4mm^2. To achieve low cost, two supply voltages are not preferred.

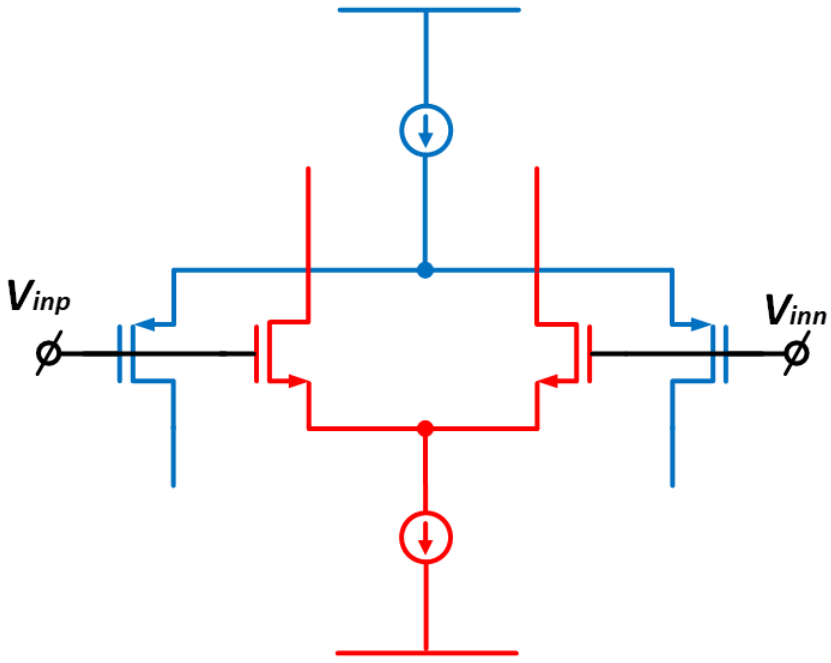


Figure 3-4: Rail-to-rail input stage

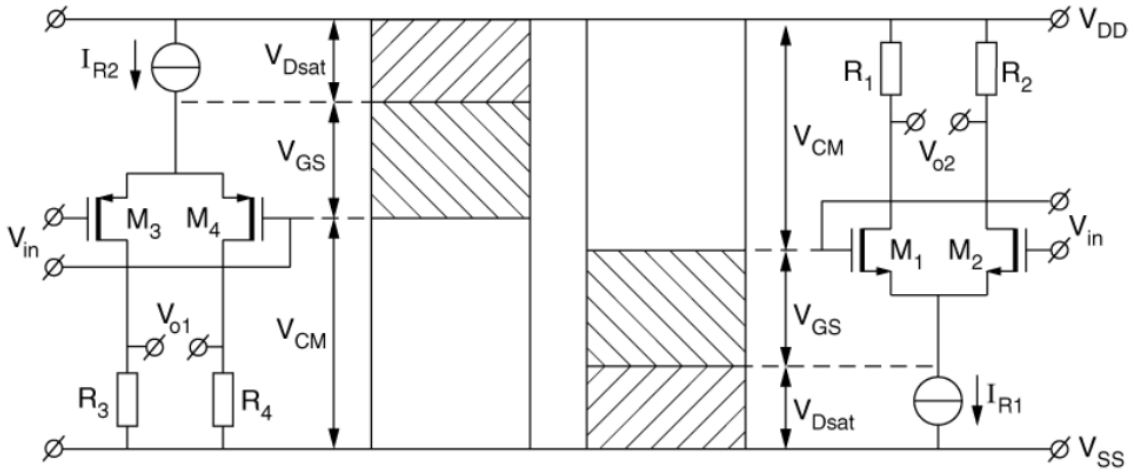


Figure 3-5: Common-mode input voltage range of a P-channel and an N-channel input stage[10]

Another rail-to-rail solution is achieved by connecting a PMOS and an NMOS in parallel, as shown in Figure 3-4. As shown in Figure 3-5, the PMOS transistors M_3 and M_4 will be ON in the lower ICMR from V_{SS} to V_{DD}-V_{Dsat}-V_{GS}. The NMOS transistors M_1 and M_4 will be ON for the upper ICMR from V_{SS}+V_{Dsat}+V_{GS} to V_{DD}, where V_{Dsat} is the saturation voltage of the transistor implementing the current source I_{R1} and I_{R2}. These two input stages were put in parallel, as shown in Figure 3-4. This input stage requires a supply voltage of at least V_{SS}+2V_{Dsat}+2V_{GS}.

One of the drawbacks of this input stage architecture is that the transconductance is not constant over the ICMR. At low ICMR, the PMOS is ON, while at high ICMR, the NMOS is ON. In the middle of the ICMR, both the PMOS and the NMOS are ON. This implies that gm in the middle of ICMR is two times the value of gm at low/high ICMR as shown in Figure 3-6, which impedes optimal frequency compensation.

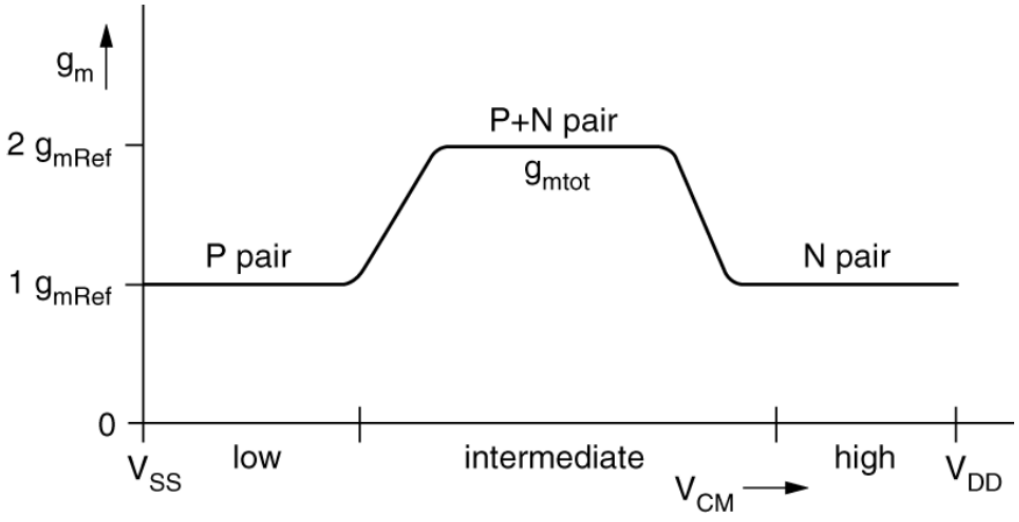


Figure 3-6: Variation of gm over the ICMR[10]

A constant g_m, over a rail-to-rail ICMR, can be obtained by:

- Keeping the sum of the tail currents of the input transistors constant, which are biased in weak inversion. [12] [13].

- Keeping the sum of the square roots of the tail current of the input transistors constant, which are biased in strong inversion. Here the gm varies by 40% over the ICMR [10].
- Using Zener diodes to make the total gm of the input pairs constant. Here the gm varies by 5% over the ICMR [10].
- Using the current spill-over technique. Here the input transistors are biased in weak inversion. The gm varies by less than 2% over the ICMR.

This design employs the current spill-over technique because of its minimal gm variation over the ICMR, faster transition from PMOS to NMOS, and simple implementation.

3.1.1. The current spill-over gm control input stage

The current spill-over gm control input stage circuit is shown in Figure 3-7.

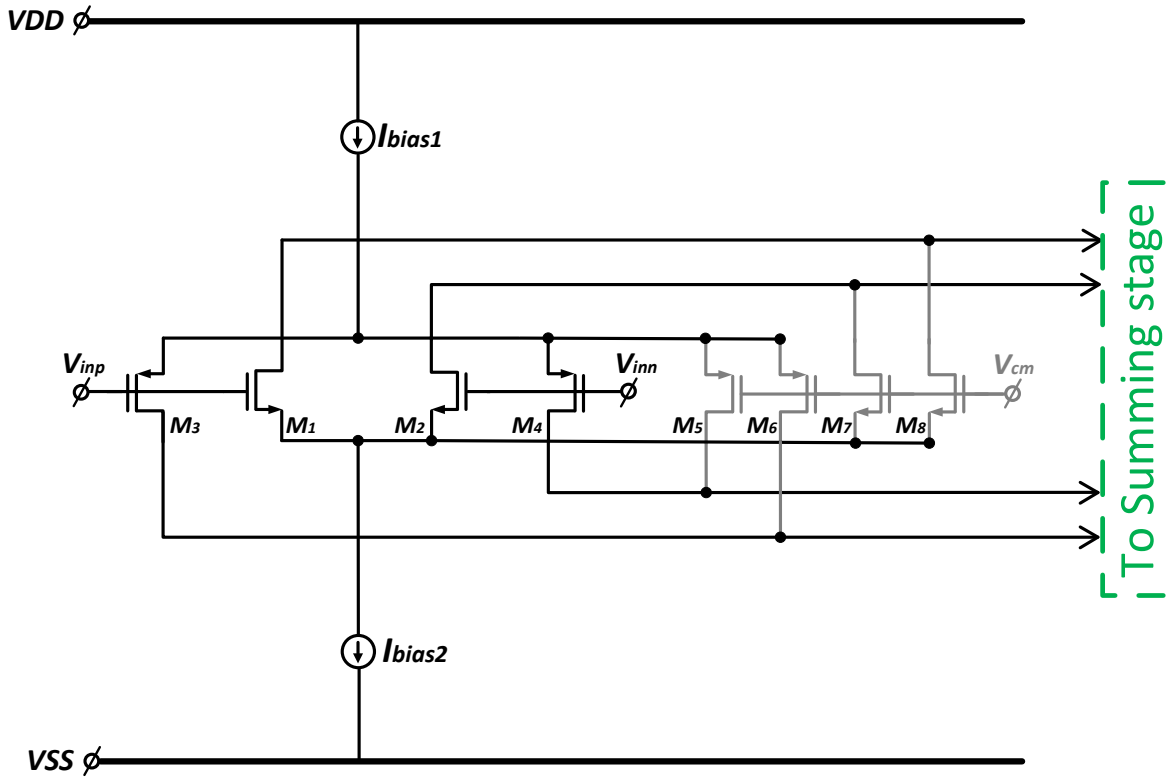


Figure 3-7: Current spill-over input stage

Here M_1, M_2 are the NMOS input transistors, M_3, M_4 are the PMOS input transistors. M_5, M_6, M_7, and M_8 are the switching transistors used to spill the current to the summing stage. These switching transistors are biased at an input voltage of 0.9V, denoted by V_{cm}. To keep a constant current in the output stage, the drains of the switching transistors M_5-M_8 are connected to the drains of the input transistors M_1-M_4, as shown in Figure 3-8. This puts the switching transistors parallel to the input transistors and spills the current to the appropriate summing node that biases the output stage.

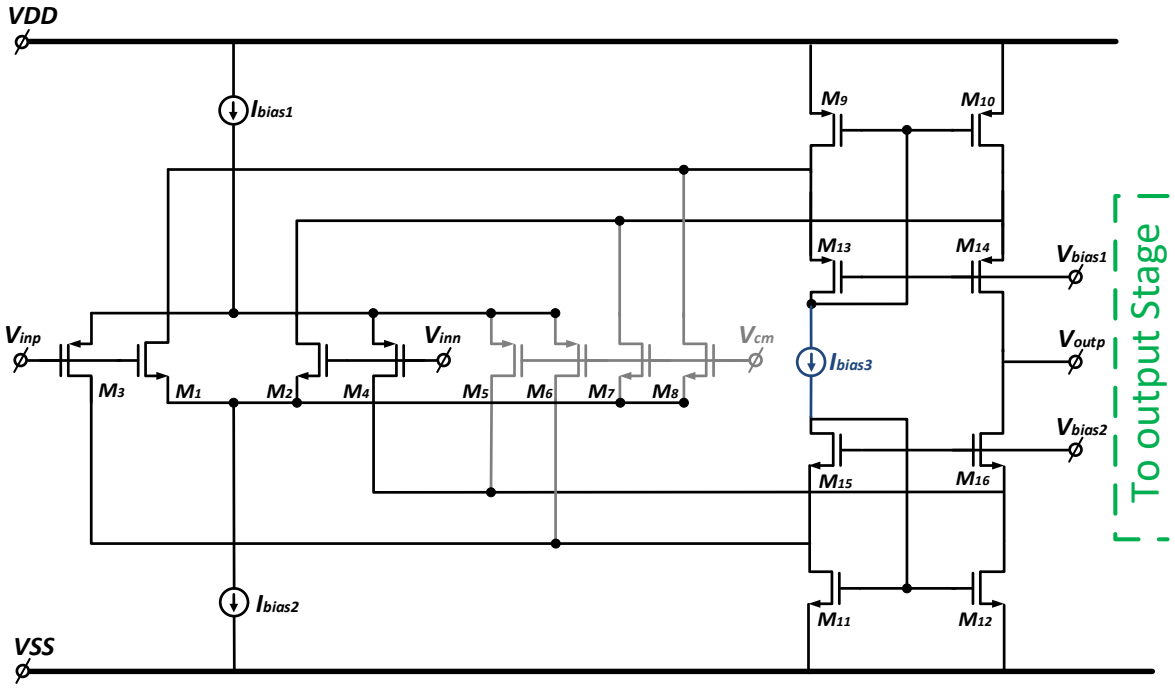


Figure 3-8: Rail-to-rail input stage with the summing circuit

3.1.2. Summing Circuit

In the summing circuit shown in Figure 3-9, there are two current mirrors, the PMOS current mirror formed by M_9-M_{10} and the NMOS current mirror formed by M_{11}-M_{12} which are biased by the floating current source I_{bias3}. In this way, the noise and the offset of the current mirrors are cancelled. I_{bias3} keeps the current in the summing circuit constant irrespective of the current flowing from the input stage. This will help in maintaining constant quiescent in the output stage. The floating current source is implemented by two head to tail connected transistors M_{17} and M_{18}, as shown in Figure 3-9

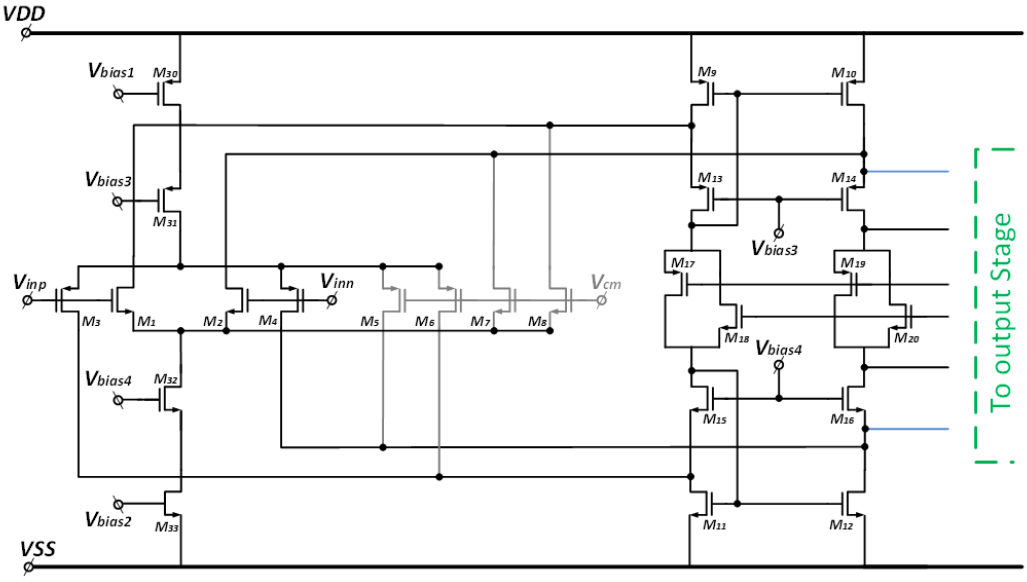


Figure 3-9: Rail-to-rail input stage with the floating current sources in the summing circuit

Cascode transistors M_{13} to M_{16} are present to increase the DC-gain.

3.1.3. Sizing of the input stage and the summing circuit

An important parameter of the input stage is the input offset voltage. Offset is mainly caused by the mismatch in the threshold voltage (Vth) and current-factor (beta) of transistors. To see the dominant contributors of the offset in the input stage, consider the folded-cascode input stage shown in Figure 3-10.

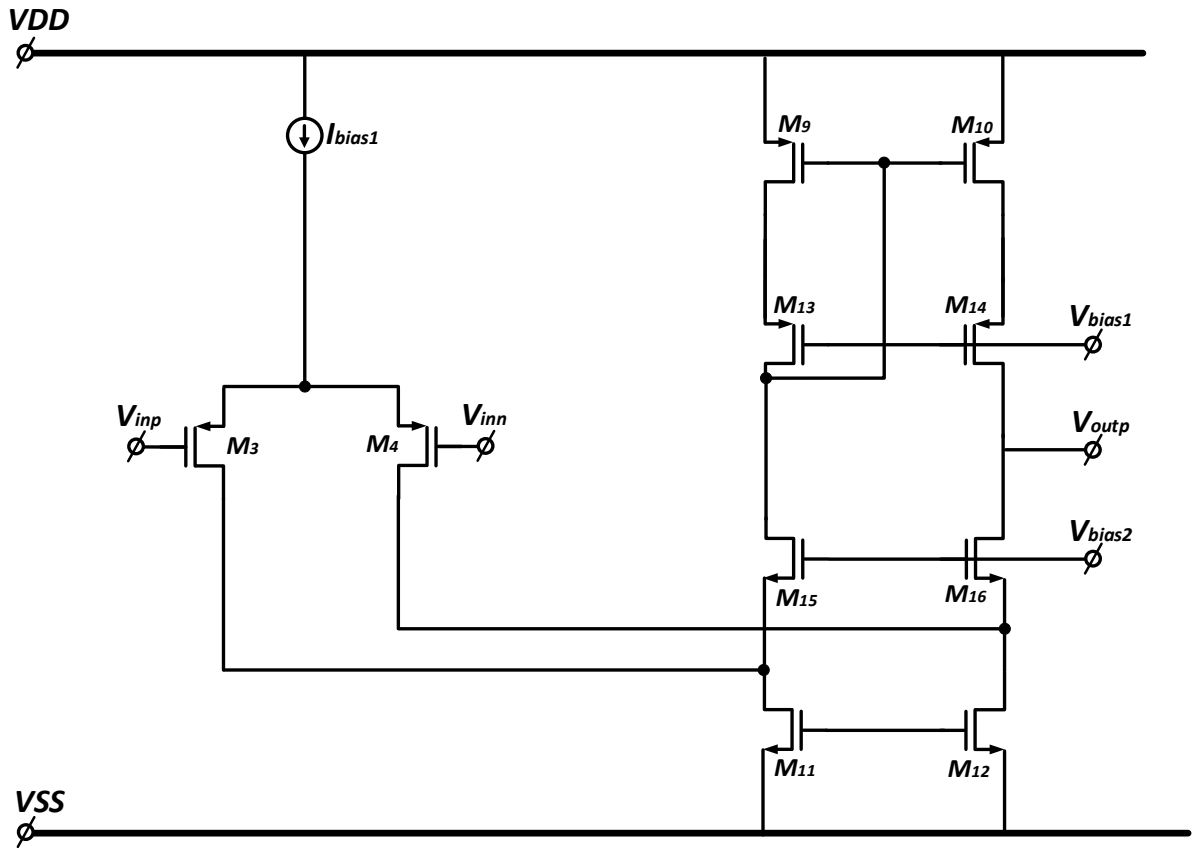


Figure 3-10: Folded cascode input stage

The offset of the folded-cascode input stage can be determined from the following equation:

$$V_{os} = \Delta V_{th1} + \frac{g_{m2}}{g_{m1}}\Delta V_{th2} + \frac{g_{m3}}{g_{m1}}\Delta V_{th3} + \frac{1}{g_{m1}}\left(\frac{\Delta\beta_1}{\beta_1} + 2 * \frac{\Delta\beta_2}{\beta_2} + \frac{\Delta\beta_3}{\beta_3}\right) \quad (3.1)$$

where ΔV_{th1}, ΔV_{th2}, ΔV_{th3} is the mismatch between the threshold voltages of M_3 and M_4, M_{11} and M_{12}, M_9 and M_{10}. g_{m1}, g_{m2}, g_{m3} is the transconductance of M_3 and M_4, M_{11} and M_{12}, M_9 and M_{10}. $\Delta\beta_1$, $\Delta\beta_2$, $\Delta\beta_3$ is the mismatch of the current-factor of transistors M_3 and M_4, M_{11} and M_{12}, M_9 and M_{10}. Equation 3.1 can be extended to equation 3.2 for a rail to rail input stage shown in Figure 3-8 assuming that the transconductance ($g_{m,\,in}$=g_{m1}+g_{m2}) remains constant over the ICMR.

$$V_{os} = \Delta V_{th1} + \Delta V_{th2} + \frac{g_{m2}}{g_{m,in}}\Delta V_{th2} + \frac{g_{m3}}{g_{m,in}}\Delta V_{th3} + \frac{1}{g_{m,in}}\left(\frac{\Delta\beta_1}{\beta_1} + 2 * \frac{\Delta\beta_2}{\beta_2} + \frac{\Delta\beta_3}{\beta_3}\right) \quad (3.2)$$

where ΔV_{th1} and ΔV_{th2} are the mismatch between the threshold voltages of PMOS and NMOS input pairs, g_{m1} is the transconductance of M_3 and M_4, g_{m2} is the transconductance of M_1 and M_2. From the above equation, it can be seen that the offset can be reduced by making the transconductance of the current mirrors and current sources small and making the transconductance of the input transistors large. For this reason, the input transistors were biased in weak inversion and had a large area to reduce the mismatch. The current sources and current mirrors were biased in strong inversion to have less gm than the input transistors.

The design was started by sizing the PMOS input transistor for an offset voltage of 4mV. The PMOS input transistors were biased in weak inversion. Later it was extended to a rail to rail configuration by placing PMOS and NMOS in parallel. The size of the PMOS is three times that of the NMOS to account for the lower mobility. For PMOS input pair M_3 and M_4, a width over the length of $\left(\frac{120}{1.2}\right)\mu m$ and for NMOS input pair M_1 and M_2, a width over the length of $\left(\frac{40}{1.2}\right)\mu m$ is used. The current mirrors M_9-M_{10}, M_{11}-M_{12} in the summing stage are biased in strong inversion with large length to reduce noise and offset. A maximum length of 20µm was chosen for this purpose for M_9-M_{10} and M_{11}-M_{12}. So, for M_9-M_{10}, a width over the length of $\left(\frac{4}{20}\right)\mu m$ and for M_{11}-M_{12} a width over the length of $\left(\frac{2.2}{20}\right)\mu m$ is used. Those sizes were derived from running Monte Carlo (MC) simulations to meet the offset specification. Figure 3-11, Figure 3-12, Figure 3-13 show the MC simulation of the buffer for input voltages V_{in}=0.1V, V_{in}=0.9V, V_{in}=1.7V, respectively

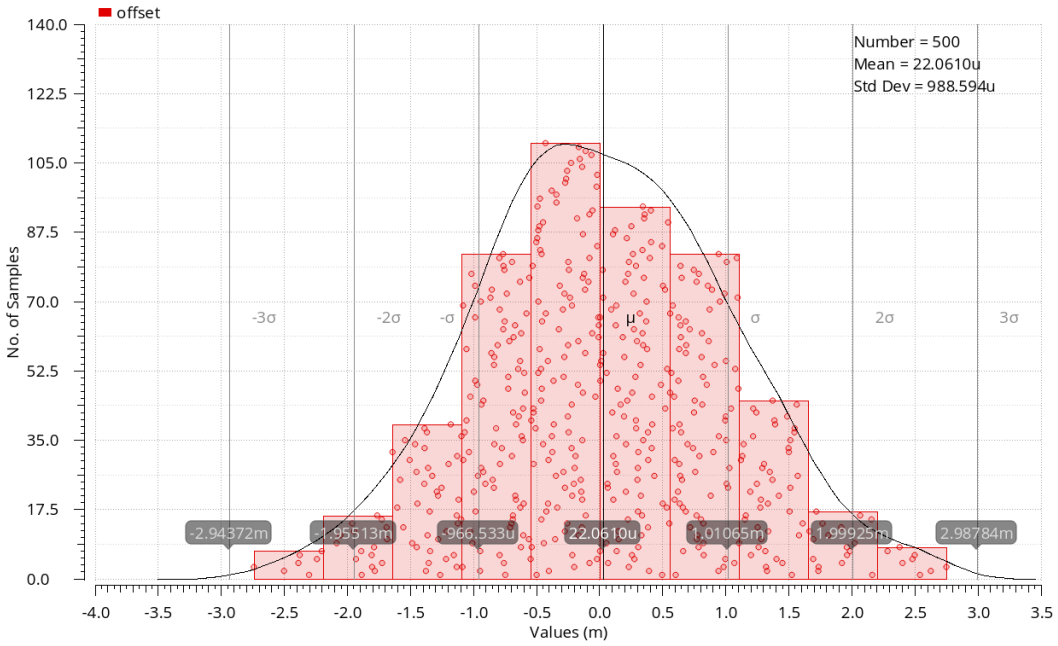


Figure 3-11: Monte Carlo simulation for Vin=0.1V

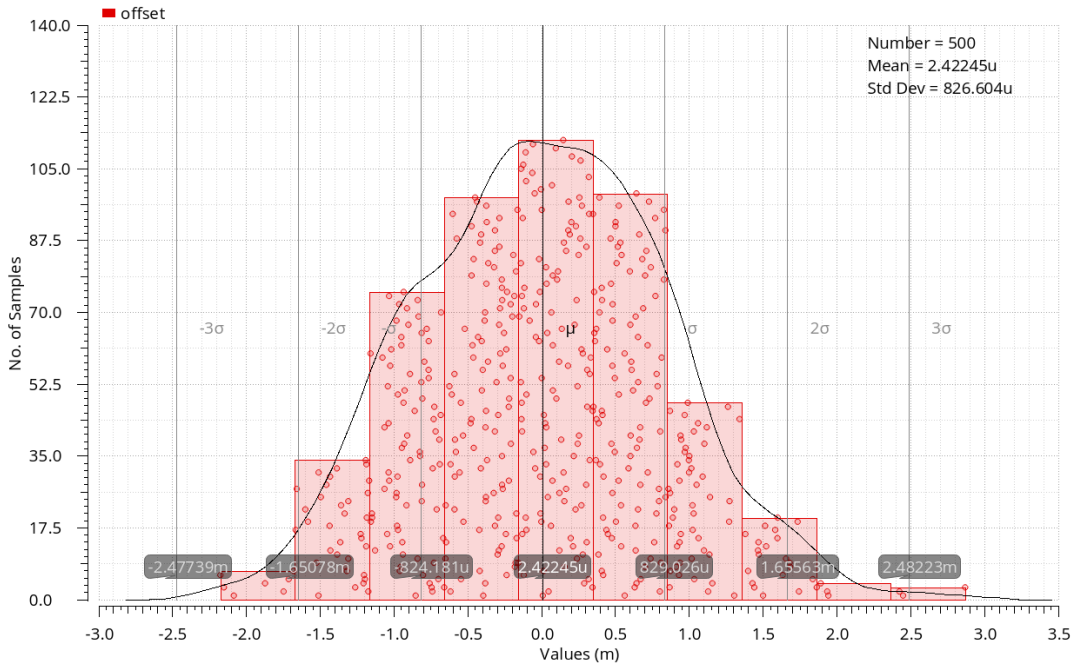


Figure 3-12: Monte Carlo simulation for Vin=0.9V

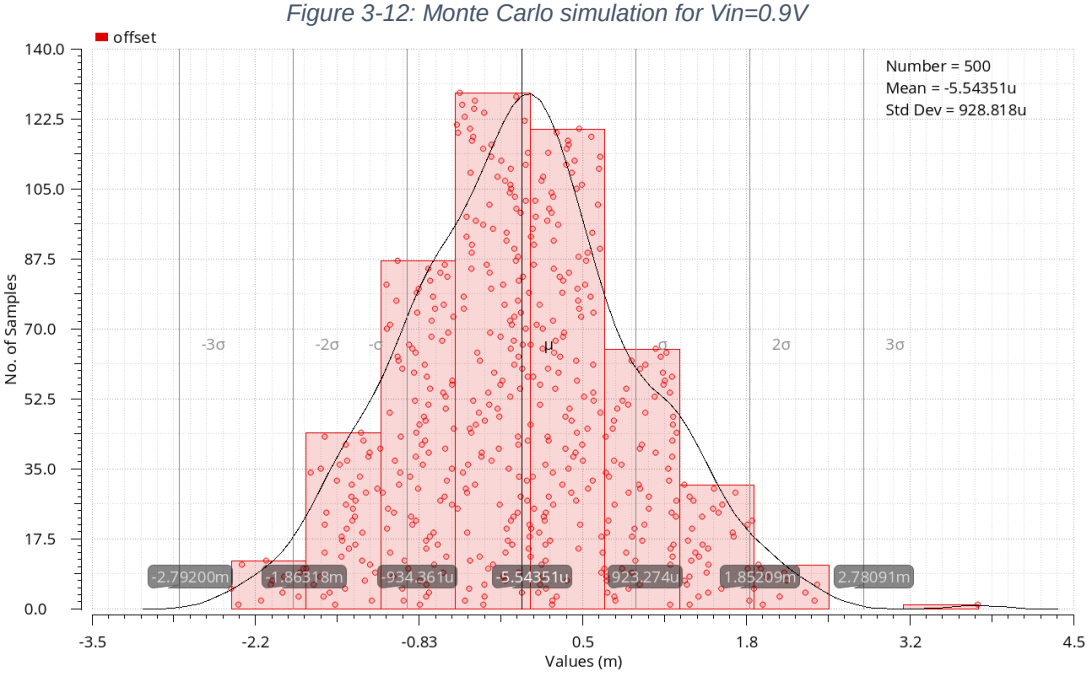


Figure 3-13: Monte Carlo simulation for Vin=1.7V

The three-sigma offset from MC simulations for V_{in}=0.1V, 0.9V, 1.7V is less than 4mV, which meets the specification described in Table 1. Usually, the offset for V_{in}=1.7V should be worse than the offset for V_{in}=0.1V because the NMOS transistors are smaller in size than the PMOS transistors. This behavior is not seen here because the offset here is dominated by the switching transistors due to the asymmetric spilling of current to the summing stage, resulting in an input common-mode voltage-dependent offset. The systematic offset is relatively low here due to the floating current source's presence in the summing circuit because it makes the current in both the PMOS and NMOS current mirrors equal. The offset was also simulated for different corners and temperatures after the post layout simulations and is shown in Figure 3-14.

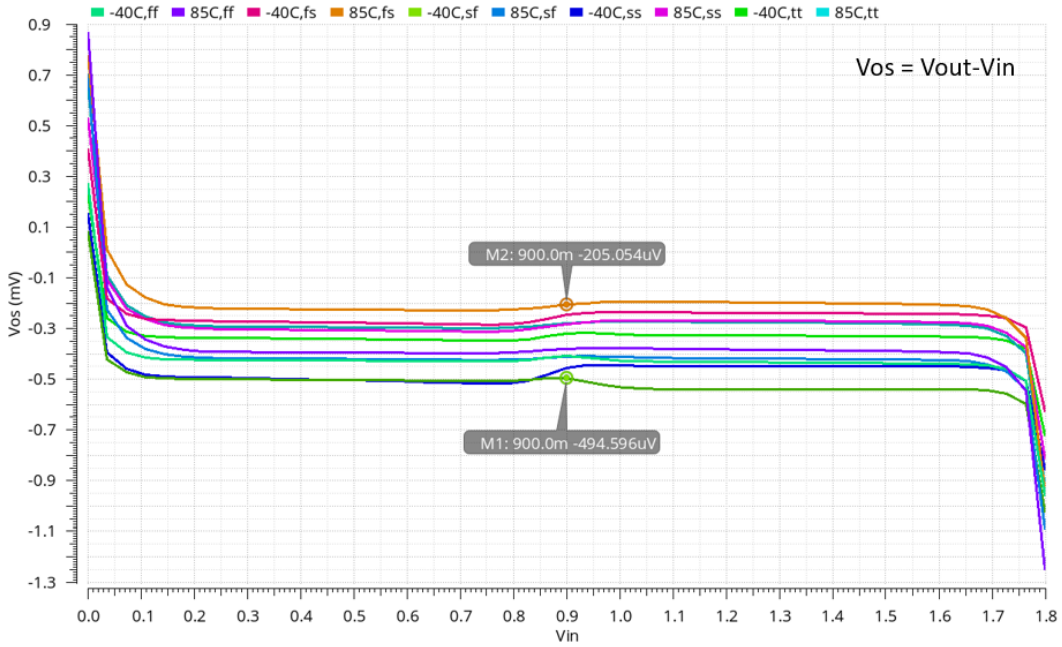


Figure 3-14: Offset of the buffer

This additional offset of 0.6mV is the systematic offset introduced by the mismatch in the layout's routings. A high resistance path was created due to a single via at the drains of one of the NMOS current mirrors, which led to this offset. It could be solved by increasing the number of vias, then the offset after the post layout sims reduced to zero for V_{in}=0.1V-1.7V.

The switching transistors are allocated the same size as the input transistors for constant gm over the ICMR. Figure 3-15 shows the simulated plot of constant gm over the ICMR at 27°C, without any mismatch.

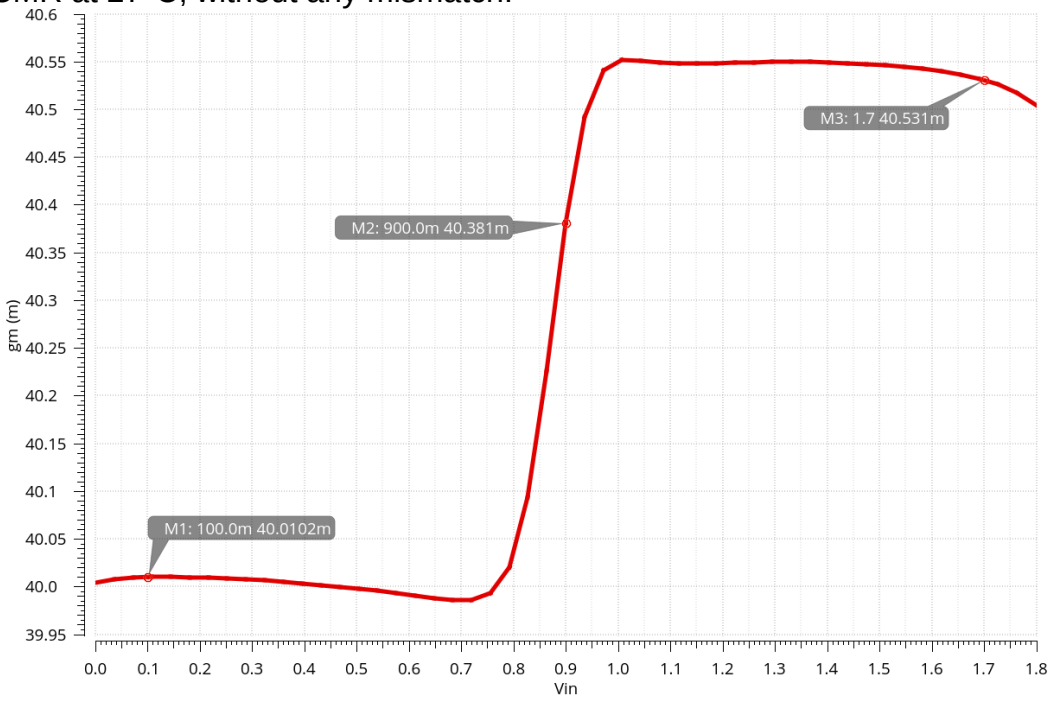


Figure 3-15: Plot of gm v.s. ICMR for T = 27 °C

Figure 3-15 shows the simulated gm v.s. ICMR at the typical corner without mismatch. There is a switch-over point at 0.9V where the gm change is minimal when there is a transition from PMOS to NMOS. Figure 3-16 shows the plot of gm over ICMR for T=-40°C, 85°C. It can be seen that for high-temperature gm is low. A constant gm biasing circuit has been used in the biasing network [10]. The variation in gm over temperature is due to the TC of the resistor in the constant gm biasing circuit.

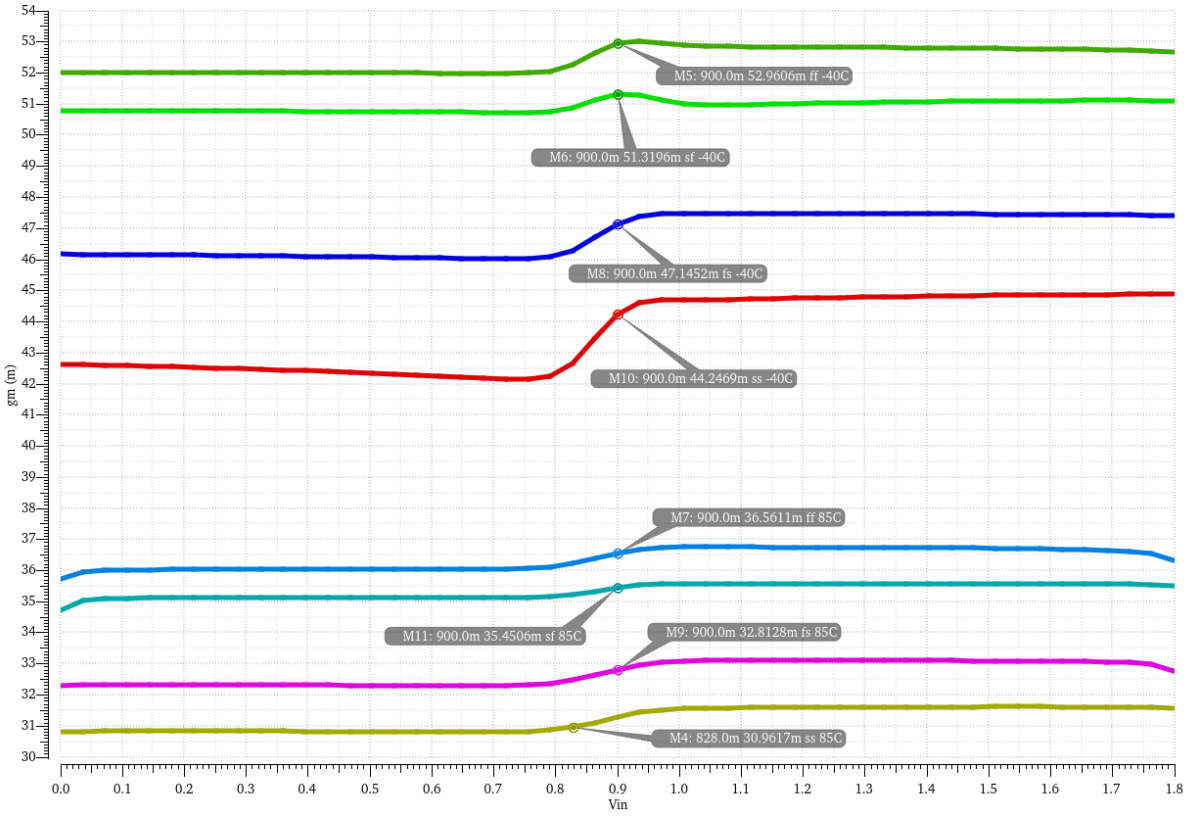


Figure 3-16: Plot of gm versus ICMR for T = -40°C, T=85°C

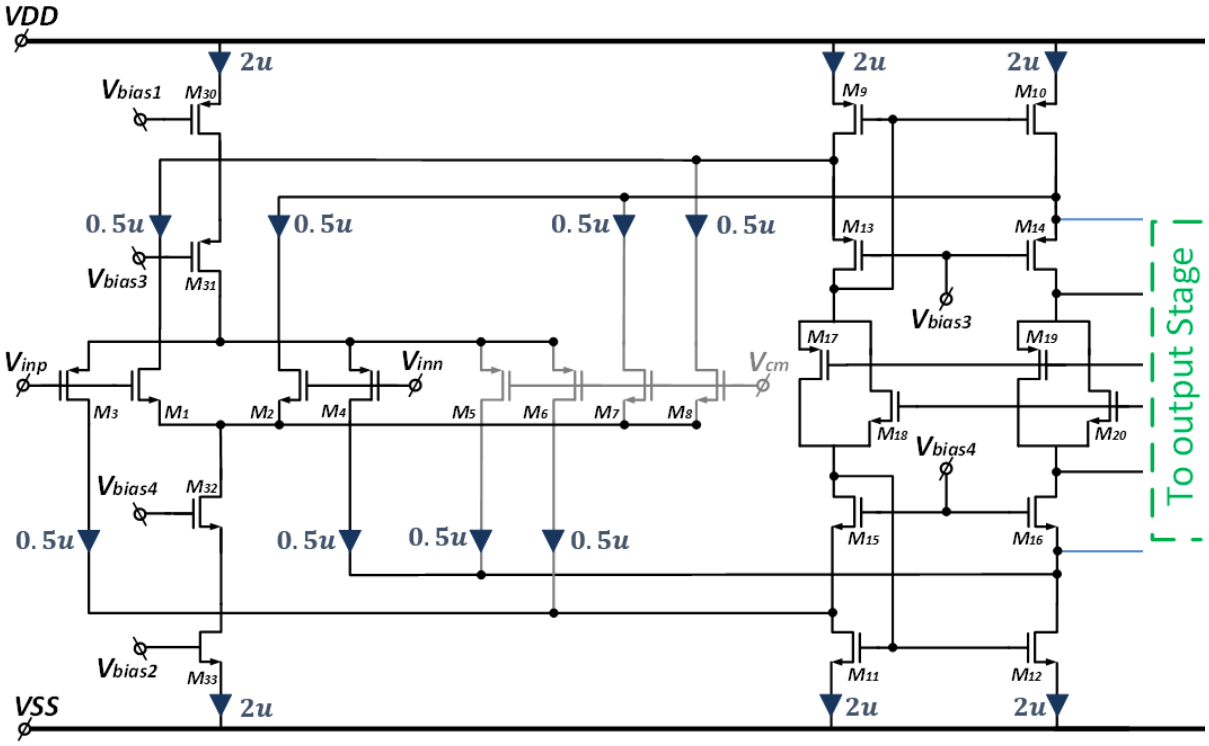


Figure 3-17: Current allocation in the input stage and the summing circuit at Vin=0.9V

Figure 3-17 shows the current flowing in the input stage and the summing circuit at V_{in}=0.9V. The 1uA current flowing in the input stage pair will then flow into the summing circuit. PMOS current mirrors source 2uA of current, and NMOS current mirrors sink 2uA of current. The cascode transistors M_{13} to M_{16} are biased at the edge of weak inversion. These contribute to the gain of the first stage while keeping the parasitic capacitance low. Table 2 below shows the width and the length of transistors in the input stage and summing circuit.

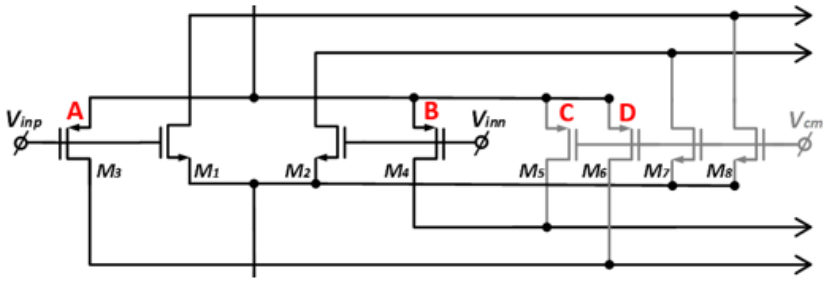
Table 2: Sizing of the transistors in the input stage and summing circuit

Transistor	W (μm)	L(μm)	No of fingers (M)
M_1,M_2	5	1.2	8
M_3,M_4	15	1.2	8
M_5,M_6	15	1.2	8
M_7,M_8	5	1.2	8
M_9,M_{10}	4	2	4
M_{30}	2	3	4
M_{11},M_{12}	2.2	20	4
M_{33}	2.2	20	4
M_{13},M_{14}	0.88	0.72	1
M_{31}	0.22	0.18	1
M_{15},M_{16}	1.76	0.36	1
M_{32}	0.22	0.18	2

3.1.4. Layout

Fabrication steps like photolithography, etching, ion implantation, and oxide growth/deposition introduce non-uniformity across a wafer and between wafers. This is called process variation. These process variations introduce mismatch. Because of the mismatch in transistor features, it becomes difficult to match their performance for circuits where matching the transistor's size is vital to get expected performance. For example, in the target application, it is crucial to keep the buffer's offset as low as possible. Thus, the transistors need to be matched as closely as possible. Matching techniques are used in layout to minimize the error caused by process variations.

In the input stage layout, to match the input transistor pairs, they were placed in a common centroid manner where each transistor is distributed throughout the array. Common centroid layout reduces the effect of linear gradients. As the input transistors are the dominant contributors to the offset, the metal routings are done such that the current flows in the same direction through the unit elements. Dummies are placed all around so that all transistors see the same environment. Figure 3-18 shows the pattern implemented for the input and switching transistors.



dum	dum	dum	dum	dum	dum
dum	C	D	A	B	dum
dum	D	C	B	A	dum
dum	dum	dum	dum	dum	dum

Figure 3-18: Layout pattern implemented for input transistors and switching transistors

This pattern matches transistor A with transistor B and transistor C with transistor D, but it does not match transistor AB with CD. Matching transistors AB with CD is unnecessary because only transistor A and transistor B contribute to the offset. So, matching transistor A with transistor B is essential.

All the transistors were placed in the same direction (poly orientation) because silicon is anisotropic. Figure 3-19 shows the layout of the PMOS input pair and its corresponding switching transistors. Figure 3-20 shows the layout of the NMOS input pair and its corresponding switching transistors.

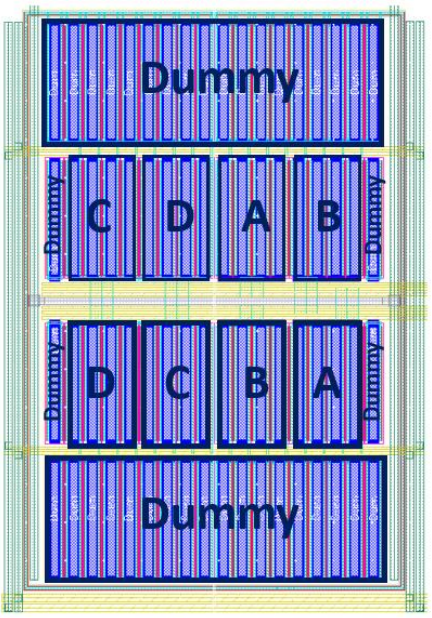


Figure 3-19: Layout of PMOS input pair and corresponding switching transistors

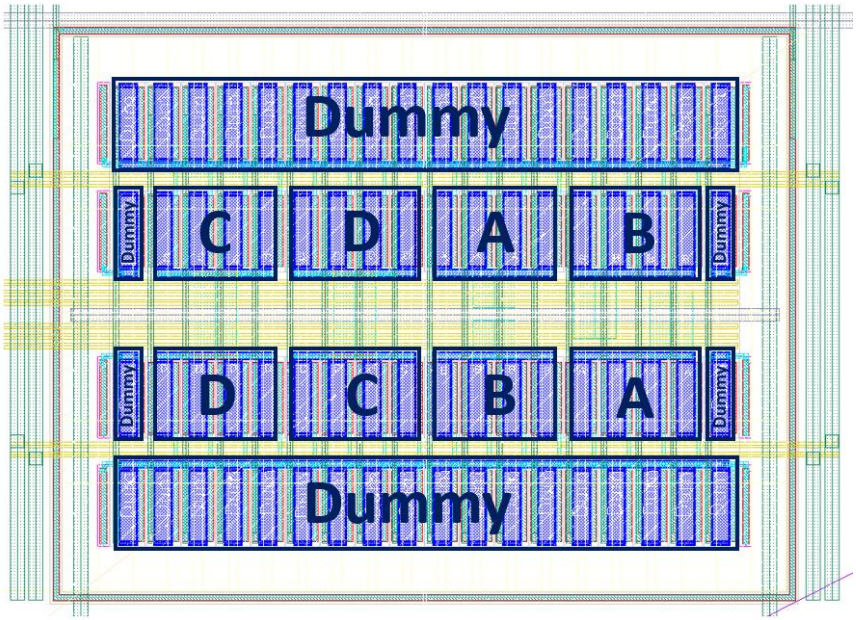


Figure 3-20: Layout of NMOS input pair and corresponding switching transistors

Matching the current mirrors is also essential. Common centroid technique was used for the matching of the current mirrors.

3.2. Rail-to-Rail Output Stage

The main goal of the output stage is to provide sufficient current to drive the load. For the power efficiency to be maximum, the output should swing till the supply rails and should be biased by a small quiescent current. There are mainly three configurations for the output stage out [14]. They are described below:

Class A output stage: The schematic diagram of the Class-A output stage is shown in Figure 3-21.

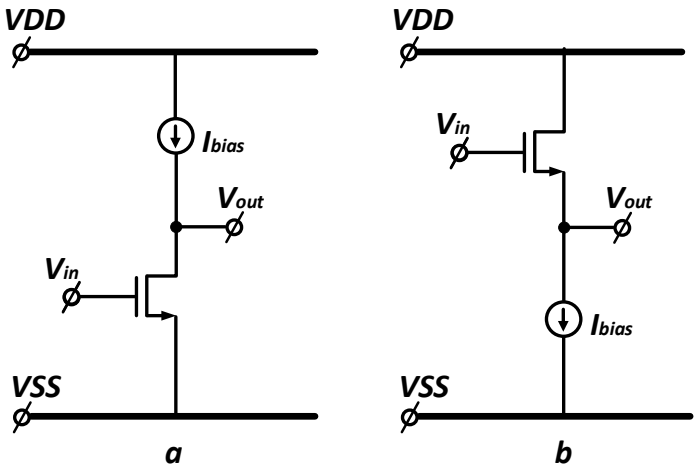


Figure 3-21: Class A output stage configuration: a. Inverting amplifier, b. voltage follower

It is characterized by an output transistor that is always ON even when the load is not drawing any current. The current sourced or sinked into the load by the voltage follower or by the inverting amplifier is limited by the bias current of the transistor. Thus, it has the least power efficiency among the three. Furthermore, it cannot swing rail-to-rail because the current source's saturation voltage limits the output.

Class B output stage: The circuit diagram of the Class B output stage is shown in Figure 3-22

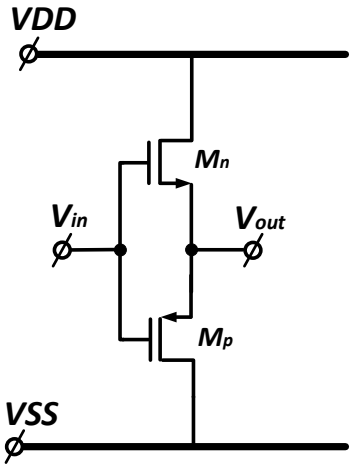


Figure 3-22: Class-B Output stage

When V_{in}=0, both the transistors M_n and M_p are OFF, and the output is zero. If V_{in} goes above M_n's threshold voltage, it starts conducting and acts as a source follower. The output V_{out} will follow V_{in}, and M_n delivers current into the load. Similarly, if V_{in} goes below M_p's threshold voltage, it will sink all the current from the load. The current flowing in the output transistor is zero when the transistors are not conducting. So, the power efficiency is better than Class A. There exists a dead band region in the middle when V_{in} is smaller than the V_{gs} of the M_p, M_n, and they are not conducting. This causes cross-over distortion, and therefore this configuration doesn't provide a linear response.

Class AB configuration: A compromise between Class A and Class B can be achieved with the Class AB output stage. Here a small quiescent current is added to the output transistors. The circuit diagram is as shown in Figure 3-23.

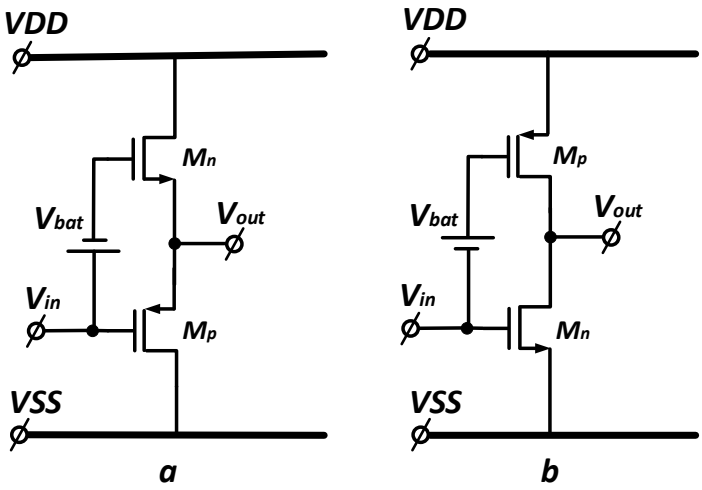


Figure 3-23: Class AB output stage configuration:
a. Common-drain stage, b. Common-source stage

A voltage source V_{bat} is connected to the gates of the output transistors. Even when the input voltage is equal to zero, assuming that the V_{bat} is large enough to turn both the transistors on, there will be some quiescent current. Hence this avoids cross-over distortion. V_{bat} should be large enough to turn on the output transistors. During the positive half cycle, when V_{in} increases, V_{out} also increases. The NMOS Mn is ON and is sourcing current into the load. During this, the PMOS M_p is not switched off. It is still conducting the quiescent current. The quiescent current is the current that flows from VDD to VSS when there is no input signal applied, and the circuit is not supplying current to any load. As the input voltage reached zero, both the transistors are conducting. There is a cross-over period where it is a very smooth transition between the current through the NMOS decreasing and the current through the PMOS increasing. So, the transition from sourcing current to sinking current is smooth. Therefore, this eliminates cross-over distortion.

Two types of Class AB stage:

- *Class AB with CD configuration:* Here, the output transistors are connected in a common drain as in Class - B stage, shown in Figure 3-23, a. The output swing here is limited to supply voltage minus the output transistor's gate-source voltage, which is significant.
- *Class AB with CS configuration:* Here, the output transistors are connected in an inverting amplifier configuration. The output can swing up to supply voltage and is only limited by the output transistor's saturation voltage. So, this configuration is used in this design.

Now that the output stage configuration is chosen, the next problem is to find a way to bias the gates of these transistors, i.e., to implement $V_{bat.}$ Various techniques are proposed in the literature, like biasing using diodes, common-mode resistive coupling [14]. Among the most popular for a rail-to-rail output stage is the Class-AB Monticelli biasing, which is also used in this design [15].

For this design, it is desirable to have a circuit that controls the gates of the output transistors so that the current that flows through these transistors from VDD-M_p-M_n-VSS is well controlled. The current provided by the bias circuit should not depend on the supply voltage; otherwise, the quiescent current through the output transistors will not be constant. The classical way to do this is to use a translinear loop. Figure 3-24

shows the circuit diagram of the Class AB output stage with Monticelli biasing used in the design.

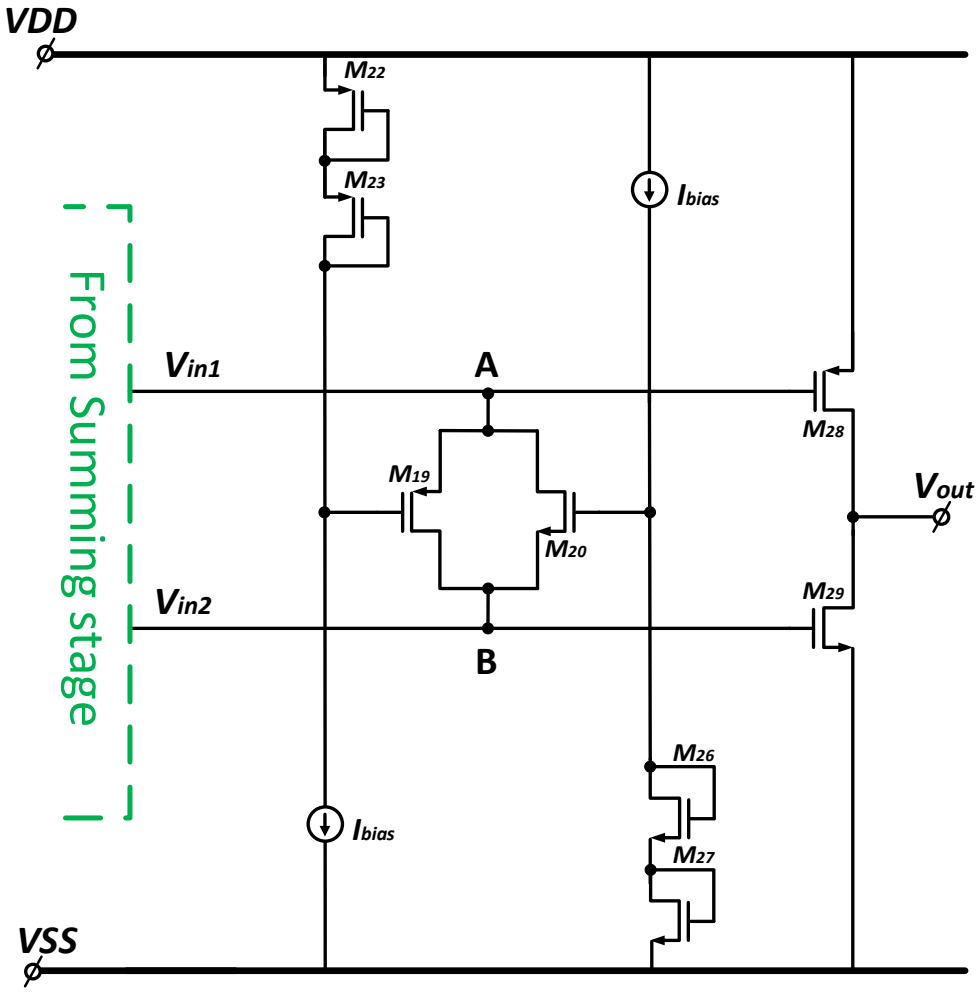


Figure 3-24: Class AB output stage with Monticelli biasing

The translinear loops are formed by the transistors M_{22}-M_{23}-M_{19}-M_{28} on the PMOS side and M_{27}-M_{26}-M_{20}-M_{29} on the NMOS side and are given by the equations below

$$V_{gs,22} + V_{gs,23} = V_{gs,19} + V_{gs,28} \tag{3.3}$$

$$V_{gs,27} + V_{gs,26} = V_{gs,20} + V_{gs,29} \tag{3.4}$$

The translinear loop is used to bias the output transistors and prevent them from shutting down. During the design, the sizing was done such that the current density in all the transistors forming the translinear loop was the same. Any signal entering node A or node B from the summing circuit sees a low impedance at the output transistor's gate. This low impedance is formed by the sources of transistors M_{19} and M_{20} at nodes A and B. It appears that the signal current will be lost. But the mesh formed by transistors M_{19} and M_{20} is connected head to tail and creates a positive feedback loop. Therefore the signal that will flow into the source will return. Transistors M_{19} and M_{20} provide good coupling between the two inputs V_{in1} and V_{in2}. If a signal current flows into node B, the voltage at node B increases; therefore, the gate-source voltage of M_{29}

increases, whereas the gate-source voltage of M_{20} decreases and turns off, diverting all the current to M_{19}. This will increase the potential at node A. V_a follows V_b, so transistors M_{19} and M_{20} behave like floating voltage sources.

3.2.1. Sizing of the output stage

The output transistors M_{28} and M_{29} are biased in weak inversion. So, they provide significant transconductance increasing the efficiency of the output stage. Since this design needed to operate at low currents, the output stage was sized to carry a quiescent current of 2uA. It is also desirable to have the same current densities in all the transistors in the translinear loop biasing the output stage. So similar (w/l) ratios were used even for the transistors in the translinear loop. Figure 3-25 shows the current flowing in the translinear loop and the output transistors for V_{in}=0.9V.

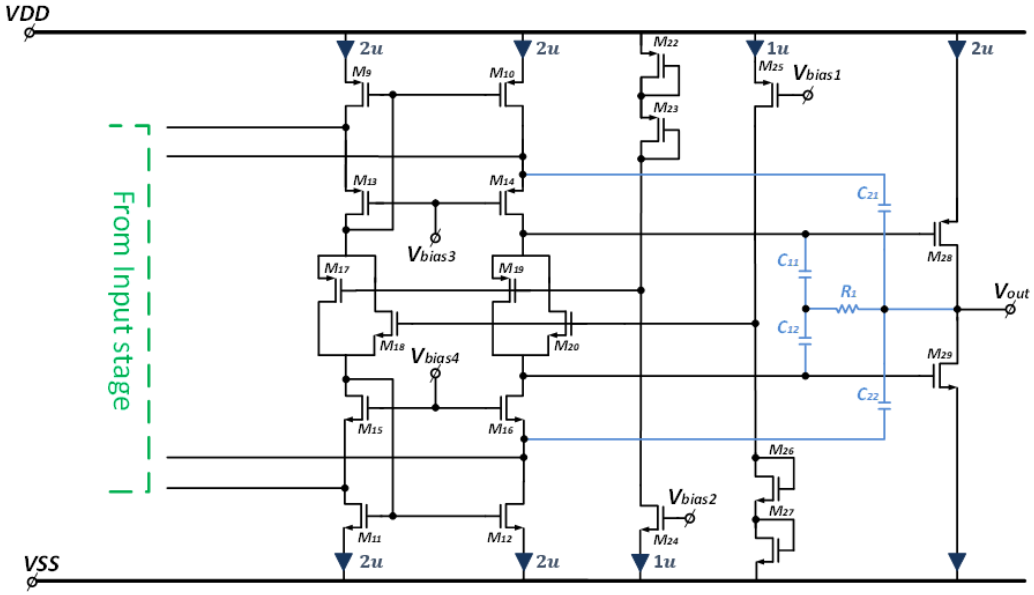


Figure 3-25: Current flowing in the translinear loop and the output stage

The width and length of the transistors in the output stage and translinear loop are shown in Table 3.

Table 3: Sizing of the transistor in the output stage and translinear loop

Transistor	Width(μm)	length(μm)	No of fingers (M)
M_{17}	2	3	1
M_{18}	2.2	20	1
M_{19}	2	3	1
M_{20}	2.2	20	1
M_{22}	2	3	2
M_{23}	2	3	2
M_{24}	2.2	20	2
M_{25}	2	3	2
M_{26}	2.2	20	2
M_{27}	2.2	20	2
M_{28}	2	3	4
M_{29}	2.2	20	4

3.3. Frequency compensation

Frequency compensation is necessary to make the system stable. Since negative feedback is applied to the amplifier to improve its performance, it is needed to ensure that the amplifier is stable and without any oscillations and ringing. To ascertain the stability of the amplifier, the frequency response of the amplifier is determined. From the frequency response, it can be inferred whether the amplifier will become unstable during the operation. Typically Miller compensation is used to stabilize a two-stage amplifier because it provides a smooth -20dB/decade roll-off using one capacitor. But Miller capacitor introduces a Right Half Plane (RHP) zero, which reduces the phase margin. It also reduces the unity-gain bandwidth of the amplifier [10]. To mitigate this issue, cascoded Miller-Compensation is used, where cascoded transistor is the part of the Miller loop. This has two advantages. First, due to the presence of a cascode transistor, the finite gain is introduced in the Miller loop, and the bandwidth is doubled. This is achieved with no increase in current, and hence the power consumption remains the same. Second, the Miller capacitor is connected to a low-impedance node – the source of the cascode transistor. Because of this, the RHP zero is shifted to higher frequencies, and hence the phase margin is unaffected at lower frequencies. Figure 3-26 shows how the Cascoded-Miller compensation is used in the circuit.

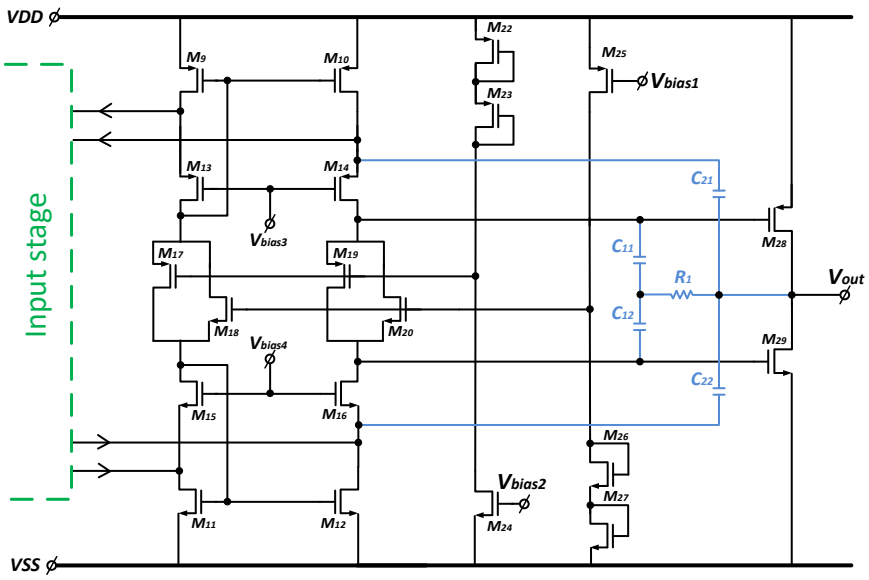


Figure 3-26: Cascoded-Miller compensation used for making the amplifier stable

C_{21} and C_{22} form the main Miller capacitors, which are connected to the source terminal of the cascode transistor M_{14} and M_{16}. Now, in the loop from the drain of M_{28}-C_{21}-to the source of M_{14}-M_{28}, two poles are present. To push these poles apart, an auxiliary Miller capacitor C_{11} is used. R_1 is used to cancel the RHP zero introduced by the Miller capacitor C_{11}.

3.3.1. Sizing of Capacitors and resistors

The formula calculates the value of the capacitor C11:

$$C_{miller} = C_{21}, C_{22} = \frac{g_m\ of\ the\ input\ transistor}{\omega_{unity}}$$

The auxiliary Miller capacitor should be $\frac{1}{3}rd$ of the value of the main Miller capacitor to provide enough phase margin.

$$C_{auxiliary} = \frac{1}{3} * C_{miller}$$

The value of R_1 should be equal to 1/gm of the output transistors. Figure 3-27 shows the loop gain, and the buffer's phase margin after the compensation is applied.

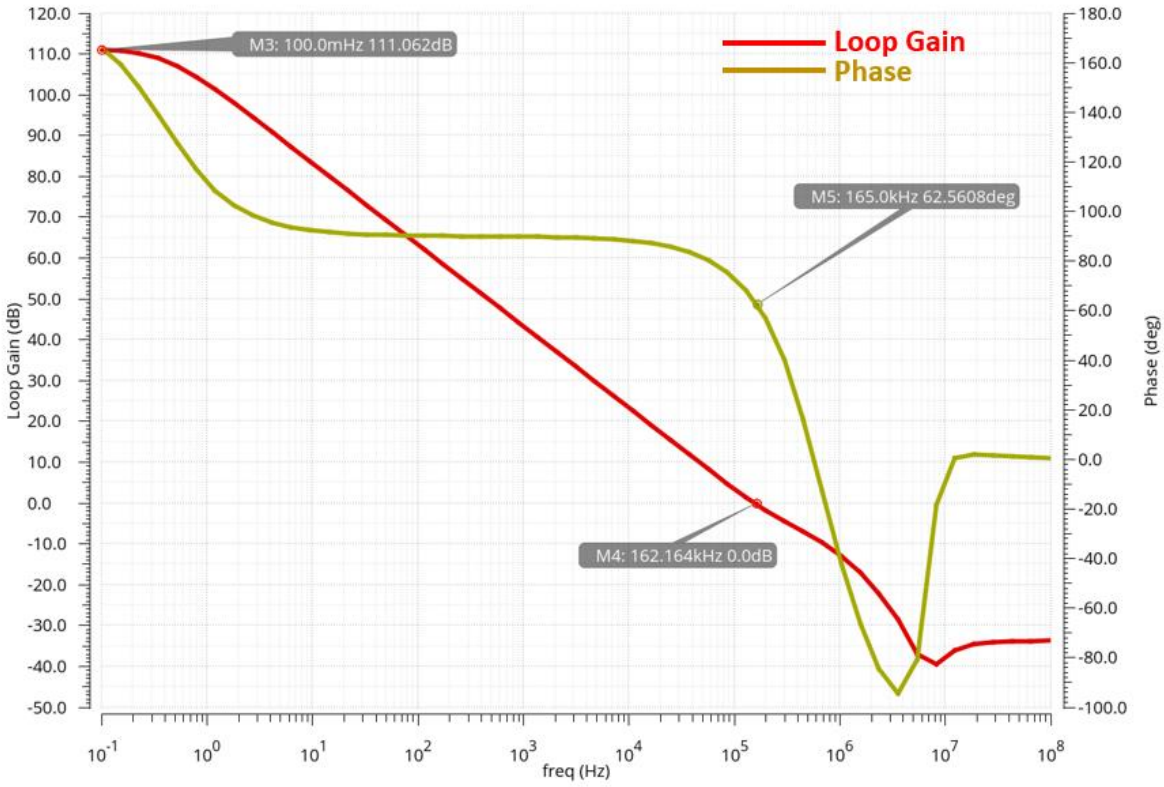


Figure 3-27: Loop Gain and phase margin of the buffer

The buffer has an open-loop DC gain of 111dB and has a 62° phase margin. The amplifier is hence stable and has a unity gain frequency of 164kHz.

3.4. Bias circuit

The biasing circuit used in the design is shown in Figure 3-28.

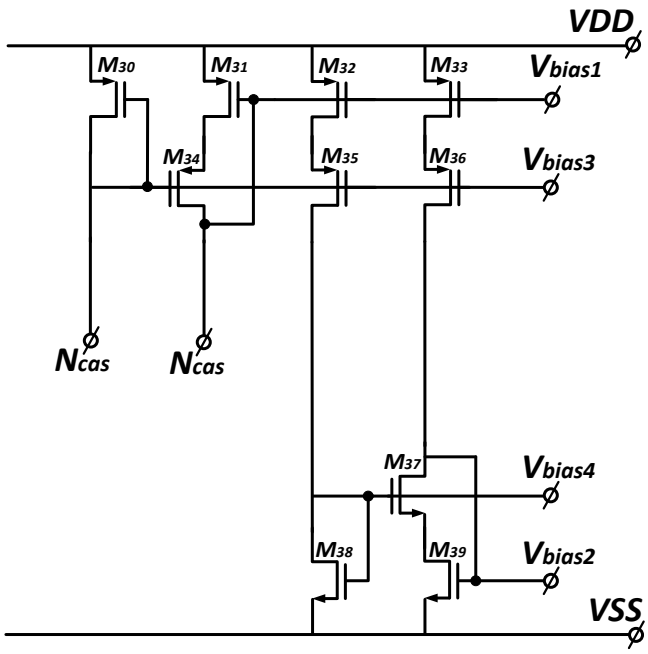


Figure 3-28: Biasing circuit used in the design

Cascoded current mirrors are used for biasing. Current mirrors are used to copy the reference current from an accurately defined current source. The reference current is generated by a constant gm biasing block [10]. In Figure 3-28, M_{34} and M_{39} form the current mirrors. They have been cascoded by M_{34} and M_{37} so that the drain to source voltage, V_{ds}, across the current mirrors is the same, hence reducing channel length modulation. There is a constant current flowing through M_{30} and M_{38}. M_{30} and M_{38} are sized to increase the voltage at the gate of the cascode such that the current mirrors M_{31} and M_{39} are in saturation with some margin. The biasing circuit is designed to carry a current of 1uA. The sizing of the transistors in the biasing circuit is shown in Table 4

Table 4: Sizing of the transistors in the biasing circuit

Transistor	Width (µm)	Length(µm)	No of fingers (M)
M_{30}	0.33	1.4	1
M_{31}	2	3	2
M_{32}	2	3	2
M_{33}	2	3	2
M_{34}	0.22	0.18	1
M_{35}	0.22	0.18	1
M_{36}	0.22	0.18	1
M_{37}	0.22	0.18	1
M_{38}	0.22	4	2
M_{39}	2.2	20	2

3.5. On-chip bootstrapped ESD diode structure with on-chip AZ amplifier

After the design of the on-chip buffer, it was combined with the existing AZ amplifier and taped out with the bootstrapped ESD diode structure. Figure 3-29 shows the layout of the whole chip. In Figure 3-30 the zoomed-in part of the bootstrapped diode region of the chip and the pads where the diodes are placed are shown.

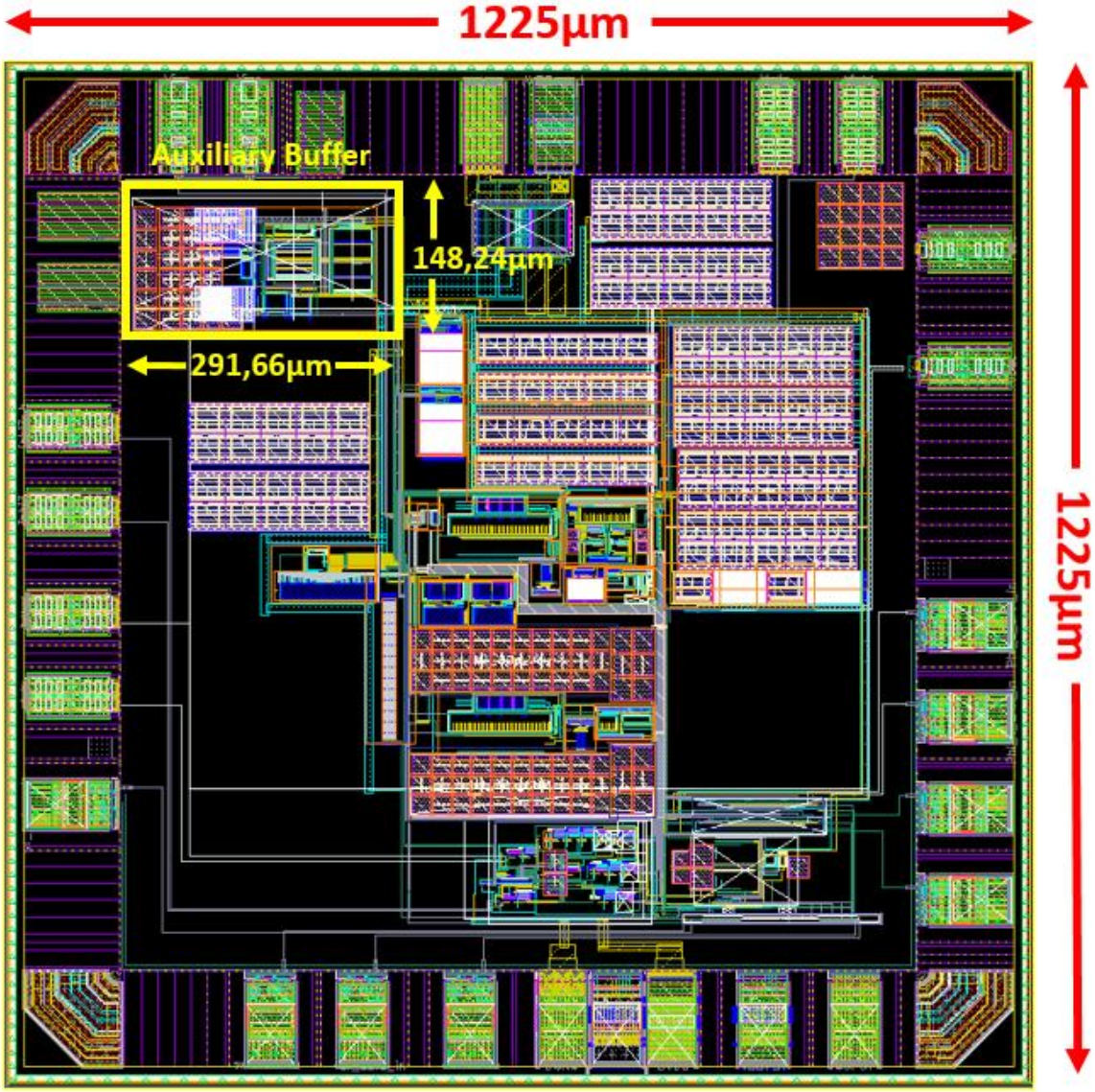


Figure 3-29: Chip layout in Cadence

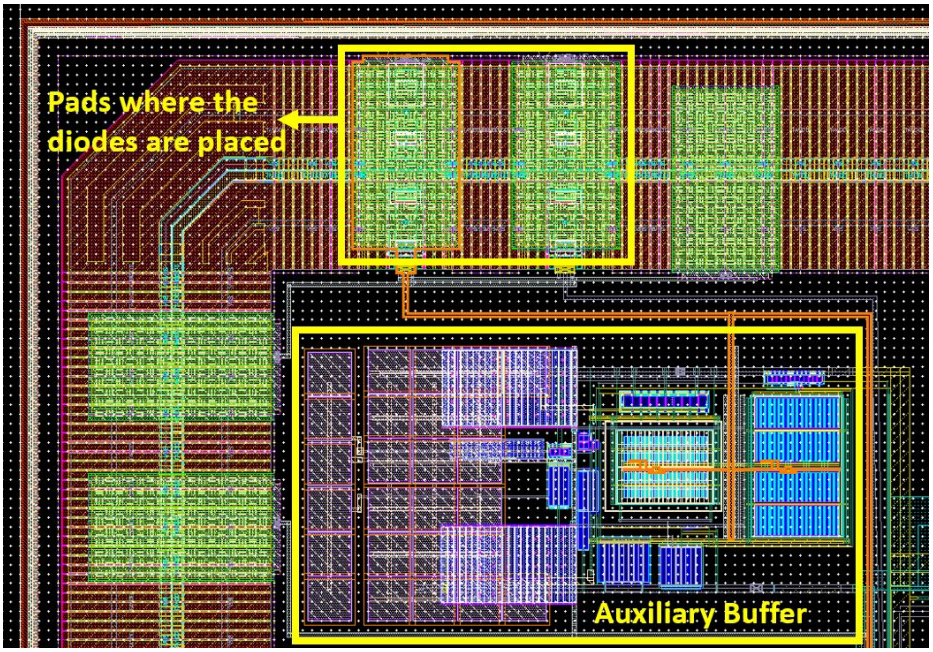


Figure 3-30: Zoomed in part of the chip layout showing the buffer and the diodes in the pad

The measurements of these chips are described in Chapter 5.

4. Low leakage measurement challenges

Measuring ultra-low input current (<1pA) is challenging because of a host of factors. These factors range from the instrument's limitation to measure the low current, pinout, electrostatic coupling, selection of the PCB material, PCB design, and contamination. A few of the challenges that were faced during measurements and some of the solutions are described below:

a) Measuring ultra-low input current

To measure currents greater than 1uA, Digital Multimeters (DMM) are typically used. However, their input voltage drop (input burden) is very high. Furthermore, typically DMM resolution is not better than 1nA [16]. This does not allow measurements in the range of 10pA, which is required in the application.

An electrometer is an ammeter used for measuring very low currents and is limited by its input bias current [16]. Electrometers have a very high input impedance of about 100TΩ to 10PΩ [17]. Since electrometers have a very low input bias current and minimal input voltage burden, they can measure the input current for our application. It can detect currents as low as 1fA (10^{-15} A), sufficient for our target of 50fA at room temperature.

b) Pinout

Since the aim is to design a general-purpose amplifier, the chips were bonded in a DIP package because a commercially sold amplifier will always be packaged. The chips that were taped out first were bonded in a 24-pin DIP package. Care was taken while routing the input pin lead of the DIP package both at the PCB level and the package level. Guarding is applied both at the PCB level and the package level. Care was also taken that the input pin is not close to the supply pins or ground pins because the pin spacing and nearby signals influence the input current. [8]

c) Guarding

While doing low current measurements, the major problem is leakage. If there is any trace around the input signal whose potential is different than that of the input signal, there will be a leakage current due to this potential difference. One technique to minimize this leakage is guarding. Guarding is a technique to surround the input trace with another trace (GRD trace) driven by a guard voltage. The GRD trace will be at the same potential or very close to the input trace.

For example, in Figure 4-1, there is a signal trace surrounded by a GRD trace.

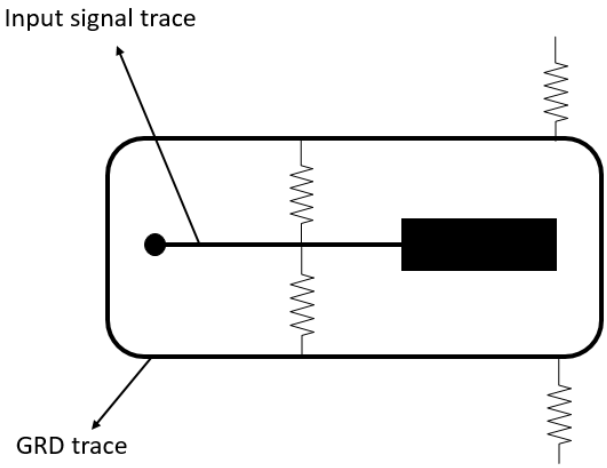


Figure 4-1: Guarding technique on the PCB

If the GRD trace's potential is equal to the input signal trace, there will be no potential difference between the input signal trace and GRD trace, and hence no leakage current. Figure 4-2 shows how the guarding has been implemented in the PCB.

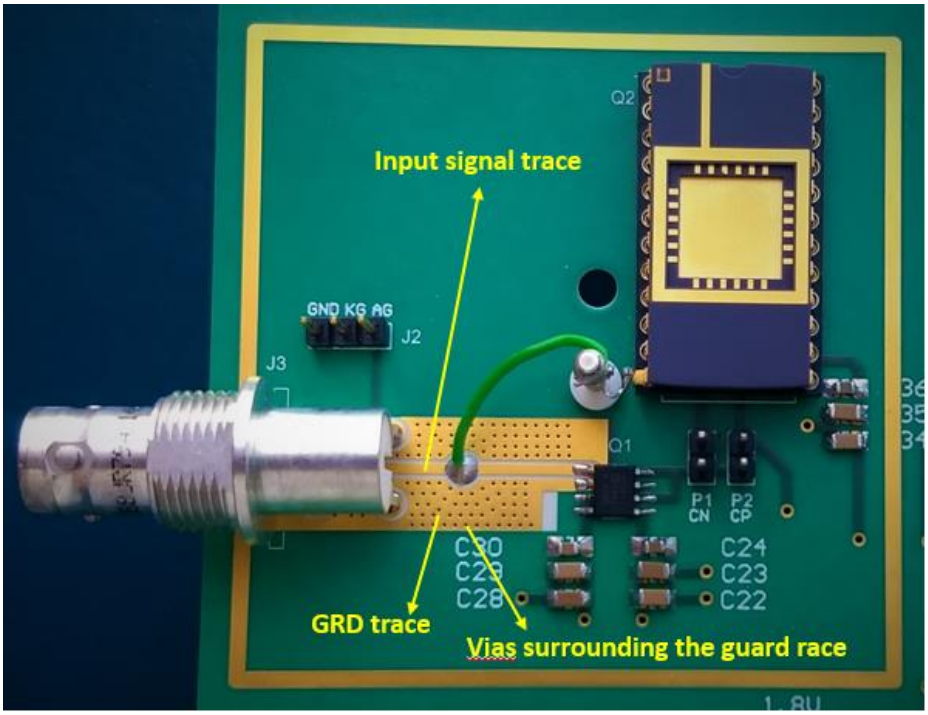


Figure 4-2: A portion of the PCB showing the input trace, GRD trace, and the vias

Here, the guard ring is a filled copper trace surrounding the input pin (gold plated). This guard ring also guards against any surface leakage. The solder mask and silkscreen have been removed from the guard ring and traces. This ensures that the guard traces do not make any electrical contact with any surface leakage path and avoid moisture absorption by solder mask and silkscreen. The guard traces can be driven by an external amplifier or the integrated GRD Buffer of the Keithley 6514 electrometer.

Another technique that is applied in the PCB was to implement a GRD plane below the input trace. The GRD plane structure is shown in the cross-section of the PCB in Figure 4-3 [17].

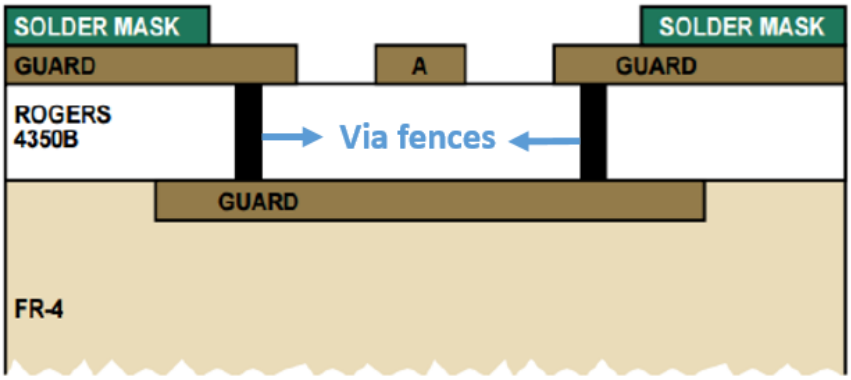


Figure 4-3: Cross-section of PCB showing the GRD pane [17]

It is a filled Cu trace placed directly below the input trace. The GRD plane is connected to the GRD trace on the surface using vias.

d) Moisture

Another issue that needs to be considered while selecting the PCB material is moisture. Moisture can adhere to the surface of the board or get into the bulk of the board. So, the appropriate material that reduces the problem with humidity needs to be chosen. Roger 4350-B material provides superior insulation resistance in moisture than glass/epoxy material, thereby minimizing leakage [17].

e) PCB material

The PCB is a four-layered hybrid stack-up dielectric material board. The outer layers (top and bottom layers) are Roger 4350B material to minimize leakage currents [17]. The core layers are conventional FR-4. Guarding was done in all four layers. Another structure that was implemented is via-fence. A via-fence guards the lateral leakage paths. It can be implemented by surrounding the guard rings with vias going from the top layer to the bottom layer and are connected to all the layers. The rounded circle dots in Figure 4-2 are the vias. To prevent the input pin from going through the 4 layered board, it was air wired using a Teflon insulator standoff.

f) Contamination

Another challenge while doing low input current measurement is contamination. The sources of contamination are solder flux residue, dust, dirt, and body oils. It was observed that the contaminants act as an electrolyte. They form a weak battery. The error caused by contamination cannot be suppressed efficiently by guarding because it can easily overpass the guard lines. The only way to deal with it is by properly cleaning the board [17]. So, the board was cleaned after every experiment. If the board is contaminated too much, ultrasonic cleaners can be used. Ultrasonic cleaners are very effective because they create

ultrasonic frequencies, and these create cavitation that could remove contaminants from the hard-to-reach areas and mounted components on the board.

g) Shielding

The input signal trace is very susceptible to interference and coupling from the surrounding environment. To shield the input signal, a box of conducting material is placed around the PCB to shield it from external interference sources. The shield acts as an electrical barrier and interrupts the capacitive coupling path. Then the displacement current from the interference source is shunted by the metal box. The shield is often connected to a low impedance source, i.e., ground. Figure 4-4 shows the picture of the PCB inside the metal shield.

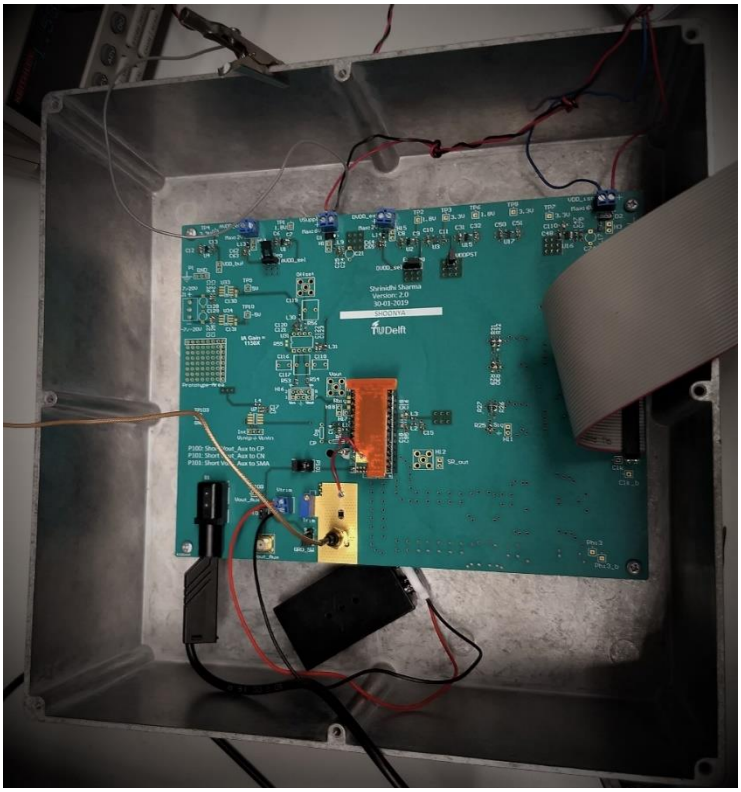


Figure 4-4: PCB inside the metal shield

The metal shield also prevents contamination from fingerprints, dust, and other contaminants from reaching the input pin while doing measurements. The PCB was placed inside the metal box and covered with a lid while measuring the input current. The shield was connected to GND potential.

h) Cables and Connectors

Guarding cables & connectors are equally important as they are on the PCB level. Triax, SMA (SubMiniature version A) cables, and connectors are used. Triax has an extra inner conductor (GRD conductor) to guard the signal, as shown in Figure 4-5.

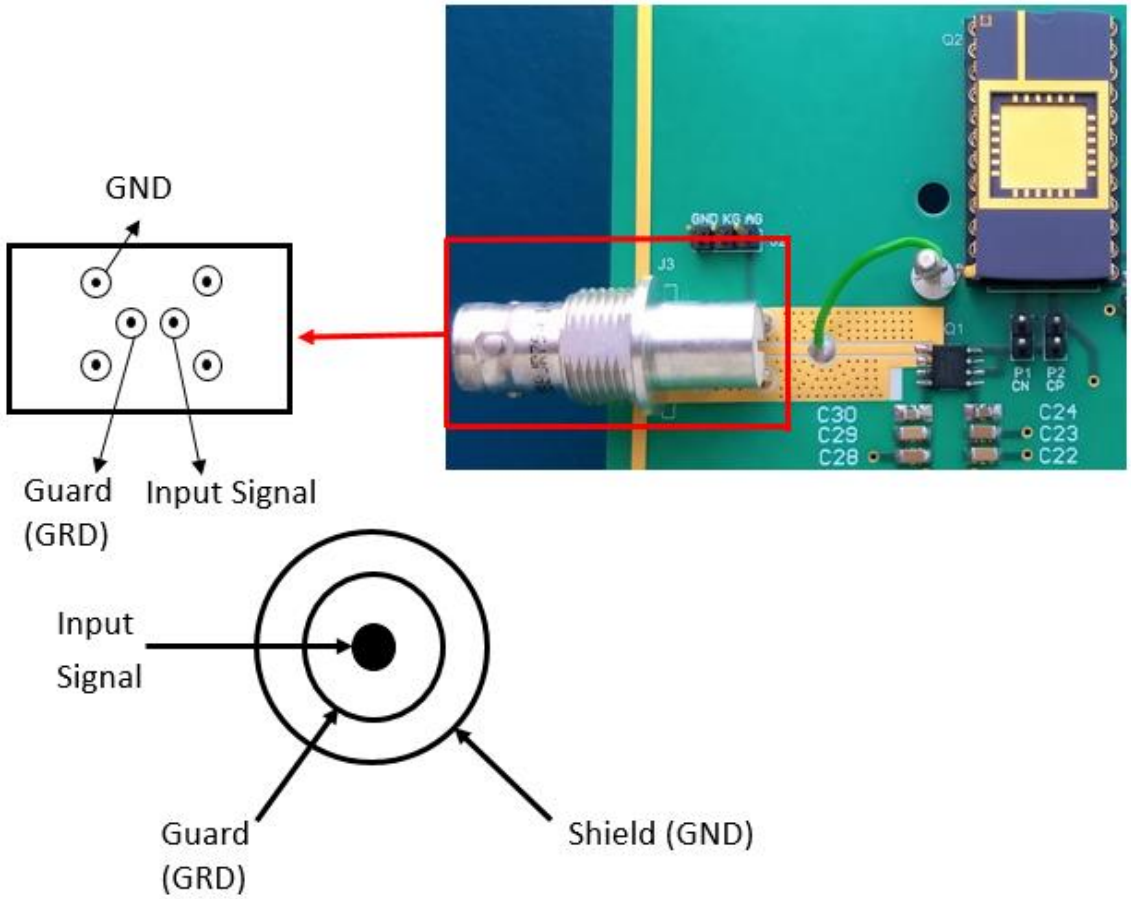


Figure 4-5: Triax Connector

The guard (GRD) conductor will surround the inner conductor that is connected to the input pin. Since there is no potential difference between the input pin and the GRD, there will not be leakage current. The shield which is the outer conductor is connected to GND. Coaxial cables like SMA and SMB (SubMiniature version B) can also be used if there is a small potential difference between the center conductor and the shield. If coax cables are used for low input current measurement, the inner conductor is typically connected to the input pin and the outer conductor to the GRD potential.

Triax cables are used to connect to Keithley and measure the current in the first tapeout. The GRD is driven by external equipment like the Keithley electrometer or the external buffer.

Cables can also be tied down to reduce triboelectric effects. The triboelectric effect is the generation of electric charges due to the friction of dissimilar material. The flexing or moving of cables could generate charges. Fixing the position of cables will help to reduce the triboelectric effect.

Figure 2.14 is the picture of the PCB board that tackles all of the measurement challenges described earlier.

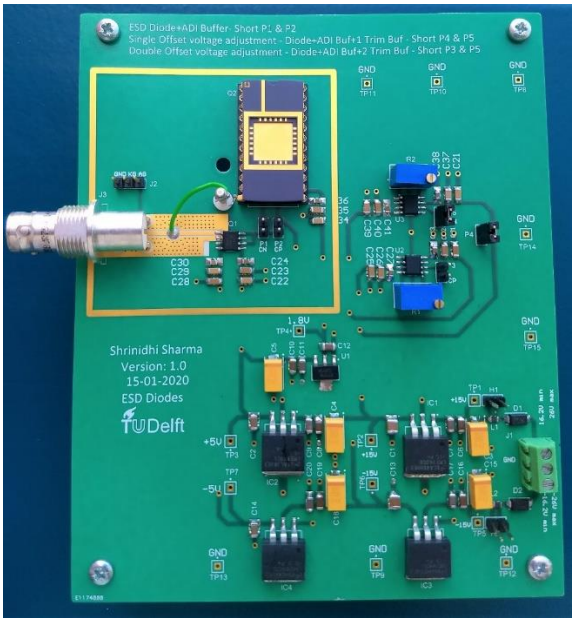


Figure 4-6: PCB Board

PCB board is made up of Roger 4350-B material for low moisture absorption, low dielectric absorption. Decoupling capacitors and regulators are also mounted on the PCB. The input voltage is varied using a battery and a potentiometer to get a low noise variable voltage source. The board can be directly connected to the electrometer using a Triax cable for current measurements.

5. Measurements and Future Work

This section presents the measurement results of the On-chip bootstrapped ESD diode structure.

5.1. Measurement Setup

The measurement setup is illustrated in Figure 5-1.

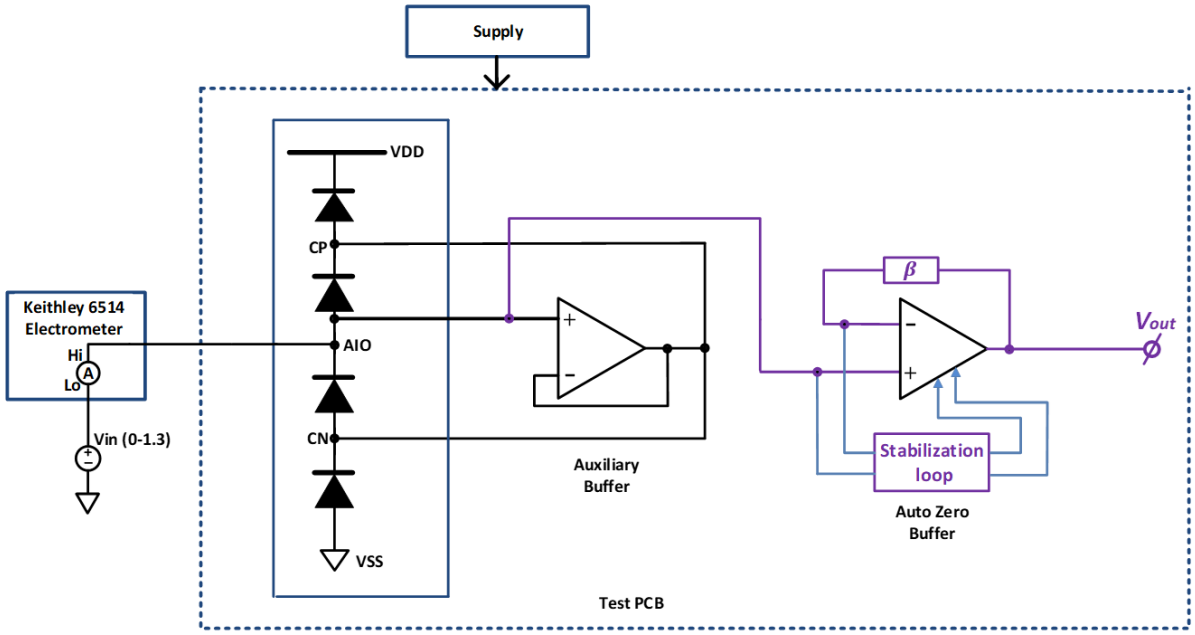


Figure 5-1: Measurement Setup

The input current is measured by varying the input voltage from 0 to 1.3V. The AZ amplifier operates for the ICMR from 0V to 1.3V. So, the measurements are also done for this ICMR. The measurement procedure is explained in section 2.4.

5.2. Die Micrograph

The bootstrapped ESD diode structure is realized in 0.18μm standard CMOS technology. The die micrograph is shown in Figure 5-2.

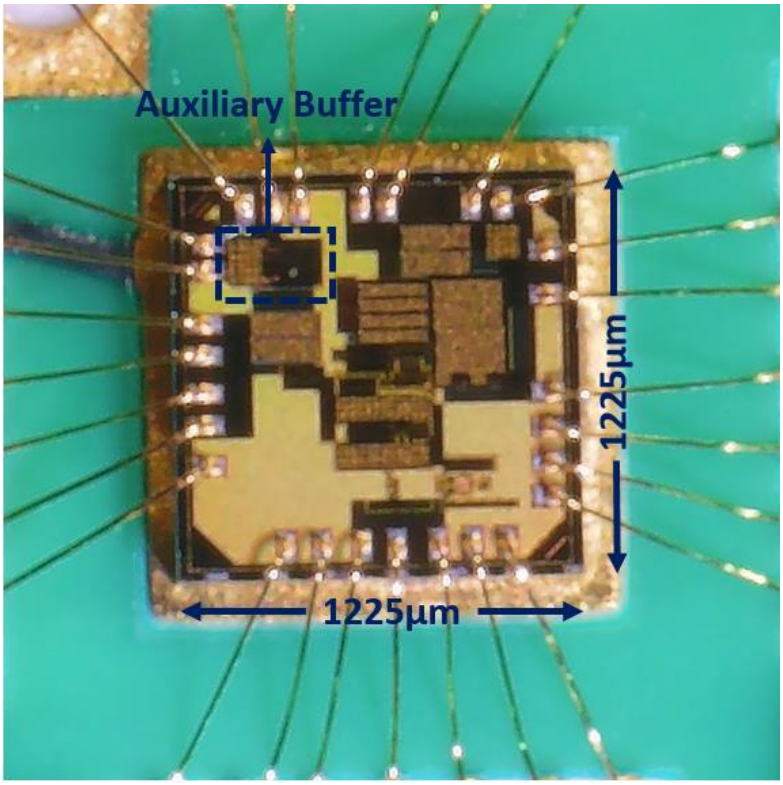


Figure 5-2: Die micrograph

The auxiliary buffer dissipates 17µA current from a 1.8V supply and occupies an area of 0.043mm^2. The diodes are placed under the pads and are connected to the input pins. The die has 28 pads and was encapsulated in a 28-pin DIP package, as shown in Figure 5-3.

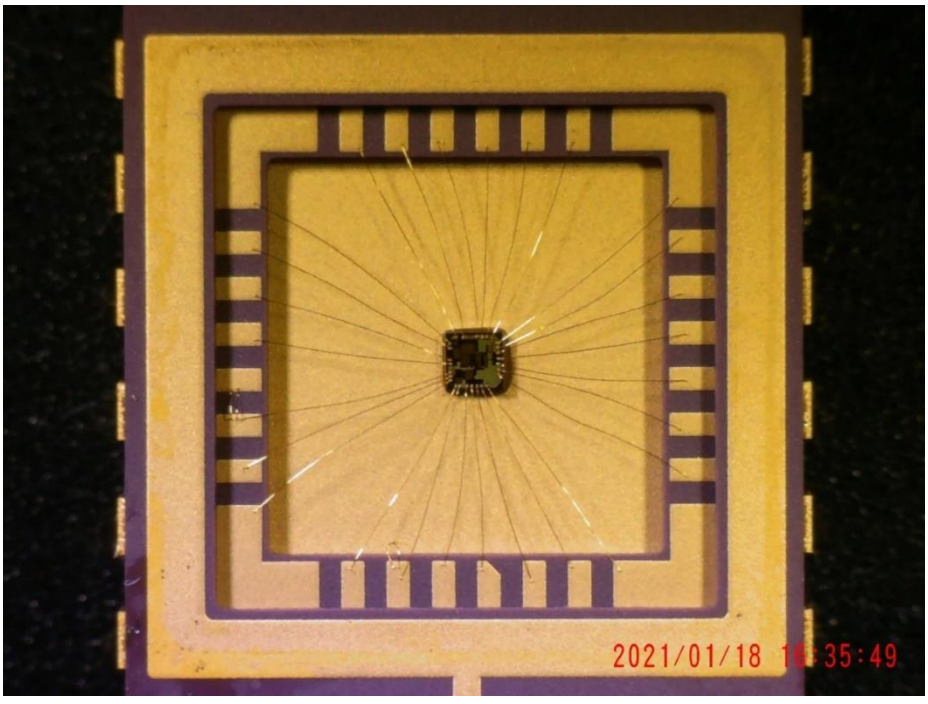


Figure 5-3: Chip bonding in the 28-pin DIP package

5.3. PCB Board

The PCB board is shown in Figure 5-4.

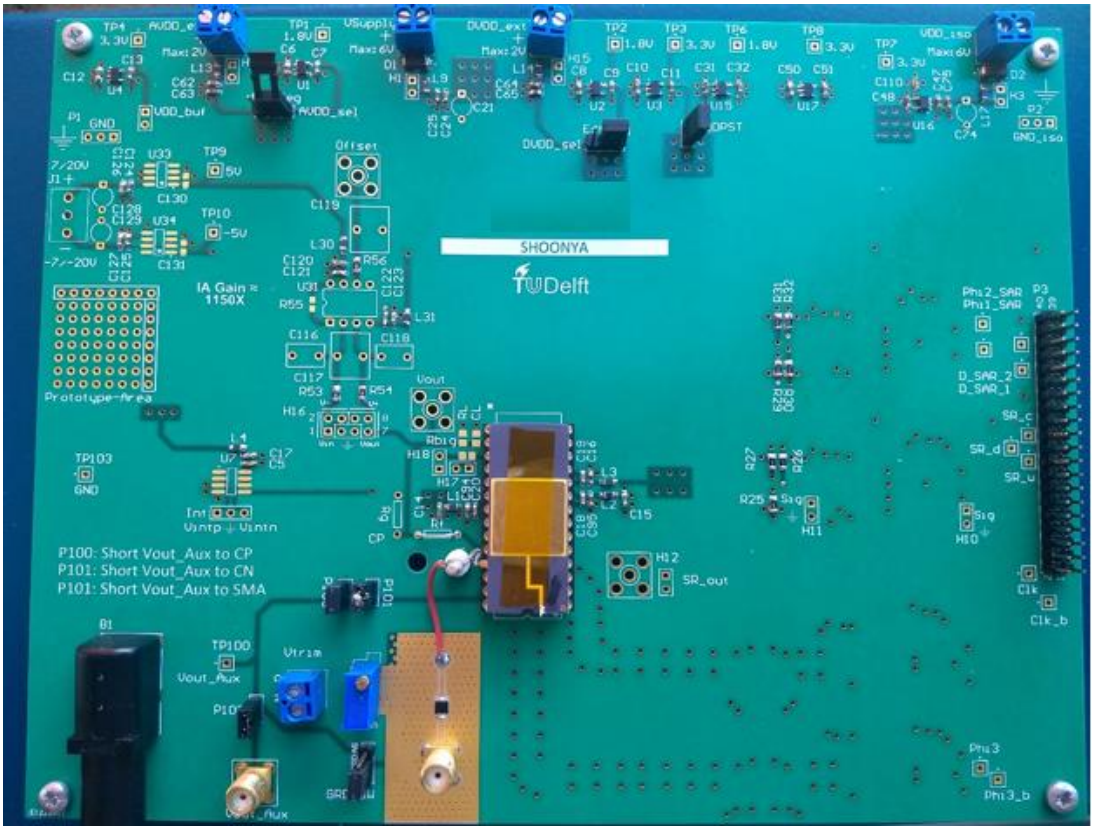


Figure 5-4: PCB board

To reduce leakage, Roger's material is used as the PCB base material. All other techniques discussed in Chapter 4 were followed to minimize the leakage.

5.4. Measurement results

The input current was measured before mounting the chip on the PCB to characterize the PCB leakage current, as shown in Figure 5-5.

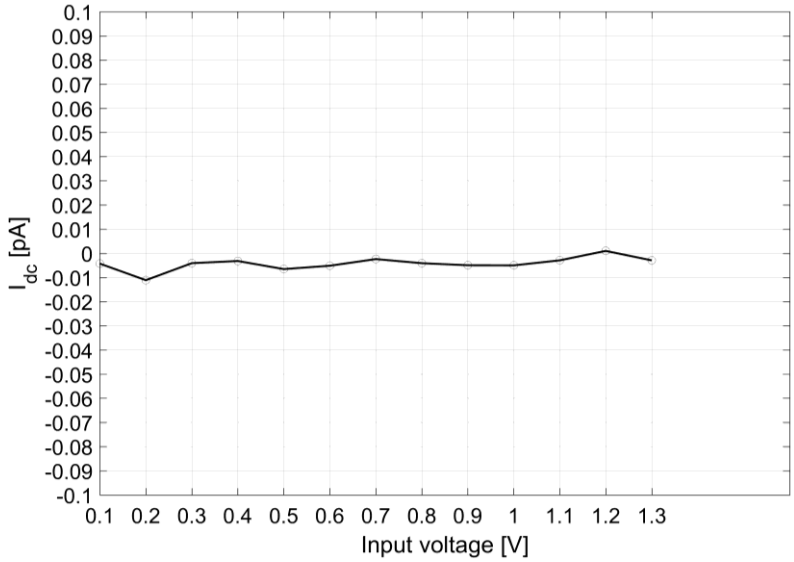


Figure 5-5: Plot of measured input leakage current without chips

The leakage current of the PCB is less than 10fA, which is smaller than the chip's expected input leakage current. Therefore, it can be ignored for the rest of the measurements. After the packaged chips were plugged in, input current measurements were performed. The input current of two different samples is shown in Figure 5-6.

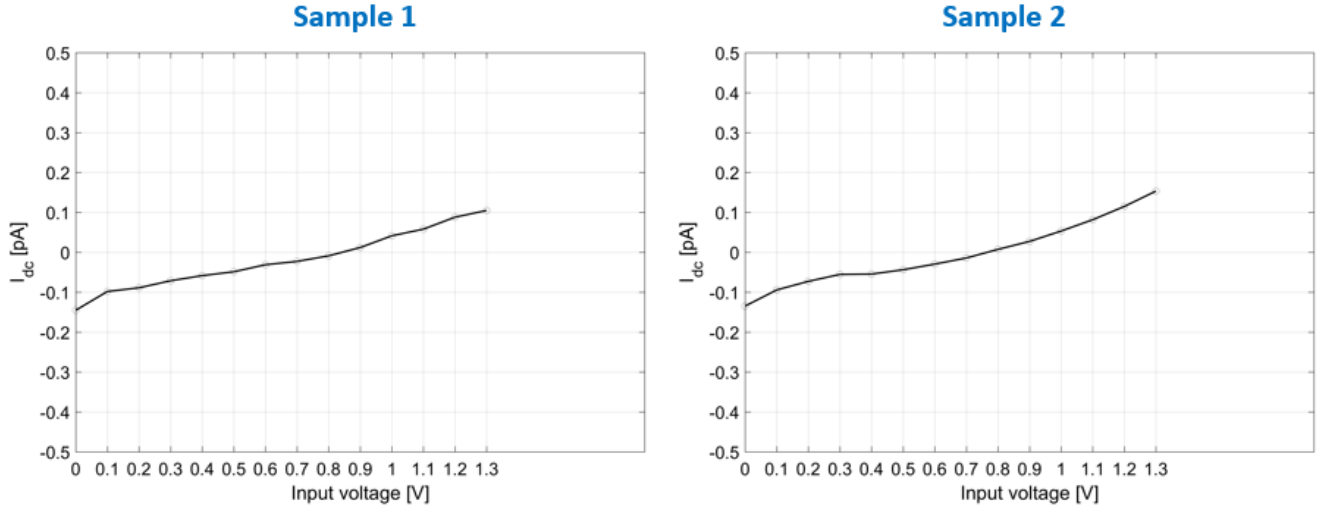


Figure 5-6: Plot of measured input leakage current of 2 samples

The total input current for V_{in}=0V-1.3V is around 250fA for both chips. The expected input current was 50fA. To check if the package is also leaking, the experiment was repeated with an empty package. The measurement result is shown in Figure 5-7.

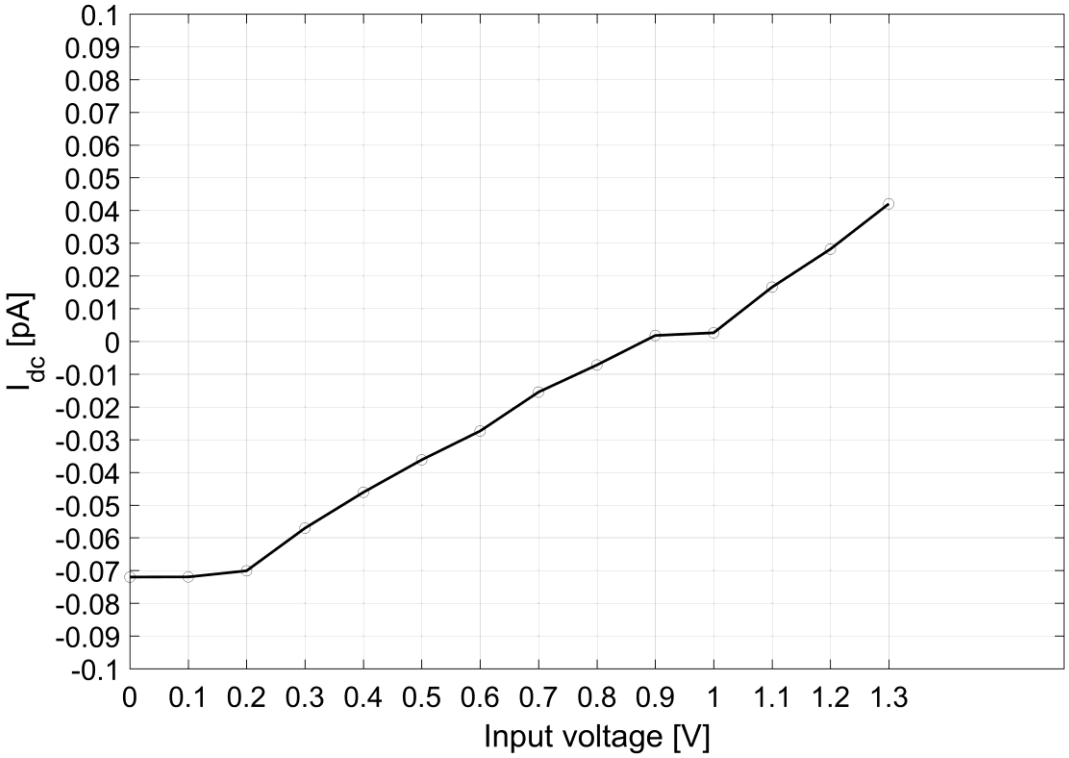


Figure 5-7: Leakage from the 28-pin empty package

The leakage of the 28 pins empty package measured is 150fA which does not satisfy the requirements. To check if the leakage is different for a package with fewer pins, the same experiment was performed with a 24-pin empty package. Figure 5-8 shows the input leakage current measurement with the 24-pin empty package.

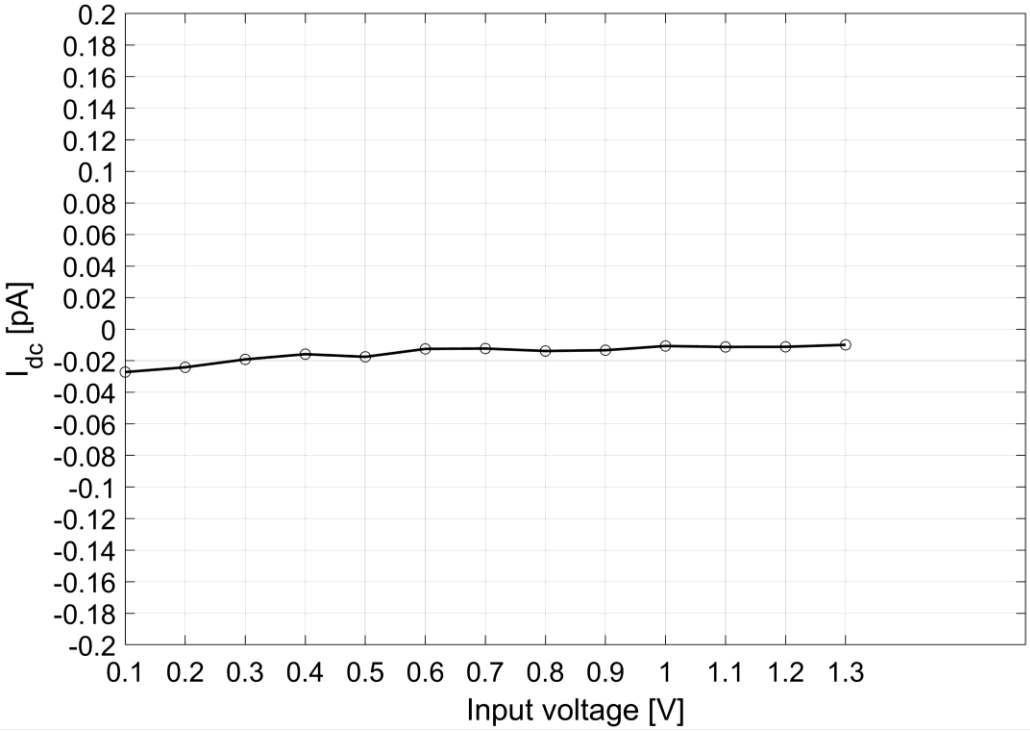


Figure 5-8: Leakage from 24-pin empty package

The leakage of the 24-pin package is around 10fA which is considerably lower than the leakage of the 28-pin package and the expected value of the input current of the chip. As the next step, the chips were bonded in a 24-pin DIP package, and the input current of two samples was measured.

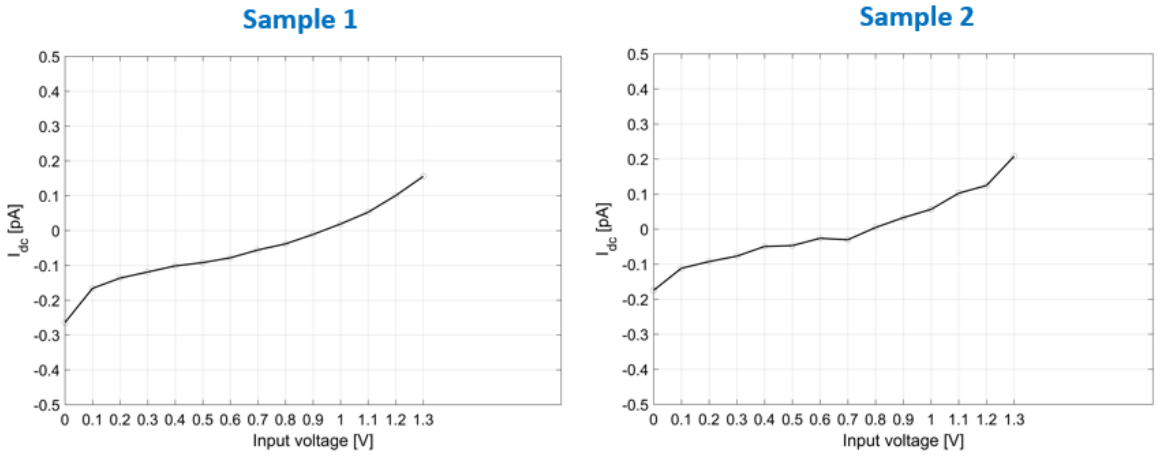


Figure 5-9: Input current measurement with 24-pin package

The input current of two different samples was found to be around 400fA, as shown in Figure 5-9, which is 8× more than expected. Moreover, the measured input current is higher than the input current measured with the 28-pin package. To determine whether the packages are becoming leaky when the chip is bonded or the diode's leakage is high, the chips were directly wire-bonded on a PCB, and the input current was measured. By doing this, the input current of the diodes alone could be measured.

To not change the measurement PCB, a daughterboard having the exact dimensions with a standard 28 pin DIP package was designed and implemented as shown in Figure 5-11. The layout of the daughterboard is shown in Figure 5-10. The daughterboard is a two-layered board made of Roger's material. Guarding and via fence techniques described in Chapter 4 have been applied here. Figure 5-12 shows the daughter board plugged into the main PCB. The connection between the daughterboard and the main measurement PCB was realized by using DIP headers.

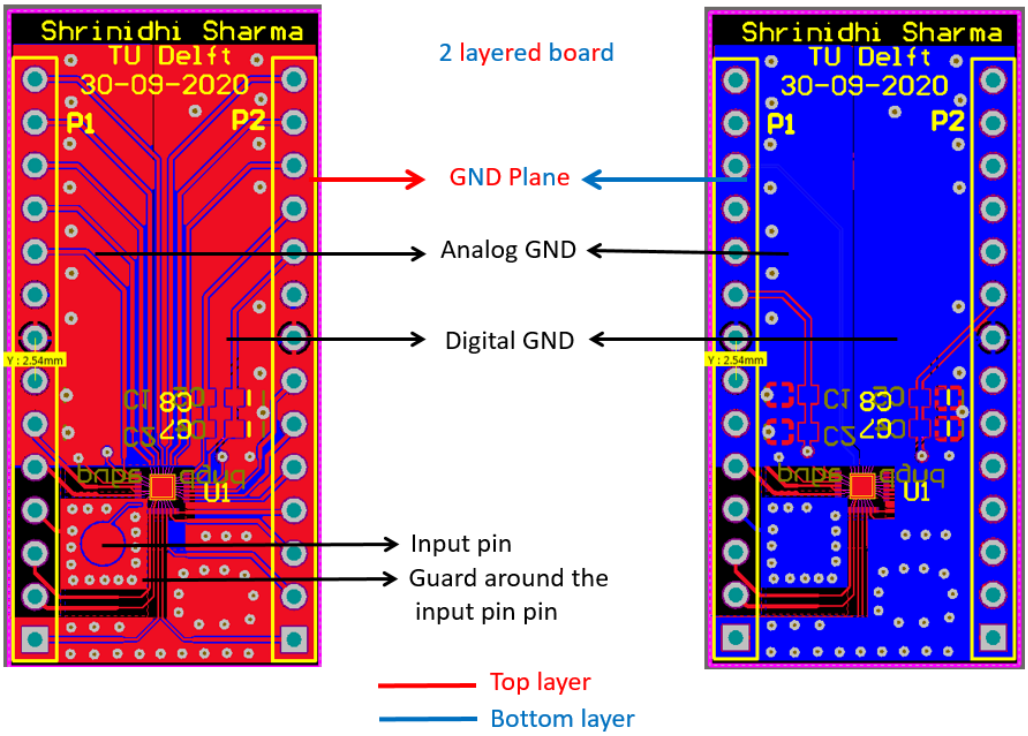


Figure 5-10: PCB layout of the daughterboard

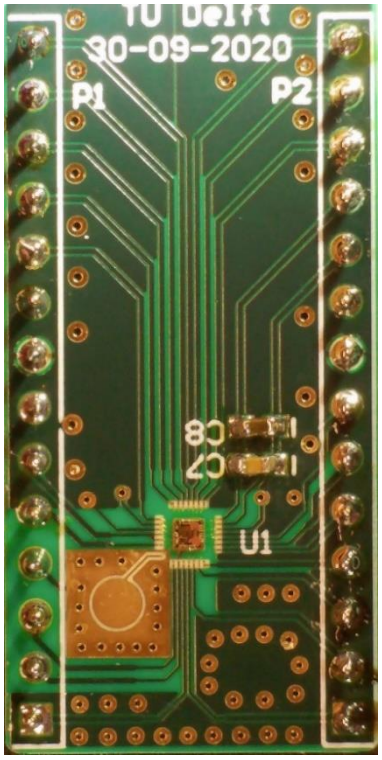


Figure 5-11: Daughterboard PCB

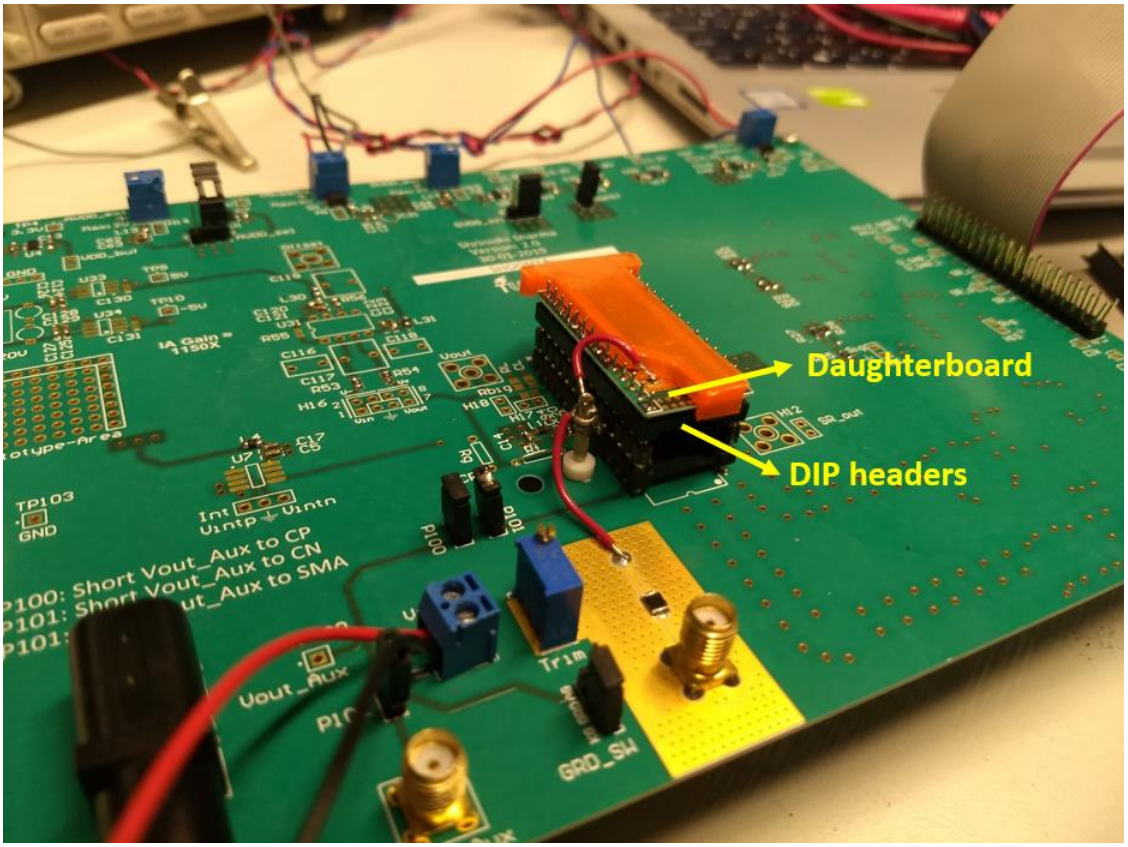


Figure 5-12: Daughterboard plugged into the main PCB and input pin connected to a Teflon standoff

The input pin is connected to a Teflon standoff through a wire which is then connected to the board through a wire. A plastic cap was mounted on the top for shielding from light and to handle the wire bond chips safely during measurements.

Before measurements, the daughterboard was baked in an oven at 80°C for 45 minutes to evaporate the moisture. To check if the input current is affected by the humidity, the input current was measured on the unbaked and baked PCB when the input voltage is 0.9V. Two consecutive measurements were done without any changes. The measurement results with two different samples before baking the daughterboard are shown in Figure 5-13.

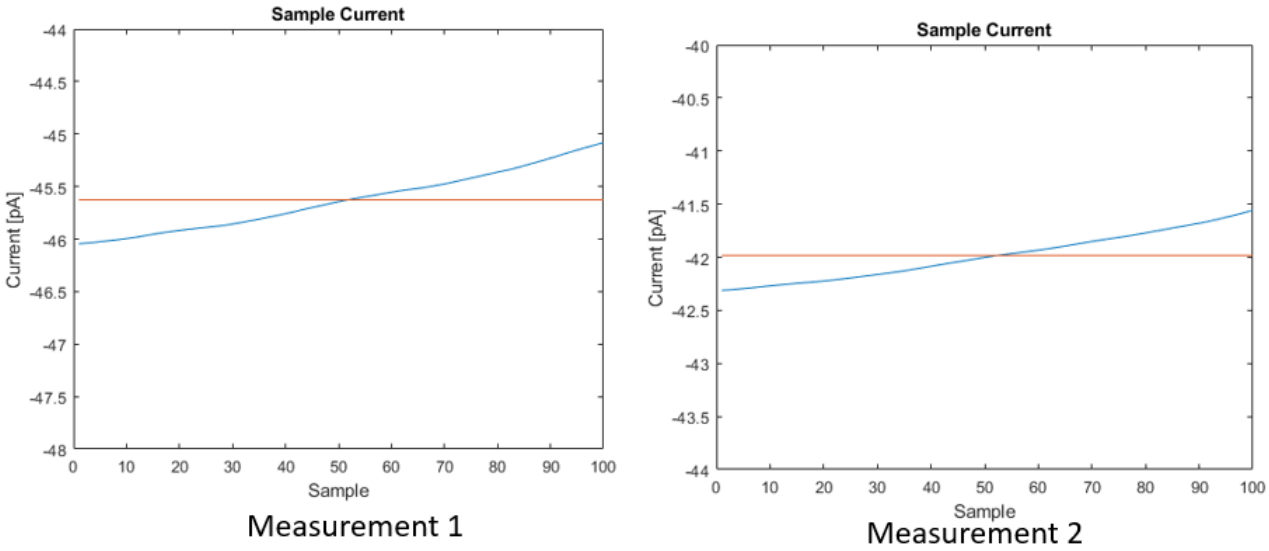


Figure 5-13: Daughterboard measurements before baking

The input current is measured for 100 seconds. The blue line shows the variation of input current every 10 seconds, and the orange line shows the average. The input current is around 45.5pA during 1st measurement and 42pA during the second measurement.

As a next step, the daughterboard was baked in the oven at 80°C for 45 minutes. Figure 5-14 shows the input current measurement for V_{in}=0.9V after baking.

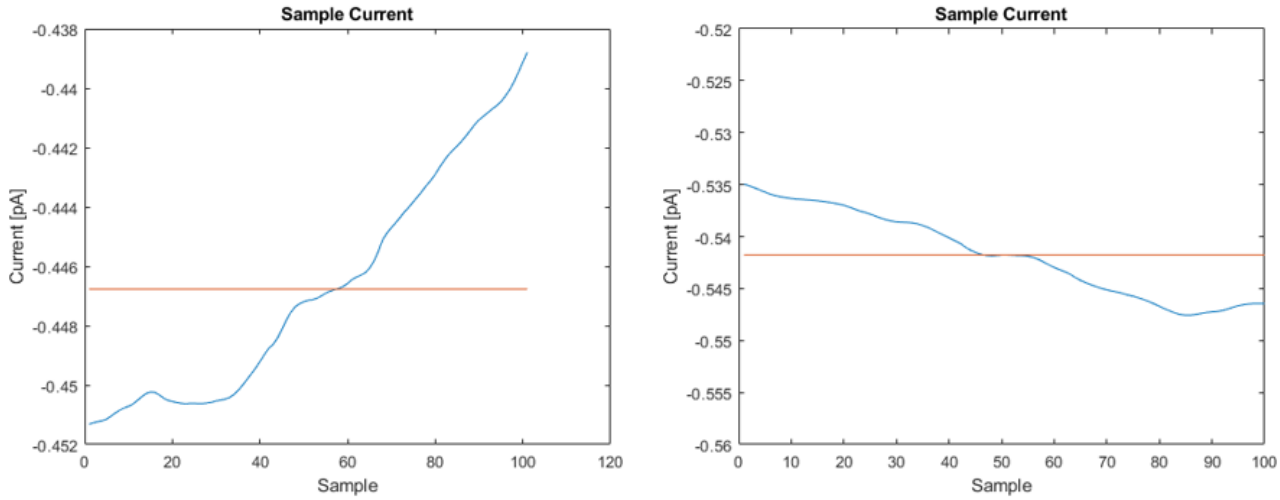


Figure 5-14: Daughterboard measurements after baking

The input current is 0.44pA during the first measurement and 0.54pA during the second measurement, which is 100× smaller than before baking. This result shows that the moisture on the chip has a significant impact on input current measurements.

Figure 5-15 shows the input leakage current measurement of the daughterboard sample for input voltage varying from 0V to 1.8V.

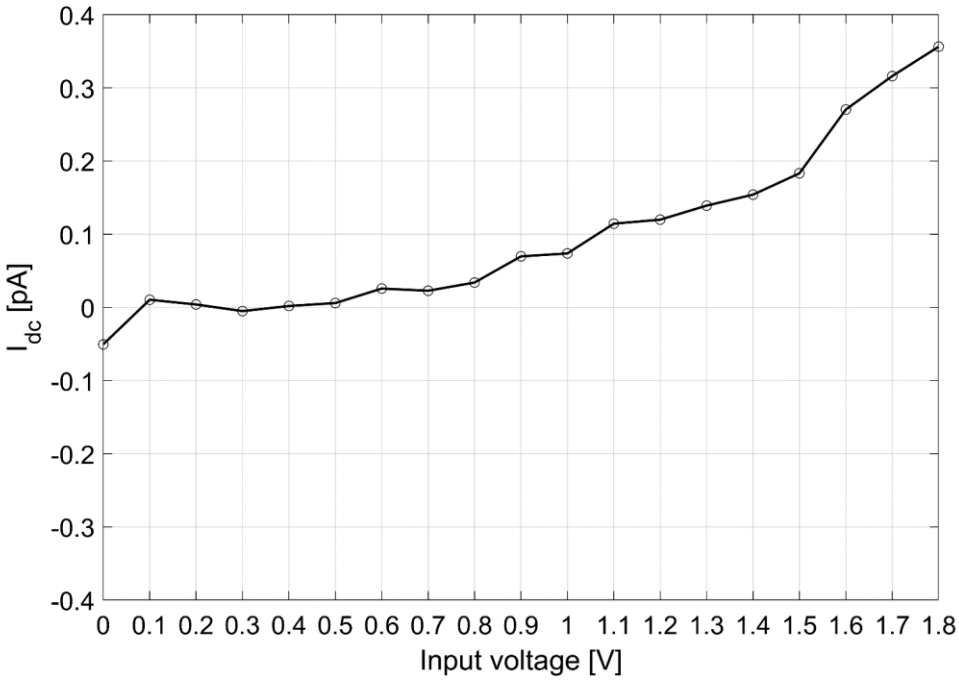


Figure 5-15: Input current measurement of the daughterboard sample

The input current in the voltage range of 0V-1.3V is measured around 150fA, which is still higher than the expected input current value of 50fA. The increase in current at higher input common-mode voltages can be attributed to the parasitic P-sub/N-well diode.

From the above measurement results of the wire-bond samples it can be concluded that moisture is one of the source of leakage which can be solved upon baking

5.5. Miscellaneous Measurements

The offset of the buffer was measured using a Keithley Digital Multimeter. Figure 5-16 shows the buffer's measured offset for eight samples at room temperature for V_{in} varying from 0V to 1.8V. The offset is less than 3mV for the whole input voltage range from 0.1V to 1.8V. This matches with the simulated results shown in section 3.1.3.

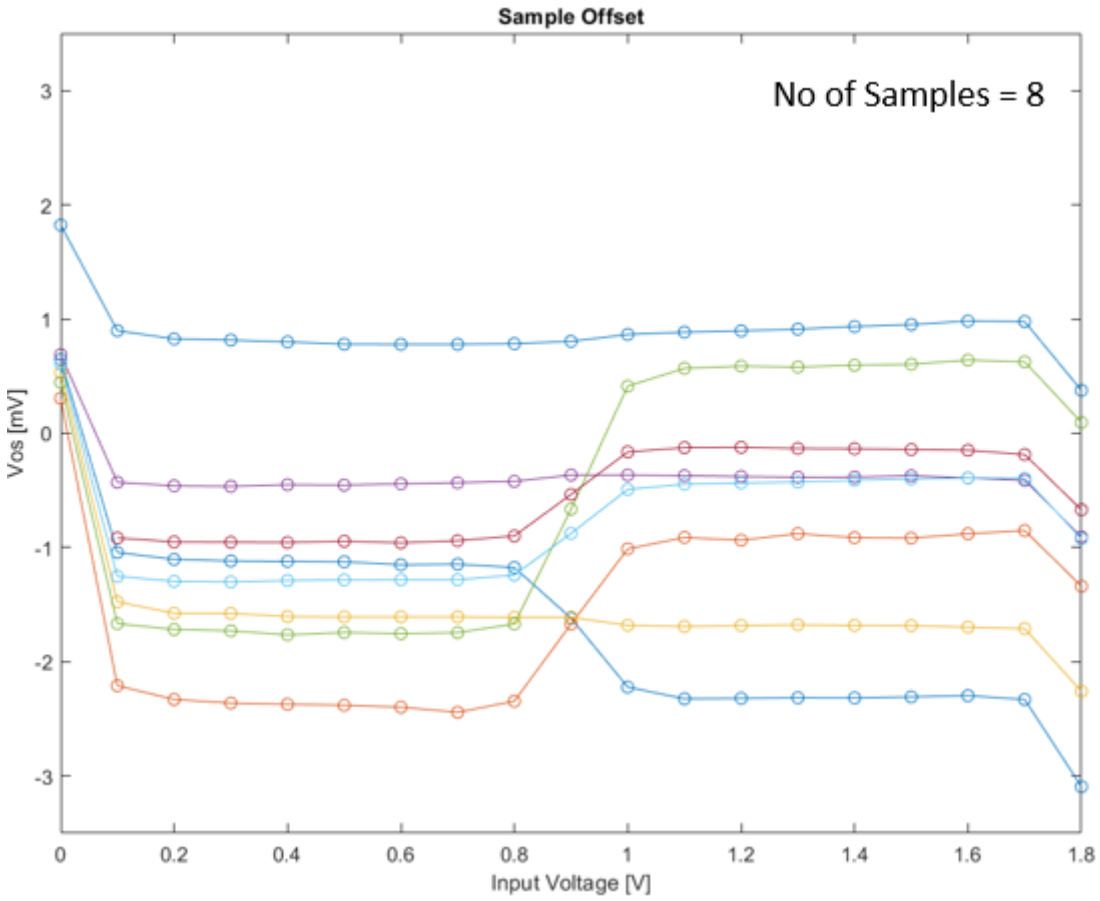


Figure 5-16: Buffer offset

To check the buffer's rail-to-rail capability, a 1.8V_{p-p} signal was applied at 1kHz, and the output was observed in an oscilloscope. Figure 5-17 shows the corresponding measurements

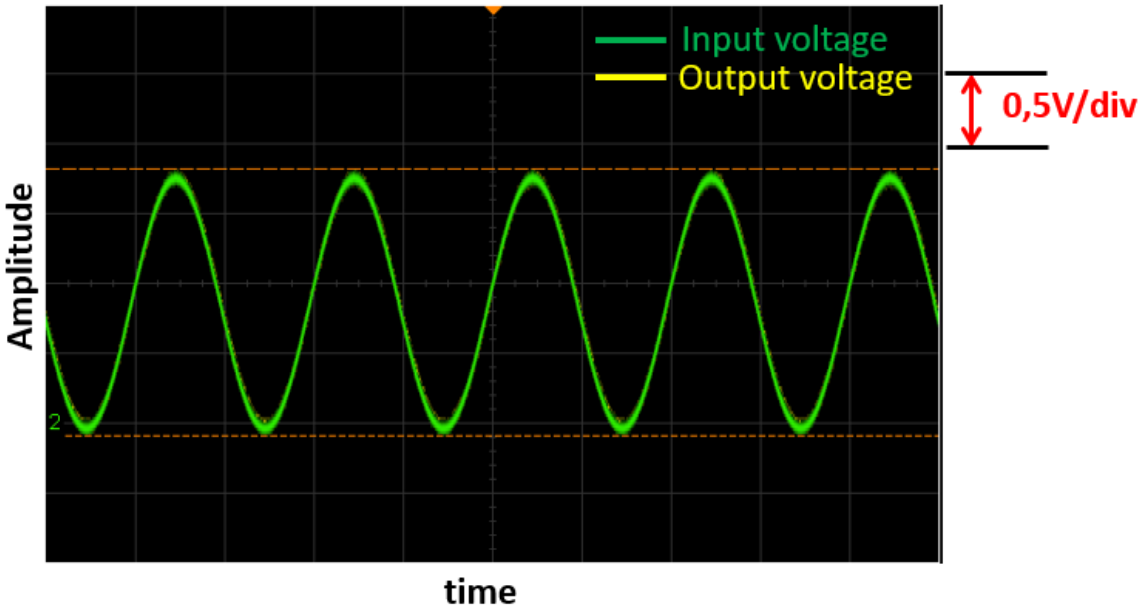


Figure 5-17: Rail-to-rail capability of the buffer with V_{in}=1.8Vp-p

The buffer is proven to be working rail-to-rail. When a 2Vp-p signal was applied, the output starts clipping, as shown in Figure 5-18 since the input signal applied is beyond the supply rail of 1.8V.

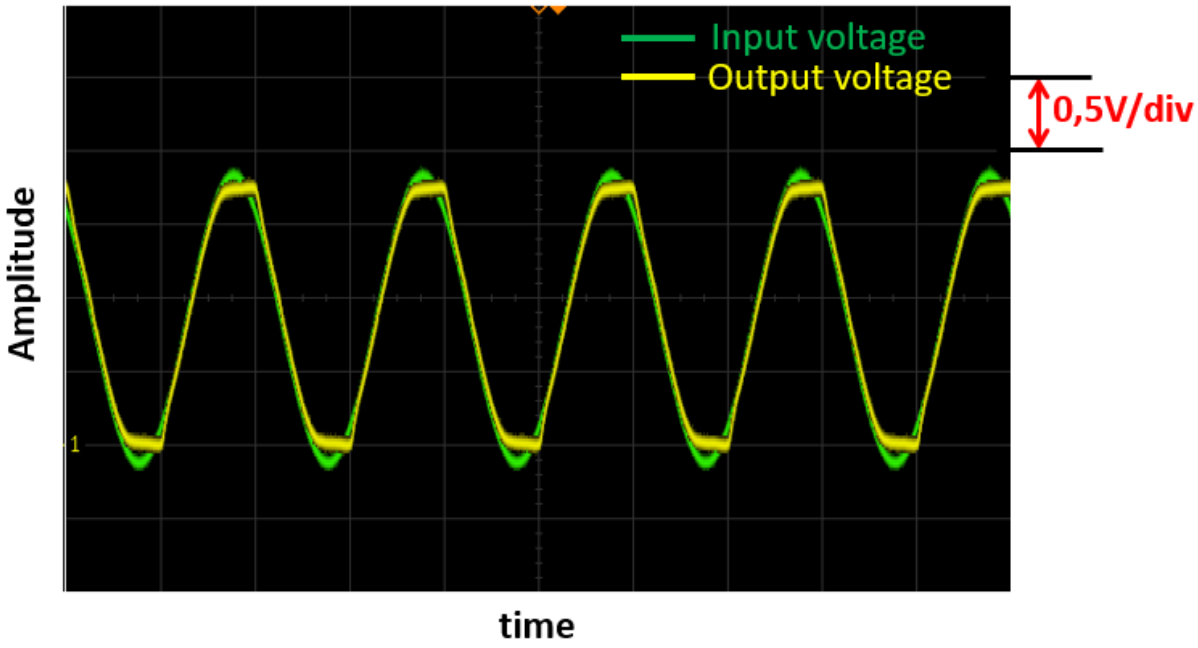


Figure 5-18: Buffer output clipping with V_{in}=2Vp-p

The difference between the output and the input voltage was measured for different frequencies up to 2MHz. The plots are shown in Figure 5-19 and Figure 5-20.

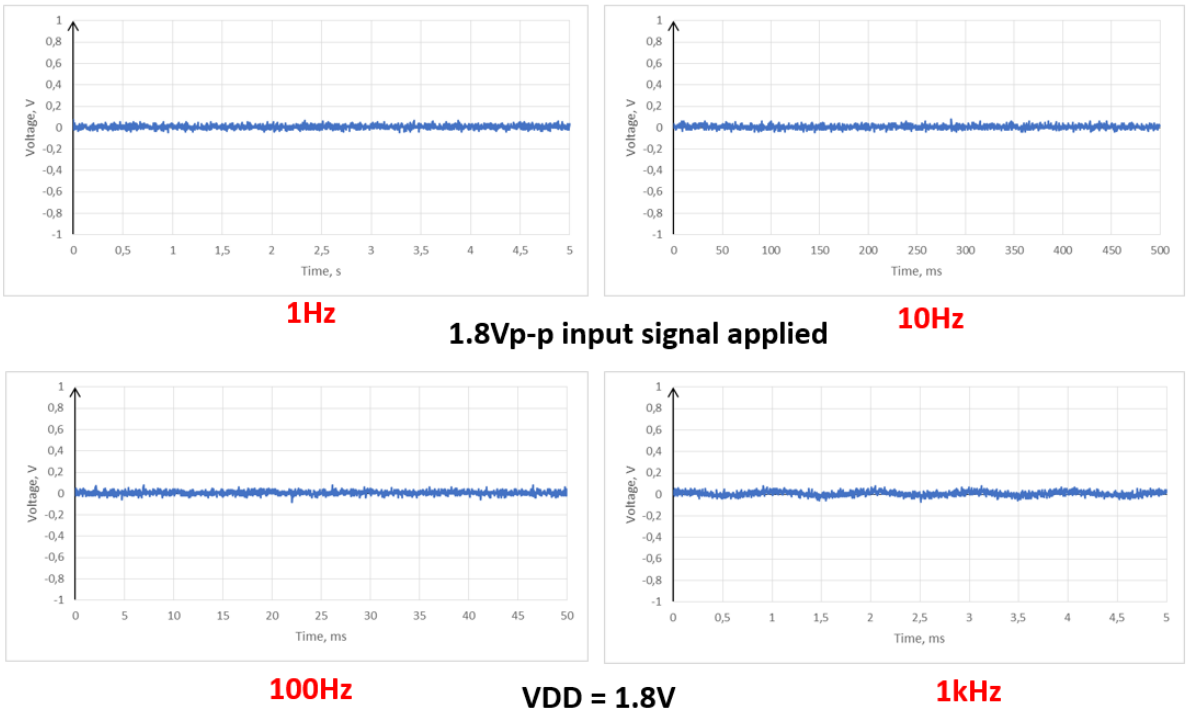


Figure 5-19: V_{out}-V_{in} for 1Hz, 10Hz, 100Hz, and 1kHz

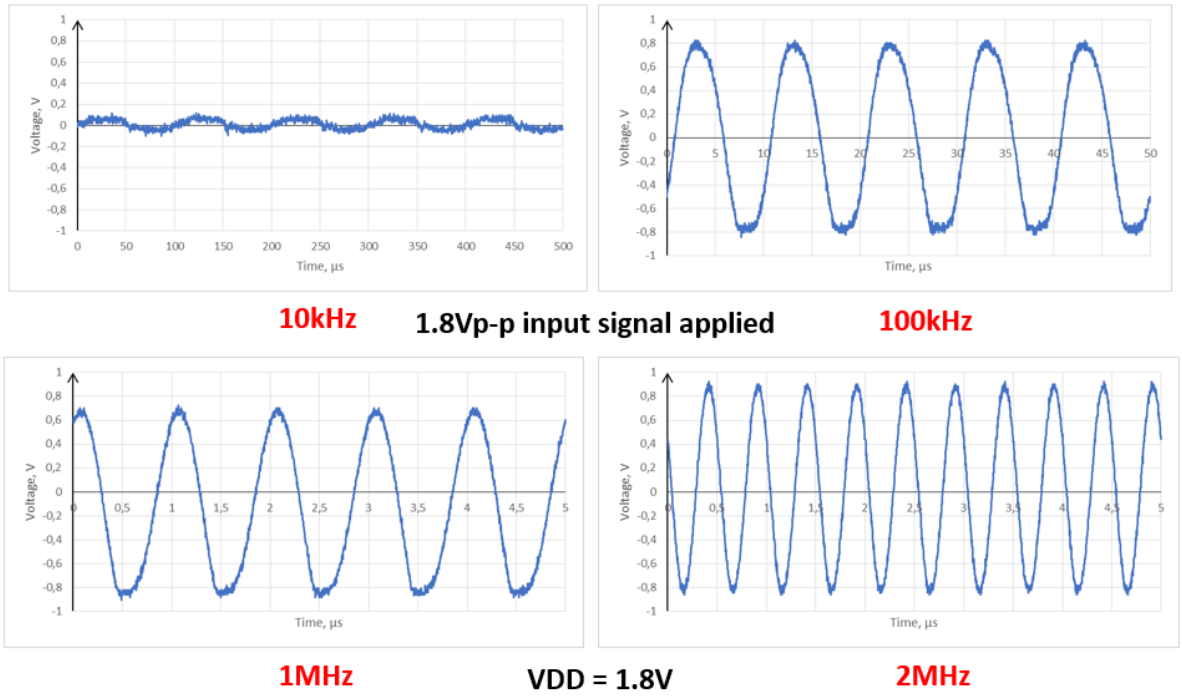


Figure 5-20: V_{out}-V_{in} for 10kHz,100kHz,1MHz, 2MHz

The difference is small up to 10kHz, which is the bandwidth of the amplifier. As frequency increases, the difference increases since the buffer's gain decrease with a rate of -20dB/decade.

5.6. Future work

In this work, an input leakage current up to 150fA is measured. A potential source of leakage at high common mode voltages is the parasitic diodes of P-diodes. In the next design, bootstrapped N-diodes can be used since they don't have the parasitic N-well/P-sub diodes.

Measurements clearly show that the leakage of the packaged samples dominates the input current of the designed chip. This leakage was not reduced by moving to a 24 pin package with increased pin spacing. Existing fA amplifiers utilize 8 pin package with large pin spacing to minimize the package leakage [8], [9]. One of the solutions would be to measure the leakage in a package with a fewer number of pins.

The measurement of one of the wire-bonded samples shows that the leakage current decreases significantly after evaporating the chip's moisture. It was also observed that exposure to the light increases the leakage current. So, it is better for accurate results to clean the PCB, bake them, and do these measurements in a dark room.

This design can be moved to Silicon on Insulator (SOI) process. Since the substrate is not present, parasitic diodes are absent, hence no leakage path. Therefore it is possible to get the ultimate low leakage performance.

6. Conclusion

In this thesis, the design, implementation, and measurement of a bootstrapped ESD diode structure for ESD protection are presented. It aims at reducing the input leakage current, which is seen in the standard ESD diode structures. Lower leakage is achieved by adding a series of two diodes to VDD and VSS and biasing the diodes' mid-point by a buffered version of the input voltage [8]. This connection, which is called bootstrapping, ensures that the voltage across the diodes connected to the input pin is nearly zero and reduces the leakage through it.

The low leakage bootstrapped ESD diode structure is implemented in a standard TSMC 180 nm MS/RF CMOS technology. First, two kinds of diodes were taped out, and their I-V characteristics were measured using an external buffer. From these measurement results, the specifications for the auxiliary buffer design, which will be used for bootstrapping the diodes, were determined. The auxiliary buffer was designed to meet these specifications. It also consumes less power and area than the AZ amplifier since it is used only for the bootstrapping of the diodes. The designed auxiliary buffer can operate rail-to-rail which was confirmed by the measurements. The auxiliary buffer was integrated with the ESD diode structure along with the already existing AZ amplifier and taped out. The integrated circuit with the bootstrapped ESD diode structure and the auxiliary buffer was characterized.

One of the main challenges is the measurement of the low current. Extreme care was taken both at the chip level during circuit design, layout design, and during the structural design of PCB to minimize the stray leakage. PCB design included guarding, shielding, and via-fence techniques, making the bare PCB leakage well below 20 fA. However, the measurement of input current of < 50fA was limited by the measurement setup (cleaning, baking, and measuring in a dark room) and a large number of pins on the package.

Although we were unable to measure the expected low leakage current of 50fA, this thesis acted as a good starting point or groundwork for the future design of low input current ESD protection circuit and the measurement of low input current.

7. References

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