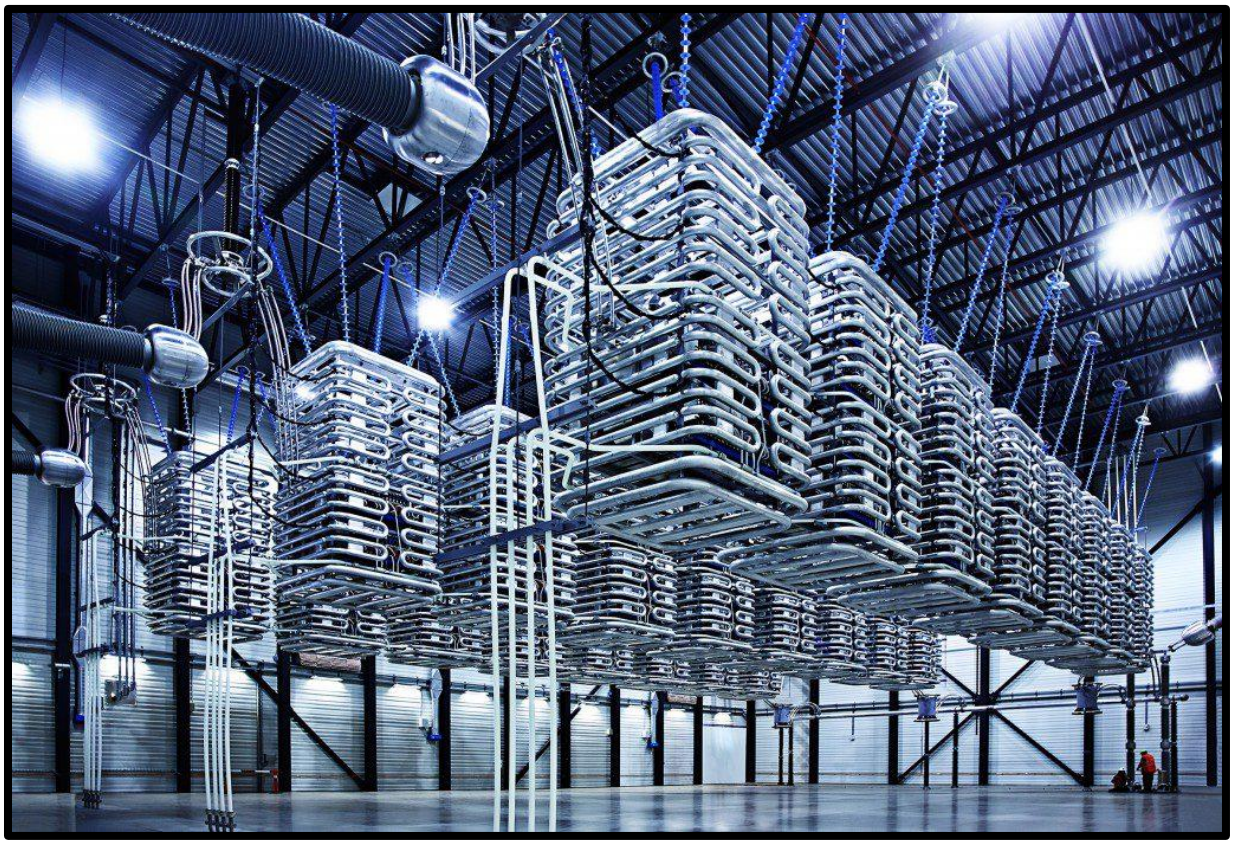
Multi-port DC hub based on the Modular Multilevel Converter for Multi-terminal HVDC grids



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Multi-port DC Hub based on the Modular Multilevel Converter for Multi-terminal HVDC grids

By

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in partial fulfilment of the requirements for the degree of

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TU Delft

To the memory of my beloved grandmother,

Despoina

Contents

Abstract

It is expected that DC grids will evolve into large meshed networks, which will have multiple DC voltage levels. Two DC grids operating at different voltage levels could be interconnected using a DC-DC converter. The role of the DC-DC converter in meshed DC networks is similar to the role of a transformer in traditional AC systems. The DC-DC converter could take a range of functions in DC grids. The DC-DC converter should prevent the propagation of DC faults and should also have the ability to isolate DC faults. Because of its high cost, the DC-DC converter cannot be used as DC breaker in meshed DC grids, but it can be strategically placed in the DC grid to provide protection zone separation. In case multiple HVDC (High Voltage Direct Current) lines need to be interconnected, a multiport DC-DC converter should be used. The DC hub is a multiport DC/DC converter which consists of an inner AC circuit and AC/DC converters interfacing each HVDC line. The main goal of the DC hub is the interconnection of multiple HVDC lines operating at different voltage levels and with different DC grid configurations.

In this thesis, the operation of a DC hub based on the MMC (Modular Multilevel Converter) converter was investigated. A three-port MMC-based DC hub was simulated using *Matlab/Simulink.* An important contribution of this thesis is a comparison of different DC hub topologies which could be used for the interconnection of multiple HVDC lines. Several designs for the inner AC circuit are suggested and the advantages and disadvantages of each recommended design are described in detail. Furthermore, a methodology is presented for the clearing of AC faults within the DC hub and the protection of the system during the fault. An AC fault within the DC hub should be cleared by opening the AC circuit breaker of the faulted port. A methodology is also presented for the safe connection or disconnection of additional ports from the DC hub. Any port should be easily connected or disconnected from the DC hub without affecting the operation of the other ports. The DC hub should also offer connection points to allow the interconnection of more ports. Finally, the operation of the DC hub is investigated when generation or consumption units are connected to its inner AC circuit. In case the DC hub is used for the interconnection of multiple offshore HVDC cables, the loads of the offshore platform or a nearby offshore wind farm could be directly connected to its inner AC circuit.

With the concepts analysed in this thesis, HVDC network system designers will be able to select the most suitable DC hub topology for the interconnection of multiple HVDC lines, use a methodology for the clearing of AC faults within the DC hub, use a methodology for the safe connection or disconnection of ports and understand the design limitations of the DC hub when generation or consumption units are connected to its AC side.

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Michalis Poikilidis

Delft, The Netherlands

September 5, 2017

1.Introduction

1.1 Motivation

It is expected that DC grids will evolve into large meshed networks, which will have multiple DC voltage levels. For this reason, a DC/DC converter will be needed in order to interconnect two DC grids operating at different voltage levels. One possible DC/DC application could be the interconnection of DC cables (which have DC voltage up to 600 kV) with overhead lines (which may have higher DC voltage levels). Given that the existing HVDC (High Voltage Direct Current) links have wide range of highly optimized DC voltage levels, their integration into the DC grid will require DC/DC converters. It is also expected that medium-voltage DC grids (like those with offshore wind farms) will need to be integrated into the DC grid and their connection with the DC grid will require high-stepping ratio DC/DC converters. The role of the DC-DC converter in DC grids is similar to the role of the transformer in traditional AC systems [54].

A DC/DC converter is a versatile device, which can take a range of functions in DC grids. The DC/DC converter should prevent the propagation of DC faults and should also have the ability to isolate DC faults. Because of its cost, the DC-DC converter cannot be used as DC circuit breaker but it can be strategically placed in the DC grid to provide protection zone separation [54].

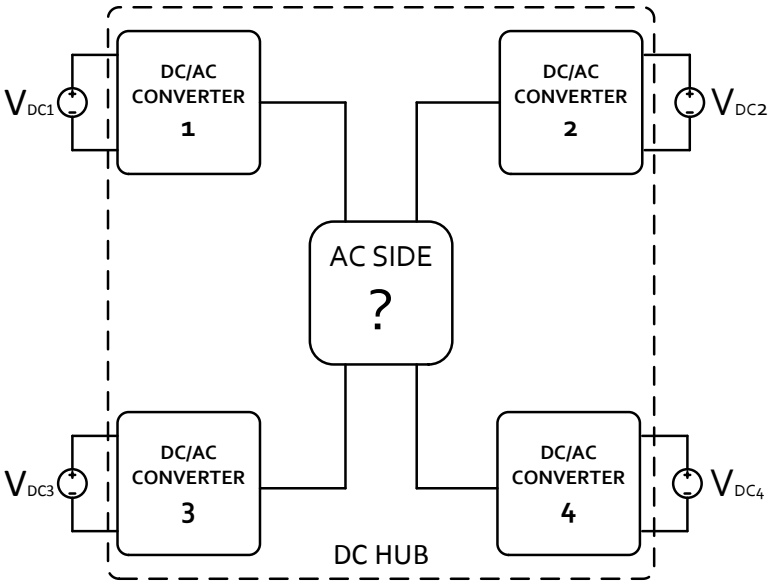


Figure 1.1 Four-port DC hub topology.

The DC hub is a multiport DC/DC converter, which consists of an inner AC circuit and AC/DC converters interfacing each DC line. Figure 1.1 shows the topology of a four-port DC hub. The inner AC circuit of the DC hub may contain transformers, LCL filters and AC circuit breakers for port isolation. The inner AC circuit should operate at high frequencies. In this way, the size of its components (filters, transformers etc) and the footprint of the system would be smaller. A multiphase topology would increase the power transfer capability of the DC hub. It would also increase its reliability and redundancy, given that a faulted phase could be replaced by a standby

phase. The inner control systems of the DC hub will be complex and they should manage the power flow and stability of the isolated inner AC circuit. The interconnected DC lines could have different voltage levels and different DC link configurations. In case a DC fault occurs at any port of the DC hub, the fault can be easily isolated by opening the mechanical AC circuit breaker of the faulted port [54].

The DC hub could be viewed as a DC transformer in DC grids, which has the following functions:

- Voltage stepping between two interconnected DC lines
- Power flow control on each DC line
- DC fault isolation on each line
- Connection points for expansion. Any number of additional DC lines can be connected to the DC hub

Multiple DC hubs will be required for large, geographically dispersed grids, but the exact number of DC hubs will be determined using complex optimization while considering technical performance, reliability, power security, costs and losses [54].

1.2 Research questions

The key research questions this thesis addresses are:

- Which is the most appropriate design for the inner AC circuit of the DC hub?
- How does the connection/disconnection of a port affect the normal operation and stability of the system?
- How do AC faults within the DC hub affect the normal operation and stability of the system?
- How could the DC hub be expanded to allow the interconnection of multiple ports?
- Could generation or consumption units be connected to the inner AC circuit of the DC hub?

As mentioned in section 1.1, the main goal of the DC hub is the interconnection of multiple HVDC lines operating at different voltage levels and with different DC grid configurations. In case the voltage levels of the DC lines are different, the use of transformers may be necessary. Otherwise, in case the voltage levels of the DC lines are similar, the lines could be interconnected directly or using LCL filters. Several designs for the inner AC circuit of the DC hub will be suggested and the advantages and disadvantages of each recommended design will be described in detail. Any port should easily connect and disconnect from the DC hub without affecting the operation of the other ports. For this reason, a methodology will be presented for the safe connection or disconnection of ports. Moreover, the DC hub should offer connection points to allow the interconnection of more lines. The connection of additional ports may affect the operation of the other ports and several design limitations should be taken into account. A methodology will be presented for the connection of additional ports and the effect on the operation of the other ports will also be discussed.

Furthermore, any AC faults within the DC hub should be cleared by opening the mechanical AC circuit breaker of the faulted port. A methodology will be presented for the clearing of AC faults within the DC hub and for the protection of the system during the fault. Finally, the operation of the DC hub will be investigated when generation or consumption units are connected to its inner AC circuit. One possible application of the DC hub is the interconnection of multiple offshore HVDC cables. In this case, the loads of the offshore platform could be directly supplied by the inner AC circuit of the DC hub. Thus, the use of additional generation units for the supply of the loads of the offshore platform would not be needed. Moreover, a nearby offshore wind farm could also be connected to the AC side of the DC hub. In this manner, the use of additional offshore cables for the connection of the wind farm to the onshore grid would not be necessary and the installation cost of the wind farm would be significantly lower.

1.3 Contributions

The original contributions of the thesis are listed below:

- A comparison of different DC hub topologies which could be used for the interconnection of multiple DC lines;
- A methodology for the clearing of AC faults within the DC hub;
- A methodology for the connection or disconnection of additional ports from the DC hub;
- Investigation of the operation of the DC hub when generation or consumption units are connected to its AC side.

1.4 Thesis Outline

To answer the research questions and meet the objectives, the thesis is structured as follows:

Chapter 2 presents the DC hub concept and the candidate DC-DC converter topologies which could be used as the building block of the DC hub. Several DC hub topologies are suggested and the most suitable one for high power applications is indicated. Chapter 3 presents the different types of multilevel converters. This analysis is succeeded by the presentation of the mathematical model of the Modular Multilevel Converter (MMC). The chapter concludes with the presentation of the control strategy and the modulation techniques of the MMC converter. Chapter 4 presents the averaged model of the MMC converter and the different control structures which were implemented in *Matlab/Simulink*. The averaged model of the MMC is subsequently used for all the simulations in this thesis. Chapter 5 presents the different possible DC hub topologies which could be used for the interconnection of multiple DC lines operating at different voltage levels. The DC lines could be interconnected using transformers, LCL filters or directly. The advantages and disadvantages of each topology are discussed and the most suitable topology for the interconnection of DC lines operating at different voltage levels is selected. The selected topology is subsequently used for all the simulations in this thesis. In Chapter 6, a methodology is presented for the connection or

disconnection of additional ports. Moreover, a methodology is suggested for the clearing of AC faults within the DC hub and the protection of the system during the fault. The expandability of the DC hub is also investigated and the necessary actions that should be taken before and after the connection of an additional port are also analysed. In Chapter 7, the operation of the DC hub is investigated when a load or a wind farm is connected to its AC side. Chapter 8 concludes the thesis by answering the research questions which were presented in section 1.2, based on the conducted research. Finally, recommendations for future work are also given in Chapter 8.

2.DC Hub and DC-DC Converter Topologies

2.1 DC Hub Concept

Two topologies are recommended for the interconnection of multiple HVDC lines operating at different voltage levels and with different DC grid configurations. The first alternative is to use DC-DC converters for the interconnection of each pair of lines. As can be seen in Figure 2.1, in case 3 HVDC lines must be interconnected, three DC-DC converters should be used. In this case, the power flow between the lines must be controlled by a reliable communication system. Furthermore, in case an extra HVDC line need to be connected to the DC hub, three additional DC-DC converters should be used, one for the connection of the new HVDC line to each of the existing three. Thus, the cost of this solution would be high and a complex protection mechanism would be required. As a consequence, this alternative is not reliable and has limited design modularity [35].

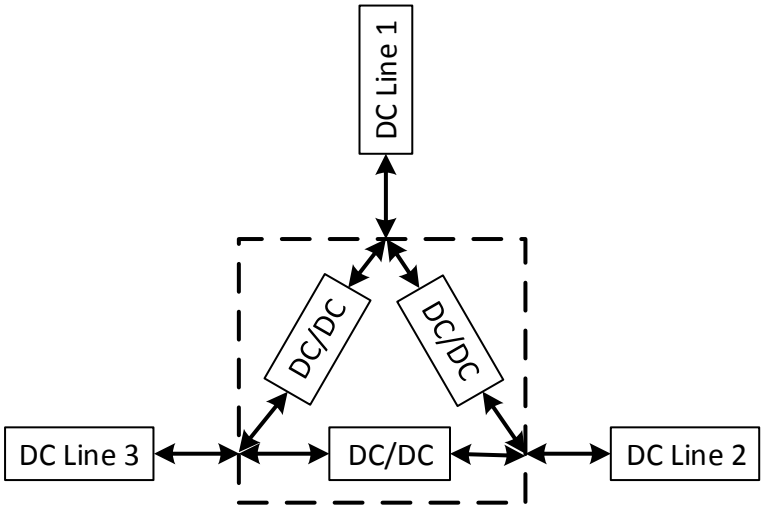


Figure 2.1 Multiple DC-DC converters to interconnect DC lines [35].

A more promising topology which assists the direct connection of all the HVDC lines on a common node can be seen in Figure 2.2. The DC hub is a multi-port DC-DC converter which is used for the interconnection of multiple ports. This topology has many advantages such as reliability and expansion capability. It can be placed in any point of the DC grid and it offers DC voltage transformation, fault ride-through ability through the common AC node and more control options. The DC hub can be used as DC transformer in DC grids, similar to the conventional AC transformer in AC grids. The main objectives of the DC hub are [35]:

- It enables the interconnection of multiple HVDC lines operating at different voltage levels and with different DC grid configurations
- Any HVDC line can controllably exchange power with any other HVDC line which is connected to the DC hub
- Any DC fault can be easily cleared by using the AC breakers of the faulted port
- Any HVDC line can be connected or disconnected from the DC hub without affecting the operation of the DC grid

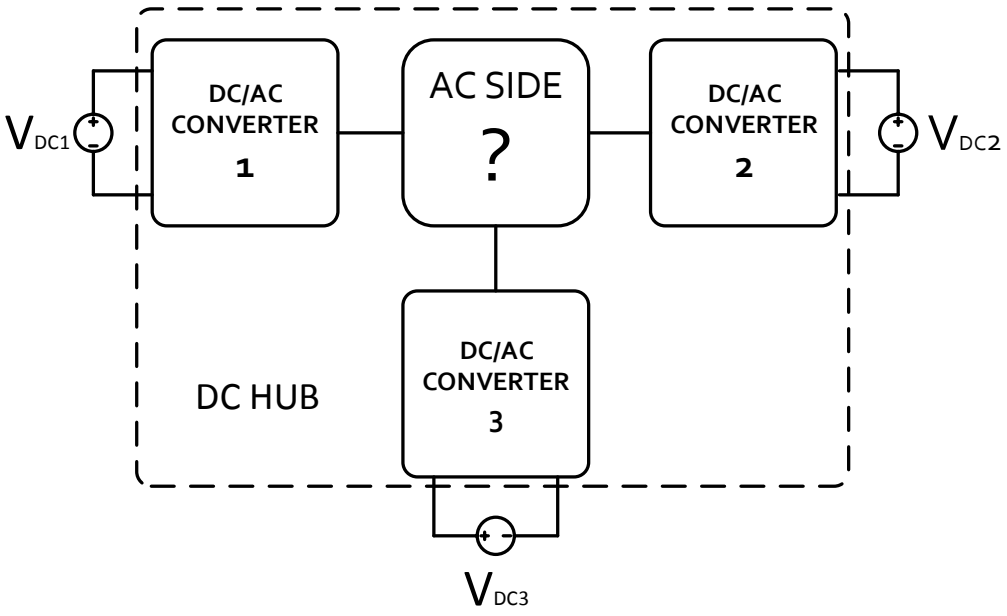


Figure 2.2 DC Hub topology [35].

2.2 DC-DC Converters for HVDC applications

With the increasing energy production from renewable energy resources and the development of voltage source converters, there has been an increasing interest in using multi-terminal HVDC networks and DC grids. Nowadays, DC grids are usually built by interconnecting multiple HVDC lines using DC circuit breakers. However, this topology is not suitable for large DC grids, since a DC fault at any point of the DC grid would cause voltage collapse of the entire system. DC breakers could be used for the isolation of the fault and the protection of the system, but their technology is still at an early stage and they cannot be used in high power, high voltage applications.

DC-DC converters could be used for the interconnection of multiple HVDC transmission lines operating at different voltage levels. In this manner, the propagation of DC faults within the DC grid would be prevented and the reliability of the entire system would be higher.

The DC-DC converter topology which could be used as the building block of the DC hub should have the following characteristics:

- **High power transfer capability**: the DC-DC converter should have high power rating and should be able to withstand high voltage and current stresses.

- **High transformation ratio**: the DC-DC converter should be able to interconnect HVDC lines operating at different voltage levels.

- **Bidirectional power transfer capability**: the DC-DC converter should be able to transfer power in both directions, since the interconnected HVDC lines exchange power and any HVDC line could either export or import power from the interconnected system.

- **Modularity**: The topology of the multiport DC-DC converter should offer connection points to allow the interconnection of more lines.

The DC-DC converters can be categorized as:

- Two-stage (or front-to-front) converters
- One-stage converters

In the two-stage converter topology, the DC lines are interconnected through an intermediate AC link and two DC/AC converters are used. In the one-stage topology, there is no distinct AC link. The main advantage of the one-stage topology is that only one converter is used. As a consequence, the number of semiconductor devices is lower, resulting in lower weight, cost and volume. However, the one-stage converters do not have modular structure and thus, cannot be used as the building block of the DC Hub. For this reason, only two-stage converters will be studied.

Several DC-DC converter topologies which could be used in high power applications are recommended in the literature. Some of the these topologies are the following:

- Hard switched full bridge converter [5]
- Phase-shift full bridge converter [5]
- Series load resonant converter [5]
- Parallel load resonant converter [5]
- Dual active bridge converter [5]
- Thyristor based resonant converter [5]
- HVDC-DC auto transformer (HVDC-AT) [6]
- Push-pull M2DC [7]
- Three-phase dual-active bridge converter [7]

However, these DC-DC converter topologies do not meet all the aforementioned criteria and thus, they cannot be used as the building block of the DC hub. The most promising DC-DC converters which could be used as the building block of the DC hub are presented in the following part of this section.

High power IGBT-based DC/DC converter

A bidirectional DC-DC converter with an LCL filter in the intermediate AC link was introduced in [34]. Although it is a promising topology, it uses thyristors. As a result, its efficiency is low, its controllability is limited and the system cannot be easily expanded to interconnect multiple DC lines. For this reason, as shown in Figure 2.3, the thyristors were replaced by IGBTs to increase the efficiency of the system [72].

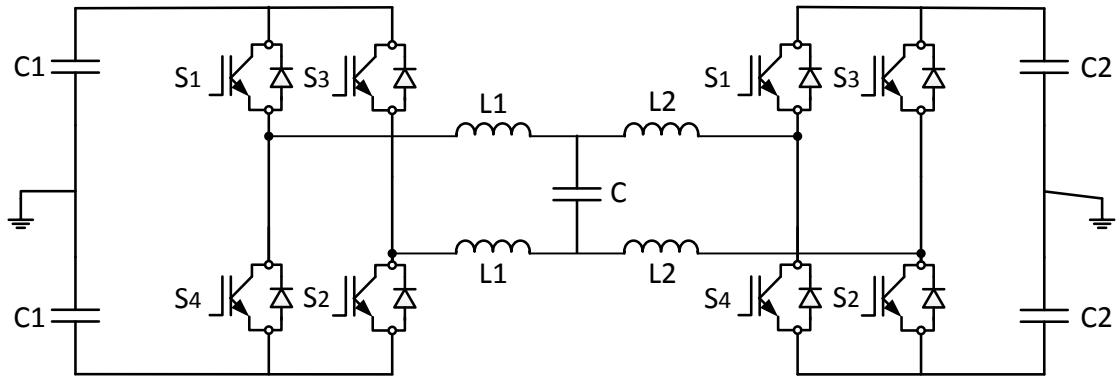


Figure 2.3 High power IGBT-based DC/DC converter [35].

With the appropriate design of the LCL filter, the cost of the L,C components can be kept low and the converter has the ability to keep control even under the worst-case faults. Furthermore, the voltage stresses on the switching devices is low and comparable to the converter topologies using transformers. The ripple of the DC current and the maximum power transfer capability of the converter depend on the number of phases [72]. One drawback of this topology is that it steps the DC voltage symmetrically around the mid-point and thus, it cannot be used with asymmetric monopolar HVDC configuration. Finally, another drawback is that it exhibits low efficiency in small transformation ratios compared to the topologies using transformers.

This converter type has high and bidirectional power transfer capability. It also supports the interconnection of multiple HVDC lines and an additional HVDC line can be easily connected to the intermediate AC link though a dedicated AC/DC converter. However, it exhibits low efficiencies in small transformation ratios and thus, it cannot be used as the building block of the DC Hub.

High Power, low Ratio DC-DC Converter

The topology of the high power, low ratio DC-DC converter can be seen in Figure 2.4. This converter type consists of two 3-phase DC-AC converters. The AC sides of the converters are directly connected without using transformer. Due to the absence of transformer, the cost of this topology is low. As can be seen in Figure 2.4, each phase leg of the DC-AC converter consists of two arms. Each arm consists of series connected full bridge submodules (red elements), a Director Switch (blue elements) and an inductor. The full-bridge submodules are rated for the maximum DC voltage of the system whereas the Director Switch is rated for the maximum DC voltage of the system plus an offset voltage that could result from a DC fault in the system. As a consequence, even without galvanic isolation, a DC fault cannot propagate from one DC side of the system to the other [8].

Each DC-AC converter comprises three phases. In case high power has to be transferred, a multiphase connection could be utilized. The frequency of the AC link should not necessarily be 50 Hz. Higher frequencies, such as 350 Hz, could be used in order to minimize the components size (eg. submodule capacitance). Moreover, given that no load is connected to the intermediate AC link, the waveform of the AC voltage should not necessarily be sinusoidal. Other waveshapes, such as trapezoidal or square-wave could be used. In this manner, both converter losses and components ratings could be optimized [8].

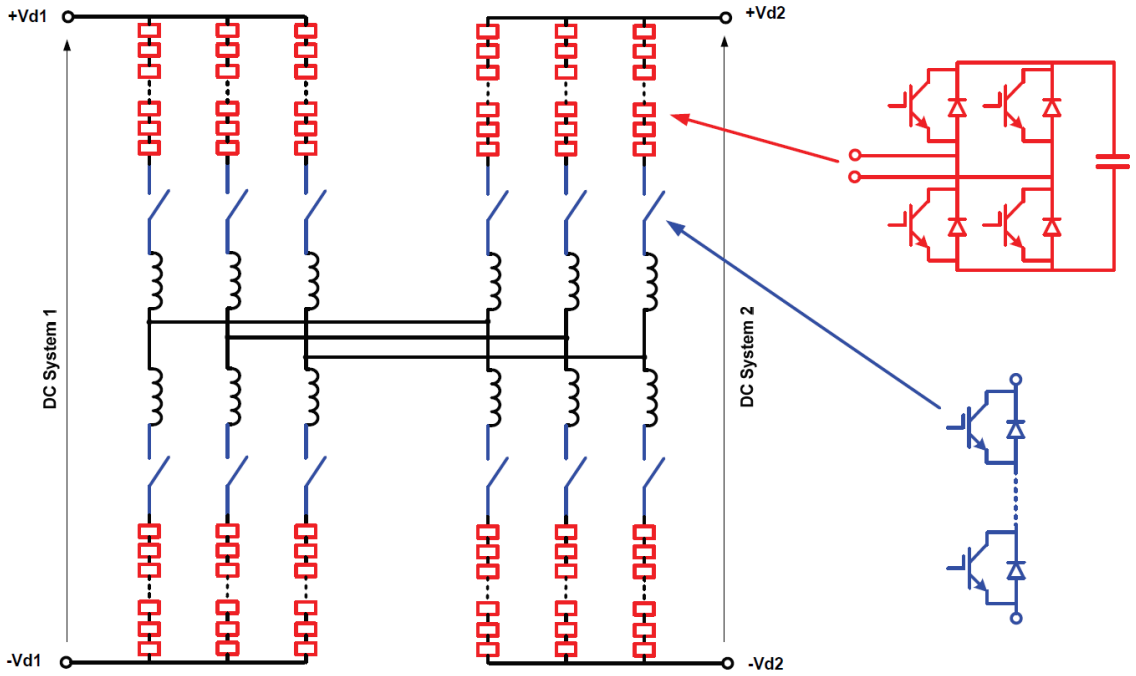


Figure 2.4 High Power, low Ratio DC-DC Converter [8].

In case the voltage levels of the DC lines are much different, a circulating DC current will flow between the two DC systems through the AC link, increasing this way the losses of the system. For this reason, this topology is only suitable for the interconnection of DC lines operating at similar voltage levels.

To summarize, this converter type has bidirectional and high power transfer capability. Due to the absence of transformer, the cost of the system is low. This topology is also suitable for the interconnection of multiple HVDC lines since an additional HVDC line can be easily connected to the AC link through a dedicated DC-AC converter. However, this topology cannot be used when the voltage levels of the DC lines are much different and it is only suitable for low transformation ratio applications. Thus, it could be used as the building block of the DC hub only in case the voltage levels of the DC lines are similar. Otherwise, the efficiency of the system would be significantly reduced.

LCC/VSC DC-DC Converter

The circuit diagram of the LCC/VSC DC-DC converter can be seen in Figure 2.5. This DC-DC converter type consists of an LCC DC-AC converter and a VSC DC-AC converter. The AC sides of the converters are connected through a three phase transformer. In case high power has to be transferred, a multi-phase AC connection could be utilized. On the other hand, single phase connection could be used for medium power transfer levels.

The VSC converter always keeps the same voltage polarity whilst the power transfer can be reversed by changing the direction of the DC current. On the other hand, in the LLC scheme, the direction of the power transfer can be reversed by changing the polarity of the DC voltage [8].

As can be seen in Figure 2.5, each phase leg of the VSC converter consists of two arms. Each arm consists of series connected full-bridge submodules (red elements), a Director Switch (blue element) and an inductor. The Director Switch is rated for the DC voltage V_{d2}. On the other hand, as shown in the same figure, each arm of the LCC converter consists of series connected full-bridge submodules and an inductor. Given that each full bridge submodule can provide both positive and negative DC voltage, energy can be transferred from the DC side of the LCC to the AC link irrespective of the polarity of the DC voltage V_{d1} [8].

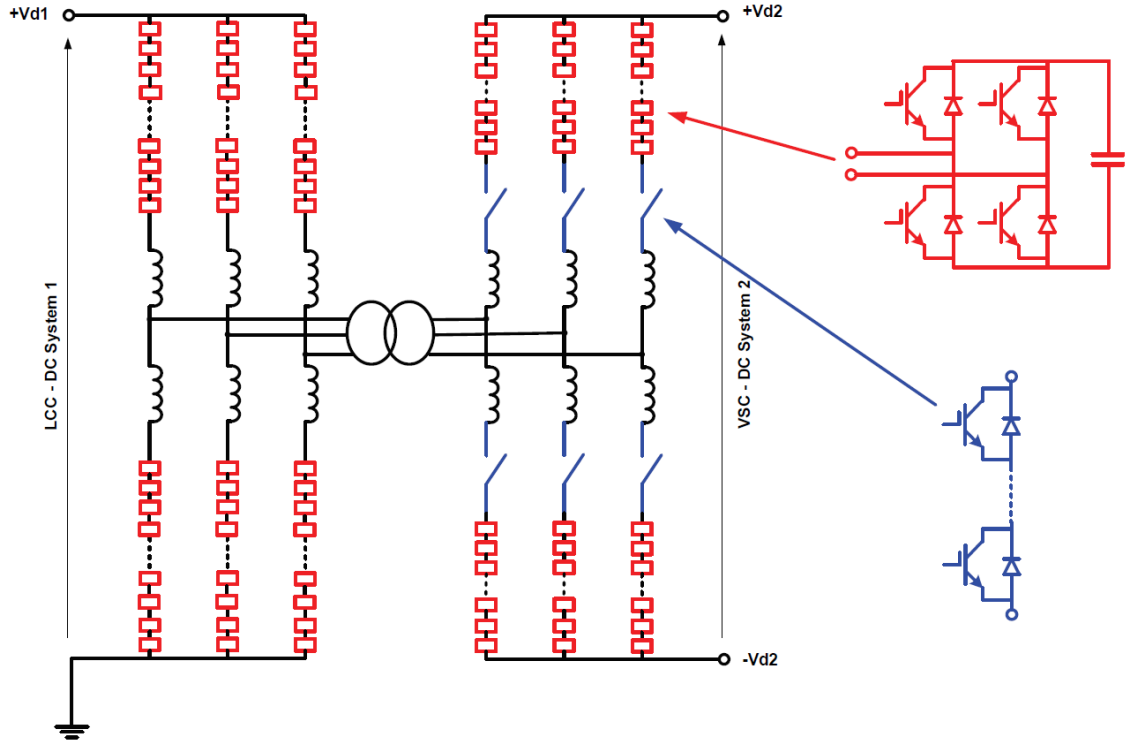


Figure 2.5 LCC/VSC DC-DC Converter [8].

The frequency of the AC voltage should not necessarily be 50 Hz. Higher frequencies, such as 350 Hz, could be used. In this way, the size of the transformer and the submodule capacitors could be reduced. However, the selection of a high operating frequency would increase the losses of the converter and thus, its efficiency would be reduced. As a result, the selection of the operating frequency of the intermediate AC link will be a trade-off between the footprint of the system and the efficiency of the converter.

This converter type has high and bidirectional power transfer capability. It also has high transformation ratio and thus, it enables the interconnection of multiple HVDC lines operating at different voltage levels. For this reason, it could be used as the building block of the DC hub. However, the VSC technology is usually preferred over the LCC. Finally, this converter type could not be used in applications in which all the interconnected DC lines have firm voltages.

MMC-based LCL DC-DC Converter

The Modular Multilevel Converter (MMC) offers higher reliability, better power transfer quality and higher efficiency. Having modular structure, it aids the DC-DC converter to have high efficiency for all transformation ratios. An MMC-based LCL converter was presented in [74] with unity transformation ratio, high efficiency and fault ride-through capability. The topology of the MMC-based LCL DC-DC converter can be seen in Figure 2.6.

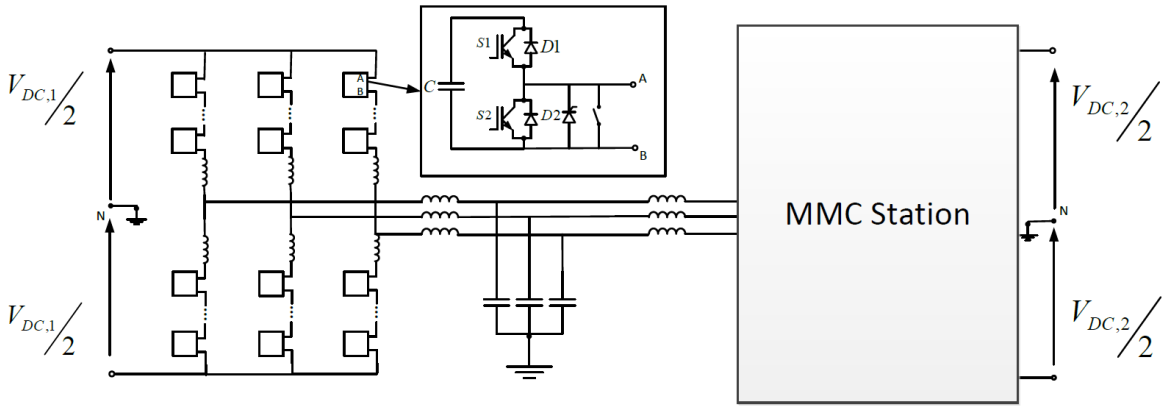


Figure 2.6 MMC-based LCL DC-DC converter [35].

This converter type has high and bidirectional power transfer capability. It is also suitable for the interconnection of multiple HVDC lines. However, it exhibits low efficiency in high transformation ratios, as will be explained in detail in Chapter 5. For this reason, it can be used as the building block of a DC hub which interconnects multiple HVDC lines operating at similar voltage levels.

Isolated modular DC-DC converter

The MMC-based DC-DC converter topology using transformer can be seen in Figure 2.7. The main advantages of this topology over the two level DAB topology are the lower switching losses and the lower voltage stresses on the isolation transformer. Moreover, at black start and during DC faults, the full modulation index is available for the control of the voltage of the AC link. The use of the isolation transformer minimizes the circulating reactive power in the AC link and offers better switching utilization. The main drawback of the suggested topology is the larger footprint due to the use of the transformer. Different AC frequency levels and AC voltage waveforms could be used. The selection of the operating frequency will be a compromise between the footprint of the converter and its efficiency (recommended range 300-500 Hz). The selection of the AC voltage level will also be a trade-off between the volume and the efficiency of the converter. The higher the AC voltage level, the higher the number of series-connected power devices will be (cell capacitors, IGBTs, diodes). On the other hand, low AC voltage values lead to high AC current values, and thus, to lower efficiency (considering constant power transfer level). The AC voltage waveform could be different than sinusoidal, such as triangular or trapezoidal, since no loads are connected to the AC link and the quality of the AC voltage is not very important. The main advantage of using trapezoidal voltage waveform is the lower submodule capacitor energy requirements, and thus, the smaller footprint of the system [75].

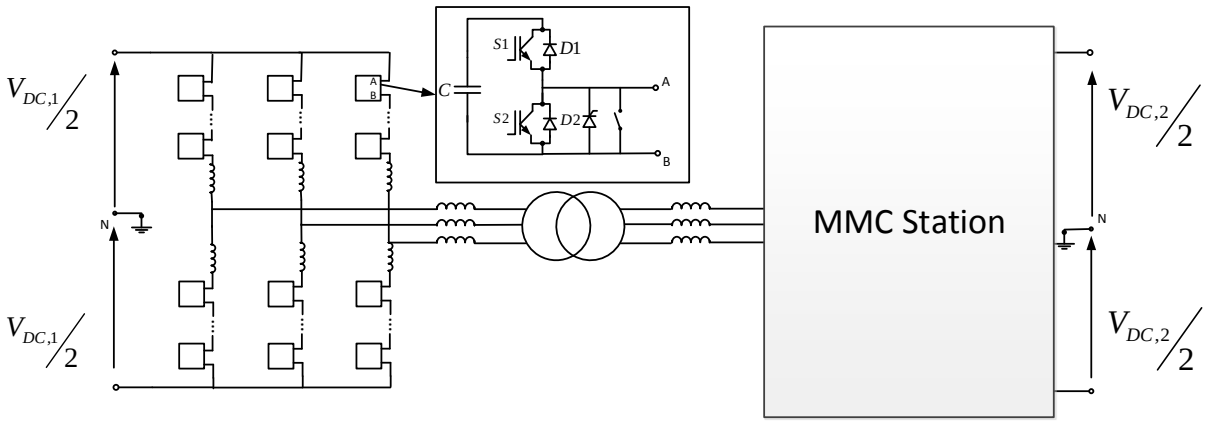


Figure 2.7 Isolated modular DC-DC converter [35].

The suggested DC-DC converter topology has high and bidirectional power transfer capability. Due to the use of transformer, it can be used for the interconnection of multiple HVDC lines operating at different voltage levels. Therefore, this DC-DC converter topology could be used as the building block of the DC Hub.

Alternate Arm MMC

The alternate arm converter could replace the traditional MMC converter in one at least of the ports of the DC-DC converter topology. The recommended topology is presented in Figure 2.8 [15]. The design of this topology leads to more efficient devices utilization because there is no path for circulating currents. Furthermore, the voltage rating of the converter is lower due to the fact that the voltage is shared between the switches and the wave shaping circuit. In contrast to the traditional MMC, the alternate arm MMC has DC fault blocking capability and smaller footprint. However, its efficiency is lower due to the larger number of switches in the conduction path.

This DC-DC converter topology has high and bidirectional power transfer capability. It is also suitable for the interconnection of multiple HVDC lines operating at different voltage levels and thus, it could be used as the building block of the DC hub.

Overall, the review of the DC-DC converter topologies showed that a few designs could be used as the building block of the DC hub. The most promising design is the MMC-based DC-DC converter. In case there is need for galvanic isolation and the voltage levels of the interconnected DC lines are different, a transformer could be placed in the intermediate AC link. The use of transformer offers better switching devices utilization and minimizes the circulating reactive power in the AC link, especially in case the DC voltage levels of the interconnected DC lines are much different. On the downside, the use of transformer increases the volume, weight and cost of the system.

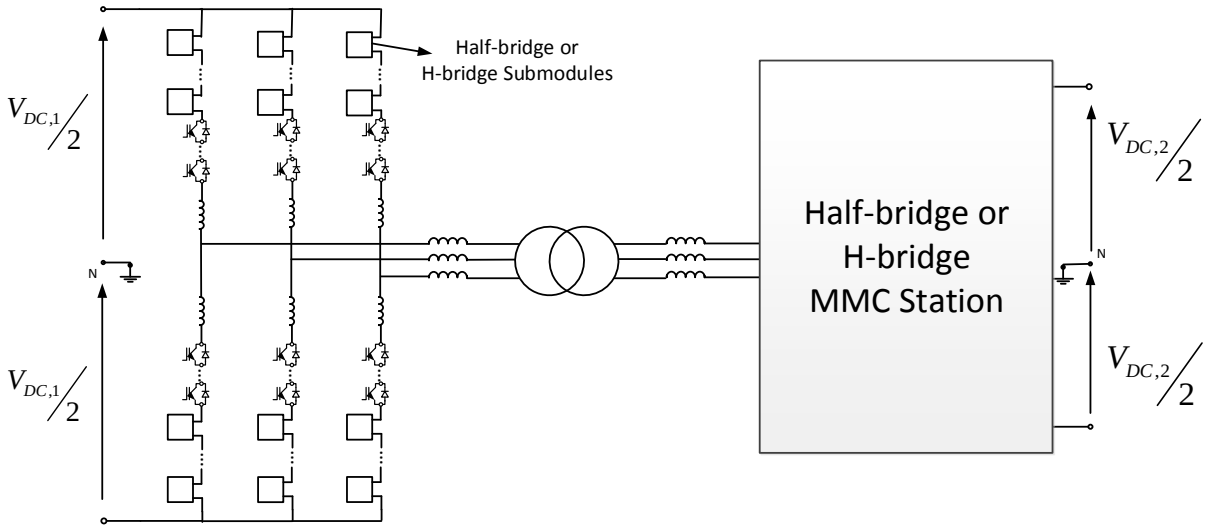


Figure 2.8 DC-DC converter using alternate arm MMC [35].

2.3 DC Hub Design

Several topologies have been proposed in the literature for the realization of the DC Hub. A DC Hub topology based on the IGBT-based DC-DC converter can be seen in Figure 2.9 [13]. As shown in Figure 2.9, this topology comprises LCL filters and mechanical AC breakers. The active and reactive power at each port can be independently controlled by controlling the dq components of the AC current of each converter. With the appropriate design of the LCL filter, the reactive power at each port can be maintained at zero. In this way, the power transfer capability of each port becomes maximal. The operating frequency of the intermediate AC link must be chosen further away from the resonance frequency in order to avoid undesired oscillations. Moreover, the selection of the L,C parameters of the filter is based on the voltage and power of each port. It implies that any HVDC line can be easily connected or disconnected from the common AC link without affecting the operation of the others. Finally, the suggested topology has fault ride-through capability and can be easily expanded to allow the interconnection of multiple ports. Due to the fact that transformers are not used, the footprint and cost of the system are low. On the downside, no galvanic isolation is present and the switching devices utilization is not the best possible.

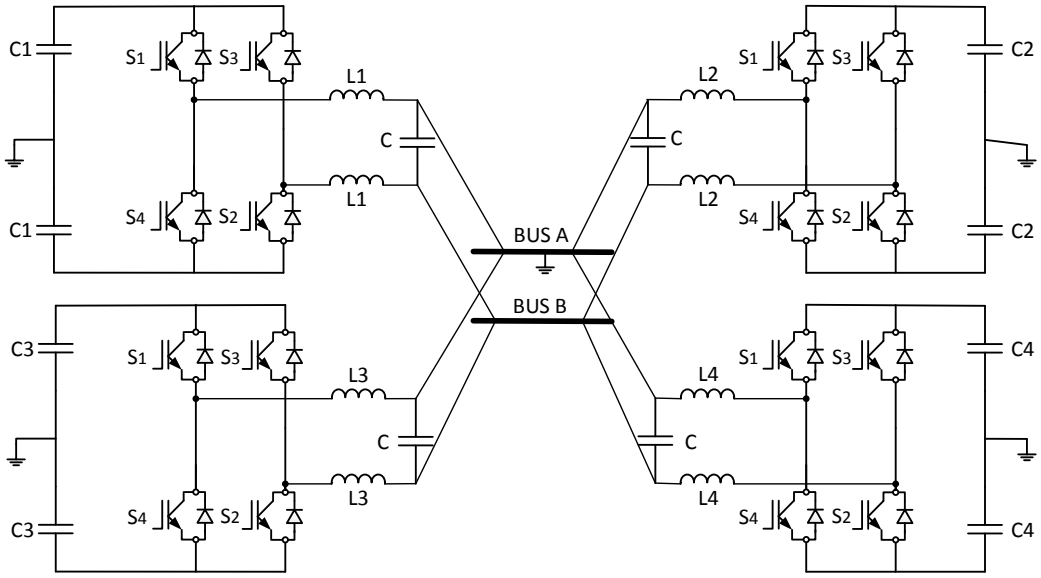


Figure 2.9 Four-port DC Hub using 2-level VSC converters and LCL filters [35].

Another possible DC hub topology is presented in Figure 2.10 [76]. Three hybrid MMC converters are interconnected through a three-winding transformer which is placed in the intermediate AC link. A chain-link of full-bridge submodules is connected on each phase of each half-bridge MMC converter. Therefore, each MMC converter has the ability to ride-through DC faults. Regarding the control structure, one converter should be responsible for the control of the voltage of the intermediate AC link, while the other two converters could operate either in DC voltage or in active power control mode. In case a fault occurs at any of the ports, only the faulted port should be disconnected from the DC hub, while the other ports could continue their operation without interruption. Finally, the design of the three-winding transformer is demanding and increases the footprint of the system, while the modularity is compromised because only one transformer is used. In case a fourth port need to be connected to the DC Hub, a fourth winding should be added to the central transformer, making the design and the expansion of the system complicated.

The most promising DC hub topology is shown in Figure 2.11 [52]. This topology is based on the multiport front-to-front type DC-DC converter. In this four-port DC Hub topology, each HVDC line is connected to the common AC bus through a dedicated MMC converter. Each port may also have a transformer if needed and a mechanical AC circuit breaker. As shown in Figure 2.11, the suggested topology can be used for the interconnection of ports with different DC line configurations. Concerning the control structure, one port should be responsible for the control of the voltage of the common AC bus, while the other ports could operate either in DC voltage or in active power control mode. The reference angle for the rotating dq frame is provided by a global voltage-controlled oscillator. The system is able to ride-through DC faults due to the use of self-blocking submodules at 50% of the converters and half-bridge submodules at the other 50%. However, the semiconductor needs of an MMC using self-blocking submodules are 25% higher compared to an MMC using half-bridge submodules. Finally, the system can be easily expanded to include additional ports. However, as the number of ports increases, the footprint of the system also increases due to the use of additional transformers. As a consequence, the use of this DC hub topology is not recommended for offshore applications.

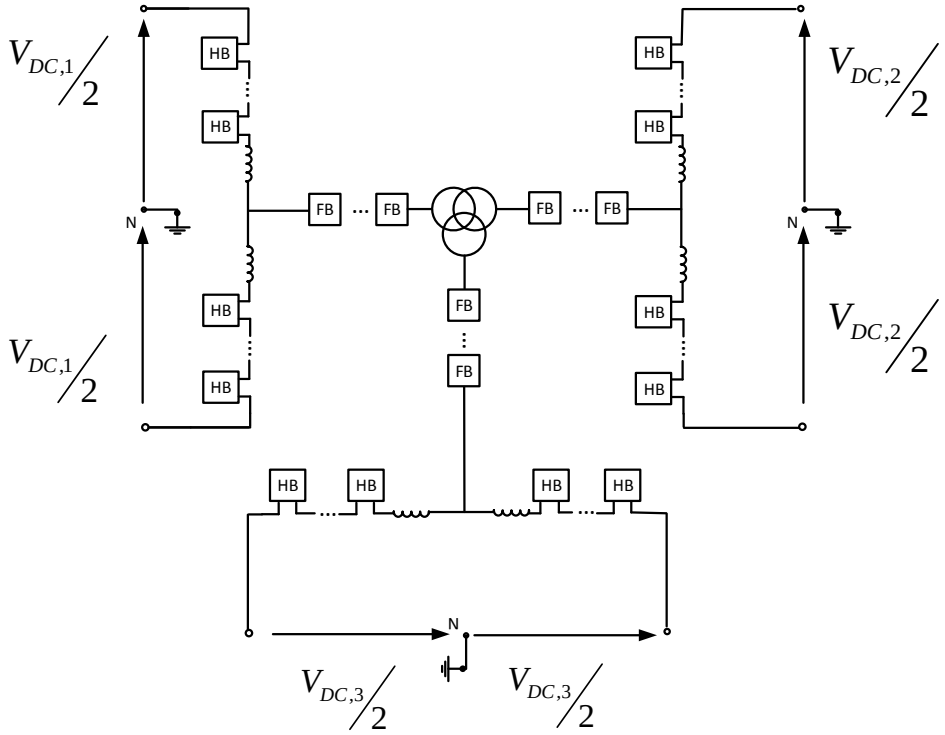


Figure 2.10 Three-port DC Hub using hybrid MMC and three-winding transformer [35].

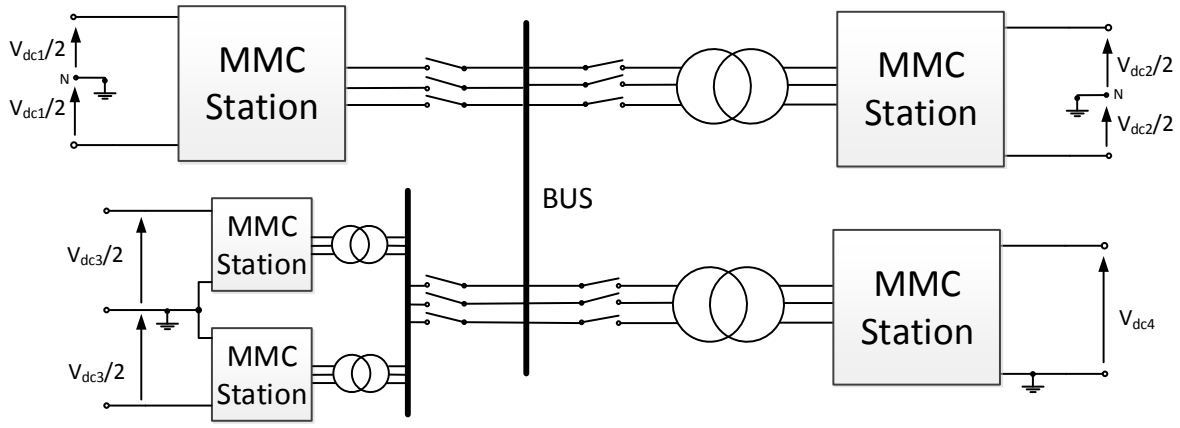


Figure 2.11 Four-port MMC-based DC Hub interconnecting different DC link configurations [35].

3.Introduction to MMC

This chapter starts with the description of the two-level voltage source converters (VSC). Then, the main advantages of the multilevel converters over the two-level converters are analysed. Finally, the mathematical model, the control strategy and the modulation techniques of the MMC converter are described in detail.

3.1 Introduction to Multilevel Converters

Two-level VSC converter

The different topologies of two-level VSC converters only differing in terms of the number of phase legs are shown in Figure 3.1.

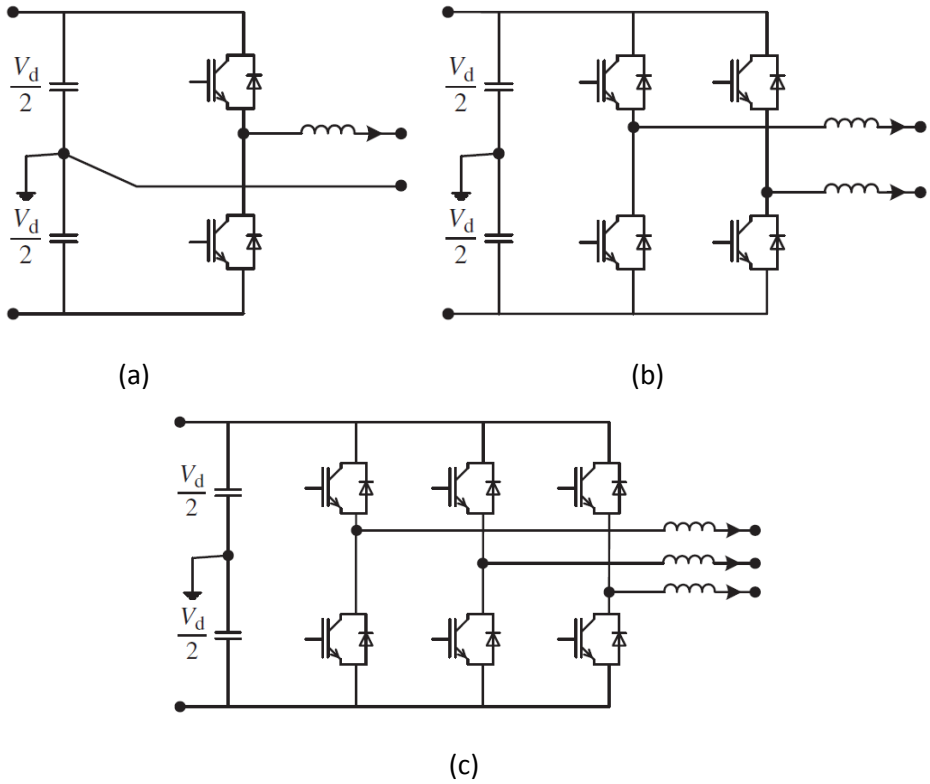


Figure 3.1 Two-level VSC converters with different number of phase legs [1].

As shown in Figure 3.1, all the VSC topologies are equipped with a DC capacitor which maintains the DC voltage of the converter constant. The terminals of this capacitor form the DC terminals of the converter. A number of phase legs are connected in parallel to these terminals. Each phase leg is equipped with two semiconductor valves connected in series. Each semiconductor valve consists of a unidirectional controllable switch (IGBT) and an anti-parallel diode. In this manner, the semiconductor valve is able to conduct current in both directions and block voltage in one direction by controlling the gate signal of the switch. The AC terminals of the converter are formed between the midpoints of the phase legs. An inductance is usually connected in series with the AC terminals of the converter to filter out the AC currents and to keep them fairly constant in the short time interval between the commutation of the phase legs [1].

As can be seen in Figure 3.1, the AC terminal of the converter can be connected to either the positive or the negative DC terminal. When the upper semiconductor switch of the phase leg is conducting, the AC terminal is connected to the positive DC terminal and thus, the output voltage is positive ($+V_d/2$). On the other hand, when the lower semiconductor switch of the phase leg is conducting, the AC terminal is connected to the negative DC terminal and thus, the output voltage is negative ($-V_d/2$). It should be mentioned that the upper and lower semiconductor valves of each phase leg cannot conduct simultaneously, as it would cause a short-circuit across the DC capacitor and it would be detrimental for the converter.

By using the switching sequence described above, the potential at the AC terminal can be switched from one of the DC terminals to the other at any desired instant and thus, the converter can behave as a controllable voltage source. Using appropriate repetitive switching, a desired AC side voltage can be achieved. This methodology is known as *pulse-width modulation* (PWM) [1]. Due to the PWM modulation technique, the AC voltage and thus, the AC current will contain a significant amount of higher-order harmonics. As mentioned before, the inductor which is connected in series with the AC terminal will filter out these harmonic components and will maintain the output current fairly constant in the short time interval between the commutation of the phase legs.

Benefits of Multilevel Converters

The two-level VSC converters have a simple structure with low number of components and are suitable for low power and voltage applications. Thus, they cannot be used in high power and voltage applications because of the following drawbacks [1]:

- The AC side voltage of the VSC converter will contain a significant amount of harmonic components around multiples of the switching frequency. The selection of a high switching frequency could offer a solution to this problem, since only high-order harmonics would appear in the spectrum. In this case, smaller AC filters could be used. However, the selection of a high switching frequency would increase the switching losses. For this reason, the selection of the switching frequency is a trade-off between the harmonic distortion of the output AC voltage (size of the AC filters) and the switching losses (efficiency of the converter).

- The maximum blocking voltage of the available power semiconductors used in VSC converters is a couple of kilovolts. In case a two-level VSC converter must be used in high voltage applications, a high number of power semiconductors should be connected in series. However, there are not available technical solutions to achieve such series connection.

- In two-level VSC converters, the AC phase voltage is always switched between the DC terminals. In order to keep the switching losses to relatively low levels, the switching operation should be very fast. In high voltage applications, the voltage slope will be high and thus, the stress on the insulation of the equipment connected to the AC side will also be high.

A transition to multilevel converters could offer many advantages. At first, multilevel converters have more than one DC link capacitors. Thus, the blocking capability requirements of each semiconductor valve depend on the individual capacitor voltages and not on the full DC link voltage. Thus, the power

rating of the converter can be increased without direct series connection of semiconductor elements. At second, the output AC voltage has more than two levels. Therefore, the harmonic distortion of the AC voltage is lower and the amplitude of the harmonics is significantly reduced. Moreover, the frequency at which the output voltage is changed can be increased without increasing the value of the switching frequency. As a result, the harmonics in the spectrum will appear at higher frequencies where they can be easily filtered out by smaller AC filters [1].

Multilevel Converter Topologies

Some of the most popular multilevel converter topologies are:

- Neutral-Point Clamped (NPC) converter [3]
- Flying Capacitor (FC) converter [3]
- Cascaded H-Bridge (CHB) converter [3]
- Modular Multilevel Converter (MMC)

Modular Multilevel Converter

The topology of the Modular Multilevel Converter (MMC) is shown in Figure 3.2. As can be seen in Figure 3.2, the fundamental building block of the MMC is the submodule. The most commonly used types of submodules are the half-bridge and the full-bridge submodules. The circuit diagram of each type of submodule is presented in Figure 3.3. The half-bridge submodule topology is the most commonly used in bidirectional power flow applications. As shown in Figure 3.3, the half-bridge submodule consists of one two-level phase leg which is connected in parallel with a DC capacitor. The external terminals of the submodule are formed by the phase leg midpoint on the one hand and one of the DC capacitor terminals on the other hand [1].

The series connection of submodules in one phase forms the leg of the converter, as shown in Figure 3.2. Each leg consists of the upper and lower arms, and the number of submodules per arm is the same. The common point connection between the upper and lower arms constitutes the AC terminal of the MMC converter. Given that the total DC voltage is equally divided among the submodule capacitors of each phase leg, there is no need for bulky DC link capacitors. Finally, an inductor is placed in each arm of the phase leg to limit the circulating current and the arm overcurrents in case of fault [3].

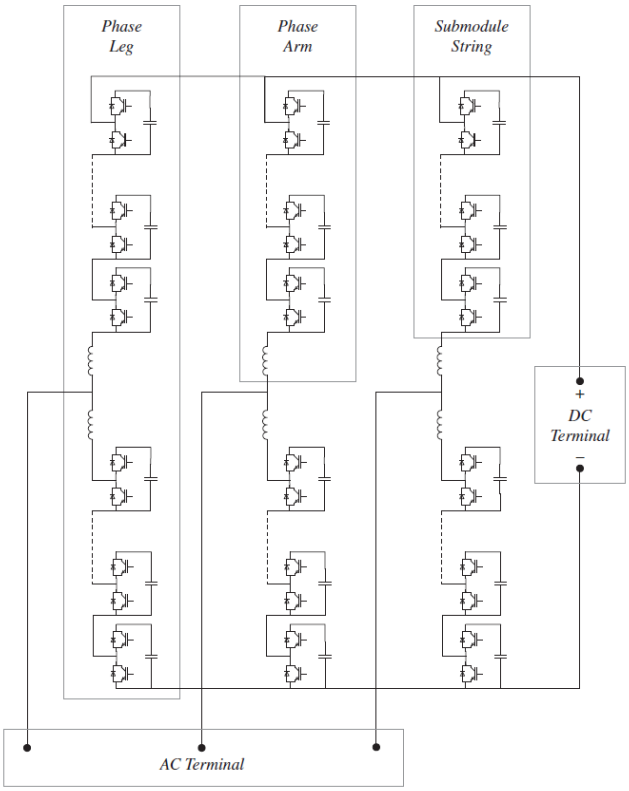
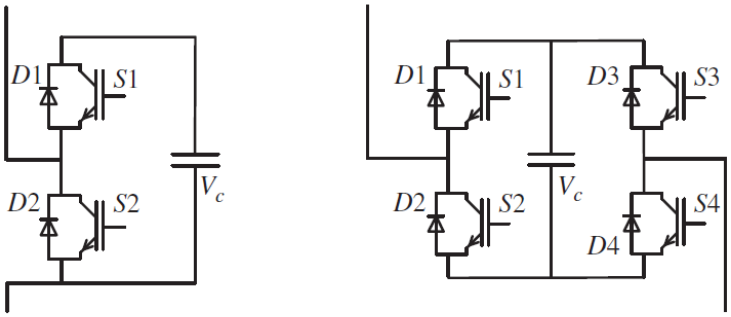


Figure 3.2 Three-phase Modular Multilevel Converter [1].

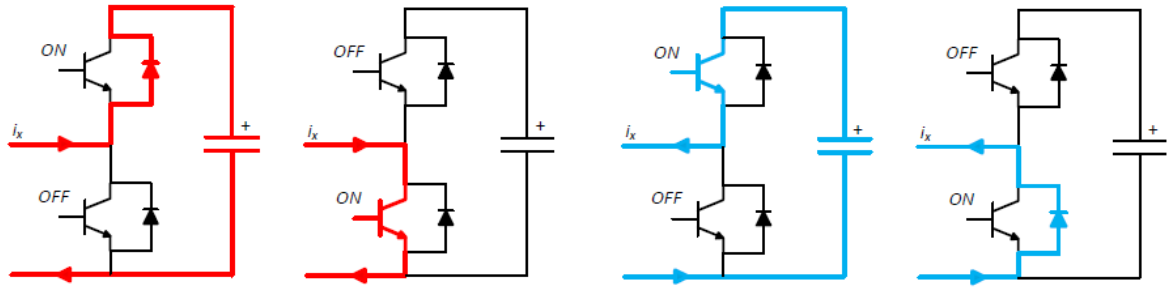


(a) (b)

Figure 3.3 Converter submodules: half bridge (a) and full-bridge (b) [1].

For the purpose of this study, the term submodule refers to the half-bridge topology. The submodule capacitor acts as DC voltage source, the switches are responsible for the insertion of the submodule capacitors into the arm and the anti-parallel diodes ensure uninterruptable flow of the current [3].

Each submodule has two states depending on the conduction state of the switches. As can be seen in Figure 3.3, when switch S1 is ON and switch S2 is OFF, the submodule is inserted into the arm and the voltage across the submodule is equal to the voltage of the inner capacitor. On the other hand, when switch S1 is OFF and switch S2 is ON, the submodule is bypassed and the voltage across the submodule is zero. It should be mentioned that switches S1 and S2 cannot be ON simultaneously, as it would cause a short circuit across the submodule capacitor. The different switching states of a half bridge submodule can be seen in Figure 3.4. By controlling the number of the inserted submodules, a staircase output voltage waveform can be generated at the AC terminals of the converter.



(a) (b) (c) (d)

Figure 3.4 Different switching states of half-bridge submodule [3].

The direction of the arm current affects the state of charge of the submodule capacitors. As can be seen in Figure 3.4, in case the submodule capacitor is inserted into the arm, a positive current will charge the capacitor whereas a negative current will discharge the capacitor. In case the submodule capacitor is by-passed, its voltage will remain constant [3].

The switching states of the submodule are shown in Table 3.1. When both switches S1 and S2 are OFF, the submodule consists of two diodes and a submodule capacitor. In this case, if the arm current is positive, it will flow through the upper diode, charging this way the capacitor. This state of operation can be used for the initial charging of the submodule capacitors [3].

State of S1	State of S2	Submodule terminal voltage	Polarity of arm current	Status of the capacitor
ON	OFF	V_C	+	Charging
OFF	ON	0	+	By-passed
ON	OFF	V_C	-	Discharging
OFF	ON	0	-	By-passed
ON	ON	Capacitor Shorted		
OFF	OFF	Open Circuit		

Table 3.1 Switching states of the submodule [3].

The main advantages of the MMC converter are [3]:

- Modularity. The series connection of multiple submodules in each arm of the converter decreases the power and voltage ratings of the semiconductor devices (diodes, switches) and submodule capacitors. In other words, the converter can be easily scaled to high power and voltage levels.
- Better AC voltage quality. The output voltage has more than two levels. As a result, the harmonic distortion of the output voltage is lower and the amplitude of the harmonics is significantly reduced.
- Redundancy. Redundant submodules can be used in case of submodule failures.
- Higher efficiency. The frequency at which the output voltage is changed can be increased without increasing the switching frequency. Thus, the low switching frequency of each submodule results in increased efficiency of the converter.
- Reduced footprint. Smaller filters can be used, because the harmonic distortion of the output AC voltage is lower. Moreover, there is no need for bulky DC link capacitors.

Due to the aforementioned advantages, the MMC topology is the most commonly used in HVDC applications.

3.2 Mathematical Model of the MMC

The simplified topology of an MMC converter can be seen in Figure 3.2 [2]. Three levels can be observed:

a) The submodules (Level I)
b) The arm (Level II)
c) The phase leg (Level III)

In order to fully understand the operation of the MMC, a continuous model should be derived based on its voltage-current equations. Using the continuous model of the MMC, a method could be developed for the control of the upper and lower arm voltages of the converter [2].

Considering that each arm consists of N submodules, each arm can be controlled by an insertion index $n(t)$. When $n(t) = 1$, all the submodules are inserted into the arm. When $n(t) = 0$, all the submodules are bypassed.

The ideal capacitance of the arm is given by:

$$C^{arm} = \frac{C}{N} \tag{3.1}$$

where C is the submodule capacitance.

The effective capacitance of the arm depends on the insertion index and can be expressed as:

$$C^{m} = \frac{C^{arm}}{n(t)} \tag{3.2}$$

where the index m corresponds to the number of the arm (in a three-phase converter m=1,2,…,6).

The development of the control schemes of the MMC could be based on its full representation, including the operation of each submodule. However, this approach would be complicated. Instead, the continuous model could be used as a base for the development of the control structure of the MMC. A simplified circuit which represents the overall operation of the MMC can be seen in Figure 3.5.

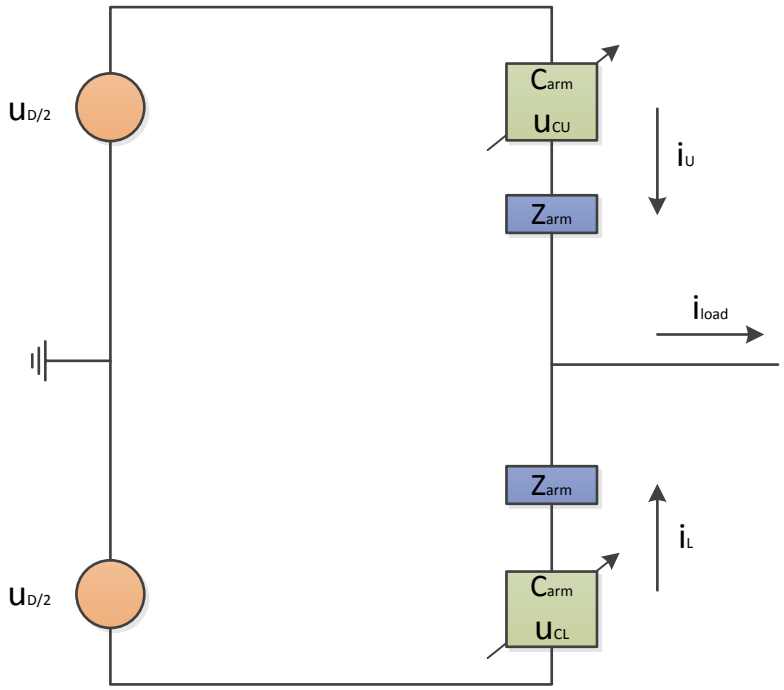


Figure 3.5 Simplified circuit of the MMC converter.

As mentioned before, the index m represents the number of the arm, $n(t)$ is the insertion index and ${u_c}^{\Sigma}(t)$ is the sum of all the submodule capacitor voltages in the m arm.

$$ {u_C}^m = n(t)\, {u_c}^{\Sigma}(t) \tag{3.3} $$

$$ \frac{d{u_C}^{\Sigma}(t)}{dt} = \frac{i(t)}{C^m} \tag{3.4} $$

As shown in Figure 3.5, i_U is the upper arm current and i_L is the lower arm current. The output current i_{load} is equal to the sum of the upper and lower arm currents. The current i_{diff} represents the circulating current that flows between the phase leg and the DC link or between two phase legs. The aforementioned relations can be written as

$$ i_U = \frac{i_{load}}{2} + i_{diff} \tag{3.5} $$

$$ i_L = \frac{i_{load}}{2} - i_{diff} \tag{3.6} $$

$$ i_{load} = i_U + i_L \tag{3.7} $$

$$ i_{diff} = \frac{i_U - i_L}{2} \tag{3.8} $$

In the ideal condition, the contributions of the arm currents i_U and i_L to the output current i_{load} should be equal and the difference current i_{diff} should be zero. In case the equivalent capacitances of the upper and lower arms of a phase leg are not equally charged, the difference current i_{diff} will be different than zero. In this case, the appropriate control of the difference current i_{diff} can lead to equal distribution of the total charge among the submodule capacitors of each phase leg. For the purpose of this analysis, it is assumed that the sum of the submodule capacitor voltages of each arm is equal to the DC link voltage u_D.

Equation (3.4) can now be rewritten as

$$\frac{du_{CU}{}^{\Sigma}(t)}{dt} = \frac{n_U i_U}{C^{arm}} \tag{3.9}$$

$$\frac{du_{CL}{}^{\Sigma}(t)}{dt} = -\frac{n_L i_L}{C^{arm}} \tag{3.10}$$

By applying the Kirchhoff voltage equations in the simplified circuit of the MMC shown in Figure 3.5, the following equations can be derived

$$\frac{u_D}{2} - Ri_U - L\frac{di_U}{dt} - n_U u_{CU}{}^{\Sigma} = u_{load} \tag{3.11}$$

$$-\frac{u_D}{2} - Ri_L - L\frac{di_L}{dt} + n_L u_{CL}{}^{\Sigma} = u_{load} \tag{3.12}$$

The expression for the calculation of the difference current i_{diff} can be re-written as

$$i_U - i_L = 2i_{diff} \tag{3.13}$$

The derivative of Equation (3.13) yields

$$\frac{di_U}{dt} - \frac{di_L}{dt} = 2\frac{di_{diff}}{dt} \tag{3.14}$$

Using Equations (3.11) and (3.12), Equation (3.14) can be re-written as:

$$\frac{di_{diff}}{dt} = \frac{u_D}{2L} - \frac{R}{L}i_{diff} - \frac{n_U}{2L}u_{CU}{}^{\Sigma} - \frac{n_L}{2L}u_{CL}{}^{\Sigma} \tag{3.15}$$

From Equations (3.5)-(3.10), the following dynamic equations for the upper and lower arm voltages can be derived:

$$\frac{du_{CU}{}^{\Sigma}}{dt} = \frac{n_U}{C^{arm}}i_{diff} + \frac{n_U}{2C^{arm}}i_{load} \tag{3.16}$$

$$\frac{du_{CL}{}^{\Sigma}}{dt} = \frac{n_L}{C^{arm}}i_{diff} - \frac{n_L}{2C^{arm}}i_{load} \tag{3.17}$$

As can be seen from Equations (3.16) and (3.17), when the difference current i_{diff} is equal to zero, the load current i_{load} is proportional to the time derivative of the upper and lower arm voltages. In other words, the load current causes the unbalance in the arm voltages. In steady state operation, the output current i_{load}, having sinusoidal waveform, fluctuates between positive and negative values. As a consequence, the time derivative of the upper and lower arm voltages also changes. Ideally, the arm voltage oscillates around a constant average value. However, the operation of the converter is not ideal. Power losses and other factors may lead to instability. As a result, the presence of the difference current is necessary for the safe operation of the converter [2].

Using Equations (3.15), (3.16) and (3.17), a dynamic and continuous model for the MMC converter can be derived:

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ {u_{CU}}^{\Sigma} \\ {u_{CL}}^{\Sigma} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{n_U}{2L} & -\frac{n_L}{2L} \\ \frac{n_U}{C^{arm}} & 0 & 0 \\ \frac{n_L}{C^{arm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{diff} \\ {u_{CU}}^{\Sigma} \\ {u_{CL}}^{\Sigma} \end{bmatrix} + \begin{bmatrix} \frac{u_D}{2} \\ \frac{n_U i_{load}}{2C^{arm}} \\ -\frac{n_L i_{load}}{2C^{arm}} \end{bmatrix} \tag{3.18}$$

Given that the desired output voltage should be sinusoidal, the reference signal for modulation should also be sinusoidal and can be given by

$$m(t) = \hat{m}\cos(\omega_N t) \tag{3.19}$$

The desired output voltage can be given by

$$u_{load}(t) = \frac{u_D}{2}\, m(t) \tag{3.20}$$

Assuming that the load current i_{load} is also sinusoidal, it can be expressed as

$$i_{load}(t) = \hat{\imath}_{load}\cos(\omega_N t + \theta) \tag{3.21}$$

where θ is the phase difference between the output voltage and the output current.

The modulation indices for the upper and lower arms can be written as

$$n_U(t) = \frac{1 - m(t)}{2} \tag{3.22}$$

$$n_L(t) = \frac{1 + m(t)}{2} \tag{3.23}$$

As can be seen from Equations (3.22) and (3.23), the sum of the modulation indices $n_U(t)$ and $n_L(t)$ is always equal to one. It implies that the sum of the upper and lower arm voltages should always be equal to the DC link voltage u_D, assuming that the capacitor voltages of the upper and lower arms are equal to the reference value.

In reality, the capacitor voltages of the upper and lower arms will not be exactly equal to the reference value. There will always be a difference between the DC link voltage and the sum of the

upper and lower arm voltages. Due to this difference voltage, a difference current will circulate between the DC link and the phase leg of the converter. The appropriate control of this difference current is crucial for achieving equal sharing of the DC link voltage among the submodule capacitors of each phase leg of the converter.

In order to create the difference voltage u_{diff}, and thus the difference current i_{diff}, an offset voltage should be added to the upper and lower arm voltages. The addition of the offset voltage does not affect the output voltage of the converter since the output voltage depends on the difference between the upper and lower arm voltages. However, it will affect the difference current i_{diff}.

3.3 Control Strategy of the MMC

From Equations (3.11) and (3.12), the following equations can be derived

$$u_{load} = \frac{u_{CU} - u_{CL}}{2} - \frac{R}{2} i_{load} - \frac{L}{2} \frac{di_{load}}{dt} \tag{3.24}$$

$$L \frac{di_{diff}}{dt} + R i_{diff} = \frac{u_D}{2} - \frac{u_{CL} + u_{CU}}{2} \tag{3.25}$$

From Equations (3.24) and (3.25), the following conclusions can be drawn:

- The output voltage u_{load} depends only on the output current i_{load} and the difference between the upper and lower arm voltages $u_{CU} - u_{CL}$.
- The term $\frac{u_D}{2} - \frac{u_{CL}+u_{CU}}{2}$ acts as an alternating voltage source, R and L as a passive impedance for the alternating current i_{diff}.
- The difference current i_{diff} depends only on the DC link voltage u_D and the sum of the upper and lower arm voltages $u_{CL} + u_{CU}$.

As mentioned in section 3.2, the addition of an offset voltage to the upper and lower arm voltages will not affect the output voltage u_{load}. However, it will influence the difference current i_{diff}.

From Equations (3.5) and (3.11), the following equation can be derived

$$\frac{u_D}{2} - \frac{R}{2} i_{load} - R i_{diff} - \frac{L}{2} \frac{di_{load}}{dt} - L \frac{di_{diff}}{dt} - u_{CU} = u_{load} \tag{3.26}$$

Equation (3.26) can be rewritten as

$$u_{CU} = \frac{u_D}{2} - u_{load} - \frac{R}{2} i_{load} - \frac{L}{2} \frac{di_{load}}{dt} - R i_{diff} - L \frac{di_{diff}}{dt} \tag{3.27}$$

Equation (3.24) can be rewritten as

$$u_{load} + \frac{R}{2} i_{load} + \frac{L}{2} \frac{di_{load}}{dt} = \frac{u_{CL} - u_{CU}}{2} = e_{load} \tag{3.28}$$

Using Equation (3.28), Equation (3.27) can be rewritten as

$$u_{CU} = \frac{u_D}{2} - e_{load} - u_{diff} \tag{3.29}$$

By following exactly the same procedure, u_{CL} can be expressed as

$$u_{CL} = \frac{u_D}{2} + e_{load} - u_{diff} \tag{3.30}$$

where u_{diff} can be given by

$$u_{diff} = Ri_{diff} + L\frac{di_{diff}}{dt} \tag{3.31}$$

The influence of the difference voltage (u_{diff}) on the upper and lower arm voltages (u_{CU} and u_{CL}) can be expressed by Equations (3.29) and (3.30).

The quantity e_{load} is equal to the output voltage u_{load} and is defined as

$$e_{load} = \frac{u_{CL} - u_{CU}}{2} \tag{3.32}$$

In order to derive a suitable control strategy for determining the value of the difference voltage u_{diff}, the energy stored in the equivalent upper and lower arm capacitances should be introduced.

Considering that the energy stored in each arm is equally shared between the submodule capacitors, the energy of the upper and lower arms of each phase leg can be given by

$$W_{CU}{}^{\Sigma} = N\left[\frac{C}{2}\left(\frac{u_{CU}{}^{\Sigma}}{N}\right)^2\right] = \frac{C}{2N}(u_{CU}{}^{\Sigma})^2 = \frac{C^{arm}}{2}(u_{CU}{}^{\Sigma})^2 \tag{3.33}$$

$$W_{CL}{}^{\Sigma} = N\left[\frac{C}{2}\left(\frac{u_{CL}{}^{\Sigma}}{N}\right)^2\right] = \frac{C}{2N}(u_{CL}{}^{\Sigma})^2 = \frac{C^{arm}}{2}(u_{CL}{}^{\Sigma})^2 \tag{3.34}$$

The power is the time derivative of the energy. Therefore, the power of the upper and lower arms can be expressed as

$$\frac{dW_{CU}{}^{\Sigma}}{dt} = i_U u_{CU} = \left(\frac{i_{load}}{2} + i_{diff}\right)\left(\frac{u_D}{2} - e_{load} - u_{diff}\right) \tag{3.35}$$

$$\frac{dW_{CL}{}^{\Sigma}}{dt} = -i_L u_{CL} = \left(-\frac{i_{load}}{2} + i_{diff}\right)\left(\frac{u_D}{2} + e_{load} - u_{diff}\right) \tag{3.36}$$

The total energy stored in a phase leg is

$$W_C{}^{\Sigma} = W_{CU}{}^{\Sigma} + W_{CL}{}^{\Sigma} \tag{3.37}$$

The difference between the energy stored in the upper and lower arms is

$$W_c{}^{\Delta} = W_{CU}{}^{\Sigma} - W_{CL}{}^{\Sigma} \tag{3.38}$$

Differentiating Equations (3.37) and (3.38) and using Equations (3.35) and (3.36), the power of the upper and lower arms can be written as

$$\frac{dW_C{}^{\Sigma}}{dt} = (u_D - 2u_{diff})i_{diff} - e_{load}i_{load} \tag{3.39}$$

$$\frac{dW_C{}^{\Delta}}{dt} = \left(\frac{u_D}{2} - u_{diff}\right) i_{load} - 2e_{load}i_{diff} \tag{3.40}$$

Supposing that the difference current i_{diff} has only a DC component, the quantity $u_D i_{diff}$ represents the power which is delivered to the AC side (load and submodule capacitors). The quantity $u_{diff}i_{diff}$ represents the power losses on the arm resistance R and the variation of the magnetic energy in the arm inductance L. The quantity $e_{load}i_{load}$ represents the power which is delivered to the load. As can be seen from Equation (3.40), the DC component of the difference current i_{diff} does not affect the difference between the energy which is stored in the upper and lower arms of the converter, since the output voltage e_{load} has no DC components. For this reason, the DC component of the difference current i_{diff} can be used for the control of the total energy which is stored in each phase leg of the converter [2]. Moreover, the AC component of the difference current i_{diff}, having the same fundamental frequency with the output current i_{load}, could be used to control the distribution of the capacitor energy between the upper and lower arms of each phase leg. In fact, the quantity $e_{load}\, i_{diff}$ has a DC component which can be used to force the energy difference between the upper and lower arms to change.

3.4 Modulation Techniques

There are two different types of modulation techniques:

- PWM with carrier wave – Level and Phase Shifted
- Nearest Level Control

PWM methods with carrier wave – Level and Phase Shifted

The carrier-based PWM methods are based on the comparison of a reference signal with a high frequency triangular signal (carrier waveform). The carrier waveform can be either bipolar or unipolar. The switching instants are determined by the intersections of the reference signal and the carrier waveform [3].

In case of the MMC, each carrier is assigned to a particular submodule of the phase leg of the converter. This technique allows independent submodule control and modulation.

There are two types of carrier-based modulation methods:

I. The Level Shifted Carrier (LSC)-PWM
II. The Phase Shifted Carrier (PSC)-PWM

In the Level Shifted Carrier (LSC)-PWM method, the amplitude of the carriers is divided with N and an offset is added to each carrier. The number of carrier signals is $N-1$, and all the carriers have the same amplitude and frequency. Several ways of phase shifting the level-shifted carriers with respect to each other have been proposed in the literature.

The most commonly used methods are:

- Phase disposition (PD): carriers have the same phase angle and only differ in terms of a level offset [1].
- Phase opposition disposition (POD): carriers above zero level are π rad phase shifted with respect to those below zero [1].
- Alternative phase opposition disposition (APOD): alternating phase shifts of zero and π rad are used so that adjacent carriers will be in anti-phase [1].

In the Phase Shifted Carrier (PSC)-PWM method, the amplitude of the carriers is identical, while each carrier has a different phase. An advantage of this method is that each submodule is switched with the same frequency. As a consequence, the switching losses are better distributed among the submodules of the converter [4]. This method has $N-1$ carrier signals with the same amplitude and frequency. A staircase multilevel output waveform can be obtained by applying the following phase shift between the carriers:

$$\theta = \frac{360^o}{N-1} \tag{3.41}$$

The waveforms of the carrier signals, the reference signal and the multilevel output signal can be seen in Figure 3.6. As mentioned before, this method provides equal duty and power allocation among the submodule capacitors. Thus, capacitor voltage balancing can be achieved by selecting the appropriate carrier frequency [3]. For this reason, the Phase Shifted Carrier - PWM method is usually preferred over the Level Shifted Carrier – PWM method.

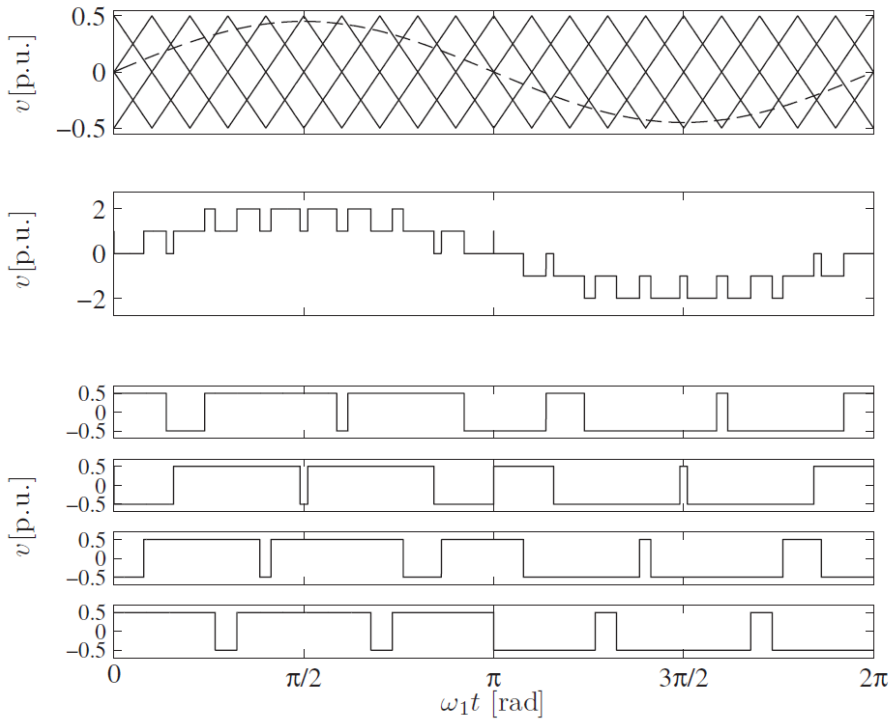


Figure 3.6 Phase Shifted Carrier (PSC)-PWM method. First diagram (upper): carriers and reference waveform, Second diagram: modulated output voltage waveform, Third diagram (lower): two-level modulated waveforms [1].

Nearest Level Control (NLC)

The main idea behind *NLC* is to sample the reference signal at high frequency and to approximate it with the nearest available level. Supposing that the submodule capacitor voltages are constant and equal to $V_C = u_D/N$, the converter arms can produce the following $N + 1$ voltage levels: $0, u_D/N, 2u_D/N, \ldots, u_D$. The number of submodule capacitors which should be inserted and bypassed can be given by the following formulas [3]

$$n_{on,u} = round\left[N\left(\frac{1}{2} - \frac{u_{ref}(t)}{u_D}\right)\right] \tag{3.42}$$

$$n_{off,u} = N - n_{on,u} \tag{3.43}$$

$$n_{on,l} = round\left[N\left(\frac{1}{2} + \frac{u_{ref}(t)}{u_D}\right)\right] \tag{3.44}$$

$$n_{off,l} = N - n_{on,l} \tag{3.45}$$

The function $round(x)$ is defined as [1]

$$round(x) = \begin{cases} floor(x) & x < floor(x) + 0.5 \\ ceil(x) & x \geq floor(x) + 0.5 \end{cases} \tag{3.46}$$

where $floor(x)$ is the largest integer lower than x and $ceil(x)$ is the lowest integer higher than x. As a result, the output voltage waveform becomes a staircase. The insertion and bypassing of submodules generates an output AC voltage which is very close to the reference waveform. This technique is recommended for the control of MMC converters with high number of submodules due to the low switching frequency and the small voltage steps [3]. The waveforms of the output staircase voltage and the reference voltage can be seen in Figure 3.7.

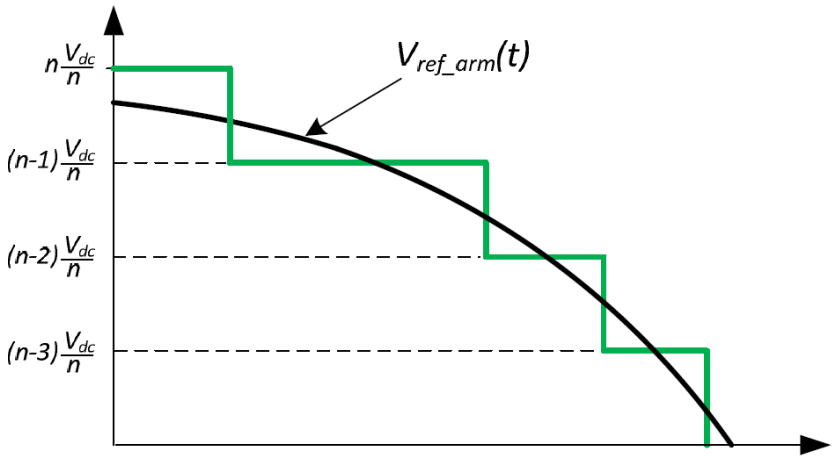


Figure 3.7 Nearest Level Modulation (NLC), output voltage waveform-reference waveform [3].

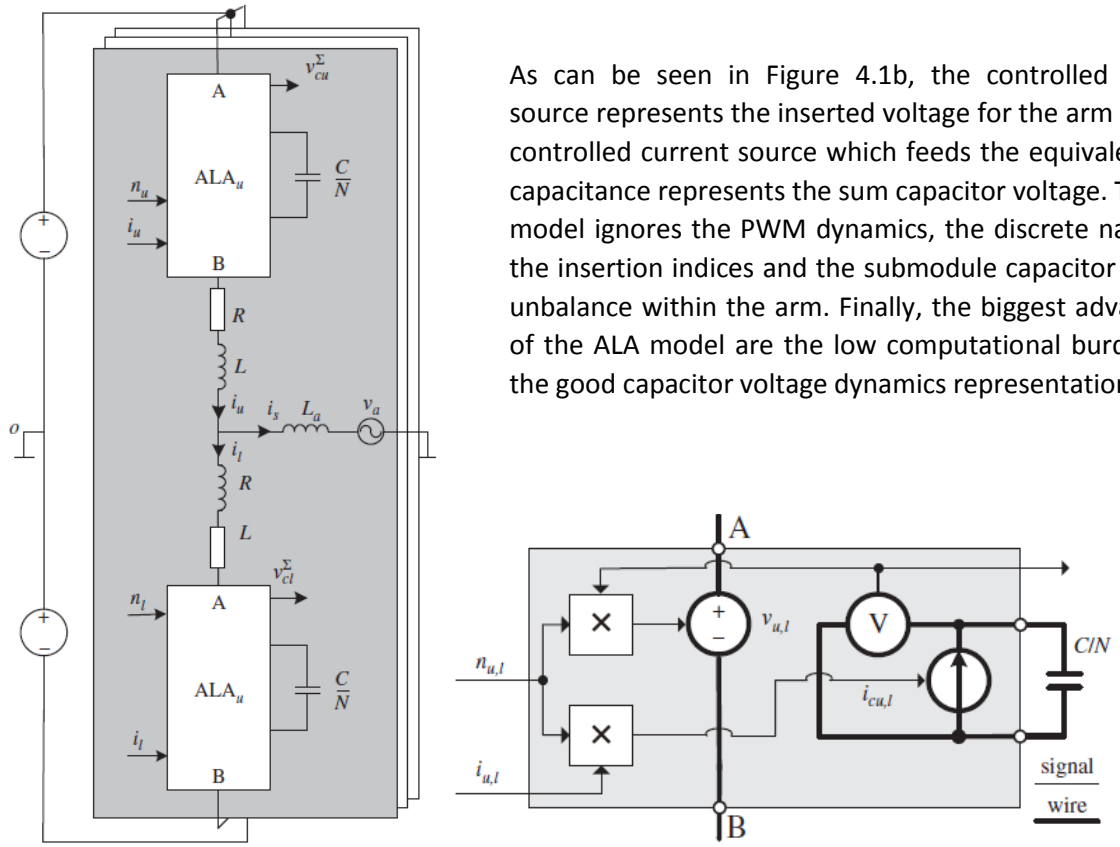
To summarize, the PWM method is a widely used technique to control power electronic converters. In case of the MMC, the most commonly used techniques to control the switching operation of the submodules are the Carrier-less and the Carrier-Based methods. In the Carrier-less methods (NLC), the reference is approximated by the nearest level resulting in a staircase output which determines directly the number of submodules which should be inserted. In the Carrier-Based methods (LSC-PWM, PSC-PWM), a high frequency carrier is assigned to each submodule. In Level-Shifted PWM, an offset is added to each carrier, whereas in Phase-Shifted PWM, the phase of the carriers is shifted [4].

According to [4], when the number of submodules per arm is above 12, the use of the NLC method is recommended due to the lower switching frequency. However, in case the number of submodules per arm is below 12, the Carrier-based methods are preferable because they generate output voltage of better quality.

4.Modeling of the MMC converter

4.1 Averaged model of the MMC

The MMC converters which are used in HVDC applications usually include hundreds of submodules per arm. In case the detailed model of the MMC is used for the modelling of the system, the computational effort will be enormous. For this reason, averaged models of MMCs are used, which provide satisfactory dynamic properties (as the detailed models). In this project, the Arm-Level Averaged (ALA) Model of the MMC converter was used. In this model, each converter arm is represented by an aggregated ideal voltage source averaged over the switching period. The inputs of the ALA model are the insertion indices and the arm currents of the converter. The insertion indices are assumed continuous in the range [0,1]. The equivalent electrical circuit of the converter leg and the ALA arm model can be seen in Figures 4.1a and 4.1b [1].



As can be seen in Figure 4.1b, the controlled voltage source represents the inserted voltage for the arm and the controlled current source which feeds the equivalent arm capacitance represents the sum capacitor voltage. The ALA model ignores the PWM dynamics, the discrete nature of the insertion indices and the submodule capacitor voltage unbalance within the arm. Finally, the biggest advantages of the ALA model are the low computational burden and the good capacitor voltage dynamics representation.

(a) (b)

Figure 4.1 ALA model (a) Electrical circuit (b) ALA arm model [1].

4.2 Calculation of the MMC parameters

The input parameters of the MMC model which was implemented in Simulink are:

- the number of phases (M)
- the DC voltage (V_d)
- the amplitude of the line-to-neutral AC voltage (V_{sMax})
- the rated power of the converter (S_{rated})
- the amplitude of the output current ($I_{sMax} = (2 \cdot S_{rated})/(M \cdot V_{sMax})$)
- the operating frequency (f_{grid})

The MMC parameters which were calculated based on the input parameters are:

- the grid angular frequency (rad/s): $\omega_1 = 2 \cdot \pi \cdot f_{grid}$
- the rated energy storage capability of the converter: $W_{rated} = 30 \cdot 10^{-3}\, J/VA$
- the arm inductance (8% of base impedance-[H]): $L = (0.16 \cdot V_{sMax})/(\omega_1 \cdot I_{sMax})$
- the arm resistance (10% of X-[Ω]): $R = 0.1 \cdot L \cdot \omega_1$
- the submodule capacitance (F): $C = (N \cdot 2 \cdot W_{rated} \cdot S_{rated})/6/V_d{}^2$
- the equivalent arm capacitance for ALA type model (F): $C_{arm} = C/N$
- the average voltage of each submodule (V): $V_{sm} = V_d/N$

4.3 MMC control strategies

In this section, the main control structures of the MMC which were implemented in *Matlab/Simulink* will be presented. As mentioned in Chapter 2, in a three-port DC Hub topology, one MMC should be responsible for controlling the voltage of the intermediate AC link, while the other two MMCs should operate in active power or in DC voltage control mode. The control system of an MMC operating in active power (P_{ac}) or in DC voltage (V_{dc}) control mode can be seen in Figure 4.2, while the control system of an MMC operating in AC voltage (V_{ac}) control mode can be seen in Figure 4.3. The insertion indices n_u and n_l of the MMC are defined as

$$n_u = \frac{V_c^* - V_s^*}{V_{dc}} \tag{4.1}$$

$$n_l = \frac{V_c^* + V_s^*}{V_{dc}} \tag{4.2}$$

where V_s^* is the voltage which drives the output current, V_c^* is the voltage which drives the circulating current and V_{dc} is the voltage on the DC side of the converter.

It is assumed that the insertion indices are continuous in the range [0,1]. Irrespective of the control mode in which the MMC operates, its control can be achieved by controlling the values of the insertions indices. In this manner, the number of submodule capacitors which are inserted into each arm of the converter can be controlled at all times.

In the following, the control structure of the MMC and the tuning process of each individual controller will be described in detail.

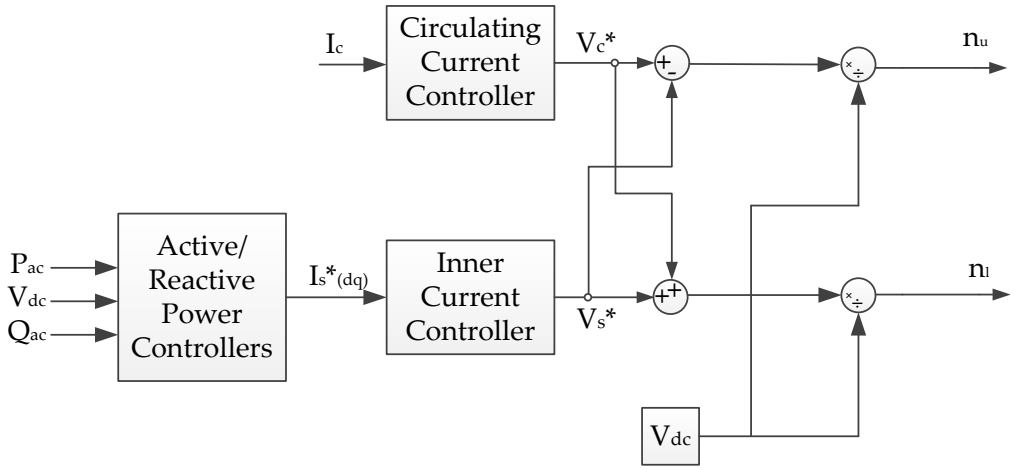


Figure 4.2 Control system of an MMC working in active power or in DC voltage control mode.

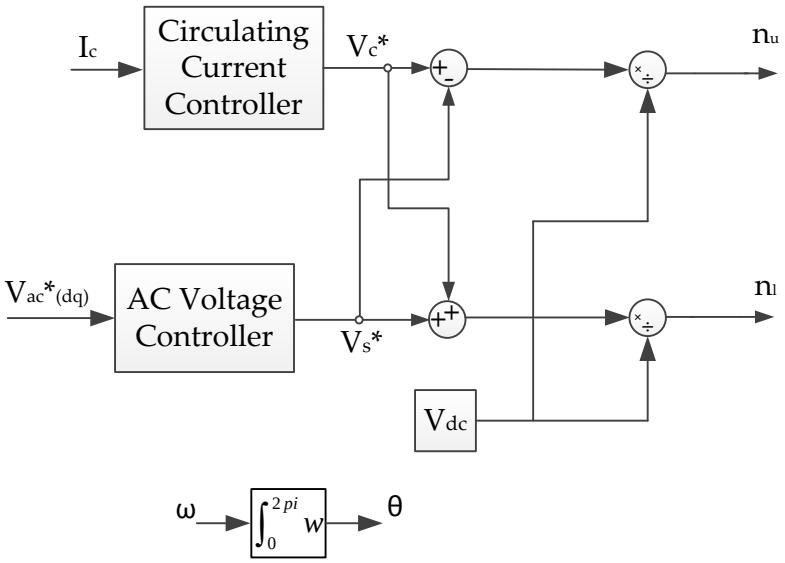


Figure 4.3 Control system of an MMC working in AC voltage control mode.

4.4 Phase Locked Loop (PLL)

PLLs are commonly found in radio-frequency electronic systems where they are used for synchronization purposes. The PLL in a converter control system is also used for performing synchronization. More specifically, the output AC voltage of the MMC is measured and it is transformed into the dq system (Park transformation). Then, the d component of the voltage is controlled at zero. In this way, the rotating vector of the AC voltage of the MMC can be aligned with the q axis. This synchronization makes the control of the active power and DC voltage of the converter simpler as will be explained in the following sections of this chapter. The block diagram of the PLL which was implemented in *Matlab/Simulink* can be seen in Figure 4.4.

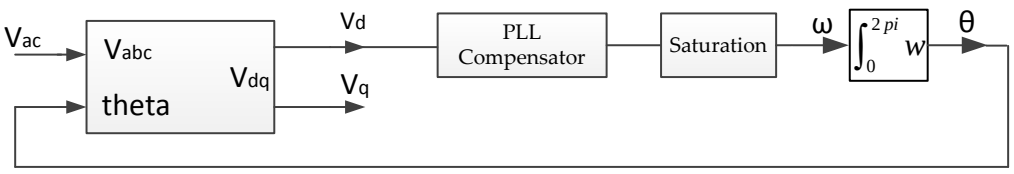


Figure 4.4 Phase Locked Loop (PLL)-Synchronization with the q axis of the AC voltage.

It should be mentioned that the use of a PLL is necessary only in case the MMC converter operates in active power or in DC voltage control mode. In case the MMC works in AC voltage control mode, the value of the rotating angle *theta* of the output AC voltage can be manually set by selecting the desired value of the angular frequency ω, as shown in Figure 4.3.

4.5 Active/Reactive power and DC voltage controllers

In this section, the active/reactive power and DC voltage controllers will be analysed. These controllers receive as input the reference of the active/reactive power or DC voltage of the MMC and give as output the d and q components of the output current. The diagram of this controller can be seen in Figure 4.5.

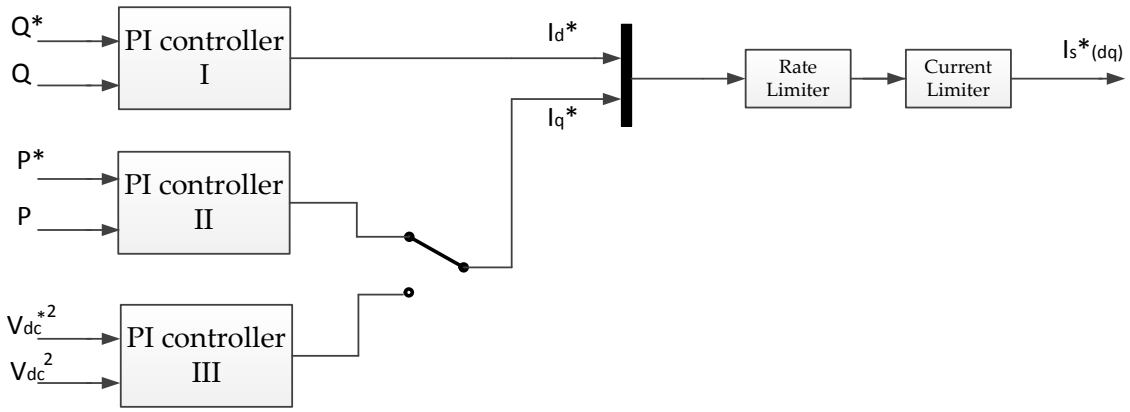


Figure 4.5 Active/reactive power and DC voltage controller.

As described in the previous section, the PLL is responsible for aligning the rotating vector of the AC voltage of the MMC with the q axis of the rotating dq frame. As a consequence, the d component of the AC voltage will be zero (V_d=0). The active and reactive power from a periodic set of three-phase voltages and currents expressed in the $dq0$ reference frame can be expressed as:

$$P = \frac{3}{2}(V_d I_d + V_q I_q) \tag{4.3}$$

$$Q = \frac{3}{2}(V_q I_d - V_d I_q) \tag{4.4}$$

Given that $V_d = 0$, Equations (4.3) and (4.4) can be rewritten as

$$P = \frac{3}{2} V_q I_q \tag{4.5}$$

$$Q = \frac{3}{2} V_q I_d \tag{4.6}$$

Equations (4.5) and (4.6) indicate that the active and reactive power of the MMC converter can be independently controlled by controlling the q and d components of the current. The q and d components of the current need to be saturated before fed to the Inner Current Controller. For this reason, a current limiter is used to keep the current references within the acceptable limits.

As shown in Figure 4.5, the MMC converter could operate either in active power or in DC voltage control mode. If the converter works in active power control mode, the q reference of the current is given by the active power controller (PI controller II). Otherwise, if the converter works in DC voltage control mode, the q reference of the current is given by the DC voltage controller (PI controller III).

The DC voltage controller aims to keep the DC voltage of the converter at a certain level. The controller could be operating on the error of the DC voltage. In this case, the closed-loops dynamics would depend on the operating point, because the DC current (I_{dc}) is inversely proportional to the DC voltage (V_{dc}). To avoid non-linearity problems, the control should be based on the square of the DC voltage (${V_{dc}}^2$).

The equivalent diagram of the active power controller (PI controller II) is shown in Figure 4.6.

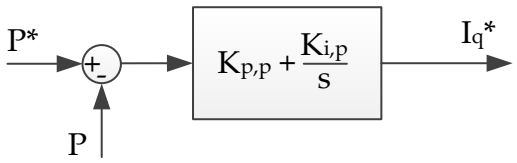


Figure 4.6 Active power controller.

The tuning of the active power controller was performed according to the following formulas:

$$K_{p,p} = \frac{bw \cdot 12 \cdot \pi \cdot f_s \cdot \frac{C_m}{N} \cdot {V_{dc}}^2}{\sqrt{3} \cdot S_b \cdot V_b} \tag{4.7}$$

$$K_{i,p} = \frac{(bw \cdot 2 \cdot \pi \cdot f_s)^2 \cdot 6 \cdot \frac{C_m}{N} \cdot {V_{dc}}^2}{\sqrt{3} \cdot S_b \cdot U_b} \tag{4.8}$$

where b_w is the selected bandwidth (b_w=0.01), f_s is the switching frequency ($f_s = 600\ Hz$), C_m is the submodule capacitance (F), N is the number of submodules per arm, V_{dc} is the voltage on the DC side of the converter, S_b is the power base of the converter and U_b is the AC voltage base of the converter.

The equivalent diagram of the reactive power controller (PI controller I) is shown in Figure 4.7.

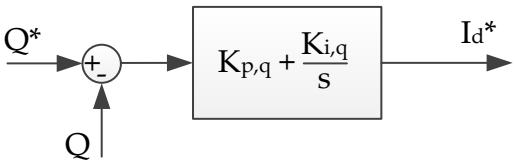


Figure 4.7 Reactive power controller.

The tuning of the reactive power controller was based on the same formulas and the gains are exactly the same as in the previous case.

$$K_{p,q} = K_{p,p} \tag{4.9}$$

$$K_{i,q} = K_{i,p} \tag{4.10}$$

The equivalent diagram of the DC voltage controller (PI Controller III) is shown in Figure 4.8.

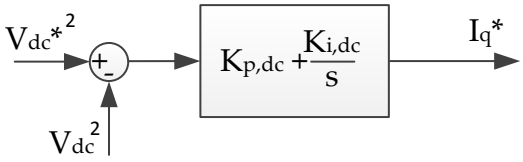


Figure 4.8 DC voltage controller.

The tuning of the DC voltage controller was performed according to the following formulas:

$$K_{p.dc} = \frac{bw \cdot 12 \cdot \pi \cdot f_s \cdot \frac{C_m}{N}}{\sqrt{3} \cdot U_b} \tag{4.11}$$

$$K_{i,dc} = \frac{(bw \cdot 2 \cdot \pi \cdot f_s)^2 \cdot 6 \cdot \frac{C_m}{N}}{\sqrt{3} \cdot U_b} \tag{4.12}$$

where b_w is the selected bandwidth (b_w=0.01), f_s is the switching frequency ($f_s = 600\ Hz$), C_m is the submodule capacitance (F), N is the number of submodules per arm, V_{dc} is the voltage on the DC side of the converter and U_b is the AC voltage base of the converter.

4.6 Inner Current Controller

The AC current that flows from/to the converter through the equivalent phase inductance should also be controlled. The Inner Current Controller (ICC) regulates the current to a reference value, without exceeding the maximum current limitation of the converter. The reference values for the current are provided by the outer controllers and the role of the ICC is to evaluate the voltage drop across the equivalent reactance L_p, which is equal to the sum of the phase reactance (L_{phase}) and the equivalent arm reactance ($0.5 \cdot L_{arm}$), to produce the reference current. The voltage drop across the equivalent reactance L_p can be expressed as

$$V_f - U_c = R_p \cdot I_s + L_p \cdot \frac{d}{dt}(I_s) \tag{4.13}$$

where R_p is the equivalent phase resistance ($R_p = R_{phase} + 0.5 \cdot R_{arm}$), L_p is the equivalent phase reactance ($L_p = L_{phase} + 0.5 \cdot L_{arm}$), V_f is the voltage at the AC filter, at one end of the phase inductor and U_c is the inner converter voltage [50].

Equation (4.13) can be expressed in the dq-frame (Park transformation) as

$$V_{fd} - U_{cd} = R_p \cdot I_{sd} + L_p \cdot \frac{d}{dt}(I_{sd}) - \omega \cdot L_p \cdot I_{sq} \tag{4.14}$$

$$V_{fq} - U_{cq} = R_p \cdot I_{sq} + L_p \cdot \frac{d}{dt}(I_{sq}) + \omega \cdot L_p \cdot I_{sd} \tag{4.15}$$

The control diagram of the ICC which was implemented in *Matlab/Simulink* is presented in Figure 4.9. The output of the ICC is the AC voltage V_s^*, which is used for the calculation of the insertion indices n_u and n_l, as shown in Figure 4.2.

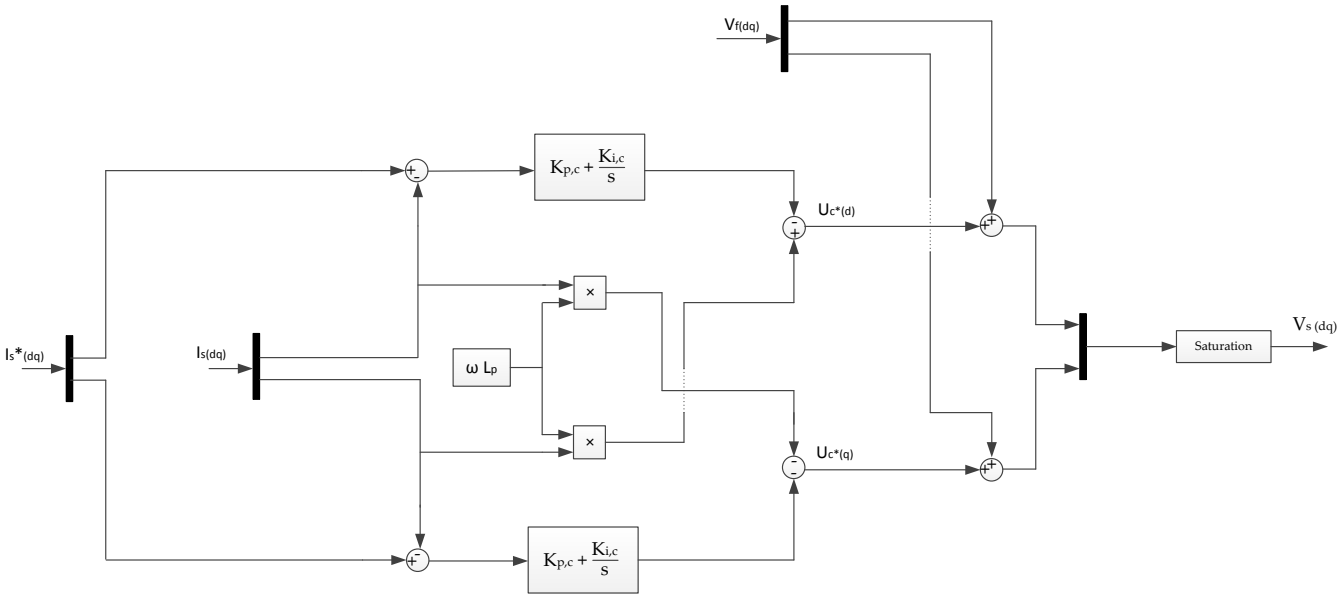


Figure 4.9 Inner Current Controller.

The tuning of the inner current controller was performed according to the following formulas

$$K_{p,c} = bw \cdot 2 \cdot \pi \cdot f_s \cdot \left(L_{phase} + 0.5 \cdot L_{arm}\right) \tag{4.16}$$

$$K_{i,c} = bw \cdot 2 \cdot \pi \cdot f_s \cdot \left(R_{phase} + 0.5 \cdot R_{arm}\right) \tag{4.17}$$

where bw is the selected bandwidth ($bw = 0.1$) and f_s is the switching frequency ($f_s = 600\ Hz$).

4.7 Circulating current controller

In this section, the operation of the circulating current controller will be described. The circulating current is the vehicle for transferring energy in and out of the converter arms and it is critical for the efficient and reliable operation of the MMC. The circulating current need to be suppressed in order to decrease the conduction losses of the power devices. On the other hand, it is the only mean to maintain the voltages of the submodule capacitors balanced. The control diagram of the circulating

current controller which was implemented in *Matlab/Simulink* can be seen in Figure 4.10. As mentioned in Chapter 3, the circulating current can be expressed as

$$I_c = \frac{i_U + i_L}{2}$$

As shown in Figure 4.10, the circulating current is filtered by a Butterworth second order Low Pass Filter (LPF). The transfer function of the filter can be written as

$$H_1(s) = \frac{alpha^2}{s^2 + \sqrt{2} \cdot alpha \cdot s + alpha^2} \tag{4.18}$$

and it is implemented using a second-order generalized integrator (SOGI) with transfer function

$$H_2(s) = \frac{k \cdot \omega^2 \cdot s}{s^2 + \cdot k \cdot \omega \cdot s + \omega^2} \tag{4.19}$$

where $k = \sqrt{2}$ and $\omega = alpha$=80 [rad/s].

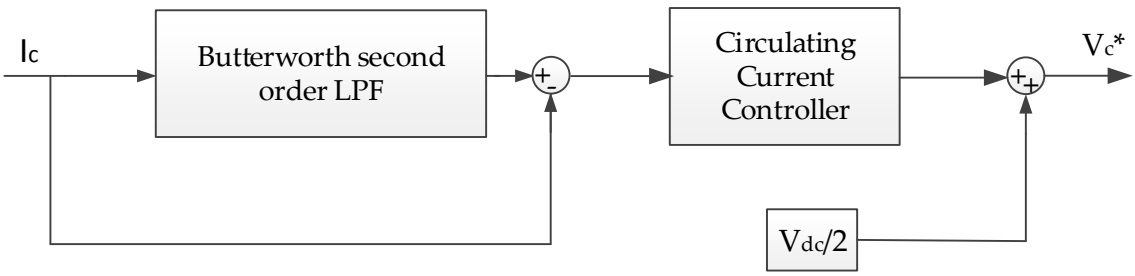


Figure 4.10 Circulating Current Controller.

The actual value of the circulating current is then subtracted from the filtered value, giving as output the AC components of the circulating current. Then, the AC components of the circulating current are led to the circulating current controller. Finally, the difference voltage V_c^* is given by the sum of the output of the circulating current controller and the half of the DC voltage of the converter ($V_{dc}/2$). The detailed diagrams of the Butterworth second order LPF and the circulating current controller are shown in *Appendix A.*

4.8 AC Voltage controller

The control diagram of the AC voltage controller which was implemented in *Matlab/Simulink* can be seen in Figure 4.11. As explained previously, the use of a PLL is not necessary in this case. The value of the angle *theta* of the AC voltage can be manually set by selecting the desired value of the angular frequency ω. As shown in Figure 4.11, the reference of the d component of the AC voltage V_d^* is set at zero. In this way, the rotating vector of the AC voltage can be aligned with the q axis. Therefore, the amplitude of the AC voltage can be controlled by controlling its q component. Using this control method, the output current of the MMC converter cannot be controlled, since the outputs of the PI controllers correspond to the dq components of the voltage reference V_s^*, as shown in Figure 4.11.

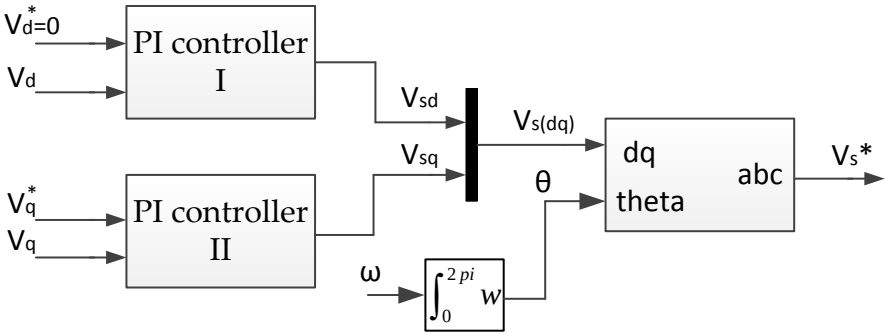


Figure 4.11 AC Voltage Controller.

The equivalent diagram of each individual PI controller is presented in Figure 4.12.

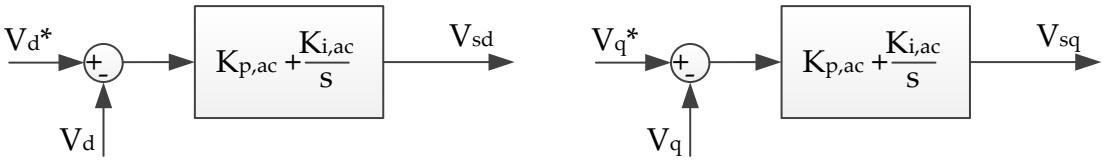


Figure 4.12 PI controllers of AC voltage controller.

The tuning of the AC voltage controller was performed according to the following formulas:

$$K_{p,ac} = \frac{bw \cdot 12 \cdot \pi \cdot f_s \cdot \frac{C_m}{N} \cdot {V_{dc}}^2}{\sqrt{3} \cdot {U_b}^2} \tag{4.20}$$

$$K_{i,ac} = \frac{(bw \cdot 2 \cdot \pi \cdot f_s)^2 \cdot 6 \cdot \frac{C_m}{N} \cdot {V_{dc}}^2}{\sqrt{3} \cdot {U_b}^2} \tag{4.21}$$

where b_w is the selected bandwidth (b_w=0.01), f_s is the switching frequency ($f_s = 600\,Hz$), C_m is the submodule capacitance (F), N is the number of submodules per arm, V_{dc} is the voltage on the DC side of the converter and U_b is the AC voltage base of the converter.

5.Case Study 1:Design of the inner AC circuit of the DC Hub

In this chapter, the different possible designs for the inner AC circuit of the DC hub will be presented. Multiple HVDC lines could be interconnected using transformers, LCL filters or directly. In this chapter, the advantages and disadvantages of each recommended topology will be analytically described.

5.1 Interconnection of HVDC lines using transformers

The DC hub topology with transformers which is used for the interconnection of three HVDC lines operating at different voltage levels is presented in Figure 5.1. As shown in Figure 5.1, the port which works in AC voltage control mode is directly connected to the AC bus. The other two ports (operating in active power or in DC voltage control mode) are connected to the common AC bus through transformers. In case the DC voltage levels of the ports are different, the use of transformers is recommended. Using transformers, the output voltage of each MMC is close to its rated value. Assuming that the power transfer through the converter is constant, the higher the output voltage of the converter, the lower the output current will be. Given that the voltage level of each MMC is the highest possible, the output current and thus, the losses of each converter will be the lowest possible. In other words, the use of transformers increases the efficiency of each MMC and thus, the overall efficiency of the system. As will be described in the following sections of this chapter, in case DC lines with much different voltage levels are interconnected without using transformers, some ports will be underutilized and the operation of the DC hub will not be efficient.

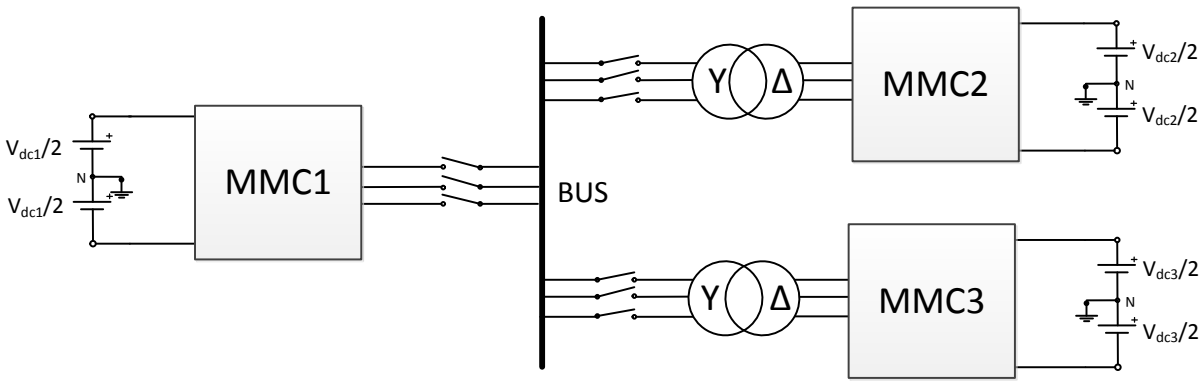


Figure 5.1 Three-port DC hub using transformers.

The use of transformers offers many other advantages. At first, it offers galvanic isolation and leads to reduction of the size of the passive elements such as cell capacitances and arm reactors [8,26]. Furthermore, the use of transformers offers better switching utilization and minimises the circulating reactive power in the AC link (especially in case the DC voltage levels of the interconnected lines are much different) [21, 31]. On the downside, the use of transformers increases the overall investment cost and volume of the system. It is noteworthy that the volume of the transformer can be decreased by increasing the operating frequency.

Regarding the transformer connection, most VSC-HVDC schemes adopt a star/delta winding group [1]. In case of fault at the primary of the transformer (AC bus side), the delta connection of the secondary of the transformer blocks the zero-sequence component of the current. As a result, the zero-sequence current does not flow from the AC network into the converter. For this reason, only the positive-sequence and negative-sequence components of the current need to be controlled, and thus, the control of the converter under fault conditions becomes simpler. Finally, the stray inductance of the transformer serves as an integrated filter element and as a current limiting reactor.

To evaluate the operation of the three-port DC Hub shown in Figure 5.1, the three-port converter was simulated in *Matlab/Simulink*. All the DC links use symmetric monopolar configuration as it is the most commonly used in HVDC connections [77]. For this case study, ideal voltage sources grounded at a mid-point were used on the DC sides. The complete Simulink model which was used for this case study can be seen in *Appendix A*.

The network parameters and the specifications of the MMC converters are presented in Table 5.1

Network parameters	**Unit**	**Value**
Rated power ($S_{b1}/S_{b2}/S_{b3}$)	GVA	1.2/0.6/0.6
DC voltage ($V_{dc1}/V_{dc2}/V_{dc3}$)	kV	600/500/120
Transformer voltage ratio (port 2)	kV	250/300 (Δ/Y)
Transformer voltage ratio (port 3)	kV	60/300 (Δ/Y)
Transformer rated power (port 2)	GVA	0.6
Transformer rated power (port 3)	GVA	0.6
Transformer leakage inductance (port 2)	pu	0.1
Transformer leakage inductance (port 3)	pu	0.1
MMC 1 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	0.4
Arm inductance (L)	mH	57.3
Arm resistance (R)	Ohm	1.8
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20
MMC 2 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	0.288
Arm inductance (L)	mH	79.6
Arm resistance (R)	Ohm	2.5
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20
MMC 3 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	5
Arm inductance (L)	mH	4.6
Arm resistance (R)	Ohm	0.144
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20

Table 5.1 Interconnection using transformers. Network parameters and MMC specifications.

In a three-port DC hub topology, one port should be assigned to the control the voltage of the intermediate AC link and the other two ports could operate either in active power or in DC voltage control mode. Even when a port operates in DC voltage control mode, its active power is controlled

by the other MMC converter of the point-to-point HVDC connection. As a result, in a three-port DC hub topology, the active power of the port controlling the voltage of the AC link will be determined by the sum of the active power of the other two ports. For this reason, the port with the highest power rating should be responsible for the control of the AC voltage, since its active power is equal to the sum of the active power of the other two ports. It was also shown through simulations (which are not presented) that the higher the DC voltage of the port controlling the voltage of the AC link, the more stable the operation of the DC hub will be. More specifically, steps were performed on the active power references of the other two ports, and it was shown that the higher the DC voltage of the port controlling the AC voltage, the more stable the voltage of the AC link will be. Thus, the port controlling the voltage of the AC link should have the highest power rating and, if possible, the highest DC link voltage.

For this reason, port 1, having the highest power rating and DC link voltage, should be responsible for the control of the common bus AC voltage and frequency. Ports 2 and 3 could operate either in active power or in DC voltage control mode. In this case study, both ports 2 and 3 operate in active power control mode. The control structures of the AC voltage, active/reactive power and DC voltage controllers were presented in Chapter 4.

To evaluate the steady state operation and the power flow control performance of the investigated DC hub topology, the AC voltage was controlled at 0.95pu. The modulation index of an MMC is defined as

$$m_f = \frac{V_{phase\_peak}}{V_{dc}/2} \tag{5.1}$$

where V_{phase_peak} is the amplitude of the output phase-to-ground voltage and V_{dc} is the voltage on the DC side of the converter. Therefore, the modulation index (m_f) was set at 0.95. The active power references of ports 2 and 3 were set at 1pu.

In the following part of this section, the steady state operation of the suggested three-port DC hub topology will be investigated. All the quantities will be expressed in pu. The bases that were used for the conversion into the pu system are given in Table 5.2.

Base	Value
AC voltage of MMC 1 (V_{b1})	$V_{b1} = \frac{V_{dc1}}{2} = 300\ kV$
Power bases ($S_{b1}/S_{b2}/S_{b3}$)	$S_{b1}/S_{b2}/S_{b3}$ =1.2/0.6/0.6 GVA
AC current of MMC 1 (I_{b1})	$I_{b1} = \frac{2 \cdot S_{b1}}{3 \cdot V_{b1}} = 2.667\ kA$
DC current of MMC 1 (I_{b_dc1})	$I_{b\_dc1} = \frac{S_{b1}}{V_{dc1}} = 2kA$
Arm current of MMC 1 (I_{b_arm1})	$I_{b\_arm1}=\frac{I_{b1}}{2}+\frac{I_{b\_dc1}}{3}=2\ kA$
Arm voltage of MMC 1 (V_{b_arm1})	$V_{b\_arm1} = V_{dc1} = 600\ kV$

Table 5.2 Power, voltage and current bases of MMC 1.

As can be seen in Figure 5.2, the MMC 1 converter maintains the AC link voltage at 0.95 pu (since m_f=0.95) at all times. The operating frequency is controlled at 50 Hz and the waveform of the voltage is close to sinusoidal, as shown in Figure 5.3. As shown in Figure 5.4, the active power of ports 2 and 3 is controlled at 1pu and the active power of port 1 is maintained at -1pu. Thus, ports 2 and 3 transfer their maximum power to port 1 (P_1=P_2+P_3). For this reason, the sign of the active power of

ports 2 and 3 is positive and the sign of the active power of port 1 is negative. The rated power of ports 2 and 3 is 0.6 GVA and the rated power of port 1 is 1.2 GVA. For this reason, the absolute value of the active power at each port is 1pu.

As can be seen in Figure 5.5, the reactive power at each port is maintained at zero at all times. The apparent power S can be expressed as $S = \sqrt{P^2 + Q^2}$. When $Q = 0$, the apparent power is equal to the active power ($S = P$). Therefore, when the reactive power at a port is controlled at zero, the port has maximum power transfer capability. As a result, when the reactive power at each port of the DC hub is controlled at zero, the power transfer capability of the DC hub is the highest possible.

As shown in Figure 5.6, when the AC voltage and active power at each port are maximum, the AC current of MMC 1 can be maintained within the acceptable limits ($\leq 1.1pu$). As shown in Figure 5.7, the arm current of MMC 1 can also be kept within the specified limits ($\leq 1.1pu$). The arm current can be expressed as $I_{arm} = \frac{I_{dc}}{3} + \frac{I_{ac}}{2}$, where I_{dc} is the DC current and I_{ac} is the AC current of the MMC. The DC and AC components of the arm current can also be observed in Figure 5.7.

As shown in Figure 5.8, the voltage across the upper arm of phase A of MMC 1 fluctuates between 0 and 1pu. According to the theory presented in Chapter 3, the voltage across the arm is zero when all the submodule capacitors are bypassed and the voltage is equal to 1pu when all the submodule capacitors are inserted into the arm. The sum of the submodule capacitor voltages of the upper arm of phase A of MMC 1 is presented in Figure 5.9. The sum of the capacitor voltages should ideally be maintained at 1pu. However, the submodule capacitors are not ideal voltage sources and their voltage levels could variate depending on the state of charge. For this reason, there is a small fluctuation which is kept within the acceptable limits (0.9-1.1 pu). Finally, the insertion indices of phase A of MMC 1, which indicate the number of submodules being inserted into each arm at any moment, are presented in Figure 5.10.

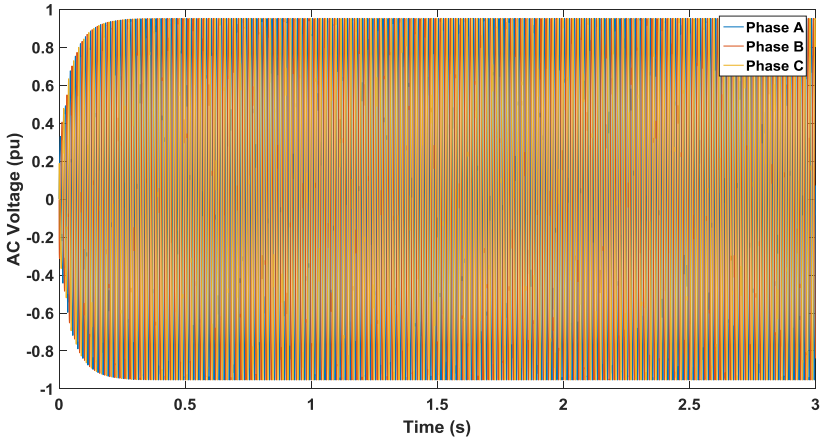


Figure 5.2 Steady state operation of the three-port DC hub using transformers. AC voltage at MMC 1 station.

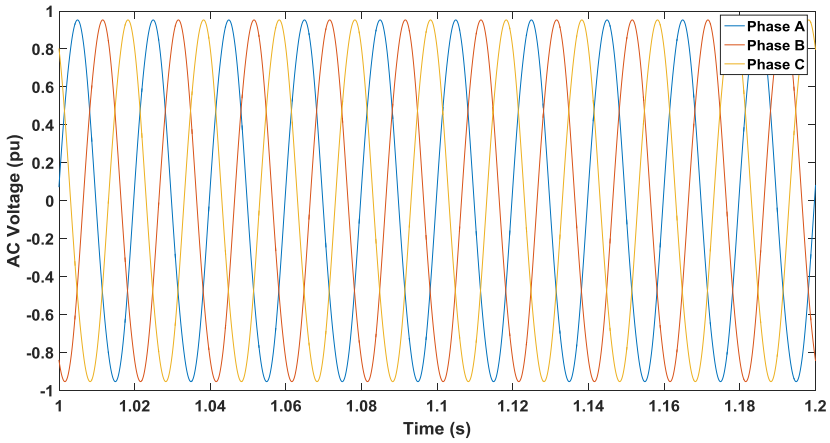


Figure 5.3 Steady state operation of the three-port DC hub using transformers. Zoomed view of AC voltage waveform at MMC 1 station.

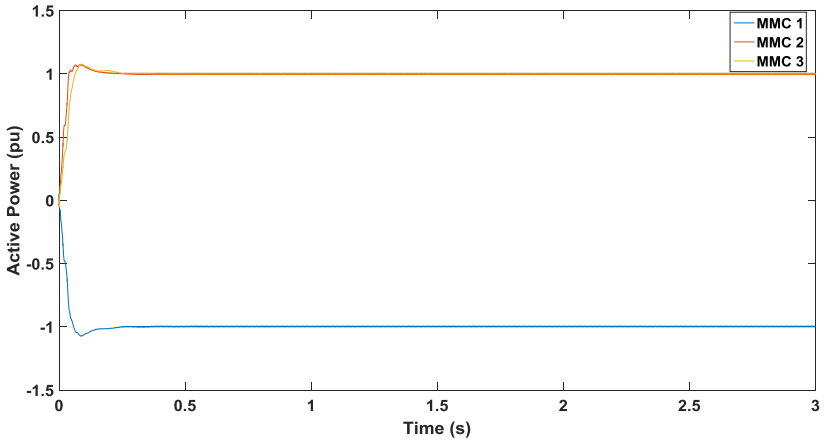


Figure 5.4 Steady state operation of the three-port DC hub using transformers. Active Power at the three ports.

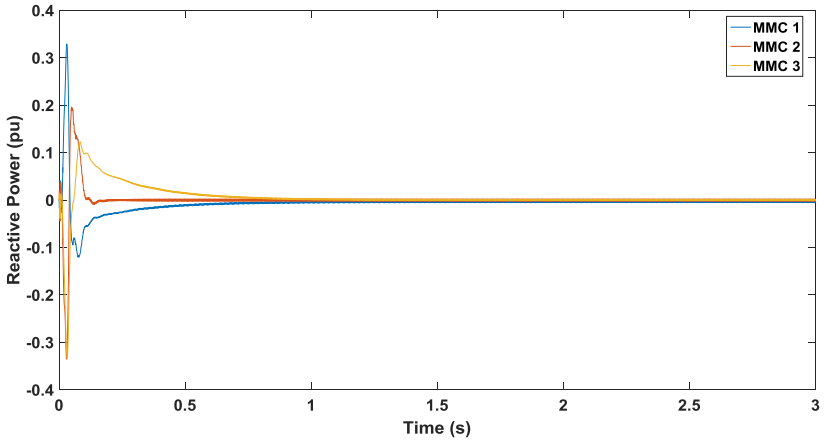


Figure 5.5 Steady state operation of the three-port DC hub using transformers. Reactive power at the three ports.

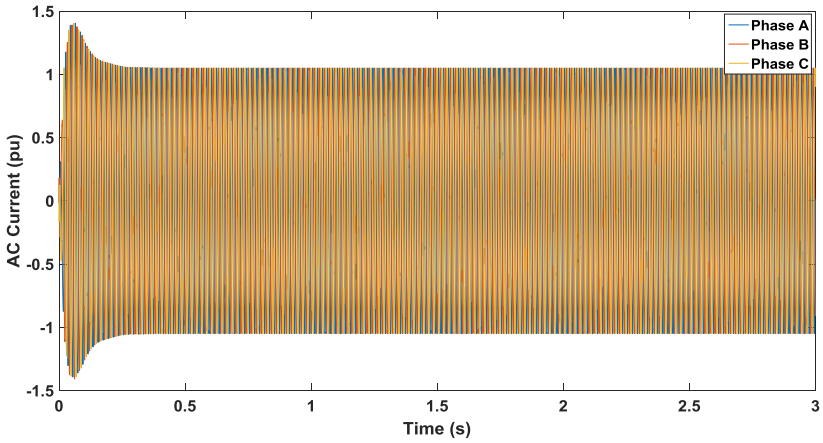


Figure 5.6 Steady state operation of the three-port DC hub using transformers. AC current at MMC 1 station.

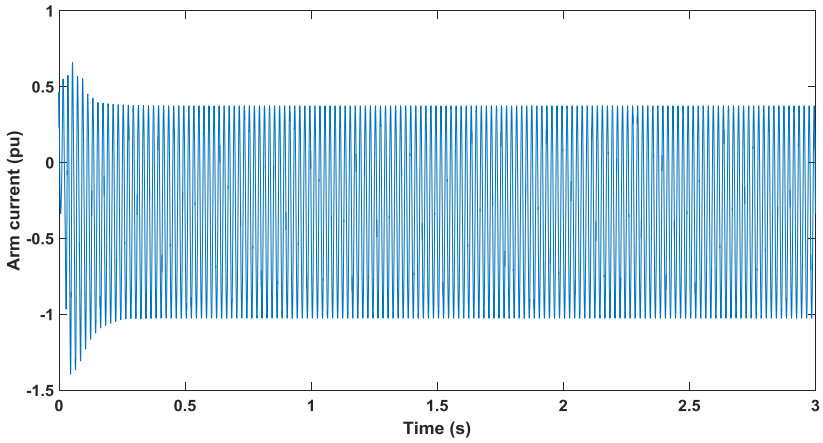


Figure 5.7 Steady state operation of the three-port DC hub using transformers. Upper arm current of phase A of MMC 1 station.

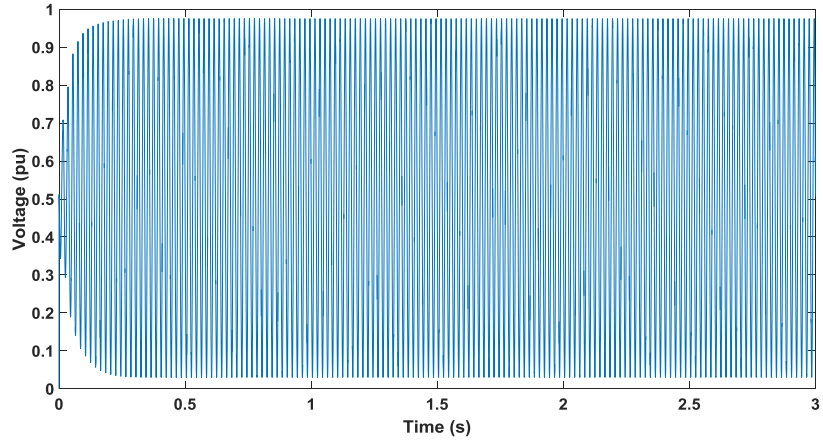


Figure 5.8 Steady state operation of the three-port DC hub using transformers. Voltage across the upper arm of phase A of MMC 1 station.

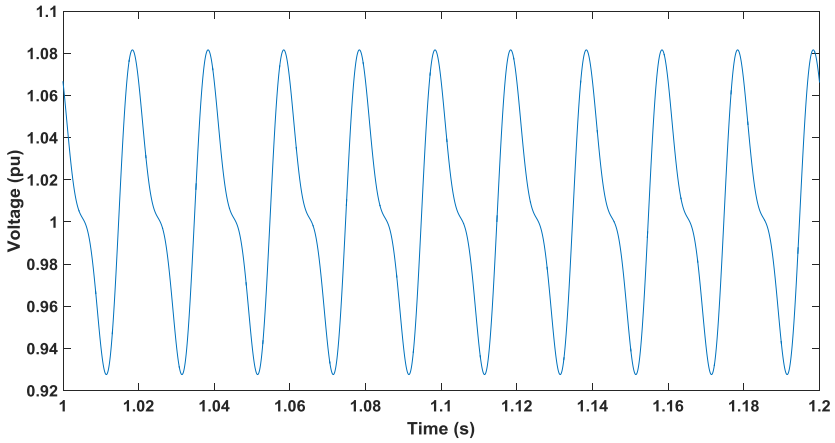


Figure 5.9 Steady state operation of the three-port DC hub using transformers. Zoomed view of the sum of the capacitor voltages of the upper arm of phase A of MMC 1 station.

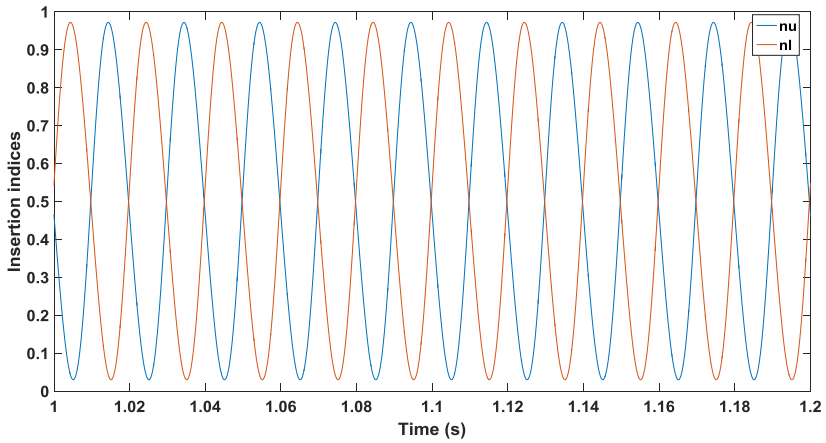


Figure 5.10 Steady state operation of the three-port DC hub using transformers. Zoomed view of the insertion indices n_u and n_l of phase A of MMC 1 station.

To evaluate the power flow control performance of the investigated DC hub, the AC voltage was again controlled at 0.95 pu and steps were performed on the active power references of MMCs 2 and 3. The sequence of the events is presented in Table 5.3.

Time (s)	**0**	**1**	**2**
MMC 2 $p_{ac}{}^{*}$ (pu)	1	-1	0.5
Time (s)	**0**	**1.5**	**2.5**
MMC 3 $p_{ac}{}^{*}$ (pu)	1	0.6	0.2

Table 5.3 Power flow control performance. Case study timeline.

The active power control is fast and the references are followed with a rise time of 60 ms, as shown in Figure 5.12. Independent of the power flow direction, the DC hub control operation is stable and Figure 5.13 shows that the reactive power at each port is maintained at zero at all times. Furthermore, as shown in Figure 5.11, MMC 1 maintains the AC link voltage at 0.95 pu. As can be seen from Table 5.3 and Figure 5.11, the larger the active power step, the larger the distortion of the AC link voltage will be. As shown in Figure 5.11, the distortion of the AC link voltage is higher at t=1s and t=2s. At t=1s, the active power of port 2 changes from 1 pu to -1 pu, causing a voltage drop. At t=2s, the active power of port 2 changes from -1 pu to 0.5 pu, causing a voltage increase. On the

other hand, at t=1.5s and t=2.5s, the steps which are performed on the active power of port 3 are smaller and the power flow direction remains the same. As a result, the distortion of the AC link voltage is lower, as shown in Figure 5.11. Finally, it was shown through simulations (which are not presented) that steps on the active power of the port with the highest DC link voltage (port 2) result in larger distortion of the voltage of the AC link.

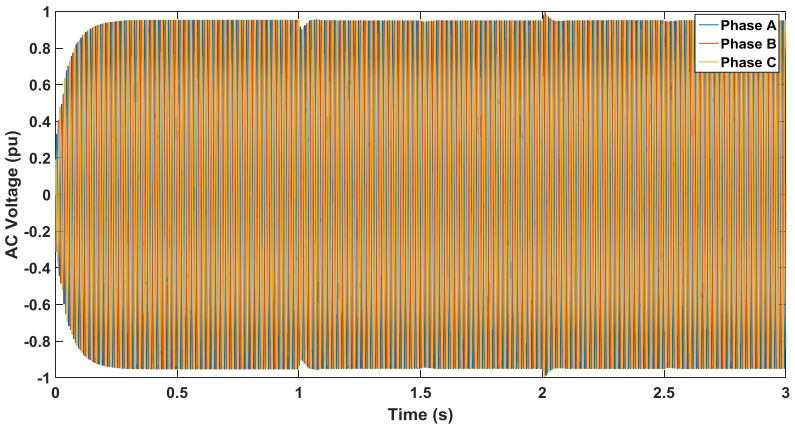


Figure 5.11 Steps on the active power references of MMCs 2 and 3. AC voltage at MMC 1 station.

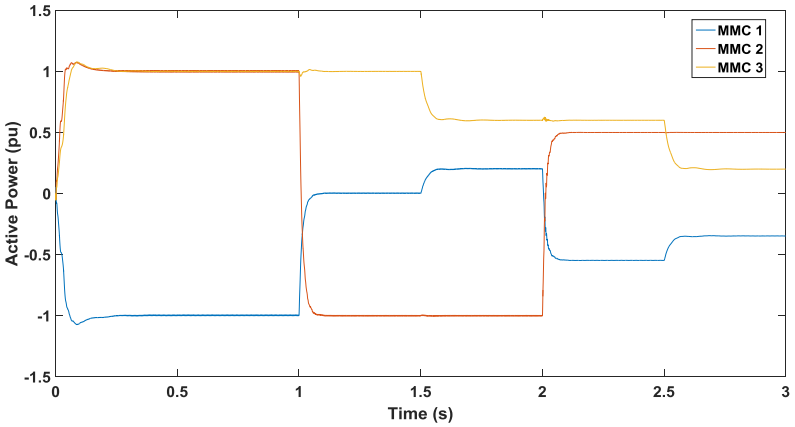


Figure 5.12 Steps on the active power references of MMCs 2 and 3. Active Power at the three ports.

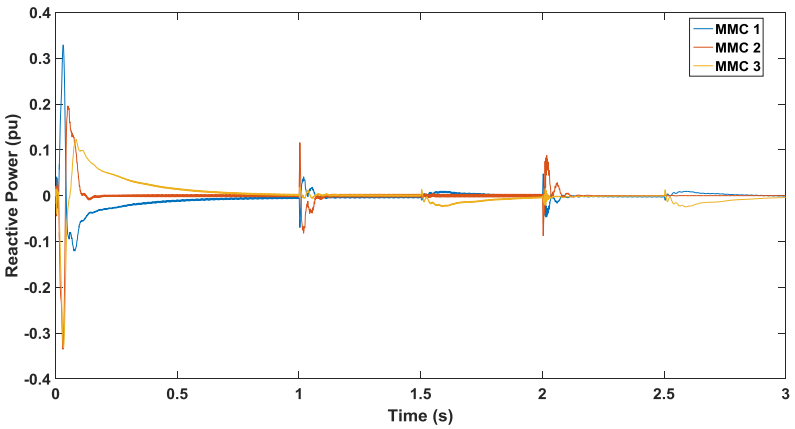


Figure 5.13 Steps on the active power references of MMCs 2 and 3. Reactive Power at the three ports.

In the following case study, the control mode in which the MMC 2 converter operates changed. MMC 2 was set to work in DC voltage control mode. Thus, MMC 2 is responsible for the regulation of the voltage of the DC line 2. The MMC 1 converter was set to operate in AC voltage control mode and the MMC 3 converter was set to operate in active power control mode. To evaluate the DC voltage control performance of MMC 2, the modulation index was set at 0.85 pu and the active power reference of MMC 3 was set at 1pu. Moreover, steps were performed on the DC voltage reference of MMC 2 and the sequence of the events is shown in Table 5.4.

Time (s)	**0**	**1.5**	**3**	**4**
MMC 2 V_{dc}^{*} (pu)	1	1.05	1	0.95

Table 5.4 DC voltage control performance of MMC2. Case study timeline.

Figure 5.15 shows that the DC voltage control of MMC 2 is fast and the references are followed with a rise time of 200 ms. Independent of the DC voltage level of MMC 2, the DC hub control operation is stable and Figure 5.17 shows that the reactive power at each port can be maintained at zero. As can be seen in Figure 5.14, the MMC 1 converter maintains the AC link voltage at 0.85 pu at all times. Finally, Figure 5.16 shows that the active power at the three ports is maintained at 1 pu, irrespective of the DC voltage level of MMC 2.

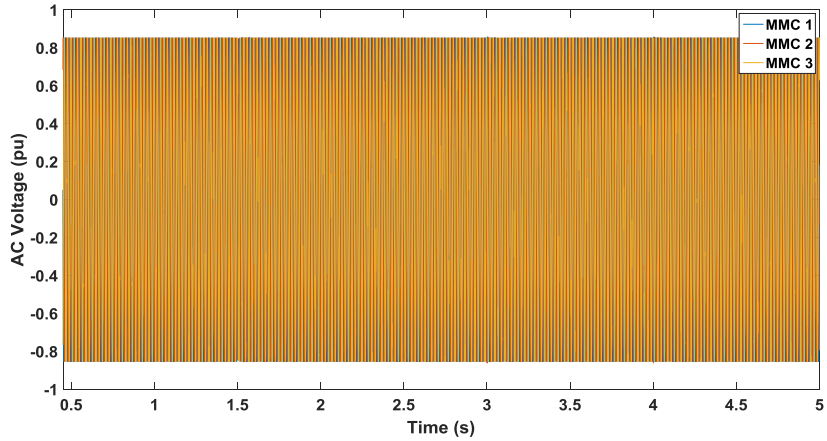


Figure 5.14 Steps on the DC voltage reference of MMC 2. AC voltage at MMC 1 station.

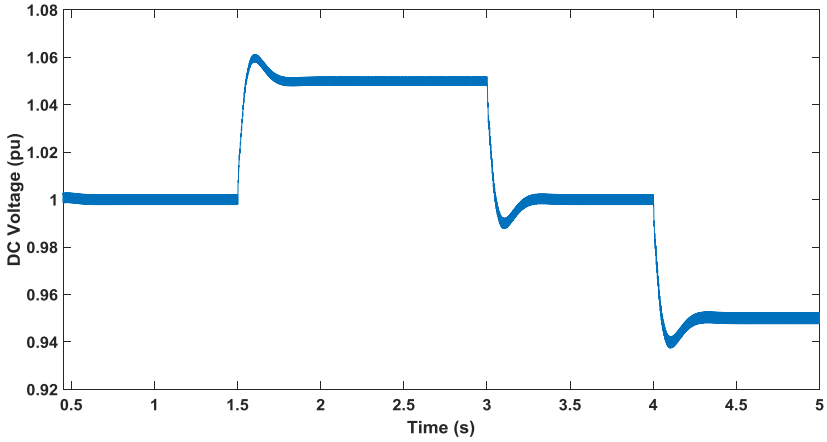


Figure 5.15 Steps on the DC voltage reference of MMC 2. DC voltage of MMC 2.

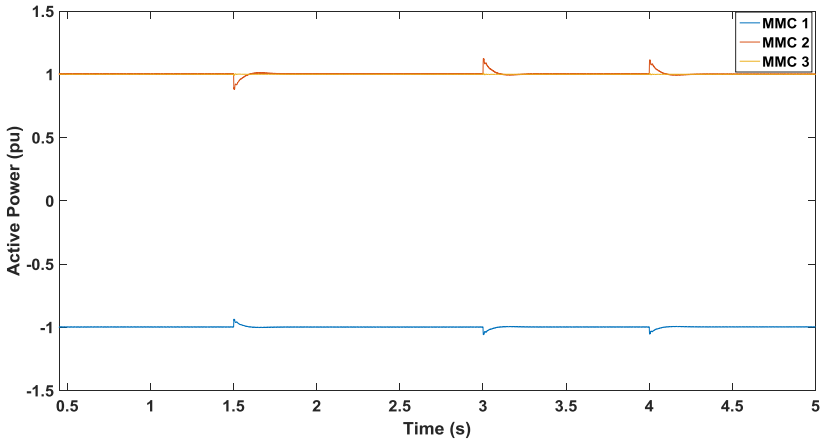


Figure 5.16 Steps on the DC voltage reference of MMC 2. Active Power at the three ports.

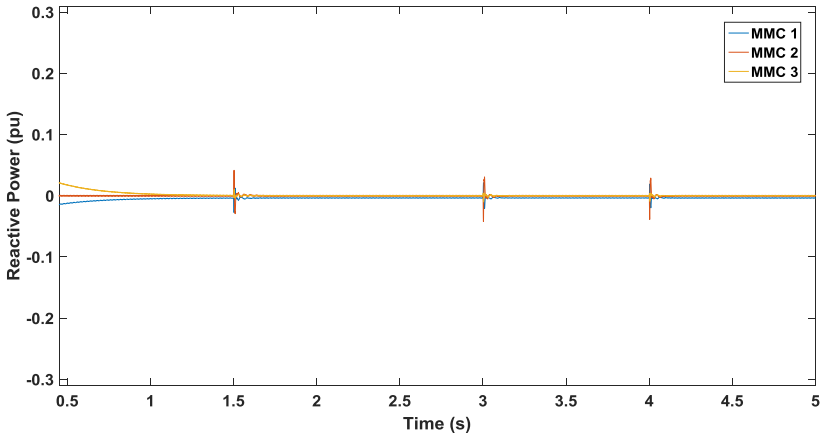


Figure 5.17 Steps on the DC voltage reference of MMC 2. Reactive Power at the three ports.

5.2 Power transfer capability of the MMC converter

According to the theoretical analysis presented in [25], there is a direct relation between the amount of energy that can be stored in the MMC converter and its power transfer capability. The theoretical analysis presented in this paper indicates that the minimum energy storage to power transfer ratio of a modular multilevel converter with a 50 Hz sinusoidal voltage reference is 20.6 J/kW, assuming that the capacitor voltages are allowed to increase by 10% above their nominal values. A decrease in the modulation index m_f (AC voltage) results in a decrease in the maximum value (peak value) of the insertion indices. A decrease in the maximum value of the insertion indices entails that the maximum number of inserted capacitors per arm is lower and as a consequence, the available amount of energy that can be stored in the MMC becomes lower. It should be mentioned that the total amount of energy that can be stored in the MMC remains constant, since the number of capacitors per arm (N) remains the same. However, the available amount of energy which is stored in the MMC is dependent on the modulation index. A low modulation index leads to low number of inserted capacitors per arm and thus, to low available stored energy per arm. Since there is a direct relation

between the energy storage and the power transfer capability of the converter, it is expected that the power transfer capability of the MMC will also be reduced.

To evaluate the relation between the amount of energy that can be stored in the MMC converter and its power transfer capability, steps were performed on the modulation index m_f of MMC 1. Given that the three MMC converters are interconnected through transformers, the modulation indices of MMCs 2 and 3 are exactly the same as the modulation index of MMC 1. The sequence of the events can be seen in Table 5.5.

As shown in Table 5.5, the modulation index m_f decreases from 0.95 to 0.35 at t=1s. The reduction of the modulation index results in a reduction of the AC voltage of MMCs 1, 2 and 3, as shown in Figure 5.18. Figure 5.19 shows that the maximum value of the insertion indices of all the MMCs also decreases. As a result, the maximum number of inserted submodule capacitors per arm and the available amount of energy which is stored in the MMC converter decrease. Due to the relation between the energy storage and the power transfer capability of the MMC, when the modulation index decreases, the active power at each port also decreases. This can be clearly seen in Figure 5.20. When the modulation index reduces from 0.95 to 0.35 (at t=1s), the active power of MMCs 2 and 3 decreases to 0.72 and 0.69 pu respectively, despite the fact that their references are set at 1pu. Finally, as shown in Figure 5.21, the average value of the sum of the capacitor voltages of each arm of MMC 1 is maintained constant at 1pu. Assuming that the voltage profile of each submodule capacitor is the same, the average value of the voltage of each capacitor is also kept constant at 1pu ($\overline{V_{sm}} = 1pu$). The total energy which is stored in the converter can be expressed as $W_{conv} = 6 \cdot W_{arm}$, where W_{arm} is the total energy stored in each arm of the converter. The total energy which is stored in each converter arm is equal to $W_{arm} = N \cdot \frac{1}{2} \cdot C \cdot \overline{V_{sm}}^2$, where N is the number of submodules per arm and C is the submodule capacitance. Thus, the total energy which is stored in the converter can now be rewritten as $W_{conv} = 6 \cdot N \cdot \frac{1}{2} \cdot C \cdot \overline{V_{sm}}^2$. Given that $\overline{V_{sm}}$ is maintained constant at 1pu, the total converter energy remains constant, despite the fact that the modulation index decreases.

Time (s)	**0**	**1**
Modulation index m_f	0.95	0.35

Table 5.5 Reduction of modulation index. Case study timeline.

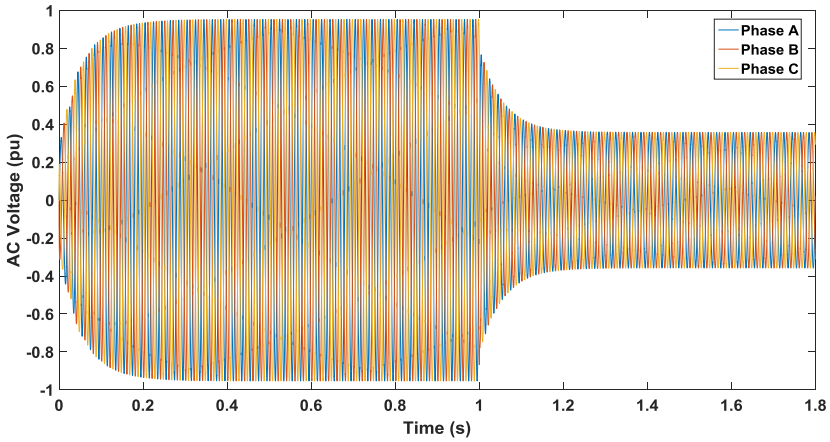


Figure 5.18 Reduction of the modulation index of MMC 1. AC voltage at MMC 1 station.

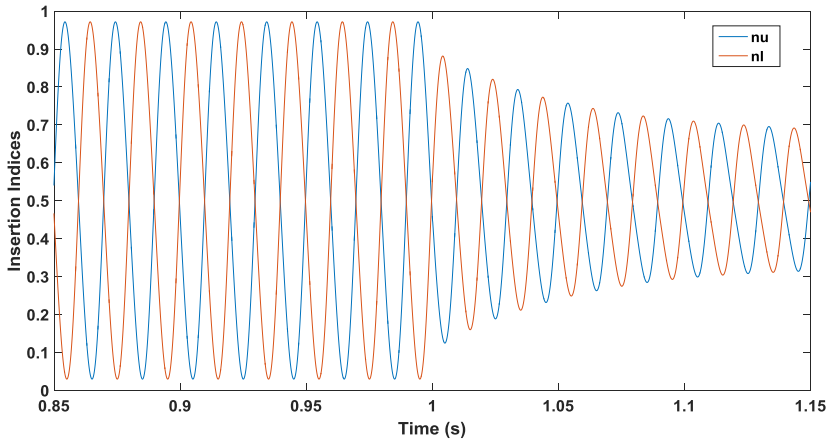


Figure 5.19 Reduction of the modulation index of MMC 1. Zoomed view of the insertion indices n_u and n_l of phase A of MMC 1 station.

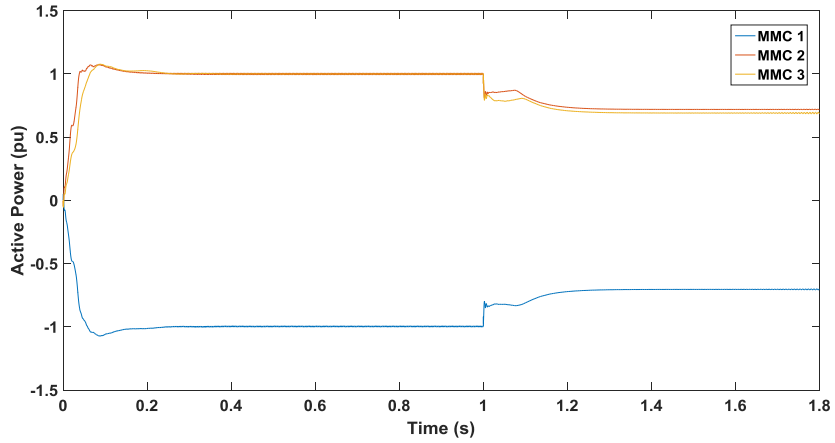


Figure 5.20 Reduction of the modulation index of MMC 1. Active power at the three ports.

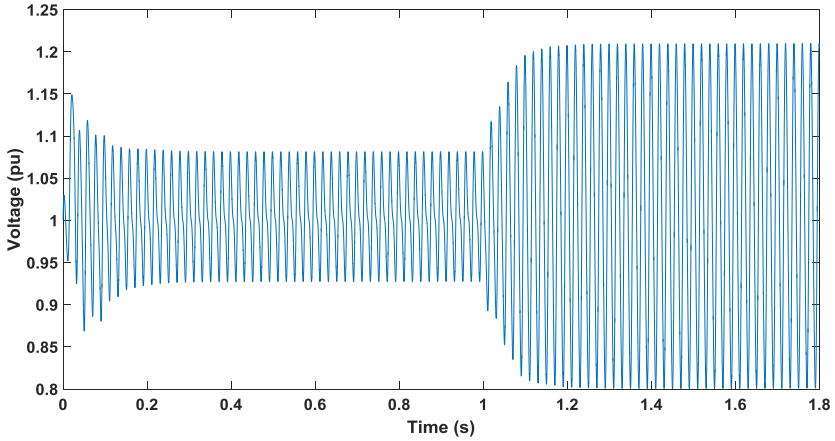


Figure 5.21 Reduction of the modulation index of MMC 1. Zoomed view of the sum of the capacitor voltages of the upper arm of phase A of MMC 1 station.

Table 5.6 shows the relation between the modulation index and the active power of MMCs 2 and 3. It is clear that a reduction in the modulation index leads to a reduction in the power transfer capability of the MMC. Moreover, an MMC operating with low modulation index has lower efficiency due to the fact that for the same power transfer, the voltage is reduced and thus, the current and the losses of the converter increase.

Figure 5.22 shows the relation between the active power of MMC 2 and the modulation index. All the data were taken from Table 5.6. The graph was approached using a 4^{th} degree polynomial function. The function that relates the active power of MMC 2 with the modulation index was calculated using *Matlab* and can be given by the following formula

$$P_2 = a_1 \cdot {m_f}^4 + a_2 \cdot {m_f}^3 + a_3 \cdot {m_f}^2 + a_4 \cdot m_f + a_5 \tag{5.2}$$

where $a_1 = 4.7928,\ a_2 = -9.089,\ a_3 = 3.588,\ a_4 = 1.7416\ and\ a_5 = 0.00094276.$

m_f	$P_2(pu)$	$P_3(pu)$
0.95	1	1
0.9	1	1
0.85	1	1
0.8	1	1
0.75	1	1
0.7	1	1
0.65	1	1
0.6	1	1
0.55	1	1
0.5	0.94	0.93
0.45	0.87	0.86
0.4	0.8	0.77
0.35	0.72	0.69
0.3	0.64	0.6
0.25	0.55	0.52
0	0	0

Table 5.6 Relation between the modulation index and the active power of MMCs 2 and 3.

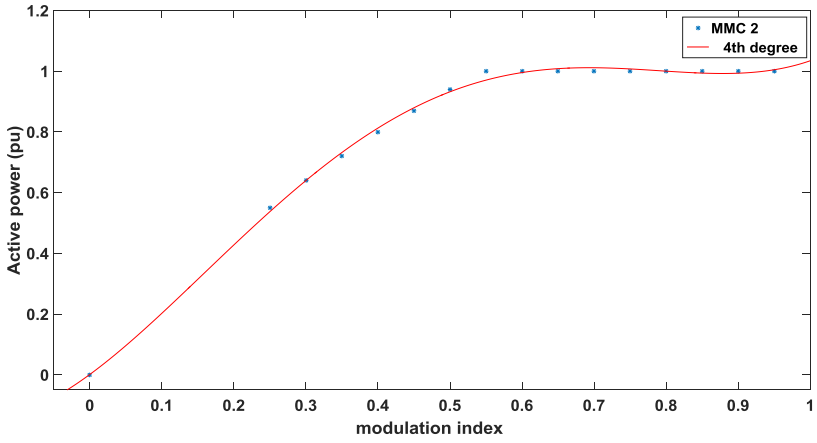


Figure 5.22 Relation between the modulation index and the active power of MMC 2.

5.3 Direct interconnection of HVDC lines

The three HVDC lines with characteristics as shown in Table 5.1 could also be directly interconnected without using transformers. The recommended topology can be seen in Figure 5.23. In this case, the MMC with the lowest DC link voltage determines the voltage level of the AC link. It implies that the MMCs with higher DC link voltage will be underutilised since their output AC voltage will be lower than the rated. As a result, for the same power transfer , the currents and thus, the losses of these converters will be higher. Moreover, as discussed in section 5.2, the power transfer capability of these converters will also be reduced due to the lower modulation index.

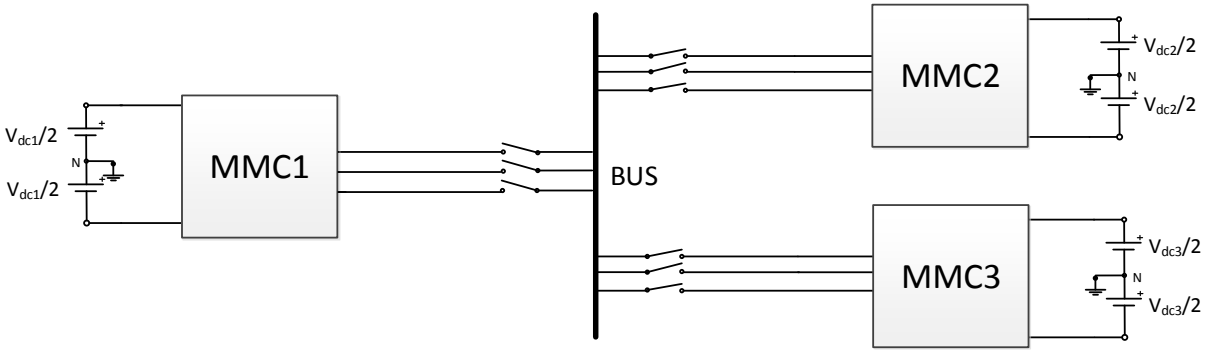


Figure 5.23 Direct interconnection of HVDC lines.

As mentioned before, the MMC converter with the lowest DC voltage determines the voltage level of the AC link. As a result, the other MMC converters of the DC hub topology will be underutilized. This can be clearly seen in Figures 5.24 and 5.25. The AC voltages of MMCs 1 and 2 are 0.2 and 0.24 pu respectively. On the other hand, as can be seen in Figure 5.26, the AC voltage of MMC 3 is maintained at 1 pu.

Due to the relation between the modulation index and the power transfer capability of the MMC, the power transfer capability of MMCs 1 and 2 will be reduced. It should be mentioned that the power transfer capability of MMC 3 is not affected since its AC voltage is equal to the rated. However, the active power of MMC 1 is equal to the sum of the active power of MMCs 2 and 3 ($P_1 = P_2 + P_3$), since MMC 1 works in AC voltage control mode and its active power is determined by the other two converters which operate in active power control mode. For this reason, the sum of the active power of MMCs 2 and 3 should be low, given that MMC 1 is underutilized and its power transfer capability is reduced. To evaluate the steady state operation of the investigated DC hub, the active power references of MMCs 2 and 3 were set at 0.3 pu. As shown in Figure 5.27, the active power of ports 2 and 3 follows the references and the active power of port 1 is equal to the sum of the active power of the other two ports. Finally, Figure 5.28 shows that the reactive power at the three ports can be maintained at zero.

The main disadvantages of this topology are the reduced efficiency and power transfer capability of the system. On the other hand, the cost and the footprint of the system are significantly lower since bulky power transformers are not used. In general, the DC hub topology with direct interconnection is recommended for applications in which the voltage levels of the lines are similar.

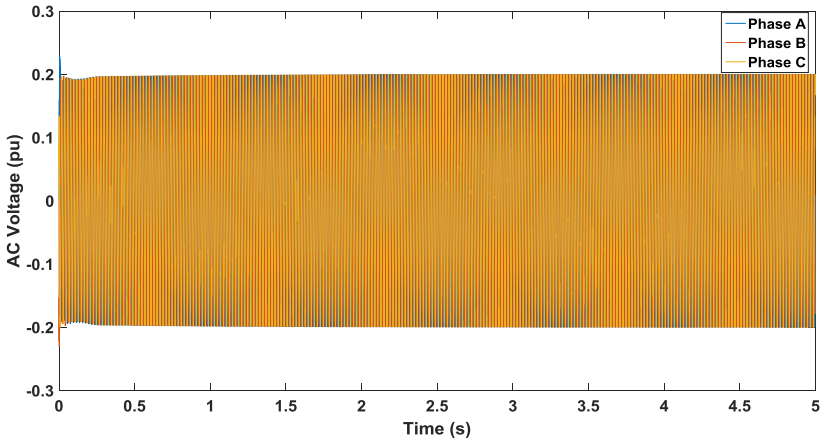


Figure 5.24 Direct interconnection of HVDC lines. AC voltage at MMC 1 station.

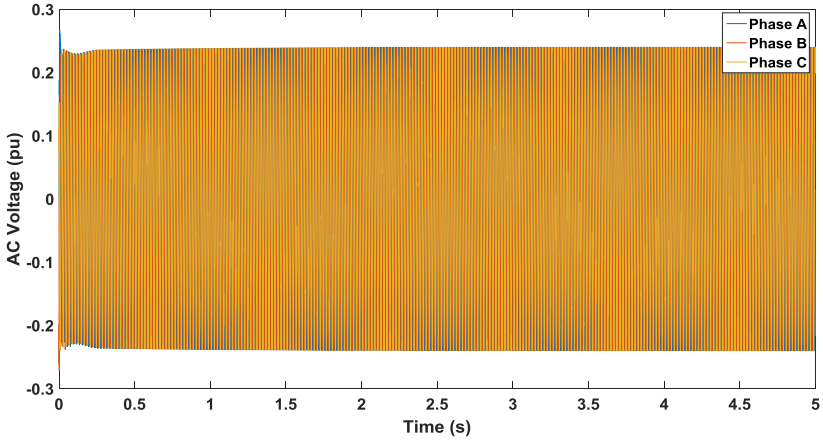


Figure 5.25 Direct interconnection of HVDC lines. AC voltage at MMC 2 station.

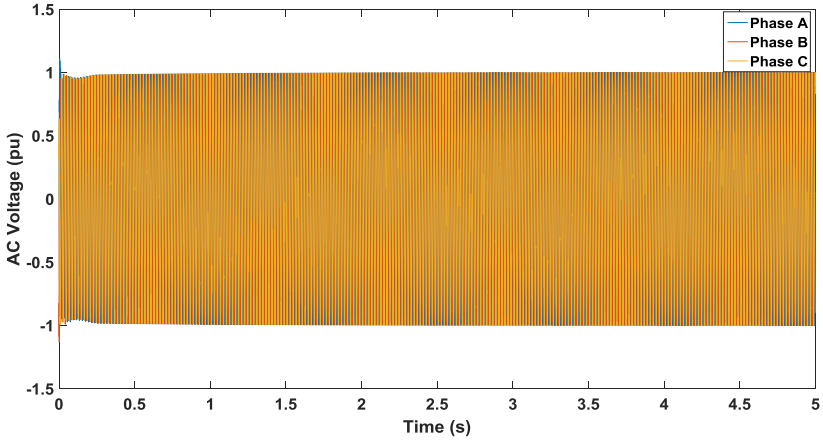


Figure 5.26 Direct interconnection of HVDC lines. AC voltage at MMC 3 station.

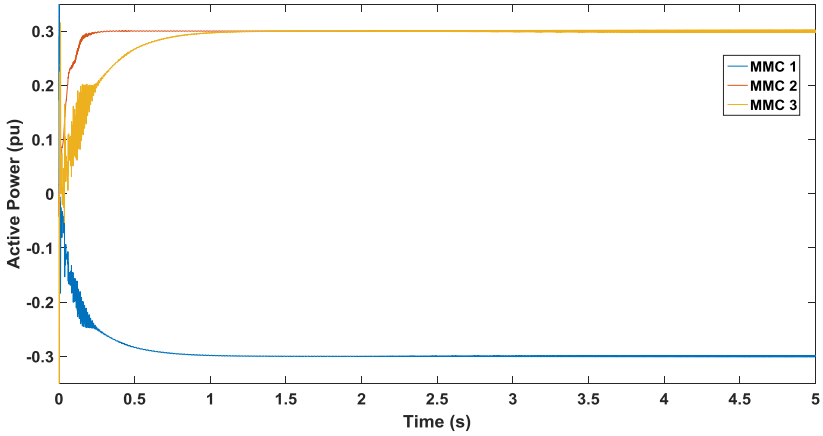


Figure 5.27 Direct interconnection of HVDC lines. Active power at the three ports.

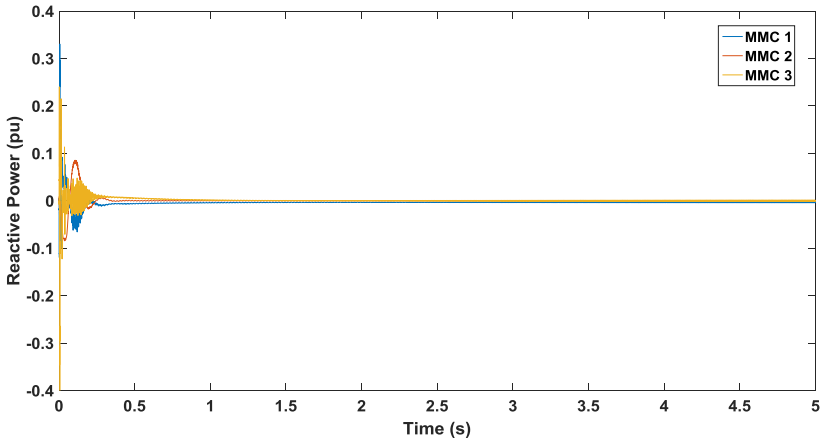


Figure 5.28 Direct interconnection of HVDC lines. Reactive power at the three ports.

5.4 Interconnection of HVDC lines using LCL filters

As described in section 5.3, the direct interconnection of HVDC lines is recommended for applications in which the voltage levels of the lines are similar. Otherwise, the efficiency and the power transfer capability of the system will be reduced. In case a fault occurs at the DC or AC side of a port, the MMC-based DC hub has an intrinsic property to limit the fault current prior to any control actions. More specifically, the arm inductors of each MMC can act as current limiting inductors. In contrast to the 2-level converters, where series inductors need to be connected to the AC side of the converter in order to offer protection against faults, in case of the MMC, these inductors are incorporated into the arms of the converter, giving the converter an inherent capability to limit fault currents and protect its power devices (IGBTs, capacitors, diodes).

However, in case enhanced protection against faults is necessary, series inductors could be connected to the AC side of each MMC converter. In the three-port DC hub topology described in the previous sections, the reactive power at ports 2 and 3 can be maintained at zero by controlling the d component of the current of each MMC. In case series inductors are connected to each port, the reactive power at ports 2 and 3 will be controlled at zero and the whole amount of the reactive

power which is absorbed by the series inductors will be provided by port 1, which is responsible for the control of the voltage of the AC link and its currents are uncontrolled. This is not desired since the power transfer capability of port 1 will be reduced. For this reason, parallel capacitors should be connected to the AC side of each port to provide the reactive power which is absorbed by the series inductors. In this manner, the reactive power at each port can be maintained at zero and the power transfer capability of the DC hub will be the highest possible. The DC hub topology using LCL filters can be seen in Figure 5.29.

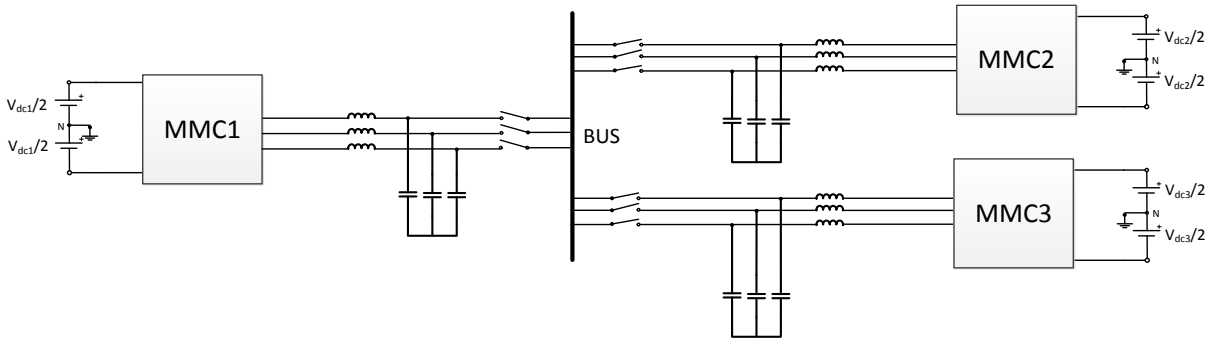


Figure 5.29 Interconnection of HVDC lines using LCL filters.

Some formulas for the computation of the L, C components of the LCL filter are presented in [10]. However, the value of the series inductance L which is given by the suggested formulas is very high and as a consequence, the voltage drop across the series inductor is also high. For this reason, the values of the L, C components will not be calculated according to the formulas presented in [10].

The use of LCL filters increases the footprint and cost of the system. The DC hub topology is used for the interconnection of multiple HVDC lines and as the number of the lines increases, the number of the LCL filters which should be connected to each line also increases. In order to keep the cost and the volume of the system as low as possible, the series inductors which are connected to each port should be as small as possible. As mentioned before, in case of the MMC, the use of series inductors is not necessary, since the arm inductors of the converter can also limit the fault currents.

For this reason, a series inductance equal to 20% of the arm inductance will be connected to each phase of each MMC. Moreover, parallel capacitors should be connected to each MMC to provide the reactive power which is absorbed by the inductors. In this manner, the reactive power at each port can be maintained at zero, and any port can be connected or disconnected from the DC hub without affecting the reactive power of the other ports (modularity). The formulas that will be used for the computation of the L, C components of the filter are given below

$$L = 0.2 \cdot L_{arm} \tag{5.3}$$

$$C = \frac{L \cdot P^2}{9 \cdot {U_{ph\_rms}}^4} \tag{5.4}$$

where L_{arm} is the arm inductance of the MMC, P is the active power which is transferred through the MMC and U_{ph_rms} is the rms value of the line-to-ground voltage of the MMC.

To evaluate the operation of the DC hub using LCL filters, three HVDC lines were interconnected through LCL filters and the network parameters along with the MMC specifications are shown in Table 5.7. Given that transformers are not used, the port with the lowest DC voltage determines the voltage level of the intermediate AC link. As shown in Figure 5.30, the AC voltage at MMC 1 is maintained at 0.67 pu. The active power references of ports 2 and 3 were set at 1 pu. As shown in Figure 5.31, the active power references at each port are respected and the active power of port 1 is equal to the sum of the active power of the other two ports ($P_1=P_2+P_3$). Finally, the capacitors which are connected in parallel to each port provide all the necessary reactive power which is absorbed by the series inductors and as a consequence, the reactive power at each port is maintained at zero, as shown in Figure 5.32.

Network parameters	**Unit**	**Value**
Rated power ($S_{b1}/S_{b2}/S_{b3}$)	GVA	1.2/0.6/0.6
DC voltage ($V_{dc1}/V_{dc2}/V_{dc3}$)	kV	600/500/450
MMC 1 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	0.4
Arm inductance (L)	mH	57.3
Arm resistance (R)	Ohm	1.8
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20
MMC 2 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	0.288
Arm inductance (L)	mH	79.6
Arm resistance (R)	Ohm	2.5
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20
MMC 3 specifications	**Unit**	**Value**
Cell capacitance (C)	mF	0.35
Arm inductance (L)	mH	64.5
Arm resistance (R)	Ohm	2
Number of SMs per arm (N)	-	12
Carrier frequency (f_c)	Hz	600
Sampling frequency (f_s)	kHz	20
LCL filters	**Unit**	**Value**
Series inductance at MMC 1 (L_1)	mH	11.5
Parallel capacitance at MMC 1 (C_1)	μF	4.6
Series inductance at MMC 2 (L_2)	mH	15.9
Parallel capacitance at MMC 2 (C_2)	μF	1.6
Series inductance at MMC 3 (L_3)	mH	12.9
Parallel capacitance at MMC 3 (C_3)	μF	1.3

Table 5.7 Interconnection using LCL filters. Network parameters and MMC specifications.

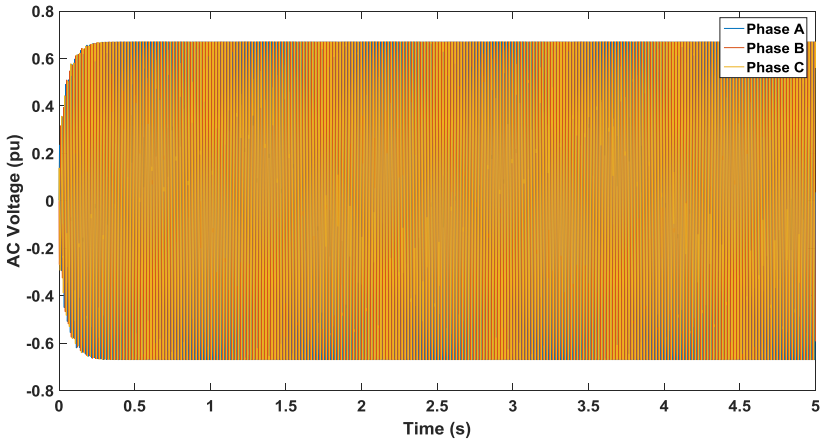


Figure 5.30 Interconnection of HVDC lines using LCL filters. AC voltage at MMC 1 station.

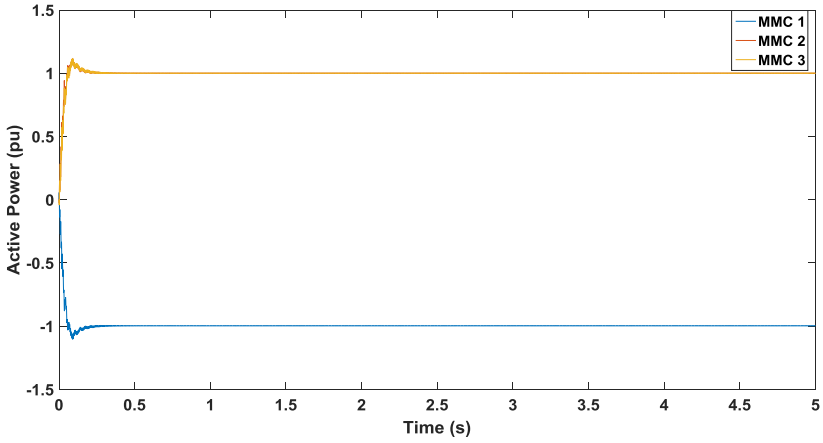


Figure 5.31 Interconnection of HVDC lines using LCL filters. Active power at the three ports.

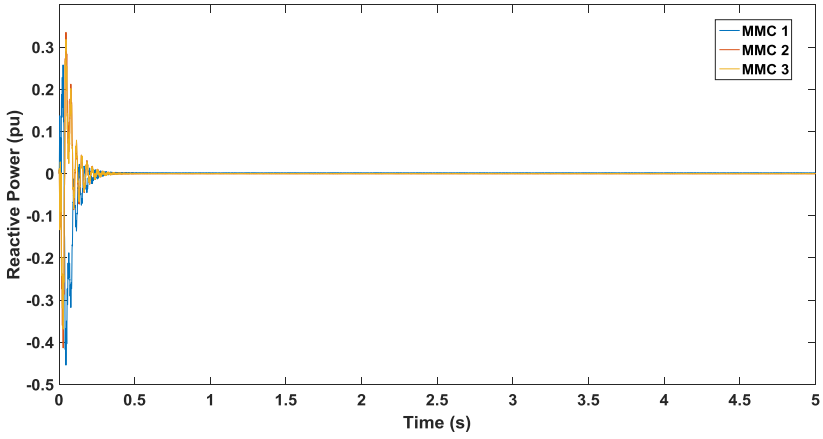


Figure 5.32 Interconnection of HVDC lines using LCL filters. Reactive power at the three ports.

5.5 Conclusion

In this chapter, different DC hub topologies which could be used for the interconnection of multiple HVDC lines operating at different voltage levels were investigated. In case the voltage levels of the interconnected HVDC lines are different, the DC hub topology using transformers is the most suitable one, since each MMC converter can operate close to its rated characteristics (rated voltage) and the efficiency and the power transfer capability of the system are the highest possible. However, the use of transformers increases the total investment cost and volume of the system. The HVDC lines could also be interconnected without using transformers. They could be interconnected directly or using LCL filters. In case the HVDC lines are interconnected without transformers and their voltage levels are different, the efficiency and the power transfer capability of the system will be significantly lower. On the other hand, in case the HVDC lines are interconnected without transformers and their voltage levels are similar, the efficiency and the power transfer capability of the system will be high. In case enhanced protection against faults is necessary, the use of the DC hub topology with LCL filters is preferable. However, the use of filters increases the total cost and volume of the system and thus, the L,C components should be as small as possible. Depending on the voltage levels of the interconnected lines, the system requirements, the available budget and the application (onshore or offshore), it is up to the system designer to select the most appropriate DC hub topology and to optimize the operation of the system. Given that the main goal of the DC hub is the interconnection of multiple HVDC lines operating at different voltage levels, the DC hub topology using transformers is the most suitable one. For this reason, this is the topology which will be used in the following case studies.

6.Case Study 2: Connection/Disconnection of ports and AC faults within the DC Hub

In this chapter, a methodology will be presented for the connection or disconnection of ports from the intermediate AC link of the DC hub and the expandability of the DC hub will also be investigated. Moreover, a methodology will be presented for the clearing of AC faults within the DC hub.

6.1 Methodology for the connection/disconnection of ports

Any port should be easily connected or disconnected from the DC hub without affecting the operation of the other ports. In this section, a methodology will be presented for the safe connection or disconnection of ports from the DC hub. As shown in Figure 6.1, port 2 needs to be disconnected from the DC hub. The necessary actions that should be taken before the disconnection of port 2 are the following:

1. The active power reference of port 2 should be set at zero a few milliseconds before the disconnection. In this way, the active power of port 2 will be zero at the moment of the disconnection. It was shown through simulations (which are not presented) that when the active power of port 2 is different than zero at the moment of the disconnection, the distortion of the AC link voltage and the active power waveforms of the other two ports are higher. For this reason, the active power of port 2 should be controlled at zero at the moment of the disconnection.

2. The mechanical AC breaker of port 2 should open.

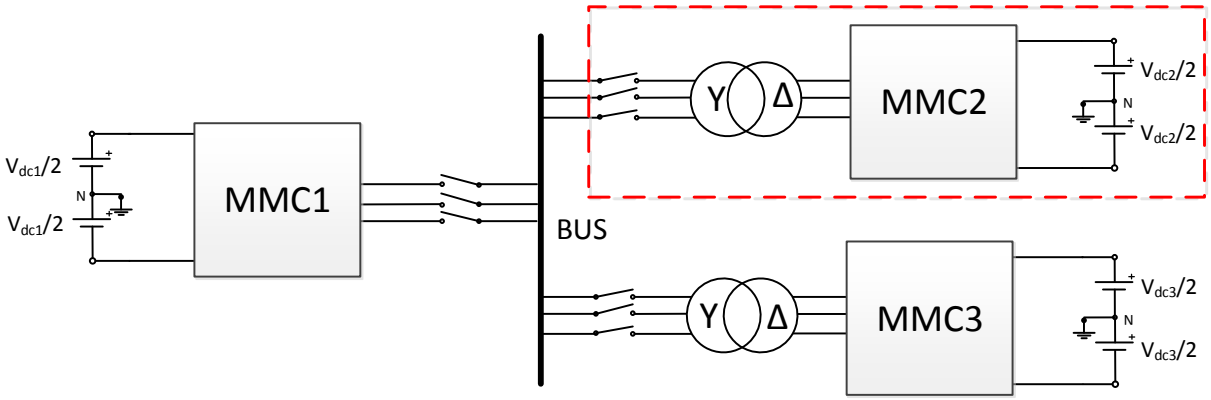


Figure 6.1 Connection/Disconnection of MMC 2.

To evaluate the operation of the system during the disconnection of port 2, three HVDC lines with characteristics as shown in Table 5.1 were interconnected. The modulation index was set at 0.95 and the active power references of ports 2, 3 were set at 1 pu. The AC circuit breaker of port 2 opens at t= 1s. The active power reference of port 2 is set at zero 80 ms before the opening of the AC circuit breaker (at t=0.92 s) because the active power of port 2 can change from 1 pu to 0 pu within 80 ms. As a consequence, the active power of port 2 is zero at the moment of the disconnection. As shown

in Figure 6.2, the voltage of the AC link is maintained at 0.95 pu and it is not affected by the disconnection of port 2. At t=0.92 sec, the active power of port 2 decreases and a voltage drop is observed in the voltage waveform of the AC link. As shown in Figure 6.3, the amplitude of the arm current of MMC 1 is reduced from 1 pu to 0.5 pu because port 2 is disconnected from the DC hub at t=1s and this results in a reduction of the active power that is transferred through port 1. Given that the voltage of the AC link remains constant, the AC current of MMC 1 decreases ($P = V \cdot I$). Figure 6.4 shows that the arm current of MMC 2 becomes zero after its disconnection and Figure 6.5 shows that the arm current of MMC 3 is not affected by the disconnection of MMC 2. It should be mentioned that after the disconnection of port 2, the amplitude of the arm currents of all the MMCs is maintained within the acceptable limits and the DC hub can continue its normal operation. As can be seen in Figure 6.6, after the disconnection of port 2, the active power of port 2 goes to zero, the active power of port 1 changes from 1 pu to 0.5 pu and the active power of port 3 is kept at 1 pu. Figure 6.7 shows that the reactive power at the three ports is maintained at zero at all times. Finally, it was shown through simulations (that are not presented) that the higher the DC link voltage of the port which is disconnected from the DC hub, the higher the variation of the active power waveform of port 1 and the AC link voltage will be.

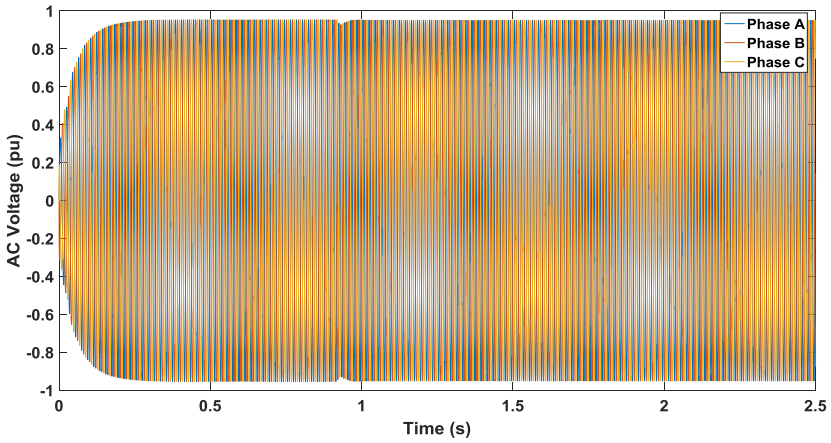


Figure 6.2 Disconnection of MMC 2. AC voltage at MMC 1 station.

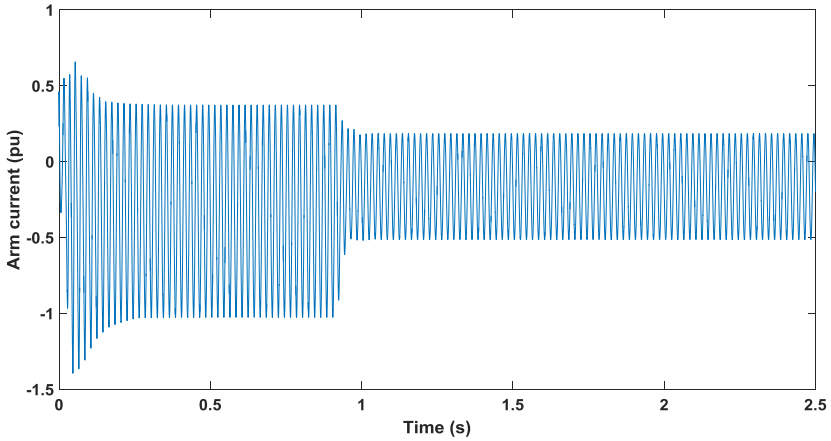


Figure 6.3 Disconnection of MMC 2. Upper arm current of phase A of MMC 1 station.

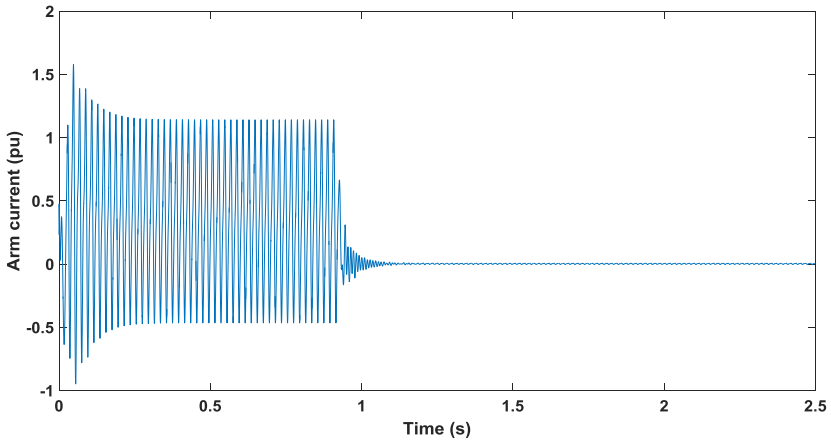


Figure 6.4 Disconnection of MMC 2. Upper arm current of phase A of MMC 2 station.

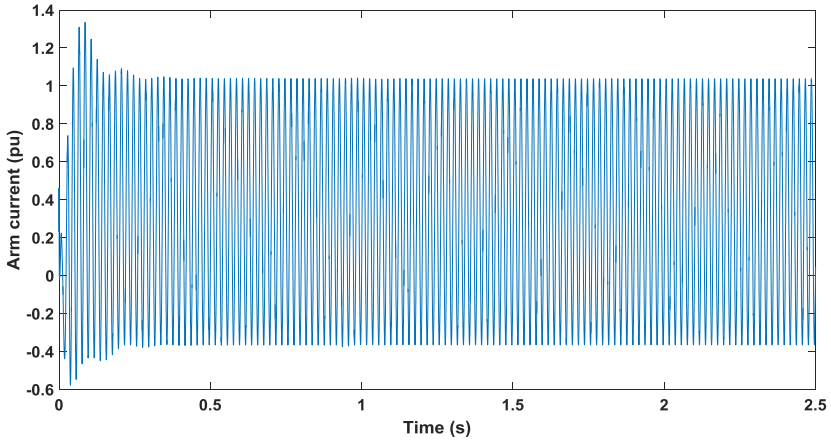


Figure 6.5 Disconnection of MMC 2. Upper arm current of phase A of MMC 3 station.

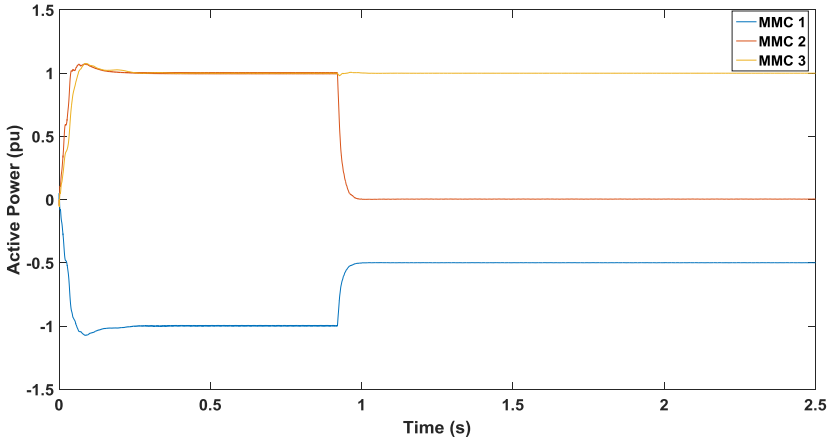


Figure 6.6 Disconnection of MMC 2. Active power at the three ports.

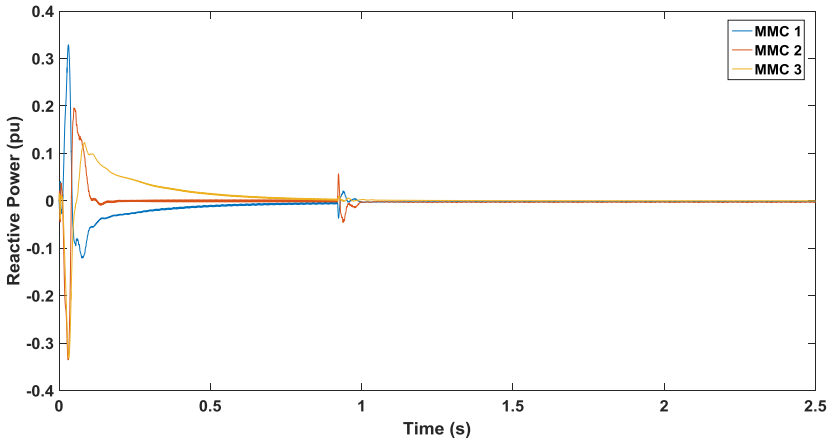


Figure 6.7 Disconnection of MMC 2. Reactive power at the three ports.

In the following part of this section, the methodology for the connection of a port will be presented. In case port 2 needs to be inserted, the necessary actions that should be taken are the following:

1. The active power of port 2 should be zero at the instant of the insertion. It was shown through simulations (which are not presented) that when the active power of port 2 is different than zero at the moment of the insertion, the distortion of the AC link voltage and the active power waveforms of the other two ports is higher. For this reason, the active power of port 2 should be zero at the moment of the insertion.
2. The AC voltage of MMC 2 should be synchronized with the voltage of the AC link at the instant of the insertion.
3. The mechanical AC breaker of port 2 should close.
4. The active power reference of port 2 should be set at the desired value right after the closing of the AC breaker.

To evaluate the stability of the system during the insertion of port 2, three HVDC lines with characteristics as shown in Table 5.1 were interconnected. The modulation index was set at 0.95 and the active power references of ports 2 and 3 were set at 1 pu. The AC circuit breaker of port 2 closes at t=1s. At the moment of the insertion, the active power of port 2 is zero and the AC voltage of MMC 2 is synchronized with the voltage of the AC link. As shown in Figure 6.8, the AC voltage of MMC 1 is maintained at 0.95 pu. Figure 6.9 shows that, after the insertion of port 2, the amplitude of the arm current of MMC 1 changes from 0.5 to 1.05 pu. The active power of port 1 is equal to the sum of the active power of ports 2 and 3. Thus, the insertion of port 2 results in an increase in the active power that is transferred through port 1, and given that the AC voltage at MMC 1 is kept constant, the arm currents of MMC 1 increase ($P = V \cdot I$). Figure 6.10 shows that the amplitude of the arm currents of MMC 2 changes from 0 to 1.05 pu at t=1s. Before the insertion of port 2, its active power and thus, its current is zero. After its insertion, its active power is controlled at 1 pu and as a result, its current increases. Figure 6.11 shows that the amplitude of the arm current of MMC 3 is maintained at 1.05 pu and it is not affected by the insertion of port 2. It should be mentioned that, after the insertion of port 2, the voltage of the AC link is controlled at 0.95 pu and the active power of each port is controlled at 1 pu. Given that the reactive power at each port is maintained at zero, as shown in Figure 6.13, the relation between the active power, voltage and current of each port can be written as $p = u \cdot i$, where u is the voltage of the port (in pu) and i is the current of the port (in pu). Given that u=0.95 pu and p= 1pu, the current of each port (i) should be equal to 1.05 pu. For this

reason, after the insertion of port 2, the amplitude of the arm currents of each port is equal to 1.05 pu. Figure 6.12 shows the active power at the three ports before and after the insertion of port 2. The active power of port 3 is maintained at 1 pu and it is not affected by the insertion of port 2. The active power of port 2 is zero before its insertion and it is controlled at 1pu after its insertion. The active power of port 1 is 0.5 pu before the insertion of port 2, since it is only connected to port 3 and the power rating of port 3 is half of the power rating of port 1. After the insertion of port 2, the active power of port 1 is controlled at 1 pu.

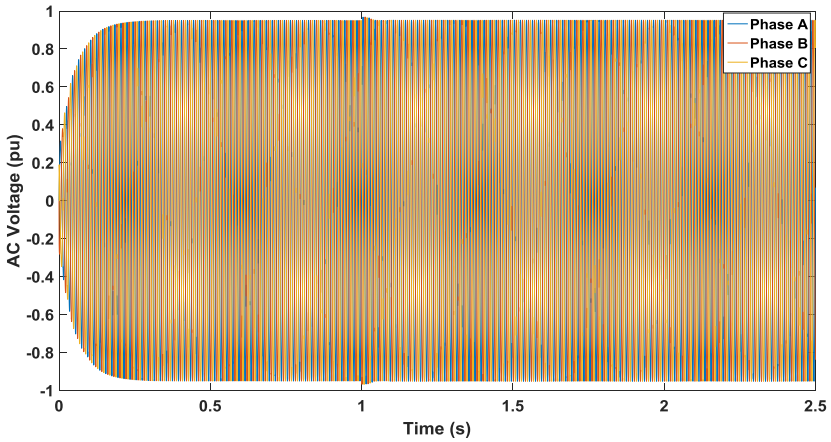


Figure 6.8 Connection of MMC 2. AC voltage at MMC 1 station.

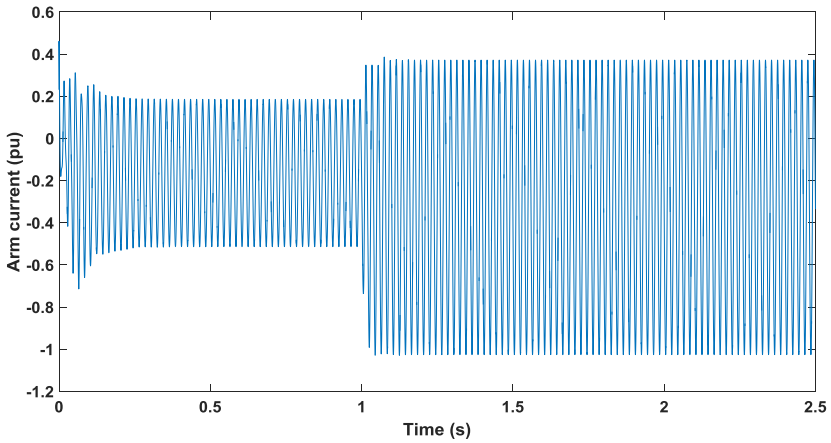


Figure 6.9 Connection of MMC 2. Upper arm current of phase A of MMC 1 station.

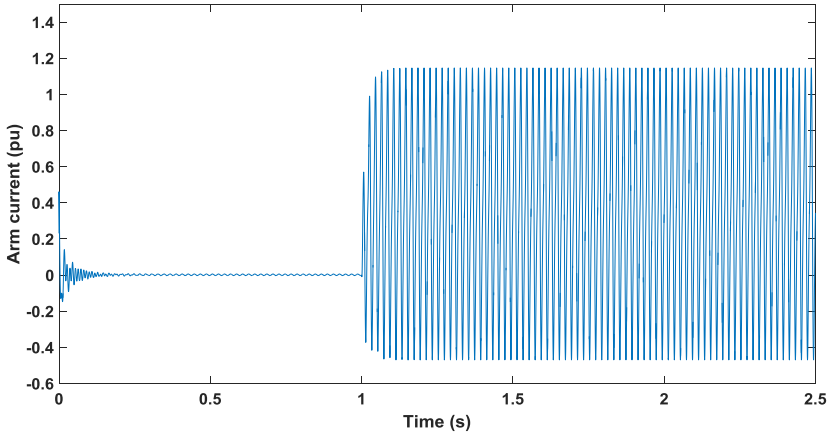


Figure 6.10 Connection of MMC 2. Upper arm current of phase A of MMC 2 station.

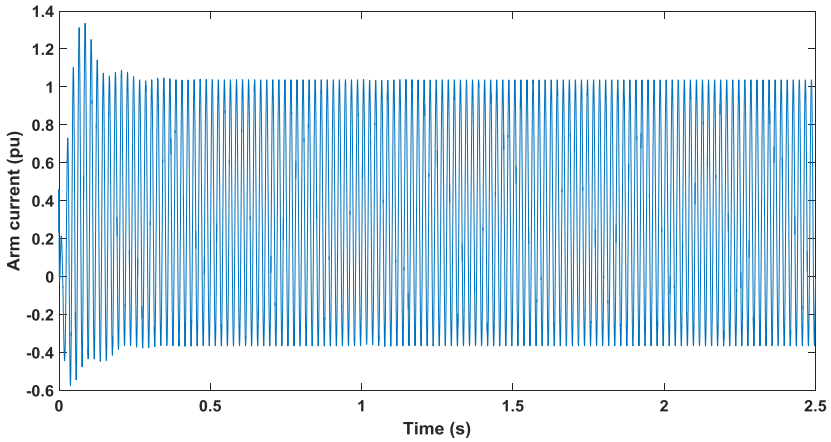


Figure 6.11 Connection of MMC 2. Upper arm current of phase A of MMC 3 station.

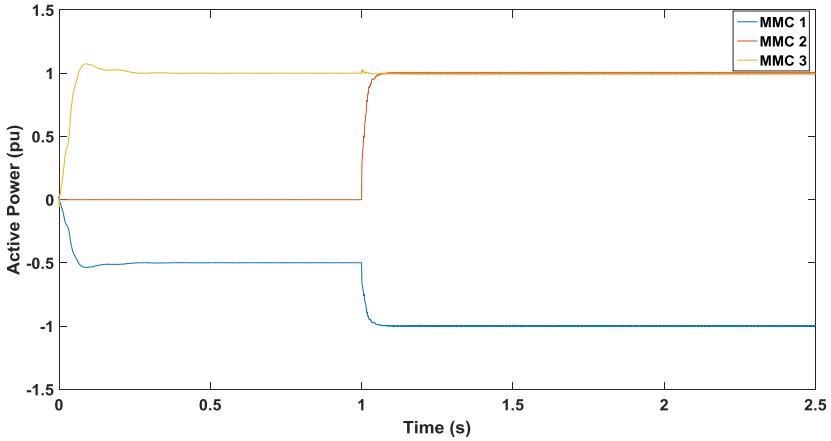


Figure 6.12 Connection of MMC 2. Active power at the three ports.

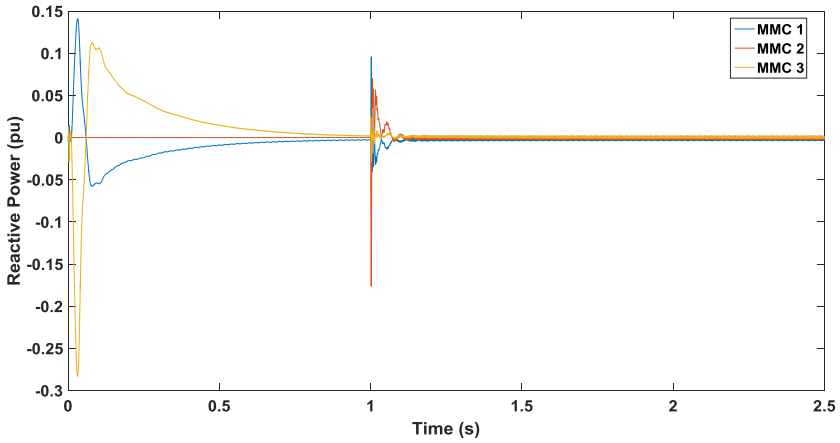


Figure 6.13 Connection of MMC 2. Reactive power at the three ports.

6.2 Methodology for clearing AC faults within the DC Hub

In this section, a methodology will be presented for the clearing of AC faults within the DC hub. As can be seen in Figure 6.14, a three-phase-to-ground fault occurs at the primary of the transformer which is connected to port 2. Before presenting the analytical methodology, the behaviour of the DC hub under the occurrence of AC faults will be investigated without performing any control actions.

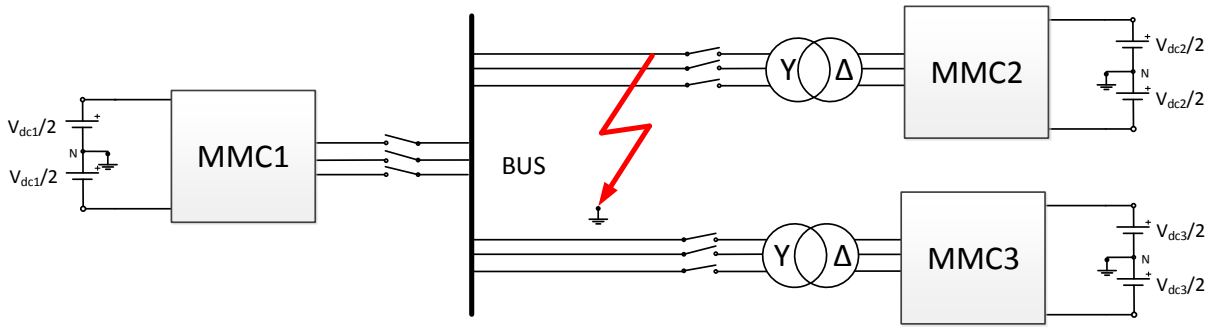


Figure 6.14 AC fault at MMC 2.

To investigate the operation of the DC hub under the occurrence of AC faults, three HVDC lines with characteristics as shown in Table 5.1 were interconnected. The modulation index was set at 0.95 pu and the active power references of ports 2 and 3 were set at 1 pu. A three-phase-to-ground fault occurs at port 2 at t=1sec. The fault can be detected within a few milliseconds by current sensors which are connected to the arms of the converters. Once the fault is detected, the AC breaker of port 2 should open. The mechanical AC breakers are generally slow and can open within 2-3 cycles [79]. Given that the operating frequency is 50 Hz, the mechanical AC breaker of port 2 can open within 40-60 ms. In the worst case scenario, the AC breaker of port 2 will open within 60ms after the occurrence of the fault (at t'=1.06s). Once the arm current of any MMC converter exceeds its maximum acceptable value (1.1 pu), the fault can be detected by current sensors which are connected to the arms of the converters. It was shown through simulations that the fault can be detected within 2ms after its occurrence and this time interval will not be taken into account.

As shown in Figure 6.15, at the instant of the fault (t=1s), the voltage of the AC link goes to zero. Then, it starts increasing again because MMC 1 works in AC voltage control mode and its AC voltage reference is set at 0.95 pu (equal to the modulation index). The fault current can be expressed as

$$I_F = \frac{V_f}{R_f} \tag{6.1}$$

where V_f is the voltage of the AC link and R_f is the fault resistance. A typical value of the fault resistance is 20 Ω [78]. Given that the voltage of the AC link is high and the fault resistance is too small, the resulting fault current will be too high. As can be seen in Figure 6.15, in the time interval between 1 and 1.06 s (before the opening of the AC breaker), the voltage of the AC link gradually increases from 0 pu to 1.1 pu. As a result, the fault current will also increase. MMCs 2 and 3 operate in active power control mode and their currents are controlled. However, MMC 1 operates in AC voltage control mode and its arm currents are not controlled. For this reason, MMC 1 will have the largest contribution to the fault current. Figure 6.16 shows that the arm currents of MMC 1 gradually increase in the time interval between 1 and 1.06 s and they reach values up to 20 pu. On the other hand, as shown in Figure 6.17, the arm currents of MMC 3 are controlled and can be maintained within the acceptable limits during the same time interval (lower than 2 pu). The maximum acceptable limit for the arm current is 2 pu and it is determined by the maximum current that the IGBTs can withstand [80]. As a consequence, in case a fault occurs at port 2 and no extra control actions are performed, the IGBTs of MMC 1 could not withstand its arm overcurrents and the MMC 1 converter would be damaged.

The amplitude of the arm currents of MMC 1 could be reduced if series inductors were connected to each port (current limiting inductors). The series inductors should be very large and extra parallel capacitors should be connected to each port to provide the reactive power which is absorbed by the inductors. In this case, the cost and volume of the system would be significantly higher and thus, the addition of LCL filters is not recommended.

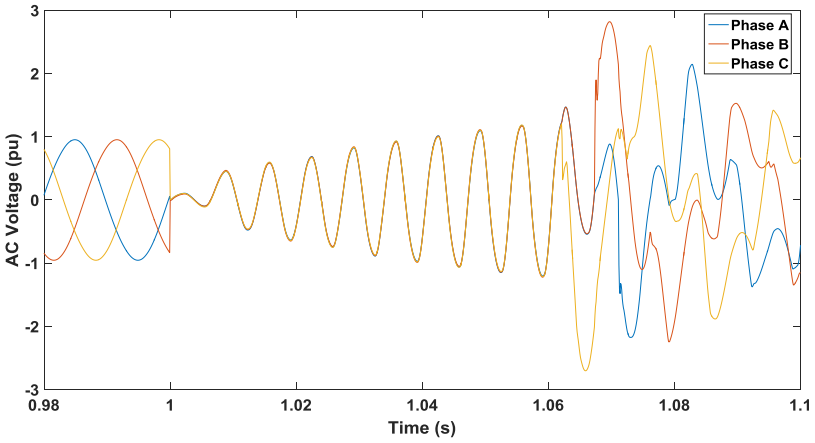


Figure 6.15 AC fault at MMC 2 (no extra control actions are performed). AC voltage at MMC 1 station.

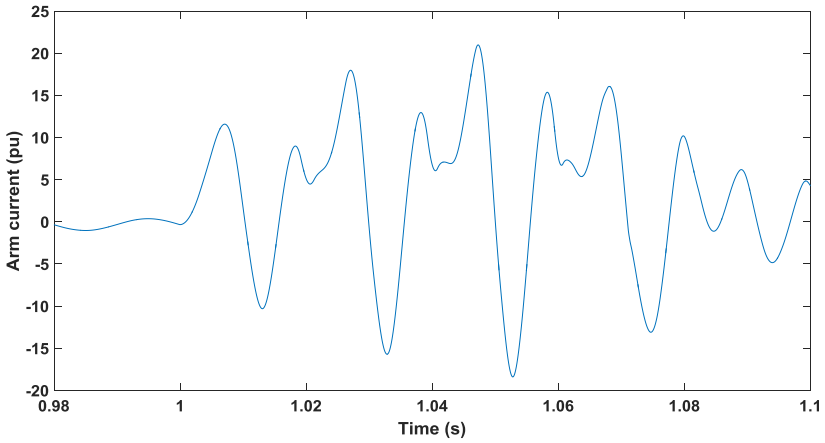


Figure 6.16 AC fault at MMC 2 (no extra control actions are performed). Upper arm current of phase A of MMC 1 station.

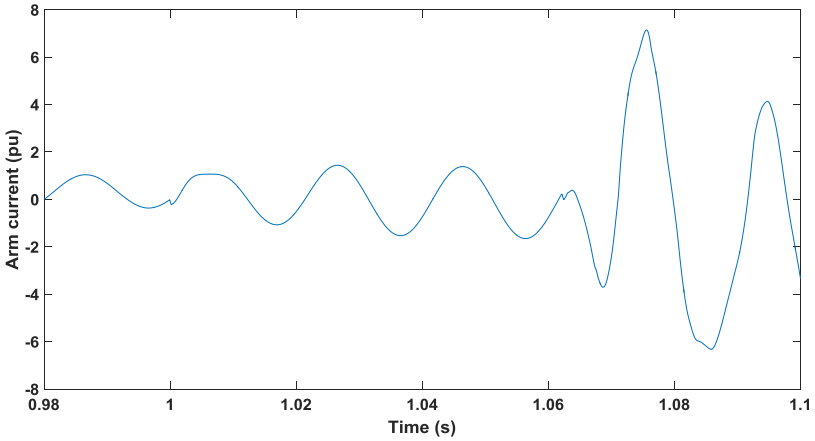


Figure 6.17 AC fault at MMC 2 (no extra control actions are performed). Upper arm current of phase A of MMC 3 station.

Given that the use of series inductors is not recommended, a control-based solution should be found. The traditional way to face faults which occur at the AC side of an MMC is to implement positive and negative sequence current controllers. After the detection of the fault, the controllers are activated and they can keep the AC voltage constant by injecting reactive power. However, in case of a fault within the DC hub, the objective is different and the voltage of the AC link should be kept as low as possible during the fault. Otherwise, the fault current will be very high (since the fault resistance is small) and the amplitude of the arm currents of the MMC which operates in AC voltage control mode will be unacceptable since its currents are not controlled. As a consequence, the MMC would be damaged since the IGBTs cannot withstand so high arm currents.

For this reason, the system should first be protected and then, the fault should be isolated. To protect the system in the time interval between the occurrence of the fault and the opening of the AC breaker of port 2, a control-based methodology will be used. To evaluate the operation of the system when an AC fault occurs at port 2, the modulation index of MMC 1 was set at 0.95pu and the active power references of ports 2 and 3 were set at 1pu. The sequence of the events and the necessary actions that should be taken after the occurrence of the fault are given below:

1. Three-phase fault occurs at the primary of the transformer of port 2 at t=1s.
2. The fault can be detected by current sensors which are connected to the arms of the MMCs. Once the arm current of any MMC exceeds its maximum acceptable value (1.1pu), the fault can be detected by the current sensors. In this case study, the fault is detected by the current sensor which is connected to the upper arm of phase A of MMC 1 station at t'=1.0023s (2.3ms after the occurrence of the fault).
3. The insertion indices n_u and n_l of MMCs 1 and 3 are set at 0.5 in the time interval between the detection and the isolation of the fault (1.0023s and 1.07s). The insertion indices n_u and n_l of MMC 2 are set at 0.5 after the detection of the fault (at t=1.0023s) and their value does not change since port 2 will be disconnected. By setting the insertion indices at 0.5 in the time interval between the detection and the isolation of the fault, the voltage of the AC link can be controlled at zero and the fault current will be significantly lower. In general, in the time interval between the detection and the isolation of the fault, the insertion indices of all the MMCs should have the same value. In this way, the operation of the DC hub is suppressed and the voltage of the AC link is controlled at zero. Ideally, the insertion indices should be set at zero. In this case, all the capacitors would be bypassed and protected by the arm overcurrents. Thus, each arm would consist of the arm inductance and the arm resistance. In this case, the impedance of each arm of the MMC would be very small and as a consequence, the DC voltage source which is used for the modelling of the HVDC line would be short-circuited. Thus, a higher value for the insertion indices should be selected. It was shown through simulations that the minimum value of the insertion indices which ensures satisfactory suppression of the DC hub is 0.5. As mentioned before, the AC breaker will open within 60 ms after the detection of the fault. Given that the fault is detected at t=1.0023s, the AC breaker will open at t'= 1.0623s. Right after the isolation of the fault, the control system of each converter is activated again (at t=1.07s) and the DC hub returns to normal operation.
4. The active power references of ports 2 and 3 are set at zero in the time interval between the detection and the isolation of the fault (1.0023s and 1.07s). It was shown through simulations that when the active power references of ports 2 and 3 are different than zero in the same time interval, the distortion of the active power waveforms of ports 1 and 3 is higher. For this reason, the active power references of ports 2 and 3 should be set at zero in the aforementioned time interval.
5. The AC breaker of port 2 opens at t''= 1.0623s (in the worst case scenario, 60ms after the detection of the fault).

As can be seen in Figure 6.18, the voltage of the AC link is controlled at zero in the time interval between 1.0023s and 1.07s. As a result, the fault current and the arm currents of the MMCs will be low. Figure 6.19 shows that the amplitude of the arm currents of MMC 1 is acceptable and it does not exceed the limit of 2pu (in contrast to the previous case where no extra control actions were performed). Figure 6.20 shows that the arm current of MMC 2 goes to zero after the occurrence of the fault since it is disconnected from the DC hub. Figure 6.21 shows that the amplitude of the arm currents of MMC 3 is kept within the acceptable limits in the same time interval ($\leq 2\ pu$). As shown in Figure 6.22, the active power of port 2 goes to zero after the occurrence of the fault since port 2 is disconnected from the DC hub. The active power of port 3 is controlled at 1pu during the normal operation of the system. However, in the time interval between 1.0023s and 1.07s, the active power of port 3 is controlled at zero. The active power of port 1 is controlled at 1pu before the occurrence of the fault since it is equal to the sum of the active power of ports 2 and 3. After the occurrence of the fault, in the time interval between 1.0023s and 1.07s, the active power of ports 2 and 3 goes to

zero, and thus, the active power of port 1 also goes to zero. After the isolation of the fault, the active power of port 1 is controlled at 0.5 pu since port 2 is disconnected from the DC hub and port 1 is only connected to port 3. Finally, as can be seen in Figure 6.23, the reactive power at the three ports is maintained at zero at all times.

According to the suggested control-based methodology, the operation of the DC hub is suppressed only for 70 ms and the system returns to normal operation and regains its full power transfer capability within 150 ms after the occurrence of the fault. Given that the mechanical AC breakers are slow and ideal AC breakers do not exist, the control-based methodology is a very good alternative for the protection of the system against AC faults.

It was proven through simulations that three-phase-to-ground faults are more dangerous than two-phase-to-ground faults. In case of a three-phase-to-ground fault, all the three phases of the AC link are grounded and thus, the transient phenomenon is more intense. Finally, it was proven through simulations that the higher the voltage of the AC link, the more dangerous the three-phase-to-ground fault will be. Considering that the fault resistance is constant, the higher the voltage of the AC link, the higher the fault current will be (due to the relation $I_F = V_f / R_f$).

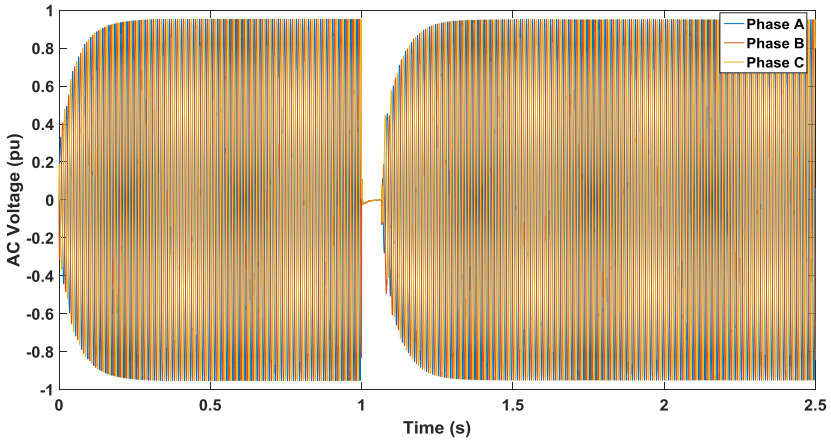


Figure 6.18 AC fault at MMC 2. AC Voltage at MMC 1 station.

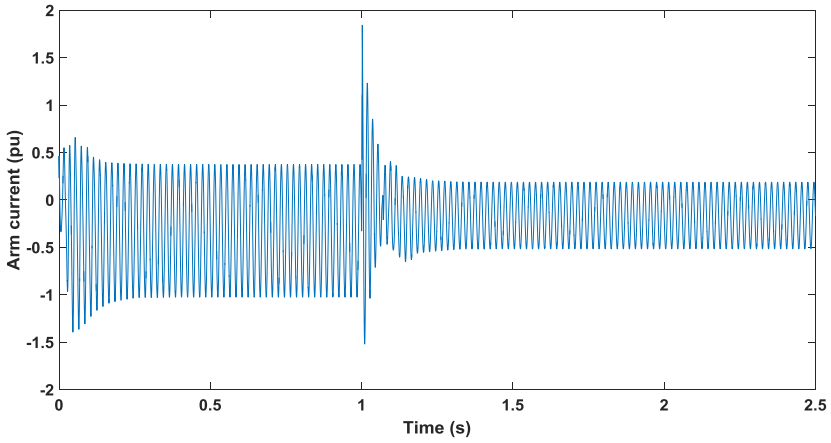


Figure 6.19 AC fault at MMC 2. Upper arm current of phase A of MMC 1 station.

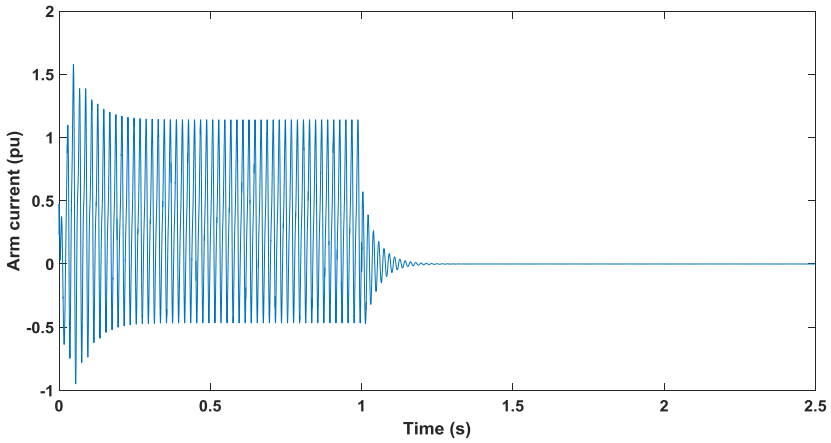


Figure 6.20 AC fault at MMC 2. Upper arm current of phase A of MMC 2 station.

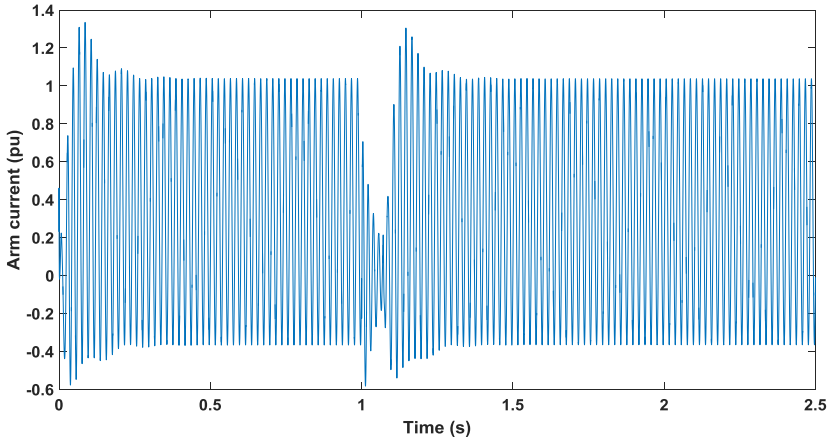


Figure 6.21 AC fault at MMC 2. Upper arm current of phase A of MMC 3 station.

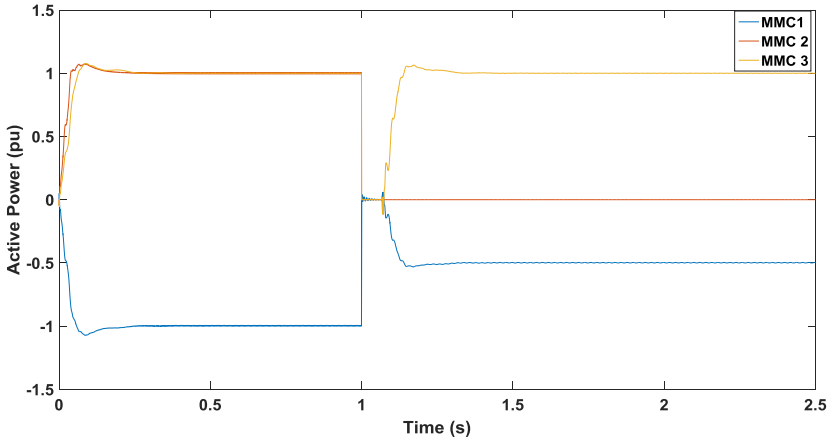


Figure 6.22 AC fault at MMC 2. Active Power at the three ports.

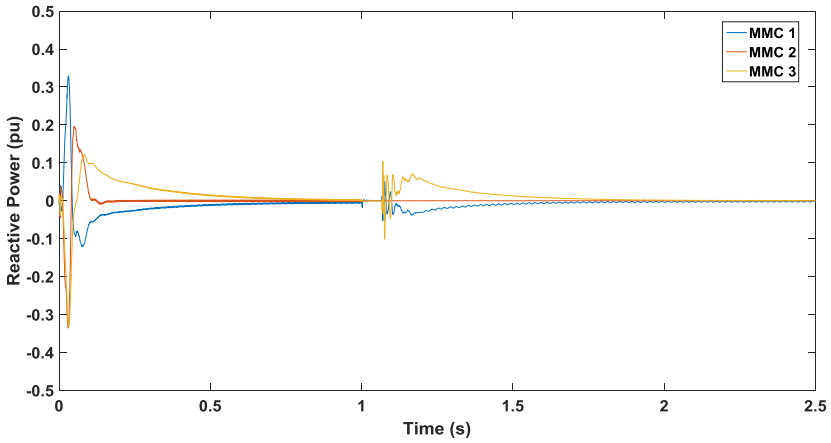


Figure 6.23 AC fault at MMC 2. Reactive Power at the three ports.

6.3 Methodology for clearing AC faults at the port controlling the voltage of the AC link

In this section, a methodology will be presented for the clearing of AC faults which occur at the port controlling the voltage of the AC link. As shown in Figure 6.24, a three-phase-to-ground fault occurs at port 1. After the isolation of the fault, the faulted port is disconnected from the DC hub and the port with the highest power rating should undertake the control of the voltage of the AC link (as explained in Chapter 5). To investigate the operation of the DC hub when a three-phase-to-ground fault occurs at port 1, three HVDC lines with characteristics as shown in Table 5.1 were interconnected. The modulation index was set at 0.95 pu and the active power references of ports 2 and 3 were set at 1 pu. Given that ports 2 and 3 have the same power rating, the port with the highest DC link voltage should undertake the control of the voltage of the AC link (as explained in Chapter 5). Thus, port 2 should undertake the control of the AC link voltage after the isolation of the fault. Port 3 will keep operating in active power control mode after the clearing of the fault.

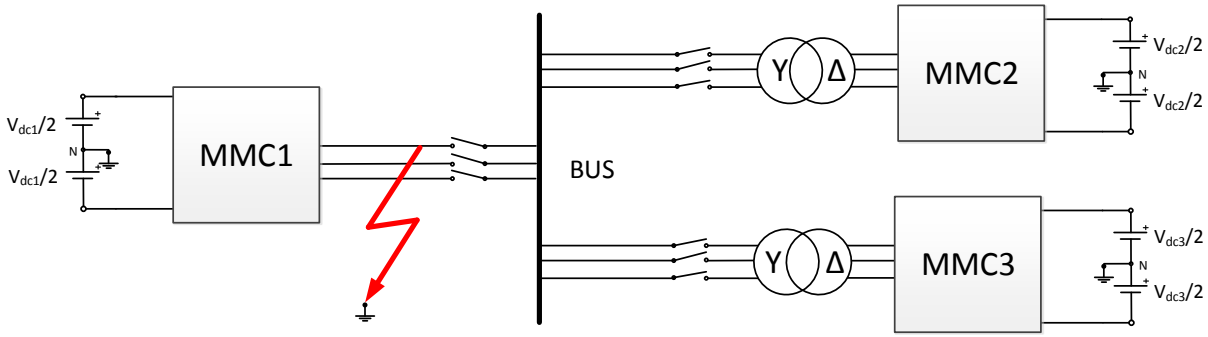


Figure 6.24 AC fault at MMC 1.

The sequence of the events and the necessary actions that should be taken after the occurrence of the fault are given below:

1. Three-phase fault occurs at port 1 at t=1s.
2. The fault can be detected by current sensors which are connected to the arms of the MMCs. Once the arm current of any MMC exceeds its maximum acceptable value (1.1pu), the fault can be detected by the current sensors. In this case study, the fault is detected by the current sensor which is connected to the upper arm of phase A of MMC 1 station at t'=1.0023s (2.3ms after the occurrence of the fault).
3. The insertion indices n_u and n_l of MMCs 2 and 3 are set at 0.5 in the time interval between the detection and the isolation of the fault (1.0023s and 1.07s). The insertion indices n_u and n_l of MMC 1 are set at 0.5 after the detection of the fault (at t=1.0023s) and their value does not change since port 1 will be disconnected. As mentioned before, the AC breaker will open within 60 ms after the detection of the fault. Given that the fault is detected at t=1.0023s, the AC breaker will open at t'= 1.0623s. Right after the isolation of the fault, the control system of each converter is activated again (at t=1.07s) and the DC hub returns to normal operation.
4. The active power references of ports 2 and 3 are set at zero in the time interval between the detection and the isolation of the fault (1.0023s and 1.07s).
5. The AC breaker of port 1 opens at t''= 1.0623s (in the worst case scenario, 60ms after the detection of the fault).
6. The control mode in which port 2 operates changes from active power to AC voltage control mode at t'''=1.07s.

Before the fault

Figure 6.25 shows that the voltage of the AC link is maintained at 0.95pu. As shown in Figure 6.26, the arm current is controlled at 1.1pu and its DC component is negative. Figure 6.27 shows that the arm current of MMC 2 is controlled at 1.1pu and its DC component is positive. The arm current of MMC 3 is also controlled at 1.1pu and its DC component is positive, as shown in Figure 6.28. As can be seen in Figure 6.29, the active power of ports 2 and 3 follows the references. Thus, the active power of ports 2, 3 is controlled at 1pu. The active power of port 1, which is equal to the sum of the active power of the other two ports, is controlled at -1pu. Finally, Figure 6.30 shows that the reactive power at the three ports is maintained at zero at all times.

During the fault

In the time interval between the detection and the isolation of the fault, the insertion indices of all the ports are set at 0.5. As a result, the voltage of the intermediate AC link is controlled at zero, as shown in Figure 6.25. In the time interval between the occurrence and the detection of the fault, the MMC 1 converter operates in AC voltage control mode and its currents are not controlled. For this reason, the peak of the upper arm current of phase A of MMC 1 is 1.8 pu, as shown in Figure 6.26. In the same time interval, the arm currents of MMC 2 and 3 are controlled and thus, they are kept within the specified limits, as shown in Figures 6.27 and 6.28. Given that after the detection of the fault, the insertion indices of all the ports are set at 0.5, the active power at the three ports is controlled at zero, as shown in Figure 6.29. Finally, Figure 6.30 shows that the reactive power at the three ports is maintained at zero in the same time interval.

After the fault

After the isolation of the fault and the disconnection of port 1, the control system of MMCs 2 and 3 is activated again and the DC hub returns to normal operation. Port 2, having the highest DC link voltage, undertakes the control of the voltage of the AC link. As shown in Figure 6.25, the voltage of the AC link is maintained at 0.95pu. As can be seen in Figure 6.26, the arm current of MMC 1 goes to zero, since port 1 is disconnected from the DC hub. As shown in Figure 6.27, the arm current of MMC 2 is -1.1pu and its DC component is now negative since port 2 is only connected to port 3 and the power flow through port 2 changes direction. As shown in Figure 6.28, the arm current of MMC 3 is again controlled at 1.1pu and its DC component is positive. The active power of port 1 goes to zero since it is disconnected from the DC hub, as shown in Figure 6.29. The active power of port 3 is again controlled at 1pu and the active power of port 2 is now controlled at -1pu since it undertakes the control of the voltage of the AC link and it is only connected to port 3. Finally, Figure 6.30 shows that the reactive power at the three ports is maintained at zero at all times.

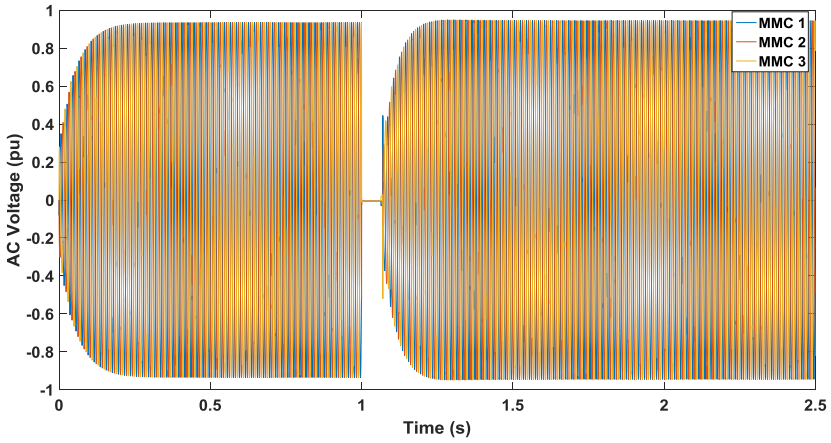


Figure 6.25 AC fault at MMC 1. AC Voltage at MMC 2 station.

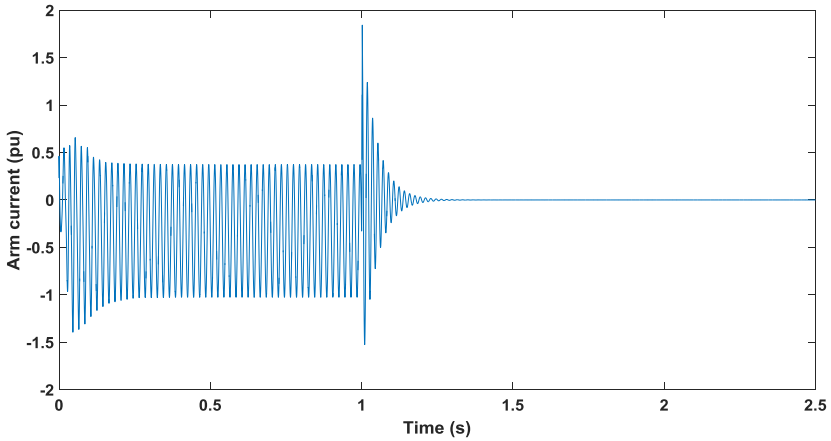


Figure 6.26 AC fault at MMC 1. Upper arm current of phase A of MMC 1 station.

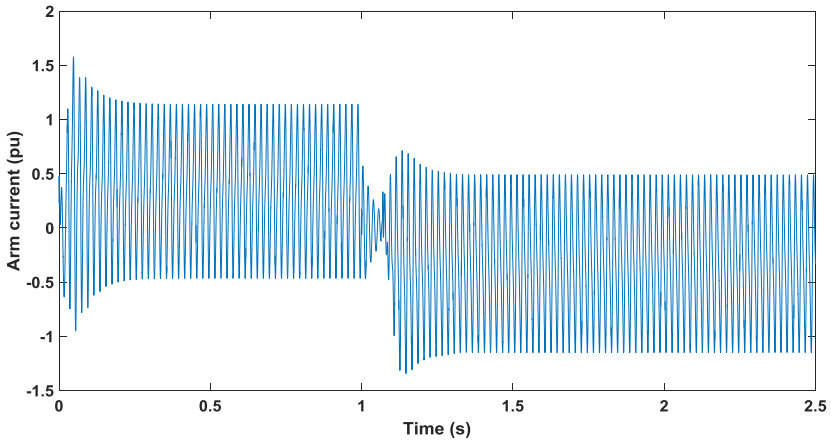


Figure 6.27 AC fault at MMC 1. Upper arm current of phase A of MMC 2 station.

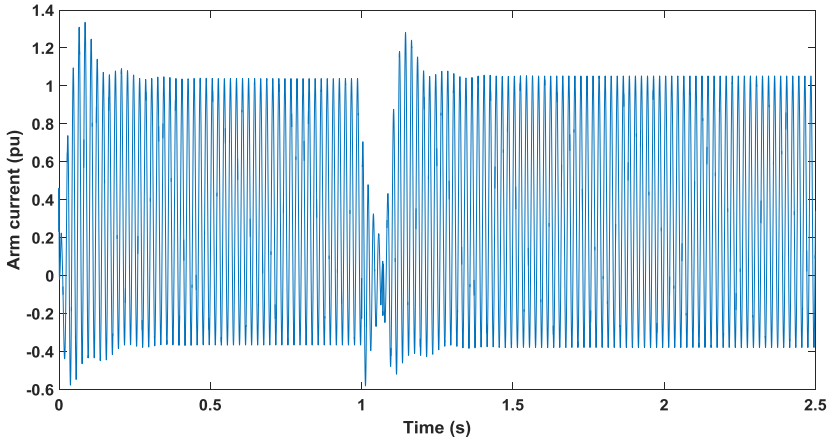


Figure 6.28 AC fault at MMC 1. Upper arm current of phase A of MMC 3 station.

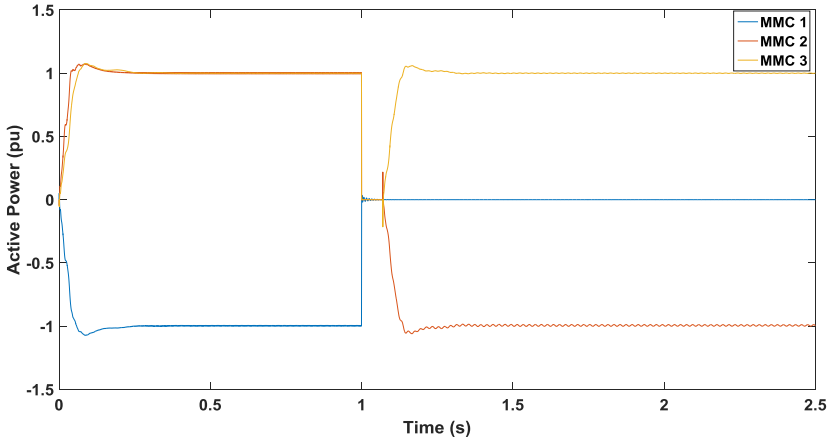


Figure 6.29 AC fault at MMC 1. Active power at the three ports.

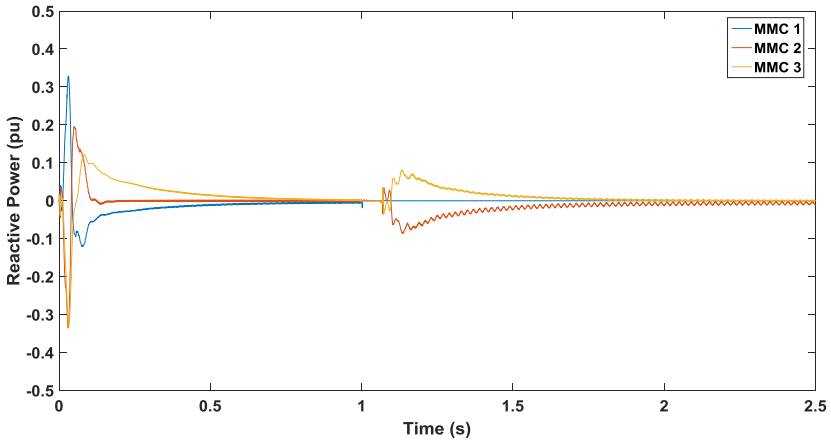


Figure 6.30 AC fault at MMC 1. Reactive power at the three ports.

6.4 Expandability of the DC Hub

In this section, the expandability of the DC hub will be investigated. The main target of the DC hub is the interconnection of multiple HVDC lines operating at different voltage levels and with different DC grid configurations. Any additional HVDC line should be easily connected or disconnected from the DC hub without affecting the operation of the others. To evaluate the expandability of the DC hub, four HVDC lines were interconnected as shown in Figure 6.31. The characteristics of the MMCs are given in Table 6.1. Initially, the DC hub interconnects HVDC lines 1, 2 and 3 and then, HVDC line 4 is inserted. In case the rated power of port 4 is higher than the rated power of the other ports, port 4 should undertake the control of the voltage of the AC link. In fact, the port operating in AC voltage control mode should have the highest power rating since its active power is equal to the sum of the active power of the other ports. Otherwise, in case the rated power of the inserted port is not the highest, port 1, having the highest power rating, will keep operating in AC voltage control mode. In this case, the active power that is transferred through port 1 will be equal to the sum of the active power of the other ports ($P_1=P_2+P_3+P_4$). In case after the insertion of port 4, the active power of port 1 exceeds its rated value, the active power references of ports 2, 3 and 4 should be lowered such that port 1 works within its specified limits. This design limitation should always be taken into account. Otherwise, the MMC converter of the port controlling the AC link voltage (MMC 1) could be damaged.

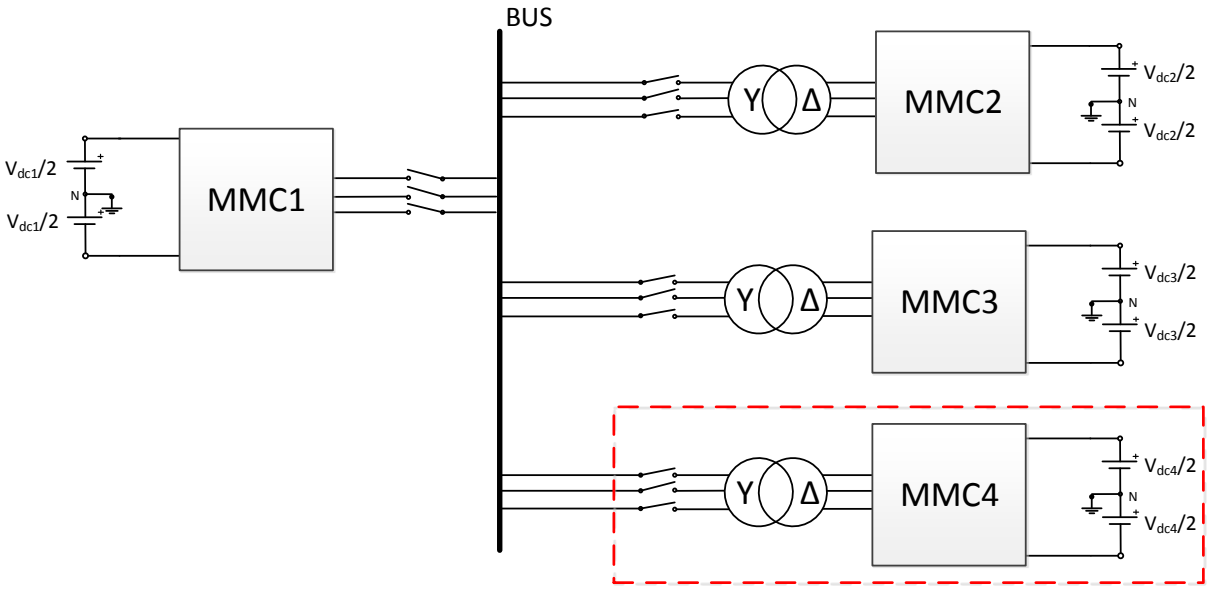


Figure 6.31 Insertion of a fourth port.

To evaluate the operation of the DC hub when an additional port is inserted, the modulation index was set at 0.95. The additional port 4 is inserted at t=1s. Before the insertion of port 4, the active power references of ports 2 and 3 are set at 1 pu and the active power of port 1 is equal to the sum of the active power of the other ports (1 pu). After the insertion of port 4, the active power references of ports 2 and 3 are lowered such that the active power of port 1 does not exceed its rated value. The characteristics of the interconnected MMCs can be seen in Table 6.1 and the case study timeline is shown in Table 6.2.

Specifications	MMC 1	MMC 2	MMC 3	MMC 4
V_{dc} (KV)	600	500	120	450
S_{rated} (GVA)	1.2	0.6	0.6	0.6

Table 6.1 Insertion of a fourth port. MMC specifications.

Time (s)	0	1
MMC 2 p_{ac}^* (pu)	1	0.7
MMC 3 p_{ac}^* (pu)	1	0.7
MMC 4 p_{ac}^* (pu)	-	0.6

Table 6.2 Insertion of a fourth port. Case study timeline.

Figure 6.32 shows that the voltage of the AC link is maintained at 0.95 pu. At the instant of the insertion, the active power of port 4 is zero and the AC voltage of MMC 4 is synchronized with the voltage of the AC link. As a result, the insertion of port 4 is smooth and the amplitude of the arm currents of MMC 4 is kept within its specified limits, as shown in Figure 6.33. Before the insertion of port 4, the active power of ports 2 and 3 is controlled at 1 pu and the active power of port 1, which is equal to the sum of the active power of ports 2 and 3, is controlled at -1pu, as shown in Figure 6.34 ($P_1=P_2+P_3=$ 1·0.6 GVA+1·0.6 GVA=1.2 GVA=1pu). After the insertion of port 4, the active power references of ports 2, 3 and 4 should be lowered such that the active power of port 1 does not exceed its rated value. As shown in Figure 6.34, the active power of ports 2, 3 and 4 is controlled at 0.7, 0.7 and 0.6 pu respectively. As a result, the active power of port 1 is again controlled at -1pu ($P_1=P_2+P_3+P_4$=0.7·0.6 GVA+0.7·0.6 GVA+0.6·0.6 GVA=1.2 GVA=1pu). Finally, as can be seen in Figure 6.35, the reactive power at the three ports is maintained at zero at all times.

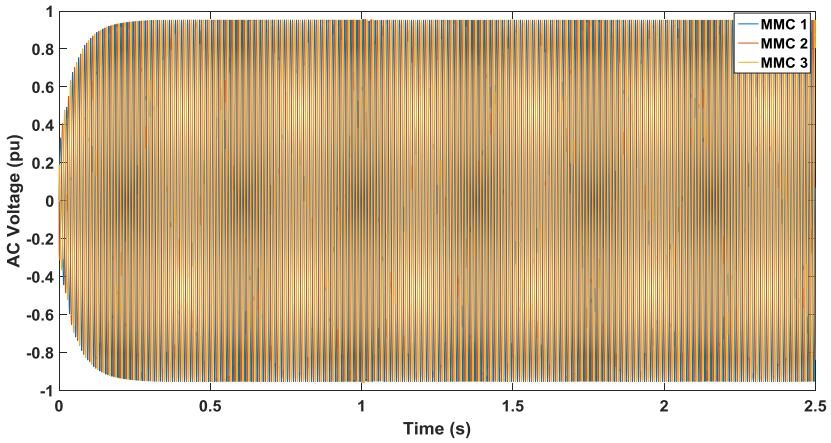


Figure 6.32 Insertion of a fourth port. AC Voltage at MMC 1 station.

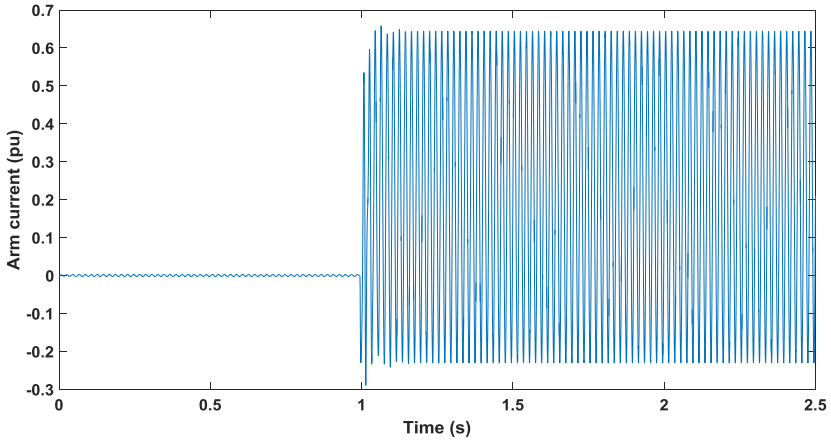


Figure 6.33 Insertion of a fourth port. Upper arm current of phase A of MMC 4 station.

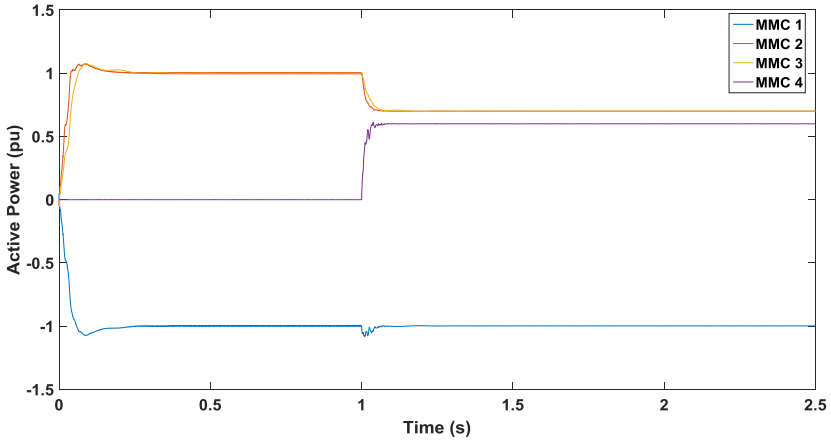


Figure 6.34 Insertion of a fourth port. Active Power at the three ports.

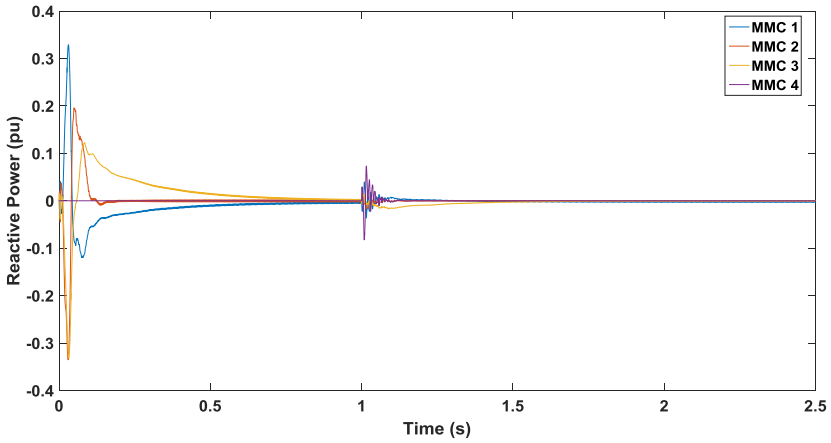


Figure 6.35 Insertion of a fourth port. Reactive Power at the three ports.

6.5 Conclusion

In this chapter, a methodology was presented for the connection or disconnection of additional ports from the DC hub. It was shown that any additional port can easily connect or disconnect from the DC hub without affecting the operation of the others. Moreover, a methodology was presented for the clearing of AC faults within the DC hub. Once the fault is detected by current sensors which are connected to the arms of the MMC converters, the operation of the system is suppressed. As a result, the amplitude of the arm currents of the port operating in AC voltage control mode does not exceed its maximum acceptable value and the system is protected. Then, the AC breaker of the faulted port opens. It was shown through simulations that within 150 ms after the occurrence of the fault, the system returns to normal operation and regains its full power transfer capability. In case of AC fault at the port controlling the voltage of the AC link, the faulted port disconnects from the DC hub and the port with the highest rated power should undertake the control of the voltage of the AC link. However, in case of fault at the common AC bus, the AC circuit breakers of all the ports should open and the operation of the DC hub must be interrupted. Finally, the expandability of the DC hub was investigated. It was proven that the DC hub can be easily expanded to include multiple ports. In case the inserted port has the highest rated power, it should undertake the control of the voltage of the AC link. Otherwise, the inserted port should operate in active power or in DC voltage control mode. In any case, the active power of the port controlling the AC voltage is determined by the sum of the active power of the other ports. For this reason, in case after the insertion of the additional port, the active power of the port controlling the AC voltage exceeds its rated value, the active power references of the other ports should change such that the port controlling the AC voltage operates within its specified limits.

7.Case Study 3: Connection of a load or a wind farm to the AC side of the DC Hub

In this chapter, the operation of the DC hub will be investigated when a load or a wind farm is connected to its inner AC circuit. In case the DC hub is used for the interconnection of multiple offshore HVDC cables, a nearby offshore wind farm or the loads of the offshore platform could be directly connected to the AC side of the DC hub.

7.1 Load connected to the AC side of the DC hub

In this section, the operation of the DC hub will be investigated when a load is connected to its AC side. The load should connect to the AC bus of the DC hub through a transformer because the rated voltage of the load is much lower than the operating voltage of the AC link. Given that most of the industrial loads are inductive, the load will be simulated using a three-phase RL load. Figure 7.1 shows the topology of a three-port DC hub including a three-phase load. In case an inductive load is connected to the AC link of the DC hub, the reactive power which is absorbed by the load will be provided by the MMC controlling the AC voltage because the reactive power at the other two ports is controlled at zero. In this case, the MMC controlling the voltage of the AC link will be underutilized since its power transfer capability will be reduced. For this reason, parallel capacitors should connect to the load to provide the reactive power which is absorbed by the load. In this manner, the reactive power at each port can be controlled at zero and the power transfer capability of the DC hub will be the highest possible.

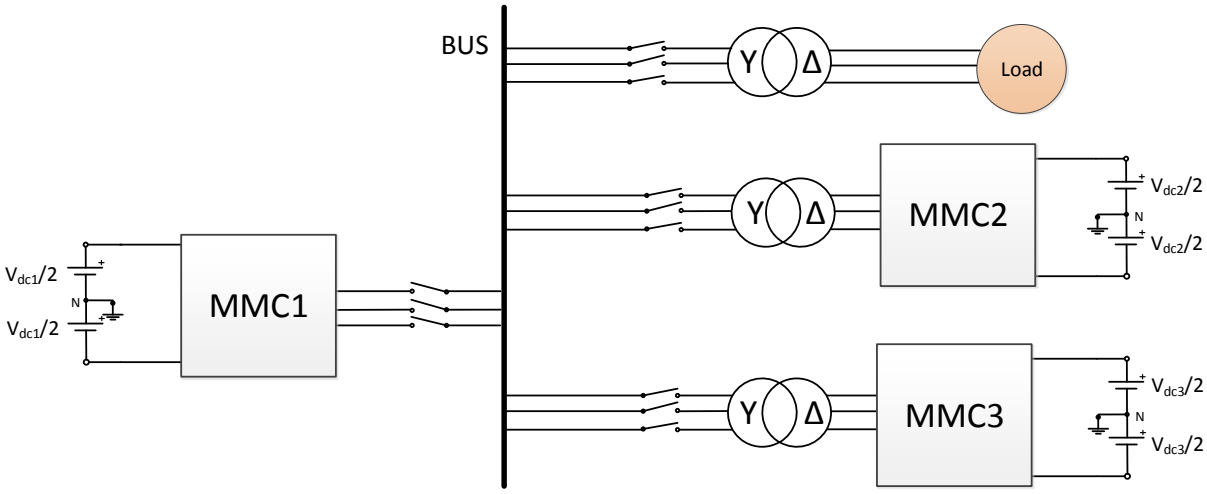


Figure 7.1 Connection of a load to the AC bus of the DC Hub.

To evaluate the operation of the DC hub when a load is connected to its AC bus, three HVDC lines and a three-phase RL load were interconnected as shown in Figure 7.1. The rated DC voltage of ports 1, 2 and 3 is 600, 500 and 120 kV respectively and the rated voltage of the load is 25 kV. The rated power of the ports and the load is given in Table 7.1.

Power Base	MMC 1	MMC 2	MMC 3	Load
S_{rated} (GVA)	**1.2**	**0.6**	**0.6**	**0.24**

Table 7.1 Rated power of MMCs and Load.

To evaluate the operation of the DC hub, the modulation index was set at 0.95 pu, the active power references of ports 2 and 3 were set at -0.8 pu and steps were performed on the active power which is consumed by the load. The sequence of the events is shown in Table 7.2.

Time (s)	**0**	**1**
MMC 2 $p_{ac}{}^{*}$ **(pu)**	-0.8	-0.8
MMC 3 $p_{ac}{}^{*}$ **(pu)**	-0.8	-0.8
Load $p_{ac}{}^{*}$ **(pu)**	-0.5	-1

Table 7.2 Load connected to the DC hub. Case study timeline.

In Figure 7.2 it can be seen that MMC 1 maintains the AC link voltage at 0.95pu at all times. As shown in Figure 7.3, the active power of MMC 1 is equal to the sum of the active power of MMC 2, MMC 3 and the load. In the time interval between 0 and 1s, MMC 1 provides active power 0.9 pu which is transferred to MMC 2, MMC 3 and the load. More specifically, MMC 2 absorbs active power 0.8 pu, MMC 3 absorbs active power 0.8 pu and the load absorbs active power 0.5 pu. In the time interval between 1 and 2s, the active power which is provided by MMC 1 increases because the load also increases from 0.5pu to 1pu. As can be seen in Figure 7.3, MMC 1 transfers active power 1pu to the other MMCs and the load. More specifically, MMC 2 absorbs active power 0.8 pu, MMC 3 absorbs active power 0.8 pu and the load consumes active power 1 pu. Finally, as can be seen in Figure 7.4, the reactive power at the three ports and the load is kept at zero at all times. As a result, the power transfer capability of each port is the highest possible.

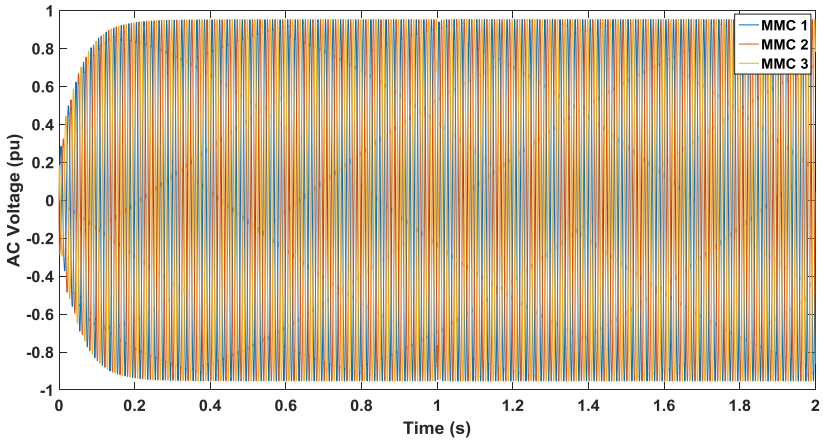


Figure 7.2 Load connected to the DC hub. AC voltage at MMC 1 station.

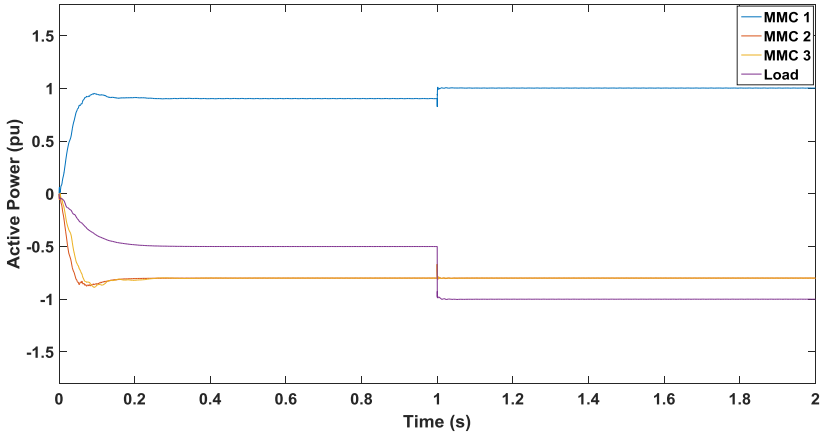


Figure 7.3 Load connected to the DC hub. Active power of the MMCs and the load.

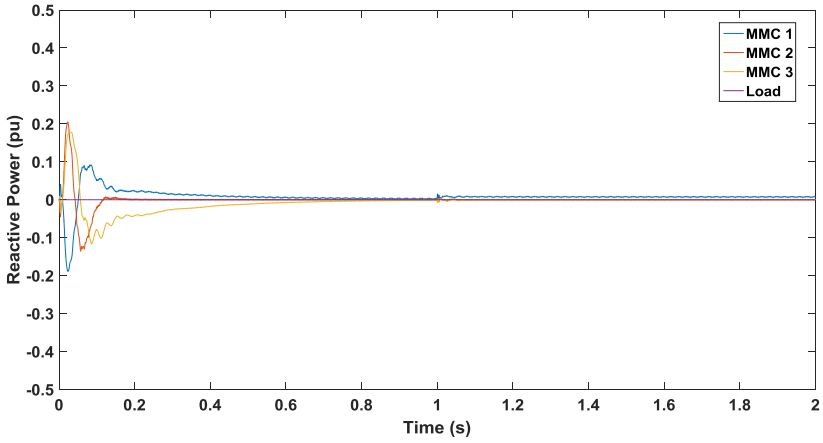


Figure 7.4 Load connected to the DC hub. Reactive power of the MMCs and the load.

7.2 Wind farm connected to the AC side of the DC hub

In this section, the operation of the DC hub will be investigated when a wind farm is connected to its AC bus. The DC hub could be used for the interconnection of multiple offshore HVDC cables. In case an offshore wind farm is close to the location of the DC hub, it could directly connect to the AC link of the DC hub. In this manner, the use of costly offshore cables for the connection of the wind farm to the onshore grid would not be necessary. As can be seen in Figure 7.5, the wind farm is connected to the AC link of the DC hub through transformers, because the operating voltage of the wind generators (Doubly Fed Induction Generator-DFIG) is much lower than the voltage level of the AC link. Moreover, it is assumed that the distance between the wind farm and the DC hub is 30 km.

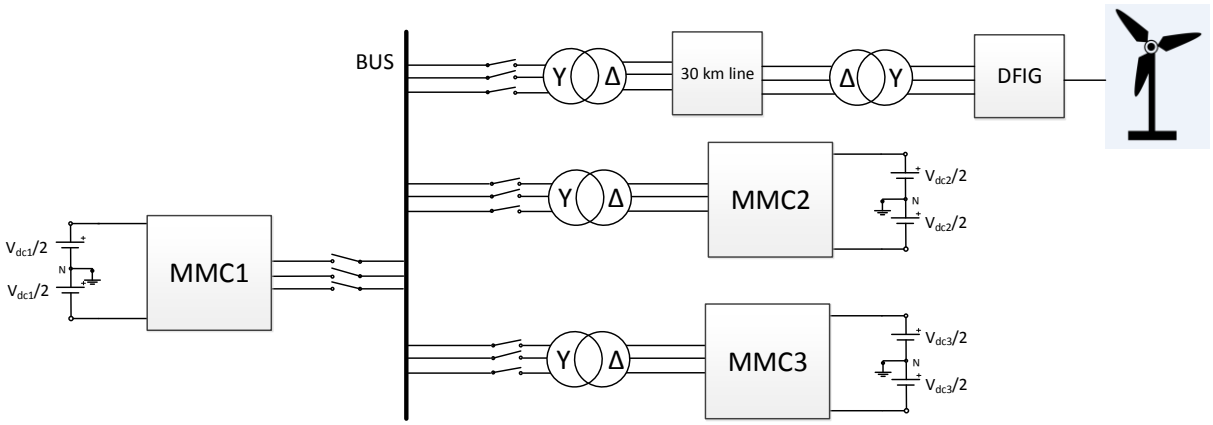


Figure 7.5 Connection of a wind farm to the AC bus of the DC hub.

To evaluate the operation of the DC hub when a wind farm is connected to its AC link, three HVDC lines were interconnected as shown in Figure 7.5. The DC voltage levels of ports 1, 2 and 3 are 600, 500 and 120 kV respectively. MMC 1 works in AC voltage control mode and MMCs 2 and 3 work in active power control mode. The rated power of the ports and the wind farm is given in Table 7.3.

Power Base	MMC 1	MMC 2	MMC 3	Wind farm
S_{rated} (MVA)	**50**	**25**	**25**	**9**

Table 7.3 Rated power of MMCs and Wind farm.

To evaluate the power flow control performance of the investigated DC hub, the AC voltage was controlled at 0.95 pu. The active power references of ports 2 and 3 were set at 0.8 pu and steps were performed on the active power of the wind farm (on the wind speed). The sequence of the events is shown in Table 7.4.

Time (s)	**0**	**10**
MMC 2 $p_{ac}{}^{*}$ **(pu)**	0.8	0.8
MMC 3 $p_{ac}{}^{*}$ **(pu)**	0.8	0.8
Wind farm $p_{ac}{}^{*}$ **(pu)**	1	0.55
Wind speed (m/s)	15	10

Table 7.4 Wind farm connected to the DC hub. Case study timeline.

Figure 7.6 shows that MMC 1 maintains the AC link voltage at 0.95 pu at all times. The active power of MMC 1 is always equal to the sum of the active power of MMC 2, MMC 3 and the wind farm. For this reason, the active power of MMC 1 is negative and the active power of the other two MMCs and the wind farm is positive, as shown in Figure 7.7. As can be seen in Figure 7.7, in the time interval between 0 and 10s, the active power of ports 2 and 3 is controlled at +0.8 pu and the active power of the wind farm is controlled at +1pu. The active power of port 1 can be expressed as $P_1=P_2+P_3+P_w$, where P_1, P_2 and P_3 represent the active power of ports 1, 2 and 3 respectively and P_w represents the active power of the wind farm. Thus, the active power of port 1 can be computed as

$$P_1 = 0.8 \cdot 25MW + 0.8 \cdot 25MW + 9MW = 49\ MW$$

For this reason, in the time interval between 0 and 10s, the active power of port 1 is controlled at -0.98pu. As can be seen in Figure 7.7, at t=10s, the active power of the wind farm drops from 1pu to 0.55pu. Therefore, in the time interval between 10 and 20s, the active power of ports 2 and 3 is again controlled at +0.8pu and the active power of the wind farm is controlled at +0.55pu. The active power of port 1 can now be calculated as

$$P_1 = 0.8 \cdot 25MW + 0.8 \cdot 25MW + 5MW = 45\ MW$$

For this reason, in the time interval between 10 and 20s, the active power of port 1 drops to -0.9pu. Finally, Figure 7.8 shows that the reactive power at the three ports and the wind farm is maintained at zero at all times. Therefore, the efficiency and the power transfer capability of the DC hub are the highest possible.

The active power of the port controlling the voltage of the AC link (port 1) is always equal to the sum of the active power of the other two ports and the wind farm (P_1=P_2+P_3+P_w). In case after the insertion of the wind farm, the active power of port 1 exceeds its maximum acceptable value (1pu), the active power references of the other two ports should be lowered such that port 1 operates within its acceptable limits. This design limitation should always be taken into account. Otherwise, the MMC controlling the voltage of the AC link (MMC 1) could be damaged.

In case a wind farm is connected to the AC side of the DC hub and an AC fault occurs within the DC hub, the wind farm should remain connected and thus, the voltage of the AC link should be maintained close to its rated value. As a result, the operation of the DC hub should not be suppressed as suggested in Chapter 6. In case of AC fault within the DC hub, the MMC converter controlling the voltage of the AC link (MMC 1) should be equipped with positive and negative sequence current controllers to inject reactive power during the fault and to keep the AC link voltage as high as possible. In case the AC link voltage is maintained high during the fault, the fault current will be high since the fault resistance is very small ($I_F = V_f / R_f$). Since the currents of the MMC controlling the AC link voltage are not controlled (MMC 1), its arm currents will exceed its maximum acceptable limit (2pu) and the converter will be damaged, as explained in Chapter 6. For this reason, series inductors should be connected to each port of the DC hub to limit the contribution of each MMC converter to the fault current and to maintain the arm currents of each MMC within the specified limits. Parallel capacitors should also be connected to each port to provide the reactive power which is absorbed by the series inductors. In this way, the power transfer capability of each MMC will be the highest possible.

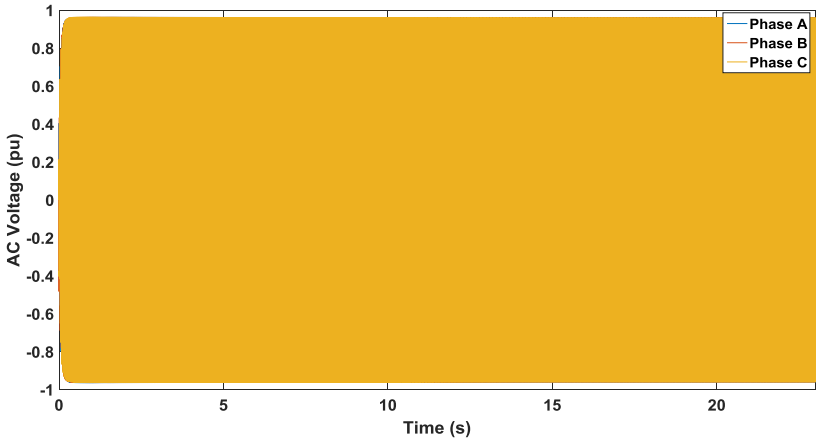


Figure 7.6 Wind farm connected to the DC hub. AC voltage at MMC 1 station.

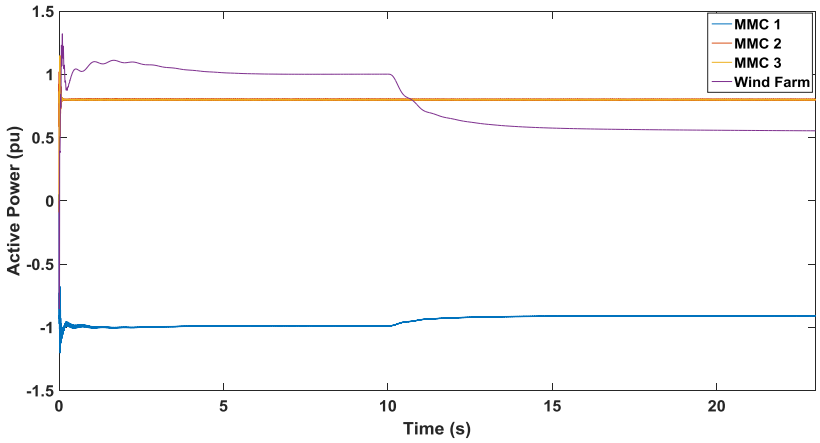


Figure 7.7 Wind farm connected to the DC hub. Active power of the MMCs and the load.

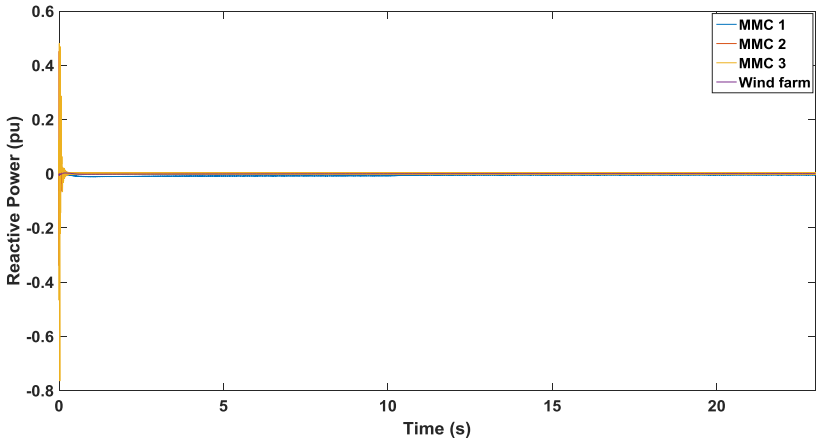


Figure 7.8 Wind farm connected to the DC hub. Reactive power of the MMCs and the load.

7.3 Conclusion

In this chapter, the operation of the DC hub was investigated when a load or a wind farm was connected to its AC link. It was shown through simulations that the DC hub can continue its normal operation when steps are performed on the active power of the generation or consumption units. Thus, the DC hub could be used not only for the interconnection of multiple HVDC lines but also for the interconnection of HVDC lines with generation and consumption units. In case the DC hub is used for the interconnection of multiple offshore HVDC links, the loads of the offshore platform could be directly supplied by the AC link of the DC hub. In this way, the use of extra generation units for the supply of the loads of the platform would not be necessary. Moreover, a nearby offshore wind farm could be directly connected to the AC link of the DC hub. In this manner, the use of costly offshore cables for the connection of the wind farm to the onshore grid would be avoided and thus, the cost of the wind farm installation would be significantly reduced.

8.Conclusion-Future work

Conclusion

In this project, several DC hub topologies which can be used for the interconnection of multiple HVDC lines operating at different voltage levels and with different DC link configurations were investigated. Given that the use of the MMC converter is recommended for high power and high voltage applications, the MMC-based DC-DC converter is the most suitable DC-DC converter type which could be used as the building block of the DC hub. The operating principles, the control strategies and the modulation techniques of the MMC converter were analytically presented in Chapter 3. The averaged model (ALA model) and the control structures of the MMC which were implemented in *Matlab/Simulink* were presented in Chapter 4. As described in Chapter 4, each port could operate in AC voltage, in DC voltage or in active power control mode. In a three-port DC hub topology, one port should undertake the control of the voltage of the AC link and the other two ports could operate either in DC voltage or in active power control mode. When a port operates in DC voltage or in active power control mode, its AC currents can be controlled. In a three port DC hub topology, the current of the port controlling the voltage of the AC link is equal to the sum of the currents of the other two ports. Given that the currents of the other two ports are controlled, the current of the port controlling the AC link voltage will be determined by the sum of the currents of the other two ports and thus, it cannot be controlled. As a result, in case an AC fault occurs within the DC hub, appropriate actions should be taken for the protection of the port controlling the voltage of the AC link. Otherwise, the arm currents of this port will exceed their maximum acceptable value and the system could be damaged.

Research Question 1: Which is the most appropriate design for the inner AC circuit of the DC hub?

In Chapter 5, several DC hub topologies were suggested for the interconnection of multiple HVDC lines operating at different voltage levels. In case the voltage levels of the interconnected HVDC lines are different, the DC hub topology using transformers is the most suitable one, since each MMC operates close to its rated characteristics and the efficiency and the power transfer capability of the system are the highest possible. However, the use of transformers increases the total investment cost and volume of the system. The HVDC lines could also be interconnected without using transformers. They could be interconnected using LCL filters or directly. In case the HVDC lines are interconnected without transformers and the voltage levels of the lines are much different, the efficiency and the power transfer capability of the system will be significantly lower. However, in case the DC lines are interconnected without transformers and the voltage levels of the lines are similar, the efficiency and the power transfer capability of the system will be high. In case the DC lines are interconnected without transformers and enhanced protection against faults is necessary, the DC hub topology using LCL filters is the most suitable one. On the downside, the use of filters increases the total cost and volume of the system, and thus, the L and C components of the filters should be as small as possible. Depending on the voltage levels of the interconnected lines, the system requirements, the available budget and the application (onshore or offshore), it is up to the system designer to select the most appropriate DC hub topology and to optimize the operation of the system. Given that the main target of the DC hub is the interconnection of multiple HVDC lines operating at different voltage levels, the DC hub topology using transformers is the most suitable one. For this reason, this topology was used in the case studies of Chapters 6 and 7.

Research Question 2: How does the connection/disconnection of a port affect the normal operation and stability of the system?

In Chapter 6, a methodology was presented for the safe connection or disconnection of ports from the DC hub. It was shown through simulations that any port can easily connect or disconnect from the DC hub without affecting the operation of the other ports.

Research Question 3: How do AC faults within the DC hub affect the normal operation and stability of the system?

In Chapter 6, a methodology was presented for the clearing of AC faults which occur within the DC hub. As described in Chapter 6, in the time interval between the detection and the isolation of the fault, the operation of the DC hub should be suppressed and the voltage of the AC link should be controlled at zero. In this manner, the amplitude of the arm currents of the port controlling the voltage of the AC bus does not exceed its maximum acceptable limit and the system is protected. It was shown through simulations that the operation of the DC hub is suppressed only for 70 ms and the system returns to normal operation and regains its full power transfer capability within 150 ms after the occurrence of the fault. Finally, in case an AC fault occurs at the port controlling the voltage of the AC bus, the faulted port should disconnect from the DC hub and the port with the highest rated power should undertake the control of the voltage of the AC link.

Research Question 4: How could the DC hub be expanded to allow the interconnection of multiple ports?

In Chapter 6, the expandability of the DC hub was also investigated. It was shown through simulations that the DC hub can be easily expanded to include multiple ports. In case the rated power of the inserted port is higher than the rated power of the other ports, the inserted port should undertake the control of the voltage of the AC link. Otherwise, the inserted port could operate in active power or in DC voltage control mode. In any case, the active power of the port controlling the voltage of the AC bus will be determined by the sum of the active power of the other ports. For this reason, in case after the insertion of the additional port, the active power of the port controlling the AC link voltage exceeds its maximum acceptable limit, the active power references of the other ports should be lowered such that the active power of the port controlling the AC link voltage is maintained within its specified limits. This design limitation should always be taken into consideration. Otherwise, the port operating in AC voltage control mode will be overloaded.

Research Question 5: Could generation or consumption units be connected to the inner AC circuit of the DC hub?

In Chapter 7, the operation of the DC hub was investigated when a load or a wind farm was connected to its AC link. It was shown through simulations that the DC hub can continue its normal operation when steps are performed on the active power of the generation or consumption units. Thus, the DC hub could be used not only for the interconnection of HVDC lines but also for the interconnection of HVDC lines with generation and consumption units. In case the DC hub is used for the interconnection of offshore HVDC cables, the loads of the offshore platform or a nearby wind

farm could directly connect to its AC link. In this way, extra generation units for the supply of the loads of the offshore platform would not be necessary and the use of expensive offshore cables for the connection of the wind farm to the onshore grid would be avoided.

Future work

In a three-port DC hub topology, one port should undertake the control of the voltage of the AC bus and the other two ports could operate either in active power or in DC voltage control mode. As described in Chapter 4, the currents of the ports operating in active power or in DC voltage control mode can be controlled. The current of the port operating in AC voltage control mode is determined by the sum of the currents of the other two ports and thus, it cannot be controlled. As a consequence, in case an AC fault occurs within the DC hub, the arm currents of the port controlling the voltage of the AC link will exceed their maximum acceptable limit, whereas the arm currents of the ports operating in active power or DC voltage control mode can be maintained within their specified limits (since they are controlled). For this reason, in the time interval between the detection and the isolation of the fault, the operation of the DC hub should be suppressed and the voltage of the AC link should be controlled at zero. Otherwise, the MMC controlling the voltage of the AC link could be damaged. If the currents of the port operating in AC voltage control mode could also be controlled, the operation of the DC hub should not be suppressed and the DC hub could continue its operation in the time interval between the occurrence and the isolation of the fault. In case enhanced protection against faults was desired, LCL filters could be connected to each port to limit the fault currents and to maintain the arm overcurrents of the MMC converters within their specified limits. Thus, as future work, another structure for the AC voltage controller of the MMC converter could be suggested, in which the currents of the MMC should be controlled. Moreover, a methodology could be suggested for the clearing of AC faults within the DC hub without suppressing its operation in the time interval between the detection and the isolation of the fault.

Moreover, the operation of the DC hub under the occurrence of DC faults at any of its ports could also be investigated. In case a DC fault occurs at one of the ports, the IGBTs of the MMC of this port should be blocked. In this way, the fault current will pass through the anti-parallel diodes and the IGBTs will be protected. Given that DC faults could occur at any port of the DC hub, a different methodology for the clearing of DC faults at any of the ports could be suggested, depending on the control mode in which the faulted port operates.

Finally, the operation of the DC hub could be investigated when AC faults occur within the DC hub and a wind farm is connected to its AC bus. In general, in case a wind farm is connected to the AC side of an MMC converter and an AC fault occurs, the AC voltage should be maintained close to its rated value and the wind farm should remain connected to the MMC. In this case, the MMC converter should inject reactive power to keep its AC voltage as high as possible. As described in Chapter 6, in case an AC fault occurs within the DC hub, the voltage of the AC link should be controlled at zero and the operation of the DC hub should be suppressed. In this manner, the fault current will be reduced (since the voltage of the AC link is reduced) and the arm currents of the MMC controlling the voltage of the AC link will be maintained within the acceptable limits. As a result, in case a wind farm is connected to the DC hub, it should immediately disconnect from it since the voltage of the AC link is controlled at zero. Thus, a methodology could be suggested for the clearing of AC faults within the DC hub when a wind farm is connected to it. During the fault, the operation of the DC hub should not be suppressed, the voltage of the AC link should be maintained high and the wind farm should remain connected to the DC hub.

Appendix A: Simulink model

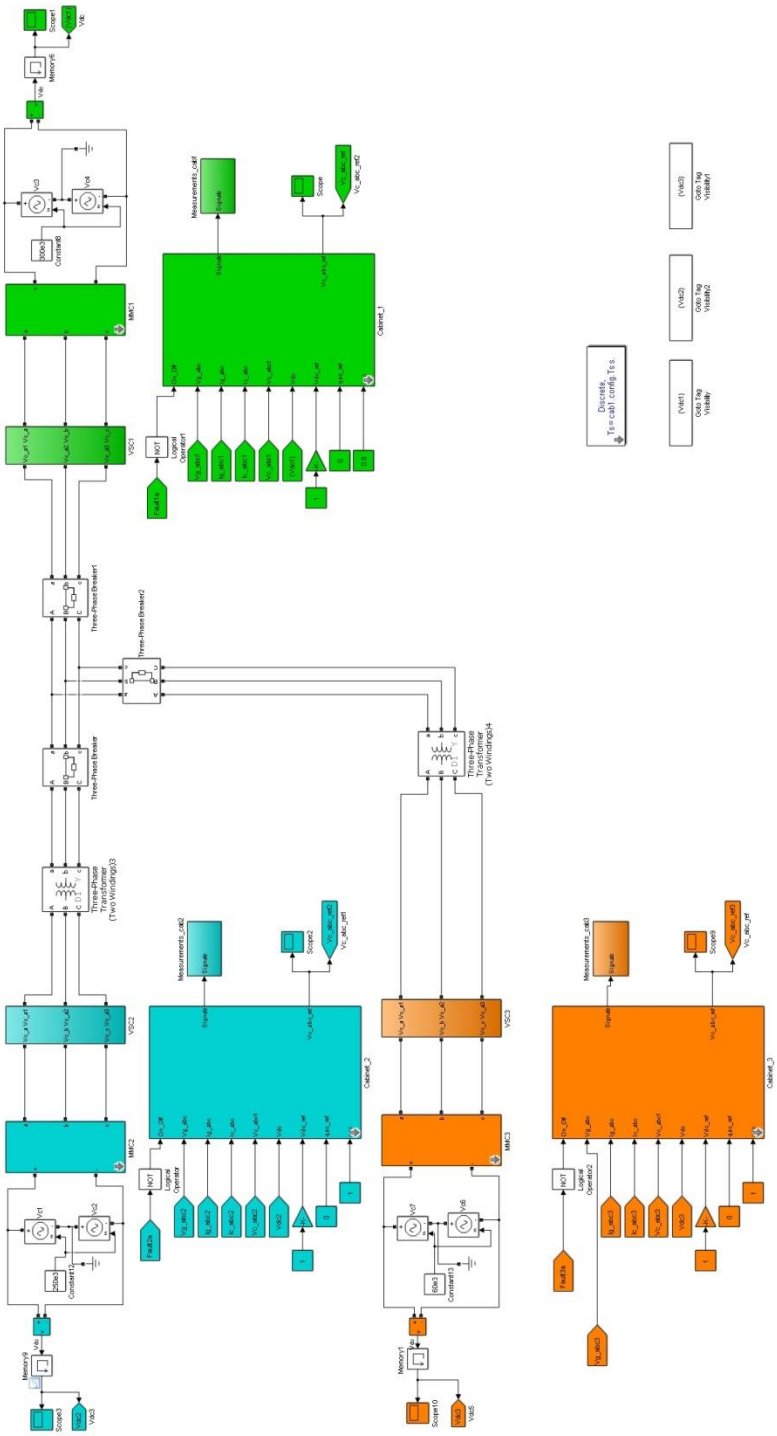


Figure A.1 Simulink model. Three-port DC Hub using transformers.

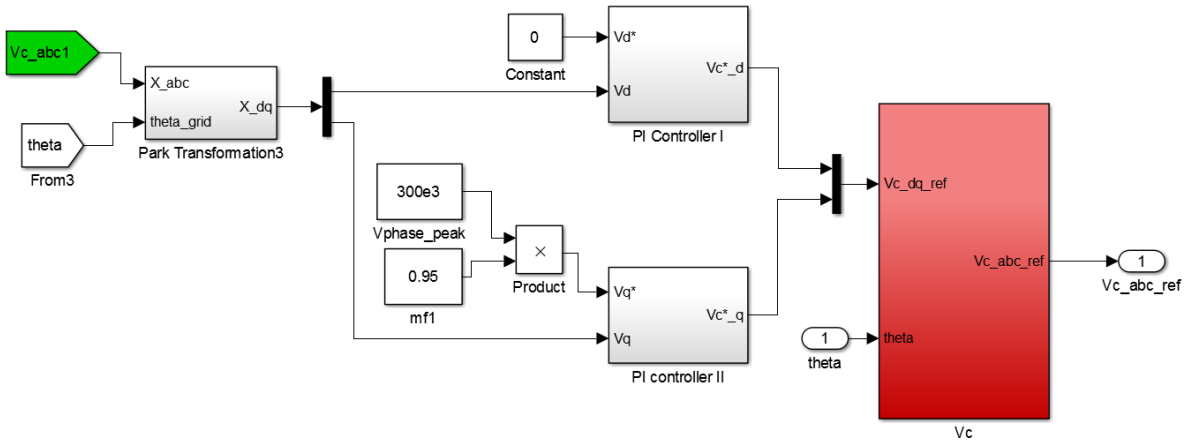


Figure A.2 Simulink model. AC voltage controller.

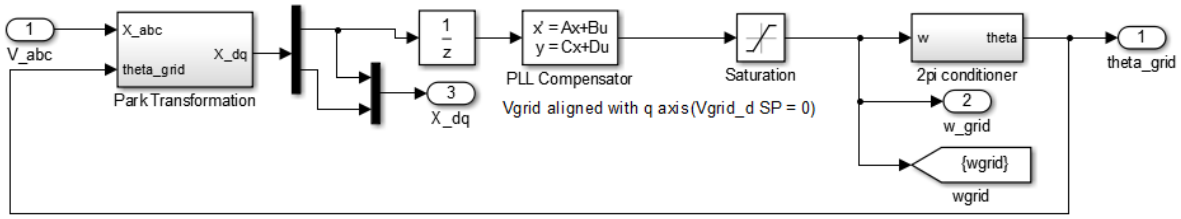


Figure A.3 Simulink model. Phase Locked Loop (PLL).

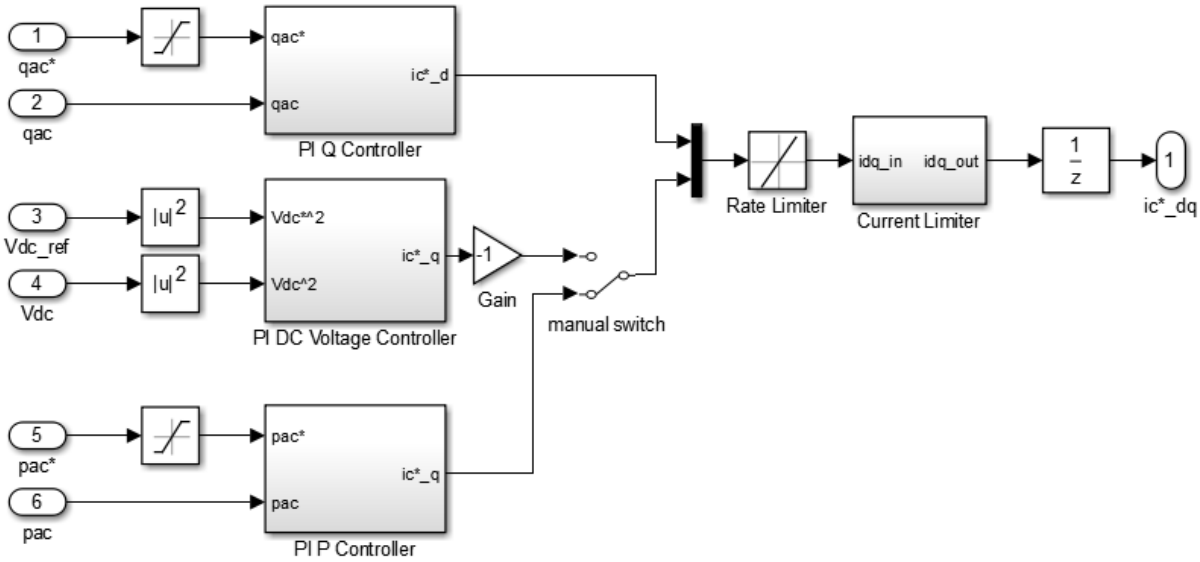
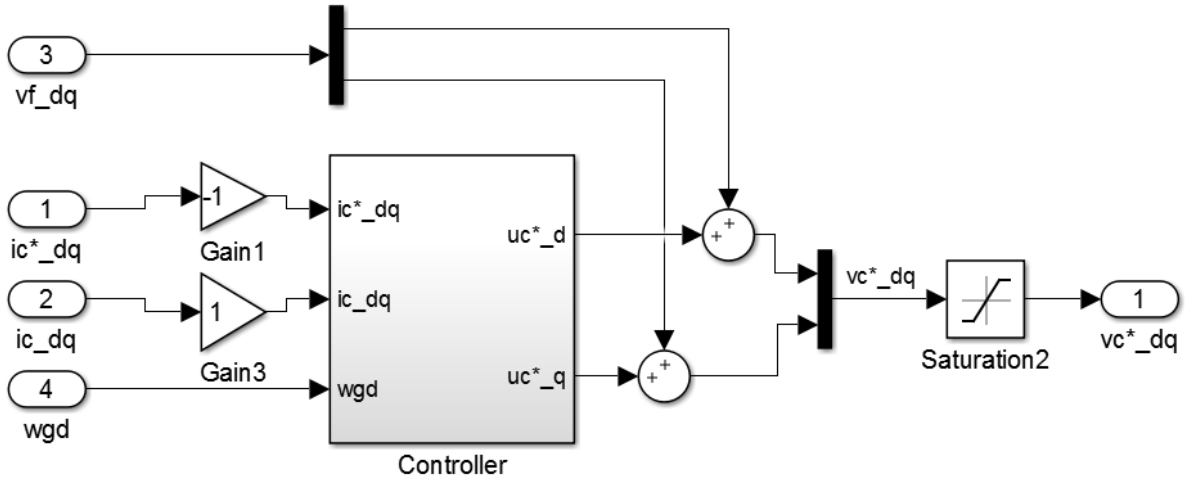
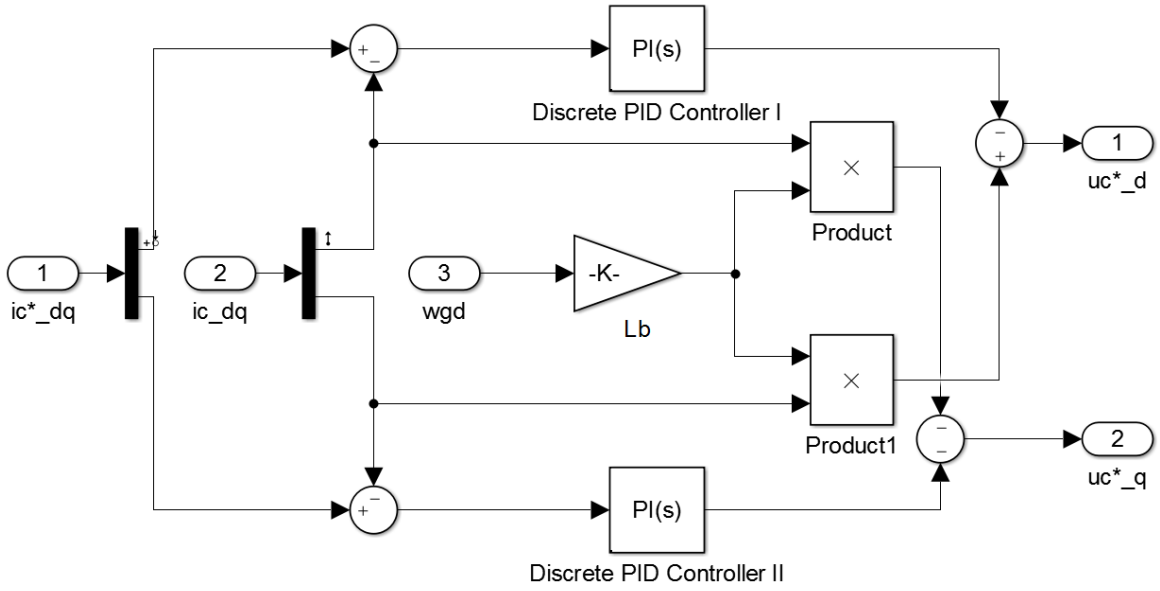


Figure A.4 Simulink model. Active/Reactive power and DC voltage controllers.

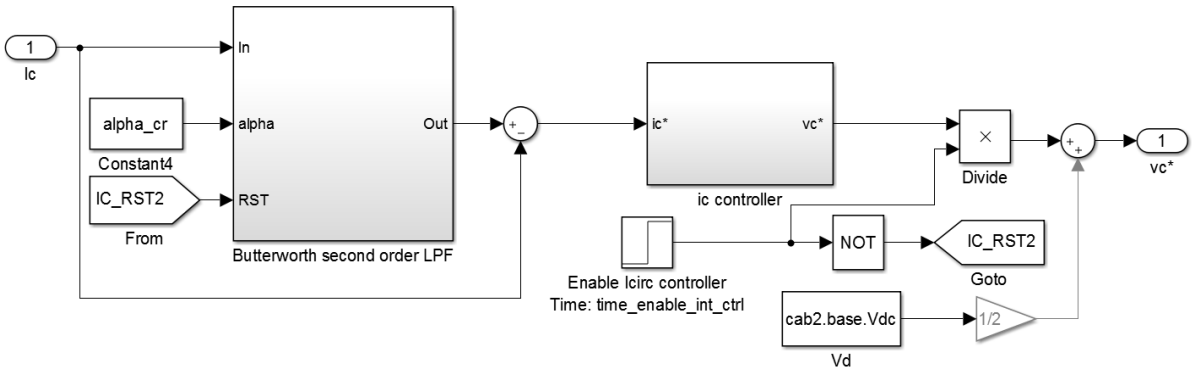


(a)

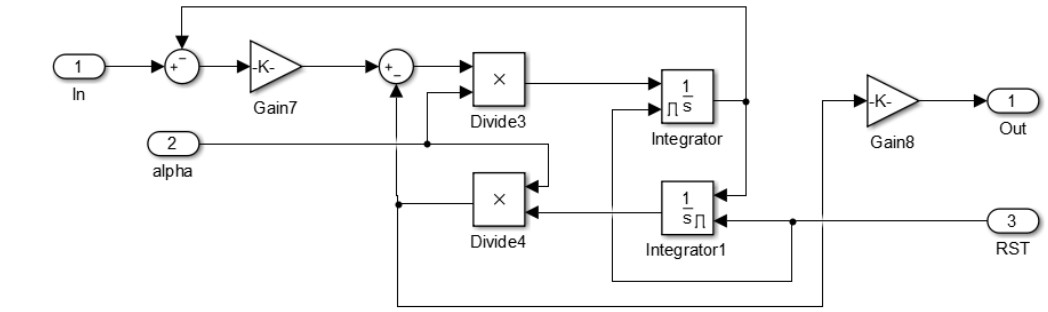


(b)

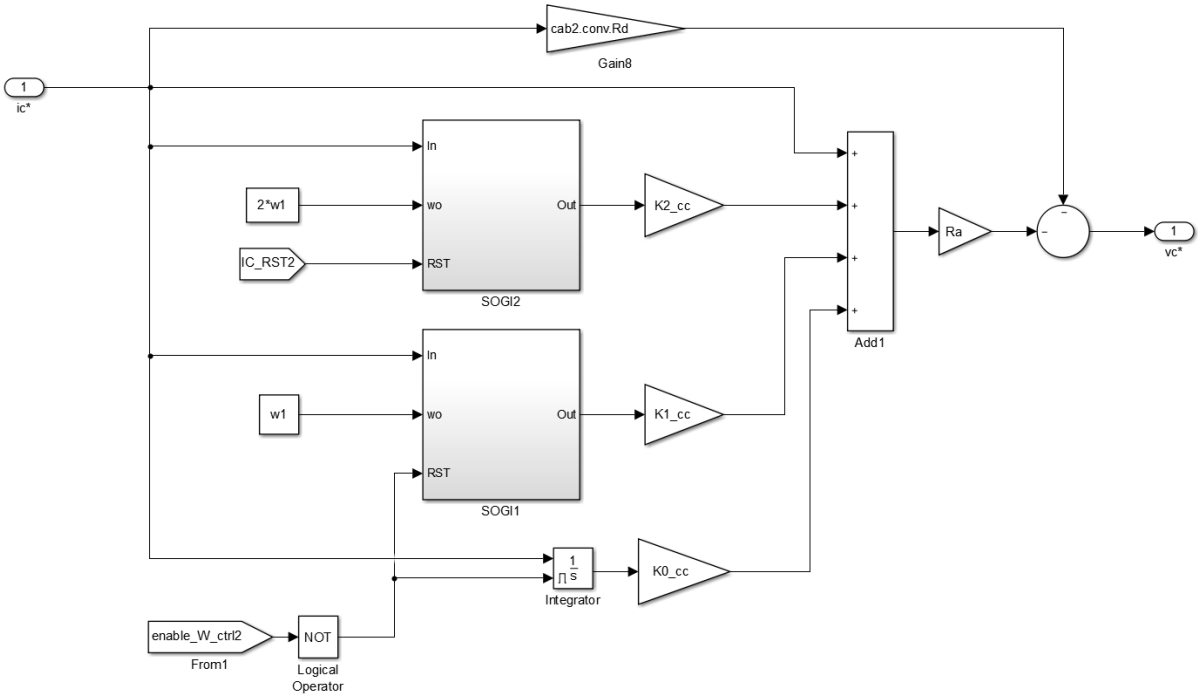
Figure A.5 Simulink model. Inner Current Controller (a) control diagram (b) analytical diagram of Controller's block.



(a)



(b)



(c)

Figure A.6 Simulink model. (a) Circulating Current Controller (b) Butterworth filter (c) i_c controller.

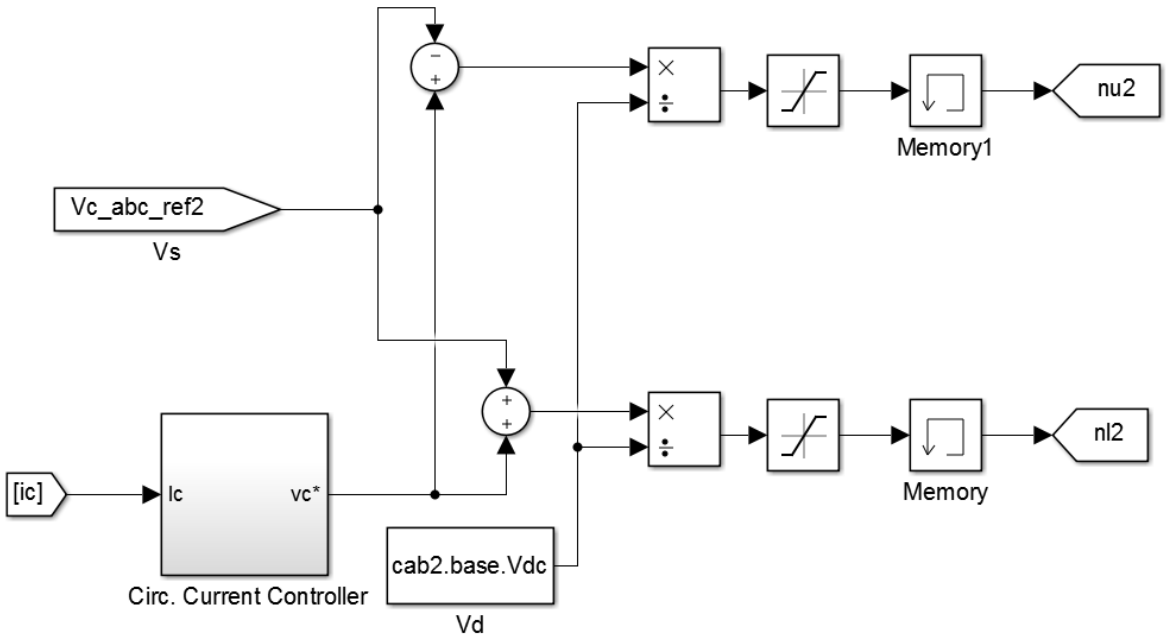


Figure A.7 Simulink model. Internal MMC control.

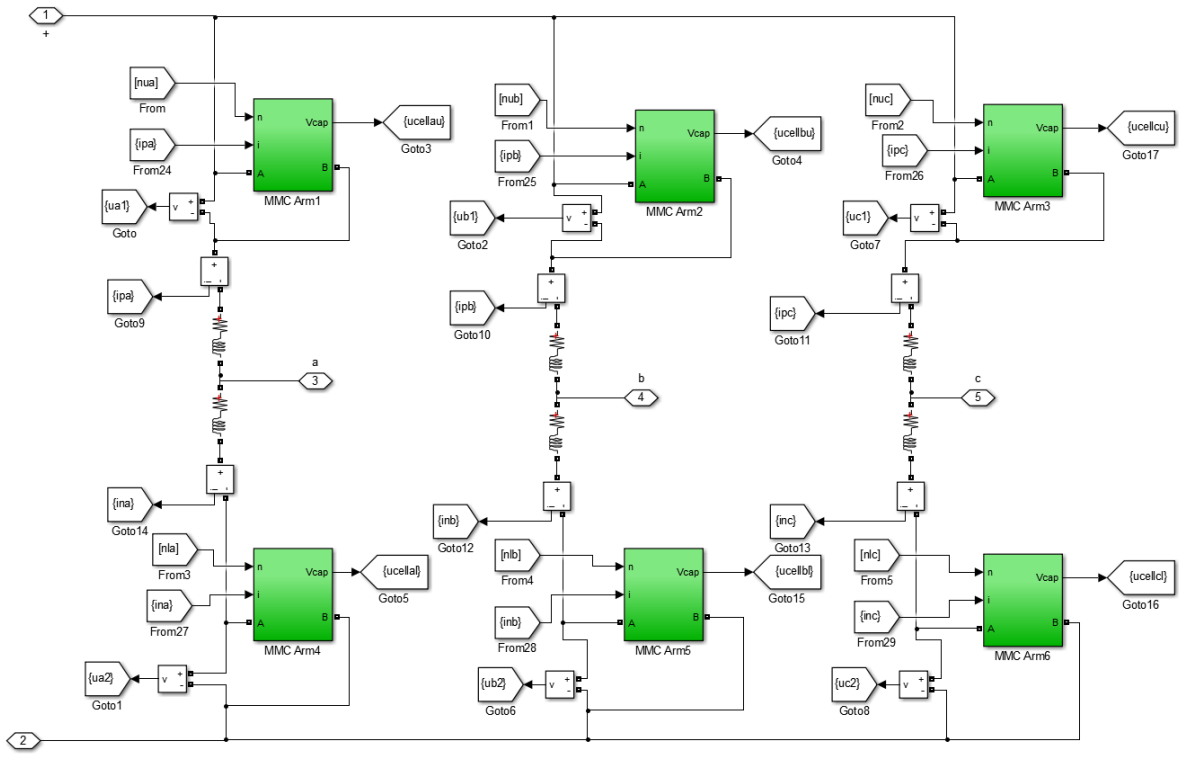


Figure A.8 Simulink model. MMC model.

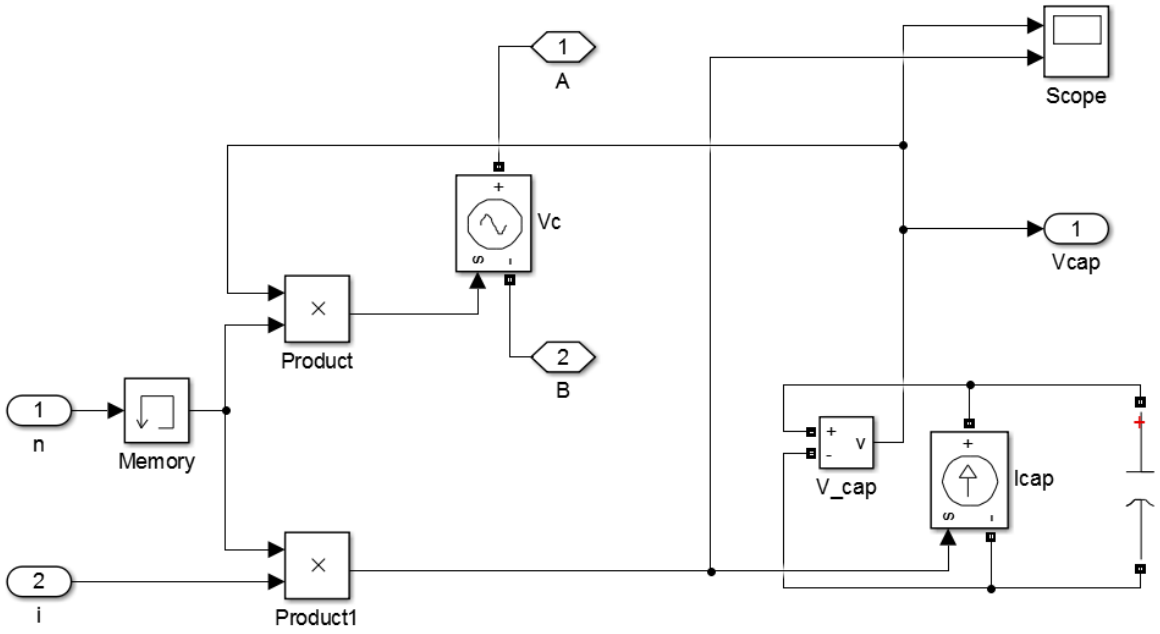


Figure A.9 Simulink model. ALA arm model.

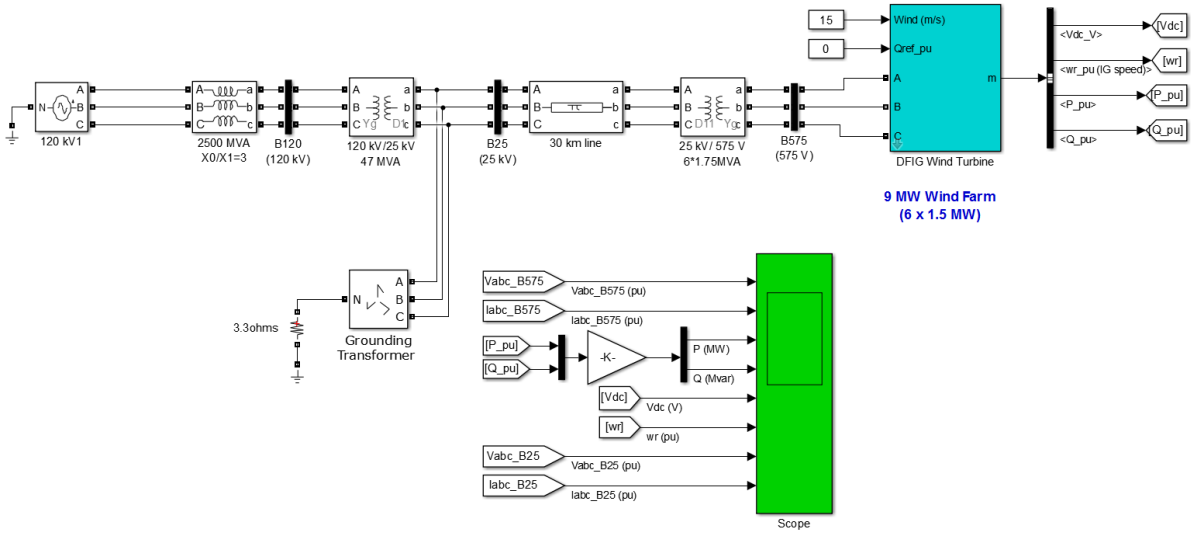


Figure A.10 Simulink model. Wind Farm model.

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