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Pimenta, Matheus; Gürleyük, Çağri ; Walsh, Paul; O'Keeffe, Daniel ; Babaie, Masoud ; Makinwa, Kofi A.A.

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A 200-μW Interface for High-Resolution Eddy-Current Displacement Sensors

Matheus Pimenta, *Member, IEEE*, Çağri Gürleyük, *Student Member, IEEE*, Paul Walsh, Daniel O'Keeffe, Masoud Babaie, *Member, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article presents a low-power eddy-current sensor interface for touch applications. It is based on a bang-bang digital phase-locked loop (DPLL) that converts the displacement of a metal target into digital information. The PLL consists of a digitally controlled oscillator (DCO) built around a sensing coil and a capacitive DAC, a comparator-based bang-bang phase/frequency detector (PFD), and a digital loop filter (DLF). The PLL locks the DCO to a reference frequency, making its digital input a direct representation of the sensing coil inductance. To compensate for the coil inductance tolerances, the DCO's center frequency can be trimmed by a second capacitive DAC. This approach obviates the need for a reference coil. When combined with a 5-mm-diameter sensing coil located 500 μm from a metal target, the interface achieves a displacement resolution of 6.7 nm (rms) in a 3-kHz bandwidth. It consumes 200 μW from a 1.8-V power supply, which represents the best-reported tradeoff between power consumption, bandwidth, and resolution.**

***Index Terms*— Digitally controlled oscillator (DCO), displacement, eddy-current sensor interface, low power, phase-locked loop (PLL).**

I. Introduction

TOUCH over metal (ToM) is a technology found in consumer products, such as smartwatches, cellphones, and car panels that allow buttons and sliders to be realized on existing metal surfaces [1]. It works by translating the touch-induced displacement of such surfaces into digital information. This enables the realization of robust buttons, with no moving parts, for weather-resistant products. However, high-resolution displacement sensors are required to detect the micrometer-level displacements associated with a touch. Furthermore, depending on the application, the touched surface may be made of different metals, with different thicknesses and distances from the sensor, and so these sensors must also be able to deal with such variability [2]–[4].

Eddy current (EC) displacement sensors are well suited for ToM applications. Compared with capacitive sensors, their insensitivity to dirt and moisture and their inherent galvanic isolation make them safer and more robust. In addition, when implemented with grounded metal targets, EC sensors can provide excellent immunity to electromagnetic interference.

EC sensors with high resolution have been reported in the past [5]–[8]. These designs typically employ two coils, a sensing coil, and a matched reference coil, which are part of an *LC* oscillator. The oscillation amplitude is then a function of target displacement. This differential sensing scheme cancels the large sensor offset caused by the non-zero standoff distance between the coil and the metal target. Due to their use of wide-bandwidth analog front ends, however, they typically consume tens of milliwatts, making them unsuitable for use in battery-powered products. Furthermore, the need for a reference coil makes them too bulky and expensive for use in mobile applications, where physical space is at a premium.

In contrast, the EC sensor interface in [3] does not require a reference coil. The sensing coil is still part of an *LC* oscillator, but now the oscillation frequency, rather than the oscillation amplitude, is digitized. When paired with a 5-mm-diameter sensing coil, this design dissipates 3.4 mW and achieves about 100-nm resolution in a 1-kHz noise bandwidth, at the target distances of about 500 μm. It draws an average current of 6 μA when operated at 6 samples/s.

In this work, the sensing *LC* oscillator is embedded in a bang-bang digital phase-locked loop PLL (DPLL), which directly digitizes its oscillation frequency. To compensate for coil inductance tolerances, a capacitive DAC is used to trim the oscillator's resonant frequency, resulting in a simple and highly configurable sensor architecture [9]. Low-power operation is achieved by using a comparator to digitize the zero crossings of the oscillator's output. In a 3-kHz noise bandwidth, the EC sensor interface achieves 6.7-nm (rms) resolution and dissipates 200 μW, which is 45$\times$ less than previous high-resolution EC sensors [6].

This article is organized as follows. Section II provides insights into the operation of EC sensors and describes the physical challenges and limitations commonly faced when designing them. In Section III, the architecture of the proposed sensor interface is introduced, along with a linear model of the sensor. Section IV presents the circuit implementation of the interface. In Section V, the measurement results are discussed and compared with other state-of-the-art designs. Section VI concludes this article.

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Matheus Pimenta, Paul Walsh, and Daniel O'Keeffe are with Infineon Technologies, Cork T12F76C, U.K. (e-mail: pimentaferreira.m@gmail.com).

Çağri Gürleyük, Masoud Babaie, and Kofi A. A. Makinwa are with the Department of Microelectronics, Delft University of Technology, 2628CD Delft, The Netherlands.

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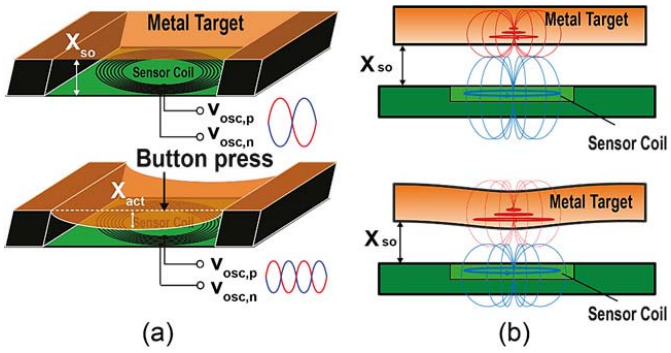

Fig. 1. (a) EC touch sensor application. (b) Operating principle.

TABLE I
SKIN DEPTH AND THERMAL DRIFT AT DIFFERENT EXCITATION FREQUENCIES

	Copper		Aluminum	
Excitation frequency	Skin Depth	Thermal drift	Skin depth	Thermal drift
100kHz	210µm	320nm/ºC	250µm	554nm/ºC
1MHz	66µm	99nm/ºC	82µm	175nm/ºC
24MHz	13.5µm	20nm/ºC	16µm	35nm/ºC
100MHz	6.6µm	9.9nm/ºC	8.2µm	17.5nm/ºC

II. SENSING SYSTEM

A. Sensor and Touch System

The proposed EC sensor is shown in Fig. 1. It consists of a flexible metal target placed at a certain standoff distance (X_{so}) from a sensing coil (L_{sen}), which forms part of an *LC* oscillator [1], [4]. When excited by an ac signal, the magnetic field produced by the sensing coil will induce ECs in the target. In turn, these currents generate a magnetic field that opposes the one generated by the sensing coil, partially canceling its nominal inductance and degrading its quality factor [10]. As the intensity of the ECs is inversely proportional to the standoff distance, a touch-induced displacement (X_{act}) results in a lower L_{sen} and quality factor.

As the magnetic fields generated by the sensor and the ECs are insensitive to dust and humidity, EC sensors are quite robust to harsh environments. However, their accuracy and stability are limited by the skin effect [7], [11]. This is because the ECs induced in the target are not constrained to its surface but actually penetrate it, with their amplitude decaying exponentially with the distance from the surface. The skin depth is defined as the distance at which the EC amplitude drops to 1/e (~0.37) of its maximum value at the conductor surface. It can be approximated by

$$\delta = \sqrt{\frac{1}{\pi \mu \sigma f_{sen}}} \tag{1}$$

where f_{sen} is the excitation frequency and μ and σ are the magnetic permeability and electric conductivity of the target, respectively. Table I shows the skin depth for aluminum and copper targets at different frequencies and its thermal drift due to the temperature dependence of the target's electrical conductivity. Temperature variations will change the skin depth and appear as a change in displacement, thus impairing the sensor's accuracy and thermal stability.

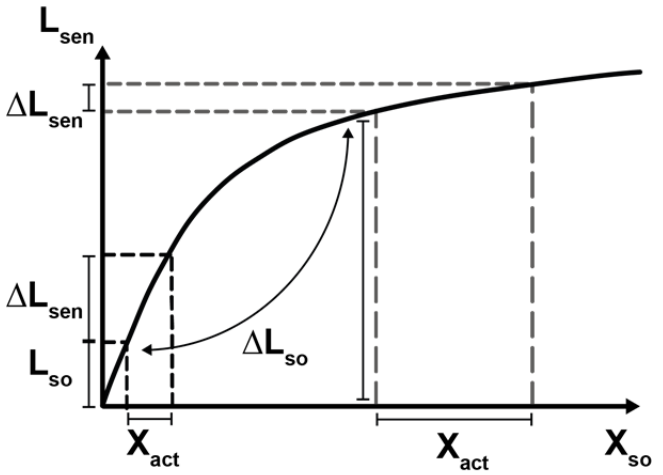

Fig. 2. Sensing coil inductance profile versus standoff distance. The nonlinear profile reduces the sensing coil sensitivity with the target distance, while the sensor offset requires compensation.

In previous works, high excitation frequencies (>100 MHz) were chosen to minimize the skin depth and achieve nanometer-level accuracy [5], [6], [12]. However, this choice significantly complicates sensor design. At such frequencies, parasitic elements, such as ESD capacitance and bond wire inductance, will have a significant effect on the resonant frequency of the sensing *LC* tank and may even cause parasitic resonances [5]. In this work, the sensor is excited at a lower frequency (~24 MHz) commensurate with the more relaxed requirements of touch applications. This also simplifies the design of the sensor interface and reduces the power consumption of the overall system.

Fig. 2 shows a conceptual plot of L_{sen} versus X_{so} for a typical EC sensor. To simplify mechanical assembly and reduce cost, X_{so} should be as large as possible. However, this imposes two challenges on the interface circuit. First, the sensor's sensitivity decreases as X_{so} increases, which typically limits the achievable displacement resolution. Second, the inductance change due to the expected target displacement (ΔL_{sen}) is only a small fraction of the sensor's inductance at standoff (L_{so}), leading to a tough dynamic range requirement. This, in turn, leads to higher power dissipation and a more complex interface design.

B. Sensor Excitation and Readout

As shown in Fig. 3(a), the sensing coil is combined with a capacitor and a pair of cross-coupled transistors to form an *LC* oscillator. In this case, the oscillation frequency (f_{sen}) and output amplitude (V_{sen}) are given by

$$V_{sen} = \eta I_{ss} R_p \tag{2}$$

$$f_{sen} = \frac{1}{2\pi\sqrt{L_{sen}C}} \tag{3}$$

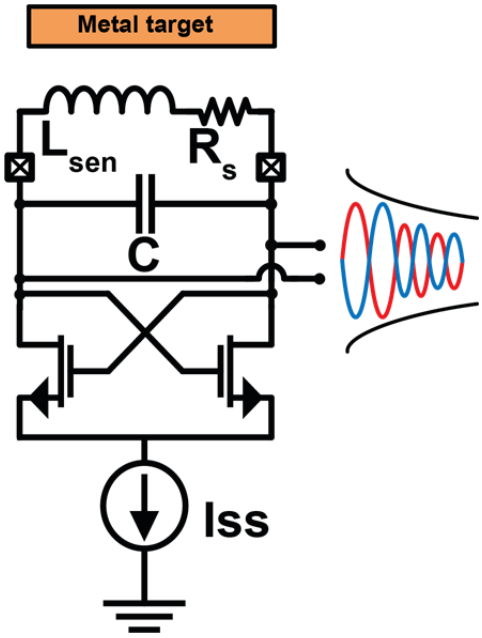

Fig. 3. Example of the sensor-controlled oscillator. With the target proximity, the oscillation amplitude decreases, and the frequency of oscillation increases.

where C is the nominal tank capacitance (plus parasitics) and η is the oscillator's current efficiency factor, which is defined as the ratio of the amplitude of the fundamental harmonic of the tank current to the oscillator's dc supply current, I_{ss}. For NMOS-only and complementary cross-coupled oscillators, η is $\sim$0.6 and 1.2, respectively [13]. R_p is the parallel resistance of the tank defined by $2\pi L_{sen} f_{sen} Q$, where Q is the quality factor of the tank. In prior art [5]–[8], sensor inductance changes were measured by sensing $V_{sen.}$ However, the various demodulation schemes required to do this consume extra power.

In this work, a bang-bang DPLL senses the changes in f_{sen} caused by target displacement. The sensing LC tank is incorporated into a digitally controlled oscillator (DCO), whose tuning word is then dynamically adjusted by the DPLL such that f_{sen} is locked to a reference clock f_{ref}. As a result, the target's displacement is directly converted into digital information, thus obviating the need for an additional ADC.

III. Proposed Architecture

A. Architecture Overview

Fig. 4(a) shows the block diagram of the DPLL-based sensor interface. It consists of a comparator-based bang-bang phase–frequency detector (PFD), a digital loop filter (DLF), and a DCO. The latter is formed by the sensing coil L_{sen}, a pair of coarse/fine capacitive banks (C_{cs} and C_{fn}), and an off-chip capacitor C_{off}. It is designed to oscillate at a nominal frequency f_{DCO} of $\sim$24 MHz.

The bang-bang PFD consists of a latched comparator. By sub-sampling the DCO's differential output at the rising edges of a 3-MHz reference clock (f_{ref}), the comparator outputs a binary signal that indicates whether the DCO's output phase is either leading or lagging the reference phase. Since $f_{DCO} = 8^* f_{ref}$, the comparator only samples the DCO's relative phase once every eight cycles, significantly reducing its power consumption and that of the succeeding DLF. The DLF consists of a programmable PI controller, whose proportional and integral path gains can be adjusted in powers of two. Compared with an analog loop filter, the DLF can be tuned in a flexible and area-efficient manner to ensure loop stability with different coil configurations and stand-off distances. The output of the DLF is then quantized to produce a bitstream (BS) that drives a 1-bit capacitive DAC (C_{fn}) such that, on average, $f_{DCO} = 8^* f_{ref}$. The BS average will thus be a digital representation of the change in L_{sen} and, hence, of the displacement X_{act} of the metal target.

To avoid metastability, the output of the comparator should settle before the rising edge of the DLF clock. To ensure this, a frequency divider generates both the comparator (f_{ref} = 3 MHz) and the DLF clocks from a 6-MHz reference frequency. The divider ensures that the DLF clock always lags the reference clock by precisely 90°.

Fig. 4(b) shows the transient response of the interface to a touch event. Initially, the DPLL is locked and f_{DCO} dithers around an average frequency of $8^* f_{ref}$. The touch event then displaces the metal target, making L_{sen} smaller and momentarily increasing the DCO frequency. In response, the DPLL reduces f_{DCO} by increasing the BS density, thus increasing the tank's effective capacitance. After a few microseconds, the DPLL settles, at which point the BS average is again proportional to the new value of X_{act}.

B. Dynamic Range and Sensor Offset Compensation

For a 5-mm-diameter coil, Fig. 5(a) shows a plot of the variation of f_{sen} as X_{so} varies from 500 μm to 1 mm. To set f_{sen} to 24 MHz at X_{so} = 1 mm, an external 69-pF capacitor was placed in parallel with the coil. As X_{so} decreases, L_{sen} decreases, thus increasing f_{sen}. Based on the requirements of the target application, a touch force of 3 N is expected to induce a displacement between 1 μm and 2 μm depending on parameters such as metal material and thickness [4]. When X_{so} = 500 μm, a displacement range of 40 μm corresponds to a DPLL lock-in range of 250 kHz. For X_{so} = 1 mm, the corresponding displacement range is $\sim$3$\times$ larger. To cover this range of stand-off distances, as well as other mechanical tolerances, the tank capacitance can be trimmed via a coarse capacitive DAC (C_{cs}) to set f_{sen} close to the desired 24 MHz, as shown in Fig. 5(b).

The tolerances of the capacitive DAC cause gain errors, which alter the PLL's lock-in range and the sensor's maximum displacement range. By adjusting C_{cs} properly, a maximum displacement range of 30 μm can be achieved. As long as the SNR is not too low, such gain errors should not prevent the detection of a touch-induced displacement.

Ambient temperature changes are another source of error. However, the temperature coefficient (TC) of on-chip capacitors is quite small (<30 ppm/°C), as is that of the coil, and so changes in ambient temperature will only cause a small drift in the DAC input. This can then be suppressed by a digital

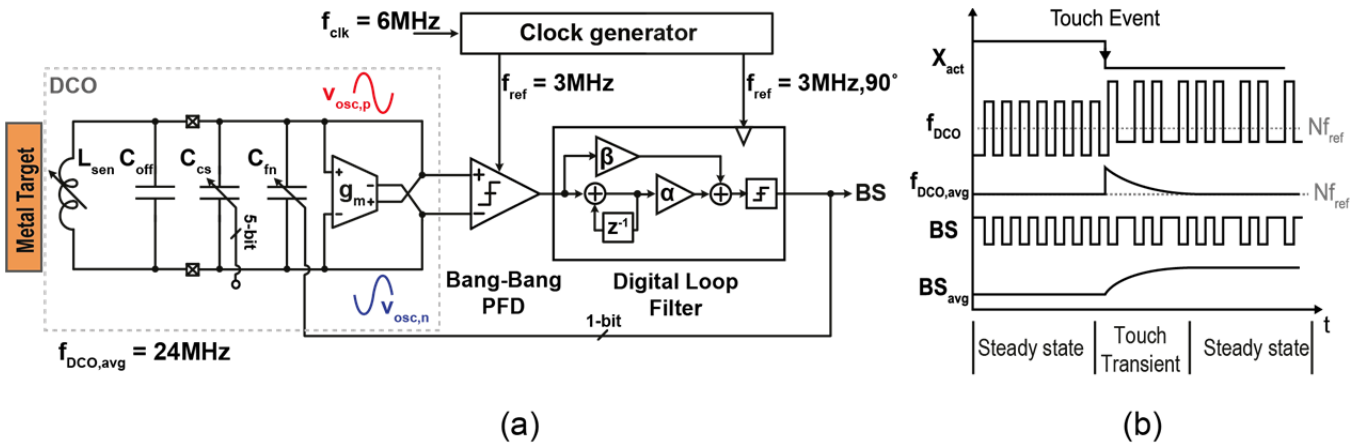

Fig. 4. Architecture of (a) PLL-based EC sensor interface and (b) its operating timing diagram.

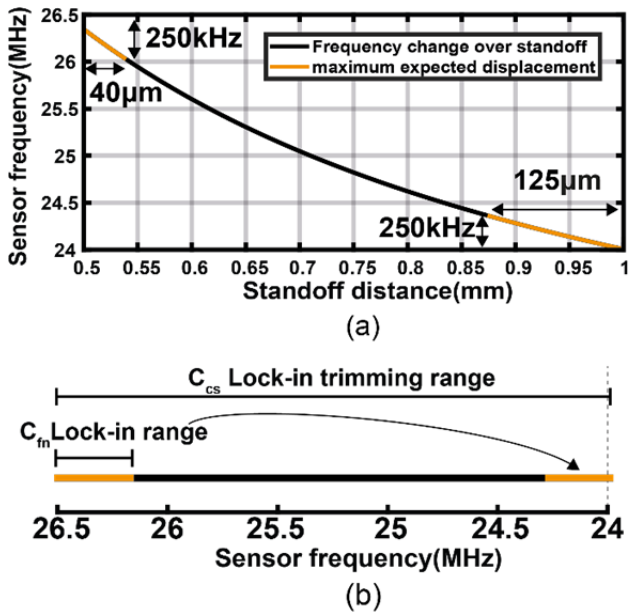

Fig. 5. Frequency profile of the free-running sensor oscillator with (a) fixed tank's capacitance and (b) employing C_{cs} switched capacitor banks to trim the oscillator center frequency to the desired 24 MHz for different standoff distances.

high-pass filter [3] since a touch creates a transient signal that is much larger than the drift.

C. Linear Model and Noise Analysis

The use of a bang-bang PFD to digitize phase error introduces a hard nonlinearity in the DPLL's feedback loop. Nevertheless, the use of a linear model provides useful insights into loop dynamics and allows the displacement resolution to be estimated. Fig. 6 shows a simplified linear model of the proposed DPLL-based EC sensor.

The bang-bang PFD is modeled as a time-domain subtractor that compares the timestamps of the rising edges of the reference clock (t_{ref}), and the DCO (t_{DCO}), followed by an equivalent gain:

$$K_{\text{pfd}} \approx \frac{1}{\sqrt{2\pi}\,\sigma_{\text{terr}}} \tag{4}$$

which converts the resulting time error (t_{err}) into binary form. Note that K_{pfd} is a strong function of t_{err} jitter (σ_{terr}), which in turn depends on the dynamics of the DPLL itself [14]. The output of the bang-bang PFD is applied to the DLF with a transfer function of

$$L(z) = \left(\beta + \frac{\alpha z^{-1}}{1 - z^{-1}}\right) z^{-D} \tag{5}$$

where α and β are the integral and proportional gains of the filter, respectively, and z^{-D} models the loop delay. The output of the loop filter (D_{out}) is truncated and fed back to the DCO.

Both D_{out} and metal target displacement (X_{act}) can change the oscillator frequency through the gains K_{DCO} (Hz/LSB) and K_L(Hz/nm), respectively. The DCO acts as a digital-to-analog converter, holding the frequency constant between two D_{out} samples. This zero-order hold (ZOH) behavior is modeled by $\text{sinc}(f/f_r)$. The following integrator finally converts the oscillator frequency into its corresponding phase.

In the model, the main noise sources are the reference jitter ($\sigma_{j,\text{ref}}$), the PFD's equivalent input jitter ($\sigma_{j,\text{pfd}}$), the DCO's quantization noise ($Q_{n,,\text{DCO}}$), and phase noise ($\varphi_{n,\text{DCO}}$). These have power spectral densities (PSDs) of $\sigma^2_{j,\text{ref}}/f_r$, $\sigma^2_{j,\text{pfd}}/f_r$, $1/12f_r$, and $\mathcal{L}(f) = \varphi^2_{n,\text{DCO}} \propto (1/f^2)$. Note that all these PSDs are white except for $\mathcal{L}(f)$, which drops by 20 dB/decade, as shown in Fig. 7(a). $\sigma_{j,\text{pfd}}$ and $\mathcal{L}(f)$ are dependent on circuit parameters and will be quantified in Section IV.

The abovementioned noise sources appear at the output with the following noise transfer functions (NTFs):

$$H_{\text{ref}} = H_{\text{pfd}} = \frac{K_{\text{pfd}} L(z)}{1 + K_{\text{pfd}} L(z) \frac{K_{\text{dco}}}{s} \text{sinc}\left(\frac{f}{f_r}\right) \frac{1}{f_{\text{dco}}}} \tag{6}$$

$$H_{\text{DCO}} = \frac{D_{\text{out}}}{\varphi_{n,dco}} = \frac{K_{\text{pfd}} L(z) \frac{1}{2\pi f_{\text{dco}}}}{1 + K_{\text{pfd}} L(z) \frac{K_{\text{dco}}}{s} \text{sinc}\left(\frac{f}{f_r}\right) \frac{1}{f_{\text{dco}}}} \tag{7}$$

$$H_{\text{DCO},q} = \frac{D_{\text{out}}}{Q_{n,\text{dco}}} = \frac{1}{1 + K_{\text{pfd}} L(z) \frac{K_{\text{dco}}}{s} \text{sinc}\left(\frac{f}{f_r}\right) \frac{1}{f_{\text{dco}}}}. \tag{8}$$

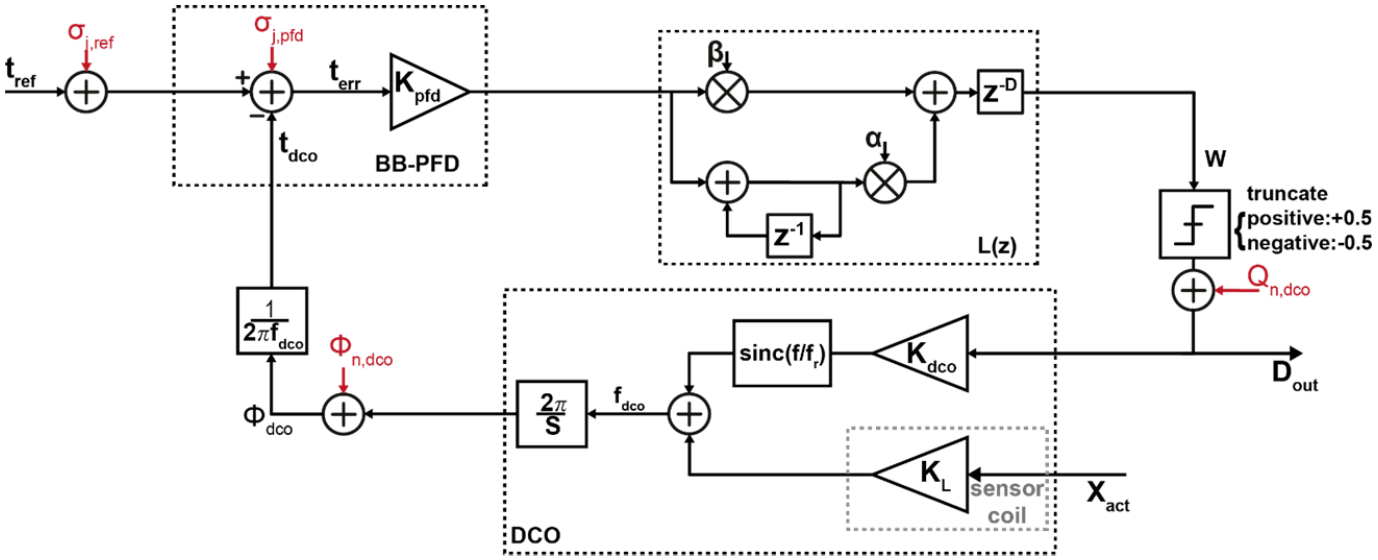

Fig. 6. Simplified linear model of the proposed DPLL-based EC sensor interface.

All the NTFs are shown in Fig. 7(b). Since both the oscillator and the DLF act as integrators, the PFD's noise and the DCO's phase noise are first-order shaped with a bandwidth of

$$f_{\text{pll}} = \frac{\beta K_{\text{DCO}} K_{\text{pfd}}}{2\pi f_{\text{DCO}}}. \tag{9}$$

However, the DCO's quantization noise is attenuated with a 40-dB/decade slope up to

$$f_1 = \frac{\alpha}{2\pi\beta} f_{\text{ref}} \tag{10}$$

and with a 20 dB/decade from f_1 to f_{pll}. Consequently, more aggressive attenuation can be achieved by increasing α/β. In principle, the impact of the DCO's quantization noise can also be reduced by setting f_1 close to f_{pll}. However, this will reduce the phase margin of the PLL and increase the risk of instability.

Fig. 7(c) shows the contribution of the different noise sources to the output noise PSD. Due to thermal noise up-conversion, the DCO's phase noise has a $1/f^2$ characteristic around the carrier frequency. After first-order shaping, this dominates the in-band noise of the output BS and thus determines the system's resolution. Beyond a particular frequency, the other noise sources start to become dominant, increasing the output noise by 20 dB/decade. For optimal energy efficiency, the maximum conversion bandwidth (BW_{conv}) of the sensor should be at the intersection of the flat and 20-dB/decade regions of the output PSD. With a phase noise -76 dBc/Hz at 1-kHz offset frequency, the in-band noise floor will be ~ -120 dB, corresponding to an effective resolution of $\Delta F = 20.5\ \text{Hz}_{\text{rms}}$ in a 3-kHz bandwidth. The displacement resolution is then found to be 3.3 nm_{rms} by dividing ΔF by $K_L = 6$ Hz/nm.

It is worth mentioning that the use of a non-linear PFD will cause limit cycles when the average value of D_{out} is a rational number, e.g., 0, $+1/3$, and $-1/3$. To mitigate the effect of such limit cycles, enough noise needs to be generated at the input of the bang-bang PFD [15] such that

$$\sigma_{\text{terr}} \geq \frac{(1+D)N\beta}{\sqrt{3}} \frac{K_{\text{DCO}}}{f_{\text{dco}}^2}. \tag{11}$$

Consequently, the reference and/or the DCO must be noisy enough to satisfy the above condition. Since the DCO's phase noise determines the system resolution, choosing a sufficiently noisy reference clock and/or comparator is the logical choice. Hence, the main contributors to σ_{terr} are $\sigma_{n,\text{ref}}$ and $\sigma_{j,\text{pfd}}$.

Fortunately, they appear at the output with a high-pass NTF and their contributions are greatly attenuated at low frequencies. The large noise power needed to meet the limit cycle criterion will then impose a limitation on the maximum conversion bandwidth.

IV. Circuit Implementation

A. Digitally Controlled Oscillator

Fig. 8 shows the schematic of the DCO. It consists of the sensing coil, a cross-coupled pair, a pair of coarse/fine switchable capacitor banks (C_{cs} and C_{fn}), and a programmable bias tail current DAC (I_{ss}).

A complementary cross-coupled oscillator is used since its transconductance is set by both the NMOS($M_{1,2}$) and PMOS($M_{3,4}$) pairs, making it an attractive solution for low-power designs [16]. Furthermore, the maximum gate–drain–source voltage of all transistors is always kept below the nominal supply voltage (V_{DD}), conferring robustness to failure mechanisms such as time-dependent oxide breakdown and hot-carrier injection [17]. The NMOS and PMOS pairs are sized such that the ratio of their transconductances sets the output common-mode voltage to $\sim$0.5 V_{DD}. This maximizes the oscillator's output swing and minimizes its phase noise [13].

The two capacitive DACs are implemented, as shown in Fig. 8(b). A 5-bit, 24-pF full-scale, coarse DAC C_{cs} allows the system to cope with a wide range of standoff distances

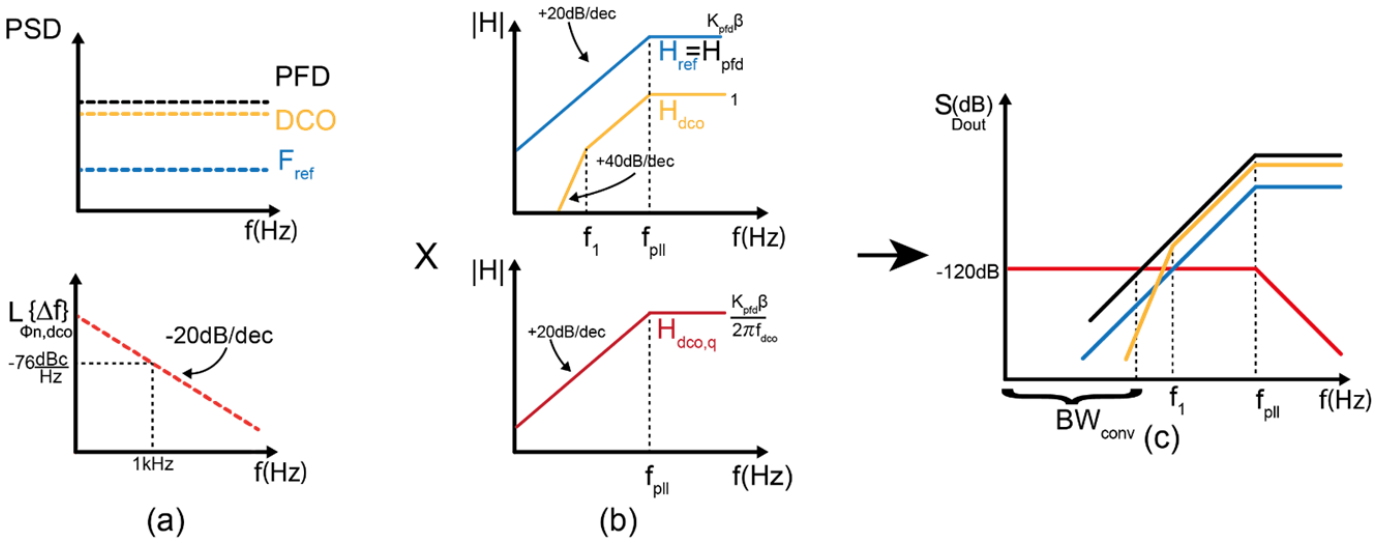

Fig. 7. (a) PSD of main noise sources. (b) NTFs. (c) Output contribution of each noise source at the output. The main inband noise results from the DCO phase noise.

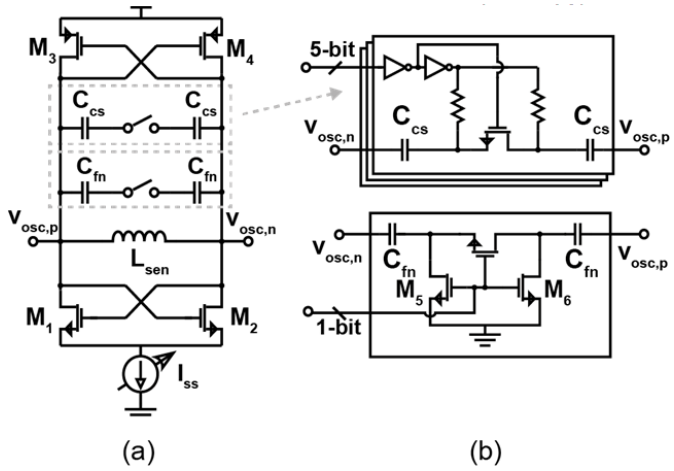

Fig. 8. Schematics of (a) DCO and (b) capacitive banks.

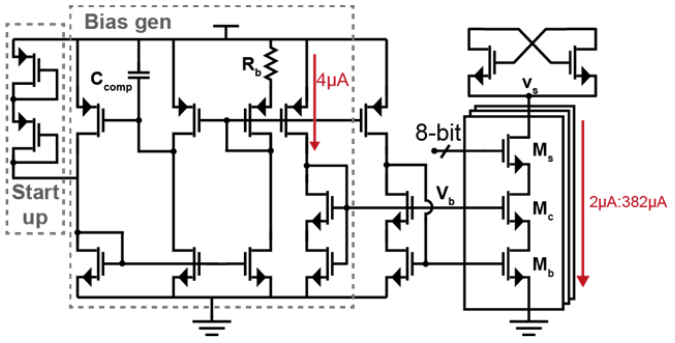

Fig. 9. Current DAC implementation along with bias generator.

and their associated frequency offsets. Its LSB is ∼0.75 pF, or approximately half of $C_{\rm fn}$, which ensures that their tuning ranges overlap, relaxing their matching requirements. To minimize their "OFF" capacitance and thus maximize the DCO's tuning range, large (1.25 MΩ) resistors are used to reverse-bias the drain/source-to-bulk diodes of the coarse DAC switches. To avoid compromising the tank's quality factor, the switches are sized such that the quality factor of the capacitive DAC banks is $>20\times$ higher than that of the external sensing coil.

To cover the targeted displacement range, the fine DAC $C_{\rm fn}$ is a 1.6-pF switchable capacitor. To minimize its switching time and achieve a compact layout, the function of the biasing resistors of the coarse DAC is realized by two transistors ($M_{5,6}$).

The total parasitic capacitance ($C_{\rm par}$) is ∼22 fF or ∼1.5% of $C_{\rm fn}$. This is acceptable because the sensor's absolute accuracy is not critical. Since $C_{\rm fn}$and$C_{\rm cs}$ are much larger than $C_{\rm par}$, the tank's OFF capacitance is approximately $C_{\rm par}$.

From (2), the DCO's dc current ($I_{\rm ss}$) is inversely proportional to $L_{\rm sen}$. To enable the use of a wide range of sensing coils, the DCO's current source is implemented as an 8-bit current DAC with a 2-μA LSB. This also allows the transconductance (gm) of the cross-coupled transistors to be tuned so that the Barkhausen start-up criteria ($gm > 1/R_p$) is met over PVT. Furthermore, the 2-μA LSB allows the oscillator amplitude to be fine-tuned to optimize phase noise.

Fig. 9 shows the schematic of the current DAC and biasing circuit. The cascode structure reduces the dependence of the tail current on the source coupled node (V_s) and also isolates this node from the parasitic capacitance of the current source transistors (M_b). As a result, M_b can be larger, thus minimizing its $1/f$ noise contribution to the bias current [18]. From simulations, the phase noise at 1 kHz is −87 dBc/Hz.

B. Comparator-Based Phase and Frequency Detector

Fig. 10(a) shows the schematic of the bang-bang phase detector. This block is implemented as a single-stage latched comparator. An input pair converts the differential voltages of the oscillator into a differential current, which drives the cross-coupled latch. As shown in Fig. 10(b), by comparing the complementary voltages of the DCO at the rising edge of the reference clock, this block digitizes the sensor phase with respect to the reference phase.

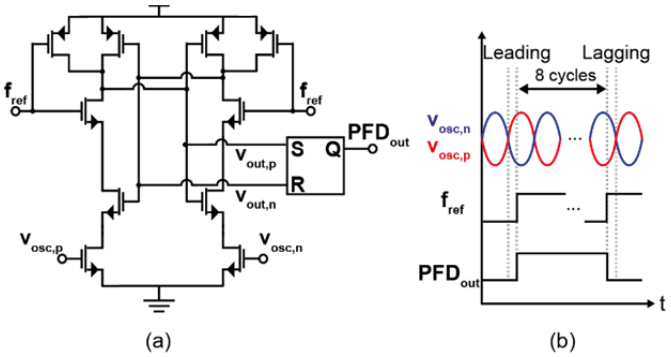

Fig. 10. (a) Comparator-based PFD schematic and (b) its operation principle.

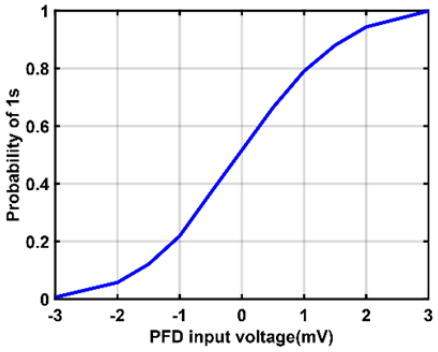

Fig. 11. Cumulative distribution function of PFD. Integrated noise $\sigma_{v,\mathrm{pfd}} = 1.25\ \mathrm{mV_{rms}}$.

Being a dynamic comparator, the power dissipation of the circuit can be expressed as

$$P = \gamma f_{\mathrm{ref}} C_L V_{dd}^2 \tag{12}$$

where C_L is the comparator capacitive load and γ is the switching probability, which is equal to 1, because the comparator is always reset before the phase comparison [19]. From (12), locking the DCO frequency to a lower reference frequency linearly reduces the comparator power consumption. However, it comes at the expense of lower DPLL bandwidth and smaller conversion bandwidth. By considering this tradeoff, f_{ref} is reduced from f_{DCO} to $f_{\mathrm{DCO}}/8$, decreasing the comparator's average current consumption from 45 to 5.6 μA.

The input-referred noise of the comparator was evaluated by transient noise simulations; 1500 comparisons were made for different values of input voltages, and the resulted cumulative distribution function is shown in Fig. 11. The simulated input-referred noise is 1.25 $\mathrm{mV_{rms}}$, which can be translated to the comparator equivalent input jitter ($\sigma_{j,\mathrm{pfd}}$) by [20]

$$\sigma_{t,\mathrm{pfd}} = \frac{\sigma_{v,\mathrm{pfd}}}{dV/dt} = \frac{\sigma_{v,\mathrm{pfd}}}{2\pi f_{\mathrm{osc}} \cdot A_{\mathrm{osc}}} \approx 9 \quad \mathrm{psec} \tag{13}$$

where A_{osc} is the differential amplitude of the oscillator output voltage. Interestingly, a larger oscillation swing minimizes the impact of both the oscillator's phase noise and the PFD's thermal noise. Periodically resetting the comparator significantly reduces its flicker noise contribution [21], which is further attenuated by the loop, as can be seen from (6).

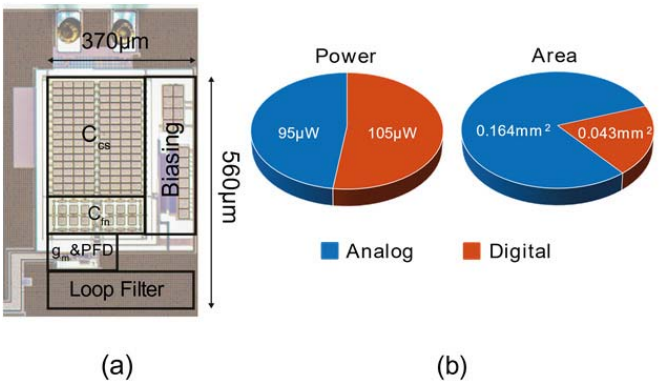

Fig. 12. (a) Micrograph of the EC sensor interface. (b) Power and area breakdown.

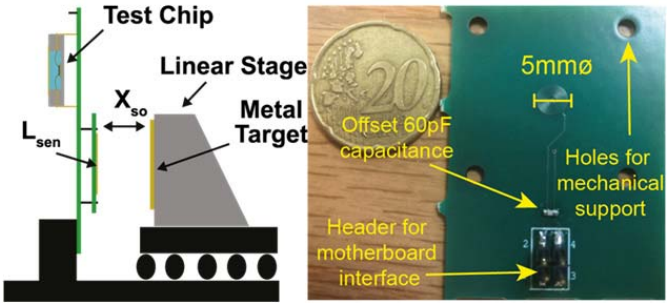

Fig. 13. (a) Measurement setup. (b) Sensing coil.

V. Measurement Results

The integrated EC sensor interface was implemented in a standard TSMC 0.18-μm process. It occupies an area of 0.2 $\mathrm{mm^2}$ and draws 200 μW from a 1.8-V supply (Fig. 12). The digital blocks of the chip include the DLF and the PFD, which occupy an area of 0.043 $\mathrm{mm^2}$ while consuming 105 μW. Locking the DCO frequency to $f_{\mathrm{DCO}}/8$ instead of f_{DCO} reduces the digital power consumption by nearly 3×. The analog blocks consist of the DCO and biasing circuitry. They occupy an area of 0.164 $\mathrm{mm^2}$, of which approximately 50% is due to C_{cs}, and consume 95 μW. As the accuracy requirements on the coarse DAC are quite relaxed, the biasing resistors of its switches were placed under the capacitive DAC. For flexibility, the output of the PLL is decimated by an off-chip $\mathrm{sinc^2}$ filter.

In Fig. 13(a), the measurement setup used for characterizing the EC sensor interface is shown. A field-programmable gate array (FPGA) is used to program the internal registers of the chip and thus trim the oscillator and set the gains of the DLF. A low-jitter waveform generator (Agilent 33600a) was used as the reference frequency for the PLL. To accurately control its distance from the EC sensor, a copper metal target was mounted on an M-605.1DD linear stage. This was placed on an optical table to suppress the effect of ambient vibration. Although a touch will actually bend, rather than displace, the metal target, this setup allows the sensor's dynamic range and resolution to be accurately evaluated.

Fig. 13(b) shows the PCB sensor used for characterization. It consists of a two-layer ten-turn coil with 5 mm outer

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF PUBLISHED EC SENSING INTERFACES

	This work	[5]	[6]	[3]	[7]	[8]	[22]
Tech (µm)	**0.18**	0.18	0.18	-	0.35	0.35	0.6
Area (mm^2)	**0.207**	1.177	0.264	-	2.64	3.96	13
X_{so} (m)	**500µ**	105µ	55µ	500µ	3m	3m	3m
f_{sen} (MHz)	**24**	126	145	24	20	15	0.312
ENOB	**12.7**	14.1[#]	12.4	12	15.5[#]	15	10
Res (nm)	**6.7**	0.6	1.85	~100[&]	65	136	2930
Res (pH)	**2.5**	0.58	1.02	-	1.5	3.8	-
BW (kHz)	**3**	2	2	1	1	1	10
Power (mW)	**0.2**	19.8	9.1	3.4[&]	18	18	7.3*
FoM (nm^2J)	**3.0µ**	3.6µ	15µ	34m	76m	328m	6.27

[#]Analog Output *Disconsidering Digital Filter [&]Considering similar L_{sen}, X_{so} and f_{sen}

diameter and 0.1 mm trace width and spacing and a 60-pF NP0 external capacitance. The coil has a nominal inductance of 850 nH, which drops to 550 nH when a target is positioned at 500-μm X_{so}. The self-resonant frequency of this coil sensor was measured with an impedance analyzer and was found to be higher than 120 MHz, making it suitable for use at the intended 24-MHz excitation frequency [10]. For test flexibility, two headers were used to connect the sensing coil to the PCB, allowing the chip to be tested with different sensors. The parasitic inductance of the headers is ~2 nH.

A. Transfer Characteristic

Fig. 13(a) shows the BS average versus the metal target position measured at two different standoff positions with the PCB sensor. The target is positioned at the desired standoff distance and C_{cs} trimmed until the PLL locks f_{sen} to $8^* f_{ref}$. The metal target is then shifted in steps of 2 μm by the linear stage. The transfer characteristic is measured at two near extremes of C_{cs}, corresponding to 500-μm and 1-mm standoffs. This results in conversion ranges of 42 and 135 μm due to the loss in sensor sensitivity at larger standoffs.

The dynamic range of the interface is about 95% of the tuning range provided by C_{cs}. Fig 14(b) shows the decimated BS during ~1 s of measurement time. The standard deviation of 3300 decimated samples is 6.7 and 26.8 nm at the 500-μm and 1-mm standoff distances, respectively.

B. Noise Characteristic

Fig. 15(a) shows the PSD of the output BS. The EC sensor interface is thermal noise limited up to 3 kHz and achieves a peak SNR of 77.4 dB or an ENOB of 12.7 bits. For a sensing coil inductance $L_{sen} = 550$ nH with a metal target placed at $X_{so} = 500$ μm, the interface achieves an inductance resolution of 2.5 pH. The in-band noise floor is mainly due to the DCO's phase noise, which is flattened by the first-order noise shaping behavior of the PLL. The reference and PFD noise initially dominate the out-of-band noise. At higher frequencies, the contribution of the second-order shaped quantization noise of the DCO becomes dominant.

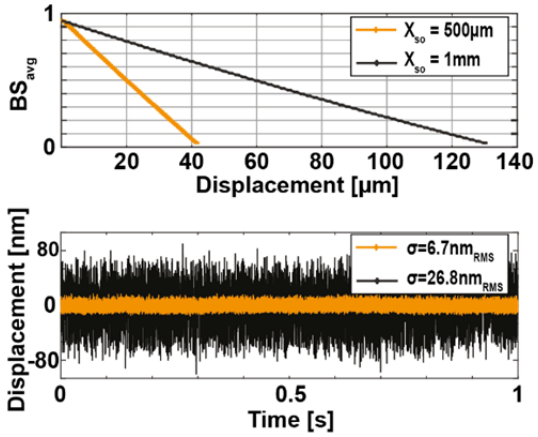

Fig. 14. (a) Measured sensor transfer for different X_{so}. (b) Equivalent sensor decimated output.

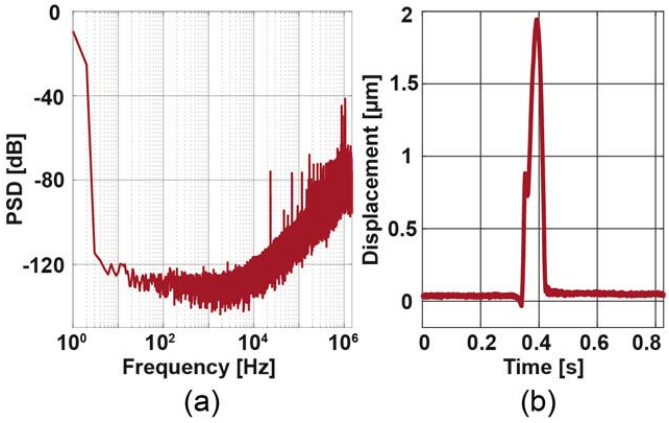

Fig. 15. (a) Measured PSD of the output BS. (b) Sensor response to touch after decimation.

With $X_{so} = 500$ μm, the sensor's output in response to a transient touch event is shown in Fig. 15(b). It can be seen that

the touch corresponds to a ∼2-μm displacement of the metal target. This result demonstrates that the sensor has sufficient bandwidth and resolution to distinguish actual touch events.

C. Performance Comparison

Table II summarizes the performance of the proposed EC sensor interface and compares it with state-of-the-art interfaces. Compared to prior work, the presented interface achieves a competitive 6.7-nm (rms) resolution in a relatively wide 3-kHz bandwidth while consuming 200 μW, which is 45× better than [6]. To objectively compare the efficiency of the interfaces, we define the following resolution figure of merit (FoM)

$$\text{FoM} = \frac{\sigma_{\text{nm}}^2 \cdot P}{\text{BW}} \tag{14}$$

where σ_{nm} is the interface resolution in meters, P is the power consumption, and BW is the integrated noise bandwidth.

Despite not achieving as much resolution as in [5] and [6], the massive reduction in power consumption achieved by this EC sensor interface results in the best reported FoM. Moreover, the low-power operation of the proposed readout makes it a promising candidate for use in battery-powered applications and in safety-critical sensing nodes with limited power budget.

VI. Conclusion

This article presents a low-power integrated EC sensor interface intended for touch on metal applications. The readout circuit incorporates the EC sensor in a bang-bang DPLL to efficiently digitize the displacement of a flexible metal target. The interface uses a comparator-based front end to digitize the sensor or phase information. Changing the sensing from voltage to frequency along with the inclusion of a coarse capacitive DAC allows compensating for the sensor offset without the need for an external reference coil.

Due to the system's high-pass response to all noise sources, a 6.7-nm (rms) displacement resolution in a 3-kHz bandwidth is achieved while consuming only 200 μW from a 1.8-V supply. Compared to prior art, this work achieves the best FoM and the smallest die area while consuming 45× less power than similar high-resolution interfaces. Moreover, the proposed digital-intensive design benefits from technology scaling, promising to achieve even better energy and area efficiency.

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References

[1] B. Kasemsadeh and L. Lapointe. (2016). *Inductive Sensing Touch-On-Metal Buttons Design Guide*. [Online]. Available: https://www.ti.com/lit/an/snoa951/snoa951.pdf

[2] Texas Instruments. (2015). *LDC1000 Inductance-to-Digital Converter*. [Online]. Available: https://www.ti.com/

[3] Texas Instruments. *LDC2112, LDC2114 Inductive Touch Solution for Low-Power HMI Button Applications*. Accessed: Dec. 18, 2020. [Online]. Available: https://www.ti.com/lit/ds/symlink/ldc2114.pdf

[4] P. Walsh and D. Mani. *Inductive Sensing Design Guide*. Accessed: Dec. 18, 2020. [Online]. Available: https://www.cypress.com/documentation/application-notes

[5] V. Chaturvedi, J. G. Vogel, K. A. A. Makinwa, and S. Nihtianov, "A 19.8-mW eddy-current displacement sensor interface with sub-nanometer resolution," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2273–2283, Aug. 2018.

[6] V. Chaturvedi, J. G. Vogel, K. A. A. Makinwa, and S. Nihtianov, "A 9.1 mW inductive displacement-to-digital converter with 1.85 nm resolution," in *Proc. Symp. VLSI Circuits*, Jun. 2017, vol. 37, no. 12, pp. .C80–C81.

[7] M. R. Nabavi, M. A. P. Pertijs, and S. Nihtianov, "An interface for eddy-current displacement sensors with 15-bit resolution and 20 MHz excitation," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2868–2881, Nov. 2013.

[8] A. Fekri, M. Nabavi, N. Radeljic-Jakic, Z.-Y. Chang, M. Pertijs, and S. Nihtianov, "An eddy-current displacement-to-digital converter based on a ratio-metric delta-sigma ADC," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 403–406.

[9] M. Pimenta, Ç. Gürleyük, P. Walsh, D. O'Keeffe, M. Babaie, and K. Makinwa, "A 200 μW eddy current displacement sensor with 6.7 nm RMS resolution," in *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, Jun. 2020, pp. 6–7.

[10] S. D. Roach, "Designing and building an eddy current position sensor," *Sensors J. Appl. Sens. Technol.*, vol. 15, no. 9, pp. 56–74, 1998.

[11] M. R. Nabavi and S. N. Nihtianov, "Design strategies for eddy-current displacement sensor systems: Review and recommendations," *IEEE Sensors J.*, vol. 12, no. 12, pp. 3346–3355, Dec. 2012.

[12] S. Nihtianov, "Measuring in the subnanometer range: Capacitive and eddy current nanodisplacement sensors," *IEEE Ind. Electron. Mag.*, vol. 8, no. 1, pp. 6–15, Mar. 2014.

[13] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[14] N. D. Dalt, "Markov chains-based derivation of the phase detector gain in bang-bang PLLs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1195–1199, Nov. 2006.

[15] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 1, pp. 21–31, Jan. 2005.

[16] N. Seshan, J. Rajagopalan, and K. Mayaram, "Design of low power 2.4 GHz CMOS LC oscillators with low phase-noise and large tuning range," in *Proc. IEEE Int. Symp. Circuits Systems. Proc.*, May 2002, pp. 409–412.

[17] M. Babaie and R. B. Staszewski, "A study of RF oscillator reliability in nanoscale CMOS," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2013, pp. 63–66.

[18] P. Andreani and A. Fard, "More on the 1/f^2 phase noise performance of CMOS differential-pair LC-tank oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2711, Dec. 2006.

[19] N. E. H. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, vol. 53, no. 9. 2013.

[20] S. Levantino, L. Romano, S. Pellerano, C. Samori, and A. L. Lacaita, "Phase noise in digital frequency dividers," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 775–784, May 2004.

[21] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, E. A. J. M. Van Tuijl, and B. Nauta, "Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 1022–1025, Jul. 1999.

[22] M. Oberle, R. Reutemann, R. Hertle, and Q. Huang, "A 10-mW two-channel fully integrated system-on-chip for eddy-current position sensing [in biomedical devices]," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 916–925, Jul. 2002.

Matheus Pimenta (Member, IEEE) received the B.Sc. degree in electronic engineering from the University of Brasília, Brasília, Brazil, in 2015, and the M.Sc. degree from the Electronic Instrumentation Laboratory, Delft University of Technology (TU Delft), Delft, The Netherlands, in 2019.

Since 2020, he has been with Infineon Technologies, Cork, U.K., where he is working with low-power analog building blocks for capacitive and inductive sensing. His research interests include low-power sensor interface ICs and energy-efficient data converters.

Çağrı Gürleyük (Student Member, IEEE) was born in Istanbul, Turkey, in 1987. He received the B.Sc. and M.Sc. degrees from Istanbul Technical University, Istanbul, Turkey, in 2011 and 2015, respectively. He is currently pursuing the Ph.D. degree with the Delft University of Technology, Delft, The Netherlands, with a focus on high-accuracy integrated frequency references.

From 2014 to 2016, he was a Design Engineer with Analog Devices, Istanbul, where he worked in the high-data-rate group on low-noise transimpedance amplifiers for LiDAR applications. He is currently a Senior Member of Technical Staff with Ethernovia, San Jose, CA, USA, working on data converter systems for automotive Ethernet applications.

Paul Walsh was born in Limerick, Ireland. He received the B.E. degree in electronic engineering from the University of Limerick (UL), Limerick, in 1999, and the M.Eng. degree from the University of Michigan, Ann Arbor, MI, USA, in 2004.

He is currently working with Infineon, Cork, where he is a Sr MTS Architect. He is responsible for both capacitive and inductive sensing and leads the Sense Centre of Excellence (COE), Infineon. At Infineon, he has led to the development of capacitive and inductive sensing IP for touch and fingerprint controllers. He currently manages a Systems Research and Development Team with a focus on next-generation sensing.

Daniel O'Keeffe was born in Cork, Ireland. He received the B.E. degree in electronic engineering from University College Cork (UCC), Cork, in 2000, and the M.Eng.Sc. degree from the Tyndall National Institute, UCC, in 2003.

He is currently a Senior Principal Design Engineer with Infineon, Cork. He is also the IP lead for human–machine interface (HMI) products. At Infineon, he has led to the development of various capacitive, inductive, fingerprint, and touch sensing IPs for both the consumer and automotive divisions. He is currently leading teams that are developing next-generation solutions in capacitive and touch sensing technologies.

Masoud Babaie (Member, IEEE) received the Ph.D. degree (*cum laude*) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016.

In 2006, he joined the Kavoshcom Research and Development Group, Tehran, Iran, where he was involved in designing wireless communication systems. From 2009 to 2011, he was the CTO of the Kavoshcom Research and Development Group. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently a tenured Assistant Professor. He has coauthored one book, three book chapters, 11 patents, and over 60 technical articles. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie has been a Committee Member of Student Research Preview (SRP) of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017 and a Technical Program Committee of the IEEE European Solid-State Circuits Conference (ESSCIRC) since 2020. He was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, the 2019 IEEE ISSCC Best Demo Award, and the 2020 IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper. In 2019, he received the Veni Award from the Netherlands Organization for Scientific Research (NWO).

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, where he worked on interactive displays and digital recording systems. In 1999, he joined the Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has resulted in 16 books, over 250 technical articles, and over 30 patents.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences and the Editorial Board of the PROCEEDINGS OF THE IEEE. He was a co-recipient of 15 best paper awards, including two from the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and three from the International Solid-State Circuits Conference (ISSCC). At the 60th anniversary of ISSCC, he was recognized as a Top-Ten Contributor. He has been on the program committees of several IEEE conferences. He has served the IEEE Solid-State Circuits Society as a Distinguished Lecturer and as an elected member of its AdCom. He has also served as a Guest Editor of the IEEE JSSC. He is also the Analog Subcommittee Chair of the ISSCC and a co-organizer of the Advances in Analog Circuit Design (AACD) Workshop and the Sensor Interfaces Meeting.