Power Consumption Analysis of 5G Transmit Antenna Topologies and Beamforming Schemes.

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Power consumption analysis of 5G transmit antenna topologies and beamforming schemes.

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Abstract

An exponential growth in the mobile communications industry over the past decade has raised concerns over it's energy consumption, especially in light of the current climate crisis. 5G technologies in particular exhibit features that imply high power consumption, such as the densification of 5G base stations. Implementing mitigation measures requires accurate a priori knowledge of the power consumption of 5G array architectures in various scenarios; however, there are large gaps in the literature on this topic, and existing power consumption models for 5G array architectures only address a limited scope of use cases and array topologies. Recent works have focused on the energy efficiency of array architectures, but not on the actual amount of power being consumed.

In this thesis, an integrated system-level power consumption model is devised for 5G base station multi-beam transmitter topologies and beamforming schemes, which accounts for the use cases and architectures missing from the literature. The model is then applied to novel use cases in the enhanced urban Mobile Broadband (eMBB) scenario to obtain the estimated power consumption per component, per array and per user for five different beamforming schemes. A thorough parametric analysis is conducted for the optimality and trade-offs of each use case. Recommendations are made on the optimal topology, beamforming scheme and front-end technology from a power consumption perspective. Initial results show that the choice of technology, architecture and topology can lead to an improvement in the per-user power consumption of 41-80%.

Key words – 5G, MIMO, power consumption, beamforming, antenna

Contents

Nomenclature

3GPP 3rd Generation Partnership Project

ABF analog beamforming
ADC analog-to-digital converter
ASIC application-specific integrated circuit

BB baseband
BBU baseband unit
BPF band pass filter
BS base station

CMOS complementary metal-oxide semiconductor
CSI channel state information

DAC digital-to-analog converter
DBF digital beamforming
DL downlink
DMBA digital multi-beam array
DPD digital pre-distortion
DSP digital signal processing

EE energy efficiency
EIRP effective isotropic radiated power
eMBB enhanced Mobile Broadband
ENOB Effective Number of Bits

FEM Front End Module
FOM figure of merit
FPGA field programmable gate array

GaAs gallium-arsenide
GaN gallium-nitride
GOPS giga-operations per second

HBF hybrid beamforming
HFC fully-connected hybrid array
HSA phased sub-array-based hybrid array

IL insertion loss

KPI Key Performance Indicator

LO local oscillator
LOS line-of-sight

MBPAA multi-beam phased array antenna
MIMO multiple-input-multiple-output
mmW millimeter wave
MOPS mega-operations per second
MU multi-user

NF noise factor
NLOS non-line-of-sight

PA power amplifier
PAE power added efficiency
PAPR peak-to-average power ratio
PBO power back-off
PD pre-driver
PLL phase-locked loop
PS phase shifter

RF radio frequency
Rx receiver

SDMBA fixed sub-array-based digital multi-beam array
SE spectral efficiency
SFDR spurious free dynamic range
SiGe silicon-germanium
SINAD signal-to-noise-and-distortion ratio
SINR signal-to-interference-and-noise ratio
SNR signal-to-noise ratio
SOI silicon-on-insulator
SOTA state-of-the-art

Tx transmitter

UE User Equipment
UL uplink
ULA uniform linear array

VCO voltage controlled oscillator
VGA variable gain amplifier

List of Symbols

f_c	centre frequency	$P_{out_{PA}}$	PA output power
BW	bandwidth	$P_{1dB_{PA}}$	PA output power at 1dB compression
R	data rate	P_{sat}	PA saturation power
d_{UE}	distance between BS and UE	IL	insertion loss
C_R	coding rate	f_{cor}	DAC corner frequency
M_O	modulation order	f_s	sampling frequency
SNR	signal-to-noise ratio	b	DAC resolution
T	temperature	V_{DD}	supply voltage
k_B	Boltzman constant ($1.38 \cdot 10^{-23} m^2 kgs^{-2} K^{-1}$)	N_{ip}	number of input ports to antenna array
N_{TX}	number of transmit array antenna elements	m_z	number of complex multiplications in baseband unit
N_{RX}	number of receive array antenna elements	r_z	processing rate of baseband unit
PL_α	path loss coefficient	γ_{DSP}	dependence of DSP on beamforming architecture
c	speed of light ($3 \cdot 10^8 m/s$)	η_{BBU}	baseband unit efficiency
U	number of simultaneous users	P_{DC}	power consumption
K	number of sub-array antenna elements	P	power consumption of component or module in this model
M	number of RF chains in the architecture	P_{TOT}	total power consumption
G	gain	P_{TOT_U}	per-user optimal power consumption
L	loss		

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Chapter 1

Introduction

This chapter lays out the background and context of this thesis. The need for an improved power consumption model for 5G base station beamforming schemes and antenna topologies is motivated and the relevance of the project is highlighted in Section 1.1. The research goals, scope and novel contributions of this thesis are briefly enumerated in Section. Finally, the structure of this thesis is outlined in Section 1.4.

1.1 Background, Motivation and Relevance

1.1.1 Background

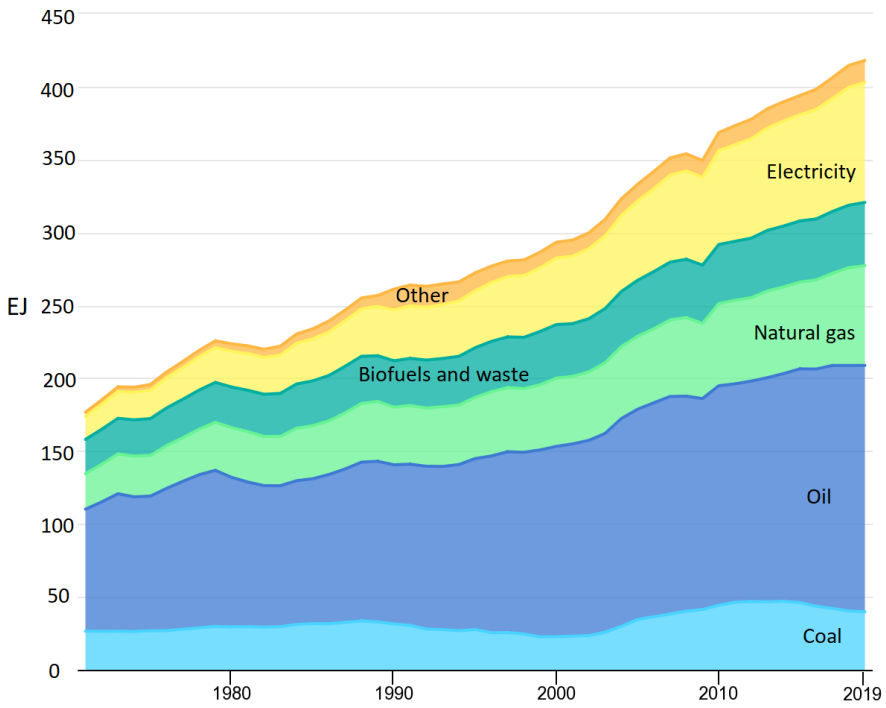


Figure 1.1: World total power consumption in exajoules [8]. Heat, solar thermal and geothermal are grouped in 'Other'.

We are living in a time when the generation, management and use of energy have become a central concern across all disciplines and industries. Over the last two decades, the global

annual energy consumption has increased by nearly 142%, from around 293 EJ in 2000 to approximately 418 EJ in 2019 (Figure 1.1). As a consequence, we are now facing the predicament of an accelerating climate crisis and a rapidly depleting fossil fuel reserve. This phenomenon is taking place at the same time as the worldwide shift from supply-driven energy sources such as coal and oil, towards more volatile, demand-driven renewable energy sources, wherein a priori knowledge of the energy demand is often required to optimise the use of energy. Hence, energy consumption estimation has become a critical decision factor in both, technical design and policy-making.

Of particular interest is the telecommunications industry. Mobile traffic has increased exponentially in the last decade (Figure 1.2) and is only expected to grow further, with the number of connected users in 2023 expected to be over 5.3 billion (i.e. over 65% of the global population) [9].

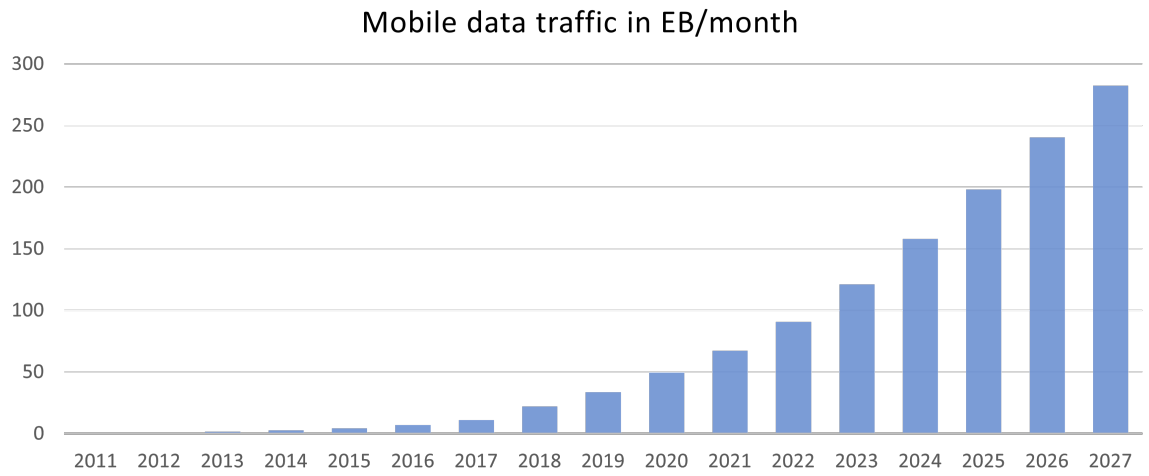


Figure 1.2: (Projected) Global mobile data traffic in exabytes per month [1]

Furthermore, the 5th Generation (5G) of mobile technology is growing faster than any other wireless access network has in the past – it is expected to carry nearly 25% of the global mobile traffic by 2025 (Figure 1.3), and nearly 60% by 2027. The 5G era heralds increased throughput requirements (Gbps) and better coverage, among other performance improvements. To meet these requirements, several techniques have been developed:

- The use of the *millimeter wave (mmW) spectrum*, featuring large bandwidths and carrier frequencies up to 300 GHz.
- The *ultra-densification* of 5G base station (BS) combined with the use of smaller coverage cells (small-cells).
- The use of *massive multiple-input-multiple-output (MIMO)* and beamforming at the transmitter to serve each user with an individual beam, as opposed to illuminating a general area with multiple users.
- *Spatial multiplexing* to serve multiple users simultaneously with the same time-frequency resources.

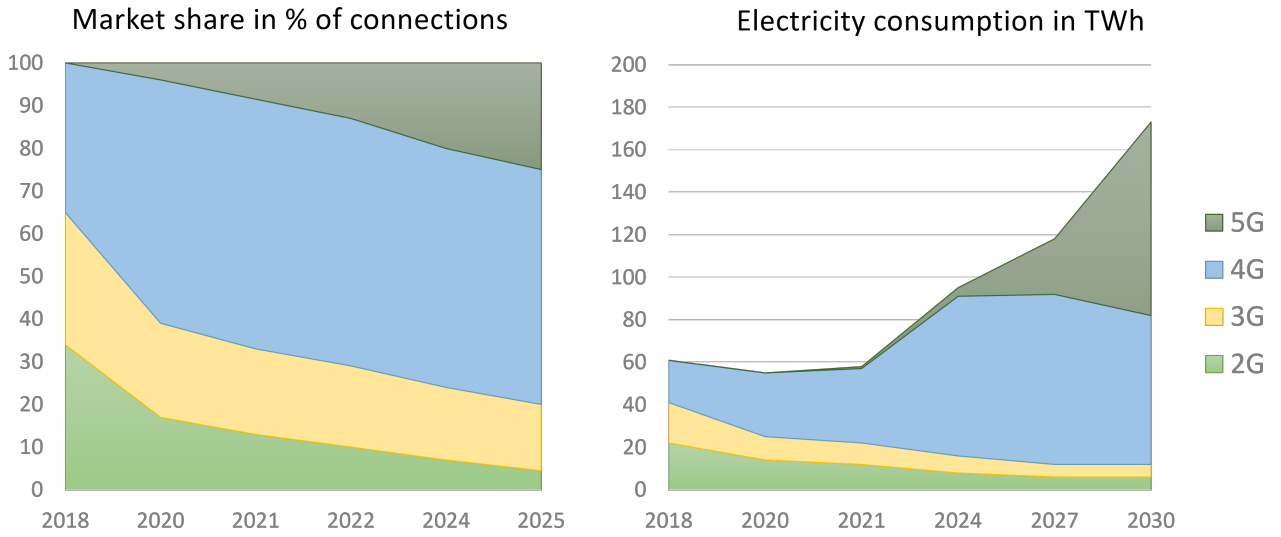


Figure 1.3: (Projected) Global market share [2, 3] and expected annual electricity demand (in terawatt-hours) [4] of wireless access networks

The growth in mobile traffic and the technological improvements related to 5G together correspond to a substantial increase in the energy consumption of the wireless access network (Figure 1.3). From 2024-2030, the total energy consumption of the wireless access networks is expected to double to over 170 TWh/year, with more than half the electricity consumption in 2030 being associated with 5G networks. Naturally, higher energy use is correlated with higher operational costs, fuel consumption and CO_2 emissions, all of which are undesirable.

1.1.2 Motivation

Despite the enormous growth of the industry, technological progress in wireless communications systems was largely focused on improving radio frequency (RF) performance, such as the radiation properties, signal-to-interference-and-noise ratio (SINR), and beamwidth. The consideration of power consumption was limited in scope to specific circuit components and implementations, and the system-level trade-offs and limitations were often not thoroughly explored. Increasing environmental concerns led to the creation of the Energy Aware Radio and Network Technologies (EARTH) project [10] in 2010, and directed special attention to the energy efficiency of a radio access network, particularly towards quantifying its power consumption in a holistic manner. An emphasis was placed on the power consumption of BSs, which are estimated to consume around 80% of the total operational power required by a cellular network. Since then, there has been increasing research interest in the power consumption estimation of 5G BS.

There are several reasons why the modelling of BS power consumption is only partially fulfilled in the literature so far. The constituent components in the BS differ based on the cost, power, size and other constraints, which make it mandatory for the power consumption model to be tailored to the specific type of BS. Additional constraints are introduced by the system's link budget requirements. Rapid improvements in semiconductor technologies and manufacturing processes must be taken into account as well, especially with regard to their compatibility with the overall system. Finally, the 5G regulations are being rolled out continuously, e.g. by the 3rd Generation Partnership Project (3GPP), and this hampers the inclusion of up-to-date reg-

ulations in the power consumption framework. These complexities and trade-offs at the system level make it a challenging exercise to model power consumption.

1.1.3 Relevance

This thesis intends to design a power consumption estimation model that takes into account the system's link budget requirements, nearly all the major components of the BS, the various types of array architectures, improvements in the state-of-the-art (SOTA), and the latest regulations. It expands upon the existing body of work by including novel use cases and parameters, and re-evaluates some of the assumptions present in the literature on this subject. Finally, it suggests optimal choices for the antenna array size, architecture, and technology to achieve the lowest power consumption under each use case.

The output of this project is relevant from several perspectives. Primarily, it provides a base for an experienced 5G designer to make decisions that consider both, performance and power. However, the results are applicable beyond 5G, as some of the architectures analysed in the project are also used in satellite communications, modern radar systems and future Terahertz systems. Accurate knowledge of the optimal system topology would help with savings in time, material, and capital required to realise the system, which is usually a cooperative effort. In the light of the current semiconductor chip crisis, the knowledge of the optimal array topology and corresponding optimal semiconductor technology can be used to more reliably estimate the number of required chips and their specifications. Having more realistic knowledge of the system's expected power consumption and optimal topology could assist the regulatory processes surrounding standardisation and deployment. Finally, the results will hopefully highlight the enduring need for energy-conscious technical design and policies.

1.2 Research Goals and Scope

1.2.1 Goals

The goal of this thesis is twofold:

1. To create a more realistic, comparative, system-level power consumption model for a BS transmitter, tailored to the enhanced Mobile Broadband (eMBB) scenario and chosen scope (see subsection 1.2).

2. To apply the model to the delineated use cases, and suggest optimal transmitter architectures choices i.e. beamforming scheme, number of constituent elements and Front End Module (FEM) technology, tailored to the chosen use case (bandwidth, number of users and transmit power).

The rest of this section briefly outlines the research scope and approach.

1.2.2 Scope

First, we focus on the dense urban eMBB case, whose Key Performance Indicators (KPIs) are shown in 1.4. We assume all users to be stationary, thereby discarding the mobility KPI.

Second, we consider a single small-cell scenario with one BS and one or more User Equipments (UEs). Several kinds of 5G small-cells are described in Table 1.1 and illustrated in Figure 1.5;

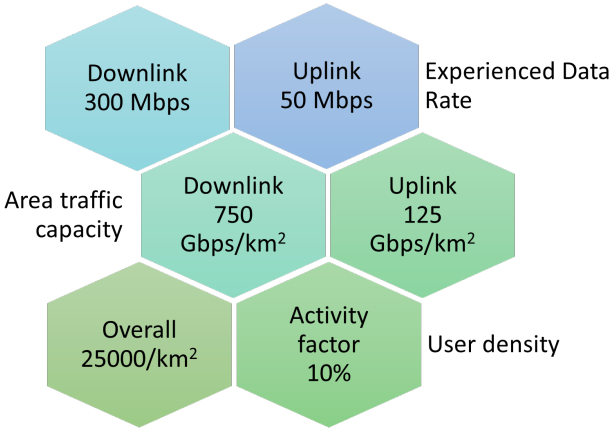


Figure 1.4: The KPIs for the dense urban mbb scenario [5], excluding the mobility indicator related to users travelling at speeds of up to 60 kmph.

note that the distinctions between them are not rigid. This thesis chooses to focus on the picocell exclusively.

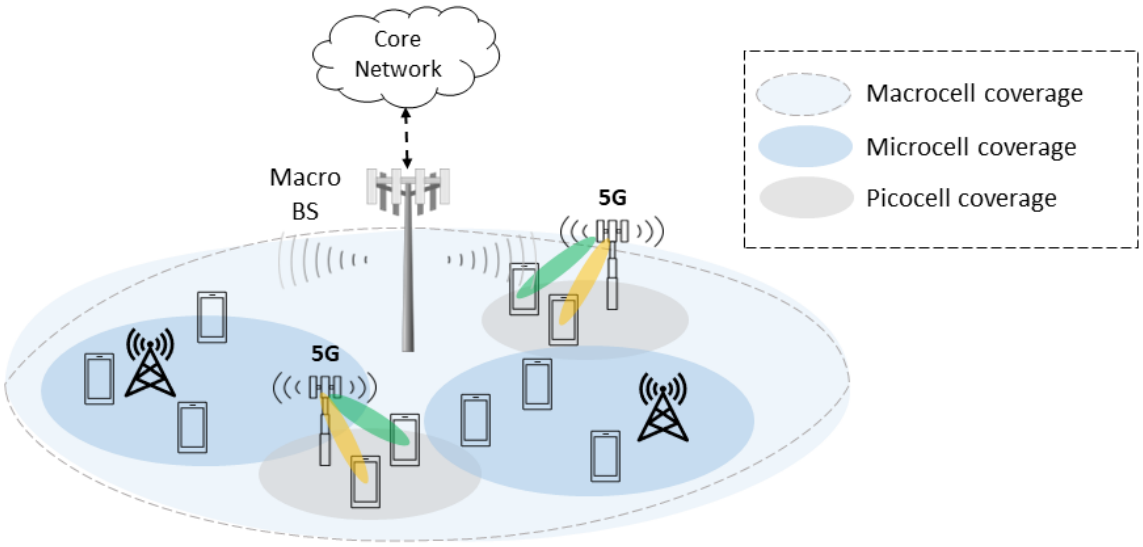


Figure 1.5: 5G small-cell illustration.

Table 1.1: 5G small-cells features [7]

Cell Type	Number of Users	Location	Radius
Femtocell	10-30	Indoor	10-100 m
Picocell	30-100	Indoor and Outdoor	100-200 m
Microcell	100-2000	Indoor and Outdoor	200-2000 m

Third, the $27.5 - 29.5$ GHz frequency band, with an operating frequency of 28 GHz, is chosen as the target frequency range, as it is a strong candidate for 5G broadband communications

[11] and also compatible with the picocell coverage area.

Fourth, it has been claimed that the transmitter accounts for the bulk of the BS power consumption [7, 12], hence we focus on the transmitter architecture at the BS, and the corresponding downlink (DL) transmission channel (from BS to UE). An in-depth consideration of the UE receiver architecture is outside our scope of analysis. Similarly, modelling the uplink (UL) channel, including pilot symbol transmission and UL channel estimation, is outside the scope of this thesis.

Fifth, we focus on the physical RF access layer. Any other layers (e.g. the network layer or the medium access control layer) are excluded from our analysis.

Sixth, concerning the baseband unit (BBU) power consumption, we consider only the power used for baseband (BB) signal computations and exclude the power consumption due to AC-DC conversion, cooling etc.

Finally, we use the 3GPP technical specifications, as per *Release 16-18* [5, 13–16], e.g. for bandwidth or effective isotropic radiated power (EIRP) specifications. Technical reports from *Release 17* and *Release 18* are currently in various stages of publication or pending approval.

1.3 Novelties

1. This project improves upon earlier power consumption models of 5G mmW beamforming architectures in the 28 GHz frequency band by incorporating additional architectures, modelling parameters, FEM technologies and up-to-date state-of-the-art.

2. The results of this project include the comparative analysis of the resultant power consumption within several use cases of bandwidth and transmit EIRP, which are in addition to the use cases in the literature.

A detailed list of the project's contributions can be found in Section 2.4.

1.4 Thesis Structure

The thesis is organised as follows.

- **Chapter 1** provides the motivation behind the thesis, defines the scope, states the research goal and shortly describes the novelty of the project.

- **Chapter 2** furnishes the reader with a brief introduction to transmitter beamforming architectures. This is followed by a review of the SOTA on power consumption models for the aforementioned architectures, and a summary of this project's contribution to the existing body of work. Lastly, the research methodology is introduced.

- **Chapter 3** lays out the first part of the power consumption model, which consists of the system-level framework. It covers the definition of use cases, the RF link budget, and high-level parametric modelling of the array topology.

- **Chapter 4** presents the second part of the power consumption model, which is the component-level framework. It dives into the individual components that form the base station transmitter and covers their unit power consumption estimation. Lastly, it presents the integrated system power consumption model.
- **Chapter 5** presents the model validation using existing analyses in the literature.
- **Chapter 6** examines and discusses the results of the model, which constitute the power consumption estimate for the various pre-defined use cases.
- **Chapter 7** summarises the main conclusions of the thesis, suggests improvements to the model, and provides direction for future work in this field.

Chapter 2

Literature Review and Proposed Methodology

This literature review begins with a description of the various types of multi-beam array architectures in Section 2.1. Next, Section 2.2 presents the literature on existing power consumption models for beamforming-based array architectures, followed by their limitations in Section 2.3. The novel contributions of this thesis to the existing literature are put forth in Section 2.4, and the research methodology used towards for purpose is explained in Section 2.5. The chapter concludes with a recap of the research goals in Section 2.6.

2.1 Base Station Multi-Beam Array Architectures

In line with the currently proposed array configurations for concurrent multiple beam generation, there are broadly three types of beamforming array architectures considered in this thesis:

- analog beamforming (ABF) [17], of which we consider an active multi-beam phased array antenna (MBPAA) scheme using (active) RF phase shifters to control multiple beams simultaneously.
- digital beamforming (DBF), of which we consider two variations:
  - digital multi-beam array (DMBA) [17], where individual antenna elements are digitally controlled through dedicated RF chains.
  - fixed sub-array-based digital multi-beam array (SDMBA) [17], where antenna elements are digitally controlled at the sub-array level.
- hybrid beamforming (HBF), which is a generic term for configurations that combine analog and digital beamforming. Examples of HBF are:
  - fully-connected hybrid array (HFC) [18], which is similar to the MBPAA architecture but with added digital control in the baseband.
  - phased sub-array-based hybrid array (HSA) [18], where antenna elements are digitally controlled at the sub-array level and steered using analog phase shifters within the sub-array.

For these architectures, in-depth explanations of their radiation patterns and RF performance can be found in the source papers. In this thesis, however, we are primarily concerned with the power consumption perspective. Illustrations of the models can be found in Section 3.5 of the System-Level Modelling chapter.

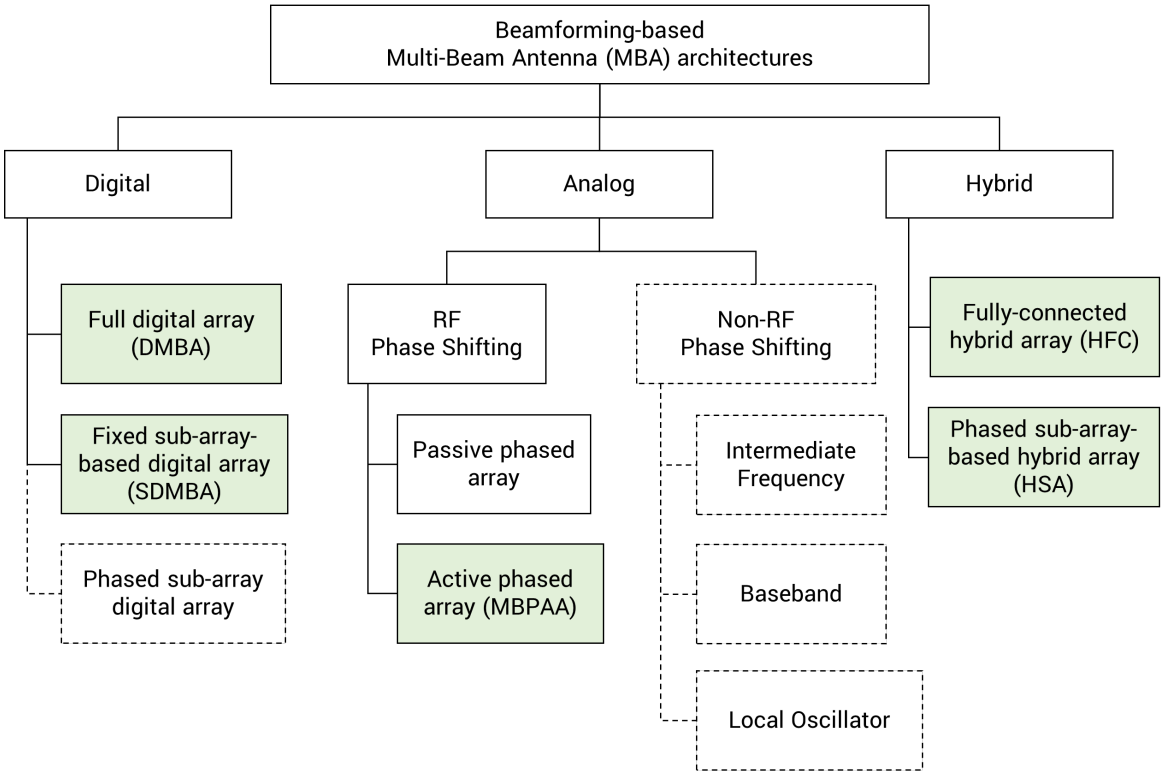


Figure 2.1: Common types of beamforming-based multi-beam architectures. The green boxes indicate the ones discussed in this thesis.

While mobile broadband systems in the pre-5G generations usually use 4-16 antenna elements, 5G massive MIMO uses arrays with 64 or more elements, while the number of RF chains and other circuit components varies based on the beamforming architecture.

2.1.1 Analog beamforming

Conventional analog beamforming used a single RF chain and was the most cost- and energy-efficient, but could only generate a single beam at a time (or two concurrent beams in the case of dual-polarisation [7]), and was therefore of limited use in the 5G eMBB scenario, where spatial multiplexing with multiple beams is often required. Analog multi-beam antenna transmitters using RF phased arrays were later developed for directional transmission in (traditional) mmW systems [19]. In this scheme, at least as many RF chains are needed as the number of independent beams i.e. the minimum number of RF chains is limited by the beams (channels) that can be simultaneously generated. A recent implementation of ABF at 28 GHz is [20], which uses a

64-element array to achieve a 10 Gbps link in a single beam at a distance of 300 m. Compared to the conventional single-user ABF scheme, MBPAA can quickly grow in complexity and cost as the number of users increases.

2.1.2 Digital beamforming

In contrast, digital beamforming makes use of a large number of antennas to achieve spatial multiplexing and multi-stream transmission to serve several users simultaneously. Multiple beams can be controlled digitally in the elevation and azimuth planes. [21] presents the first fully-digital DBF implementation targeted toward 5G eMBB standards. The 64-channel 2D array operates at 28 GHz, with a 500 MHz bandwidth. In the multi-user (MU) massive MIMO scenario, it can deliver 20 data streams to eight 4-channel UEs, thereby reaching a peak data rate of 50.73 Gbps; for a single-user case, it delivers 2 data streams to achieve a steady 5.3 Gbps data rate.

Unfortunately, at mmW frequencies, the increased digital processing power and the large number of analog/digital converters in DBF could lead to prohibitive costs and power consumption levels [22]. Furthermore, the transceiver in [21] is composed of field programmable gate array (FPGA) circuits as opposed to optimised application-specific integrated circuit (ASIC), and remains the only reported fully-digital beamformer today. While both FPGA and ASIC have their advantages [6], the power consumption of FPGA is certainly not comparable with the prevalent phased-array systems. The commercially available monolithic RFSoC from Xilinx [23] offers integrated data conversion and removes the need for power-hungry FPGA-to-Analog interfaces; the optimal configuration, though, would be a custom ASIC with more advanced data conversion systems [24]. Custom ASICs for DBF are still a fairly new concept [25].

2.1.3 Hybrid beamforming

The apparent disadvantages of DBF eventually led to an interest in the development of HBF, which combined the flexibility and multi-stream capabilities of DBF with the lower implementation complexity and power consumption of ABF [26]. A consolidated list of reported developments in HBF up to 2015 is provided in [27]. More recently, the spectral efficiency (SE) and energy efficiency (EE) of HBF schemes, particularly fully-connected and sub-array hybrid beamforming, have been extensively explored in [22], [28], and [18], but mainly from a signal processing optimisation perspective. The performance and power differences between phase shifter (PS)-based and switch-based hybrid schemes were covered in [29]. However, there are a limited number of implementations of either type of hybrid architecture, particularly for HFC implementations with more than 8 antennas [6].

The SDMBA architecture in a general form has been discussed in [17]. In this implementation, digital beamforming is used to control the beam in the azimuth plane, while the beam is fixed in the elevation plane by the architecture. The simulated beam pattern of SDMBA in [17] suggests that it may only be useful for small angular scanning ranges. A prototype of this architecture was developed in recent years at the TU Delft [30] [11], which nevertheless supports wide-angle scanning of $\pm 60^\circ$ in azimuth.

Other types of beamforming-based architectures theoretically exist, such as lens-based architectures [31], switch-based architectures [29], and architectures based on the use of the spread spectrum [32]. However, these have been excluded from this thesis due to a lack of implementation details in the literature, particularly for multi-beam scenarios.

2.2 Power Consumption Models

As mentioned earlier, previous research in 5G applications was focused mainly on the enhancement of the RF performance; nonetheless, the ultra-densification aspect of 5G, combined with the elevated demands from a large number of simultaneous users, necessitates the enhancement of the BS EE in order to directly lower the cost and environmental impact of the network [7, 12]. Rising interest in energy-efficient massive MIMO-based 5G networks has led to the exploration of several avenues for EE-maximisation. [19] gives suggestions for designing EE massive MIMO-based 5G networks, such as scaling the number of BS antennas and the use of heterogeneous networks. [33] provides a recent survey of trends and open issues addressing the EE of 5G networks, with suggestions like improved BS architectures, caching, and optimal resource allocation via machine learning.

The advantages of HBF led to a preconception that HBF is always more energy-efficient than DBF. However, previous studies on the power consumption of beamforming schemes did not take all array components into account [34]; furthermore, many of these studies used legacy, energy-inefficient digital-to-analog converter (DAC) technology in their models [34]. The above-stated preconception was recently challenged by [34] and [6], who found that not only could DBF outperform HBF in select scenarios, but also that improvements in the state-of-the-art would demand a fresh look at the comparative power consumption analysis of different beamforming schemes.

On top of that, the trade-off between RF performance and power consumption in 5G systems is highly dependent on the specifics of the end-to-end implementation and use case. Due to a large number of permutations in 5G system configurations related to the various (a) bandwidths, (b) transceiver architectures, (c) number of simultaneous beams, (d) FEM technologies and (e) transmit power, any realistic power consumption model comparing several different beamforming architectures needs to be tailored to the desired scenario.

The remainder of this section presents the main contributions of the existing frameworks in the literature that study the power consumption of beamforming-based array architectures for 5G applications.

One of the earliest power consumption models to compare ABF and DBF is found in [32]; however, it neglected BB digital signal processing (DSP) power consumption and was targeted to a different use case than eMBB.

The impact of **antenna scaling** on power consumption was explored in [6, 7, 29], where it was found that an optimal point for the lowest power consumption exists for ABF, DBF and HBF schemes when the number of antenna elements is large enough. [7] laid out an 8-step methodology for mmW transmitter system sizing to find the optimal power consumption, and applied it to the eMBB pico-cell use case for 28 GHz transceivers. Figure 2.3 shows the resultant optimal total power consumption as computed by [7]: 93.9 W with 135 antenna elements

for MBPAA, and 54.5 W with 220 elements for DMBA.

[26] investigated how the number of **spatially-multiplexed users** impacted the trade-off between HBF and DBF, while also including more complete modelling of the DSP power consumption. They presented the specific scenarios where fully-digital schemes are preferable over hybrid schemes, albeit for the 60 GHz scenario.

[35] looked into how the transmitter system parameters and constraints on service quality affected the *average* **EE-per-BS** in a multi-cell network, albeit with a simplistic power model.

The **SE-EE trade-off** of array architectures has been a topic of interest in power consumption modelling. [22] attempted jointly optimising the SE and EE for HBF transmitter architectures using a simple power consumption model, and found that optimal 'green points' exist where maximum EE is achieved. A similar SE-EE joint analysis for receiver architectures by [34] found that when the power consumption model accounted for all mmW components (as opposed to just analog/digital converters), the margin by which HBF outperformed DBF was narrow and very fragile. They claimed it could be easily overturned by sota improvements in analog-to-digital converters (ADCs), or when there is any mismatch between the channel rank and the number of RF chains built in the array architecture.

As the ADC/DAC **quantisation** has a significant influence on the system power consumption, the effect of bit-width optimisation was investigated in [36], although they focus on a single-beam case.

Until recent years, energy efficiency evaluation models for cellular networks, particularly for the BS, used to consider transmission power consumption as dominant and the DSP computational power as a small fixed constant (sometimes even 0 W [32]). However, while the densification of small-cells as part of the 5G network has led to a drop in the transmission power, the **DSP computation power** has simultaneously increased. A preliminary analysis in 2017 of the massive MU massive MIMO scenario showed that the total BBU power consumption of a 5G small-cell BS could approach 800 W in high-volume traffic [12]. While EE enhancement techniques such as caching and improved signal processing algorithms are likely to reduce the BBU's DSP power consumption going forward, it is still necessary to have an accurate representation of the computational power consumption of different array architectures today for them to be fairly compared.

In [12], the authors investigated the impact of varying the array size and signal **bandwidth** on the BB unit computation power of a 5G small-cell BS. However, [12] only looked at DBF, and they did not sufficiently take mmW effects into account. [26] presents a more recent study where they compared the estimated DSP power consumption for DBF, HFC and HSA schemes in a single-input-single-output link for the 60 GHz scenario. It was seen that for a large number of simultaneous users (e.g. 32) DBF had better EE compared to HBF due to the *per-user* processing increasing drastically in the hybrid schemes with the number of users.

So far, the only comprehensive analysis for the 28 GHz eMBB scenario for transmitter architectures is [6], wherein the authors compared the trade-offs between system capacity, power consumption and IC area for the DBF, HSA and HFC architecture. Their model included analog processing power and digital computation power, and concluded that DBF has the low-

est power consumption, which then decreases further with an increase in spatial multiplexing. Figure 2.2 shows the breakdown of power consumption at the BS as computed by [6], with varying numbers of antenna elements and spatially-multiplexed users.

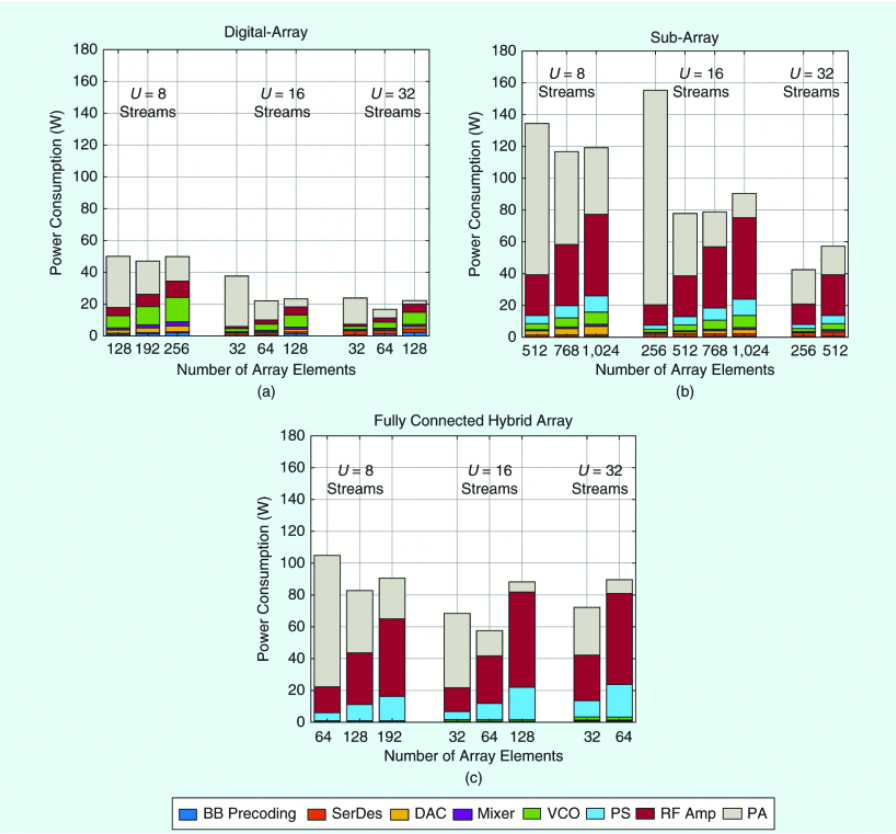


Figure 2.2: Power consumption analysis from [6] for DMBA ('DBF', top left), HSA (top right) and HFC (bottom) operating in the eMBB use case at 28 GHz, with 850 MHz bandwidth and at 100m distance.

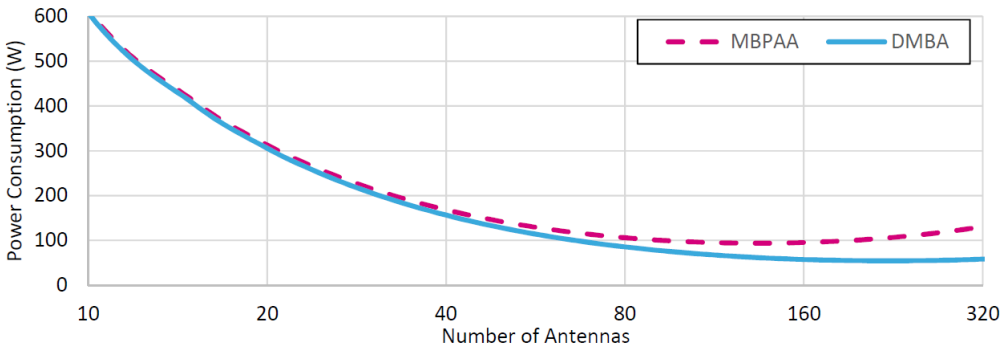


Figure 2.3: Power consumption analysis from [7] for MBPAA and DMBA architectures operating in the eMBB use case at 28 GHz, for 67 users, 100 MHz bandwidth and at 200m distance.

2.3 Limitations of Existing Models

Unfortunately, there are several shortcomings of existing power consumption estimation frameworks. Firstly, it is common that only the power consumption of ADCs/DACs and power amplifier (PA) was taken into account, and other components with non-negligible power signatures (for e.g. signal splitters/combiners, loss compensation amplifiers) were excluded [34].

Secondly, due to the fast-moving technological developments in semiconductor technologies and signal processing, there exists a large gap between the SOTA and some of the existing power consumption models [7, 26]. For example, although the technology for analog/digital converters has come a long way in terms of their EE, some older power consumption models still use legacy converters' power figure of merit (FOM) values in their computations, which makes them overestimate the power consumption of the DBF scheme [34].

Thirdly, many models operate under the initial assumption that HBF has better EE than DBF, which has recently been challenged [6, 34]; nevertheless, the assumption leads them to evaluate HBF against an ideal full-precision DBF scheme as opposed to the more practical, carefully quantised low-bit DBF architecture. The optimal number of bits is an open research question.

Fourthly, the DSP module's power consumption is assumed to be very small or even negligible similar to the pre-5G BS models [7, 32, 34], whereas this assumption is not valid for 5G small-cell BSs.

Finally, even the most extensive analysis for our use case of eMBB at 28GHz, which is furnished by [6], falls short of complying with the most recent 3GPP RF link budget requirements. For instance, key differentiating aspects in this model are the large 850 MHz bandwidth and the use of a *variable* per-beam EIRP; this deviates significantly from the maximum bandwidth of 400 MHz and the *fixed* per-beam EIRP proposed in the 3GPP regulations. It is therefore difficult to extend the model's results to practical 3GPP-based use cases. Hence, an updated model is required that is in line with the latest regulations.

These limitations make a strong case for an up-to-date and more extensive power consumption framework for beamforming schemes under the 5G eMBB use case, with improved transmitter topology modelling and considering the RF performance trade-off.

The Tables 2.1-2.2 summarise the literature on power consumption modelling for 5G beamforming-based antenna arrays. Table 2.1 presents the models' system-level scope, use case and main limitations, while Table 2.2 shows the component-level choices, including a breakdown of which components of the 5G transmitter and receiver were explicitly included in the modelling.

2.4 Contributions

This thesis aims to make the following contributions to the existing body of work:

1. It extends previous work on the power consumption modelling and analysis of 5G mmW beamforming architectures in the 28 GHz band by

   (a) including additional architectures in each analysis.

(b) including a more complete set of circuit components in the model.

(c) expanding the set of use cases under analysis.

(d) Aligning the model with the latest 3GPP standards, such as the recently proposed EIRP and bandwidths.

(e) using up-to-date sota for all components.

2. Based on the above, this study recommends optimal transmitter architectures (beamforming scheme, number of constituent elements and the like) tailored to the use case (EIRP, bandwidth and number of users).

3. To the best of the author's knowledge, this is the first power consumption analysis of the SDMBA architecture.

These contributions can be compared to the existing literature in Tables 2.1-2.2.

2.5 Proposed Methodology

Figure 2.4 illustrates the proposed methodology for the development, validation and evaluation of the power consumption model in this thesis.

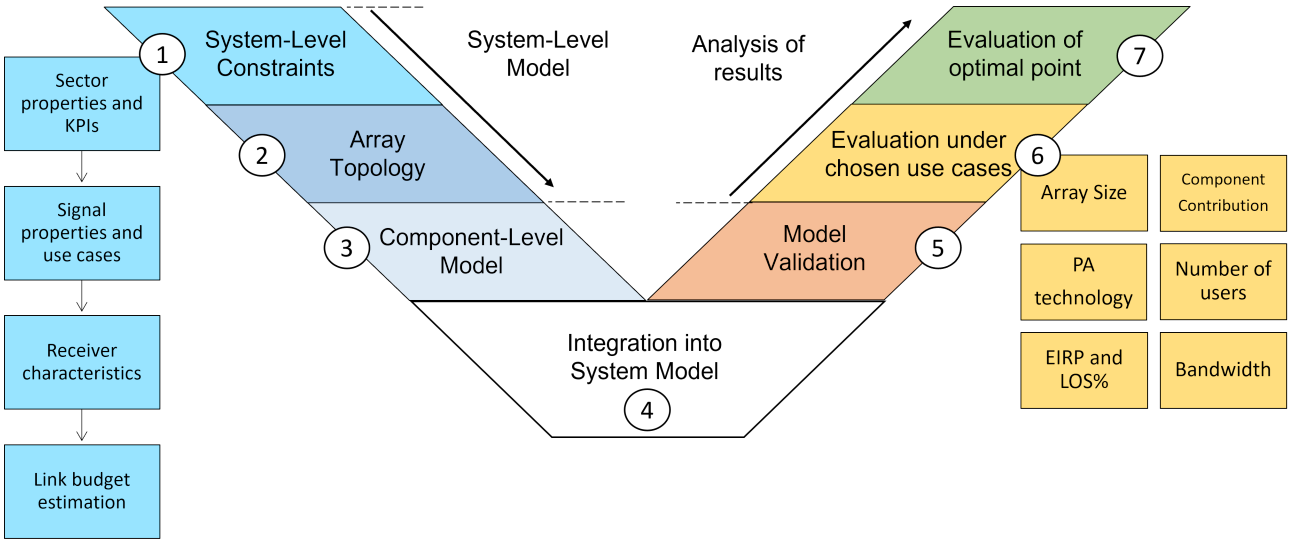


Figure 2.4: Thesis Methodology

2.6 Conclusion

In this chapter, the state-of-the-art in power consumption models for beamforming architectures, along with their limitations, were discussed. A summary of the power consumption models is presented in Tables 2.1 and 2.2.

The literature highlights the need for an up-to-date power consumption framework for 5G multi-beam antenna topologies and beamforming schemes, with improved transmitter topology modelling and considering the RF link budget performance trade-off – specifically for the

eMBB scenario and tailored to various use cases of bandwidth, transmit power, semiconductor technology, and the number of simultaneous users. This thesis aims to fulfil that need.

Table 2.1: Summary of scope, use cases & main limitations of surveyed 5G array power consumption models.

Ref.	Tx/Rx	Topologies considered	Operating Frequency	Bandwidth	Cell Radius	Number of cells	Number of users	LOS/ NLOS	Propagation Channel Model	Model's Main Limitation
[22]	Tx	HFC, HSA	$<$ 6 GHz	20 MHz	-	-	-	-	Only pathloss provided as -100 dB	Simplistic
[32]	TRx	MBPAA, DMBA	28 GHz	500 MHz	femto	single	1	both	2-tap Rayleigh fading-channel	Assumes 0 W BB DSP power, low order modulation schemes
[29]	Rx	HFC, HSA (PS, switch-based)	60 GHz	500 MHz	-	-	1-4	-	Narrow-band mmW clustered channel from [37][38] [39]	Incomplete modelling of losses
[34]	Rx	(1 beam) PAA, DMBA, HFC	$>$ 30 GHz	1 GHz	-	-	1	both	Small-scale fading mmW 28 GHz channel from [40]	Superficial modelling of losses and DSP power, analysis cannot be extended to Tx
[6]	Tx	DMBA, HFC, HSA	28 GHz	850 MHz	pico	single	8-32	LOS	Flat fading 3GPP model channel [?]	Not end-to-end optimised
[7]	Tx	MBPAA, DMBA	28 GHz	100-250 MHz	pico	single	1-67	both	NYUSIM 2.01	Large gap between proposed model and SOTA, superficial modelling of DSP power
[26]	TRx	DMBA, HFC, HSA	60 GHz	1.76 GHz	pico	single	2,4	LOS	Quasideterministic WLAN channel	Large gap between proposed model and SOTA
[36]	Rx	(1 beam) PAA, DMBA	28 GHz	380 MHz	-	-	2	-	-	Analysis cannot be extended to Tx
[35]	Tx	DMBA	$<$ 6 GHz	20 MHz	pico	multiple	0-80	-	Block Rayleigh-fading channel	Simplistic
This Work	**Tx**	**MBPAA, DMBA, HFC, HSA, SDMBA**	**28 GHz**	**100-400 MHz**	**pico**	**single**	**2-32**	**both**	**3GPP UMi C.I model** [41]	

Table 2.2: Design choices & included components in the surveyed 5G array power consumption models with LG = legacy, SOTA = state-of-the-art, FL = future-looking, COM = commercial

Ref.	Front End Module			RF Chain					Analog		Digital Signal/ Processing		Other
	Switch	Filter	PA technology	LO/ Mixer	DAC Type	DAC ENOB	ADC Type	ADC ENOB	PS	Splitter/ Combiner	Precoding	FFT/IFFT	
[22]													
[32]			40nm CMOS [42]		COM [43]	16	COM [44]	12					Assumes 0 mW BB processing power
[29]	✓	✓	*N/A*	✓			FL	$>$ 4	✓		*N/A*		BB amp. [45]
[34]		✓	*N/A*	✓			LG, SOTA, FL	1,2 ... 8	✓	✓			BB amp. considered
[6]		✓	GaAs [46]	✓	SOTA [47]	8	*N/A*	*N/A*	✓	✓	✓	✓	SerDes: Rx [48], Tx [49]
[7]	✓	✓	45nm SOI [50]	✓	SOTA [51]	8			✓	✓			
[26]		✓	class-A CMOS	✓	COM [52]	7	SOTA [53] [52]	10 (DBF), 12 (HBF)	✓	✓	✓	✓	
[36]		✓	*N/A*	✓	*N/A*	*N/A*	*N/A*	4 (DBF), 8 (HBF)	✓		*N/A*	✓	
[35]			Only η_{PA} provided [54]								✓		
This Work		✓	**Bulk CMOS, GaAs, CMOS SOI, SiGe, GaN**	✓	**Modelled**	**8**	-	-	✓	✓	✓		**Hierarchical RF amplifiers**

Chapter 3

Model: System-Level

This chapter presents the first, system-level part of the developed power consumption framework, and covers steps 1 and 2 of the thesis methodology. System-level constraints are elaborated in Sections 3.1-3.4. This is followed by the array topology sizing in Section 3.5.

3.1 Sector Properties and KPIs

Our system operates in the 28 GHz FR2 band, for which the following 3GPP standards have been described as of *Release 18* [5]:

- Maximum user density: 25000 users/km^2
  This is consistent with very large urban settings, such as Paris and Mumbai.
- Maximum DL area throughput: 750 $Gbps/km^2$
- Ratio of simultaneously active users: 10%

As mentioned in the research scope (Section 1.2), we assume a single picocell scenario with 3 sectors and the BS in the centre. The cell radius is defined as the maximum distance between the BS and a UE (user) being served by that BS. To simplify the model, we assume that the picocell is circular with a radius of $d_{CELL} = 100$m (Table 1.1), and the UEs are uniformly distributed along the cell circumference such that the distance between the BS and any UE, denoted by d_{UE}, is

$$d_{UE} = d_{CELL} = 100\text{m} \tag{3.1}$$

For simplicity, the radial beamwidth coverage i.e. the distinction between the 'inner' and 'outer' radius is not considered in this thesis.

We define the intersite distance ISD as the distance between two adjacent BSs. In order to minimise the interference between them, the ISD is related to the cell radius as

$$ISD = 2 \cdot d_{CELL} \tag{3.2}$$

Since we have a single-cell scenario, the ISD is mainly used to translate the 3GPP requirements from an areal density basis to a per-cell or per-sector basis. By setting the $ISD = 200$m, we get a cell density of 25 cells/km^2, and consequently, the maximum number of UEs is

$$\begin{aligned} U_{max_{CELL}} &= \frac{25000 \text{ users}/km^2}{25 \text{ cells}/km^2} \cdot 10\% = 100\text{users/cell} \\ U_{max} &= 33 \text{ users/sector} \end{aligned} \tag{3.3}$$

Furthermore, we can derive the maximum data rate per cell based on the 3GPP standards of areal throughput.

$$R_{max_{CELL}} = \frac{750 \text{ Gbps}/km^2}{25 \text{ cells}/km^2} = 30\text{Gbps/cell}$$
$$R_{max_{SECTOR}} = 10 \text{ Gbps/sector} \tag{3.4}$$

The derived sector properties are summarised in Table 3.1.

Parameter		Value	Unit
f_c	Centre frequency	28	GHz
-	Frequency band	26.5-29.5	GHz
d_{CELL}	Cell radius	100	m
d_{UE}	UE-distance (BS to UE)	100	m
ISD	Intersite distance (BS to BS)	200	m
$R_{max_{SECTOR}}$	Max. throughput per sector	10	Gbps
U_{max}	Max. users per sector	33	-

Table 3.1: Sector properties

3.2 Signal Properties and Use Cases

Having set up the per-sector properties, we now focus on the signal properties, which apply to each independent beam i.e. each user. The proposed model considers the following signal properties: bandwidth BW, data rate per user R_{user}, coding rate C_R, QAM-modulation order M_O and the signal-to-noise ratio (SNR) required to achieve the data rate SNR_{req}.

Let us denote the number of simultaneous users (per sector) as U. We choose a range of U based on U_{max} as follows:

$$U = [2 \quad 4 \quad 8 \quad 16 \quad 32] \text{ users} \tag{3.5}$$

The 3GPP standards specify 3 possible values for the bandwidth BW which are

$$BW = [100 \quad 200 \quad 400] \text{ MHz} \tag{3.6}$$

Therefore, based on the choice of bandwidth, three 'use cases' can be defined, each with a specified value of BW, R_{user}, SNR_{req}, M_O and C_R. In addition, since the signal bandwidth covers a fairly wide frequency range, the system becomes noise-limited, instead of interference-limited [7]. Consequently, we assume the SINR to be equivalent to the SNR_{req} in our analysis.

Under the condition of no modulation or encoding, the per-user transmit signal data rate R_{user} is bounded below and above as

$$R_{user} = \frac{R_{max_{SECTOR}}}{U} \in (300, 1250) \qquad \text{for } U = 32, 8 \tag{3.7}$$

Property		Case 1	Case 2	Case 3	Unit
BW	Bandwidth	100	200	400	MHz
R_{user}	Data rate per user	300	780	1090	Mbps
SNR_{req}	SNR Required	8.5	11.45	7.51	dB
M_O	Modulation Order (QAM)	16	64	64	-
C_R	Coding Rate	0.754	0.650	0.455	-

Table 3.2: Use cases based on signal properties.

The data rate and bandwidth are related through the Shannon-Hartley theorem as

$$\begin{aligned} R_{user} &= BW \cdot \log_2(1 + SINR) \\ &= BW \cdot \log_2(1 + SNR_{req}) \end{aligned} \tag{3.8}$$

A variation of the theorem can be used to relate the signal's coding rate C_R and QAM-modulation order M_O to the data rate as

$$R_{user} = BW \cdot C_R \cdot \log_2(M_O) \tag{3.9}$$

Finally, together with the Modulation and Coding Scheme (MCS) index table for FR2 frequencies [55], Equations 3.7-3.9 are used to find feasible permutations of C_R and M_O, while taking into account the following trade-offs:

- The data rate R_{user} is preferably higher to improve performance and user experience.
- The modulation order M_O is preferably higher, to increase the user data rate R_{user}.
- The coding rate is preferably lower, to increase signal reliability.
- The required SNR SNR_{req} is preferably lower, to manage the technological requirements.

The use cases are tabulated in Table 3.2. It is interesting to note that the required SNR for case 3, which has a higher data rate, is in fact lower than the required SNR for case 2. This is achieved by appropriately changing the coding rate C_R within the MCS framework.

Not every use case applies to every value of U, due to the upper bound on the data rate given by $R_{max_{SECTOR}} = 10$ Gbps. For example, for $U = 32$ and $R_{user} = 300$ Mbps, the total data rate per sector is

$$R_{SECTOR} = 32 \text{ users/sector} \cdot 300 \text{ Mbps/user} = 9.6 \text{ Gbps/sector} < R_{max_{SECTOR}}$$

which makes case 1 feasible for 32 users. On the other hand, if $R_{user} = 780$Mbps,

$$R_{SECTOR} = 32 \text{ users/sector} \cdot 780 \text{ Mbps/user} = 24.96 \text{ Gbps/sector} > R_{max_{SECTOR}}$$

which makes case 2 infeasible for 32 users. Feasible use cases are described in Table 3.3.

U \ Use Case	Case 1	Case 2	Case 3
2	✓	✓	✓
4	✓	✓	✓
8	✓	✓	✓
16	✓	✓	
32	✓		

Table 3.3: Feasible use cases based on the number of users U.

3.3 Receiver Characteristics

The receiver can be assumed to be a UE device with an integrated phased antenna array of $N_{RX} > 1$ antenna elements. To simplify the model, we assume that each UE receiver contains a single RF chain, which implies that at any instance, it can only process a single data stream. From the 3GPP agreements in [15], the UE can be assumed to have a single antenna panel with $N_{RX} = 4$.

Based on the signal properties, the required SNR at the receiver is given by SNR_{req}. However, there is a degradation of the SNR due to the receiver circuitry, which can be expressed by the receiver noise factor (NF).

For simplicity, the UEs are considered point objects along the radial direction. In other words, beamwidth considerations in the radial direction are excluded from the system-level model.

3.4 Link Budget Estimation

In this section, the link budget is estimated to express the required power at the transmitter P_{TX}, and the associated per-beam $EIRP$. The $EIRP$ is bounded below, so as to achieve the desired SNR_{req} at the UE receiver. At the same time, the per-beam $EIRP$, together with the number of transmit antennas, determines which type of technology can be used in the transmitter's the FEM.

3.4.1 Propagation Channel and Signal-Specific Losses

One of the goals of this thesis is to align the power consumption model with 3GPP specifications, which encompasses the choice of the propagation channel model.

The 'close-in (CI) free space reference distance' channel model is a well-performing candidate model for 3GPP standards, and has been derived in [41] for a typical urban microcell (UMi) deployment, based on ray tracing results and measurements. It incorporates the path loss and shadow fading loss, as well as line-of-sight (LOS) probability for typical scenarios.

We consider two types of signal-specific losses: the frequency-dependent path loss PL, and the bandwidth-dependent thermal noise N_{AWGN}. The path loss depends on the centre frequency f_c, the type of channel, and the distance d_{UE}. The thermal noise depends on the

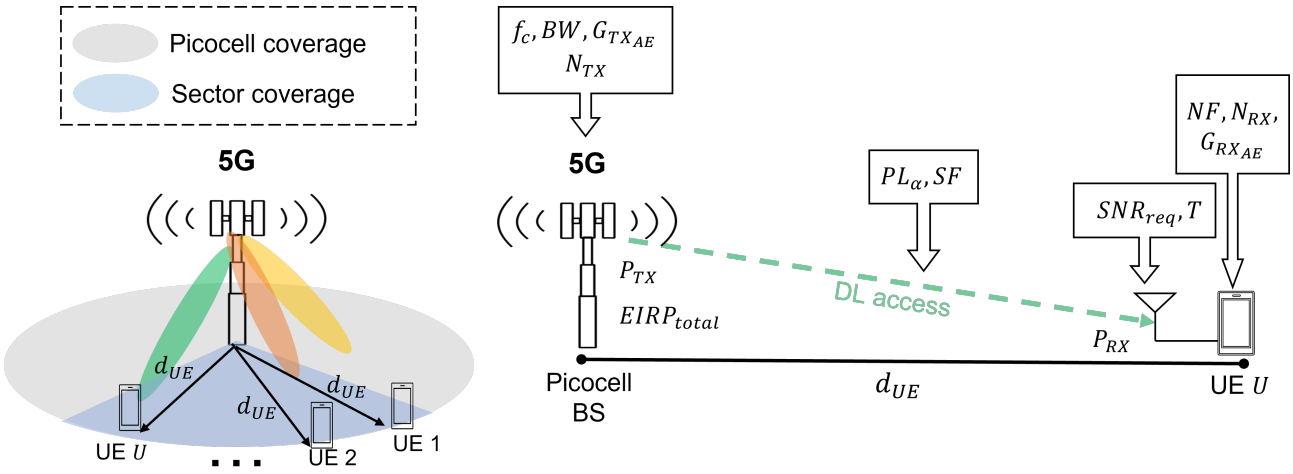


Figure 3.1: Left: The blue region shows 1 of the 3 sectors constituting a picocell. There are U UEs situated along the sector (cell) edge. Right: Illustration of link budget per UE, where P_{TX}, P_{RX} and $EIRP_{TOTAL}$ are derived.

bandwidth BW and the temperature T.

$$PL[dB] = 20\log_{10}\left(\frac{4\pi f_c[Hz]}{c[m/s]}\right) + PL_\alpha \cdot 10\log_{10}(d_{UE}[m]) + SF \tag{3.10}$$

$$N_{AWGN}[dB] = 10\log_{10}(k_B \cdot T[K] \cdot BW[Hz]) \tag{3.11}$$

where PL_α is the channel-dependent path loss coefficient, SF is the channel-dependent shadow-fading loss, c is the speed of light and k_B is the Boltzman constant ($1.38 \cdot 10^{-23} m^2 kgs^{-2} K^{-1}$). The path loss can vary considerably between LOS and non-line-of-sight (NLOS) links. For the eMBB scenario, it is expected that most of the BS-UE links are line-of-sight links, especially when $U \leq 32$ as in our model [6]. However, practically, as the number of users increases, we can expect some of them to be outside the line of sight. In our proposed model, for 16 or more simultaneously connected UEs, we consider an additional alternative scenario where a non-zero percentage of users have an NLOS link.

3.4.2 Required Transmit Power

The transmitter array gain G_{TX} and receiver array gain G_{RX} are expressed as

$$G_{TX}[dB] = G_{TX_{AE}}[dBi] + 10\log_{10}(N_{TX}) \tag{3.12}$$

$$G_{RX}[dB] = G_{RX_{AE}}[dBi] + 10\log_{10}(N_{RX}) \tag{3.13}$$

where $G_{TX_{AE}}$, $G_{RX_{AE}}$, N_{TX} and N_{RX} are the transmit antenna element gain, receive antenna element gain, number of transmit antenna elements, and number of receive antenna elements respectively. The power at the receiver P_{RX} can be expressed as the sum of the required SNR at the receiver, and the noise factor NF of the receiver, i.e.

$$P_{RX}[dBm] = SNR_{req} + NF \tag{3.14}$$

Finally, by combining Equations 3.10-3.14, we express the link budget of the system as

$$EIRP[dBm] = P_{RX} + N_{AWGN} + PL - G_{RX} + 30 \tag{3.15}$$

where the factor of 30 is added as a conversion factor from dBW to dBm.

When extending the link budget to a multi-user case with U simultaneous users, the total EIRP needed at the BS becomes

$$EIRP_{TOT}[dBm] = EIRP + 10\log_{10}(U) \tag{3.16}$$

Finally, from the required total EIRP in Equation 3.16, the transmit power per antenna element $P_{TX_{AE}}$ can be obtained as

$$P_{TX_{TOTAL}}[dBm] = EIRP_{TOTAL} - G_{TX} \tag{3.17}$$

$$\begin{aligned} P_{TX_{AE}}[dBm] &= P_{TX_{TOTAL}} - 10\log_{10}(N_{TX}) \\ &= EIRP + 10\log_{10}(U) - G_{TX_{AE}} - 20\log_{10}(N_{TX}) \end{aligned} \tag{3.18}$$

3.4.3 Probability of Line of Sight

The link budget in the previous section was derived assuming the probability of LOS/NLOS as 100%. However, realistically, the probability of a LOS link is a function of distance from the BS. Consequently, the EIRP per beam will vary not only based on the bandwidth, but also the LOS probability. According to the same path loss model from [41], the LOS probability at a distance of 100m from the BS is 25%. Table 3.4 shows the change in the EIRP per beam with LOS probability.

To account for NLOS links, along with other attenuating factors in the propagating transmit signal, the 3GPP proposes to use 40 dBm per beam [16]. This is high enough to encompass every Case and LOS probability outlined in Table 3.4. The link budget for each use case is summarised in Table 3.5.

Table 3.4: EIRP per beam, based on the bandwidth and probability of LOS link.

Case \ LOS%	0%	25%	50%	75%	100%
1	33.60	32.36	30.61	27.64	10.6
2	39.65	38.41	36.66	33.69	16.65
3	38.71	37.47	35.72	32.75	15.71

Table 3.5: Receiver characteristics and estimated link budget for eMBB per UE. Derived values are marked in bold.

Parameter		Value			Unit
f_c	Centre Frequency	28			GHz
d_{UE}	Distance	100			m
PLα	Path Loss Coefficient, LOS/NLOS [41]	1.85/2.89			-
SF	Shadow Fading Loss, LOS/NLOS [41]	4.2/7.1			dB
T	Temperature	298			K
NF	Receiver Noise Figure [7]	4			dB
$G_{TX_{AE}}$	Transmitter Antenna Gain [7]	3			dBi
$G_{RX_{AE}}$	Receiver Antenna Gain [15]	5			dBi
N_{RX}	Num. Receiver Antennas [15]	4			-
		Case 1	Case 2	Case 3	
BW	Bandwidth	100	200	400	MHz
SNR_{req}	Required SNR	8.5	11.45	7.51	dB
PL	**Path Loss**, LOS/NLOS	103/126	103/126	103/126	dB
N_{AWGN}	**Thermal Noise**	-123.9	-120.8	-117.8	dB
P_{RX}	**Rx Power at UE**	12.5	15.45	11.51	dB
EIRP	**Tx EIRP per beam**, LOS/NLOS	10.6/33.6	16.65/39.65	15.71/38.71	dBm

3.5 Array Topology

The five beamforming architectures considered in this thesis were briefly described in Chapter 2. In this section, we focus on the beamforming architecture and antenna array topology.

3.5.1 Composition of Beamforming Architectures

The structure, or topology, of the various 5G beamforming-based transmitter architectures consists of combinations of a few underlying functional modules, which are presented in Figure 3.2 along with their underlying components. The number of components varies based on the type of beamforming scheme (ABF, DBF or HBF), as well as a selection of RF- and application-based parameters, which are defined in Table 3.6.

Table 3.6: Basis parameters of the beamforming architectures

Parameter	Definition	Range of Values
N_{TX}	Number of transmit antenna elements	16 32 64 128 256 512
K	Number of antenna elements in a sub-array	2 4 8 16 32
U	Number of simultaneous users (beams)	2 4 8 16 32
M	Number of RF chains / independent data streams	$2 - 512$

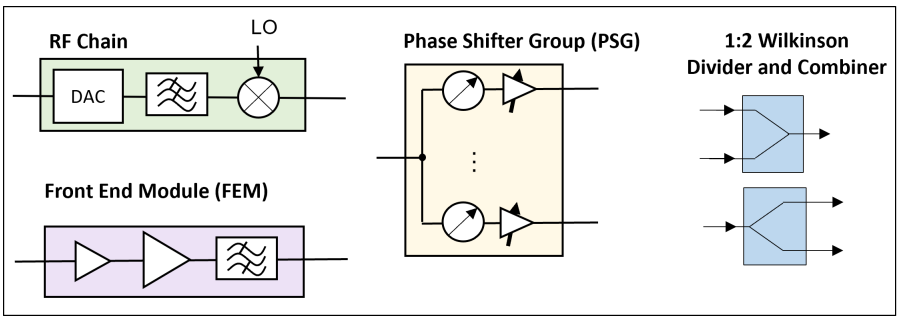


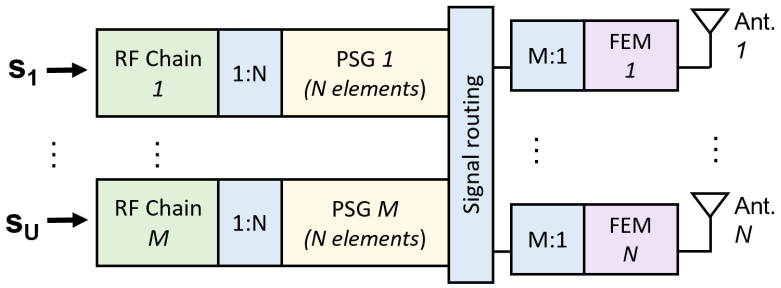
Figure 3.2: Functional modules and internal components of beamforming-based transmitter architectures

The number of RF chains M is associated with the number of independent data streams being transmit by the BS, and is bounded below by the number of users, i.e. $M \geq U$. For a multi-user setting where each UE is assumed to receive a single data stream (Section 3.3), the number of RF chains is set equal to the number of users, that is,

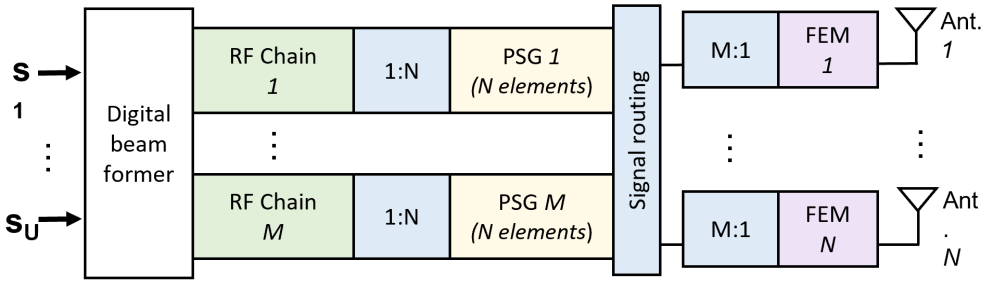
$$M = U = \frac{N_{TX}}{K} \tag{3.19}$$

This applies to all architectures except DMBA, which by nature has $M = N_{TX}$. The consequence of this assumption is that all other architectures have reduced dimensions compared to DMBA. For sub-array architectures, Equation 3.19 logically means that for a fixed value of M, any increase or decrease in array size N_{TX} appears as a corresponding increase or decrease in the sub-array size K.

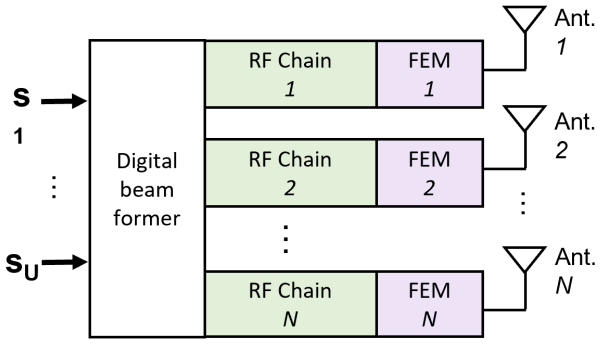
Based on these considerations, Figure 3.3 presents a high-level schematic of the five architectures, which will be used further in our power consumption framework.



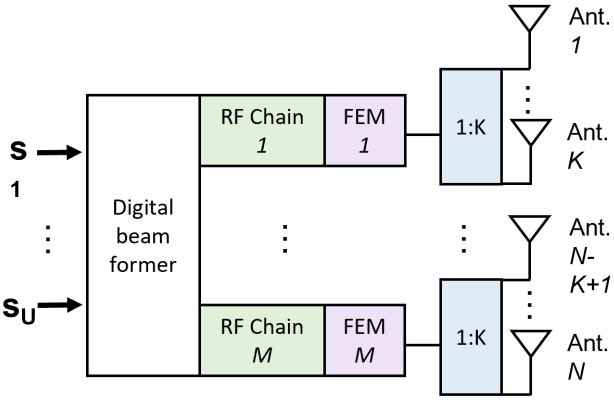
(a) Multi-beam phased antenna array (MBPAA)



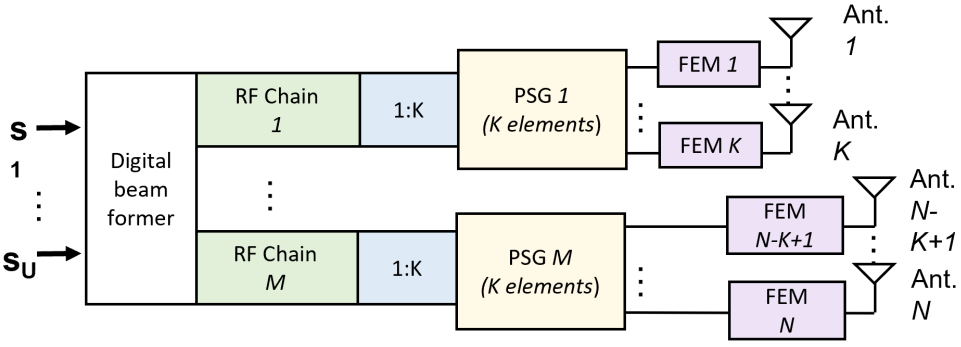
(b) Hybrid fully-connected array (HFC)



(c) Digital multi-beam array (DMBA)



(d) Fixed-subarray based digital array (SDMBA)



(e) Phased-subarray based hybrid array (HSA)

Figure 3.3: Beamforming schemes and their array topologies

3.5.2 Power Distribution and Combining

An important, but sometimes neglected, aspect of the system-level power consumption modelling is related to the signal splitting and combining losses in the architecture. This section elaborates on these losses and relates them to the system topology.

Power distribution and/or combining is present in all architectures except DMBA. The RF signal output from the RF chains must be split or combined in some way before being fed into the next component module. There is little prior work on power distribution circuits for array sizes in the massive MIMO range, hence, some models in the literature anticipate an approach that can be easily generalised. For example, the approach in [6] uses a network of common binary (1:2 or 2:1) CMOS Wilkinson Dividers/Combiners, which they have a fairly low insertion loss $IL_{WD} = 1$dB and are compatible with large bandwidths. This approach is used as a basis in the proposed model, and is thereafter optimised based on the topology.

The number of splitters needed depends on the number of antenna elements N_{TX}, RF chains M and sub-array structure K. If all other losses are neglected, the signal power of each split signal will be 3dB lower than the input signal. After passing through $n_{sp} = \log_2(N_{TX})$ splitters, the reduction in signal power compared to the source signal will be $3n_{sp}$ dB due to splitting and another $1n_{sp}$ dB due to insertion loss. For large antenna arrays or sub-arrays, this reduction in signal power may be extremely large (e.g. 20 dB for $N_{TX} = 32$ stages of splitting) and must be boosted to a reasonable level before the signal is phase shifted and combined. Relying on a single pre-splitter high-gain RF amplifier, although cost-effective, may not be feasible as it raises signal distortion concerns. Instead, cascaded RF amplifiers are used along the splitter network to compensate for the splitter loss in stages, based on the proposed structure in [6]. Figure 3.4 illustrates the splitting network and splitter amplifier distribution.

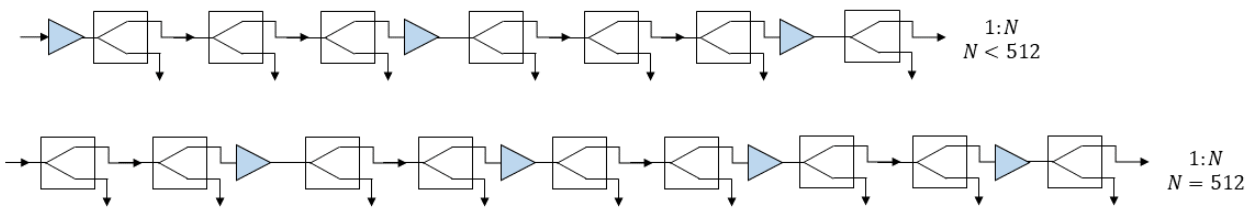


Figure 3.4: Illustration of splitting network for fully-connected architectures MBPAA and HFC. The splitting network for sub-array architectures can be constructed similarly.

The same reasoning can be applied to the combining network. When two signals from different sources are combined, there is a 3dB loss in the combiner, in addition to the insertion loss. After passing through $n_{cb} = \log_2(M)$ combiners, the reduction in signal power compared to any of the input signals will be $3n_{cb}$ dB due to splitting and another $1n_{cb}$ dB due to insertion loss. Cascaded RF power amplifiers may be used in the combining network to compensate for the losses. The remainder of this section examines the power distribution and combining network of the various beamforming architectures in more detail.

MBPAA and HFC

The output of each RF chain is split into N_{TX} paths, which needs $N_{sp} = N_{TX} - 1$ splitters per RF chain. After phase shifting, M signals are combined and fed into a FEM. This requires $N_{cb} = M - 1$ combiners before each FEM. The total number of Wilkinson Dividers/Combiners needed in the architecture is

$$\begin{aligned} N_{WD_T} &= M(N_{TX} - 1) + N_{TX}(M - 1) \\ &= N_{spT} + N_{cbT} \end{aligned} \tag{3.20}$$

Three stages of splitting induce a loss of 12dB. To mitigate this, we assume the placement of a loss-compensation RF amplifier after every three stages of splitting, starting right before the first splitter. The number of RF splitter amplifiers per RF chain is then N_{spA}. This number can become excessively large for arrays of size $N_{TX} = 512$, so for this specific array size, we choose to place RF amplifiers with a slightly higher gain after every two stages of splitting instead. This yields a more practical number of total RF amplifiers in the network.

$$N_{spA} = \Sigma_i^{\Gamma} 2^{\epsilon i} \tag{3.21}$$

$$N_{spA,tot} = M N_{spA} \tag{3.22}$$

$$i = 0, \epsilon = 3, \Gamma = \lfloor \frac{log_2 N_{TX}}{3} \rfloor \qquad N_{TX} < 512$$

$$i = 1, \epsilon = 2, \Gamma = \lfloor \frac{log_2 N_{TX}}{2} \rfloor \qquad N_{TX} = 512$$

In the combining network of up to three stages ($M = 8$), the combining and insertion loss is at most $4 \cdot 3 = 12$dB, which can easily be compensated by placing a single variable gain amplifier (VGA) after the phase shifter, without the use of additional RF amplifiers along the combining branches. For additional stages, however, RF amplifiers are placed symmetrically before the final combiner. The number of RF combining amplifiers per RF chain is N_{cbA}.

$$N_{cbA} = 0 \qquad M < 16 \tag{3.23}$$

$$= \log_2 M - 3 \qquad M = 16, 32 \tag{3.24}$$

$$N_{cbA,tot} = N_{TX} N_{cbA} \tag{3.25}$$

HSA

For HSA, there is no combining network. The splitting network is similar to that in the HFC case. The output of each RF chain is split into K paths, which needs $N_{sp} = K - 1$ splitters per RF chain. To compensate for splitter losses, RF amplifiers are placed after every two stages of splitting, leading to N_{spA} splitter amplifiers in every RF chain. The total number of Wilkinson Dividers and associated RF amplifiers is

$$N_{WD_T} = M(K - 1) \tag{3.26}$$

$$N_{spA} = \Sigma_i^{\Gamma} 2^{\epsilon i} \tag{3.27}$$

$$N_{spA,tot} = M N_{spA} \tag{3.28}$$

$$i = 1, \epsilon = 2, \Gamma = \lfloor \frac{log_2 N_{TX}}{2} \rfloor \qquad K \leq 32$$

SDMBA

For SDMBA, there is no combining network. The splitting network is similar to that of HSA, with the notable difference being that it appears *after* the FEM i.e. between the FEM PA and the antenna elements. Since the output of the splitting network is directly fed into the antenna sub-array, the splitting loss does not play a role, and therefore no RF amplifiers are placed along the splitting network. The FEM PA in SDMBA must therefore compensate for the insertion loss of the splitters, leading to more demanding PA requirements compared to the other architectures.

3.5.3 Overview of Array Topology

Table 3.7 presents an overview of the composition of the five architectures from the system-level model.

Table 3.7: Summary of BS transmitter architecture composition.

Component		Symbol	MBPAA	DMBA	SDMBA	HFC	HSA
Antenna Elements		N_{TX}	N_{TX}	N_{TX}	N_{TX}	N_{TX}	N_{TX}
RF Chains		M	M=U	M=N_{TX}	M=U	M=U	M=U
Sub-array Elements		K	-	-	K	-	K
Sub-arrays ‡		-	-	-	N_{TX}/K	-	N_{TX}/K
BPF	band pass filter	N_{BPF}	N_{TX}	N_{TX}	N_{TX}	M	N_{TX}
Divider		N_{spT}	M($N_{TX}-1$)	-	M(K-1)	M($N_{TX}-1$)	M(K-1)
Combiner		N_{cbT}	$N_{TX}(M-1)$	-	-	$N_{TX}(U-1)$	-
BBU	baseband unit	N_{BBU}	-	1	1	1	1
DAC	digital-to-analog converter	N_{DAC}	M	N_{TX}	N_{TX}/K	M	N_{TX}/K
Mixer,LO	mixer and LO	N_{mxLO}	M	N_{TX}	M	M	M
PS	phase shifter	N_{PS}	MN_{TX}	-	-	MN_{TX}	N_{TX}
VGA	variable gain amplifier	N_{VGA}	MN_{TX}	-	-	MN_{TX}	N_{TX}
PD	pre-driver	N_{PD}*	$f(Pin)$	$f(Pin)$	$f(Pin)$	$f(Pin)$	$f(Pin)$
Split. Amp.	splitting network amplifier	N_{spA}†	$f(N_{TX})$	-	-	$f(N_{TX})$	$f(K)$
Comb. Amp.	combining network amplifier	N_{cbA}†	$f(M)$	-	-	$f(M)$	-
PA	power amplifier	N_{PA}	N_{TX}	N_{TX}	N_{TX}	M	N_{TX}

‡ From our assumption of $M = U$ in Equation 3.19.
* Depends on input power $P_{in_{PD}}$ (see Section 4.6).
† See Section 3.5.2.

3.6 Conclusion

This chapter focused on steps 1-2 of the modelling methodology (Figure 2.4). The key points are summarised below.

- The delineated Use Cases are associated with (a) the 3GPP-specified values of the signal bandwidths where $BW = 100, 200, 400$ MHz, and (b) A varying number of simultaneously connected users, $U = 2 - 32$.
- For the eMBB scenario which captures this project's scope, $U = 8$ is currently the most practical use case, since there are few existing implementations of beamforming architectures that consider more than 8 simultaneous streams. Meanwhile, $U = 32$ can be regarded as a future scenario.
- Based on 3GPP recommendations, we assume a standard EIRP of 40 dBm per beam in the proposed model. However, a more realistic scenario with a variable probability of line of sight (LOS%) is also considered.
- Five beamforming-based multi-beam transmitter architectures are considered in this model. An overview of their topologies has been tabulated in Table 3.7.
- We make a strong assumption where the number of RF chains is set to be equal to the number of users, i.e. $M = U$ (Equation 3.19). This way, each user only receives a single stream from the BS transmitter. Without discarding the assumption, we can consider U to represent the number of beams and U' to represent the number of users, where $U \neq U'$. The model can thereby be extended to a multi-stream scenario where $M = U \geq U'$.
- The power distribution and combining network within the transmitter architectures, along with the associated loss compensation RF amplifiers, was not adequately considered in the literature. This gap is addressed in by the proposed power consumption model.

In the following chapter, we dive into the next two steps of the methodology, which consist of the component-level modelling and its integration into the system-level model.

Chapter 4

Model: Component-Level

This chapter presents the second, component-level part of the developed power consumption framework, and covers steps 3 and 4 of the thesis methodology. Each component's relevant properties are tabulated at the end of the respective section. Section 4.7 combines the system-level and component-level models into the integrated power consumption model.

4.1 FEM Power Amplifier

The FEM power amplifier is the most critical component in the base station transmitter, as it needs to satisfy constraints from both, the link budget perspective, and the BS hardware perspective. Notably, the PA technology must have a high enough Gain G_{PA} to boost the input signal to the required transmit power, and a high enough saturation power P_{sat} to meet the link budget's EIRP, while also being cost-efficient with a low form factor.

For pre-5G technologies with a relatively low number of antennas in the transmitter, the PA technology was the deciding aspect of the system's operation and power consumption. However, by vastly increasing the number of antennas in 5G massive MIMO architectures, the requirements on the PA can reduce drastically. This section derives the PA's output power and power consumption, and quantitatively assesses the choice of PA technology based on the SOTA in silicon and III-V technology developments.

4.1.1 PA output power

In Equation 3.18, we established the required transmit power per antenna element, given the use case and array size. Following this, the PA output power $P_{out_{PA}}$ required for the specified transmit power per antenna element can be derived based on the number of antenna elements being served by each PA, and the losses between the PA and the antenna element.

For the MBPAA, DMBA, HFC and HSA architectures, each FEM is connected to a single antenna element, with intermediate losses due to the insertion loss of the PA and band pass filter (BPF). Filters designed for large bandwidths and mmW signals can have a non-negligible insertion loss of around 1 dB [56–58]. This yields the PA output power as

$$P_{out_{PA}}[dBm] = P_{TX_{AE}} + IL_{PA} + IL_{BPF} \tag{4.1}$$

On the other hand, for the SDMBA architecture, each FEM is connected to the K antenna elements that form a sub-array, and there are intermediate insertion losses due to the splitting network between the FEM and antennas. We assume that binary Wilkinson Dividers is used for the splitting network, owing to their fairly low insertion loss of $IL_{wd} = 1$ dB. A sub-array with K antenna elements will need $K-1$ dividers, hence, the PA output power for the SDMBA architecture is expressed as

$$P_{out_{PA}}[dBm] = P_{TX_{AE}} + IL_{PA} + IL_{BPF} + 10\log_{10}(K) + (K-1)\cdot IL_{wd} \tag{4.2}$$

It is clear that for the SDMBA architecture, having a low number of elements per sub-array will result in lower PA requirements. The lowest value of $P_{out_{PA}}$ occurs when $K = 1$, whereby the structure becomes identical to the DMBA structure. For the HSA architecture, changing the sub-array size does not affect the PA requirements, but it does impact the beam pattern of the array – a larger sub-array size will result in a narrower scanning range, thereby reducing the number of users that may be served by the array without interference.

4.1.2 PA power consumption

A PA's overall efficiency, expressed as the Power Added Efficiency or PAE, depends on the PA input power $P_{in_{PA}}$, output power $P_{out_{PA}}$ and the supplied DC power P_{PA}.

$$PAE = \frac{P_{out_{PA}} - P_{in_{PA}}}{P_{PA}} = P_{out_{PA}}\frac{1 - 1/G_{PA}}{P_{PA}} \tag{4.3}$$

where G_{PA} is the PA Gain. For reasonably high values of PA Gain i.e. 13 dB or higher, the influence of the input power reduces and the $P_{in_{PA}}$ term in Equation 4.3 may be eliminated. Consequently, the PA power consumption can be expressed as

$$P_{PA} = \frac{P_{out_{PA}}}{PAE} \tag{4.4}$$

Higher PA efficiency, therefore, has a desirable impact on power consumption reduction. The PAE varies with the PA technology and specific implementation; in this model, to retain generalisability, we only consider the difference based on technologies and do not discuss any particular implementations.

Equations 4.1-4.2 represent the normal operating point of the PA. To ensure that the PA stays in the linear region despite amplitude fluctuations, we assume the PA operates at an output power-backoff of $PBO = 6$ dB from its 1 dB compression point. The maximum PA output power can then be expressed as

$$P_{1dB_{PA}} = P_{out_{PA}} + PBO \tag{4.5}$$

While the average power consumption of the PA depends on its normal operating point given by Equations 4.1-4.2, the saturation point of the chosen PA technology must be high enough to accommodate the maximum required output power $P_{1dB_{PA}}$.

To restrict our analysis to practical scenarios, we introduce a lower bound on the maximum output power as

$$P_{1dB_{PA}} \geq 0 \text{ dBm} \tag{4.6}$$

whereby any combination of (N_{TX}, U, K) where the maximum output power drops below 0 dBm is excluded from the analysis.

4.1.3 Choice of PA technology

Table 4.1 highlights the differences between the P_{sat}, G and PAE of various PA technologies that operate at 28 GHz. The first four are currently widely used in wireless transceivers, while gallium-nitride (GaN) is an emerging technology that is also being explored for Terahertz systems. The full survey of PAs upon which this summary is based can be found in Appendix A.1. The following conclusions can be drawn about the average performance of the various technologies:

1. Silicon technologies have a fairly high average Gain and are the most cost-effective, but have a similarly low average P_{sat} and PAE.

2. GaAs has a reasonably high average P_{sat} (around 5 dB more than silicon technologies) and a moderate PAE at 28 GHz (4-6% more than silicon technologies). However, it is less cost-effective than CMOS and has a lower average Gain.

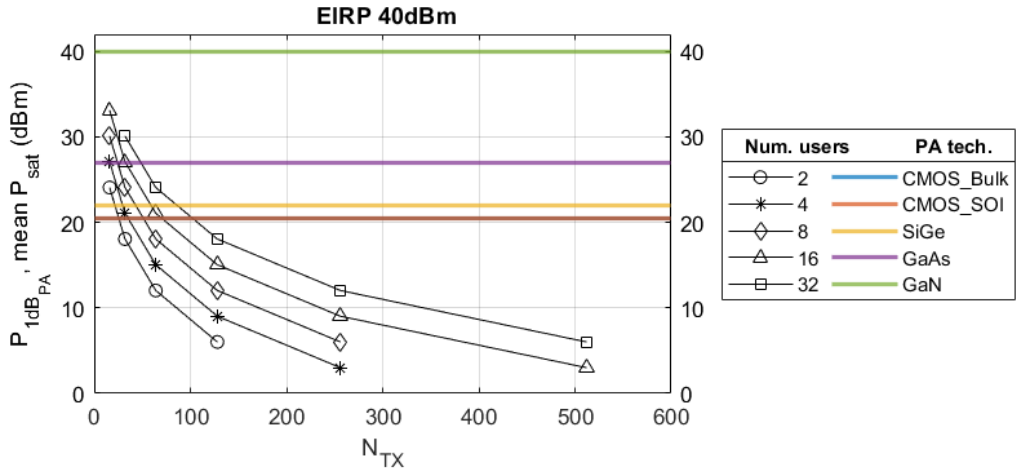
3. GaN shows the best overall performance, but is expensive and difficult to manufacture. Furthermore, considering that the Gain is much less than the P_{sat}, it is clear that GaN PAs require one or more high-output-power pre-driver amplifiers to boost its input power to a suitable level. This implies additional costs and circuit complexity.

4. SiGe and GaN PAs have a large range of P_{sat} and Gain, which highlights the large influence of implementation particularities on the performance of these technologies.

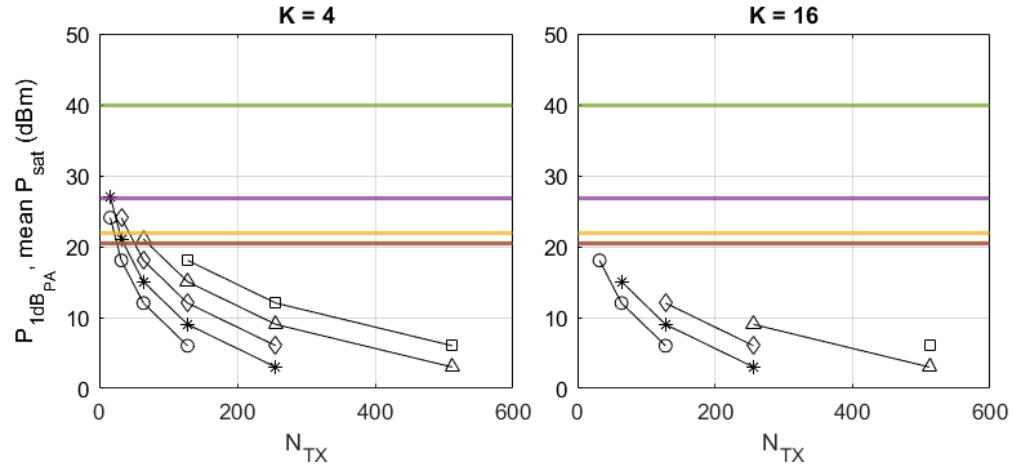
Table 4.1: Summary of SOTA PA technologies at 28 GHz.

Tech.	$P_{sat}(dBm)$			Gain (dB)			PAE (%)			Cost
	min	max	mean	min	max	mean	min	max	mean	
Bulk CMOS	17.50	23.20	20.47	14.80	28.00	20.63	0.12	0.19	0.16	Low
CMOS SOI	18.20	22.50	20.42	16.80	27.00	22.08	0.07	0.25	0.14	Low
SiGe	16.30	28.30	21.96	14.10	36.00	20.01	0.11	0.19	0.14	Low
GaAs	24.00	28.70	26.90	14.40	23.00	18.63	0.10	0.27	0.20	Moderate
GaN	33.00	52.50	39.99	14.00	34.00	21.58	0.21	0.27	0.23	High

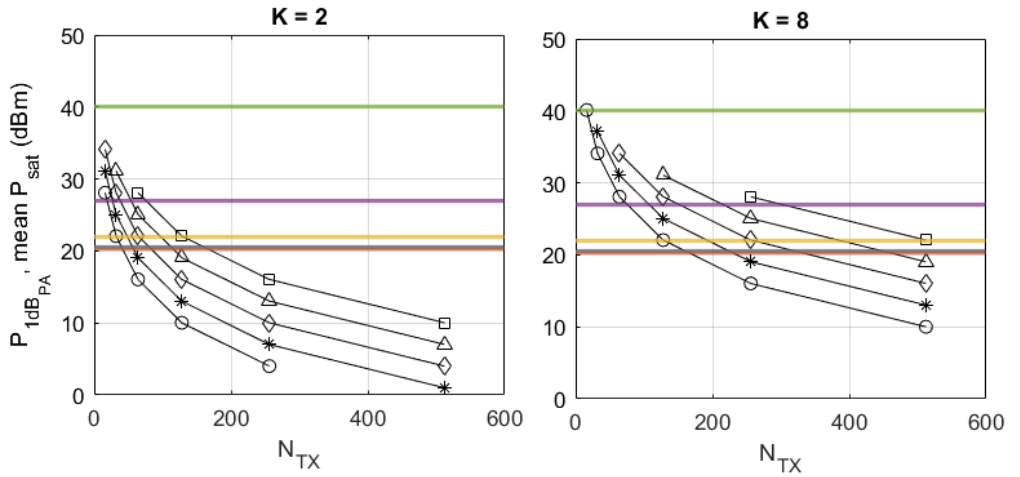
Figure 4.1 shows the required maximum PA output power $P_{1dB_{PA}}$ for $EIRP = 40$ dBm, as a function of the antenna array size N_{TX}, number of simultaneous users U, and sub-array size K. As expected, the required PA output power is lower for large arrays, while for the SDMBA architecture, increasing the number of elements K in a sub-array for a fixed array size leads to an increase in the required PA output power. It is important to note that in the proposed model, as long as the PA can operate at the chosen signal bandwidth and centre frequency, the PA output power (and by extension, the power consumption) is dependent on the specific signal bandwidth only in so far as the EIRP depends on the bandwidth. A complete set of figures for all values of K can be found in Appendix C.



(a) MBPAA, HFC, DMBA



(b) HSA



(c) SDMBA

Figure 4.1: per-PA P_{1dB} as a function of array size N_{TX} and number of users, plotted against the mean P_{sat} of various PA technologies with $EIRP = 40$dBm. There is a strong overlap between the Bulk CMOS and SOI CMOS bars.

Figure 4.1 also depicts the mean P_{sat} of the various PA technologies from Table 4.1. It is imperative that the mean P_{sat} be greater than $P_{1dB_{PA}}$, which is a constraint on the choice of

PA technology for a given array size and number of users. In the proposed model, a 1 dBm margin is assumed when satisfying this constraint, i.e.

$$\text{Required } P_{1dB_{PA}} \leq P_{sat} + 1 \text{ dBm} \tag{4.7}$$

where P_{sat} varies per technology. We notice that GaN technology can support nearly all combinations of U, N_{TX} and K. Meanwhile, CMOS has limited utility when N_{TX} is low. In particular, CMOS cannot support the high $P_{1dB_{PA}}$ required by SDMBA in most situations. Considering the trade-offs in PA performance and cost, it is clear that there is no one-size-fits-all approach to the choice of FEM PA technology.

4.2 Digital-to-Analog Converter

The DAC converts the digital baseband communication signal to an analog signal at an intermediate frequency f_{IF} that can later be up-converted by the mixer.

The power consumption of the DAC depends on signal properties, as well as the circuit architecture of the DAC itself. In this thesis, we consider binary-weighted current-steering (CS) DACs, which are commonly used for (phased) antenna arrays. From **??**, a first-order model of the power consumption of CS DACs can be expressed as

$$P_{DAC}[W] = \frac{1}{2}\left(V_{DD} I_O (2^b - 1) + b \cdot C_p f_s V_{DD}^2\right) \qquad \beta_{DAC} = 1 \tag{4.8}$$

where f_s (Hz) is the DAC sampling frequency, b (bits) is the Effective Number of Bits (ENOB), V_{DD} (V) is the DAC supply voltage, I_O (A) is the unit current value corresponding to the least significant bit, C_p (F) is the parasitic capacitance of every current switch and β_{DAC} is a second-order-effect correction factor. The extended derivation and explanation of Equation 4.8 may be found in [59].

The following subsections describe and characterise the influence of the most important parameters from a power consumption perspective, namely f_s, b and V_{DD}. The various parameters for the DAC power consumption model in Equation 4.8 are summarised in Table 4.2 at the end of this section.

4.2.1 Sampling frequency

For a signal with a bandwidth BW GHz and corner frequency f_{cor} GHz, the sampling frequency based on the Nyquist theorem should be twice the maximum signal frequency. Further, oversampling the signal by a factor $OS > 1$ leads to improved linearity and reduces the peak-to-average power ratio (PAPR) requirements of the components further down the RF chain. The DAC sampling frequency is thus given by

$$f_{sig,max} = f_{cor} + \frac{BW}{2} \tag{4.9}$$

$$f_s = OS \cdot 2 \cdot f_{sig,max} \qquad OS >= 1 \tag{4.10}$$

$$f_{IF} = f_s \tag{4.11}$$

While a higher DAC sampling frequency is beneficial for signal quality, the large bandwidths impose stringent restrictions on DAC linearity, which makes them difficult to design and implement.

4.2.2 Effective Number of Bits

The choice of DAC resolution, expressed as ENOB, relates to an important trade-off between power consumption and performance. Higher values of ENOB result in a better performance, but also result in higher energy and computation costs. There is recent interest in exploring the spectral and energy efficiency of very low-resolution DACs with $b = 1, 2$ bits. However, since 2022, there are specific 3GPP guidelines for the minimum required spurious free dynamic range (SFDR) for a 5G New Radio signal, intending to limit interference [14], where

$$SFDR_{min} = 36dBc \tag{4.12}$$

which may not be achievable with only 1 or 2 bits.

The SFDR requirement can be used to obtain the DAC dynamic range DR. For an ideal DAC, the dynamic range is equivalent to the signal-to-noise-and-distortion ratio (SINAD), due to no harmonic distortions within SFDR frequency range. By further considering the oversampling of the DAC frequency by a factor $OS > 1$, we can use Equation 4.10 to obtain the SINAD as

$$DR_{DAC}[dB] = SFDR_{min} + HR - At_{filter} \tag{4.13}$$
$$SINAD[dB] = DR_{DAC} + 10\log_{10}(OS) \tag{4.14}$$

where HR (dB) and At_{filter} (dB) are the headroom requirement and internal filter attenuation respectively [60]. Finally, based on the SINAD, the required minimum ENOB of the DAC can be obtained through the well-known relation:

$$b[\text{bits}] = \frac{(SINAD[dB] - 1.76)}{6.02} \tag{4.15}$$

where b is *rounded up* to the closest integer number of bits. Using the values specified in Table 4.2 leads to a minimum resolution of $b = 8$ bits.

Several additional assumptions have been made for this derivation of the DAC ENOB, and are listed along with the full derivation in Appendix B.

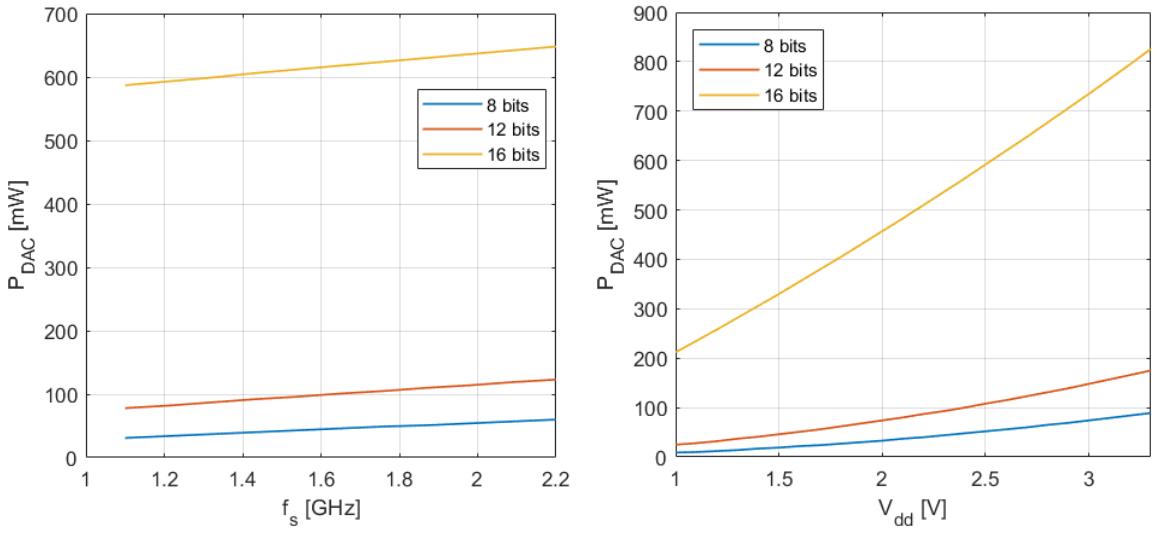
4.2.3 Supply Voltage

Accounting for topology-specific peculiarities, a higher (analog) supply voltage $V_{DD,A}$ usually implies a higher power consumption as well. Table 4.3 presents the SOTA for (CMOS) current-steering DACs in the literature, and can be used to make an informed decision on V_{DD}.

Figure 4.2 shows change in DAC power consumption with the sampling frequency, supply voltage and ENOB on the power consumption, for Case 1 ($BW = 100$ MHz). P_{DAC} increases exponentially with ENOB, going from an average of 50 mW at $b = 8$ to over 600 mW at $b = 16$. Furthermore, the impact of f_s and V_{DD} is also felt more keenly for higher-resolution DACs.

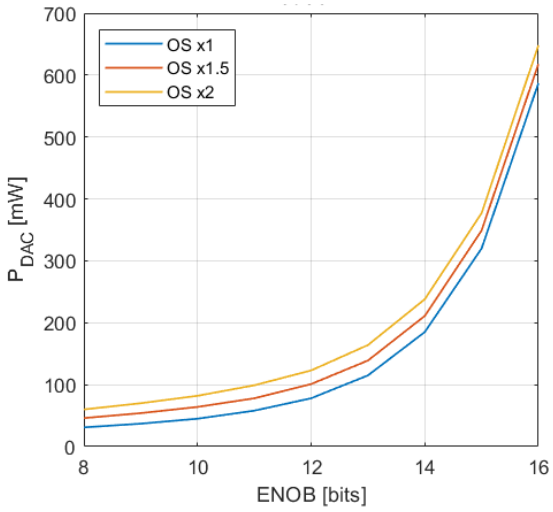
4.3 Mixer and LO

The output signal of the DAC is filtered and fed into a mixer, which is connected to a high-frequency local oscillator (LO), in order to up-convert the signal to the desired frequency. In



(a) Impact of f_s

(b) Impact of V_{DD}



(c) Impact of ENOB

Figure 4.2: Impact of f_s, V_{DD} and ENOB on DAC power consumption (Case 1, $BW = 100$ MHz, Nyquist $f_s = 1.1$ GHz)

our case, this would be the $f_c = 28$ GHz frequency.

Mixers can be categorised as active or passive. Passive mixers are simple to implement, highly linear and consume no power; however, they attenuate the signal and have high insertion loss, which is detrimental to signals at mmW frequencies. Furthermore, they impose higher requirements on the drive power for the LO.

On the other hand, active mixers provide Conversion Gain and good isolation whilst reducing the requirements on the LO drive power, in exchange for positive power consumption. In the proposed model, we use active mixers due to their advantages over passive mixers.

Table 4.4 shows the state-of-the-art active CMOS upconversion mixers intended for the 5G applications. In general, the power consumption increases with increasing operational frequency f_{OP}. Other properties of interest are the Conversion Gain, the output power at 1 dB com-

Table 4.2: Summary of DAC properties and derived parameters (in bold). The full derivation can be found in Appendix B.

Parameter		Value			Unit
$SFDR_{min}$	Min. SFDR	-36			dBc
HR	Headroom	10			dB
At_{filter}	Filter attenuation	3			dB
DR_{DAC}	Dynamic range	43			dB
OS	Oversampling factor	2			-
SINAD	**SINAD**	46.01			dB
b	**Min. resolution** ($\lceil ENOB \rceil$)	8			bits
V_{DD}	Supply voltage	2.7			V
I_O	Unit current source	10			μA
C_p	Parasitic capacitance	1			pF
β	Correction factor	1			-
		Case 1	Case 2	Case 3	
f_{cor}	Corner frequency	0.5	0.8	1	GHz
f_s	**Sampling frequency**	2.2	3.6	4.8	GHz
P_{DAC}	**DAC unit power consumed**	60	97	129	mW

Table 4.3: SOTA of various current-steering DAC properties for low-IF output signal generation. RF = radio frequency DAC, BB = baseband DAC.

Ref.	Year	f_s (GHz)	Res. (bits)	SFDR (dBc)	$V_{DD,D}$ (V)	$V_{DD,A}$ (V)	P_{DC} (mW)	Tech.	Process (nm)	Type
[61]	2021	4	16	71	1	2.5	849[1]	CMOS	65	BB
[62]	2021	1.6	10	67.08	1.1	2.2	54	CMOS	40	BB
[63]	2021	3	14	63	1	2.5	190[2]	CMOS	40	BB
[64]	2019	1	14	60	1.2	2.5	226	CMOS	65	BB
[65]	2017	6.8	14	68	-	-	330	FinFET	16	RF
[66]	2015	1.75	16	62	1.2	3.3	380[3]	CMOS	65	RF
[67]	2015	3	16	78	-	-	800[3]	CMOS	65	RF
[68]	2014	3.2	16	58	1.2	3.3	240	CMOS	65	BB
[69]	2012	0.5	10	61	-	-	24	CMOS	180	BB
[70]	2011	0.2	14	78	1	1.8	270	CMOS	140	BB
[71]	2005	0.5	12	60	-	1.8	160[4]	CMOS	180	BB
[72]	2004	0.32	12	45	1.8	3.3	82	CMOS	180	BB

[1] excluding on-chip cache
[2] including DAC core, MUXs, decoders, switch drivers and RDQS generators; excluding SerDes, interpolation filter, NCO.
[3] including DSP power consumption
[4] excluding clock buffer of 56 mW

pression i.e. OP1dB, and device linearity. However, during the design process, these are often optimised together for a particular application and set of constraints, the consideration of which is outside the scope of our model. Based on the SOTA for the 28 GHz devices, we can assume

an average mixer power consumption of

$$P_{mix} = 10 \text{ mW} \tag{4.16}$$

Next, we consider the LO. A basic LO sub-system can consist of voltage controlled oscillator (VCO) with a reference clock, a phase-locked loop (PLL) that serves as a feedback system, and at least one LO buffer. The recent trend is to use integrated VCO-PLL packages, whose power consumption can differ widely based on peculiarities in the implementation. Furthermore, a common LO for several RF chains often cannot be used, due to the high signal routing loss at mmW frequencies.

Table 4.5 shows the state-of-the-art in LO devices in CMOS, SiGe and GaAs technologies. The power consumption for CMOS LOs is much lower than the others; however, the reference frequency generation occurs off-chip, and therefore its power consumption is not accounted for in the given value of P_{DC}. In exchange for lower power consumption, the CMOS LOs also exhibit worse phase noise performance compared to the SiGe and GaAs LOs.

In the proposed model, we assume a single integrated LO per RF chain. From a power consumption perspective, we choose a 40mW CMOS VCO-PLL with an additional 90mW for eventual Reference clock generation, resulting in

$$P_{LO} = 130 \text{ mW} \tag{4.17}$$

The power consumption for an integrated mixer-LO package is thus estimated as

$$P_{mix,LO} = P_{mix} + P_{LO} = 140\text{mW} \tag{4.18}$$

This is 70-100mW higher than the estimate for mixer/LO power consumption in literature [6,7].

Table 4.4: State-of-the-art mmW mixers for the 5G FR2 frequency range.

Ref.	Year	f_{op} (GHz)	$f_{min} - f_{max}$ (GHz)	V_{DD} (V)	CG (dB)	OP1dB (dBm)	P_{DC} (mW)	Tech.	Process (nm)
[73]	2021	24.0	20.0 - 30.0	1.2	4.1	4.1	4.90	CMOS	65
[74]	2021	24.0	21.6 - 24.0	1.2	4.7	0.4	5.20	CMOS	65
[75]	2021	28.0	25.3 - 32.5	1.5	9.2	-4.2	7.00	CMOS	65
[76]	2019	28.0	27.5 - 43.5	1.0	-7.5	-3.0	14.00	CMOS	65
[77]	2017	31.5	27.0 - 40.0	1.2	3.2	-5.4	9.60	CMOS	65
[78]	2015	24.0[1]	23.4 - 29.2	1.5	-1.9	0.3	39.30	CMOS	130
[79]	2006	28.0	18.0 - 28.0	1.2	0.7	-5.0	8.00	CMOS	130

[1] For 24 GHz ISM band

4.4 Phase Shifter

In the case of the fully-connected analog/hybrid architectures, the PS output is fed into a lossy combining network, and pre-amplification using VGAs is needed to compensate for (part of) the combining loss. Without going too deep into the details, based on [6] we assume an active phase shifter with 0dB gain and the power consumption given by

$$P_{PS} = 10 \text{ mW} \tag{4.19}$$

Table 4.5: State-of-the-art mmW LOs for the 5G FR2 frequency range.

Ref.	Year	Device	f_{op} (GHz)	$f_{min} - f_{max}$ (GHz)	V_{DD} (V)	PhN@1MHz (dBc/Hz)	P_{DC} (mW)	Tech.	Process (nm)
[80]	2020	VCO	35.8	33.6 - 36.0	1.0	-94.90	20.6[1,2]	CMOS	45
[81]	2020	VCO	28.3	27.7 - 28.9	2.0	-96.30	111.0	GaAs	250
[82]	2019	VCO-PLL	26.4	25.4 - 29.5	1.0	-112.80	10.2[1,4]	CMOS	65
[83]	2019	VCO-PLL	-	20.5 - 24.9	2.0	-122.00	202.0[3]	SiGe	120

[1] Reference freq. generator is off-chip.
[2] 7.2mW RSPLL, 13.4 mW ILVCO.
[3] 120 mW from PLL, 30 mW from Reference buffer, avg. 78 mW from VCO.
[4] 6.9mW from VCO, 2.15mW from FLL, 1.15mW from VCO buffer and clock; excluding Reference buffer of 5.08mW.

The power consumption of the VGA is described in section 4.6 together with the other types of RF amplifiers used in the transmitter. A comprehensive review of phase- and amplitude-control circuits for wireless communications using various beamforming architectures, can be found in [84].

4.5 Baseband Unit

In digital and hybrid beamforming, digital precoding, consisting of several complex multiplications, is carried in the BBU before the data streams are converted to RF signals and routed to the antenna elements. In hybrid beamforming architectures, the signals undergo additional analog precoding in the phase shifter network before the antenna array. Each antenna element then transmits a separate signal.

The BBU consumes its own share of power, proportional to its processing rate [85]. Furthermore, the subject of optimal energy-efficient precoding for both, digital and hybrid systems is an open research problem that receives considerable attention in the research community [6,86,87].

In reality, the DSP power consumption in the BBU depends on several factors, among which are the signal bandwidth BW, the number of antenna elements N_{TX}, the number of simultaneous users U and the processing efficiency of the BBU. A simple model for the BBU power consumption can be made by estimating the power consumption per complex operation per sample, and then scaling it to the total number of operations and the signal bandwidth.

In the sub-array architectures, digital beamforming is applied across the K antenna sub-arrays. This is unlike the fully-digital and fully-connected analog/hybrid beamforming architectures, where it is applied to each individual antenna element. Thus, the number of digital operations for SDMBA and HSA is can be much reduced by reducing the number of sub-arrays. Similarly, for the hybrid architectures, the intensity of digital processing is lowered by the presence of a subsequent analog beamforming network, which in turn lowers the power consumption of the digital beamforming stage.

Consider an array with N_{ip} ports to the antenna array, where $N_{ip} = N_{TX}/K$ for SDMBA and HSA, and $N_{ip} = N_{TX}$ for all other architectures. From [85], for a MU massive MIMO setup

(assuming full frequency re-use), the total number of complex multiplications m_z and associated processing rate r_z are estimated as

$$m_z = N_{ip}U \tag{4.20}$$
$$r_z[OPS] = m_z BW = (N_{ip}U)BW \tag{4.21}$$

Assuming a conservative BBU efficiency of $\eta_{BBU} = 25\text{MOPS/mW}$ (derived from [7]), we can approximate the total BBU power consumption as

$$\begin{aligned} P_{BBU}[mW] &= r_z \cdot \eta_{BBU} \cdot \gamma_{DSP} \qquad \gamma_{DSP} \in [0,1] \\ &= (N_{ip}U)BW\eta_{BBU}\gamma_{DSP} \end{aligned} \tag{4.22}$$

where γ_{DSP} represents the dependence on beamforming architecture. For the digital architectures, $\gamma_{DSP} = 1$. For the hybrid architectures, the intensity of digital processing is lowered by the presence of a subsequent analog beamforming network; in the proposed model, we use $\gamma_{DSP} = 0.8$ for HSA and HFC. For the fully-analog MBPAA, $\gamma_{DSP} = 0$.

4.6 Loss Compensation and Driver Amplifiers

Apart from the main PA in the FEM, there are four other types of RF amplifiers used in the transmitter: splitter-loss compensation amplifiers, combiner-loss compensation amplifiers, VGAs in the phase shifter group, and pre-driver amplifiers used to drive the FEM PA input power. As mentioned previously, for a mmW signal with a fairly large bandwidth, relying on a single, more powerful RF amplifier may not be feasible, because it may push other active components in the circuit into a highly non-linear region, and subsequently yield a distorted output signal. Instead, a loss budget is drawn for each architecture, based on which less powerful RF amplifiers are cascaded along the splitter/combiner network to compensate for the loss in stages. A similar approach was followed by [6].

The splitter- and combiner-loss compensation amplifiers have been described extensively in Section 3.5.2. Their properties are summarised in Table 4.6.

The VGAs in the PS groups have a variable gain that depends on the number of subsequent combining stages. The state-of-the-art VGA for the 27-29 GHz frequency range and 9dB maximum Gain consumes around 15mW [88].

The pre-driver (PD) is needed to drive the input power of the FEM PA. The exact required input power to the PA, as well as the input power to the PD, is highly implementation specific. in the proposed model, we assume a PA input power of 0 dBm, and the required PD gain is calculated accordingly. In the power model in [89], the PD has a maximum gain of 15 dB and uses 40 mW DC power. Therefore, multiple PDs may be used to meet the gain requirements in steps of $G = 15$ dB. in the proposed model, to preserve generality while accounting for the variable gain, the PD power consumption is divided into three categories based on the value of G. The various categories are summarised in Table 4.6.

As an illustration, if an additional 28dB gain is needed after combining to drive the FEM PA (this is possible for GaN PAs, or certain sub-array configurations), the PD arrangement can

look as follows:

$$G_{req}[dB] = 15 \cdot N_{PD_{15dB}} + 10 \cdot N_{PD_{10dB}} + r \tag{4.23}$$

$$P_{PD}[mW] = 40 \cdot N_{PD_{15dB}} + 20 \cdot N_{PD_{10dB}} + 10 \cdot min(r, 1) \tag{4.24}$$

where r is the gain of the final PD. In this example, $N_{PD_{15dB}} = 1, N_{PD_{10dB}} = 1$ and $r = 3$. The power consumption will then be $P_{PD} = 70$mW.

Table 4.6: Summary of RF amplifiers for loss compensation in splitting/combining networks and the FEM.

Arch.	Type of RF Amplifier	G (dB)	IL (dB)	P_{DC} (mW)
MBPAA, HFC	Splitter Amp.	13 if $N_{TX} = 512$	1	20
		12 if $N_{TX} < 512$	1	20
	VGA	4 if U = 2	1	15
		8 if U = 4	1	15
		9 if U $\geq$ 8	1	15
	Combiner Amp.	4	1	10
HSA	Splitter Amp.	8	1	10
All	Pre-Driver Amp.[1]	< 10	1	10
		$10 - 14.9$	1	20
		15	1	40

[1] $G = f(P_{in_{PD}})$ where $P_{in_{PD}}$ is the signal input power to the pre-driver amplifier.

4.7 Integrated Power Consumption Model

Table 4.7 summarises the unit power consumption values from the component-level model. By integrating the system-level model and component-level model, the total power consumption can be expressed as

$$P_{TOT} = P_{BBU} + P_{RFC} + P_{PSG} + P_{RFamp} + P_{PA} \tag{4.25}$$

where

$$P_{RFC} = N_{DAC}P_{DAC} + N_{mix,LO}P_{mix,LO} \tag{4.26}$$

$$P_{PSG} = N_{PS}P_{PS} + N_{VGA}P_{VGA} \tag{4.27}$$

$$P_{RFamp} = N_{spA}P_{spA} + N_{cbA}P_{cbA} + N_{PD}P_{PD} \tag{4.28}$$

4.8 Conclusion

This chapter focused on steps 3-4 of the modelling methodology (Figure 2.4). The key points are summarised below.

- The component-level model comprises the characterisation and power-consumption modelling of several BS transmitter components, whose unit power consumption is summed up in Table 4.7.

Table 4.7: Summary of unit power consumption of BS components.

Component		Symbol	Unit P_{DC}
BBU	baseband unit	P_{BBU}	$(N_{ip}U)BW\eta_{BBU}\gamma_{DSP}$
	BBU efficiency	η_{BBU}	0.04 mW/MOPS
	DSP intensity	γ_{DSP}	0/1/0.8 ‡
DAC	digital-to-analog converter	P_{DAC}	60/97/129 mW +
mixer, LO	mixer and LO	$P_{mix,LO}$	140 mW
PS	phase shifter	P_{PS}	10 mW
VGA	variable gain amplifier	P_{VGA}	15 mW
PD	pre-driver	P_{PD}	10/20/40 mW *
Split. Amp	splitting network amplifier	P_{spA}	20 mW
Comb. Amp	combining network amplifier	P_{cbA}	10 mW
PA	power amplifier	P_{PA}	$\frac{P_{out_{PA}}}{PAE}$

‡ For ABF/DBF/HBF respectively.
+ For 8-bit ENOB and case 1/2/3 respectively.
* Depends on input power $P_{in_{PD}}$. See subsection 4.6.
x Depends on EIRP, architecture, and PA technology. See subsection 4.1.

- For the FEM PA, a lower bound on the PA output power was introduced in Equation 4.6 where

  $$P_{1dB_PA} > 0dBm$$

  in order to discard situations of a high array size with a very low number of users, and therefore restrict ourselves to more realistic situations. However, the pre-driver amplifier and loss compensation amplifiers are sensitive to this constraint, which creates an opportunity for optimising the choice of the lower bound, and consequently optimising the system's power consumption.

- In general, GaN technology is able to support nearly all combinations of U, N_{TX} and K, while CMOS technologies will be preferred for large array sizes.

- The estimated power consumption of the combined mixer and LO in this model is much higher than the estimated values in the literature. This will have consequences on the DMBA architecture, due to the large number of mixers and local oscillators required.

- An integrated system power consumption model is presented in Section 4.7.

This concludes the design of our power consumption model. In the following chapter, we proceed to assess the validity of the model with respect to the existing literature.

Chapter 5

Model Validation

Before applying the model to the various outlined use cases, it must be validated. This ensures that the model behaves as expected, in accordance with the models in the literature, and thereby lends credibility to the results in Chapter 6. Two aspects are chosen for validation: the DAC power consumption model, and the system-level model behaviour.

5.1 DAC Model Validation

The DAC power consumption model (Equation 4.8) was formulated over a decade ago. It is therefore necessary to ascertain whether the model can still reasonably estimate the power consumption of state-of-the-art implementations. To validate the DAC power consumption model, the reported properties from the DAC survey in Table 4.3 were used as input parameters to the model, and the computed P_{DAC} was compared to the reported value in Figure 5.1.

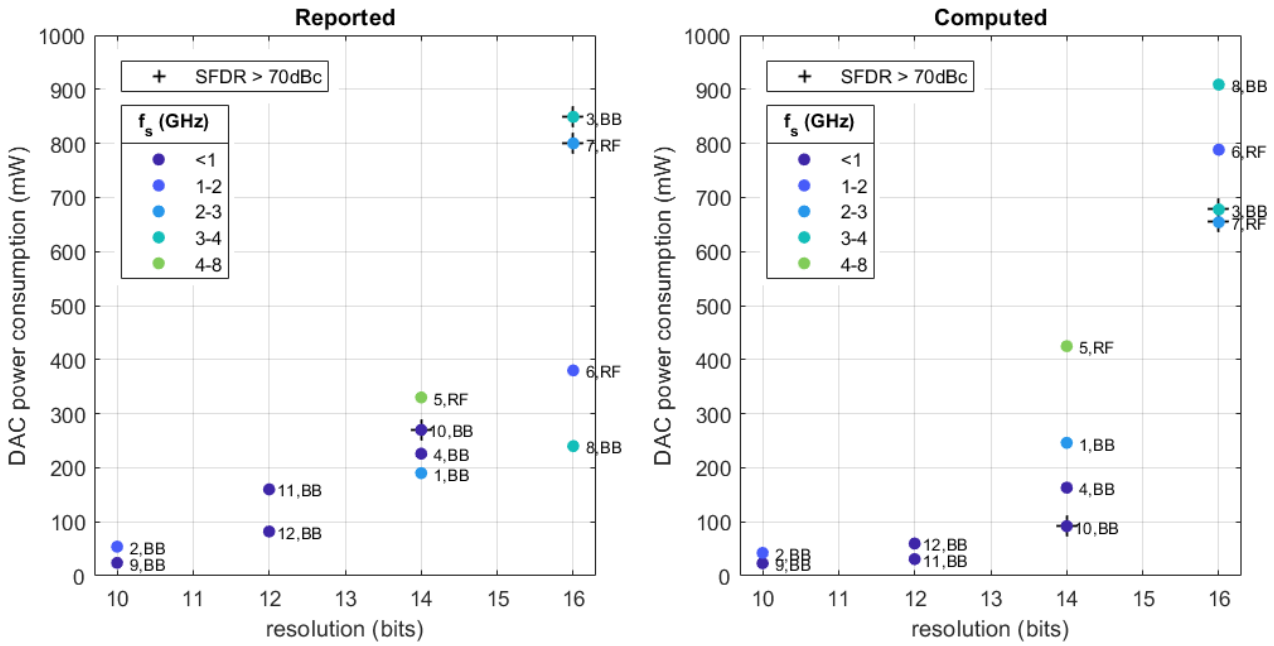


Figure 5.1: Reported DAC P_{DAC} from SOTA vs. computed DAC P_{DAC} using reported properties as inputs to the proposed model.

Since this is only a first-order model, it is possible for the error between the modelled and actual (reported) power consumption to be up to ±50%, even without considering the peculiarities of the DAC's implementation. The error between the reported and computed values for each of the surveyed DACs is displayed in Figure 5.2. The model yields an acceptable estimate of the power consumption for $ENOB < 16$.

One reason for the incorrect output for high-resolution DACs could be that these DACs are often highly optimised to consume low power or meet certain technical requirements, and the DAC consumption model does not take these optimisations into account. Similarly, the model underestimates the power consumption of DACs that were designed for very high linearity (SFDR > 70dBc) and which consequently draw more power, as the SFDR is not an explicit parameter in the model. The high resolution and high linearity cases may be treated as outside of the scope for this DAC power consumption model. By contrast, we choose an 8-bit resolution derived from an SFDR of 36dBc, which is low enough to be within the model's scope.

The mean error and the standard deviation of the error were found to be $\epsilon_{mean} \approx 9\%$ and $\epsilon_\sigma \approx 167mW$ respectively. These statistics were computed excluding ref. 8, to account for its specific implementation characteristics. While this validation method is sufficient for our purpose, it must be tested on a much larger dataset of state-of-the-art DAC implementations before drawing more concrete conclusions.

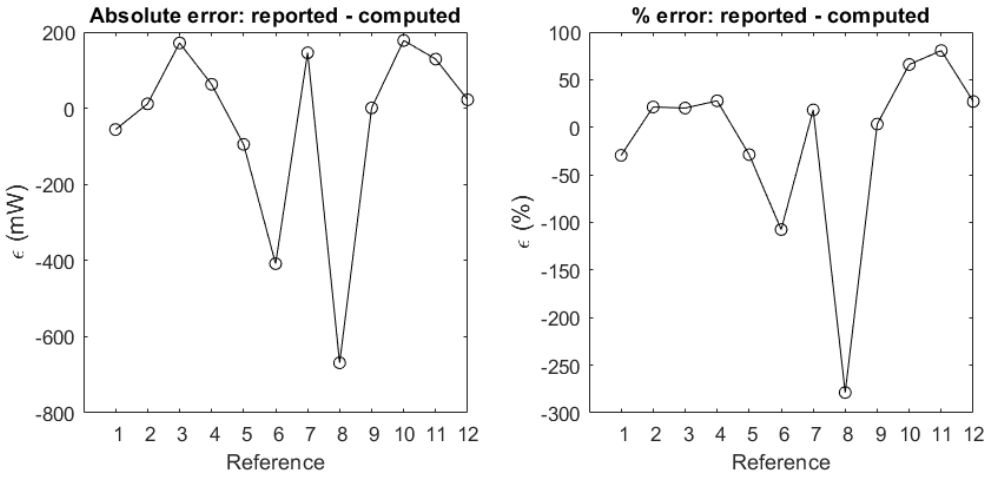


Figure 5.2: Absolute and % error between the reported and computed value of DAC P_{DC}. The reference numbers indicate the implementation in Table 4.3.

5.2 Validation of Total Power Consumption

Based on the findings in the literature [6, 7], we expect the total power consumption P_{TOT} to be a convex function of the number of antenna elements in the architecture. The system-level validation was conducted as follows: Using [7] as a reference, identical input parameters were set for both the reference model and our proposed model: (a) $U = 17$ users (b) $BW = 250$ MHz (c) $EIRP = 40$ dBm (d) FEM PA $PAE = 25\%$.

Figure 5.3 shows the result of the model validation. We notice that this model follows a similar trend to the reference model, namely, the existence of the optimal point for both architectures, and the lower $P_{DC_{TOT}}$ of DMBA compared to MBPAA. We conclude that our proposed model works as expected.

There are two main reasons for the differences between the two models, which are quantified in Tables 5.1-5.2. Firstly, the proposed model estimates a higher power consumption for each architecture due to the increased number of components considered, and secondly, the unit power consumption of several components is higher. Table 2.2 in the literature review compares the differences in the type of components that comprise each model.

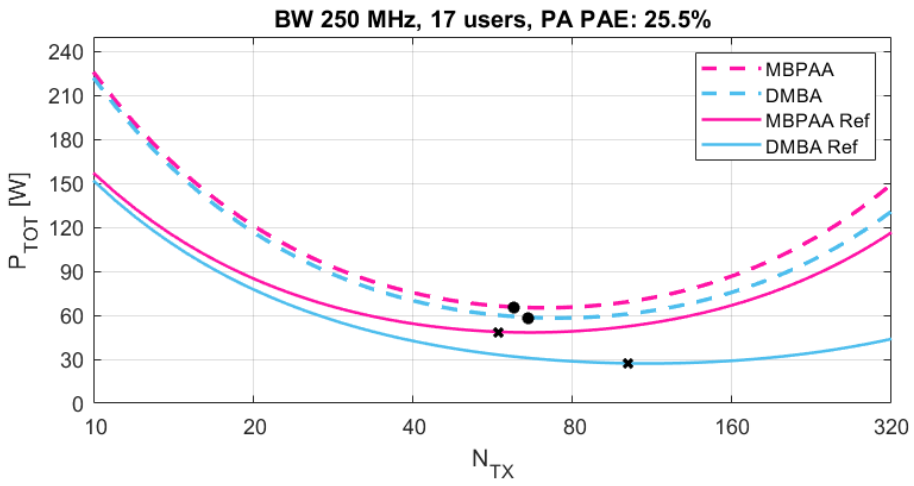


Figure 5.3: System model validation against the reference power consumption model in [7]. The markers indicate the optimal point for each architecture.

Component	Reference [7]	This model
P_{BBU}	62.5 mW/ant.	170 mW/ant.
P_{DAC}	20 mW	68 mW
$P_{mix,LO}$	40 mW	140 mW
P_{PS}	20 mW	10 mW

Table 5.1: Difference in unit power consumption.

Architecture	Reference [7]	This model
MBPAA P_{TOT}	48 W	65 W
DMBA P_{TOT}	27 W	58 W
MBPAA N_{TX}	58	62
DMBA N_{TX}	102	66

Table 5.2: Difference in optimal total power consumption and array size.

5.3 Conclusion

In this section, two aspects of the proposed power consumption model were validated against the literature. First, the DAC model was tested against more recent state-of-the-art implementations and was found to make acceptable estimates of P_{DAC}. Secondly, the model was validated at a system level by testing it against the system power consumption model in [7]. The proposed model's output is comparable, with justifiable differences based on the improvements in this thesis.

Chapter 6

Results and Discussion

In this chapter, the results of the system-level power consumption model of the beamforming architectures are presented and analysed. The chapter begins with a parametric analysis of the power consumption, with the key takeaways enumerated in Section 6.1.6 Following this, the optimally low value of the total power consumption and per-user power consumption is examined. Finally, several recommendations on the optimal choice of architecture, FEM technology and array size are formulated in Section 6.3.

6.1 Parametric Analysis

As shown earlier, the total power consumption P_{TOT} for a beamforming-based multi-beam transmitter is a convex function of the number of antenna elements. At the minima i.e. the optimal P_{TOT} point, the decrease in power consumption stemming from reduced PA output power is offset by the elevated power consumption of the other circuit components. The location of this optimal point along the range of antenna array sizes depends on several factors, which form a subset of the power consumption model's inputs: the architecture's topology, the FEM PA technology, the number of users, the EIRP per beam, and the signal bandwidth.

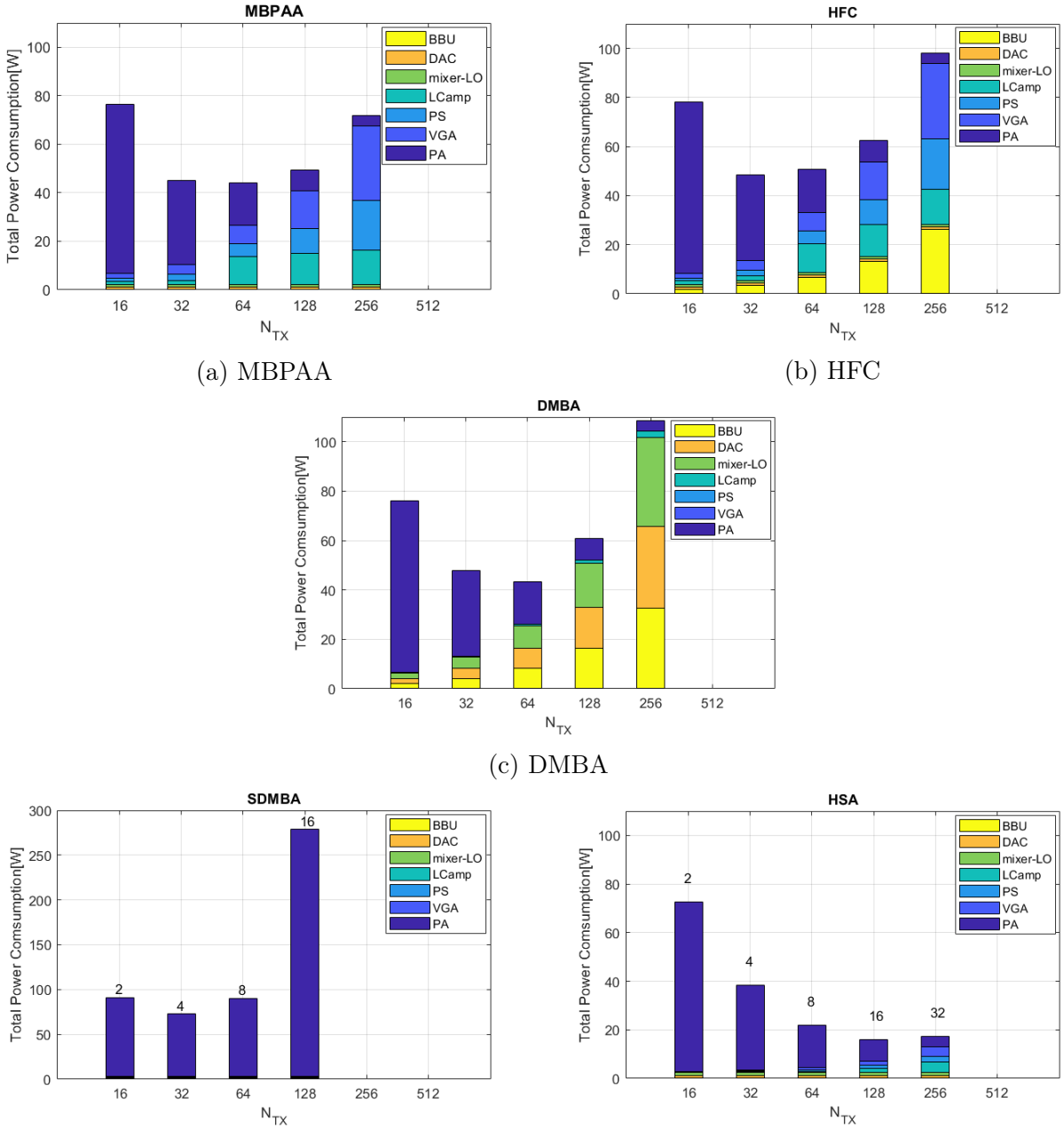
This section presents a parametric study of the impact of the above-mentioned factors on P_{TOT} for each beamforming-based array architecture. A selection of illustrative figures are presented throughout this chapter, while the complete set of figures can be found in Appendix C.

6.1.1 Component Power Contributions

In order to illustrate the component power contributions, we choose the general use case of $BW = 400$ MHz with $U = 8$ users and $EIRP = 40$ dBm, which is in line with expected future 5G applications. Based on our earlier assumption of $M = U$, all but fully digital DMBA architecture are based on 8 RF chains, and the sub-array size varies as $K = N_{TX}/8$.

Figures 6.1a-6.1e show the power consumption breakdown as a function of the array size N_{TX}, for MBPAA, HFC, DMBA, SDMBA and HSA respectively. There are several interesting conclusions to be drawn, which are listed below. This is followed by a deeper look at the sub-array architectures, due to their unique features.

- For this use case, the total power consumption is between 40W (reasonably low) and 110W



(a) MBPAA

(b) HFC

(c) DMBA

(d) SDMBA

(e) HSA

Figure 6.1: Power consumption breakdown (Case 3, $BW = 400$ MHz, $EIRP = 40$ dBm, $U = 8$). For SDMBA and HSA, the sub-array size K is indicated above each bar. *LCamp* combines the loss compensation amplifiers and pre-driver amplifier .

(fairly high) for all architectures and number of antenna elements N_{TX}. The exception is HSA for $N_{TX} \geq 32$, which will be discussed later in this section.

- For $N_{TX} = 512$ antennas, the PA maximum output power is under 0 dBm and is excluded from this analysis, according to the earlier constraint from Equation 4.6.

- The only difference between MBPAA (Figure 6.1a) and HFC (Figure 6.1b) is the digital BBU power consumption, as expected based on their respective topology. Due to this additional component, the optimal number of antenna elements for HFC is smaller than for MBPAA, occurring at $N_{TX} = 32$ and $N_{TX} = 64$ respectively. We expect this result

to endure when there are changes in the bandwidth, EIRP and other parameters.

- Loss Compensation amplifiers and VGAs take up a significant portion of the power budget, consuming almost 14% and 31% respectively of the total power at the $N_{TX} = 256$. Due to this, the HFC architecture in particular shows comparable total power consumption to the fully digital DMBA, even though it has fewer RF chains.

- In the fully digital DMBA (Figure 6.1c), there is an expected linear increase in the DAC and BBU power consumption with the number of antenna elements. At large values of N_{TX}, however, a significant portion of the power budget is allotted to the mixer-LO, which consumes almost 33% of the total power budget for $N_{TX} = 256$. The mixer-LO is not usually considered the most power-hungry component in the transceiver, hence, efforts to address its power consumption have been limited. Figure 6.1c highlights that at the large array sizes required by massive MIMO, the high number of mixer-LOs become a disadvantage of using DMBA.

- In the sub-array based SDMBA, the power consumption of the RF chains has decreased with respect to DMBA to under 5W. At the same time, the increase in PA output requirements with K leads to a substantial increase in the total power consumption, particularly when $K = 16$, which will be discussed later in this section.

- In the sub-array based HSA, the power consumption of phase shifters, RF amplifiers and RF chains has decreased with respect to MBPAA and DMBA, while the PA power consumption remains unchanged. This makes HSA the optimal choice of architecture for this use case from a purely power-consumption perspective.

- Finally, as the (sub)-array size increases, the SDMBA and HSA architectures show different trends in their total power consumption.

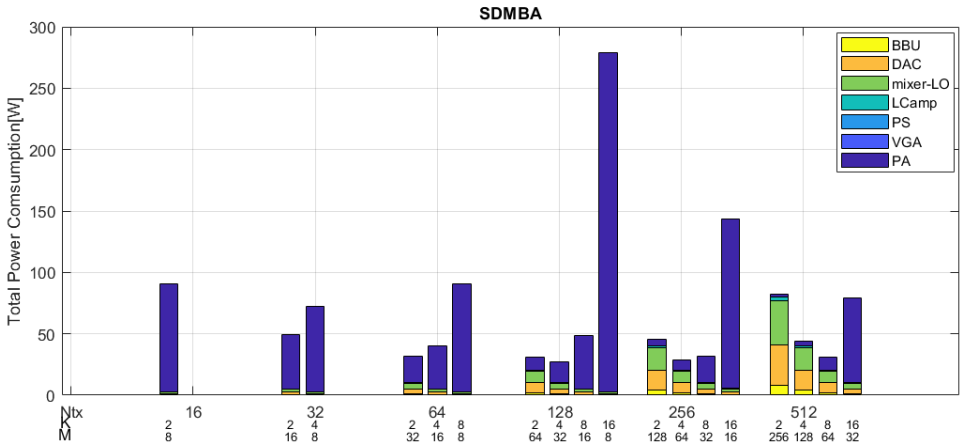
Sub-array architectures

An extended breakdown for the sub-array architectures is pictured in Figure 6.2 without the equality constraint on the number of RF chains and users, i.e. with

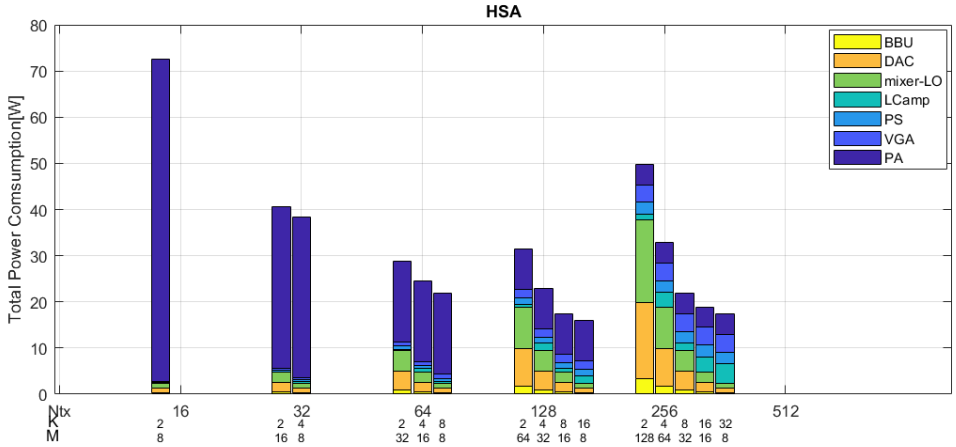
$$M = \frac{N_{TX}}{K} \geq U$$

For a fixed number of antenna elements N_{TX}, the total power consumption of SDMBA and HSA show widely different trends with an increasing number of sub-array elements K (or equivalently, decreasing number of RF chains M). This is because in the SDMBA architecture, a higher sub-array size imposes large $P_{out_{PA}}$ on the system, whereas in the HSA architecture, each sub-array antenna element has a dedicated PA, hence $P_{out_{PA}}$ remains constant for a fixed value of total antenna elements N_{TX}.

Furthermore, sub-array architectures also show characteristic radiation properties. As the sub-array size K increases, the sub-array beam becomes more focused, which may be beneficial when there are a large number of users U. At the same time, the distance between sub-array centres may also increase, particularly for uniform linear arrays (ULAs); this creates grating lobes that impose limitations on the scanning range of the antenna array. Users who are further away from the broadside will experience interference from the grating lobes.



(a) SDMBA



(b) HSA

Figure 6.2: Power consumption breakdown for sub-array architectures for all sub-array configurations, with the number of sub-array elements K and number of RF chains M indicated (Case 3, $BW = 400$ MHz, $EIRP = 40$ dBm, $U = 8$).

The SDMBA architecture shows a substantial increase in power consumption at $K = 16$. The reason for this is the splitting network introduced between the FEM PA and the antenna elements. Each 1:2 power divider introduces a loss of $IL = 1$ dB; consequently, for 16 sub-array elements, the PA must provide an additional 15 dB output power to compensate for the loss. This phenomenon can be addressed by using fewer but more sophisticated power dividers with a larger number of output ports.

6.1.2 PA technology

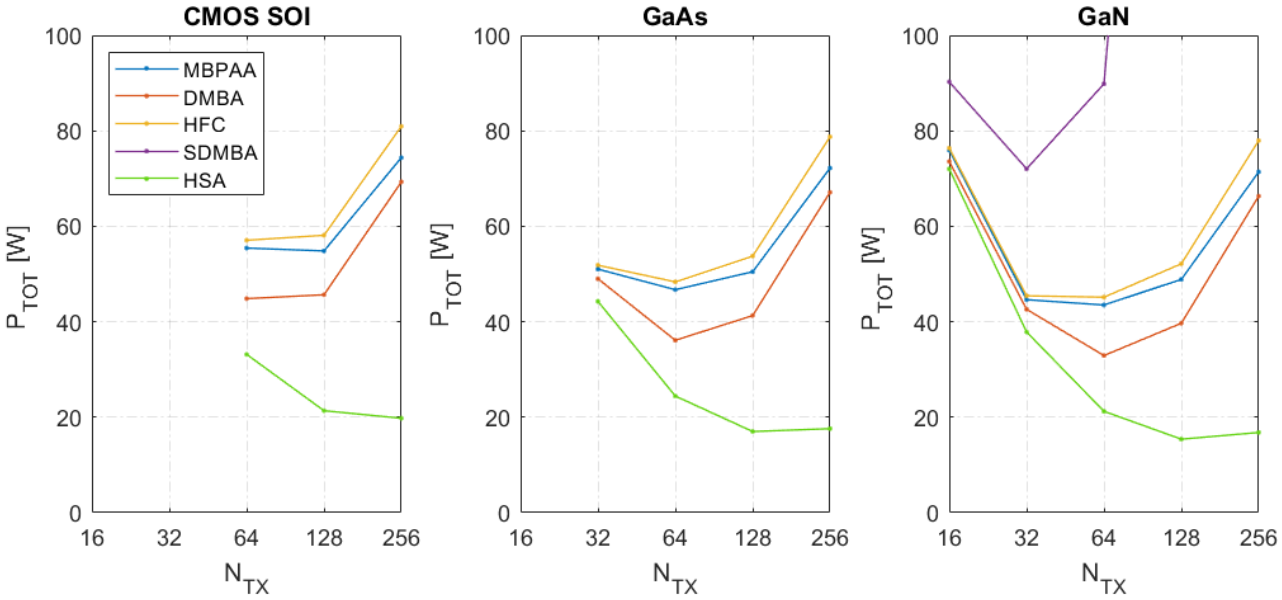


Figure 6.3: Total system power consumption with varying number of antenna elements and FEM PA technology (Case 1, $BW = 100$ MHz, $M = U = 8$, $EIRP = 40$ dBm).

Table 4.1 summarised the differences between GaN, GaAs and silicon technology-based PAs. In this chapter we proceed to analyse a selection of PA technologies, namely CMOS SOI, GaAs and GaN. Since the average PAE and P_{sat} of the Bulk CMOS and SiGe are close to that of CMOS SOI, their average power consumption is expected to be similar.

Figure 6.3 shows the total power consumption P_{TOT} of all five architectures, considering CMOS, GaAs and GaN PA technologies for Case 1 and $U = 8$. The curve for SDMBA using GaN has been cropped for better visual presentation, with the cropped data point being $P_{TOT} = 280$W at $N_{TX} = 128$. Arrays beyond $N_{TX} = 256$ are excluded based on our $P_{1dB_{PA}}$ lower bound (Equation 4.6).

Due to the higher efficiency of GaAs/GaN compared to CMOS, there is visible reduction in power consumption between 32 to 128 antenna elements using GaAs/GaN. The difference between technologies is less prominent for very small arrays i.e. $N_{TX} = 16, 32$ or for larger arrays i.e. $N_{TX} \geq 256$. This is because for these values of N_{TX}, the $P_{out_{PA}}$ term is very large (for small array size) or very small (for large array size) and dominates over the PAE term (Equation 4.4). Furthermore, GaN has the additional advantage of being able to support the high required $P_{out_{PA}}$ of SDMBA due to its high P_{sat}, while CMOS and GaAs are not able to do so.

Finally, for each type of PA technology, the fully digital DMBA architecture's power consumption lies between that of HSA and HFC. This finding reinforces the result in Section 6.1.1 that fully digital beamforming architectures do not necessarily consume more power than hybrid beamforming architectures.

For further context, Figure 6.4 presents the same setup but with $U = 32$ instead of $U = 8$. We observe that the power consumption rises more steeply with array size in this setup. The reduction in power consumption with the increase in PA technology efficiency is the least for

HSA. Additionally, GaAs technology is now able to support the SDMBA architecture when the $N_{TX} = 128$, which is within the massive MIMO range of array sizes. The influence of PA technologies is therefore more pronounced when the number of RF chains increases.

Table 6.1 highlights the power savings achieved by GaAs/GaN over CMOS, at (close to) the optimal array size for a selection of architectures.

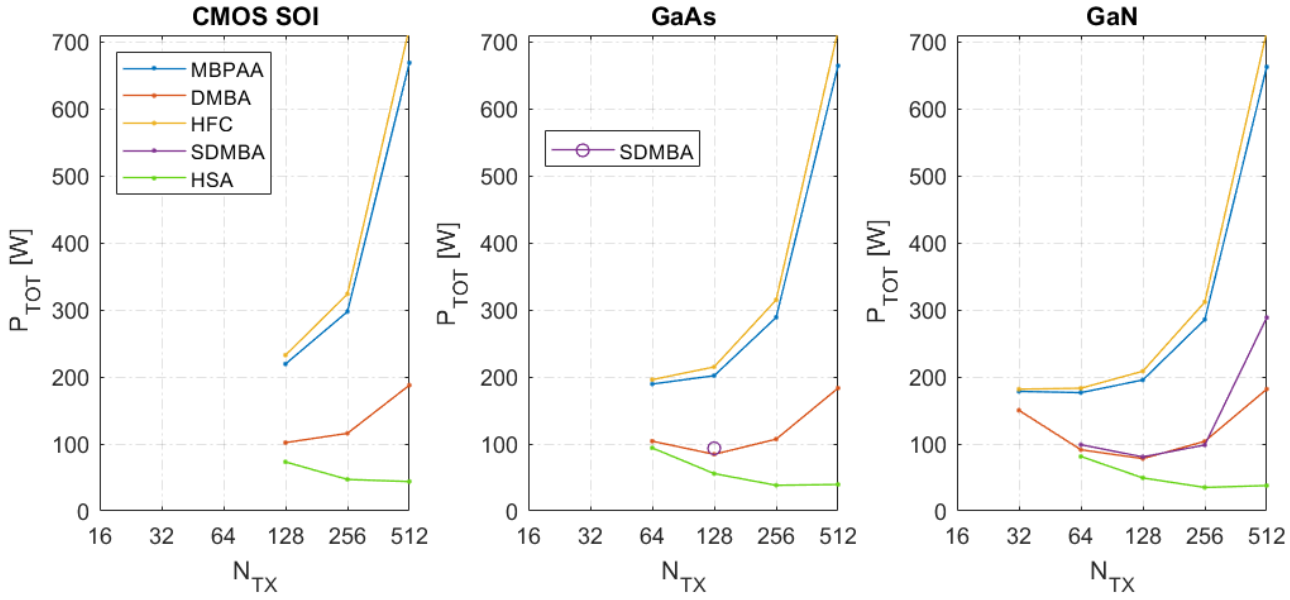


Figure 6.4: Total system power consumption with varying number of antenna elements and FEM PA technology (Case 1, $BW = 100$ MHz, $M = U = 32$, $EIRP = 40$ dBm).

Table 6.1: Total power savings by switching from CMOS SOI to III-V PA technology, for Case 1 and $EIRP = 40$ dBm.

	N_{TX}	CMOS	GaAs	GaN
HSA, $U = 8$	128	-	4.3 W	5.9 W
MBPAA, $U = 8$	64	-	8.1 W	1.1.3 W
DMBA, $U = 8$	64	-	8.7 W	12.9 W
HSA, $U = 32$	256	-	5.6 W	8.8 W
MBPAA, $U = 32$	128	-	17.4	23.8 W
DMBA, $U = 32$	128	-	17.5 W	24 W

6.1.3 Number of users

As the number of simultaneous users U increases with a fixed value of EIRP per beam, there are two main impacts: first, assuming $M = U$ (Equation 3.19), the number of RF components increases proportionally; second, the required $P_{out_{PA}}$ increases (Equations 3.18 and 4.1). In the case of digital and hybrid architectures, increasing the number of users also leads to an increase in digital signal processing (Equation 4.22).

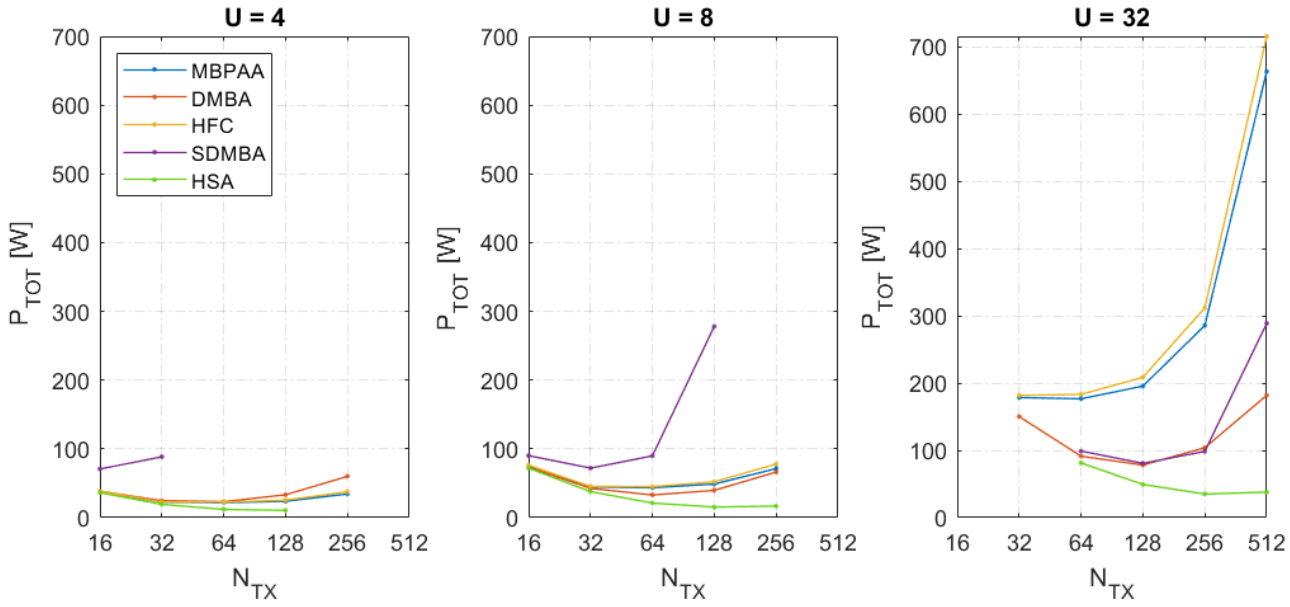


Figure 6.5: Total system power consumption with varying number of antenna elements and number of simultaneous users (Case 1, $BW = 100$ MHz, $EIRP = 40$ dBm, PA: GaN).

Figure 6.5 shows the total power consumption for $U = 4$, 8 and 32 users, for Case 1 and $EIRP = 40$ dBm. As expected, P_{TOT} increases with the number of simultaneous users for all architectures, but the magnitude of increase differs per architecture. When the array size is small, the difference stems primarily from the increase in $P_{out_{PA}}$. However, as the array size increases, the PA requirements decrease, and it is the large number of RF amplifiers that drives up the power consumption. For example, at $N_{TX} = 256$, increasing U from 8 to 32 leads to an increase of 92W in P_{VGA}, and 43W in P_{RFamp}. Figure 6.6 illustrates this difference.

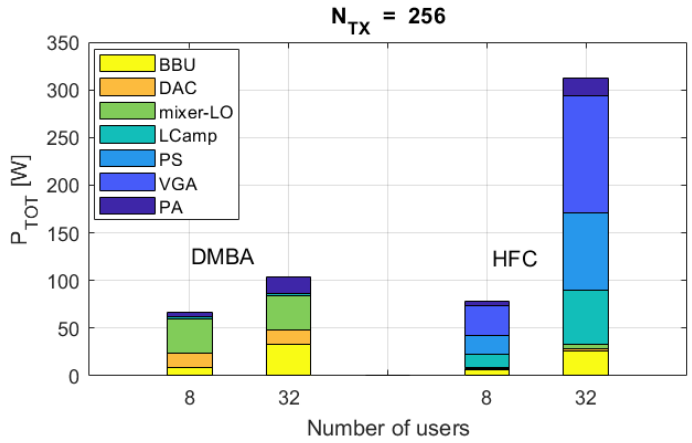


Figure 6.6: Power consumption breakdown for DMBA and HFC (Case 1, $BW = 100$ MHz, $EIRP = 40$ dBm, PA: GaN)

For a fixed value of N_{TX}, the increase in power consumption with U is the least for HSA, moderate for DMBA, and significantly large for the fully connected analog/hybrid architectures

wherein it increases by a factor of approximately

$$\Delta U = \frac{U_2}{U_1} \qquad U_2 > U_1 \tag{6.1}$$

Increasing the number of users has a demonstrable positive impact on digital beamforming architectures, as seen in Figure 6.6. For a low number of users i.e. $U \leq 4$, DMBA has a higher power consumption than MBPAA and HFC. As the number of users increases to $U = 8$, the power consumption of DMBA drops below that of MBPAA and HFC.

For SDMBA and a given array size N_{TX}, an increase in U corresponds to a decrease in the number of antenna elements per sub-array (K), and consequently, a decrease in the number of splitters after each PA. This reduces the PA's required output power by a factor of ΔK dB,

$$\Delta K = K_1 - K_2 \qquad K_1 > K_2 \tag{6.2}$$

where K_1, K_2 denote the number of sub-array elements associated with U_1, U_2 respectively. Since the PA requirements are lower, its power consumption P_{PA} subsequently decreases by a factor of $10^{\Delta K/10}$. The decrease in PA requirements with U compensates for the increase in power consumption from the higher number of RF chains, which does not occur with the other architectures.

When the number of users is high at $U = 32$, digital architectures outperform the fully connected architectures by more than 100W at their respective optimal points. Furthermore, SDMBA's power consumption is comparable to that of DMBA for a high number of users, and even drops below DMBA at $N_{TX} = 256$. Put differently, as the number of RF chains increases, SDMBA comes closer to being the preferred digital beamforming choice.

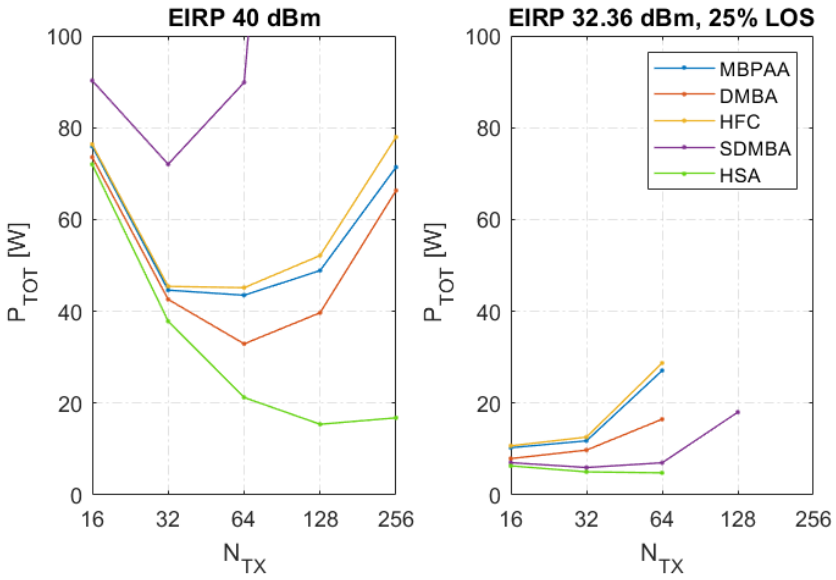
The trend of HSA's power consumption is different from the rest. The power consumption curve of HSA stays approximately flat for $N_{TX} \geq 128$. Since sub-array architectures see RF performance improvements with a smaller sub-array size, this finding signifies that there may be an acceptably small penalty in power consumption by moving from the optimal array size to a smaller number of array or sub-array size, provided $N_{TX} \geq 128$.

6.1.4 EIRP and LOS%

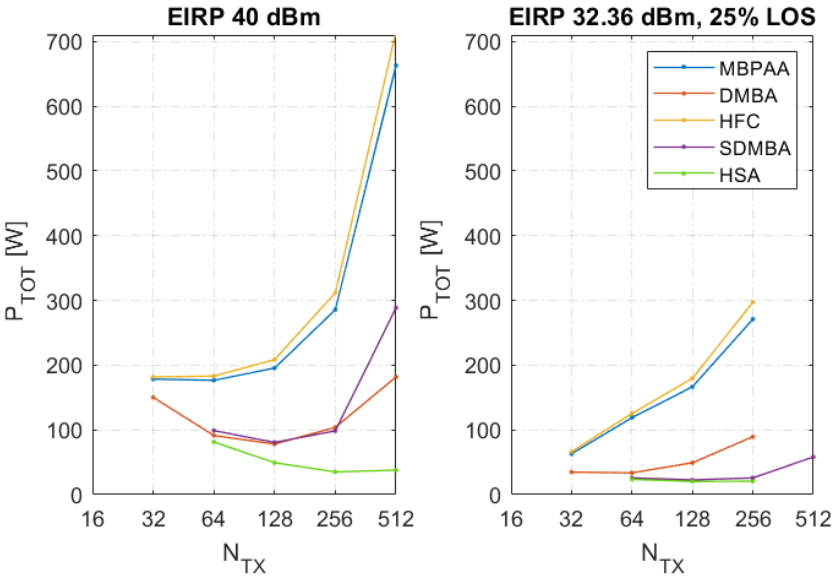
The PA power consumption is a function of the EIRP per beam (Equation 4.1). The analysis so far used a fixed $EIRP = 40$ dBm based on 3GPP recommendations, as it is high enough to accommodate fully NLOS links at a distance of 100m from the BS. In this section, using Case 1 as an example, we investigate the impact of a reduced EIRP on the total power consumption.

The link budget estimation in Section 3.4 found that for a line-of-sight probability of 25%, the per-beam EIRP for Case 1 ($BW = 100$ MHz) is a moderate 32.36 dBm. With the decrease in transmission power, we expect the total power consumption P_{TOT} to also have decreased irrespective of the architecture, PA technology, or number of users. Since the PA output power plays a dominant role at smaller array sizes and fades in importance for large array sizes, it is expected that the impact of lowering the EIRP will be more prominently visible for smaller arrays. Similarly, a lower EIRP is expected to lead to a greater relative improvement in P_{TOT} for SDMBA and HSA as compared to the other architectures, due to the stronger influence of the PA output power on these architectures. These hypotheses are validated in figures 6.7a-6.7b,

which compare the total power consumption when $EIRP = 40$ dBm and $EIRP = 32.36$ dBm.



(a) $M = U = 8$.



(b) $M = U = 32$

Figure 6.7: Total system power consumption with varying number of antenna elements for low and moderate EIRP per beam (Case 1, $BW = 100$ MHz, PA: GaN).

As expected, lowering the EIRP has a significant impact on SDMBA. In the high EIRP scenario, SDMBA requires at least 32 RF chains to achieve a P_{TOT} comparable to DMBA, but in this moderate EIRP scenario, the SDMBA power consumption achieves comparable performance with just 8 RF chains. Furthermore, when the number of RF chains increases to 32 as in Figure 6.7b, the P_{TOT} drops even more until it becomes comparable to HSA, which so far offered unparalleled power consumption performance.

Additionally, this means in the low EIRP regime, SDMBA offers a good alternative to DMBA and HSA for a moderate and high number of users respectively. It offers the benefit of cost-

efficiency compared to both DMBA and HSA, and achieves its optimal value at a lower array size (i.e. for a fixed number of RF chains, or a smaller sub-array size) than HSA, which gives it a relative RF performance boost. However, if low EIRP cannot be reliably maintained, which is anticipated to be the case for eMBB, HSA and DMBA are the best choices of architecture.

6.1.5 Bandwidth

In Section 3.2, we defined three usage cases that are primarily distinguished by their signal bandwidth BW (see Table 3.2). The signal bandwidth affects three quantitative aspects of our power consumption model.

- At a system level, the EIRP per beam is determined partly by the bandwidth-dependent thermal noise in the propagation environment. A larger bandwidth requires a higher EIRP; if we use the standard EIRP of 40 dBm, however, this aspect is discarded.
- At a component level, the DAC sampling frequency f_s increases with the bandwidth (Table 4.2).
- Also at the component level, the DSP power consumption is proportional to the bandwidth (Equation 4.22).

Hence, as we move from Case 1 to Case 3, we expect to see an increase in power consumption due to the increasing bandwidth. Figure 6.8 shows the total power consumption for Case 3, $U = 8$ and various FEM PA technologies. The SDMBA architecture cannot be supported by CMOS SOI and GaAs in this use case, and is thereby missing from their respective plot. The figure can be compared to Case 1 in Figure 6.3.

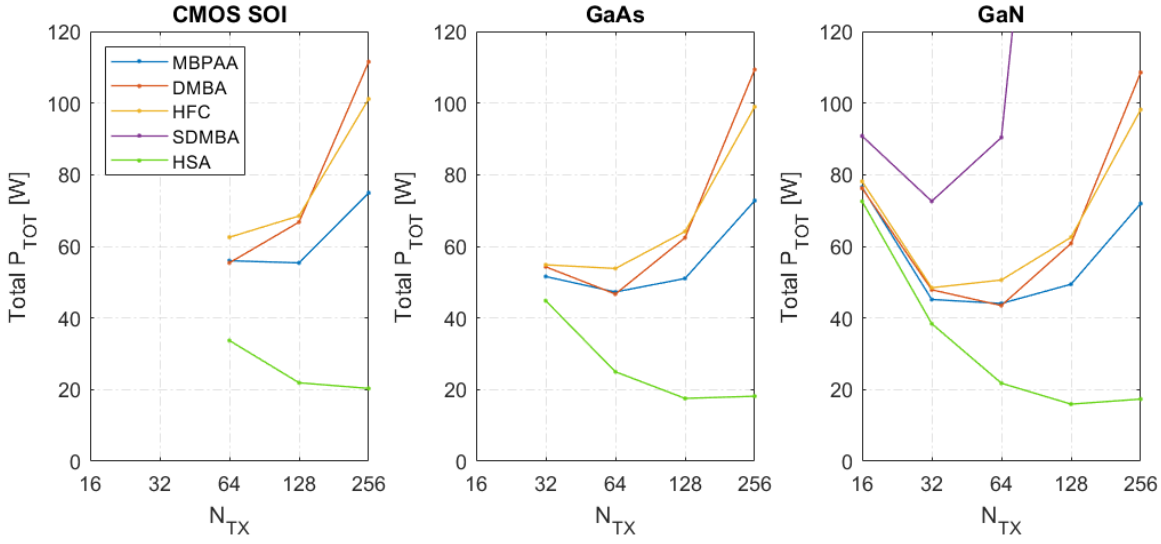


Figure 6.8: Total system power consumption with varying number of antenna elements and FEM PA technology (Case 3, $BW = 400$ MHz, $M = U = 8$, $EIRP = 40$ dBm).

We observe that for each PA technology and architecture, the general shape of the P_{TOT} curve is similar up to the optimal N_{TX}, after which the P_{TOT} rises more steeply in Case 3. The optimal array size remains nearly unchanged between Case 1 and Case 3, for all technologies and architectures except one (HFC with GaN PA). Finally, similar to Case 1, the SDMBA

architecture is not feasible with CMOS or GaAs for $U = 8$ due to their insufficient P_{sat}.

The change in BW affects DMBA the most, due to the large number of DACs and DSP operations that comprise this architecture. As a result, the gap between DMBA and MBPAA at their optimal point diminishes from about 10W in Case 1 to 0.6W in Case 3.

Similarly, the gap between HFC and MBPAA widens in Case 3, due to the increase in the former's DSP power consumption.

Finally, HSA is only slightly affected by the increase in bandwidth, due to the low number of DACs compared to DMBA, and the lower number of DSP operations compared to HFC or SDMBA.

Case 2 has a bandwidth $BW = 200$ MHz, and follows the same trends as outlined above, with its P_{TOT} curves lying between Case 1 and Case 3. The findings in this section also hold for varying different values of U and EIRP.

6.1.6 Key Takeaways

The key observations and conclusions from Sections 6.1-6.1.5 are enumerated below.

1. **Lowest power consumption:** For nearly all the discussed use cases, the flexible-sub-array hybrid architecture (HSA) displayed the lowest relative power consumption, usually with $P_{TOT} < 50$W for up to 8 users and/or 40 dBm EIRP, and $P_{TOT} < 100$W for 16-32 users and/or 32 dBm EIRP. The power consumption of HSA reduces with an *increasing* sub-array size K, which presents a trade-off with the array's RF scanning range and interference suppression.

2. **Highest power consumption:** Either the fixed sub-array digital (SDMBA) or the fully-connected hybrid (HFC) architecture had the highest power consumption, depending on the number of users and EIRP. Additionally, the model's output reinforces recent claims in the literature that the fully digital architecture (DMBA) does not always necessarily consume more power than the analog or hybrid architectures.

3. **Component power contribution:** The immensely large number of RF amplifiers, phase shifters and mixer-LO components for array sizes between 64-512 (i.e. the massive MIMO range) have a substantial impact on the total power consumption of the system. For example, the loss compensation amplifiers and VGAs together consume nearly 45 W (45% of the total power budget) in Case 3 with 8 users (Fig 6.1b). These components have not received much attention in the literature from the perspective of power consumption.

4. **PA technology:** The use of GaN and GaAs PAs leads to a lower power consumption compared to CMOS PAs, and with a smaller optimal value of N_{TX}. Depending on the architecture, GaN offers a minimum of 8.8-24W power savings over CMOS (Table 6.1). Additionally, GaN PAs are better equipped to handle signals with a higher peak-to-average power ratio (PAPR) than the 6 dB PBO used in this model. Meanwhile, if larger array sizes are necessary due to RF performance requirements, CMOS PAs are favoured because their optimal P_{TOT} point occurs for larger array sizes, along with their cost efficiency.

5. **Number of users:** In our analysis, we assume that the number of users is equal to the number of RF chains, i.e. $M = U$ (Equation 3.19). The total power consumption increases with the number of users for all architectures. The amount of increase is larger for analog beamforming architectures, due to the corresponding increase in RF amplifiers and phase shifters (Figure 6.6). For a high number of users i.e. $U = 32$, SDMBA becomes an attractive choice of architecture, achieving parity with DMBA at their respective optimal points.

6. **EIRP:** The power consumption reduces with EIRP as a result of reduced PA requirements. The impact of lowering the EIRP is more prominent for smaller array sizes, where the EIRP-dependent P_{PA} dominates the power budget. In the low-to-moderate EIRP regime, SDMBA becomes an attractive choice of architecture, achieving parity with DMBA (with $U = 8$ users) or even with HSA (with $U = 32$ users).

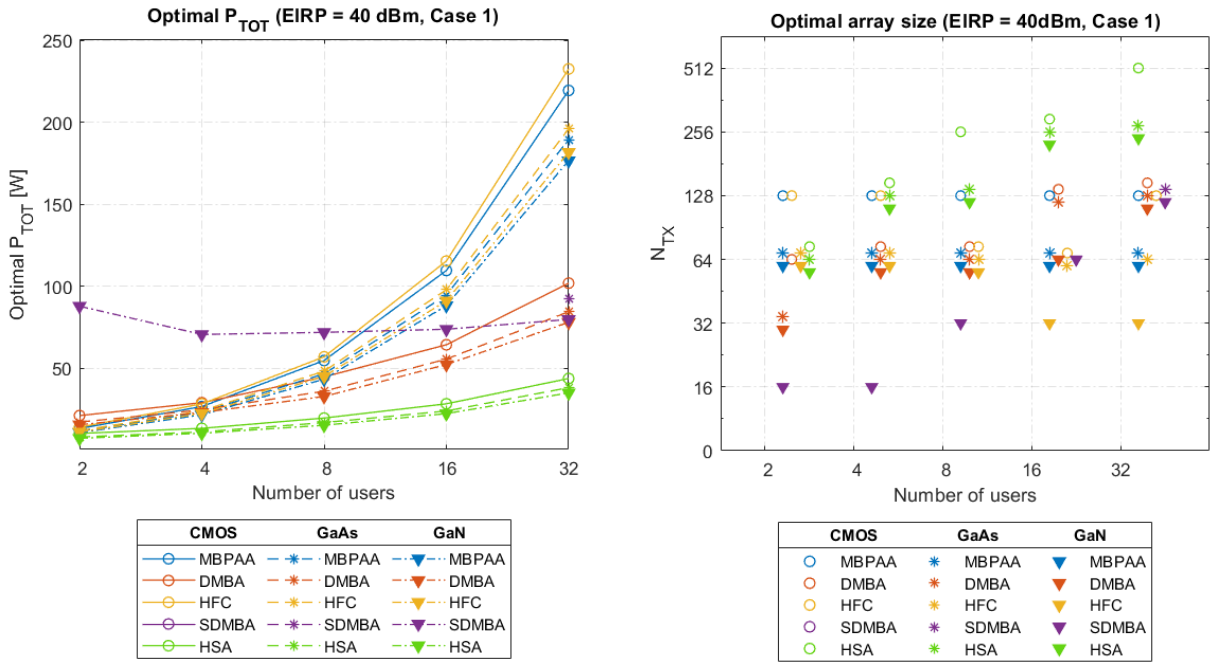
7. **Bandwidth:** The power consumption increases with the bandwidth, due to the increase in P_{BBU}, P_{DAC} and P_{PA}. Architectures such as DMBA are impacted more acutely by a change in bandwidth, due to the large number of DSP operations, DACs and PAs that characterise its topology.

6.2 Optimal Power Consumption

As observed in earlier sections, for each combination of architecture and use case, there is almost an optimal number of antenna elements N_{TX} where the resultant total power consumption is at its lowest for that specific combination of architecture and use case. In this section, the optimal point of each architecture is revisited in greater depth. Section 6.2.1 covers the magnitude of the total power consumption and the corresponding array size. Following this, Section 6.2.2 compares the power consumption *per user*, as a measure of the architecture's efficiency.

6.2.1 Optimal Total Power Consumption and Array Size

Figures 6.9-6.11 show the optimum point of each architecture for Cases 1, 2 and 3 respectively, with respect to the FEM PA technology and number of users U. First, the magnitude of optimal power consumption is discussed independently. Next, the optimal array size is considered together with the optimal power consumption. Lastly, we remark on the differences due to FEM PA technology. At each instance, the sub-array size can be derived as $K = N_{TX}/U$.

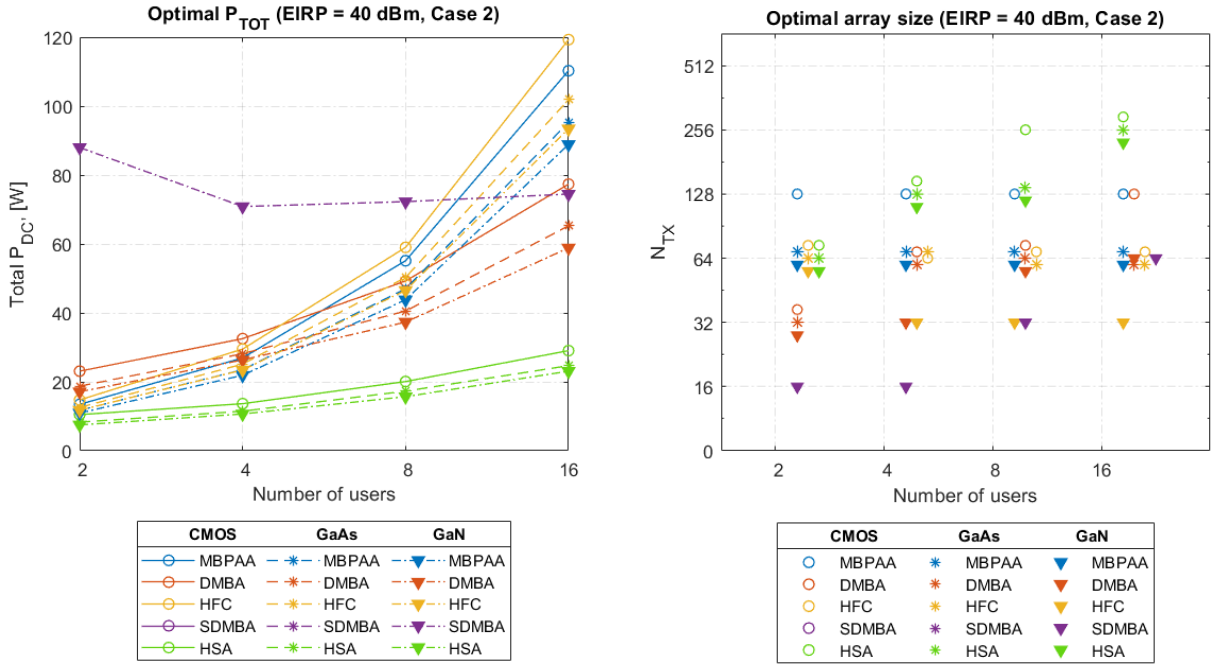


(a) (b)

Figure 6.9: The optimal power consumption and array size (Case 1, $BW = 100$ MHz, $EIRP = 40$ dBm).

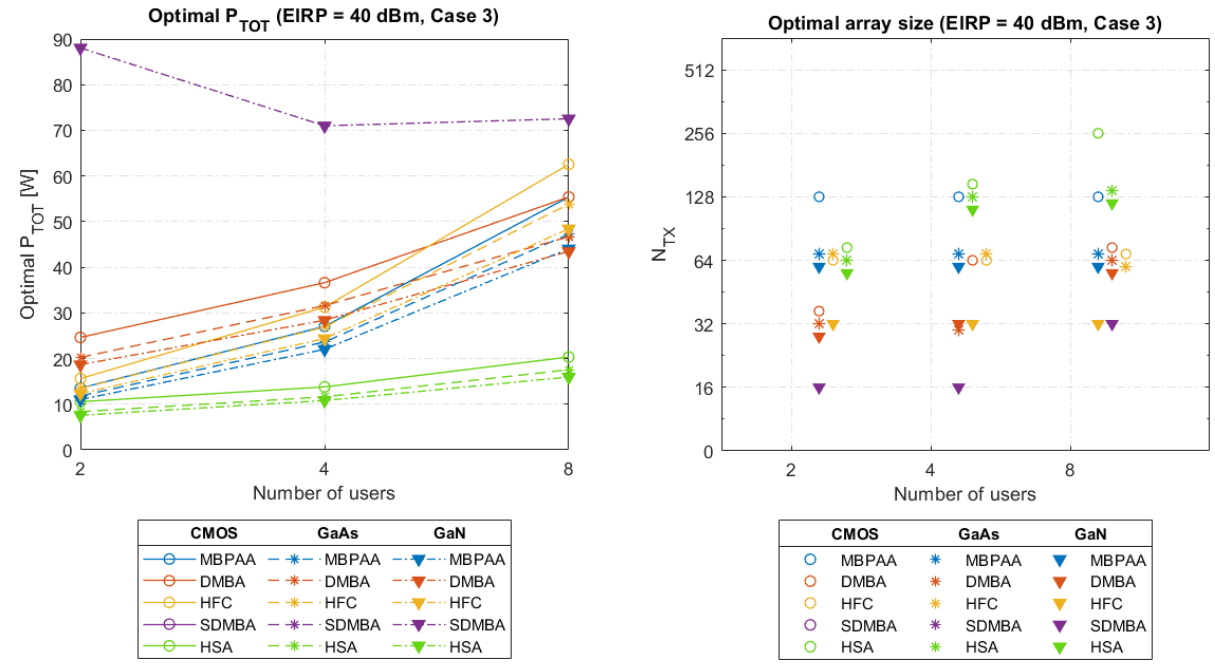
Optimal Total Power Consumption

Figures 6.9a, 6.10a and 6.11a show that the optimal value of total power consumption P_{TOT}(W) increases monotonically with U. The exception is SDMBA, for which the optimal P_{TOT} remains fairly stable as the number of users increases. The optimal P_{TOT} of SDMBA varies between 70.7-88.9W for GaN technology, and reaches 92.6W for GaAs for a single point at $U = 32$. The



(a) (b)

Figure 6.10: The optimal power consumption and array size (Case 2, $BW = 200$ MHz, $EIRP = 40$ dBm)



(a) (b)

Figure 6.11: The optimal power consumption and array size (Case 3, $BW = 400$ MHz, $EIRP = 40$ dBm)

optimal number of antenna elements per sub-array is $K = 8$ for $U = 2$, and $K = 4$ for $U > 2$.

For $U < 32$, the DMBA architecture has a lower power consumption than SDMBA by 21-73W depending on U, even though it has $\frac{N_{TX}}{U}$ times the number of components. This is a result of the high PA output power requirements imposed on the SDMBA architecture, by needing a single PA for K antenna elements. The gap between them decreases with increasing U, as the power consumption of DMBA rises to meet higher DSP demands.

Optimal Number of Antenna Elements

The optimal N_{TX} in Figures 6.9b, 6.10a and 6.11b shows very different trends, depending on the architecture, for increasing U and choice of PA technology. The optimal value occurs at $N_{TX} = 64$ or 128 for most architectures and the number of users. This is the lower end of massive MIMO array sizes. The reason for this is the excessive power consumption of various circuit components at the higher end of massive MIMO array sizes i.e. for 256+ elements.

At higher values of U, the optimal N_{TX} is correspondingly higher for DMBA, SDMBA and HSA. The optimal number of antennas for HFC drops to lower array sizes as U increases, which is explained by the increase in P_{PS} and P_{BBU} leading to a steeper rise in circuit power consumption.

The HSA architecture has consistently shown the lowest values of power consumption among all the beamforming architectures in all use cases. As a trade-off, its optimal array size is the largest among all the architectures.

Optimal PA technology

For CMOS technology, the optimal point generally occurs at a high value of N_{TX}, using between 128- 512 antenna elements. Despite this large number, the cost-efficiency and low form factor of CMOS make it possible to implement such large arrays without the steep costs associated with III-V technologies.

By contrast, for the same architectures and number of users as CMOS, the GaAs and GaN technologies generally require an array that is half that size to achieve the optimal P_{TOT}. Additionally, due to their higher PAE, their optimal P_{TOT} also has a lower magnitude than that of CMOS. Therefore, by using GaAs or GaN technology in the FEM PA, it is possible to simultaneously reduce the array size as well as the total power consumption. This can be leveraged for architectures like DMBA, where having hundreds of RF chains would be prohibitively expensive or complex; or for a large number of users $U \geq 16$, where several orders of lossy power dividers/combiners may be needed. These findings hold for Cases 2 and 3, portrayed in Figure 6.10 and Figure 6.11 respectively. The main differences as we move from Case 1 to Case 3 are:

- The magnitude of optimal power consumption increases.
- The optimal array size moves to smaller values of N_{TX}.

6.2.2 Optimal Per-User Power Consumption

In the previous section, we discussed the optimal power consumption with respect to the number of antenna elements, for each value of U, where we observed that the power consumption is

lowest for $U = 2$. However, this low number of users may be insufficient for the eMBB scenario, where they may be up to 32 users in a single picocell sector. Therefore, additional information is needed to make the best selection of architecture and PA technology.

In this section, consider the previously derived optimal total power consumption from a *per-user* perspective, as

$$\text{Per-user optimal } P_{TOT_U} = \frac{\text{Optimal } P_{TOT}(U)}{U} \tag{6.3}$$

where $P_{TOT}(U)$ represents the total power consumption for U users at its optimal point, as derived in the previous section. The per-user total P_{TOT} represents the system's efficiency, and is a useful metric not only for the design and implementation of the 5G transmitter, but also for relating the power consumption of the 5G transmitter to the projected expansion of the 5G network in the upcoming years.

Figure 6.12 presents the optimal per-user power consumption P_{TOT_U} for Case 1 and various PA technologies. The curve for SDMBA using GaN has been cropped for better visual presentation, with the cropped data point being $P_{TOT} = 43.96$ W at $U = 2$. It can be noticed that the fully-connected analog/hybrid architectures show a slight increase in per-user P_{TOT} as the number of users increases; on the other hand, the digital multi-beam array and phased sub-array-based hybrid array become more efficient as the number of users increases.

Table 6.2 encapsulates the improvement (i.e. the reduction) in per-user power consumption for HSA, DMBA and SDMBA as the number of users changes from $U = 2$ to $U = 8$ and $U = 32$. As mentioned earlier, $U = 8$ simultaneous beams is at the moment the most likely use case for the eMBB scenario. On the other hand, $U = 32$ can be seen as a future scenario. We observe that SDMBA shows an 80% improvement in per-user power consumption when generating 8 simultaneous beams as compared to the baseline. Similarly, DMBA shows a 47% improvement over the baseline when generating 8 simultaneous beams, and an additional 41% improvement when generating 32 beams.

Table 6.2: Improvement in optimal per-user P_{TOT} by increasing the number of users (Case 1, $B = 100$ MHz, $EIRP = 40$ dBm).

	Increase in U	CMOS SOI	GaAs	GaN
HSA	2 (baseline)	-	-	-
	$2 \rightarrow 8$	54%	49%	49%
	$8 \rightarrow 32$	46%	43%	43%
DMBA	2 (baseline)	-	-	-
	$2 \rightarrow 8$	47%	48%	47%
	$8 \rightarrow 32$	41%	42%	39%
SDMBA	2 (baseline)	-	-	-
	$2 \rightarrow 8$	-	-	80%
	$8 \rightarrow 32$	-	-	72%

For Case 2 and Case 3, the per-user power consumption behaves similarly to Case 1. The full set of figures may be found in Appendix C.

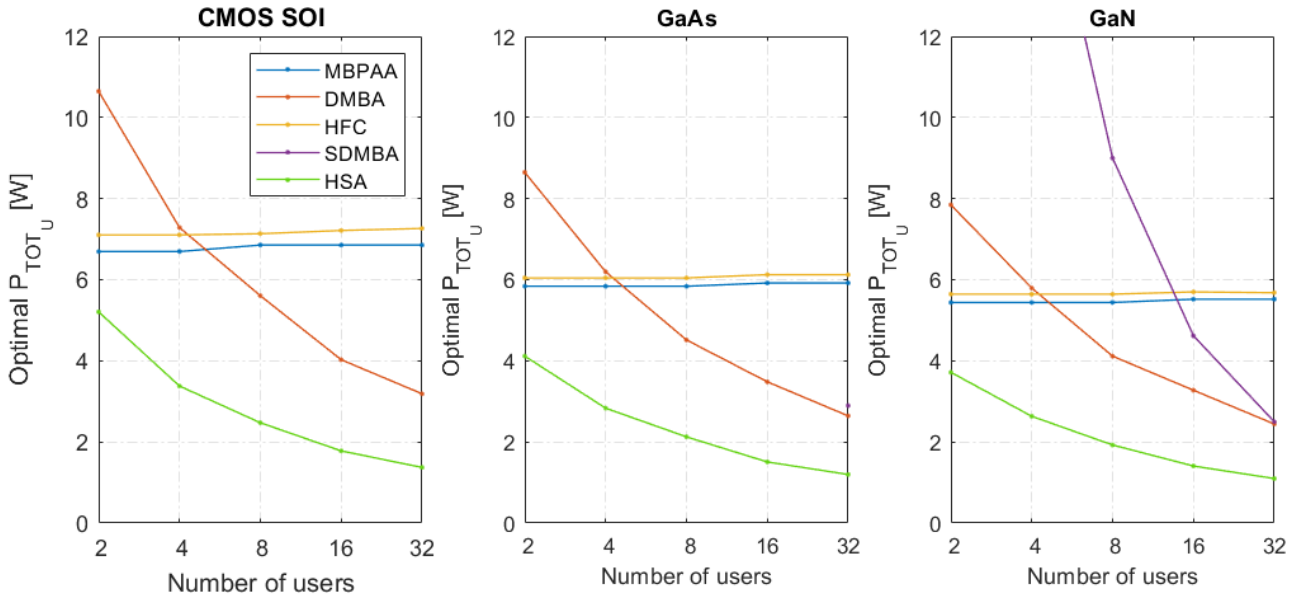


Figure 6.12: Optimal power consumption per user
(Case 1, $BW = 100$ MHz, $EIRP = 40$ dBm)

6.2.3 Key Takeaways

The key observations and conclusions from Section 6.2.1 are enumerated below.

1. **Optimal power consumption:** All architectures have an optimal P_{TOT} that increases monotonically with U (with the exception of SDMBA). The magnitude of P_{TOT} is between $5-30$ W for $U = 2$, which is a very low number of users for our eMBB scenario; it increases to a range of $15 - 75$ W for a more realistic $U = 8$.

   The SDMBA architecture has an unusual P_{TOT} curve at the optimal point; it remains stable around 70 W for $U \geq 4$. This is due to its unique topology, where the splitting network structure is the main feature responsible for the power consumption of this architecture (Section 6.1.3).

2. **Optimal array size:** For the HSA, DMBA and SDMBA architecture, as the number of users increases, the optimal point moves towards the higher range of massive MIMO array sizes. These are also the three architectures that show an exponential decrease in the per-user optimal P_{TOT}.

   MBPAA shows little variation in its optimal array size as the number of users increases, while the corresponding value of power consumption increases exponentially with the number of users. HFC shows a similar trend, except when $U = 32$ in Case 1, where the HFC optimal array size differs widely based on the PA technology.

3. **Influence of Bandwidth:** Higher bandwidths result in elevated values of P_{TOT}, hence, Case 1 shows the lowest power consumption and Case 3 the highest. At the same time, optimal array size for all architectures tends to drop to lower values of N_{TX}, implying that the power consumption contribution of the bandwidth-dependent components (baseband unit and DAC) increases sharply.

4. **Influence of PA technology:** GaN PAs are associated with lower optimal array sizes ($N_{TX} \in [16, 64]$), while CMOS PAs tend towards higher optimal array sizes ($N_{TX} \in [64, 256]$). This is a consequence of P_{PA} decreasing more rapidly when the efficient GaN PAs are used, compared to CMOS PAs.

5. **Per-user power consumption:** For all PA technologies, the per-user power consumption of fully-connected analog/hybrid architectures remains nearly constant in the range of $5.8 - 7$ W. On the other hand, there is an exponential decrease in per-PA power consumption for HSA, DMBA and SDMBA with U, which makes them more energy efficient for a higher number of users.

6.3 Recommendations on Optimal Architecture, Array Size and FEM Technology

Several recommendations can be made on the choice of the best architecture and FEM technology using the results on the optimal power consumption and array size, for a selection of use cases that are most likely under the eMBB scenario. The recommendations are differentiated based on the overarching EIRP, where we first consider the standard 40 dBm case, and then a moderate to low EIRP with 25% LOS.

Tables 6.3-6.4 propose several of the best beamforming schemes, number of antenna elements and FEM technologies with respect to the optimally low power consumption. The value of optimal total power consumption P_{TOT} is stated for each proposal. These recommendations demonstrate the trade-off between array size, technology cost, RF properties related to N_{TX} and K, and the flexibility required by 5G BS beamforming architectures. From these recommendations, the optimal combination is highlighted, and accompanied by a brief justification.

6.3.1 Standard 40 dBm EIRP Scenario

In the high EIRP scenario, we notice that the optimal number of antenna elements (AE) is 64-128, which is in the lower range of massive MIMO array sizes.

Despite the low power consumption of HSA, the corresponding large sub-array size K with respect to the total N_{TX} results in a degraded RF performance. This is particularly relevant for high U, and HSA therefore does not feature as the optimal choice. On the other hand, the higher per-user efficiency and low power consumption of DMBA places it at an advantage for this use case for $U \geq 8$. MBPAA and HFC are optimal architectures when the number of users is low i.e. $U < 8$.

Silicon-based technologies are revealed as potential candidates for Case 1 and $U \leq 16$. For higher PA requirements, where possible, GaAs FEM technology is preferred over GaN due to the former's lower cost and often comparable optimal P_{TOT}. However, the favour shifts towards GaN if there is an increase in signal PAPR, a higher number of users, or an emphasis on low form factor compared to GaAs.

The optimal choice depends greatly on the key differentiating factors between use cases, and the priorities of the antenna designer. For e.g., for the high bandwidth in Case 3 and with a high number of users $U = 32$, good RF properties take precedence over minimal power consumption,

EIRP = 40 dBm									
BW R_{user}	Case 1: 100 MHz 300 Mbps			Case 2: 200 MHz 780 Mbps			Case 3: 400 MHz 1.09 Gbps		
U	8	16	32	4	8	16	2	4	8
MBPAA	GaN 43.5 W			GaAs 25.2	GaN 43.8 W		Si-based 13.5 W 128 AE	GaAs 23.7 W 64 AE	GaAs 47.23 W
DMBA	Si-based 45 W 64 AE	Si-based 64.5 W 128 AE	GaAs 84.5 W 128 AE	GaAs 28.2 W	GaAs 40.5 W 64 AE	GaAs 65.3 W 64 AE			GaAs 46.7 W 64 AE
HFC	GaN 45.2 W			GaAs 25.2 W 64 AE	GaN 47 W		GaAs 13.5 W	GaN 24.4 W	GaN 48.5 W
SDMBA		GaN K = 4 74 W	GaN K = 4 80 W			GaN K = 4 75 W			
HSA			GaAs K = 8 38.5 W						
Details	Low P_{TOT} , more flexible array and low cost	Low P_{TOT} , more flexible array	More flexible array and good RF properties	Low P_{TOT} and good RF properties	Low P_{TOT} and low cost	Low P_{TOT} and low cost	Low P_{TOT} and low cost	Low P_{TOT} and good RF properties	Low P_{TOT} and good RF properties

Table 6.3: Optimal beamforming scheme, number of antenna elements and FEM technology using a high EIRP. Si-based technologies encompass Bulk CMOS, CMOS SOI and SiGe.

and therefore, HSA is not designated as the optimal choice, despite its power consumption being 54% lower than the recommended DMBA.

6.3.2 Moderate to High EIRP Scenario

In the moderate-high EIRP scenario with 25% LOS, the optimal array size for DMBA reduces to 32 antenna elements, which is much lower than the massive MIMO range of antenna array sizes.

Silicon-based technologies become preferred candidates for Case 1 and Case 3. For this EIRP, every architecture but SDMBA can be implemented using Si-based FEMs and 32-128 antennas, resulting in cost savings compared to the III-V alternatives.

Lastly, the sub-array architectures are placed at an advantage due to their sensitivity to changes in the EIRP. The architecture with a lower power consumption and low sub-array size together are preferred. HSA can serve 32 users with a low power consumption of only 20.5 W. However, Si-based FEMs are not optimal with sub-array architectures.

EIRP = 32 dBm, 25% LOS				EIRP = 37.5 dBm, 25% LOS		
BW R_{user}	Case 1: 100 MHz 300 Mbps			Case 3: 400 MHz 1.09 Gbps		
U	8	16	32	2	4	8
MBPAA	Si-based 20 W	Si-based 40.1 W		Si-based 8.3 W 64 AE	Si-based 21.5 W 128 AE	
DMBA	Si-based 14.8 W 32 AE	Si-based 27.7 W	Si-based 41.9 W		Si-based 23.4 W	Si-based 42.5 W 32 AE
HFC	Si-based 20.7 W	Si-based 41.7 W		Si-based 9.2 W	Si-based 27.4 W	
SDMBA	GaAs K = 4 13.9 W	GaAs K = 4 18.5 W 64 AE	GaAs K = 4 24.2 W			
HSA	Si-based K = 8 8.9 W	Si-based K = 8 13.1 W	GaN K = 4 20.5 W 128 AE			
Details	Low P_{TOT} and low cost	Low P_{TOT} and good RF properties	Low P_{TOT} and good RF properties	Low P_{TOT} , more flexible array and low cost	Low P_{TOT} , more flexible array and low cost	Low P_{TOT} and good RF properties

Table 6.4: Optimal beamforming scheme, number of antenna elements and FEM technology using a moderate-high EIRP and 25% LOS. Si-based technologies encompass Bulk CMOS, CMOS SOI and SiGe.

6.4 Conclusion

In this chapter, we focused on steps 6-7 of the modelling methodology (Figure 2.4). The key takeaways on the parametric analysis of the total power consumption are elaborated in Section 6.1.6, while the notable observations regarding the total and per-user optimal power consumption are described in Section 6.2.3. This section gathers the key conclusions from the recommendations on optimal architecture and technology.

- The recommendations on optimal architecture and technology illuminate the advantages of the DMBA architecture, which provides a balance between low power consumption, good RF properties and high flexibility.
- GaN FEMs are optimal when considered purely from a power consumption perspective, however, accounting for cost elevates GaAs as the optimal choice of FEM technology.
- The analysis on optimal technology underscores the potential of silicon-based FEMs (Bulk CMOS, CMOS SOI, SiGe), which have largely been set aside in the literature on 5G mmW BS power consumption modelling for their comparatively lower saturation power.
- When the number of sub-array elements K increases, HSA shows the lowest power consumption for every use case, but subsequently suffers from degraded RF performance. This makes it a sub-optimal choice for the eMBB scenario, which requires good RF performance in order to serve up to 32 users simultaneously.

- We observe that array sizes greater than $N_{TX} = 128$ may cease to be optimal with respect to power consumption when considered together with supplementary aspects such as cost and RF properties.
- Finally, we are reminded that these results are influenced by our assumption of $M = U$ (Equation 3.19).

The following chapter recapitulates the main themes, methodology and results of this thesis, and provides suggestions for improvements and future work.

Chapter 7

Conclusions and Future Work

This chapter recapitulates the thesis, including its methodology, key results, and contributions to the existing scientific literature. Following this, improvements to the proposed model are suggested, and potential directions for future investigation are put forth.

7.1 Conclusion

7.1.1 Relevance and Contributions

In recent years, there has been exponential growth in the telecommunications industry, especially in the 5th Generation (5G) mobile technology, whose future outlook indicates rapid large-scale adoption and a corresponding increase in the power consumption of the mobile network. This necessitates the use of accurate and application-specific power consumption modelling of the 5G array architectures, so as to make informed decisions on the design of low-power and energy-efficient systems.

This thesis makes three main contributions to the existing scientific literature on the topic:

1. A realistic, generalisable, modular and comparative power consumption model designed for 5G mmW multi-beam beamforming-based transmitter architectures in the 28 GHz band, and tailored to the eMBB scenario.

2. Using the model, a parametric study on the trade-offs, limitations and optimality of five beamforming-based transmitter architectures by applying the designed model to novel use cases.

3. Based on the parametric study, a set of recommendations on the best choice of beamforming scheme, antenna array topology, and FEM technology, based on expected future use cases in the eMBB scenario.

7.1.2 Methodology

The design and analysis of the presented power consumption model followed a systems approach. First, the system-level requirements were formulated, and a link budget was established. A high-level array topology was defined for five multi-beam transmitter architectures, namely MBPAA, DMBA, SDMBA, HFC and HSA, which are compared and contrasted all together for the first time in this thesis.

Next, the underlying components of the transmitter were individually modelled and integrated into the array topology to yield a system-level power consumption model. This included the inclusion and parametrisation of five different FEM technologies, namely Bulk CMOS, CMOS SOI, SiGe, GaAs and GaN, with respect to the beamforming architecture's requirements, which s a novel approach to PA technology selection.

The validation of the model against the existing results in the literature affirmed that the system power consumption is a convex function of the number of antenna elements in the architecture.

7.1.3 Key Results

The model was applied to a wide set of use cases which encompass the current and future state of 5G adoption. The key conclusions are:

- The immensely large number of RF amplifiers, phase shifters and mixer-LO components for array sizes between 64-512 (i.e. the massive MIMO range) have a substantial and unexpected impact on the total power consumption of the system. This leads to prohibitively large power consumption for fully-connected analog (MBPAA) and fully-connected hybrid (HFC) beamforming architectures when the number of antenna elements is large.

- The fully digital DMBA consumes less total power than the analog MBPAA and the hybrid fully-connected HFC when 8 or more users are being simultaneously served. This result challenges the pre-existing notion that digital architectures always consume more power than their analog or hybrid counterparts.

- When the number of users is very low, the optimal power consumption point of all architectures lies in the range of 5-30 W, which is low for the chosen eMBB scenario. The range of optimal power consumption increases to 15-75 W for a more realistic situation of 8 users.

- Depending on the architecture, GaN PAs offer a minimum of 8.8-24 W power savings over CMOS PAs and 3.2-6.5 W power savings over GaAs PAs. Further, they are also better equipped to handle high $PAPR$ and smaller antenna array sizes. However, the associated costliness makes GaN a sub-optimal choice of FEM technology compared to GaAs.

- The HSA architecture trades off unparalleled low power consumption with a relatively higher optimal array size, higher sub-array size (greater than 8 antenna elements per sub-array), and a corresponding degradation of its RF performance. This phenomenon is particularly relevant when the number of users is large, such as in the chosen eMBB scenario.

- The SDMBA architecture achieves parity with the extremely low power consumption of the HSA architecture in the low EIRP regime. This makes it the optimal choice when low EIRP can be reliably maintained.

The results and conclusions of this thesis are being written for an IEEE publication. Furthermore, interested readers can reproduce the system-level power consumption results using the Matlab code released in [90], and explore different designs or use cases.

7.2 Suggested Improvements to the Proposed Power Consumption Model

The model derived in this thesis was intended to be generalisable to the extent possible for various beamforming architectures and use cases, while simultaneously covering the major facets of the component characteristics inside the transmitter. However, similar to most systems projects, the generalisability naturally implies that a few aspects were left out of the investigation and can be integrated into the model in the future to improve its accuracy and expand its applicability. This section suggests improvements to the proposed model.

- The RF performance of the suggested optimal beamforming schemes and array topologies needs to be investigated, such as the beam pattern, interference, and multi-path effects. Currently, the model only considers the power consumption perspective, and puts forth a qualitative analysis of the RF performance implications. However, a *holistic* analysis of the system's power consumption would benefit from an accompanying quantitative inquiry into the RF performance of the recommended antenna architectures. Going one step further, the RF quantities could also be added to the model as input parameters or an additional set of constraints.

- Two major assumptions about the link budget were made in the modelling process: firstly, that the system is noise-limited at high bandwidths; and secondly, that all users are situated at the cell edge. These assumptions can be modified to incorporate a traffic-model-based distribution of users in the cell and account for the interference between them, which would make the model more representative of reality.

- The number of RF chains can be altered to be more than the number of users, which opens the avenue to explore the impact of multi-stream transmission and virtual grouping of transmitter RF chains.

- The modelling of the DSP power consumption in the baseband unit can be improved by accounting for advanced signal processing, such as the effect of the Inverse Fast Fourier Transform operation, Channel State Information estimation and spatial multiplexing algorithms. Similarly, the impact of digital pre-distortion on the array gain of various transmitter architectures can be incorporated. The analysis and optimisation of these mainly digital aspects are topics of active research.

- The model can be expanded to account for power-saving techniques such as sleep modes, advanced traffic models and user scheduling, which occupy the space between algorithmic optimisation and regulation/policy.

- The model assumes perfect synchronicity between the distributed LOs and Reference clocks. However, this may not always be the case at mmW frequencies, and highly accurate, cutting-edge components may have a different power consumption relationship with the antenna topology than the one employed in this model. Further exploration on this topic can be carried out and used to expand the model. On the other hand, the component-specific results of this thesis may be used a threshold against which innovative energy-efficiency technologies can be evaluated.

- Field tests can be carried out to verify the model's output, and to add relevant measurement-based features such as the power consumption of AC-DC conversion and thermal man-

agement. Testing has not been conducted during this project because system-level field tests involving 5G architectures usually require significant planning and time.

Appendix A

Additional Information

A.1 Power Amplifier Survey

Table A.1: State-of-the-art PAs at 28 GHz implemented in Bulk CMOS, CMOS SOI, SiGe, GaAs and GaN technologies.

Ref.	Year	Freq. (GHz)	Gain (dB)	Psat (dBm)	Avg. Pout (dBm)	Max. PAE (%)	Avg. PAE (%)	Process (nm)	Tech.
[91]	2021	28	14.8	20.2		30	19	28	Bulk CMOS
[92]	2021	28	20.4	17.5		27		65	Bulk CMOS
[93]	2021	28	22.2	20	10.8	30	12.4	28	Bulk CMOS
[94]	2021	28	28	20.4		35	16.5	28	Bulk CMOS
[95]	2020	28	20.4	21.5		26		28	Bulk CMOS
[96]	2020	28	18	23.2	16.1	35.5	14.9	65	Bulk CMOS
[97]	2021	28	26.1	22.5	10.9	28.5	9.2	28	CMOS SOI
[98]	2020	28	27	21.7	14.3	27.1	11.8	22	CMOS SOI
[99]	2021	28	20	19.3	14.1	47.3	25.1	45	CMOS SOI
[100]	2020	28	16.8	18.2	8	22	7	45	CMOS SOI
[101]	2020	28	20.5	20.4	11.3	45	16.6	45	CMOS SOI
[102]	2021	28	20.5	28.3	20.9	30.4	18.4	130	SiGe
[103]	2021	28	19.4	22.7	16.2	38.1	11	130	SiGe
[104]	2021	28	36	20.6	13.22	22.5	11	130	SiGe
[105]	2020	28	17.4	20.3	10.5	39.8	12.6	90	SiGe
[106]	2020	28	20.5	28	20.9	30.4	18.4	130	SiGe
[107]	2020	28	14.6					130	SiGe
[108]	2020	28	14.1	16.3		23.6		130	SiGe
[109]	2019	28	18.2	16.8	9.2	20.3	18.5	130	SiGe
[110]	2022	28	34	49.29		19		100	GaN
[111]	2021	28	20	37.78		25			GaN
[112]	2021	28	20	33		35	27	150	GaN
[113]	2020	28	22.4	33		31		150	GaN
[114]	2020	28	15.8	35.6	27.6	24	20.9		GaN
[115]	2020	28	14	36.2		29	25		GaN
[116]	2020	28	24	52.5	49	23		150	GaN
[117]	2018	28	30	46.2		25.9	23		GaN
[118]	2021	28	23	28	20.6	38	10	100	GaAs
[119]	2020	28	18.5	24		31	22.5	100	GaAs
[120]	2018	28	14.4	28.7		37	27	150	GaAs

Appendix B

Derivations

B.1 DAC minimum ENOB

The following assumptions have been made about the DAC's properties:

- We use a single-carrier signal, so that the DAC crest factor is 0.
- The DAC is operating at full-scale.
- The DAC is ideal, and therefore has no harmonic distortion ($THD = 0$), analog noise, clock jitter, or differential non-linearity ($DNL = 0$).
- The DAC has a dynamic range headroom requirement given by HR (dB) [60]. This headroom also accounts for DAC quantisation noise.
- The DAC's internal filter is assumed to operate at an attenuation, denoted as At_{filter}, from the DAC's centre frequency [60].

For a transmitter (Tx) signal in the FR2 frequency range, the SFDR requirements are as follows:

- Frequency range: 9kHz-1GHz offset from centre frequency f_c.
- Category B limit, which is more strict than Category A, due to the more stringent telecommunications laws in Europe.
- SFDR measurement bandwidth: 10MHz.

The above requirements and assumptions lead to the following choices of DAC parameters:

$$\begin{aligned} SFDR_{min} &= 36dBc \\ HR &= 10dB \\ At &= 3dB \end{aligned}$$

The Dynamic Range DR_{DAC} can be found using the three parameters above. For an ideal DAC, the dynamic range is equivalent to the SINAD, due to no harmonic distortions within SFDR frequency range. By further considering the oversampling of the DAC frequency by a factor $OS > 1$, we can use Equation 4.10 to obtain the SINAD as

$$DR_{DAC}[dB] = SFDR_{min} + HR - At \tag{B.1}$$

$$SINAD[dB] = DR_{DAC} + 10\log_{10}(OS) \tag{B.2}$$

Finally, based on the SINAD, the required minimum ENOB of the DAC can be found through the commonly used relation:

$$b[\text{bits}] = \frac{(SINAD[dB] - 1.76)}{6.02} \tag{B.3}$$

where the value of b is *rounded up* to the closest integer number of bits.

Appendix C

Additional Figures

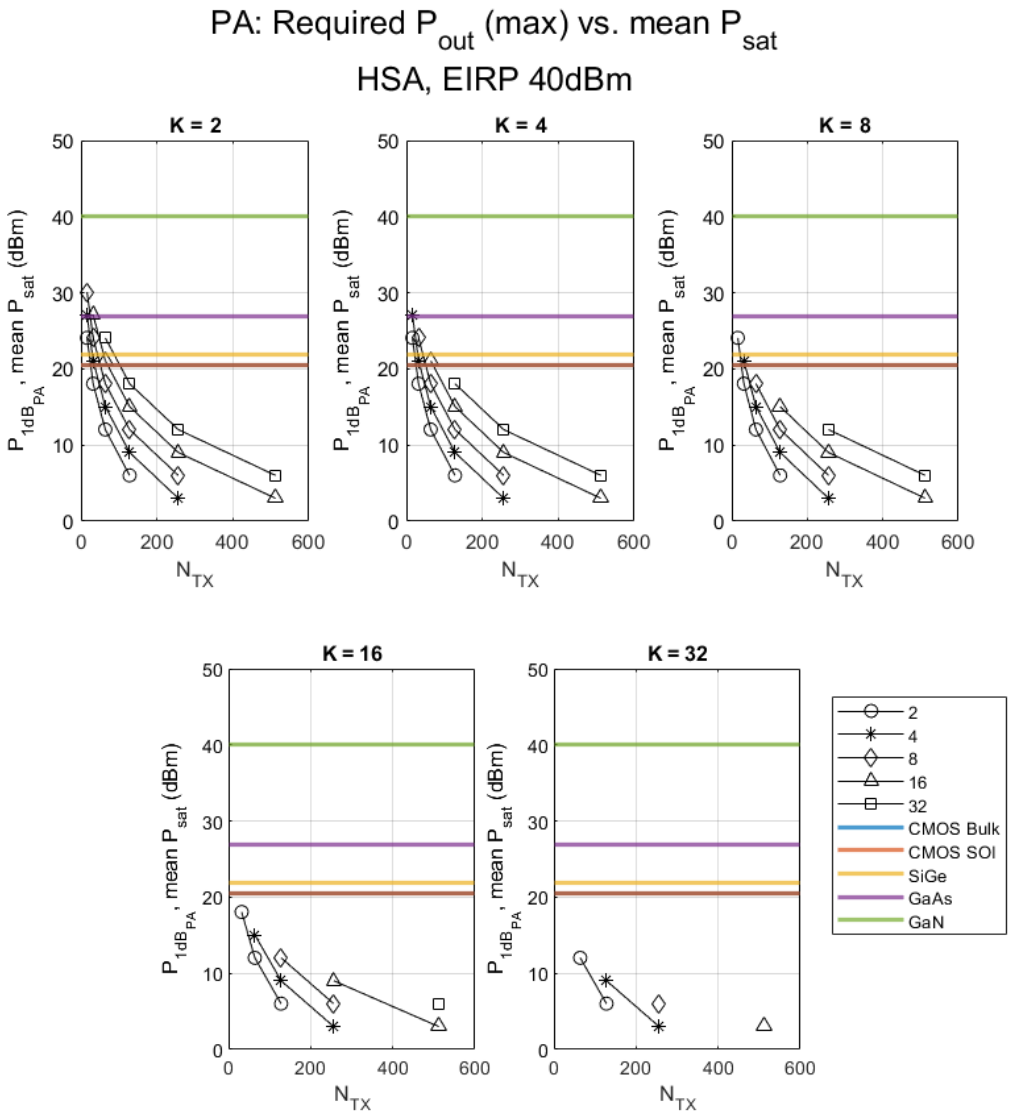


Figure C.1: HSA (full): per-PA P_{1dB} as a function of array size NTX, sub-array size K and number of users, plotted against the mean P_{sat} of various PA technologies

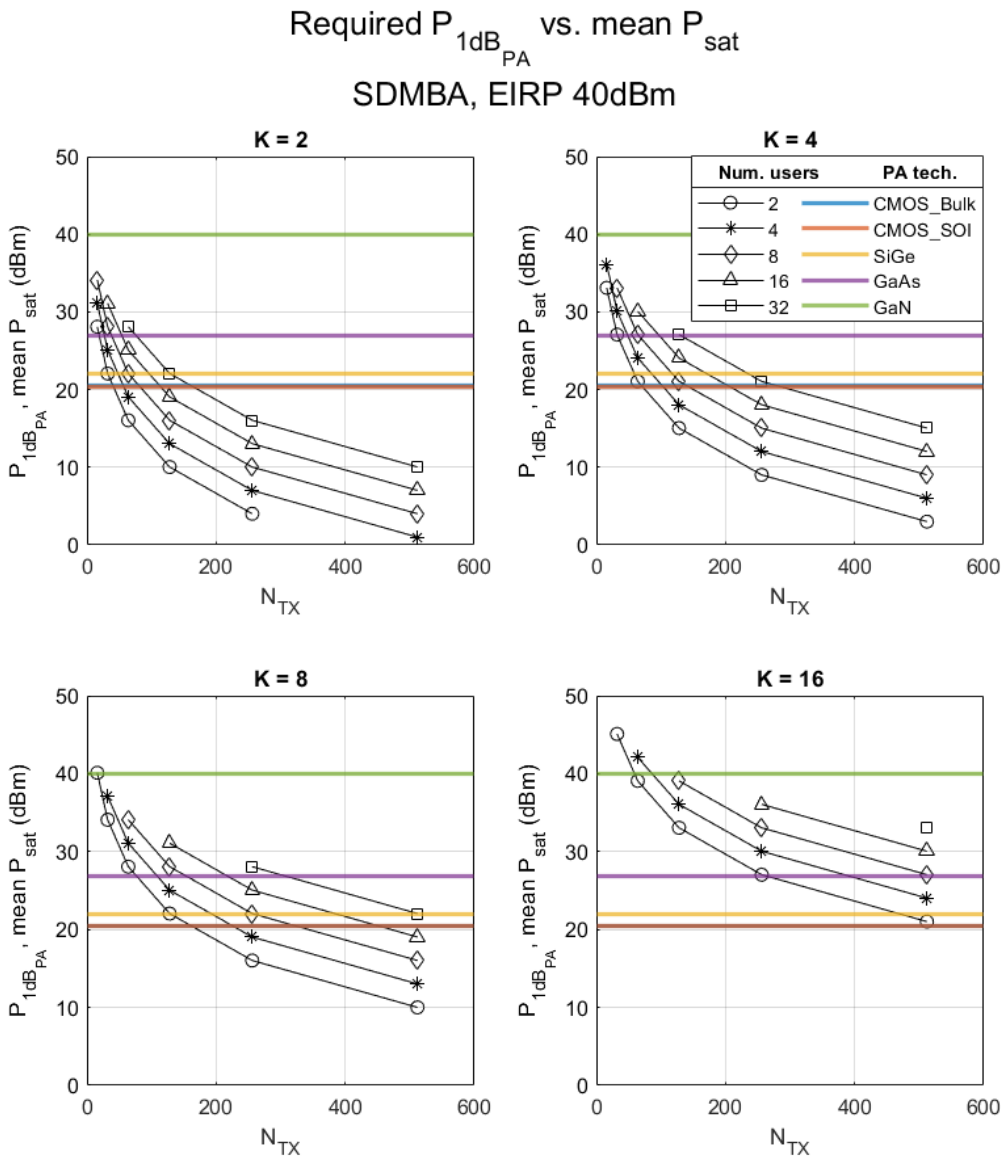
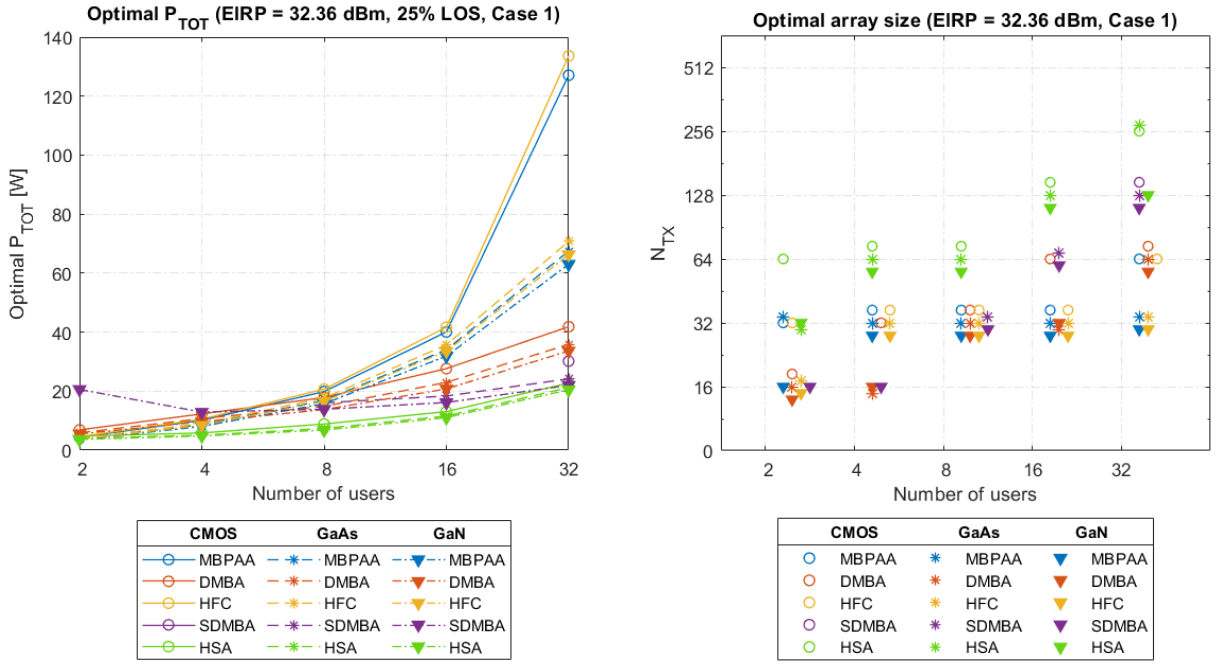
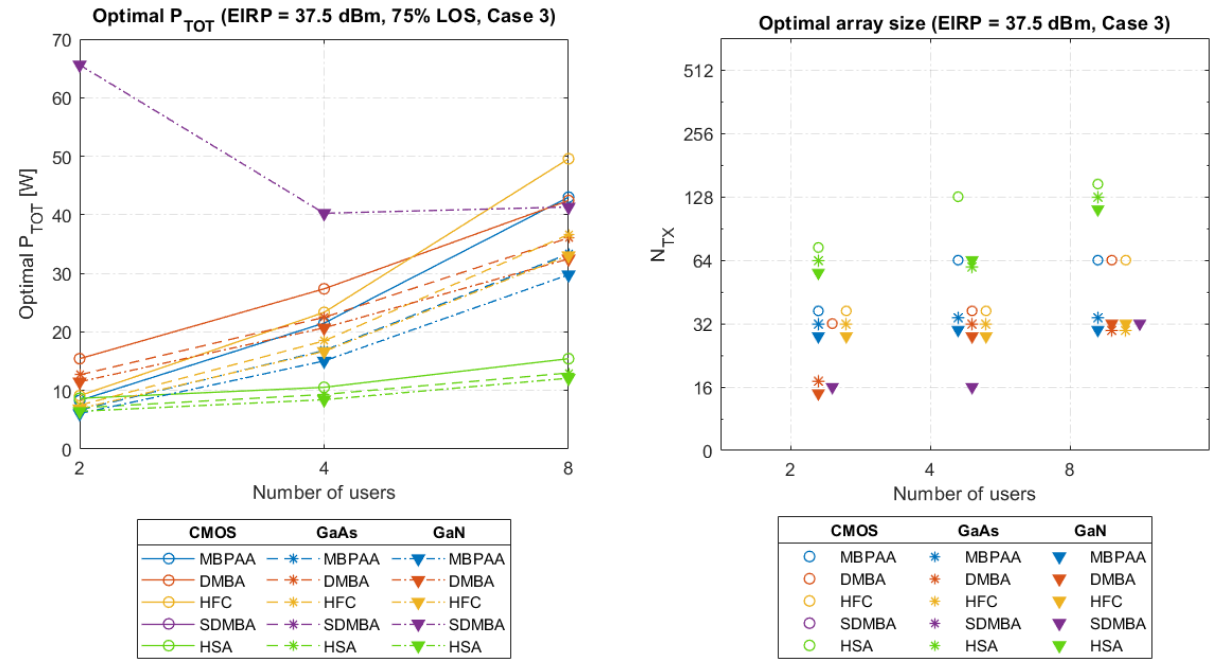


Figure C.2: SDMBA (full): per-PA P_{1dB} as a function of array size NTX, sub-array size K and number of users, plotted against the mean P_{sat} of various PA technologies



(a) (b)

Figure C.3: The optimal power consumption and array size (Case 1, $BW = 100$ MHz, $EIRP = 32.36$ dBm).



(a) (b)

Figure C.4: The optimal power consumption and array size (Case 3, $BW = 100$ MHz, $EIRP = 37.5$ dBm).

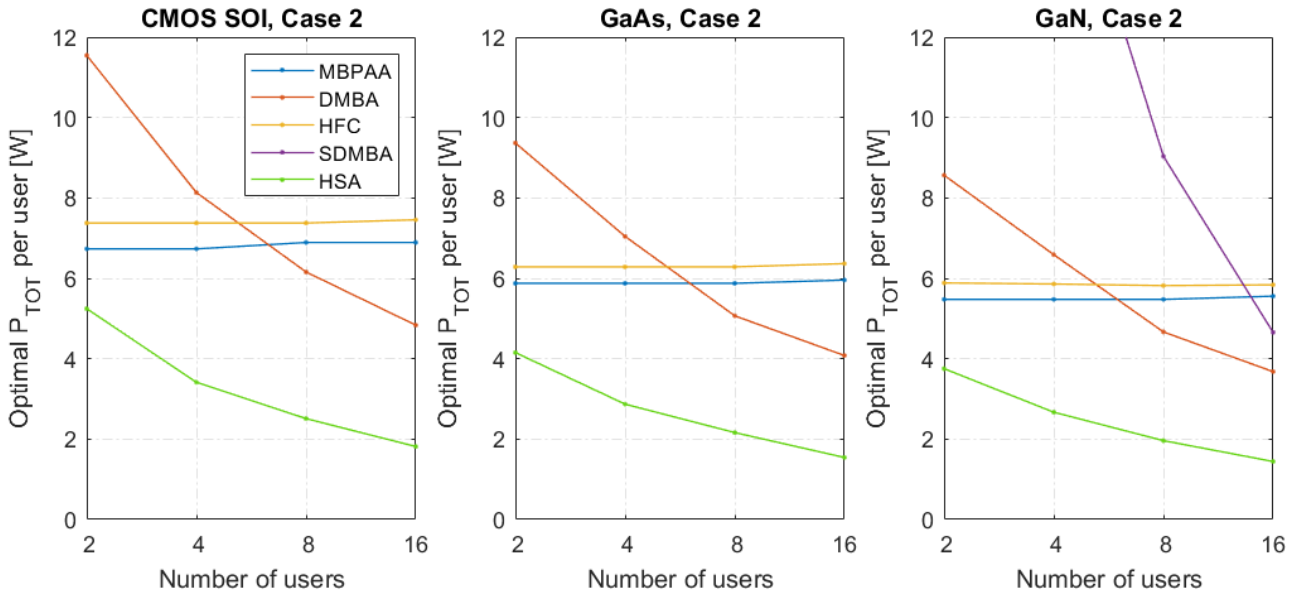


Figure C.5: Optimal power consumption per user
(Case 2, $BW = 200$ MHz, $EIRP = 40$ dBm)

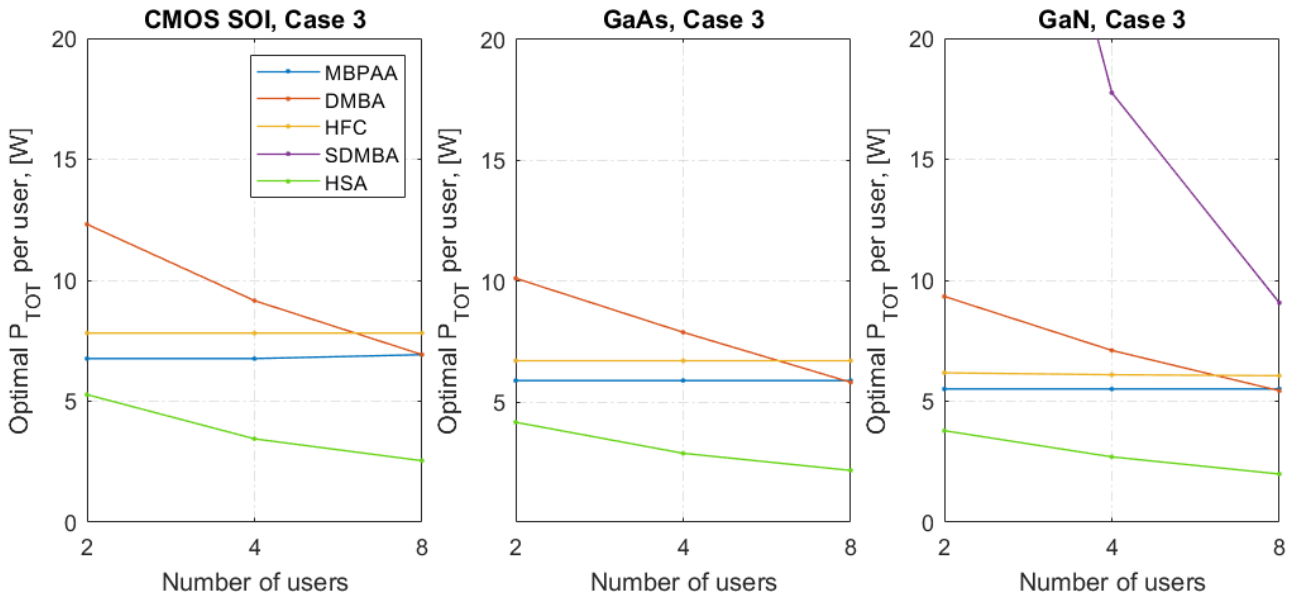


Figure C.6: Optimal power consumption per user
(Case 3, $BW = 400$ MHz, $EIRP = 40$ dBm)

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