The Design of a Global Shutter CMOS Image Sensor in 110nm Technology

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Abstract

CMOS image sensors, via their advantages, gradually become a viable alternative to CCDs. Global shutter CMOS image sensors not only can be operated at a high speed but also create images without any motion artifact.

The goal of this work described in this thesis is to design a CMOS image sensor chip, implementing pixels with a 4.8μm pitch with a peripheral readout circuitry in a 110nm CMOS process. The architecture of the CMOS image sensor is presented, with a functional illustration for every block. The 8T global shutter pixel noise, circuit and layout are described and analyzed in the thesis. The simulation results of the pixel readout speed and the output swing are presented and some other performances are shown. The Analog Front-End (AFE) circuit design of a switched capacitor amplifier and a sample and hold stage are also presented. The layout of the AFE circuit for the important blocks is done and the practical concerns of the amplifier design are discussed. The Low Voltage Differential Signaling (LVDS) driver also is implemented in this thesis, the power efficiency and common mode feedback stability issues of it are tackled as well. The simulation results of the LVDS driver with extraction of parasitics are presented and the performance summary is given.

Keywords: CMOS image sensor, global shutter pixel, AFE, LVDS

Table of Contents

List of Figures

List of Tables

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Delft University of Technology Xiaoliang Ge
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Chapter 1

Introduction

The heart of a digital camera is called an image sensor, which converts optical information into electrical signals. Nowadays, CMOS based imaging arrays have stepped into a booming stage. Beyond the low cost and low power advantages, the continued explosive growth of CMOS image sensor popularity goes to other factors such as the ability to integrate the sensors with electronics and the ability to achieve fast, customizable frame rates [1].The objective of this thesis is to design a universal image sensor test chip, implementing pixels in a 4.8μm pitch with peripheral readout circuitry in a 110nm CMOS process.

In this chapter, a brief introduction of the image sensor background about CCD and CMOS will be given in Section 1-1. Next, Section 1-2 describes the challenges in designing a large CMOS image sensor in small pitch will be discussed. Based on these discussions, the motivation and goals of this project are presented. In Section 1-3, this test chip CMOS image sensor project architecture, specification and division of work will be presented. Finally, Section 1-4 shows the structure of this thesis.

1-1 Background of the image sensor

In 1947, the first transistor was invented at AT&T's Bell Laboratories [2]. This most important electronics event of 20th century started the prosperity of semiconductor industry. Afterwards, in order to replace the film-based camera with electronic devices, which could be manufactured with semiconductor technology, two types of imaging capture devices were born, namely the Charge-coupled Device (CCD) and the Complementary Metal-Oxide-Semiconductor (CMOS) image sensor.

The milestones of image sensor history are shown in Figure 1-1. In the interval from 1964 to 1970, S. Morrison [3], IBM [4], and Westinghouse [5] developed the earliest solid-state image sensor, all these preliminary devices were implemented by bipolar and MOS processes. During this period, the focus of the image sensor research work was not only just on the conversion of photons to electrons, but also on the ability of signal readout from the pixel array. Photon

flux integration mode, which is still the predominant approach in the modern CMOS image sensor, was first proposed at that time [6].

In 1970, Bell Labs first reported a different type of solid state imaging device, the CCD [7]. This kind of device forced the detectors and imaging array based on CMOS process to lose their popularity. After 15 years solving the fabrication and reliability problems, CCDs technology realized its vast commercialization and quickly dominated almost all digital imaging applications.

However, improvements and progress in CMOS fabrication technology and ever-increasing pressure of power consumption reduction for battery operated devices began the re-emergence of CMOS image sensor as a more feasible device. Around mid 1980s, several groups led resurgence in CMOS image sensors research and development, and several kind of CMOS image sensor were reported. Among them, the most prominent one was the Passive Pixel Sensor (PPS) which was developed by VLSI Vision Ldt [8]. Finally, from 1992 to present, the Active Pixel Sensor (APS) was and still is under continuous development.

In the CCD image sensors, incident photons are converted into charge and then accumulated during an exposure time in the photodetector. During the following readout time, these accumulated charges are sequentially transferred into horizontal and vertical CCDs with phase clocks, and finally shifted to the chip level output amplifier, where charge to voltage conversion takes place. Because CCD image sensors use optimized photodetectors, they can offer low uniformity, low noise, and low dark current in combination with a high fill factor, high quantum efficiency, and high sensitivity. However, CCDs still have some technology limitations.

1. *Power consumption*: CCDs are high capacitance devices, thus, they require multiple relatively high power supplies, up to 15V. What's more, during readout, all the CCD gates are switched simultaneously with a high voltage, which lead to a large power consumption [9].

2. *Integration*: Due to the fact that a CCD image sensor uses a different technology from CMOS circuit, it is very hard to integrate all the camera function onto a single chip. Therefore, CCD image sensor based digital cameras, in general, are relatively large in size, and not well suited for portable imaging applications.

3. *Radiation*: CCD sensors are susceptible to radiation damage [10].

Like CCDs, CMOS image sensors are also made from silicon, but, unlike CCDs, which depend on specialized process, CMOS imagers can be manufactured using the relative standard CMOS processes. In contrast to CCDs, each pixel in an APS CMOS imager integrated its own individual amplifier. Via this amplifier, the CMOS pixel can drive the light induced voltages directly to the output by using row and column decoders which are very similar to those used in DRAM memories. This primary readout difference from CCDs, along with the relative standard technology process, gives CMOS imagers many advantages over CCDs.

1. *Technology*: CMOS technology is a well established technology and it will continue to become more mature. The continuous scaling down of CMOS technology provides much space for the development of CMOS image sensor.

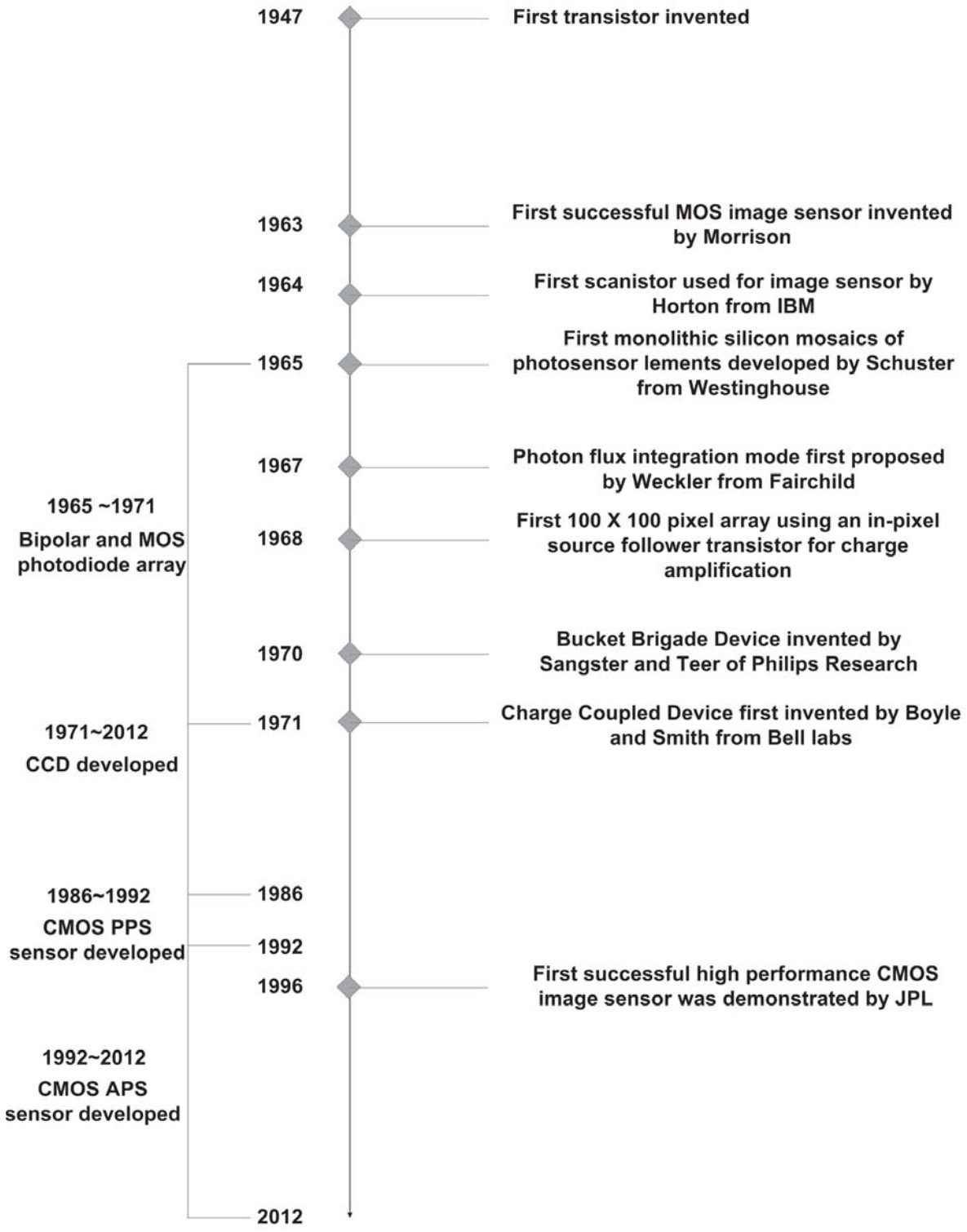

Figure 1-1: Milestone of image sensor history

2. *Integration*: CMOS technology also enables integrating the image sensors together with driver circuitry and other on- chip signal conversion and processing circuitry. This high level integration not only reduces the size of the imaging system but also simplifies the system interface.

3. *Speed*: CMOS image sensor designs are inherently fast due to parallel readout and processing; until now, frame rate up to 1Tpixel/s (10Mfps) can be achieved in burst operation [11].

Figure 1-2 shows the trends of CMOS imagers versus CCD imagers in the image sensor market. As can be seen from the figure, the sales of CMOS and CCD imagers are all increased from 2005 to 2015 by different Compound Annual Growth Rate (CAGR) thanks to the overall image sensor sales growing. Specifically, CCDs account for 40% in 2011 and predicted decreasing to 34% in 2015, while for CMOS imagers, the percentage of sales is around 60% and will increase to 66% in 2015.

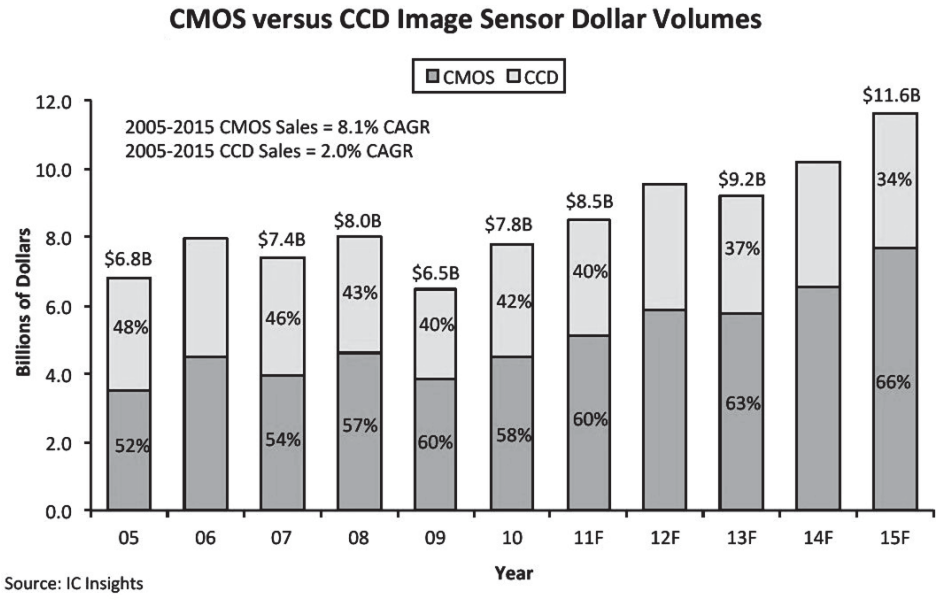

Figure 1-2: CMOS versus CCD Image Sensor Dollar Volumes, redrawn from [12]

Because of the rapidly growing demand for portable electronic device applications, the advantage of low cost and low power consumption have helped CMOS imagers gradually overtaking CCDs in the image sensor market. Moreover, in some particular and novel applications which require complex functionalities, for example:

- applications that need random accessibility, such as image compression or target tracking;
- applications which need high speed readout, such as machine vision or motion analysis;

- applications where higher radiation hardness is required, such as nuclear and space applications.

CMOS image sensor has its own superior performance to continue enhancing its share on the image sensor market.

1-2 Motivation and challenges

A continuous market demand in higher resolution image sensor has let mega-pixel sensors design become an interesting trend, in particular for low cost sensors of mobile application. For example, Nokia announced a 42-mega pixel array camera mobile phone in 2012 [13]. In order to increase the number of pixels, people can increase the chip size or shrink the pixel pitch. However, a larger die size means a higher cost, implying that the only way to produce an image with higher resolution and lower cost is to shrink the pixel pitch. Thus, there is a huge interest in the design of CMOS image sensor with smaller pixel pitch by using a smaller feature size technology. However, nothing comes for free. Accompany with the benefit from pixel size shrinking and advanced technology, it is indispensable to take some challenges, which will have an influence on the image performance, into serious consideration.

In most cases, pixel size shrinking leads to a reduced photo-sensing area. Accordingly, the maximum amount of collected electrons, named as Full Well Capacity (FWC), reduced as well. Thus, both Dynamic Range (DR) and Signal to Noise Ratio (SNR) are compromised by the decreasing full well capacity, the reason of which will be explained in Section 2-2. However, in some pixel architectures, the floating diffusion capacitor determines the charge conversion gain. A high charge to voltage conversion gain can be obtained as the pixel shrinks, which helps to suppress the input referred noise [14]. In addition to the influence on the performance of the pixel, the column parallel analog and mixed signal processing circuit pitch also decrease as a result of the pixel size shrinking. As a consequence, both circuit design and layout for the readout chain need to be carefully done for the purpose of reducing the influence of mismatch and signal coupling between adjacent columns.

The advanced manufacturing process with on-going down scaling design rules, has proved itself as a highly potential candidate for the implementation of size-reduced pixel while maintaining a reasonable pixel performance. In order to investigate a new kind of technology, this project is migrated from 180nm to 110nm technology node. In the latter technology, the minimum size for almost every layer is smaller due to a greater resolution lithographic processing. For example, the minimum parameters such as width, space, area, distance of metal, poly, and diffusion layer are all decreased compared with 180nm technology. Hence, the surrounding circuit area required in a pixel shrinks with the smaller feature size technology usage. As a consequence, in the case of the same pitch, the fill factor, which is the ratio of light sensitive area (metal and diffusion layer uncovered) to the total area of pixel, can become larger. A larger fill factor contributes to a higher Quantum efficiency (QE) and spectral responsivity, which is what we desire in an imaging system. Moreover, as mentioned above, in some pixel architectures, with the help of a larger conversion gain, the input referred noise can be compressed down. Due to the reduction of metal and transistor dimensions in smaller feature size technology, the floating diffusion capacitor becomes smaller, which leads a higher conversion gain, thus, we can get a lower noise in the same pitch size.

This project is dedicated to validate a smaller pixel operation and performance. For evaluation purposes, the image sensor should, at least, contain two different types of pixel. In this project, they are 8T global shutter pixel and 6T high dynamic range pixel with 4.8um pitch. To be able to draw conclusion from the evaluation, the pixel array needs to be fairly large to provide reliable statistical data, such as Photo Response Non-Uniformity (PRNU) and Dark Signal Non-Uniformity (DSNU). In addition to that, the readout circuit is also another important part in CMOS image sensors. The analog front-end circuit, analog-to-digital converter, and LVDS driver are all included in this project. All of them enable a high resolution, low noise and high speed data transfer readout function, and all are compatible with a wide range usage.

In order to implement a CMOS image sensor which fits into the tight specifications, a comprehensive effort on various aspects, like pixel design, analog, mixed-signal, and digital circuitry design, has to be made. To verify the pixel and peripheral circuit, some models need to be designed and simulations need to be carried out. This test chip will make the future design project become much easier if they use the same technology. It also greatly shortens the design cycle of a whole standard image sensor chip.

1-3 CMOS image sensor for this test chip project

As mentioned in the previous section, this project includes two different types of pixels: 8T global shutter pixels and 6T high dynamic range pixels, which are implemented in each chip respectively. Although the periphery circuit block can be shared with each other, the whole architecture of two test chip are not the same, which is due to the fact that the working principle of two kinds of pixels are different. This section mainly introduce the global shutter pixels test chip.

1-3-1 Introduction of CMOS image sensor architecture

CMOS image sensors routinely consist of several million transistors as well as a large quantity of both analog and digital circuitry. It can be seen as one of the most complex mixed signal integrated circuits on the market today [15].

Figure 1-3 depicts the simplified block diagram of an image sensor architecture which is used in this project. Each block functions are described below.

Pixel array: the light sensitive part of the whole image sensor. In this chip, it is implemented by 8T global shutter pixels and built up from an array of 1280 pixel columns by 1024 pixel rows. Besides the active pixel array, an additional line of dummy pixels need to be added at all sides of the array, serving as the optical dummy in order to ensure that boundary line and boundary column have the same performance as the rest of the pixels.

Y address decoder and Row Logic: the row logic blocks are used for driving the controlling lines of the pixel array; they will be foreseen on one side of the array. For 8T global shutter pixel, in this design, the global shutter row logic circuit should be used.

Analog Front-End (AFE) Readout Structure: it is a switched-capacitor circuit that can perform Correlated Double Sampling (CDS) on the pixel output signals: the light-induced signal

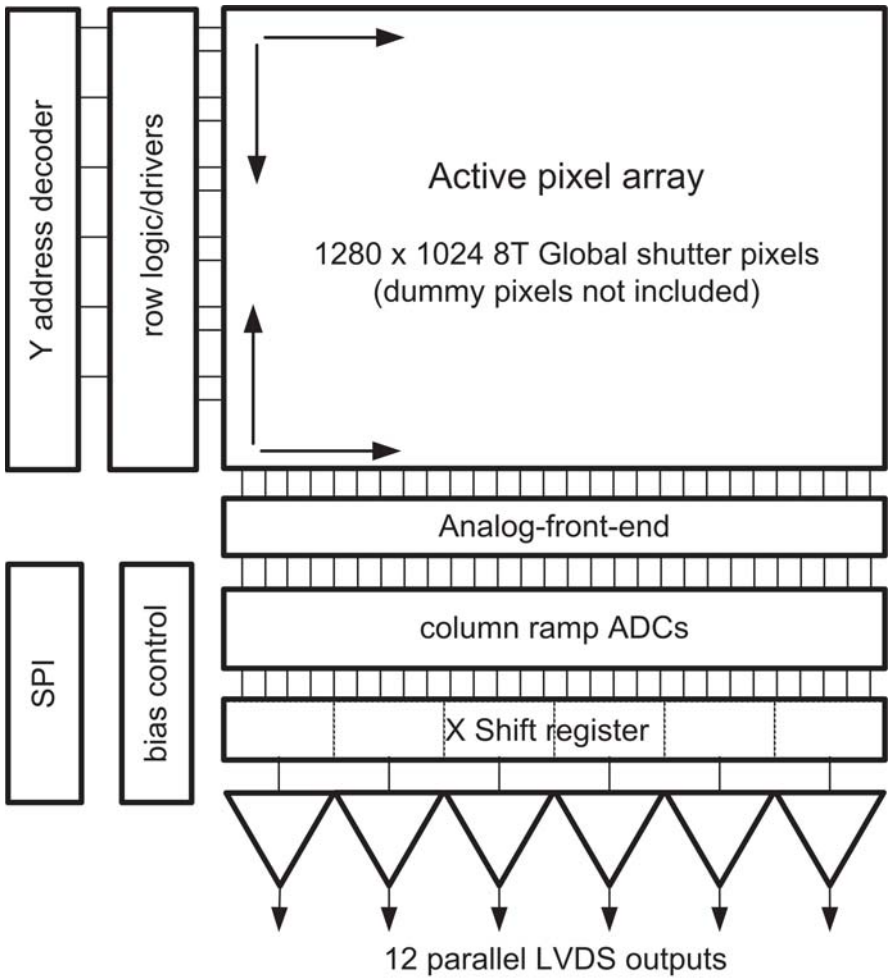

Figure 1-3: CMOS image sensor test chip architecture

and reference level of each pixel are sampled via the column amplifier into a Sample and Hold (S/H) stage. What's more, it also includes a programmable gain stage to fit the pixel output range into the readout chain swing.

Column ramp Analog-to-Digital Conversion (ADC) and registers: double sampling the signal again and digitize the sample values of the complete row to a 12bit digital value. This double sampling operation cancels any fixed pattern noise of the pixels and column cells, and the results of the doubling sampling are latched into the column registers.

X shift register: selecting the column bus to feed into the LVDS drivers, it also can be flipped for mirroring the image in horizontal direction.

LVDS driver: Low Voltage Differential Signaling (LVDS) I/O interfaces contains drivers and receivers. The driver is implemented on this chip, used for data transmission. It can achieve higher speed and lower power consumption in conjunction with low voltage swing by means of a differential scheme for transmission and termination. In this design, corresponding to 12bit ADC, a 12 channel LVDS driver should be used. The receiver, which is used for receiving the data, is built on the PCB.

Biasing and power supply: this block consists of a band-gap reference circuit which can provide a temperature independent reference voltage, and several DAC blocks each of which can be used for current and voltage biasing control and adjustment when testing and debugging the sensor.

SPI interface: the Serial Peripheral Interface (SPI) interface circuit is used to load the on-chip registers. The data stored in these registers is used to define the settings which are used for driving and readout the sensor. Features such as gain settings for the amplifier and exposure time can be programmable by using this interface. What's more, the data in these on-chip registers can also be read back for testing and debugging of the surrounding system.

1-3-2 Readout operation for whole sensor

Although a CMOS image sensor is able to be readout in a random access manner, in column parallel readout cases, a full image or frame needs to be read serially, as illustrated in Figure 1-4.

In this project, for every frame time, the imager is readout on a row-by-row basis. Each frame time can be defined by the equation presented below.

$$T_{FRAME\_TIME} = T_{FOT} + T_{ROW\_TIME} \times Nr.Row \tag{1-1}$$

where T_{FOT} is the frame overhead time, T_{ROW_TIME} is the row readout time, and $Nr.Row$ is the number of rows of the pixel array.

The sensor readout is performed in a pipelined manner, in which three processes take place at the same time: AFE readout, ADC and LVDS data readout. Figure 1-5 illustrates the working principle of pipelined readout. When one pixel row is performing the analog front-end readout, the previous rows are converted and readout by LVDS in parallel within one row readout time. Among these three processes, the AFE readout as well as the ADC process operate in a column parallel processing, the LVDS data readout operates in a serial process,

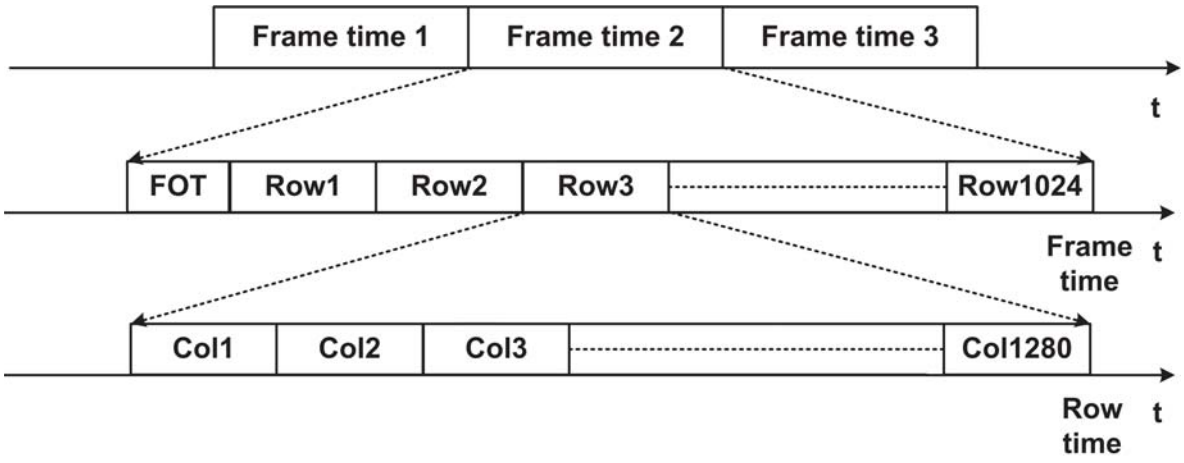

Figure 1-4: Timing diagram of CMOS image sensor column parallel signal processing readout

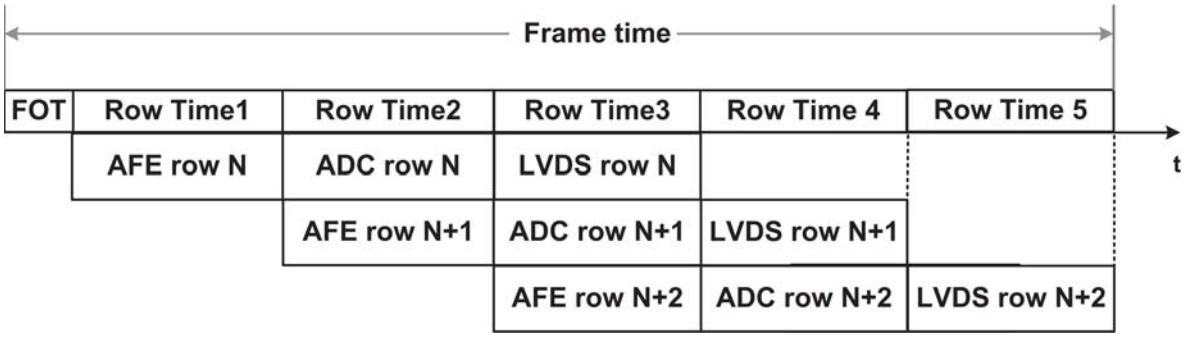

Figure 1-5: Working principle of pipeline readout

the slowest process limits the line frequency and frame rate. This relationship can be expressed as:

$$T_{ROW\_TIME} = max(T_{AFE}, T_{ADC}, T_{LVDS}) \tag{1-2}$$

where T_{AFE} is the row sampling time, T_{ADC} is the ADC conversion time and T_{LVDS} is the LVDS output time.

1-3-3 Test chip design specification

The specifications of the 8T global shutter pixel test chip from the company are shown in Table 1-1 and Table 1-2.

In Table 1-2 the speed calculation is based upon the image sensor architecture using a one-side row logic control.

Row sampling time: Assume that the Row Blanking Time (RBT) which is used for readout of one pixel from the column bus is equal to 1μs, and make the target for sampling time is as 5μs. Thus,

$$T_{AFE} = T_{RBT} + T_{SAMPLE} = 6\mu\text{s} \tag{1-3}$$

Table 1-1: Test chip design specification

Specification	Target	Unit	Comment
	Technology		
Process technology	0.11 μm CIS		Multi-layer Mask (MLM) will be used in this project. Assuming maximum reticle size of $24 \times 32\text{mm}^2$, the total available MLM area will be $12 \times 16\text{mm}^2$.
Pixel pitch	4.8×4.8	μm^2	
Pixel type	8T Global shutter		
Effective number of pixels	1280 columns×1028 rows		1.3M pixel array — SXGA. With 4.8μm results in half inch optical format.
Pixel array in Y	4915.2	μm	
Periphery core Y	3084.8	μm	
Digital output Y	400	μm	
I/O pads Y	600	μm	
Total size in Y	9000	μm	
Pixel array in X	6144	μm	
Periphery core in X	1306	μm	
I/O pads in X	500	μm	
Total size in X	7950	μm	
Die size	7.95×9	mm^2	
	Function		
Column PGA			Variable gain settings
ADC	12bits, on chip		Column ramp ADC architecture will be implemented, 12 bits is foreseen for both global and rolling shutter pixel
Digital interface	LVDS		12 channel LVDS interface will be implemented in this project
Ramp generator			Automatic scaling according to ADC clock input
SPI			Addressable SPI

Table 1-2: Test chip design specification(cont'd)

Specification	Target	Unit	Comment
	Speed		
Frame rate	>75	fps	
Frame over head time	10	μs	
Pixel access (RBT)	1	μs	
Row sampling time	6	μs	
ADC clock rate	400	MHz	The ADC clock will be applied externally for simplicity.
ADC conversion time	12.8	μs	
LVDS clock rate	400	MHz	The LVDS clock will be applied externally for simplicity.
LVDS output time	3.2	μs	
Maximum line rate	62.5	kHz	
	Power		
Power supply voltage	3.3 & 1.5	V	Ideally multiple 3.3V supplies for pixel and analog circuitry; 1.5V for digital circuitry.
Power consumption of ADC and AFE	121	mW	
Power consumption of output	168	mW	
Total power consumption	289	mW	

ADC conversion time: Since the resolution for ADC is 12bit, that means the counter needs $2^{12} = 4096$ clock cycles to accomplish the analog-to-digital conversion. Concerning a 25% design margin for the conversion of the reset value during the first ramp, the whole conversion time is equal to:

$$T_{ADC} = \frac{1}{400\text{MHz}} \times 4096 \times (1 + 25\%) = 12.8\mu\text{s} \tag{1-4}$$

LVDS output time: The clock of the LVDS readout part is 400MHz, and the number of column is 1280. In this project, 12 channel LVDS output is expected to be used. One channel corresponding to one bit ADC output, which means the LVDS needs:

$$T_{LVDS} = \frac{1}{400\text{MHz}} \times 1280 = 3.2\mu\text{s} \tag{1-5}$$

In this project, the ADC conversion time is longer than the other two terms, which determines the ultimate frame rate of the whole sensor. Thus, the expected T_{ROW_TIME} is 12.8μs, and the expected frame rate which calculated from Eq. (1-1) is 76fps. In the design specification, we assumed the target frame rate should be larger than 75fps.

Power consumption is also another important issue to be considered. In this project, the largest part of the power consumption will be burnt in the ADCs and the LVDS driver. The power estimation in Table 1-1 is made based on 1.5V digital operation and 3.3V analog operation, with the reference of previous design specifications.

The size of the sensor will be close to $72\mu\text{m}^2$.

A standard JLCC 84 pins package will be used. About 50-70 pins are required for operation control, biasing and power supplies in this test chip, so there will be a maximum of about 14-34 pins left for readout [16].

1-3-4 Project sketch

This Test Chip CMOS Image Sensor, which will be fabricated in 110nm CIS technology project, is a cooperative project in which two MSc students and one member from the company design team are involved. There are two chips in this project. My part lies in the global shutter pixel and row logic design, analog front-end readout circuit design as well as the LVDS driver design, as shown above. My colleague Yang Liu is mainly responsible for the design of high dynamic range pixel, band-gap reference circuit and biasing circuits, and the design of the ramp generator. Xu Wu is responsible for the implementation of the column ramp ADC and other circuitry which are required and listed above. Each test chip has its own pixel type while the other peripheral circuits are shared with each other. The objective with this implementation is that it should lead to a manufactured chip which can be used for the evaluation of the new pixel technology.

1-4 Thesis organization

This thesis focuses on the global shutter pixel design in 4.8um pitch, as well as analog front-end readout circuit and LVDS driver. Chapter 2 provides an overview of the architecture

and performance of CMOS image sensor pixels, especially the analysis of several kinds of global shutter pixels, and briefly introduces the pixel which will be used in this project. Chapter 3 presents the operation principle and design of an 8T pixel; also the performance analysis and layout consideration is given. In Chapter 4, the peripheral circuit design of the analog front-end readout circuit and LVDS driver are described, as well as the operation mode and simulation results. In the last chapter, some conclusions are drawn to summarize the contribution of this thesis and present the some suggestions for the future work.

Chapter 2

Overview of CMOS image sensor pixels

This chapter gives an overview of CMOS image sensor pixels performance and architectures. The purpose is to give a concise introduction of pros and cons of CMOS image sensors with different shutter modes as well as various pixel structures. In Section 2-1, the optical absorption and photodiode operation theory will be present. Section 2-2 gives some significant parameters which are used to evaluate the performance of a CMOS image sensor. Next, Section 2-3 analyze two main kinds of electronic shutter mode, rolling shutter and global shutter, using 4T pixel architecture as an example to explain some advantages and disadvantages under different operation modes. Then, a brief overview of improvement and alternative global shutter pixels that have been proposed in recent years will be provided in Section 2-4. Finally, Section 2-5 presents the basic 8T pixel structure and previous design characterization.

2-1 Optical absorption and photodiode operation

When photons with an energy $E = hv$, where h is the Plank's constant and v is the frequency, incident on a photodiode, some photons may be absorbed or they may propagate through the silicon, depending on the band-gap energy E_g and photon energy. If $E = hv > E_g$, the photon can be absorbed and interacted with a valence electron. This interaction elevates this electron into the conduction band and creates an electron-hole pair [17]. For an indirect band-gap, such as silicon, the excited electrons must change their momentum. However, incident photons cannot provide this momentum, so the probability of such an interaction taking place depends on the vibrational wave-particle, phonon. Therefore, with different semiconductor materials and incident light wavelength, the absorption coefficient α varies [18].

For a CMOS image sensor, a commonly used photodetector is the photodiode, which converts the incident light generated e-h pair into photocurrent. Figure 2-1 shows a typical p-n diode band diagram and the movement of generated e-h pairs under reverse bias. In the photodiode, the total photo generated current comes from two regions: the depletion region with an electric

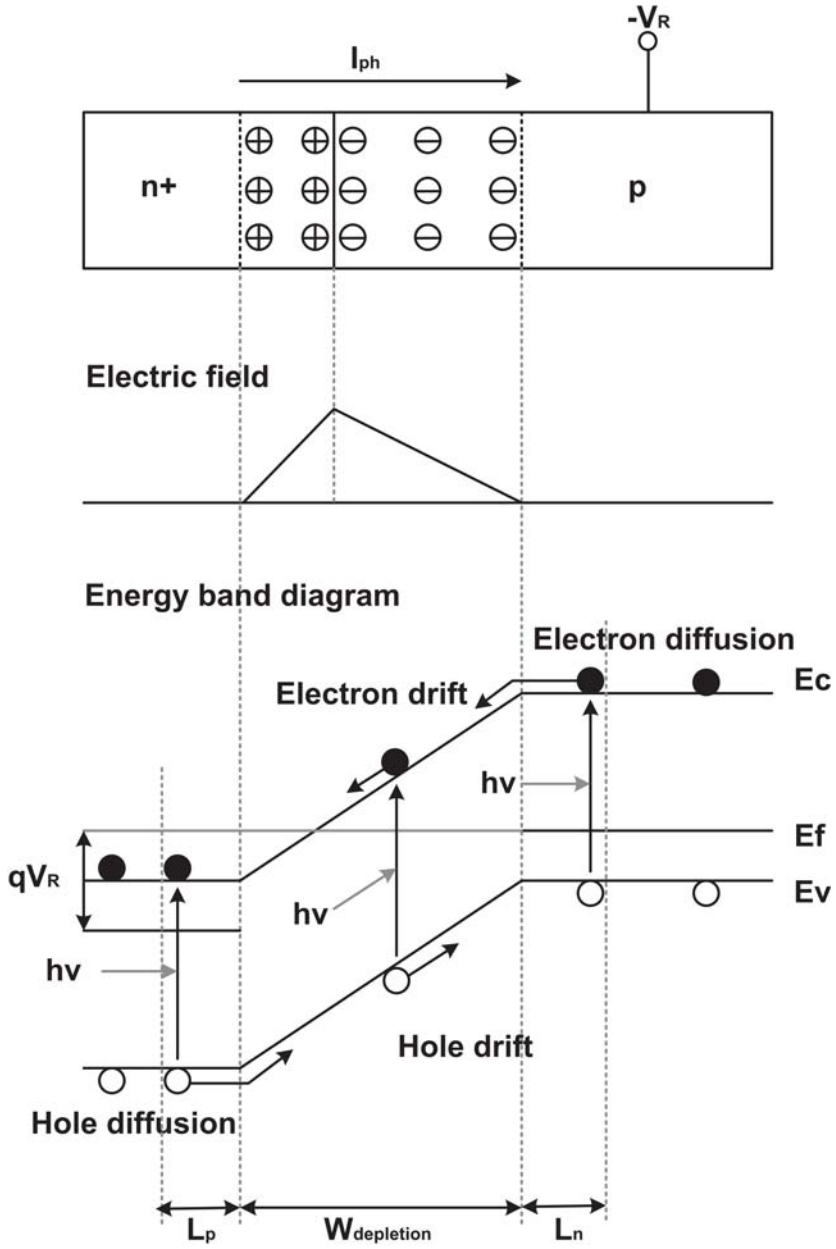

Figure 2-1: Charge movement in a photodiode, after [19]

field and quasi-neutral region where no electric field is present. Carriers that are generated in the depletion region are effectively separated because of the existence of the built-in electrical potential V_{bi} or external applied voltage. Since the carrier drift velocity is fast, recombination can be negligible for electron-hole pairs generated in the depletion region. Thus, all photo-generated carriers in the depletion region contribute to the photocurrent. On the other hand, the carriers that are generated in the quasi-neutral region cannot be collected effectively due to the absence of the electric field. Nevertheless, a quantity of minority carriers here can diffuse to the depletion region, where they can be collected. In the heavily doped n+ region, the minority carrier lifetime and diffusion length is significantly reduced, resulting in a high recombination rate [19].

In practice, the range of the typical photocurrent is so small that it is hard to detect it[6], thus, a charge integration based operation is widely used in active pixel sensors. The basic model of this operation is illustrated in Figure 2-2. Here is a description of an operation cycle:

1. First, the reset switch is closed, reset the photodiode to a reverse bias voltage of $V_M = V_{pix}$, where V_{pix} is the supply voltage for the pixel.

2. Then, the reset switch opens, and V_M begins to drop.

3. After a period of time t_{int} , read switch closes and $V_{out} = V_M$.

4. Finally, read switch opens, and then reset switch closes, the circuit is repeated for the next frame.

It is found that the voltage at node V_M is linear to the light intensity for a short period of time. Thus, light intensity to voltage conversion is obtained [20].

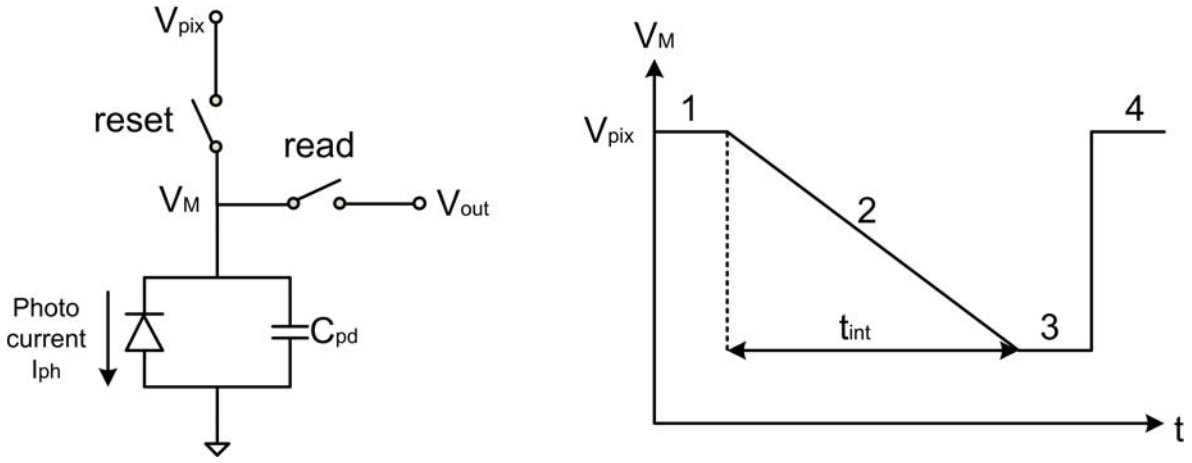

Figure 2-2: Integration operation in a photodiode, after [1]

2-2 Performance evaluation of CMOS image sensor pixels

For CMOS image sensor pixels, there are quite a number of parameters used to evaluate the performance. Some of them are mainly limited by the readout circuitries and others are determined by the pixel design. This section explains of these significant figures of merit in detail.

Fill factor: Fill factor is defined as the ratio of the photo sensitive area to the total pixel area, which can be expressed as [23]:

$$Fill\ Factor = \frac{A_{light}}{A_{total}} \tag{2-1}$$

where A_{light} is the light sensitive area of a pixel, A_{total} is the total area of a pixel. When more transistors or more routing is put into the pixel, the fill factor drops, because of the limited sensitive area.

Full Well Capacity (FWC): Photodiodes often have a maximum capacity to store carriers. This maximum capacity is called as full well capacity. For the photodiode shown in Figure 2-2, the full well capacity is given as [25]:

$$N_{sat} = \frac{1}{q}\int_{V_{pix}}^{V_{PD(min)}} C_{PD}(V_{PD})dV \tag{2-2}$$

where q is electron charge, V_{pix} is the reset voltage of the photodiode, I_{ph} is the photocurrent, C_{PD} the photodiode capacitance, and V_{PD} is the photodiode voltage. For a pinned photodiode, the reset voltage V_{pix} is normally set by the junction itself rather than the external applied voltage. Furthermore, a pixel FWC is not just limited by the photodiode FWC but also confined by FD node capacity or an other memory node which store charges.

Quantum efficiency (QE) and spectral responsitivity: quantum efficiency is defined as the ratio of the photocurrent collected by the photodiode to the photon flux incident on the device [21], it can be given by:

$$QE(\lambda) = \frac{N_{sig}(\lambda)}{N_{ph}(\lambda)} \tag{2-3}$$

where N_{sig} is the collected video signal charge, N_{ph} is the number of incident photons, λ is wavelength. Besides, spectral responsitivity is also used to reflect the photon responsitivity of an image sensor as a function of wavelength. It is defined as the ratio of the photocurrent to the optical input power [21], expressed in:

$$R(\lambda) = \frac{I_{ph}}{P} = \frac{qN_{sig}(\lambda)}{E_{ph}N_{ph}(\lambda)} = QE(\lambda)\frac{q\lambda}{hc} \tag{2-4}$$

where I_{ph} is the photocurrent, P is the optical input power, E_{ph} is the photon energy, h is the Plank's constant, c is the speed of light.

Dynamic Range (DR): a dynamic range is expressed as the ratio of the pixel saturation level to its noise floor, which is given by:

$$DR = 20\log(\frac{N_{sat}}{n_{dark}})[\text{dB}] \tag{2-5}$$

where N_{sat} is the full well capacity, and n_{dark} is the pixel noise level without illumination.As can be seen from Eq. (2-5), we can find that there are two ways to increase DR: improving the full well capacity and decrease the dark noise level. However, for a given pixel with fixed fill factor, it is difficult to increase its full well charge. Thus, High Dynamic Range (HDR) CMOS image sensors are usually adopt some special pixel structure and operation principle, such as: logarithm pixel response [22], multi-exposure [23].

*Signal to Noise Ratio (SNR):*Signal-to-Noise Ratio is defined as the ratio between the signal and the noise at a given input level, which is given by:

$$SNR = 20\log(\frac{N_{sig}}{n_{sig}})[\text{dB}] \tag{2-6}$$

where N_{sig} is the signal charges, and n_{sig} is the noise at the given signal level, both of them are measured in electrons. Under very low light conditions, the readout noise limits the SNR, and the SNR increases 20dB per decade with N_{sig} (photocurrent and integration time). While at higher illumination levels, the SNR is limited by the photon shot noise which is the square root of the input photons, and SNR increase 10dB per decade also with N_{sig}.

Conversion gain CG: conversion gain defines how much voltage change is produced by one electron. Depending on the pixel structure, it can be used for both photo-sensing node and charge storage node. It is expressed as:

$$CG = \frac{q}{C_{CG}}[\mu\text{V/e}^-] \tag{2-7}$$

where C_{CG} is the capacitance of the sensing node or the charge storage node and q is the elementary charge (1.602×10^{-19}C).

2-3 Introduction of electronic shutter mode

In digital cameras, an image is acquired by converting light into an electronic signal at the photosensitive region. Both of the light intensity and exposure time or integration time has great influence on the amount of signals generated by the CMOS imagers. Thus, like traditional film cameras, digital cameras also need some form of shutter to control the exposure time. To achieve this, an external mechanical shutter in front of the image sensor or an on-chip electronic shutter should be used. For some kinds of digital cameras, a combination of mechanical and electronic shutter are worked together, and for some other types of cameras, the control of exposure time only depends on the electronic shutter, therefore, the camera can be designed more compact by eliminating of the external mechanical shutter.

In CMOS image sensors, there are two kinds of electronic shutter modes, i.e. rolling shutter and global shutter. Two simplified timing diagrams in Figure 2-3 and Figure 2-4 illustrate how these two kinds of electronic shutter work, and show the main difference between them.

For the rolling shutter mode, pixels of rows begins to exposure sequencially controlled by a reset signal, starting, for example, at the top row and proceeding to the bottom row by row. After a short period time delay, when the reset pointer moves down, the readout process begins to work, following by the same speed and same fashion as the reset process does. This delay time between rows being reset and read is defined as integration time. By varying

the interval time of reset and read signal, the integration time can be controlled. Due to the sequential readout mode, each individual row of the whole sensor array is exposed and integrated at a different time, resulting in the geometric distortion to the image if the object or the camera moves during image capture. As a consequence, the image may manifest the phenomenon of wobble, skew, smear, partial exposure [24], slant, elongation, or even arbitrary deformed [25]. Suffered from the above intolerable motion artifacts, the visual quality of the image gravely degrades.

The global shutter mode helps to dispose of the rolling shutter undesired artifacts through a synchronous capture of all pixels in the entire frame. More specifically, after the whole array is being reset, photodiodes begin to integrate and accumulate the charges. At the end of the integration time, charges of every row are transferred to the additional memory element where the light is shielded. Finally, they will be sequentially readout row by row, which is similar to rolling shutter mode.

Furthermore, there are two sub-type of global shutter mode: triggered global shutter and pipelined global shutter. As can be seen from Figure 2-5 and Figure 2-6, in triggered global shutter mode, the image must be completely readout before the next image captured, while for pipelined global shutter mode, a new image can be captured during the data readout from the previous image. From application aspects, triggered global shutters are typically used in machine vision where an object needs to be inspected. Pipelined global shutters are popularly used in motion analysis and high frame rate cameras. In a continuous recording mode, a pixel with a pipelined shutter is sensitive at all time [36].

In order to describe and analyze rolling shutter and global shutter mode in detail, we set the typical Pinned Photodiode (PPD) 4T pixel as an example. Figure 2-7 shows the pixel structure with a cross-section of the photodiode. Timing diagrams in Figure 2-8 and Figure 2-9 presents the sequence for three control signals: RST, TG and SEL. They illustrate the working principle of 4T pinned photodiode pixel under rolling shutter mode and global shutter mode respectively.

Rolling shutter mode

1. During the pixel to column readout period, the selected row is addressed by applying a signal pulse SEL to the corresponding row, such that the voltage across the floating diffusion node becomes available to readout.

2. Within the line time, the RST signal first resets the Floating Diffusion (FD) node to the pixel supply voltage VDD, removing any redundant charges left in the sensing node. After the reset pulse, the reset level of FD V_{RESET} is sampled by switch S2 and capacitor C2, which contains the kTC noise generated within the FD node, offset as well as the flicker noise produced by source follower transistor.

3. After the first sampling, the transfer gate TG turns on, the signal charges, which generated by the incident light during the period of integration time, transferred from the pinned-photodiode to the floating diffusion node.

4. When the transfer process is finished, TG turns off, the light-induced video signal V_{SIGNAL} is sampled by switch S1 and capacitor C1. The same as reset voltage sampling, it also carries the kTC noise from floating diffusion node, offset and the flicker noise from source follower.

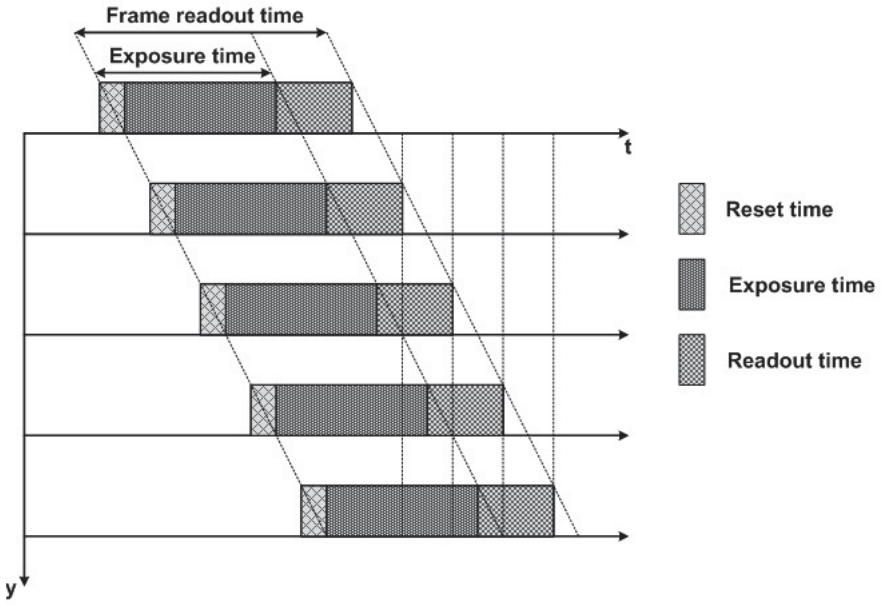

Figure 2-3: Working principle of rolling shutter mode

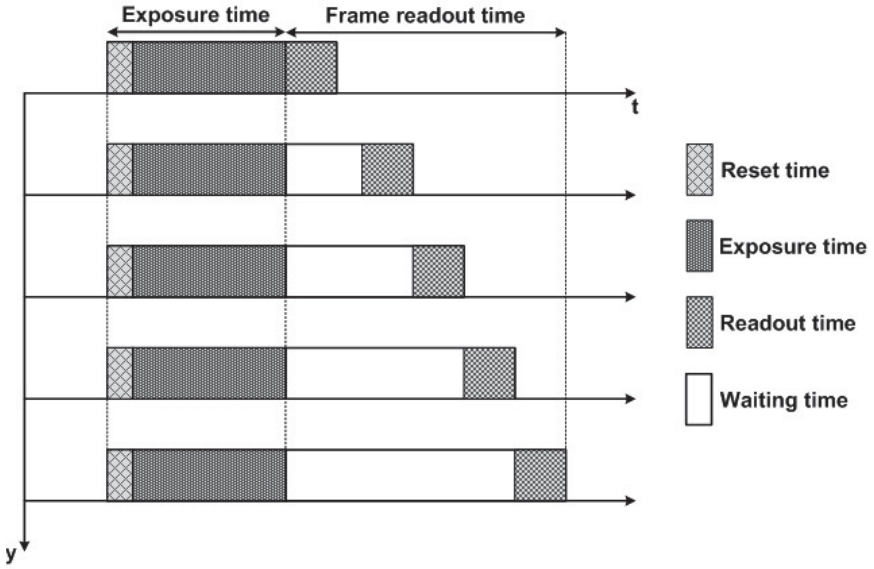

Figure 2-4: Working principle of global shutter mode

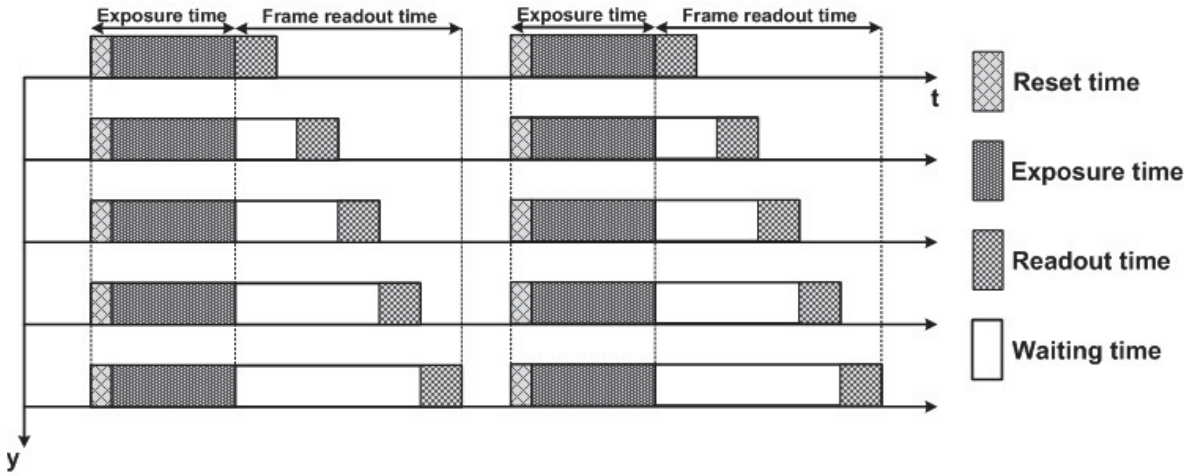

Figure 2-5: Working principle of triggered global shutter mode

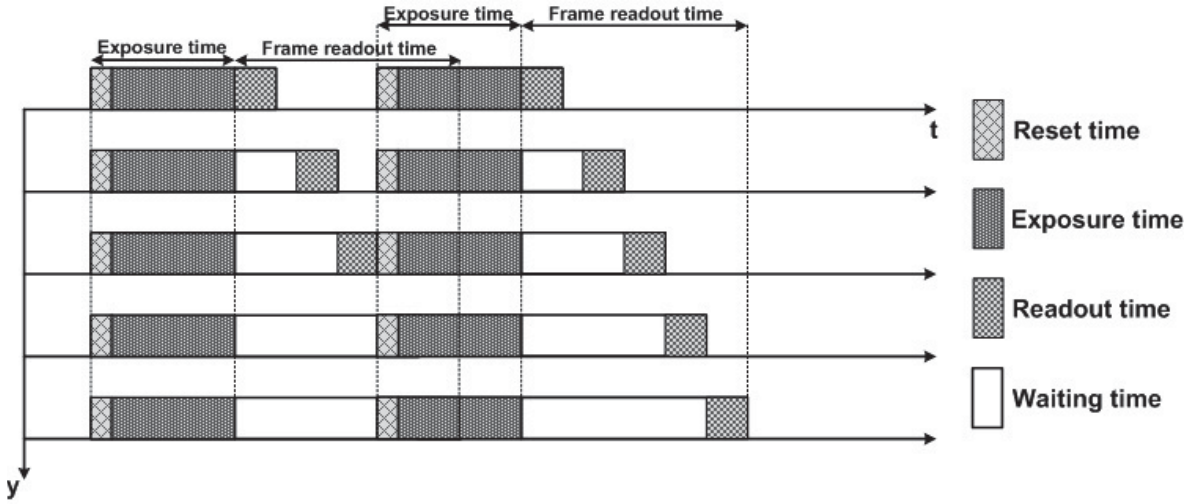

Figure 2-6: Working principle of pipeline global shutter mode

From the above timing diagram we can know that the two samplings perform in the same integration period, thus, the kTC noise carried by V_{RESET} and V_{SIGNAL} are correlated. As a result, the kTC noise can be cancelled completely by subtracting the two samples from each other, as well as the offset voltage. What's more, due to the interval period between two samplings is short, the flicker noise can be effectively reduced by CDS as well.

Global shutter mode:

1. At the end of integration time, the charge transfer operations for all rows happen simultaneously by a TG pulse.
2. During the readout time, the particular row is addressed and the floating diffusion node voltage becomes available to read.
3. The video voltage V_{SIGNAL} first sampled by switch S1 and capacitor C1.
4. After the video voltage sampling, the FD node is reset by RST pulse and this reset level is sampled again by switch S2 and capacitor C2.

Compared with the rolling shutter mode, an obvious difference of sampling operation in global shutter mode is that the first sampling value is video signal level and then is the reset level. As a result of two sampling operations are happening in different reset phases, the non-correlated noise of two sampled voltages becomes one of the main noise sources of pixel. Therefore, such readout scheme of 4T pixel structure leads to a higher pixel temporal noise.

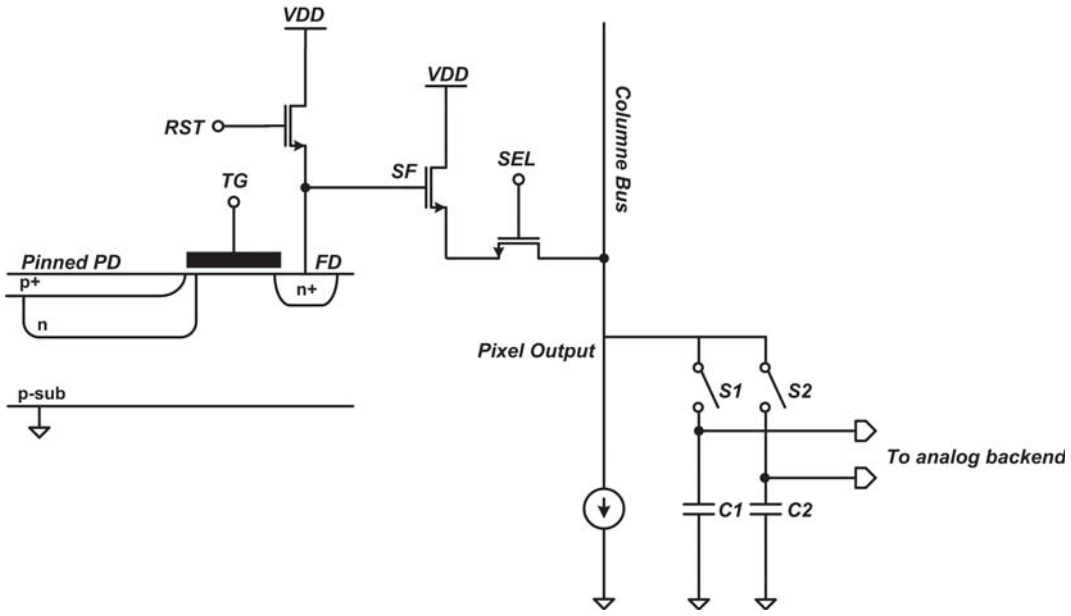

Figure 2-7: 4T pixel schematic with cross-section of the photosensing and charge transfer gate region

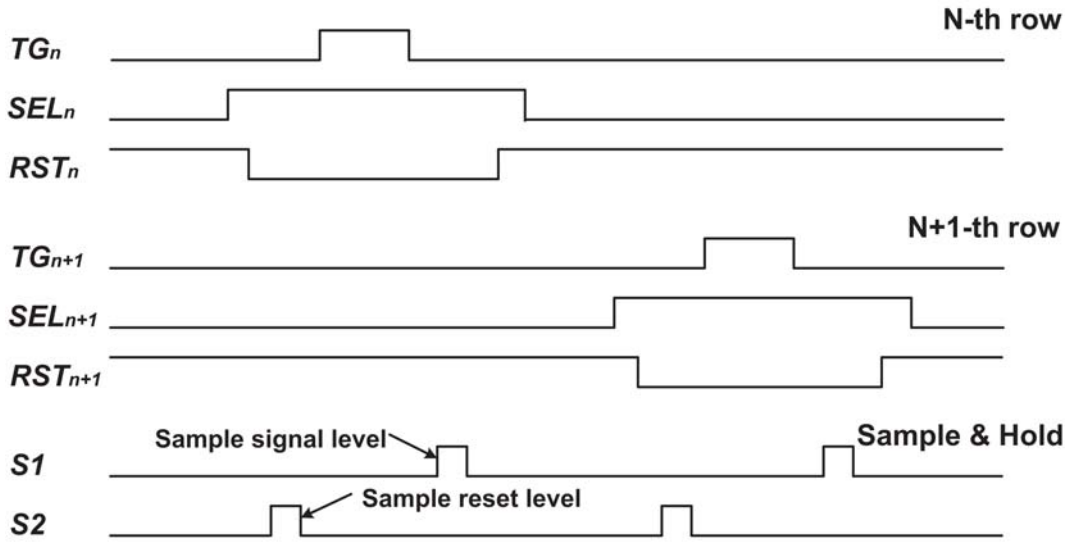

Figure 2-8: 4T PPD pixel timing diagram of rolling shutter mode

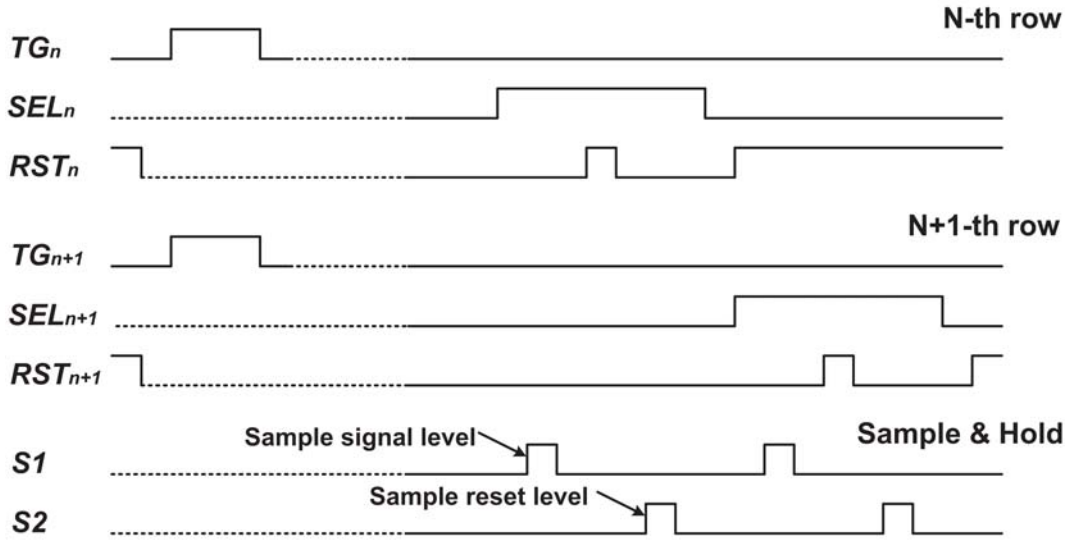

Figure 2-9: 4T PPD pixel timing diagram of global shutter mode

2-4 Overview of global shutter pixel structure

As the market of machine vision, industrial, automotive, and high speed cameras applications becomes larger than before, the requirement of CMOS image sensor with the merit of fast-moving objects acquisition without motion blur have grown steadily. However, with the usage of global shutter pixel technology, there are still some technical challenges need to be solved.

In Section 2.3, we present the typical PPD 4T pixel structure working principle by using two kinds of electronic shutters. Except for the noise problem, there are also some other issues of global shutter pixel that are of concern:

1. Fill factor and QE: for global shutter pixels, one of the chief drawbacks is the requirement of an additional pixel level memory. Due to this extra node in pixel, the fill factor of global shutter pixels is smaller than that of rolling shutter counterpart all the time. To compensate this drawback, a global shutter pixel often is larger than a rolling shutter pixel in size, as shown in Figure 2-10. Considering the FWC explained in the previous sub-session, if the charges are stored in the memory node in the charge domain, the pixel FWC is not only limited by the photodiode FWC but also by the FD node capacity. Thus, in order to hold all the electrons transferred from the photodiode, the charge storage capacity of this memory node needs to be large enough, so that the full well of the pixel can just be limited by the photodiode. In contrast, a large memory node has an adverse impact on quantum efficiency which means, for the purpose of increasing the quantum efficiency, the area of this node should be as small as possible. Therefore, we need some trade-off consideration between the photodiode and memory node. Besides, micro lenses used for global shutter pixels also need to be optimized, so that the incident light can be effectively collected by the photodiode [26].

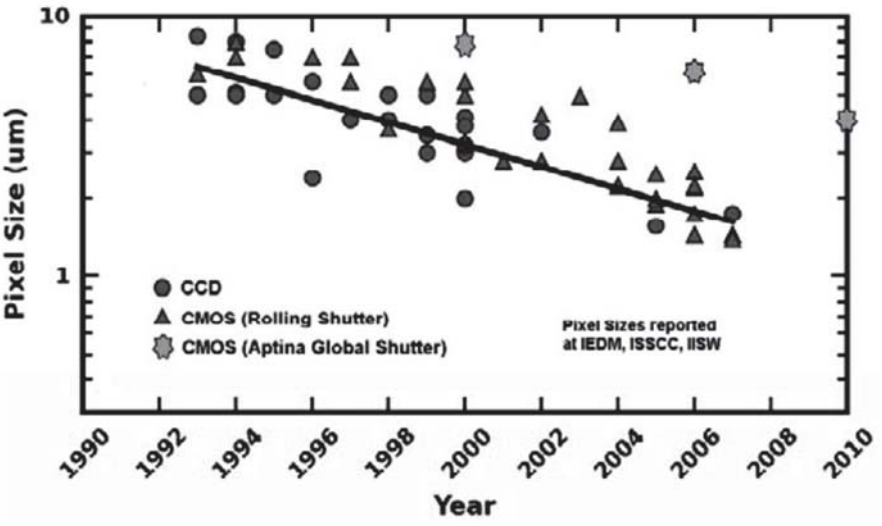

Figure 2-10: Trend in Rolling and Global shutter pixels, redrawn from [26]

2. Dark current: the floating diffusion node is a heavy dark current region in the pixel. It is caused by several serious process-induced damages, such as high dose implantation and contact etching process [27]. For rolling shutter pixels, because the "storage time" of the FD node is short, the contribution of FD generated dark current to the total count is usually negligible. Nevertheless, for global shutter pixels, if the signal is stored in the FD mode, this FD induced undesirable dark current become severe and highly contaminates the signal stored in it. In order to solve this problem, people come up some methods, for example, passivate or pin the surface of the memory node [26].

3. Parasitic light sensitivity (PLS) or Global shutter efficiency (GSE): PLS is a significant parameter for a global shutter pixel. It measures the performance of a memory node protected from parasitic light contamination. In a global shutter pixel, for example, when the incident light falls onto the pixel, due to the effect of diffraction and scattering, the photodiode cannot be 100% focused on by incident light. Furthermore, in response to incident stray light, the memory nodes act as a parasitic photodiode and generates electron-hole pairs. As a result, during the storage time, the photo leakage portion of incident light from a bright light hits the pixel memory and contaminates the stored signal, resulting in smear-like artifacts. In order to minimize PLS, the memory node requires covering by a metal light shield, and this metal light shield should be close to the memory node so as to prevent a wide angle stray light arriving [26]. What's more, as mentioned above, the micro lens needs to be optimized so that the light can be focused on the photodiode as much as possible.

In order to overcome these barriers which limit the widespread global shutter pixel utilization, CMOS image sensor developers provide various global shutter alternatives. All of their aim is to develop the global shutter pixel technology with a smaller pixel size, lower noise and dark current, larger fill factor and lower PLS, closing their counterpart performance gap between rolling and global shutter pixels. In the next subsection, we will briefly introduce the following global shutter pixel structure: pinned photodiode pixel with five transistors, hybrid charge coupled CMOS image sensor pixel with seven transistors, two stage charge transfer pixel with a dual-shuttering mode and "voltage domain" 9T pixel.

2-4-1 5T global shutter pixel

The intention of a five transistor pixel based on a pinned-photodiode sensing element is to completely empty the channel region of the photodiode after reset and readout, as well as control the exposure time [28].

As shown in Figure 2-11, a 5T PPD pixel consists of a pinned photodiode, a floating diffusion node and five transistors. Its structure is very similar to that of a 4T PPD pixel, except for the extra exposure control gate EC, the drain of which is connecting to V_{EC}.

The EC gate controls the global reset of the pixel and TG controls the charge transfer from the PPD to the FD node. During the integration time:

- All pixels are reset by the global reset signal EC first, the prior charge from the photodiode can be drained away by the positive voltage V_{EC}, the photodiode is reset.

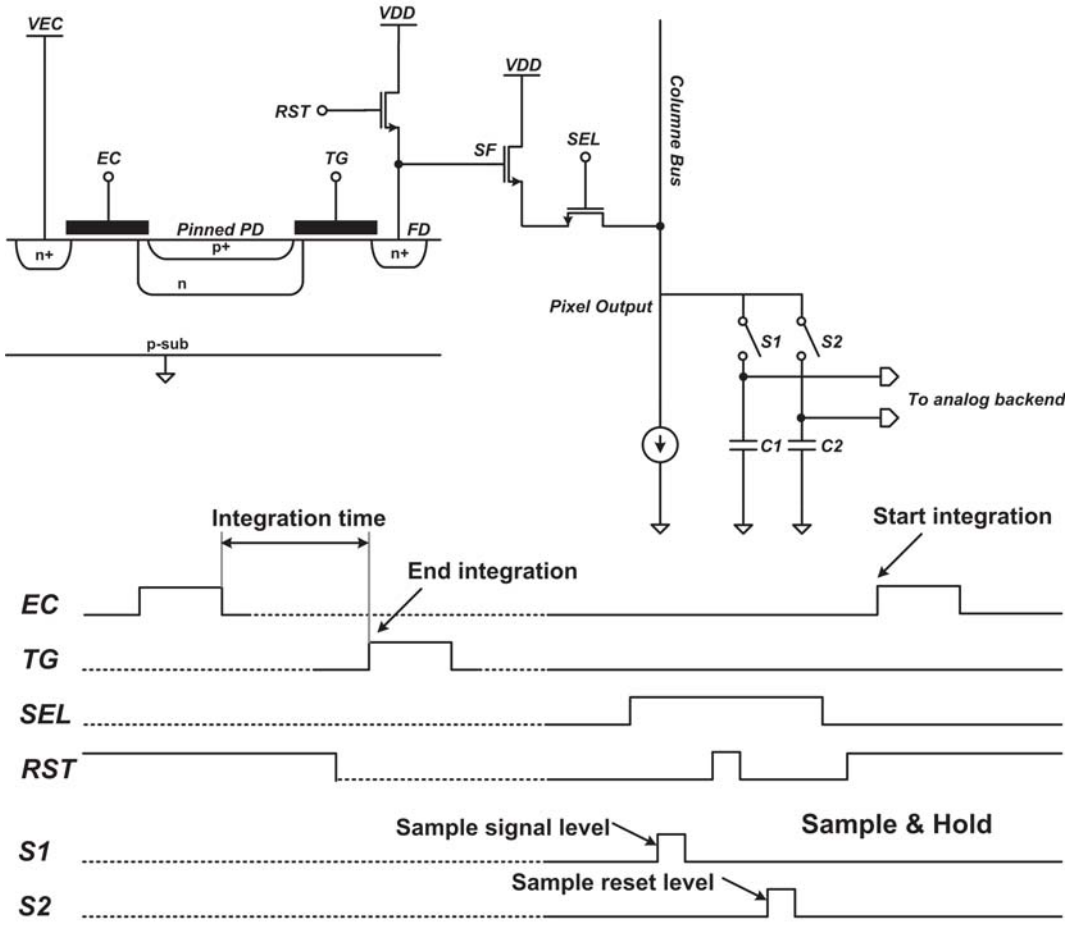

Figure 2-11: 5T PPD pixel schematic and timing diagram [28]

- At the end of integration, the global TG signal forces the accumulation charges transfer into FD node.

Readout the signal is performed in the next frame time:

- After integration, similar to the 4T PPD pixel under global shutter mode, the video signal level V_{SIGNAL} is first sampled and then FD node is reset and the reset level V_{RESET} sampled.
- The imager is able to start a new integration operation by resetting EC, while the previous frame is readout.

By adding the extra gate EC, the 5T pixel allows the exposure control and also allows for the pipeline global shutter readout mode which significantly increases the imager frame rate. However, because two sampling operations are happening in different reset phases, it does not solve the non-correlated double sampling problem. Thus, the noise level for a 5T APS in global shutter mode is still high.

2-4-2 7T hybrid charge coupled CMOS image sensor pixels

In order to do the correlated double sampling and decrease the noise level, people realized another memory node, which can store the video signal value before reset FD operation, is needed. Therefore, an active pixel that incorporates a CCD element into a CMOS image sensor is developed [29].

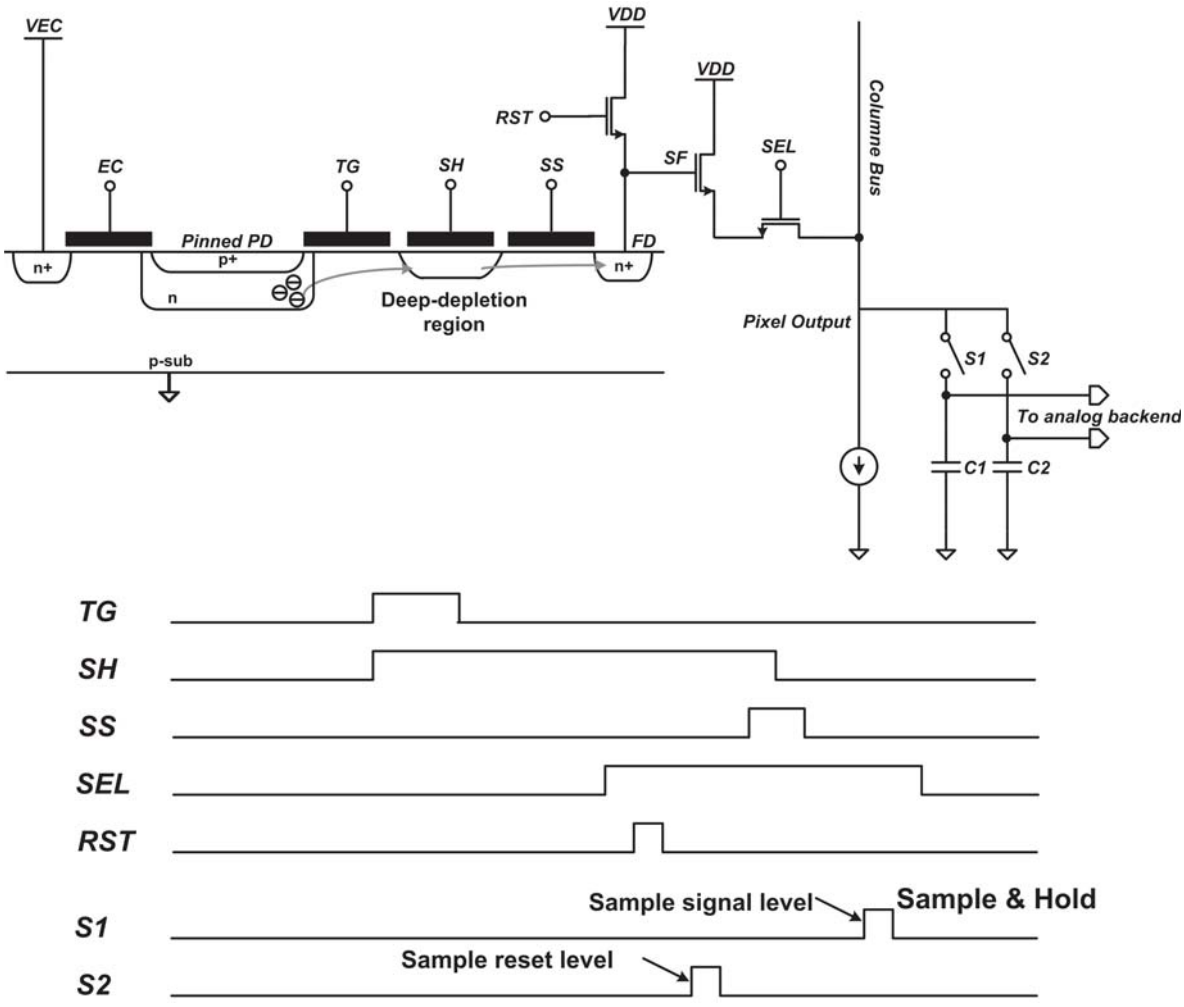

Figure 2-12: 7T PPD pixel schematic and timing diagram [29]

Figure 2-12 shows the cross section of the photo-sensing element and the pixel structure. In this pixel, the light-induced video signal charges transferring to the floating diffusion node should across three gates: transfer gate TG, memory gate SH and control gate SS. By adding the memory gate and the control gate, the pixel includes a memory node to store the video signal charges. This method is an analogous manner to CCD image sensors.

During the frame time:

- At the end of the integration time, both the transfer gate TG and memory gate SH are activated. The applied voltage on the memory gate forms a potential well underneath the memory gate. Thus, the charge generated in the photodiode flows to the memory well.
- In the readout time, the RST signal first reset the FD node and then the reset level V_{RESET} is sampled by switch S2 and capacitor C2.
- After the first sampling, the control gate SS turns on, the signal charges, which are stored in the memory well, are transferred to the FD node. When the transfer process is finished, the video signal V_{SIGNAL} is sampled by switch S1 and capacitor C1.

From the above timing diagram we can know that the two samplings perform in the same integration period, thus, the kTC noise carried by V_{RESET} and V_{SIGNAL} are correlated. As a result, the correlated noise can be cancelled by CDS and decrease the noise level.

2-4-3 Two stage charge transfer pixel with a dual-shuttering mode

Although the 7T active pixel is able to cancel the kTC noise by means of CDS, it still suffers from dark current due to the use of surface channel storage gates and the low shutter efficiency problem. What's more, charge transfer is also another severe problem existing in a 7T pixel structure. Because in CMOS technology process, there is a minimum space requirement between two poly-silicon, thus, the gate SH is unable to be closely placed near gate TG, it leads to a barrier between the deep depletion region underneath the gate SH and channel below the gate TG. This barrier has a negative impact on charge transfer between the photodiode and the memory well.

In order to perfect the performance of global shutter pixel, people continued to improve the pixels technology and structure. An improved global shutter pixel with two-stage charge transfer for reduced noise and higher shutter efficiency is developed [30].

As can be seen from Figure 2-13, the pixel structure consist of two pinned diodes the PD and the SD, and seven transistors. The PD is used for photoelectron conversion and the SD is used for charge storage, which function is similar to the memory well in 7T pixel. The two global shutter gates are respectively named by GS1 and GS2. In order to perfect the charge transfer, the potential difference between the two pinned diodes is a necessity. In their work, the potential difference is achieved by using two different doping layers. n_1 for the PD and n_2 for the SD, besides, the p-type doping layer p_1 create a stepwise potential under GS1 and GS2, it also helps to improve the charge transfer efficiency. For the purpose of decreasing the parasitic photosensitivity and anti-blooming the PD charge into the SD, a shielding layer is adopted. It is implemented by introducing the p-type doping layer p_2 beneath the n_2 layer in the SD. This shielding layer creates a potential barrier to prevent the leakage electrons from all directions [33]. As a result, parasitic light sensitivity is significantly reduced, improving the shutter efficiency.

For the application of wide dynamic range imaging, the dual global shutter operation can be used. In the dual global shutter mode, both the SD and the FD are used as memory node, thus, two snapshot images are captured for every frame. During the integration time:

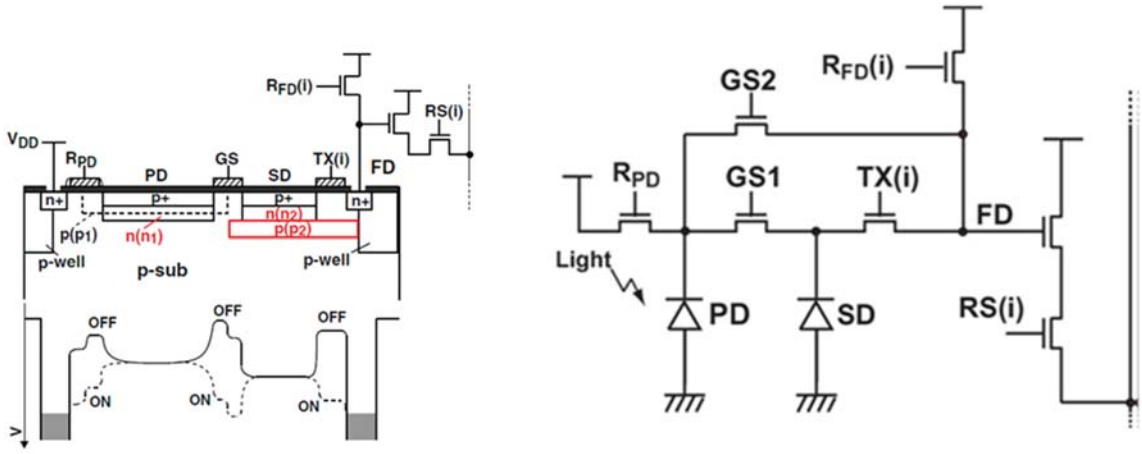

Figure 2-13: Pixel structure and the layout, taken from [30] and [31]

- PD first is reset by R_{FD} , the integration begins in the PD.
- After the first integration time, the accumulation charges in the PD are transferred to the SD by using GS1.
- PD is reset by R_{FD}, integration starts again in the PD.
- After the second integration time, the accumulation charges in the PD are transferred to the FD by using GS2.

Readout of the two signals is performed during the next frame time:

- First, readout from the FD memory node, because the video signal level is first readout and then is the reset level of FD node, the kTC noise of the two values is not correlated, thus, they just do the double sampling.
- Second, readout from the SD memory node, because the FD node is reset before readout, the kTC noise for the video signal level and reset level are correlated, they can do the correlated double sampling to decrease the noise.

In the wide dynamic range imaging, the kTC noise free SD memory signal readout with high gain column amplifiers is used for the low-illumination region. On the other hand, the noisy FD memory signal readout with low gain column amplifier is used for the high-illumination region.

2-4-4 "Voltage domain" global shutter pixels

In order to do the CDS and decrease the noise level, both hybrid charge coupled CMOS image sensor pixels and two stage charge transfer pixel, mentioned above, have a common

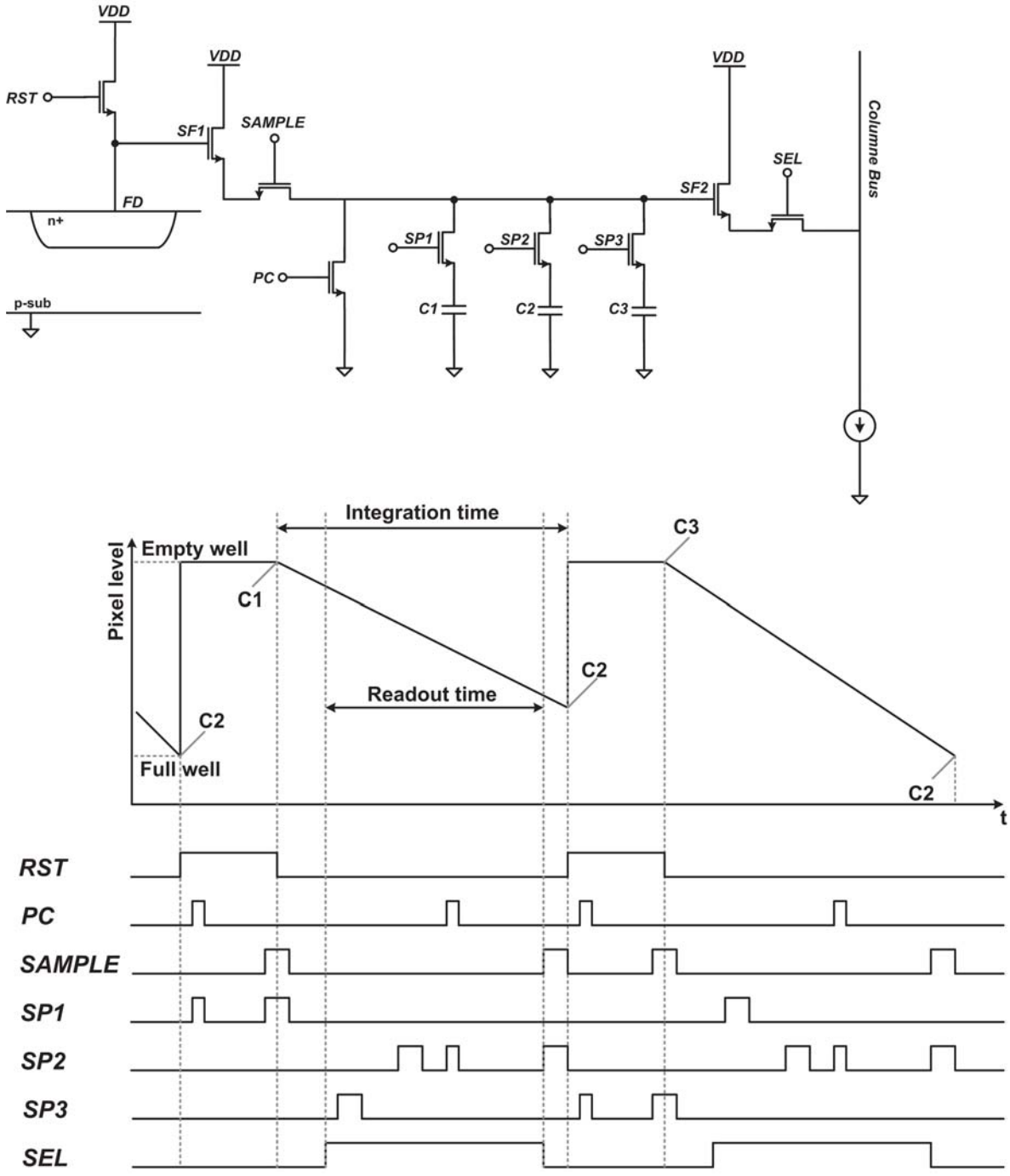

Figure 2-14: 9T PPD pixel schematic and timing diagram redrawn from [32]

characteristic. That is, when a pixel is readout, charges from the photodiode transferred to a shielded area, e.g. CCD-like memory well and diode, are stored in the form of "charge domain". Since this shielded area cannot be completely "shielded", due to the non-perfect isolation from the sensitive area of the pixel,the "charge domain" global shutter pixel sustains a relative large charge spillage and result in a parasitic image artifacts [33]. In order to significantly reduce the PLS, directly converting charges into a voltage and storing them in "voltage domain" becomes an attractive way for global shutter pixel.

The pixel structure which will be presented below is developed for spaceborne imaging application such as hyperspectral imaging [34]. The pixel architecture combines CDS with a pipelined global shutter for low noise and is implemented in a backside-illuminated approach for the purpose of large full well capacity. Figure 2-14 shows a pixel which consists of two stages: a light sensitive stage and a sample and hold stage with three storage capacitors.

During frame time:

- As a start, the photodiode is reset by RST, and this V_{RESET} value is sampled on C1 by switch SAMPLE and S1.
- After the reset operation, the photodiode begins to integrate. In order to perform CDS, at the end of the integration period, the video signal value V_{SIGNAL} is sampled on C2 by switch SAMPLE and S2.
- When the first integration period is completed, a further reset of photodiode follows and the V_{RESET} value should be sampled again. However, at this time, the sampled value from last frame still is present in C1, therefore, the V_{RESET} value of the second reset operation is sampled on C3 by switch SAMPLE and S3.
- Shortly thereafter reset, the signals stored on capacitor C1 and C2 are sequentially presented to a correlated double sampler, e.g. a differential amplifier, where the actual signal level without correlated kTC noise is obtained by subtracting the sample of the reset voltage from the second sampled signal.
- At the end of the second integration, the video signal level sampled and stored on C2 again.

In this operation, the reset value V_{RESET} is stored by toggling between C1 and C3, and the signal value V_{SIGNAL} is always stored on C2. Among all the control signals, PC, S1, S2, S3 are global signals during reset and sample phase, but readout row by row is performed under the control of SEL.

2-5 8T global shutter pixel

As previously explained, the global shutter pixel development target is towards a global shutter pixel technology with smaller pixel size, larger fill factor, higher GSE, lower noise and dark current.

In this thesis, a pixel architecture which consists of 8 transistors with 4.8μm pitch is developed. Figure 2-15 shows a basic idea of this pixel structure. This pixel supports both correlated double sampling as well as global shutter operation.

- During the Frame Overhead Time (FOT), the pixel stores the reset level into C2, after the charge transfer, the video signal level signal is stored in C1, where C1=C2.
- During Row Readout Time (ROT), the video signal charge is redistributed between C1 and C2.
- During Correlated Double Sampling (CDS), the two storage levels are subtracted from each other and the correlated reset noise is eliminated.

Since the voltage leak due to the PLS on the two capacitors is the same, this undesired effect will also be subtracted during CDS. As a result, a high shutter efficiency can be achieved. Further details of the working principle of this pixel will be explained in Section 3-1

In a previous design work, a 2.2M CMOS image sensor with 8T pixel of 5.5μm pitch was implemented [35]. The sensor is made in 0.18μm CMOS process. The noise level is as low as 13 e^- RMS and a pixel parasitic light sensitivity of 1/60000 is achieved. Table 2-1 shows the sensor characterization result. In this thesis work, with a smaller feature size technology and a smaller pixel pitch, we foresee a higher conversion gain and a lower input referred noise of this kind of pixel.

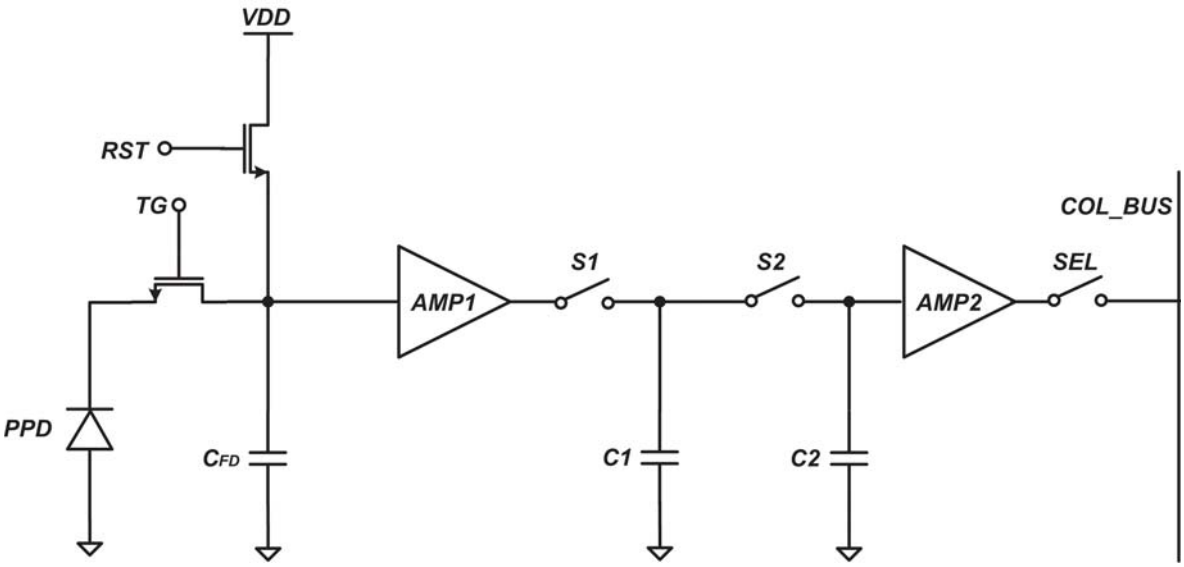

Figure 2-15: Basic 8T pixel structure [35]

2-6 Conclusion

In this chapter, we first introduced the basic concept of optical absorption and the operation of photodiode. Next, two electronic shutter modes: rolling shutter and global shutter were presented, together with their image quality and working functions. Specifically, the global

Table 2-1: Sensor specification taken from [35]

Specification	Value	Unit
Process technology	0.18 μm CIS	
Pixel pitch	5.5×5.5	μm^2
Pixel type	8T Global shutter	
Effective number of pixels	2018 columns×1088 rows	
Fill Factor	42	%
Temporal noise	13	e^-rms
Fixed pattern noise	<0.1	%
CG	85	$\mu V/e^-$
Full well charge	18	ke^-
Sensitivity	4.46	V/lux.s
DR	61	dB
PLS	1/60000	
Power consumption	600	mW
Max. frame rate	340	fps

shutter mode also can be divided into two sub-type: triggered mode and pipeline mode. We also described the characteristics of two sub-type global shutters. Based on these principles, several kinds of alternative global shutter pixels were presented. For example, 5T global shutter pixel which adds an exposure control transistor; 7T hybrid charge coupled CMOS pixel which combines the CCD element and CMOS pixel circuit together; Two stage charge transfer pixel which uses two pinned diodes to store the signals. However, since these three type pixels all store their signals in "charge domain", they more or less suffered the PLS effect. Thus, we introduced the 9T "voltage domain" global shutter pixel which store their signals in the form of voltage until readout. Finally, the basic 8T global shutter pixel structure and previous design characterizations were provided.

Chapter 3

The pixel array

In the previous chapter, we briefly introduced the characteristics of the global shutter 8T pixel. In this chapter, the circuit level implementation of this kind of pixel will be described in detail. In Section 3-1, the pixel architecture and operation will be explained. Next, the theoretical modeling of the noise analysis will be discussed in Section 3-2. Section 3-3 presents some schematics and layout considerations of 8T pixel. Finally, the pixel simulation results will be shown in Section 3-4.

3-1 Pixel architecture and operation

3-1-1 Pixel architecture

The schematic of the 8T pixel with cross-section of the photo-sensing and charge transfer gate region in this project is shown in Figure 3-1. Similar to the typical 4T pinned photodiode pixel architecture, the photo-sensing element in this pixel is a Pinned Photodiode (PPD). The transfer gate TG, connecting the photodiode and Floating Diffusion (FD) node, is intended for charge transfer. RST is the reset transistor that is used to reset the FD node. SF1 operates as a source follower to amplify the light induced signal charges. PC acts as a current source load for SF1, besides, it is also used to pre-charge the sample capacitor. The switches S1 and S2 together with the sample capacitors C1 and C2 implement the sample and hold functionality in pixel. Source follower SF2 buffers the sample signals to the column bus, and the row select transistor RS selects the pixel to readout. Block COL_PC represents the column load which contains two current source. A continuous current source I1 with a small current and a switched current source I2 with a large current ensure a fast readout speed without a voltage swing reduction in every column bus.

In this pixel, the source followers SF1 and SF2, and bias transistors PC work in the saturation region. The row select transistor RS operates in the linear region such that the pixel output voltage can follow the sampled voltage on C2 linearly. Two sample capacitors C1 and C2 are used to store the reset and video signal, both of them are MOS capacitors. For MOS

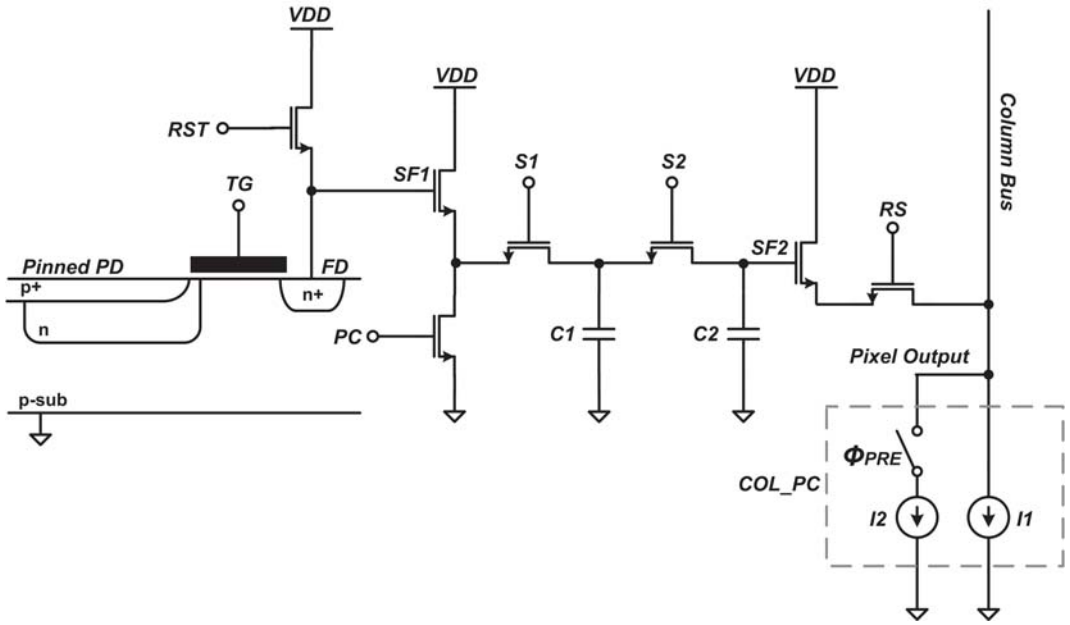

Figure 3-1: 8T PPD pixel schematic with cross-section of the photo-sensing and charge transfer gate region

capacitors, when the gate voltage is much larger than the threshold voltage, it remains in the strong inversion mode and a capacitor is formed between the gate oxide and the substrate where an inversion layer exists. If the capacitance and the parasitic current of both capacitors are equal, the voltage degradation due to PLS on both capacitors is the same and its effect will be cancelled during CDS. Thus, the final PLS is negligibly small.

3-1-2 Pixel operation

The 8T global shutter pixel potential and timing diagram are shown in Figure 3-2 and Figure 3-3 respectively. The operation at the beginning of the frame is as follows:

Integration: First, the pinned photodiode is fully depleted and is at its respective pinned potential V_{pin} as shown in Figure 3-2. The electrons are generated through the absorption of photons, and are collected in the pinned photodiode during the exposure time. At the same time, the FD node is kept reset to the pixel high power supply VDD. Apart from removing any redundant charges at FD, this continuous reset is acting as an anti-blooming control, draining away excess charge from the photodiode through the transfer gate TG and reset transistor RST when the sensor is exposed to a large amount of light.

Sample V_{RESET}: At the end of exposure time, FD is released from resetting by switching off the transistor RST. Concurrently, both switches S1 and S2 are on, capacitors C1 and C2 are discharged by the pre-charge transistor PC before they are recharged by the source follower to their final value. After that, PC still delivers a certain bias current to bias the source

follower SF1 and meanwhile the reset level V_{RESET} is sampled on both C1 and C2. When S2 is switched off, this reset level remains stored on C2.

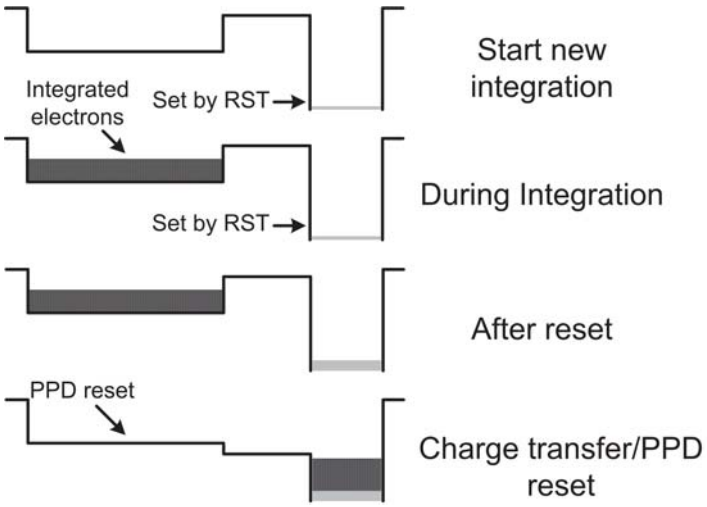

Figure 3-2: Potential diagrams of the PPD, TG and FD during integration start, charge integration, FD reset and charge transfer/PPD reset.

Charge transfer & Sample V_{SIGNAL}: After sampling the reset signal, the photon-generated electrons are transferred from the pinned photodiode to the floating diffusion by switching on the transfer gate TG. At the same time, since S1 is kept on during the complete transfer process, the video signal level V_{SIGNAL} is sampled on C1. After V_{SIGNAL} sampling, the switch S1 is off so that the V_{SIGNAL} is preserved on C1, and the PPD is automatically reset and ready for the start of the integration of the next frame. In order to ensure that all charges are evacuated from the photodiode, an additional reset can be generated after charge transfer, achieved by pulsing the reset transistor RST and the transfer gate TG together.

Readout: During the Row Readout Time (ROT), the SEL transistor is switched on, so as to activate the source follower SF2 of that row. At the start of the column sampling phase, the large current source I2 is enabled first and pulls the column bus low. Soon after that, this current source is switched off and the source follower SF2 operates with only the small current source I1 as load. Then, the reset level V_{RESET} which is stored on C2 is readout first. Afterwards, S2 is switched on to short C1 and C2 so that the light-induced signal charges stored on C1 is redistributed in both C1 and C2. During this charge redistribution, the charge on C1 and C2 is expressed as:

$$Q = C1\Delta V_{SIG} = (C1 + C2)\Delta V_{SIG2} \tag{3-1}$$

$$\Delta V_{SIG2} = \frac{C1}{C1 + C2}\Delta V_{SIG} \tag{3-2}$$

where $\Delta V_{SIG} = V_{RESET} - V_{SIGNAL}$, the voltage drop on the floating diffusion node due to the charge transfer, ΔV_{SIG2} is the voltage drop on C2 due to the charge redistribution.

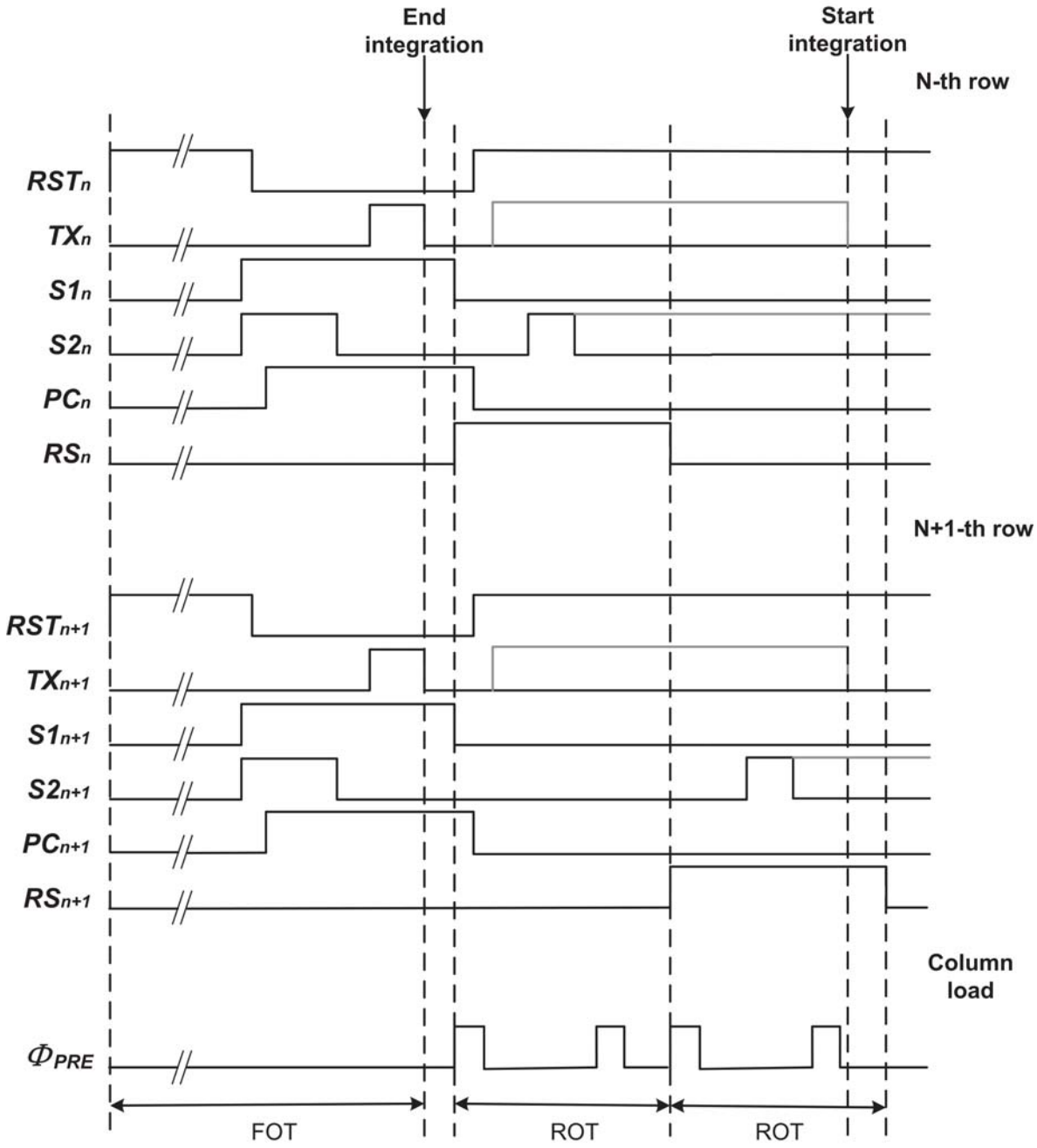

Figure 3-3: Timing diagram for 8T global shutter pixel

What's more, we have already stated that if $C1 = C2$, the PLS effect could be extremely small. Thus, the voltage drop on C2 is attenuated by a half: $\Delta V_{SIG2} = \frac{1}{2}\Delta V_{SIG}$.

Thereafter the charge redistribution, the attenuated signal $V_{SIGNAL2}$ ($V_{SIGNAL2} = V_{RESET} - \Delta V_{SIG2}$) is readout as the video signal. During this process, two operation modes can be

realized as shown in Figure 3-3. If S2 is switched off during the period of SEL pulse, C2 will see a complete switching cycle from the S2 transistor. If S2 is kept on when reading the video signal, the kTC noise from the S2 transistor is not included, which results in a reduced pixel readout noise while introducing an additional offset because of the asymmetric sampling access of Mode1 [31].

3-2 Noise analysis

3-2-1 Overview of noise in CMOS image sensors

Noise is one of the most significant parameters in CMOS image sensor. It is required to be seriously considered during the whole procedure of design, fabrication, and characterization. Based on whether the signal varies in spatial or temporal domain, the noise is divided as two types: fixed-pattern noise and temporal noise. The variation in the signals from pixel to pixels, which is "fixed" at a certain spatial position, is referred to as Fixed Pattern Noise (FPN). Another kind of noise that fluctuates within an individual pixel time-dependently, and we name it as temporal noise [36].

Usually, temporal noise in one pixel contains photon shot noise, dark current shot noise, flicker noise, reset noise and thermal noise. Due to the fact that a different noise component is originated from a different specific mechanism, these noise components mentioned above are independent from each other, thereby, the total temporal noise v_{pixel} can be approximated as:

$$\overline{v_{pixel}^2} = \overline{v_{shot\_photon}^2} + \overline{v_{shot\_dark}^2} + \overline{v_{reset}^2} + \overline{v_{theraml}^2} + \overline{v_{1/f}^2} \tag{3-3}$$

where v_{shot_photon} is the photon shot noise, v_{shot_dark} is the dark current shot noise, v_{reset} is the reset noise, $v_{thermal}$ is the thermal noise, and $v_{1/f}$ is the flicker noise. In order to make a direct comparison with the number of electrons generated from the photo-detector, the noise figures can be written in numbers of equivalent noise electron n_{noise} and referenced to the floating diffusion node. Its conversion with noise level v_{noise} can be written as:

$$\overline{v_{noise}^2} = CG^2 \times \overline{n_{noise}^2} \tag{3-4}$$

3-2-2 Fixed-pattern noise

As the leading source of FPN is varied in different conditions, FPN analysis is often separated as two categories: in the dark and under illumination. Dark FPN or offset FPN is usually evaluated by Dark Signal Non-Uniformity (DSNU), which represents the offset distribution of the voltage output across the entire pixel array without any illumination. Illumination FPN, which is also treated as gain FPN, is evaluated by Photo Response Non-Uniformity (PRNU). The definition of PRNU is similar with DSNU except for the condition is under illumination rather than in the dark. Generally, FPN in dark is considered to be the offset variation of pixel output as its value is constant for given pixels at a fixed exposure time. The main cause of this offset FPN is the mismatch between pixel-level and column-level transistors, and the dark current non-uniformities generated inside the pixel array.

Pixel-level FPN: The silicon fabrication process always introduces significant mismatches to the transistor parameters. In the case of the 8T global shutter pixel, in spite of no mismatch

report of this 110nm technology available, we can still see the parameter variations between the transistors from the corner analysis model document, such as threshold voltage V_{TH}, saturation current I_{DS} and parasitic capacitors in the transistor. The 8 transistors and 2 MOS capacitors used in pixels all introduce pixel-level FPN among the whole pixel array due to the mismatch of offset, gain and charge injection. However, even though this pixel-level FPN is caused by many sources, it can be effectively eliminated by Double Sampling (DS). In this project, it is canceled by Correlated Double Sampling (CDS): by subtracting the two voltage levels V_{RESET} and $V_{SIGNAL2}$, which are sampled before and after the charge integration, the offset induced by the in-pixel mismatch can be completely deleted.

Column-level FPN: Another mismatch-caused FPN appeas between the column circuitry of the pixel array. It is often called as column-level FPN. For the CMOS imagers with column level processing circuitries, the main source of the column-level FPN in the whole sensor is the column parallel readout chain. This test chip contains 1280 parallel readout channels, each of which consists of a Programmable Gain Amplifier (PGA) stage, a Sample and Hold (S/H) stage and an ADC stage. Any mismatch between the channels leads to the column FPN, result in the stripe-like images and severely degradation of image quality [37]. Unfortunately, compared with pixel-level FPN, column-level FPN is often more conspicuous and is harder to eliminate. Thus, in order to realize a sufficient column to column uniformity, so as to do not produce any apparent artifacts, people have come up many solutions, both in circuitry solutions and in the digital domain. For the purpose of suppressing the offset mismatch between columns, an auto-zero technique and a two step CDS have been done in this test-chip. These two circuitry techniques are chosen because they are simple, yet efficient in our case and we will return to this issue in Chapter 4.

Dark current FPN: From the previous chapter we have known that the photon current can be generated under the condition of illumination. However, even without illumination, the electron-hole pairs can also be created in the photo-sensing area and forms the current. This current that is from a pixel but without illumination is referred to as dark current. It should be noted that the dark current of each individual pixel is not uniform over the entire pixel array, thus, this dark current FPN is also difficult to eliminate [27]. As a consequence, it is indispensable to design and layout the pixel very carefully for the purpose of dark current reduction. In this 8T global shutter pixel, the pinned photodiode and the idea of storing the signal in "the voltage domain" have been adopted for the dark current reasons. Besides that, a few other methods have been used in the pixel layout also and we will refer to them later in Section 3-3.

PRNU: FPN under illumination is mainly caused by the photo-response gain mismatch of the different pixels, often called PRNU. It is noticeable that, dissimilar with dark FPN, the magnitude of FPN under illumination is often proportional to the illumination condition. In this 8T pixel case, except for the influence of dark FPN, there are three other sources causing PRNU [35].

- Non-uniformity of light collection.
- Non-uniformity of photon-electron conversion or the variation of effective fill factor.
- Non-uniformity of electron-voltage conversion or the variation of conversion gain.

3-2-3 Photon shot noise and dark current shot noise

Photon shot noise is an unavoidable noise in imaging systems due to the fundamental property of the quantum nature of light and the granularity and discrete nature of the electrons themselves. When a photo-detector is exposed to a uniform light source, the interval of photons arrivals and the amount of photon-generated electron-hole pairs in photo-sensing region are all random variables. In addition to that, the noise statistical distribution of the photon current is described by a Poisson distribution [38]. Therefore, the magnitude of the photon shot noise equals the square root of the mean number of electrons generated in the photo-sensing area. This relationship is given by:

$$n_{ph} = \sqrt{N_{sig}} \tag{3-5}$$

where N_{sig} is the signal charge, and n_{ph} is the photon shot noise in electrons. Besides the photon induced current, dark current, which mentioned in the previous subsection, also introduces the shot noise. The same as the photon-current, it is also governed by a Poisson distribution and is given by:

$$n_{dc} = \sqrt{N_{dc}} \tag{3-6}$$

where N_{dc} is the mean value of the dark count and n_{dc} is the dark current shot noise in electrons. Thus, the rms noise voltage due to photon shot noise and dark current shot noise is shown as :

$$\overline{v_{photon}} = CG \times \sqrt{N_{sig}} = CG \times \sqrt{\frac{I_{photon} t_{\text{int}}}{q}} \tag{3-7}$$

$$\overline{v_{dark}} = CG \times \sqrt{N_{dc}} = CG \times \sqrt{\frac{I_{dark} t_{\text{int}}}{q}} \tag{3-8}$$

where I_{photon} is the average photocurrent, I_{dark} represents the average dark current, t_{int} is integration time, q is the elementary charge and CG is the conversion gain. As can be seen from the above equations, the rms photon shot noise has a square root relationship with the photocurrent and integration time. Thus, different with other noise sources in CMOS image sensor, the photon shot noise is depend on the illumination level.

In this 8T global shutter pixel, when the photodiode is reset, and the light-generated electrons begin to integrate onto the photodiode. Assuming the integration time is t_{int1}, photon shot noise power can be written as:

$$\overline{v_{n,PD,shot}^2} = \frac{q I_{photon} t_{\text{int1}}}{C_{PD}^2} = \frac{q(V_{pin} - V_{INT1})}{C_{PD}} \tag{3-9}$$

where C_{PD} is the pinned photodiode capacity, V_{INT1} is the photodiode's voltage after integration, V_{pin} is the photodiode pinned voltage and q is the elementary charge. It shall be noticed that C_{PD} is not a constant, but varies with PPD voltage.

After the charge transfer, all the charges generated on the photodiode are assumed to be transferred to the FD node, according to charge balance, we get:

$$\overline{v_{n,FD,shot}^2} = \frac{q I_{photon} t_{\text{int1}}}{C_{FD}^2} = \frac{q(V_{RESET} - V_{SIGNAL})}{C_{FD}} \tag{3-10}$$

where V_{RESET} is the reset signal level, V_{SIGNAL} is the video signal level and C_{FD} is the FD node capacity.

3-2-4 Thermal noise and kTC/reset noise

Thermal noise is mainly generated by random thermally agitated motion of electrons inside an electrical conductor. Due to the fact that the power spectral density of such a kind of noise is nearly constant throughout the frequency spectrum, it is often treated as white noise.

In the pixel, the main noise sources in MOS transistors are the thermal noise and the flicker noise. For thermal noise, the most significant root is the noise generated in the channel [39]. The channel noise can be modeled as a current source between source and drain terminals with a spectral density of

$$\overline{I_n^2} = 4kT\gamma g_m \tag{3-11}$$

where $k = 1.38 \times 10^{-23}$J/K is Boltzmann's constant, T is the temperature and g_m is the transconductance of the MOSFET. Coefficient γ is derived to be equal to 2/3 for long-channel transistors and may be larger for submicron MOSFET.

What's more, we consider a capacitor C that is charged through a resistor R shown in Figure 3-4. Modeling the noise of R by a series voltage source V_R, we have the transfer function from V_R to V_{out} as [39]:

$$\frac{V_{out}}{V_R}(s) = \frac{1}{RCs+1} \tag{3-12}$$

And we have known that:

$$S_{out}(f) = S_R(f)\left|\frac{V_{out}}{V_R}(j\omega)\right|^2 = 4kTR\frac{1}{4\pi^2R^2C^2f^2+1} \tag{3-13}$$

where f is the frequency, $S_{out} = 4kTR$ and expressed in V^2/Hz. Therefore, the thermal noise spectrum of the resistor is shaped by a low-pass characteristic [37]. For calculating the total noise power and rms noise voltage, we write:

$$P_{kTC} = \int_0^\infty \frac{4kTR}{4\pi^2R^2C^2f^2+1}df = \frac{kT}{C}[V^2] \tag{3-14}$$

$$v_{kTC} = \sqrt{\int_0^\infty \frac{4kTR}{4\pi^2R^2C^2f^2+1}df} = \sqrt{\frac{kT}{C}}[V] \tag{3-15}$$

where f is the frequency. Eq. (3-14) and Eq. (3-15) implies that the total noise at the output of the circuit shown in Figure 3-4 is a function only of the absolute temperature and the capacitor value, and independent of the value of R. We often call this noise as kTC noise in analogue circuitries.

As we mentioned above, the FD node needs to be reset by the switch RST every frame before the charge integration starts. This reset operation (hard reset) effectively samples a bias voltage VDD onto the FD capacitor but also introduces a sampling noise. During the "on" period, this transistor RST works in its linear region and can be seen as a resistance R_{on} which contains thermal noise. This noise is then sampled and held by the capacitor FD capacitor. Thus the reset noise in rms voltage and noise charge in number of electrons can be given as:

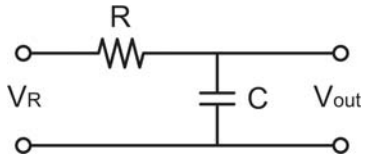

Figure 3-4: Thermal Noise generated in a RC low pass filter

$$v_{kTC,FD} = \sqrt{\frac{kT}{C_{FD}}} \tag{3-16}$$

$$n_{kTC,FD} = CG \times v_{kTC} = \frac{\sqrt{kTC_{FD}}}{q} \tag{3-17}$$

where C_{FD} is the FD capacity. At a first glance of these two equations, it seems to be s paradoxical to us since they suggest a completely opposite dependency of the noise magnitude on the FD capacitance. This is because the floating diffusion capacitance modulates not only the noise magnitude itself but also the efficiency of noise charge conversion to noise voltage. Conversion gain (CG) is inversely proportion to the capacitance, while the noise expressed in the number of electrons is only proportional to the square root of the capacitance. Since the pixel noise performance is eventually evaluated by the number of noise electrons, the FD capacitance is expected to be as small as possible in order to lower the reset noise.

In order to find the thermal noise, the kTC noise and the reset noise of this 8T global shutter pixel, an equivalent noise model is shown in Figure 3-5. In the analysis described below, noise due to the on-resistance of the switch controlled by RS is ignored to simplify analysis.

- The reset noise of this pixel is:

$$\overline{v_{kTC,FD}^2} = \frac{kT}{C_{FD}} \tag{3-18}$$

- The kTC noise of the S&H are:

$$\overline{v_{kTC,C1}^2} = \frac{kT}{C1} \tag{3-19}$$

$$\overline{v_{kTC,C2}^2} = \frac{kT}{C2} \tag{3-20}$$

- The total input-referred thermal noise of the two source followers SF1 and SF2 are [40]:

$$\overline{v_{th,sf1}^2} = \frac{8}{3}kT\frac{1}{g_{m,sf1}}(1 + \frac{g_{m,pc}}{g_{m,sf1}}) \tag{3-21}$$

$$\overline{v_{th,sf2}^2} = \frac{8}{3}kT\frac{1}{g_{m,sf2}}(1 + \frac{g_{m,col\_pc}}{g_{m,sf2}}) \tag{3-22}$$

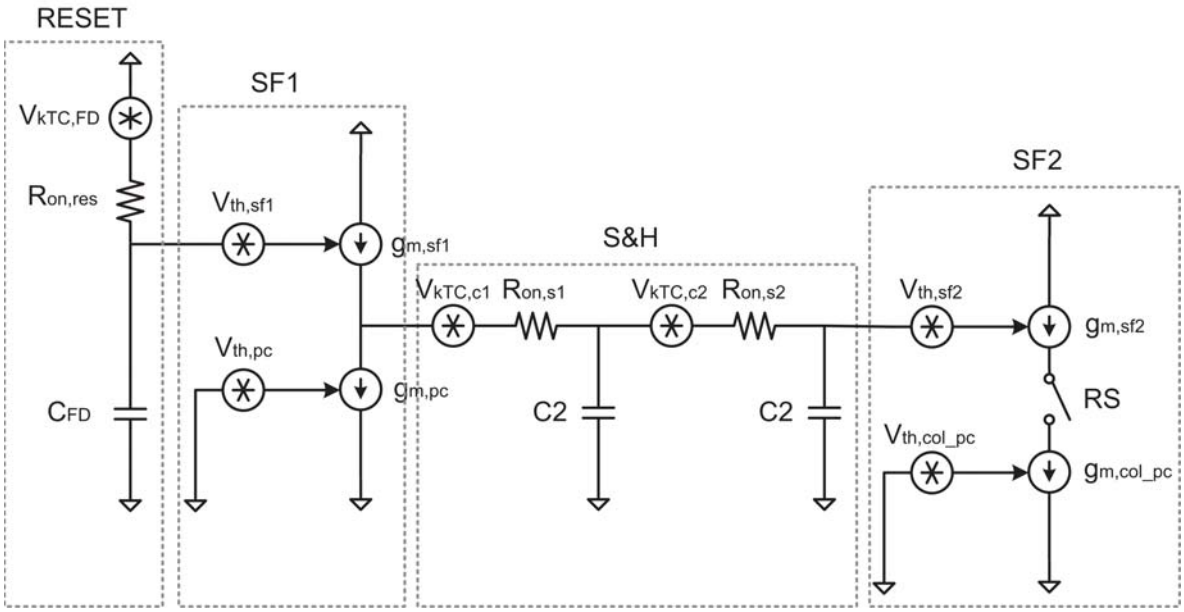

Figure 3-5: 8T global shutter pixel noise model

where $g_{m,sf1}$, $g_{m,sf2}$, $g_{m,pc}$ and g_{m,col_pc} are the transconductance of source follower SF1, SF2 and bias current source load PC and column load COL_PC (I1 or I2). Generally, the transconductance of a MOS transistor is at the order of μS and the capacitors in this pixel are of the order of fF. It is obvious that the thermal noise generated by the source followers is much smaller than the kTC noise and the reset noise, and also the flicker noise. Thus, $v^2_{th,sf1}$ and $v^2_{th,sf2}$ are allowed to be ignored in the following noise analysis.

Assuming the gain of source followers SF1 and SF2 is as one. During FOT, the reset level V_{RESET} is first sampled on C2 and the rms voltage of v_{C2} is given by:

$$v_{C2} = \sqrt{P_{kTC,FD} + P_{kTC,C2}} \tag{3-23}$$

where $P_{kTC,FD}$ is the reset noise power, and $P_{kTC,C2}$ is the kTC noise power resulting from the transistor S2 switch off.

After the charge transfer, the video signal level is sampled on C1 likewise and the rms voltage of v_{C1} is expressed as:

$$v_{C1} = \sqrt{P_{kTC,FD} + P_{kTC,C1}} \tag{3-24}$$

where $P_{kTC,C1}$ is the kTC noise power come from the transistor S1 switch off.

During ROT, the reset signal stored on C2 is first readout as the reset level. Then switch S2 is on, the video signal is redistributed on both C1 and C2, and the noise power is also added together. The signal on the two capacitors, both contains the reset noise $P_{kTC,FD}$, which is a correlated noise source. Adding them together results in a four times noise power $4P_{kTC,FD}$. Thus, the noise power on C2 after charge redistribution is:

$$v_{C2\_2} = \sqrt{4P_{kTC,FD} + P_{kTC,C1} + P_{kTC,C2}}/2 \tag{3-25}$$

As we mentioned before, after charge redistribution, there are two modes to readout the video voltage level. Mode 1 is keeping switch S2 on when reading $V_{SIGNAL2}$ and mode2 is switching off S2 before the end of SEL pulse, thus, a complete switching cycle from S2 is foresee and an additional kTC noise is added.

In operation of mode 1, the video signal is subtracted from the reset value in the CDS operation. Since the reset noise on the FD capacitor is correlated, it can be cancelled completely. What's more, the kTC noise $P_{kTC,C2}$ in the two samples is also correlated. However, the reset level contains a unity noise power while the video signal level just contains one-quarter of the noise power. As a result, there still will be one-quarter of the noise power remaining after subtracting both. This calculation is shown in the Eq. (3-26) below.

$$\begin{aligned} P_{mode1} &= \overline{v_{C2\_2}^2} - \overline{v_{C2}^2} \\ &= P_{kTC,FD} + P_{kTC,C2} + P_{kTC,FD} + \frac{1}{4}P_{kTC,C1} + \frac{1}{4}P_{kTC,C2} \\ &\quad - 2\Big(\sqrt{P_{kTC,FD}}\Big)^2 - 2\left(\sqrt{\frac{1}{4}P_{kTC,C2}}\sqrt{P_{kTC,C2}}\right) \\ &= \frac{1}{4}P_{kTC,C1} + \frac{1}{4}P_{kTC,C2} \end{aligned} \tag{3-26}$$

For the operation of mode 2, as the switch S2 is switched off before the RS pulse is completed, an additional kTC noise generated from transistor S2 on C2 needs to be considered. However, this kTC noise $P_{kTC,C'2}$ is noncorrelated with $P_{kTC,C2}$. So the noise power of final video signal readout is:

$$v_{C'2\_2} = \sqrt{4P_{kTC_{FD}} + P_{kTC,C1} + P_{kTC,C2} + 4P_{kTC,C'2}}/2 \tag{3-27}$$

Similar with mode1, the noise power remaining after CDS is calculated as:

$$\begin{aligned} P_{mode2} &= \overline{v_{C'2\_2}^2} - \overline{v_{C2}^2} \\ &= P_{kTC,FD} + P_{kTC,C2} + P_{kTC,FD} + \frac{1}{4}P_{kTC,C1} + \frac{1}{4}P_{kTC,C2} + P_{kTC,C'2} \\ &\quad - 2\Big(\sqrt{P_{kTC,FD}}\Big)^2 - 2\left(\sqrt{\frac{1}{4}P_{kTC,C2}}\sqrt{P_{kTC,C2}}\right) \\ &= \frac{1}{4}P_{kTC,C1} + \frac{1}{4}P_{kTC,C2} + P_{kTC,C'2} \end{aligned} \tag{3-28}$$

As $C1 = C2 = C$ which we explained before, the noise power of $P_{kTC,C1}$, $P_{kTC,C2}$ and $P_{kTC,C'2}$ is actually the same:

$$P_{kTC,C1} = P_{kTC,C2} = P_{kTC,C'2} = \frac{kT}{C} \tag{3-29}$$

Thus, $P_{mode1} = 0.5kT/C$ and $P_{mode2} = 1.5kT/C$.

From the above analysis, one can see that the final readout noise level is completely determined by the capacitors C1 and C2. The reset noise generated from the FD node reset is totally eliminated.

What's more, when we calculate this kTC noise referred to the FD node, due to the charge redistribution between C1 and C2, the kTC noise also attenuated by half. Therefore, the final result of two modes are:

$$P_{mode1\_final} = \frac{kT}{C} \tag{3-30}$$

$$P_{mode2\_final} = 3\frac{kT}{C} \tag{3-31}$$

And their noise figures in number of electrons referred to the FD node are:

$$n_{mode1} = \frac{kT}{C \times CG} \tag{3-32}$$

$$n_{mode2} = 3\frac{kT}{C \times CG} \tag{3-33}$$

Figure 3-6 shows the reset and kTC noise in number of electrons with respect to the in-pixel capacitors. Here, we use $CG = 103.2\mu\text{V/e}^-$, which is estimated in Section 3.3.2.

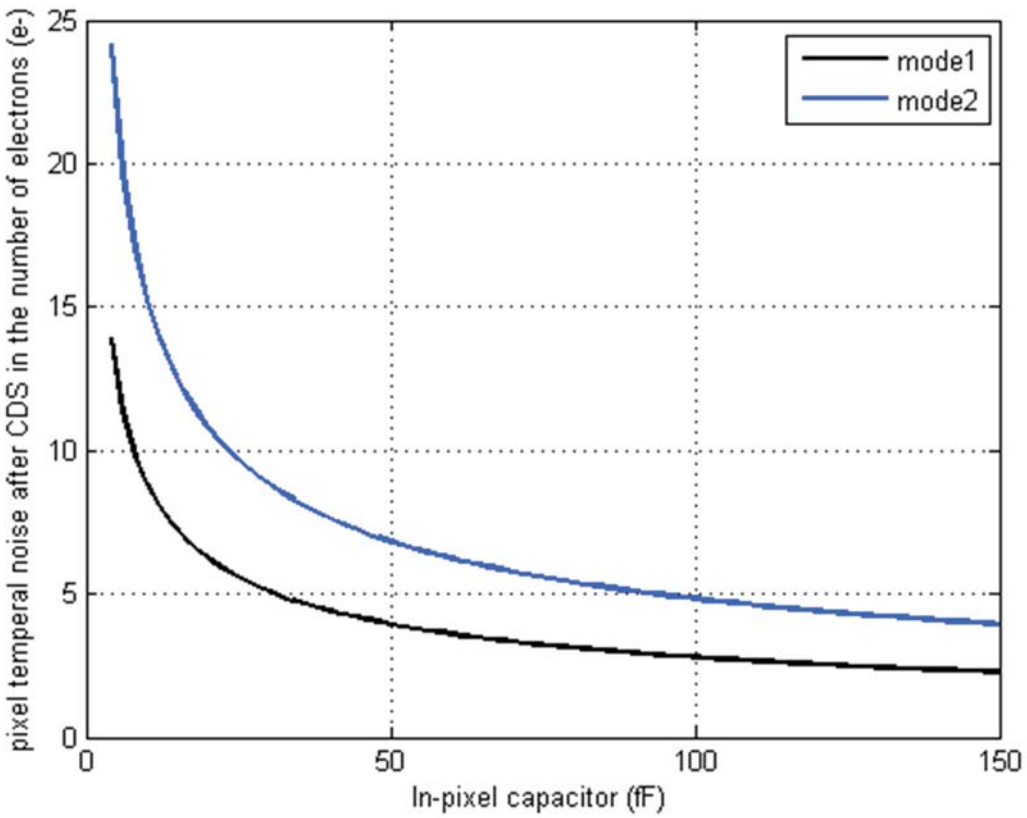

Figure 3-6: Pixel reset and kTC noise with respect to the in-pixel capacitors

3-2-5 Flicker noise

Due to the lattice defects at the interface between the gate oxide and the silicon substrate in a MOS transistor, many "dangling" bonds appear, giving rise to extra energy states. This imperfection of $Si - SiO_2$ channel introduces flicker noise in the drain current.

Commonly, the flicker noise is modeled as a voltage source in series with the gate and approximately given by [38]:

$$S_n = \overline{v_n^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{3-34}$$

where K is a process-dependent constant, W and L are the width and length of the transistor, C_{ox} is the gate capacitance, f is the frequency. For simplicity, Eq. (3-34) is denoted by

$$S_n = \frac{N_f}{f} \tag{3-35}$$

It should be noted that this model is just a very simple estimation of the flicker noise.

For this 8T global shutter pixel, the flicker noise mainly appears from the two source followers SF1 and SF2. Their noise power spectral density referred to the input is given by [40]:

$$S_{n,sf1,1/f} = \overline{v_{n,sf1,1/f}^2} = \left\{ N_{f,sf1} + \left(\frac{g_{m,pc}}{g_{m,sf1}}\right)^2 N_{f,pc} \right\} \frac{1}{f} \tag{3-36}$$

$$S_{n,sf2,1/f} = \overline{v_{n,sf2,1/f}^2} = \left\{ N_{f,sf2} + \left(\frac{g_{m,col\_pc}}{g_{m,sf2}}\right)^2 N_{f,col\_pc} \right\} \frac{1}{f} \tag{3-37}$$

where $g_{m,sf1}$, $g_{m,sf2}$, $g_{m,pc}$ and g_{m,col_pc} are the transconductance of source follower SF1, SF2 and bias current source load PC and column load COL_PC (I1 or I2), $N_{f,sf1}$, $N_{f,sf2}$, $N_{f,pc}$ and N_{f,col_pc} are flicker noise parameter of SF1, SF2, PC and COL_PC.

From Figure 3-7, one can clearly see that the flicker noise is dominant at low frequency, and drops below the thermal noise at high frequencies, which implying that the major noise contribution takes place at a frequency that is normally lower than the signal frequency. Thus, if we sample flicker noise twice in a short time, the noise will be highly correlated within a typical sampling interval time. As a consequence, if the sampling interval time is short enough, the flicker noise of the two samplings are nearly the same. Thus, CDS has a positive effect on the cancellation of flicker noise.

In the previous section, we have seen that CDS operation eliminate the correlated noise completely. What's more, if we look at the CDS operation in the frequency domain, its transfer function is given by [41].

$$|H_{CDS}(f)| = |2\sin \pi f T| \tag{3-38}$$

where $T = 1/f$ is the sampling interval between the time of reset signal sampling and video signal sampling.

Figure 3-8 shows the transfer function $H_{CDS}(f)$, where we can identify the low-frequency cutoff characteristic of the CDS system and find that the CDS system acts as a high-pass filter until $f = f_1$, $f = f_2$ and $f = f_3$, and oscillates after that frequency. The oscillation of the CDS system at a high frequency can be ignored, since the primary role of the CDS system is the noise reduction in low frequency region. Moreover, the effect of the CDS system also shows that the flicker noise is attenuated by a factor that depends on the sampling interval time, i.e. shorter sampling interval time T gives larger flicker noise reduction.

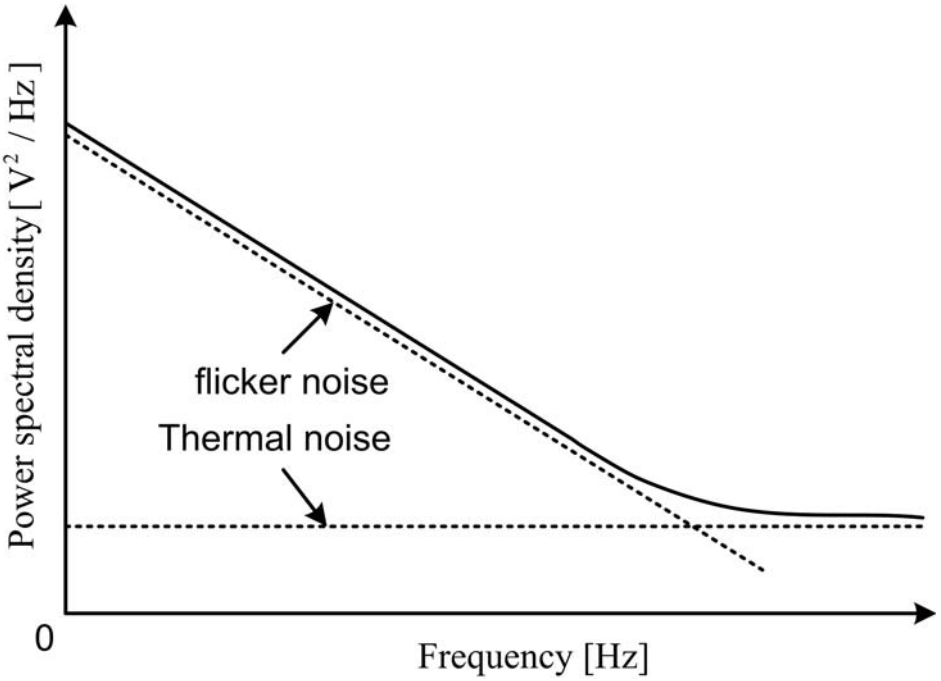

Figure 3-7: Thermal noise and flicker noise spectrum

Yet note that notwithstanding eliminating kTC and reset noise as well as suppressing flicker noise, the CDS system increases the white noise by a factor of $\sqrt{2}$ due to the two samples of the CDS system and its high pass filter characteristic [40]. In order to compensate the increase of white noise, we need to sample the voltage fast enough, so as to reduce the kTC noise and flicker noise effectively.

In this project, the interval time between sampling V_{RESET} and V_{SIGNAL} is $T = 2.5\mu$s, which is at the freqency of $f_0 = 400$kHz. The CDS system transfer function shows in Figure 3-9.

In order to estimate the residue flicker noise of two source followers after CDS operation, it is indispensable to do the noise calculation with the software of Cadence, EZwave and Matlab.

Set the calculation of source follower SF1 as an example. First we get the original output referred noise voltage level and noise Power Spectral Density (PSD) at frequency domain of SF1 from noise simulation. The simulated output referred noise is found to around $v_{n,sf1} = 376.5\mu\text{V}/\sqrt{\text{Hz}}$ and the noise PSD is shown as red line in Figure 3-10. Since both the PSD and CDS transfer function at the frequency domain, in order to find the residue noise PSD of SF1 $S_{n,sf1,afterCDS}$, we can multiply them directly, that is:

$$S_{n,sf1,afterCDS} = S_{n,sf1}(f)H_{CDS}(f) \tag{3-39}$$

where $S_{n,sf1}(f)$ is the SF1 noise PSD and $H_{CDS}(f)$ is the CDS transfer function at $f = 400$kHz. The result of Eq. (3-39) is shown as blue line in Figure 3-10.

From the AC simulation we get that the bandwidth $f_{-3dB,SF1}$ of SF1, that is around 1.85MHz.

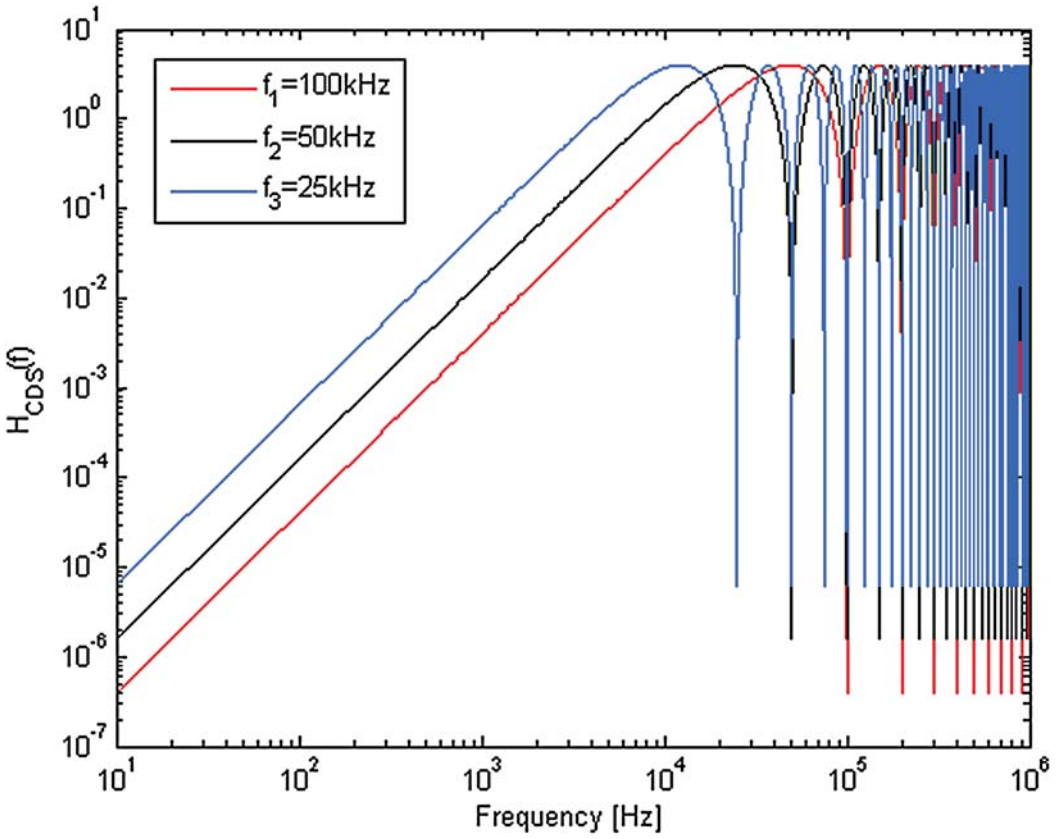

Figure 3-8: Transfer function of CDS system with f_1=100kHz, f_2=50kHz and f_3=25kHz

Then we get the noise bandwidth $f_{noise,-3dB,SF1}$ is:

$$f_{noise,-3dB,SF1} = \frac{\pi}{2} f_{-3dB,SF1} = 2.9\text{MHz} \tag{3-40}$$

Finally the residual temporal noise of SF1 is obtained using:

$$v_{n,sf1,afterCDS} = \sqrt{\int_1^{2.9\text{MHz}} S_{n,sf1,afterCDS}} = 213\mu\text{V}/\sqrt{\text{Hz}} \tag{3-41}$$

The same method used for SF2, we get the original noise level is $v_{n,sf2} = 378\mu\text{V}/\sqrt{\text{Hz}}$ and the residual noise level is $v_{n,sf2,afterCDS} = 215\mu\text{V}/\sqrt{\text{Hz}}$

Thus, we can get the input referred total source follower noise in voltage and in number of electrons as shown in Eq. (3-42) under the assumption that the gain of SF1 and SF2 is unity.

$$v_{sf} = \sqrt{v_{n,sf1,afterCDS}^2 + (2v_{n,sf2,afterCDS})^2} = 476\mu\text{V}/\sqrt{\text{Hz}} \tag{3-42}$$

$$n_{sf} = v_{sf}/CG = 4.629\text{e}^- \tag{3-43}$$

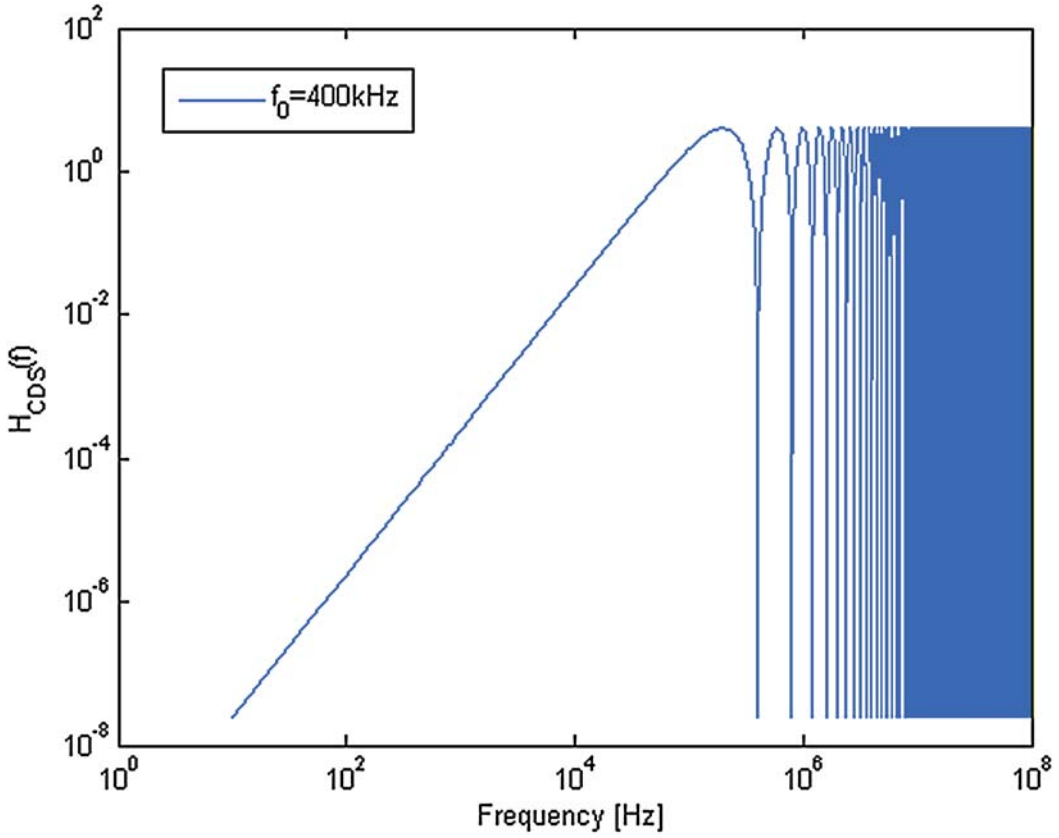

Figure 3-9: Transfer function of CDS system with f_0=400kHz

3-2-6 Noise floor (Input referred noise)

The noise floor can be seen as the limitation of the image quality in the dark region. In this 8T pixel, the noise floor in number of electrons is expressed by the following formula:

$$n_{noise} = \frac{1}{qCG}\sqrt{\left(\frac{v_{read}}{A_{col}}\right)^2 + \overline{v_{pixel}^2}} \tag{3-44}$$

where q is the elementary charge, v_{read} is the noise generated from the column chain, A_{col} is the gain of the column amplifier, v_{pixel} is the noise voltage generated from a pixel after CDS including shot noise, thermal noise and any residual kTC noise and flicker noise. From Eq. (3-44)), one can learn that both contributions of v_{pixel} and v_{read} are decreased by increasing CG and the increase of A_{col} is not able to reduce v_{pixel}. It means that increasing conversion gain (CG) is only way to reduce the input referred noise n_{noise}.

Here, we can estimate the pixel residue noise after CDS. The expression of pixel noise is given

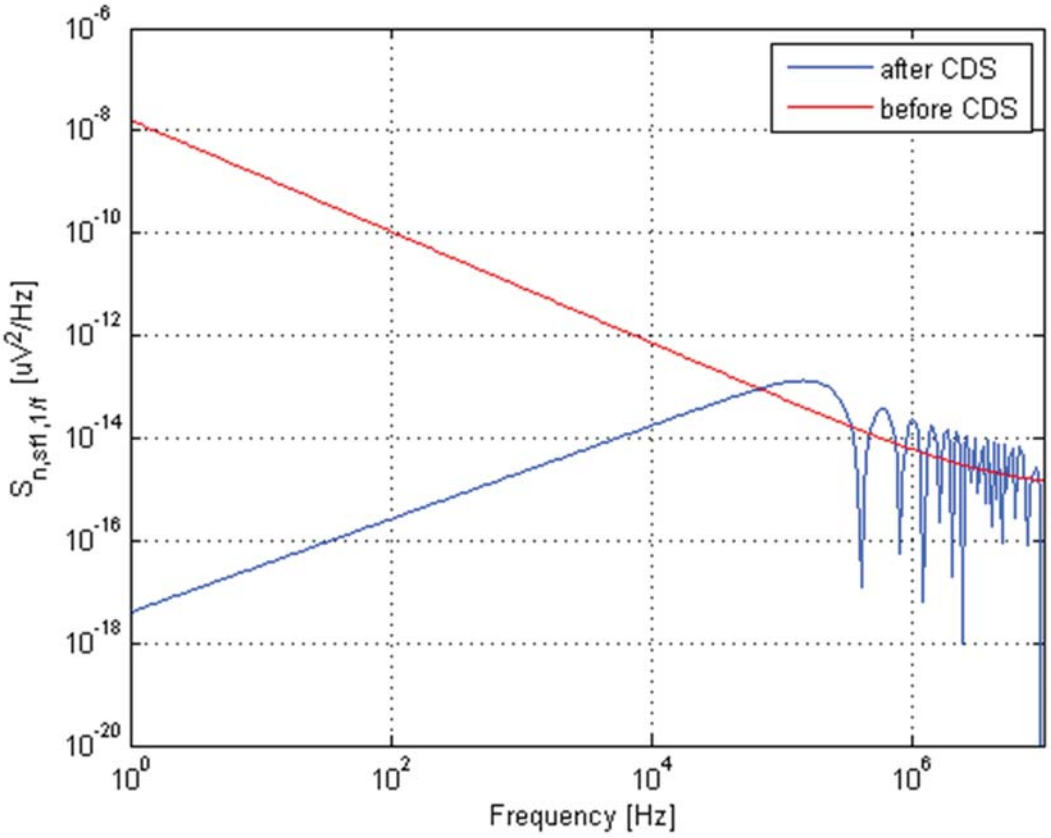

Figure 3-10: Source follower noise spectrum before and after CDS operation

by:

$$\overline{v_{pixel,mode1}^2} = 2\overline{v_{n,FD,shot}^2} + 2(\overline{v_{th,sf1}^2} + \overline{v_{th,sf2}^2}) + \overline{v_{n,sf1,afterCDS}^2} + 2\overline{v_{n,sf2,afterCDS}^2} + \frac{kT}{C}$$
$$\approx \frac{kT}{C} + v_{sf} \tag{3-45}$$

$$\overline{v_{pixel,mode2}^2} = 2\overline{v_{n,FD,shot}^2} + 2(\overline{v_{th,sf1}^2} + \overline{v_{th,sf2}^2}) + \overline{v_{n,sf1,afterCDS}^2} + 2\overline{v_{n,sf2,afterCDS}^2} + 3\frac{kT}{C}$$
$$\approx 3\frac{kT}{C} + v_{sf} \tag{3-46}$$

Figure 3-11 shows the kTC noise in number of electrons with respect to the in-pixel capacitance (calculated from Eq. (3-32) and Eq. (3-33)) and the flicker noise after CDS from source followers (calculated from Eq. (3-43)). From this figure we can see that in mode1, if the in-pixel capacitance C1 and C2 smaller than 37.3fF and in mode2 smaller than 110.5fF, the

kTC noise generated on S1, C1 and S2, C2 is larger than the source follower SF1 and SF2 noise, and vice versa. Figure 3.8 plots the estimated total noise of the pixel, we can see that from the point of 80fF, increasing in-pixel the capacitors does not make much difference in the calculation of the total noise due to the source follower noise become dominated.

3-3 Pixel design and layout consideration

3-3-1 Pinned-photodiode, transfer gate and FD node

Figure 3-13 shows the cross section of a pinned photodiode, transfer gate TG and floating diffusion node. The diode is built in a lowly doped p-epitaxial layer and this epitaxial layer is grown on bulk material which is highly doped. The photodiode is formed by a deep n-type implant and the pinned surface is constructed by a heavily doped p layer. As shown in Figure 3-14, this photo-sensing element consists of two p-n junctions: the n-p-sub junction in the silicon bulk and the n-p+ junction close to the surface. This isolates the depletion region of the photodiode from the surface and hence reduces the surface generation dark current. The doping levels are chosen such that the photodiode is fully depleted. For the photodiode pinned at a fixed voltage V_{pin}, the potential between deep n and p-epi is $V_{pin} + V_{bi}$, V_{bi} is the built-in voltage of the junction.

For the photodiode layout, the fill factor is the first point that needs to be thought of. The additional area of the other seven transistors and two in-pixel capacitors aggravate the tradeoff between the fill factor and other components performance. What's more, it shall be noted that as the pixel size becomes smaller, the total surface generated dark current is more affected by the perimeter component than the area generated one. The perimeter component of the dark current is mainly generated from the interface between the sidewall of the Shallow Trench Isolation (STI) and photodiode. Thus, to decrease the dark current, it is indispensable to separate the depletion region from STI effectively. In the layout of the photodiode, we enclose the n implant by active layer and no-well layer, so as to protect STI by p well. This method prevents the STI region from directly abutting the depletion region. Thus, the top and side-wall of the STI are all well pinned by the heavily doped p layer and p well, the surface generated current can be greatly reduced.

Except for the considerations mentioned above, another issue needs to be thought of, is the metal routings around the photodiode. If the routings are placed like Figure 3-15(a), when a beam of light with an angle incident to the photodiode, the metal layer will obstruct the incident light and create a shadow on the photodiode, thus decrease QE. Compared to (a), the layout of metal in (b) allowed the beam of light with larger incidence angle to be absorbed by the photodiode and prevent the shadow problem to some extent. This method contributes to the enhancement of QE.

The transfer gate TG controls the charge transfer between photodiode and FD node. For the layout of transfer gate TG, there are three important issues that are of concern:

- TG-induced dark current: Apart from the photodiode, the presence of the transfer gate also often introduces dark current (dependent on technology). Because photodiode depletion region towards TG touches the $Si - SiO_2$ interface under the TG gate, and the

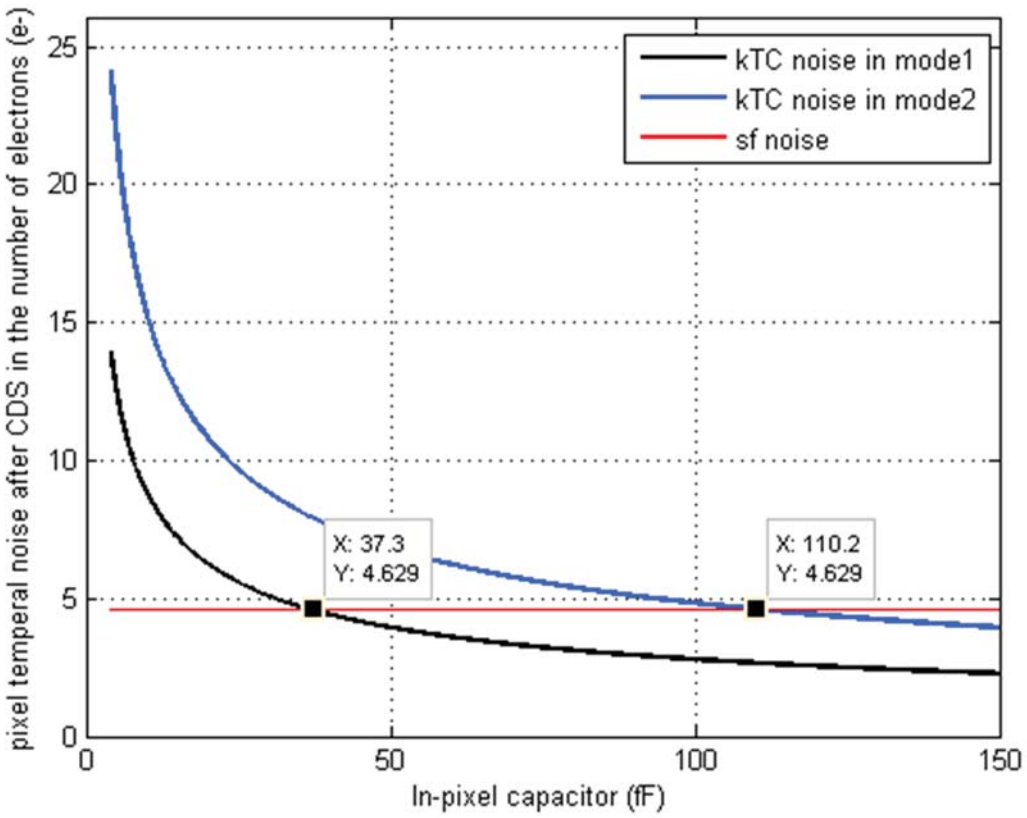

Figure 3-11: kTC noise vs. source follower noise

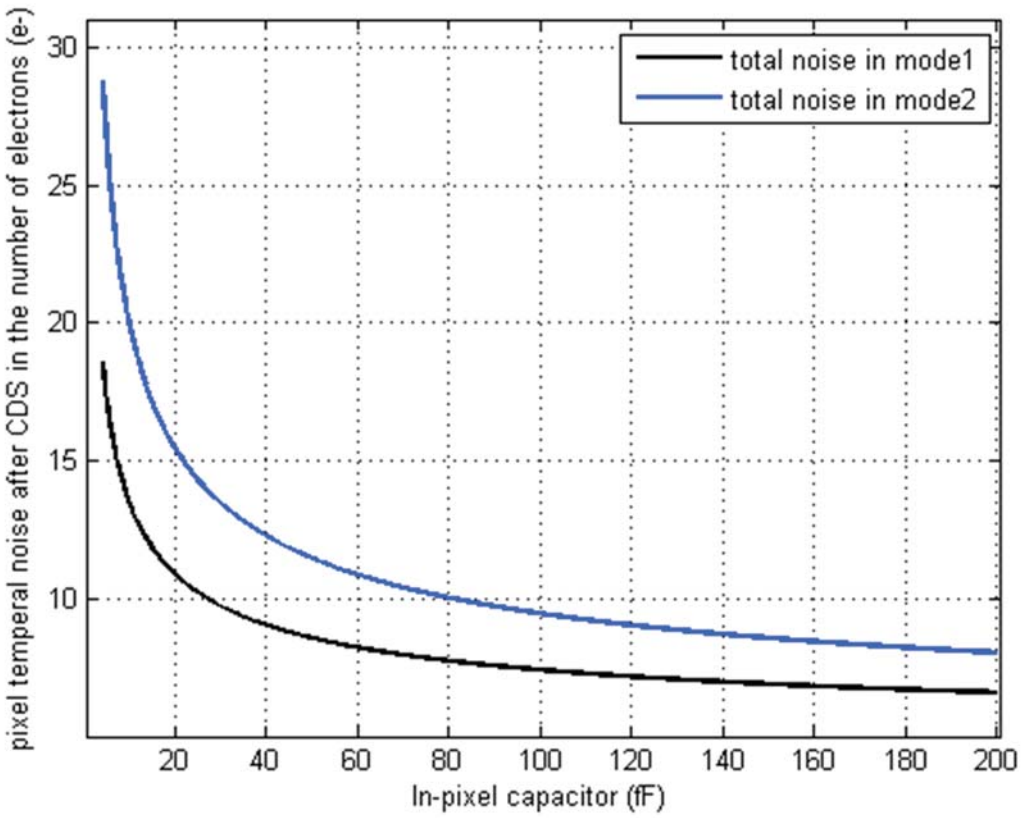

Figure 3-12: Pixel total noise

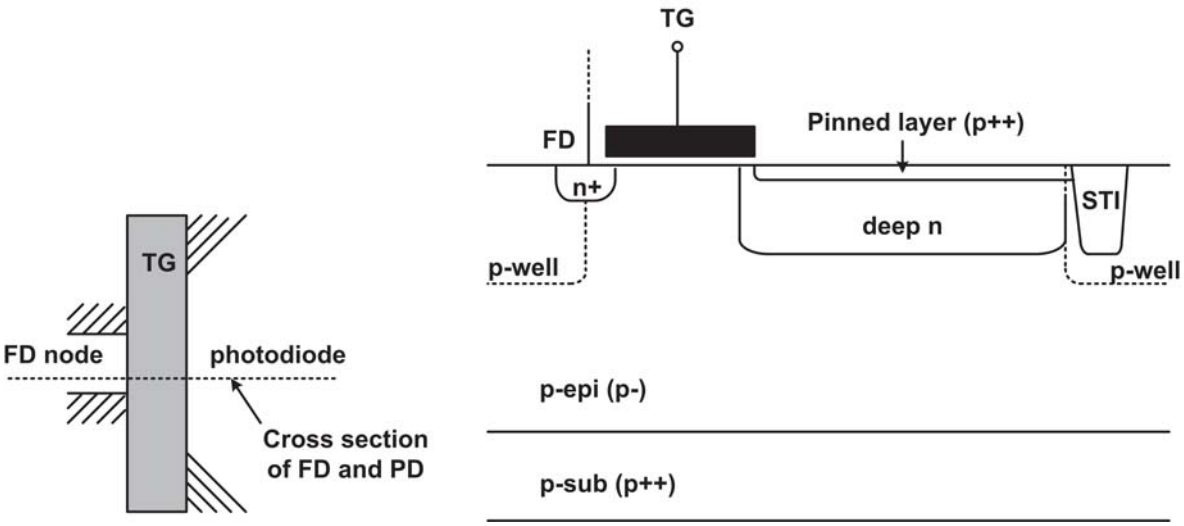

Figure 3-13: Layout and cross-section of the pinned photodiode, charge transfer gate and FD region

electric field at the overlap between the TG gate and pinned layer make this problem more severe. Thus, we usually add an extra p-type doping layer underneath the TG gate. On one hand, this p-type doping layer fills the interface defects with holes when the TG is switched off, on the other hand, because the pixel is directly built on a lowly doped p-epi layer, the threshold voltage of transfer gate is quite low, this extended p layer will also help to increase and adjust the V_{TH} .

- Charge transfer: Incomplete charge transfer from the photodiode to the FD node lead to excess noise, image lag and nonlinearity. For example, if there is an offset between the p+ surface and deep n layer in the photodiode, a potential pocket or a potential barrier will be exist at the cross section between the photodiode and the transfer gate. Both a potential barrier and a pocket will lead to image lag [42]. Apart from the photodiode, the location of the p-well in relation to the FD node region and other parameters also determine the potential barrier between the photodiode and the FD node. Therefore, it is dispensable to optimize the structure of the region between the photodiode edge and the transfer gate as well as the FD node on the layout. Besides, the length of the transfer gate should also be optimized in order for a better charge transfer performance.

- Signal coupling: From the timing diagram of a 8T global shutter pixel, one can learn that this pixel can be operated in a pipeline global shutter mode, thus, the global control signal coupling during FOT should be paid some special care.

From previous discussions, the goal of this pixel design is to have the FD node voltage swing limit the pixel full well capacity. What's more, a smaller FD capacitance means a larger conversion gain and a smaller readout noise. In practice, the FD capacitance consists of several overlap capacitances and parasitic capacitance as shown in Figure 3-16. Thus, in order

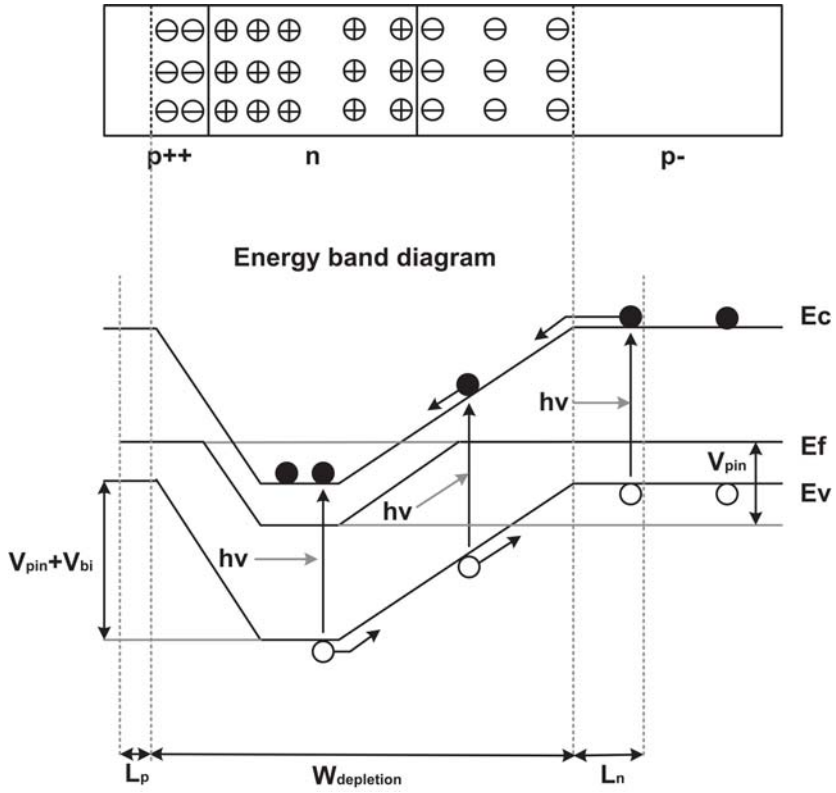

Figure 3-14: Band diagram of pinned photodiode

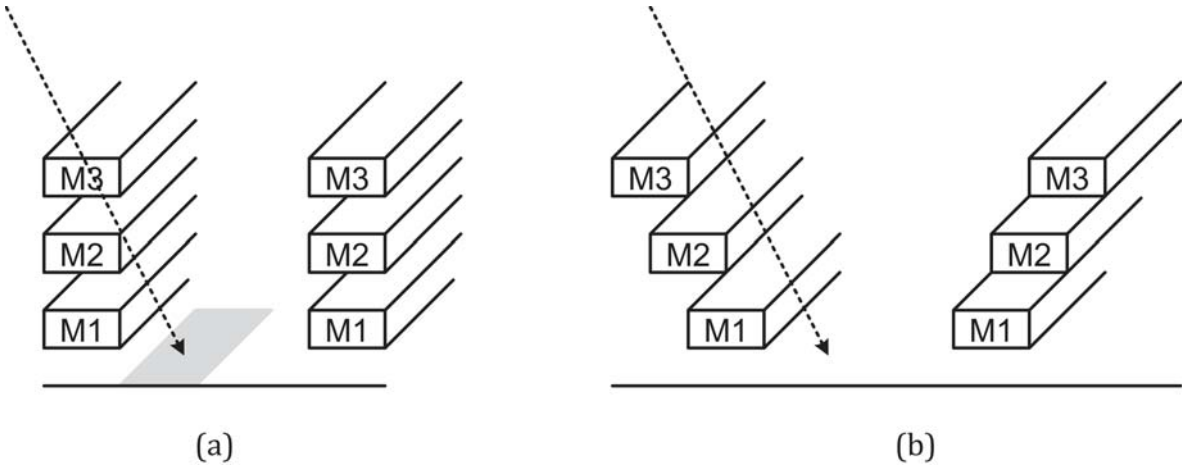

Figure 3-15: Incident light with an angle for different routing configuration

to reduce the FD capacitance, a careful pixel layout and a proper choice of the transistor size will be essential. After making the layout, the FD capacitance and the conversion gain can be estimated from the parameters of SPICE Models and the extracted parasitic capacitors coupled with the FD node, as shown in Table 3-1.

Let's consider more about the voltage swing at FD node. In order to let the bias transistor PC work at its saturation region, the floating diffusion node potential should be at least one threshold voltage higher than the minimum bias transistor PC source-drain voltage, which is 100mV in theory. What's more, the lowest voltage on the FD node also be limited by V_{pin}, which is often around 1V. Thus, here, we assume the minimum voltage at FD node is 1V. For pixel supply voltage at 3V, the FD node voltage swing is between 1V to 3V.

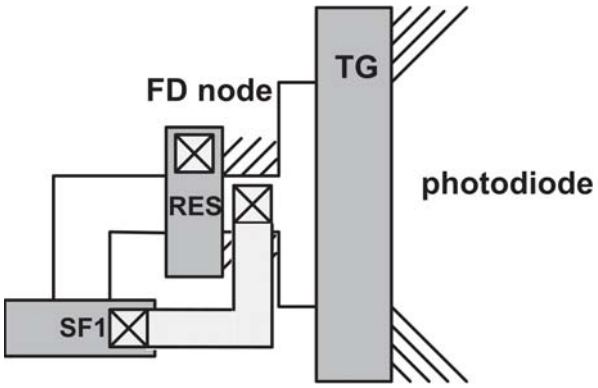

Figure 3-16: Layout of FD region

Table 3-1: FD capacity

Parameter	Value
FD bottom-plate junction capacitance	0.369fF
FD sidewall junction capacitance	0.337fF
TG gate-drain overlap capacitance	0.254fF
RST gate-drain overlap capacitance	0.0538fF
SF gate capacitance	0.260fF
Parasitic capacitance	0.276fF
Sum FD capacitance	1.55fF
CG	103.2 μV/e$^-$

3-3-2 Pixel circuit

Apart from the photodiode, the transfer gate and the floating diffusion node, the pixel still has 7 other transistors and 2 capacitors. Here for simplicity, we just call them the pixel circuit

for simplicity. The pixel circuit of an 8T pixel also plays an important role in operating the pixel in pipeline global shutter mode and processing the readout signal with CDS. However, the pixel circuit takes a relatively large silicon area and will affects the QE of the pixel. Thus, the thumb of rule of the pixel circuit design is to select the transistor size as small as possible. But, there are still many important considerations.

Reset transistor: Transistor RST periodically resets the floating diffusion node to a particular voltage. The reset transistor is often an nMOS, because the use of a pMOS would require a separate n-well inside the pixel and will negatively affect the QE, though there will be no threshold voltage drop problem occuring when a pMOS is used as reset transistor.

As the reset transistor is not an ideal switch, we need to consider the effect of channel charge injection on it. This channel charge injection mechanism will be explained in details in Chapter 4, here, we just analyse its influence to the reset transistor. When RST turns off, some portion of the channel charges will be relocated to the FD region and reduce the voltage swing. What's more, because the RST gate is very small, the Short-Channel Effect (SCE) of the MOS transistor, such as drain-induced barrier lowering effect and deep channel punch-through current [43], also needs significantly attention. This SCE forces a reduction in the threshold voltage and causes a substantially large leakage current.

Sample transistors and capacitors: Transistor S1 and S2 operate as switches in the pixel. Apart from considering the effect mentioned above, since the minimum size of the active layer contact is wider than the minimum transistor width. For the purpose of reducing the space occupied by S1 and S2, the widths of them are forced to be equal to the width of the active layer contact. Furthermore, increasing the width of sample transistors also decreases R_{on} and this principle is suitable for RST too.

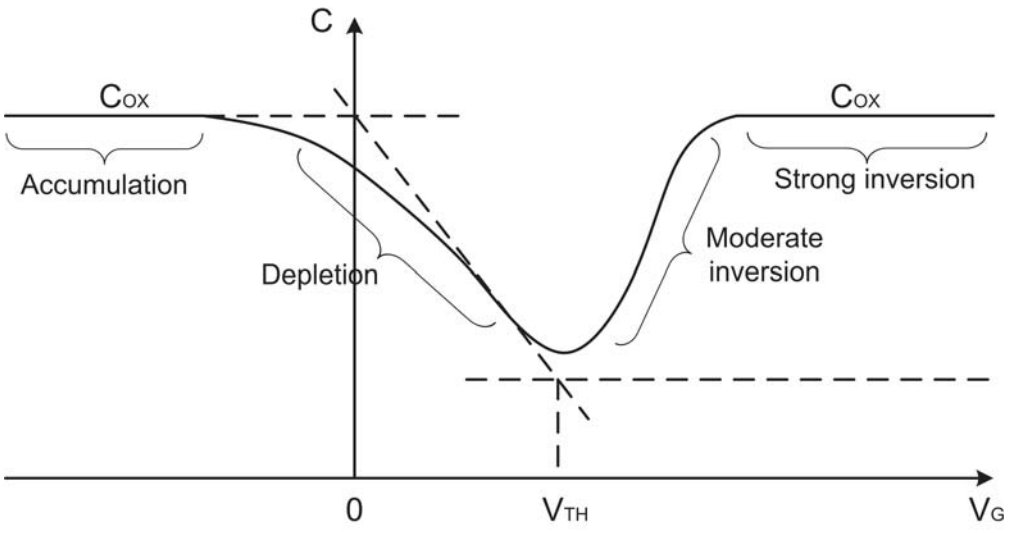

Figure 3-17: Ideal low-frequency capacitance versus gate voltage of an nMOS capacitor

Keeping the symmetry of the layout of this part is an important point to let the final capacitance of C1 and C2 become equal and reduce the influence of parasitic capacitors. The final

capacitance for C1 and C2 are 18fF, according to this value, we can get the estimated noise level is around 6.57e$^-$ for mode1 and 11.4e$^-$ for mode2.

Source follower and bias transistor: The source followers in the pixel serve two purposes: buffer the signal and amplify charges. As is state above, the input capacitance of the source follower SF1 adds up to the total FD capacitance and the area of the transistors in the pixel needs to trade with the fill factor. Thus, the size of the source follower should be minimized. What's more, the output swing together with the conversion gain and the output swing determine the saturation level. The readout speed also limits the frame rate of the CMOS imagers, thus, we still need some other consideration of the source follower from circuit characteristics level.

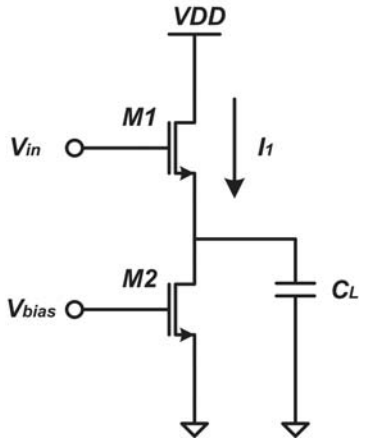

Figure 3-18: Source follower schematic

Figure 3-18 shows a source follower with a bias transistor which can represent the SF1 and SF2 in pixel. It is general, it is known that the gain of source follower is

$$A_v = \frac{g_{m1}}{g_{m1} + g_{mb1}} \tag{3-47}$$

where g_{m1} is the transconductance of M1 and g_{mb1} is body effect transconductance of M1. Usually, the value of A_v is around 0.8 to 0.9. What's more, the gain of the source follower will vary with the input voltage and this is another nonlinearity factor of the pixel.

To keep the bias transistor in saturation region, the minimum output voltage for this source follower should be:

$$V_{omin} = V_{bias} - V_{TH,M2} \tag{3-48}$$

where V_{bias} is the bias voltage of M2 and $V_{TH,M2}$ is the threshold voltage of M2. The maximum

output voltage occurs when reset level signal readout, that is:

$$\begin{aligned} V_{omax} &= V_{imax} - V_{GS,M1} \\ &= V_{imax} - V_{TH,M1} - \frac{2I_D}{g_{m1}} \\ &= V_{imax} - V_{TH,M1} - \sqrt{\frac{2L_{M1}I_{bias}}{K_n W_{M1}}} \end{aligned} \tag{3-49}$$

where V_{imax} is the maximum input voltage of source follower, $V_{GS,M1}$ is the gate-source voltage of M1, $V_{TH,M1}$ is the threshold voltage of M1, I_D is the drain current, g_{m1} is the transconductance of M1, L_{M1} and W_{M1} are the length and width of M1, K_n is the intrinsic transconductance of M1, I_{bias} is the bias current. Thus, the output swing is given by:

$$\begin{aligned} V_{out} &= V_{omax} - V_{omin} \\ &= V_{imax} - V_{GS,M1} - V_{bias} + V_{TH,M2} \\ &= V_{imax} - V_{bias} + V_{TH,M2} - V_{TH,M1} - \sqrt{\frac{2L_{M1}I_{bias}}{K_n W_{M1}}} \end{aligned} \tag{3-50}$$

A relationship between the input amplitude V_{in} and the output slew rate dV_{out}/dt also can be defined. Neglecting the channel length modulation effects on M1 and M2, the slew rate at which the output voltage V_{out} changes is

$$\frac{dV_{out}}{dt} = \left\{ \frac{1}{2} \frac{K_n W_{M1}}{L_{M1}} (V_{in} - V_{out} - V_{TH,M1})^2 - I_{bias} \right\} / C_L \tag{3-51}$$

where C_L is the load capacitor.

From Eq. (3-51), one can find that when V_{in} is rising, a large voltage difference between V_{in} and V_{out} ensures a large current flow through M1 and thereby charging C_L. This allows the output voltage to track the input voltage rapidly. When V_{in} is falling, the M1 goes into the cut-off region. Thus the load capacitor is discharged just by I_{bias}. And the slew rate is limited to I_{bias}/C_L. A large bias current I_{bias} enable a high slew rate however, it leads to an output swing reduction and will be power hungry.

Return from the circuit of Figure 3-1

For SF1, the load capacitor C1 is 18fF which is relatively small, As shown in Eq. (3-48), in order to maximize the output swing, it is dispensable to decrease V_{bias} until it is near the transistor PC threshold voltage $V_{TH,pc}$. This value is usually around 0.7V to 0.75V.

For SF2, the load capacitor is the column bus C_{col} = 1.7pF. With the aim of discharging this large capacitor in a short period, we set two current sources as load. At the start of the sampling phase, the larger source I2 (Figure 3-1) is activated and discharges the column bus capacitor. After that, this large current source is switched off and the source follower SF2 operates with only the small current source I1 as load. Assume the large current I_2 is 20μA, we can get the discharging time as:

$$t_{dis} = \frac{C_{col}\Delta V_{out}}{I_2} = 68\text{ns} \tag{3-52}$$

where ΔV_{out} is the output swing of SF2

3-3-3 Pixel layout overview

Figure 3-19 shows an example of 3×3 pixel layout in the 110nm technology, 4-metal process. The RST line, RS line, S1and S2 line, PC line route horizontally. The TG Bus and Column Bus runs vertically. The power and ground line are routed in both horizontal and vertical direction to reduce the voltage drop across the whole array. In order to reduce the area consumption of the 8T pixel transistor and reduce the overlap capacitance, the drain and source of the transistors are merged together. Two in-pixel capacitors and the FD node are fully covered with metal to reduce the PLS. The pixel layout specifications are shown in Table 3-2

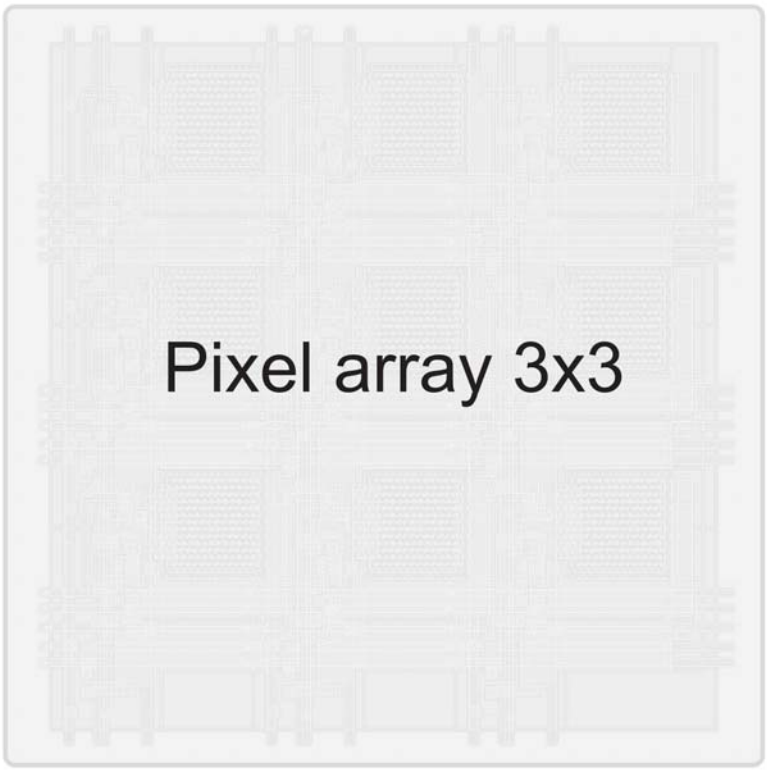

Figure 3-19: Layout of pixel

3-4 Extraction and simulation result

3-4-1 Simulation of source followers

In practice the pixel performance mainly depends on its device and process characteristics, yet we can still roughly evaluate some circuit level performance in Cadence. First, we separately

Table 3-2: Pixel layout specification

Specification	Value	Unit
Pixel pitch	4.8×4.8	μm^2
Photodiode size	2.722×2.611	μm^2
Fill factor	31	%
FD capacity	1.55	fF
In-pixel capacitor	18	fF
Conversion Gain	103.2	$\mu V/e^-$
Noise	Mode1: 6.57	e^-
	Mode2: 11.4	e^-

simulate the performance of Source followers 1 and Source follower 2 as shown in Figure 3-20. The bias current and simulated gain of two source followers which are used in this pixel are presented in Table 3-3. Accordingly, the estimated gain of the pixel circuit is

$$\begin{aligned} A_{pixel} &= A_{sf1} \times A_{sf2} \times A_{charge\_redistribution} \\ &= 0.92 \times 0.88 \times 0.5 \\ &= 0.4 \end{aligned} \tag{3-53}$$

where A_{sf1} and A_{sf2} are the gain of source follower SF1 and SF2, $A_{charge\_redistribution}$ is the attenuated factor of charge redistribution between C1 and C2. So the expected voltage swing is around 0.8V.

The transient responses of output voltage of two source followers and the output current at the output node of M and N are shown in Figure 3-21 and Figure 3-22. For source follower 2, a large bias current enhances the slew rate at falling edges, as we expected.

Table 3-3: Source followers specification

Specification	SF1	SF2	Unit
gain	0.92	0.88	
Bias current	0.53	small (I1): 1	μA
		large (I2): 20	μA
Input voltage	1 to 3	1 to 2	V
Settling time	rising: 139	rising: 655.6	ns
	falling: 148	falling: 181.4	ns

3-4-2 Simulation of single pixel

In the whole pixel circuit simulation, the FOT is chosen as 10μs. Since the accurate pixel transistor is not available, such time is just an empiric value. The FD node operation cannot be well modeled in Cadence, thus, we use a Piecewise Linear (PWL) voltage source to

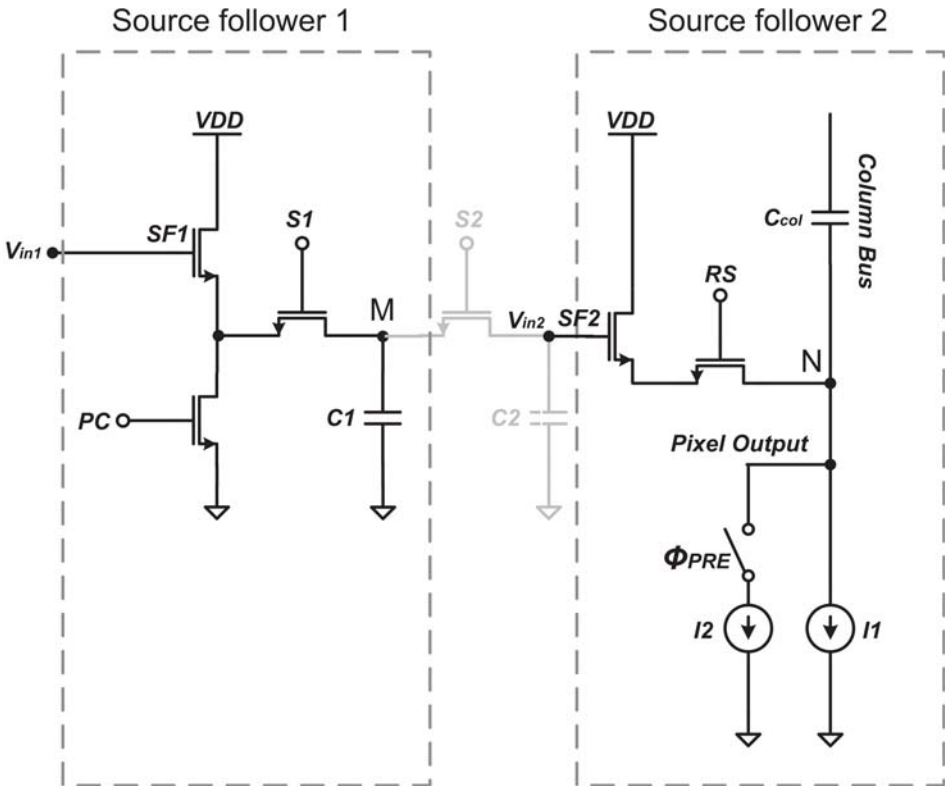

Figure 3-20: 8T pixel circuit

represent the voltage variation on the FD node. As the pinned photodiode and transfer gate operation is also not well modeled in this technology, the image lag characteristics as a function of transfer pulse width is not possible to simulate. In this simulation, it is assumed that the transfer pulse width of 2 μs is sufficient.

The comparison of pixel output for whole pixel circuit between the ideal capacitor and MOS capacitor output are shown in Figure 3-23. The x-axis is the input voltage ΔV_{SIG} (see Eq. (3-1)), and the y-axis is the output voltage ΔV_{SIG2} (see Eq. (3-2)). From this simulation result, one can see that when the ΔV_{SIG} becomes large, the linearity of the pixel circuit get worse. That is because the gate capacitor is voltage dependent which has been explained in Section 3.3.2. When the low video signal is read out, the voltage level at the gate of C1 and C2 will drop and force the capacitor into moderate inversion region, where the capacitance is linear with respect to the gate voltage. Thus, the real capacitance of C1 and C2 become smaller than 18fF. A workable solution to solve this problem is adjusting the threshold voltage of the source followers and the gate capacitors to a relatively low value via the process technology. However, the low Vt MOS model is not available by the technology. Hence, we model it as a DC voltage source in series with an nMOS source terminal. Assumed is to have a DC voltage source of 500mV, then we get the simulation result of the ideal and the real capacitor again. Figure 3-24 shows the comparison of pixel output between the ideal and MOS capacitor which

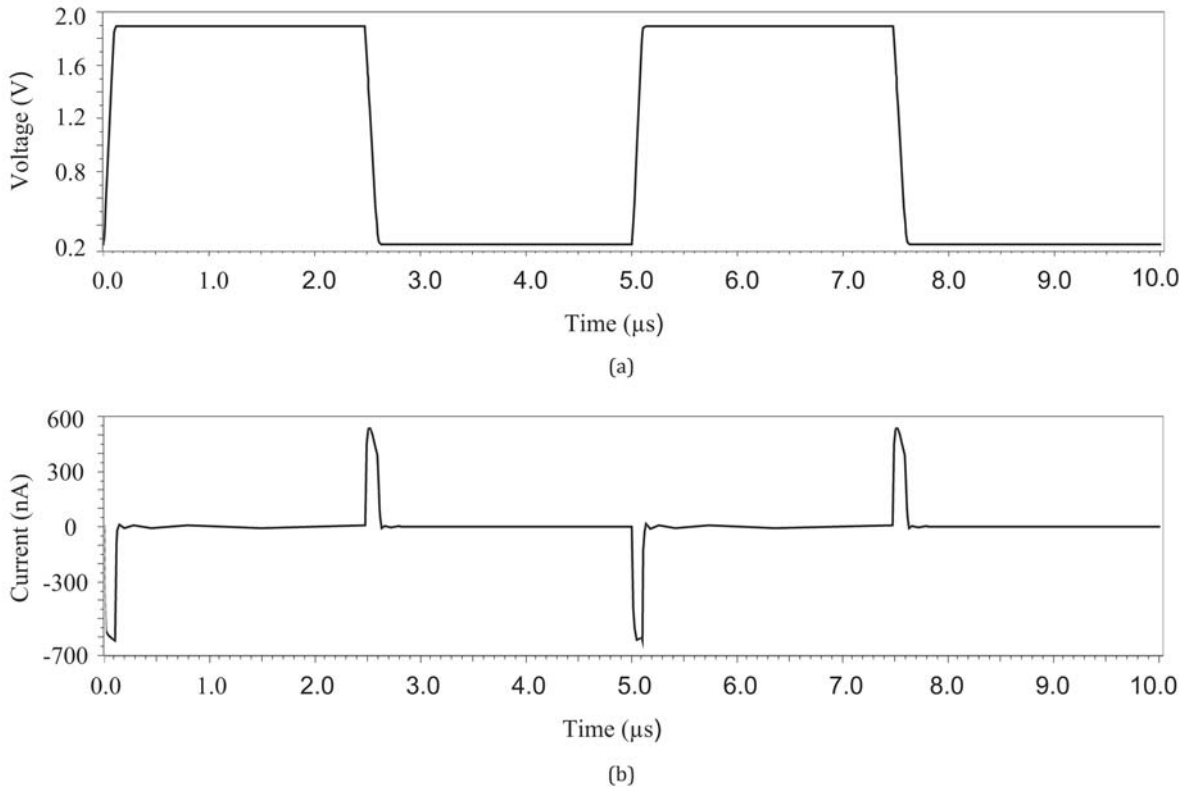

Figure 3-21: Transient responses of source follower 1 (a)output voltage (b)output current at node M

is after DC voltage adjustment. We can indicate that the when ΔV_{SIG} becomes large, the linearity of pixel circuit which use MOS capacitors is still almost the same as the one that use ideal capacitors.

As indicated before, there are two operation modes to readout the video signal from the pixel to the column. The outputs of the two modes are plotted in Figure 3-25. The offset of the output between mode1 and mode2 is 0.012V. This offset is originated from the asymmetric sampling access of mode1.

For the corner simulation, the typical (TT), slow (SS) and fast (FF) corners at 27 °C are simulated as well as the typical corner with different temperature (27 °C, 85 °C, −40 °C). The corner simulation result for the output is listed in Table 3-4.

3-4-3 Simulation of pixel array

For a large pixel array CMOS imager, one of the design challenges is to minimize the offset FPN that is introduced during the global shutter operation of the FOT. As explained previously, both the reset and video signal value are sampled to the in-pixel sampling capacitor during the FOT. During this operation, significant current will be drawn from the power

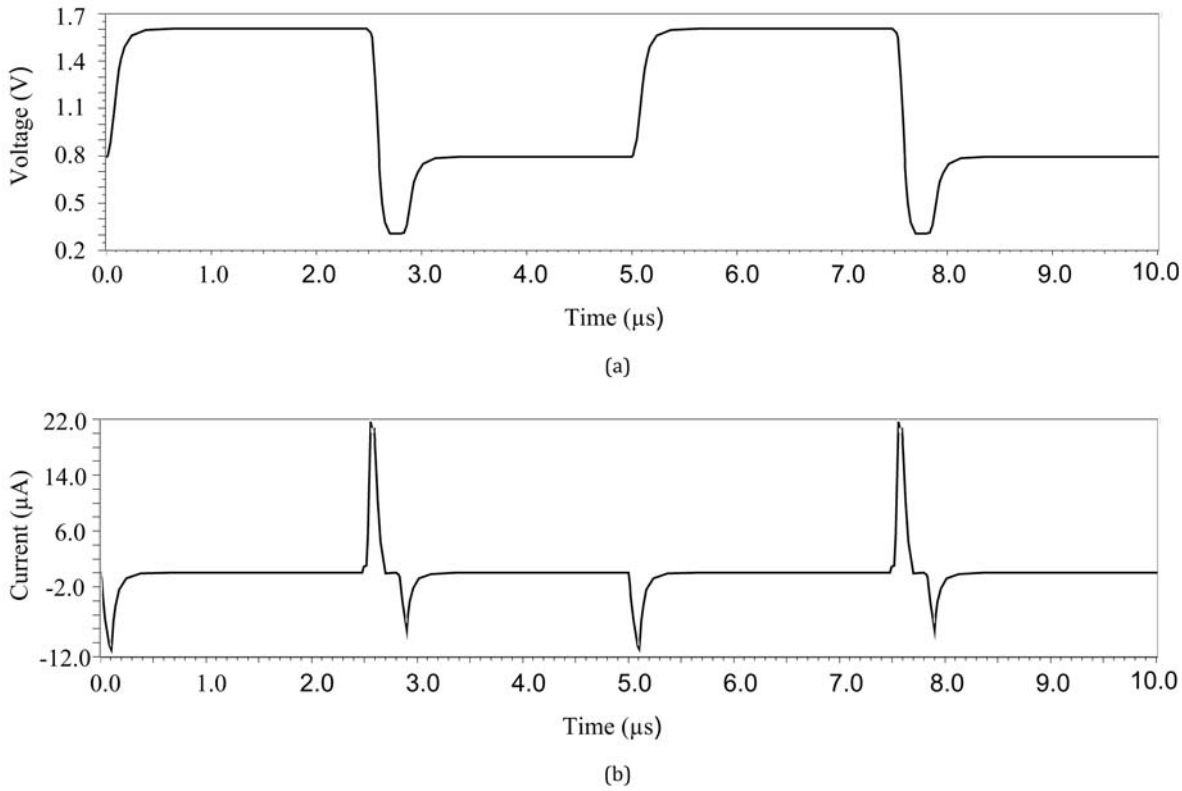

Figure 3-22: Transient responses of source follower 2 (a)output voltage (b) output current at node N

Table 3-4: Output swing of pixel for corner simulation

Corner	TT 27 °C	FF 27 °C	SS 27 °C	TT 85 °C	TT −40 °C
Output swing ΔV_{SIG2}	0.652V	0.656V	0.649V	0.657V	0.648V

supply which may introduces fluctuations or glitches of the power supply. Depending on the exact location of the pixel in the array, such glitches from the supply will introduce offset. Therefore, a complete pixel array is created for FPN simulation.

Before the offset FPN simulation, the line resistances and capacitances of each control signal, ground, power supply and column bus is first extracted from the layout, their values are shown in Table 3-5. RST, PC, TG, S2, VSS and VDD are global signal buses; RS and COL_OUT are line signal buses. During the FOT, S1 is a global signal and during the ROT, S1 is a line signal. According to these values, the lumped RC models of these wires are constructed, as shown in Figure 3-26. And the complete simulation block is shown in Figure 3-27.

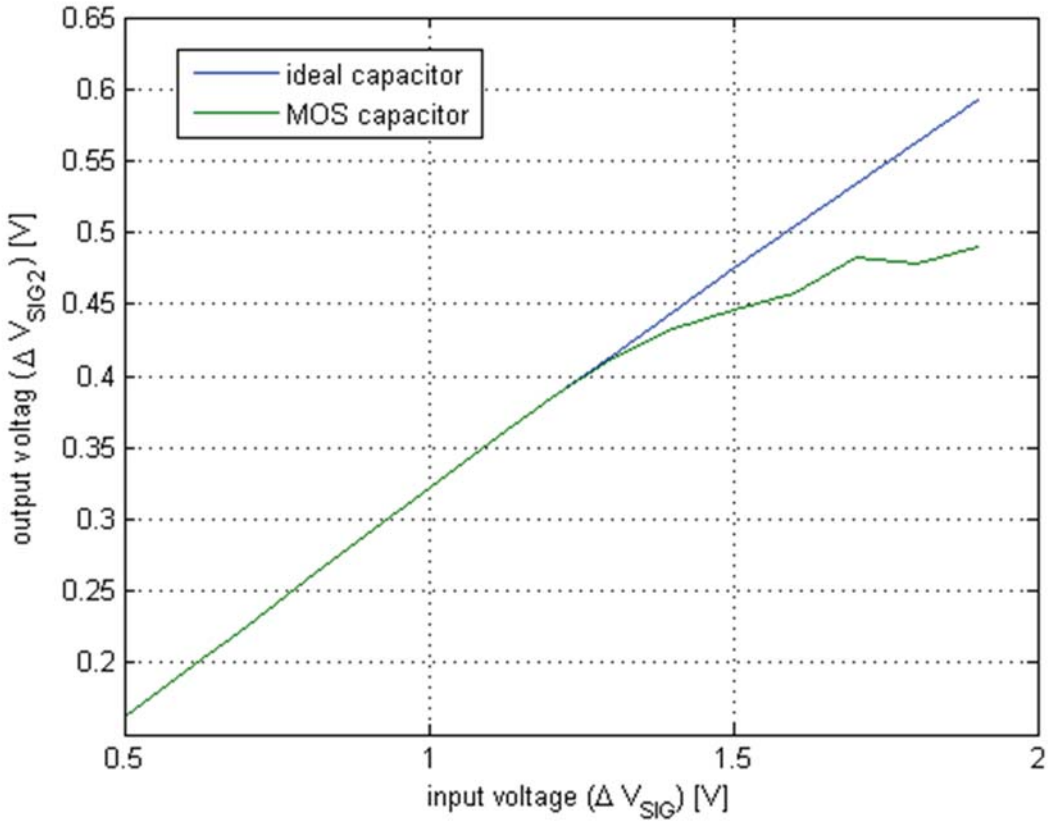

Figure 3-23: Output voltage comparison between ideal capacitor and MOS capacitor

Figure 3-28 shows a simulation result of the sampled signal on C1 and C2 of two pixels during the FOT. The two pixels are chosen as one at the edge of the array (with zero RC), and the other one at the other side edge of the array (with maximum RC for signal bus and power supply bus),which are shown as the red boxes in Figure 3-27. For simplicity, We call these two pixels as Left_pixel and Right_pixel in this simulation. The dash line and the solid line represent the voltage variance on C2 and C1. The magnify point A is chosen at the time after reset signal V_{RESET} and the magnify point B is chosen at the point after charge redistribution and video signal $V_{SIGNAL2}$ sampling. C2_left and C2_right shows the sampled voltage on C2 at Left_pixel and Right_pixel respectively, and C1_left and C1_right shows the sampled voltage on C1 also at left_pixel and right_pixel severally. With a grid power and ground connection configuration within each pixel and optimized row logic for the global signal, the offset between pixels to pixel at C2 is 0.0008V and the offset at C1 is 0.00001V.

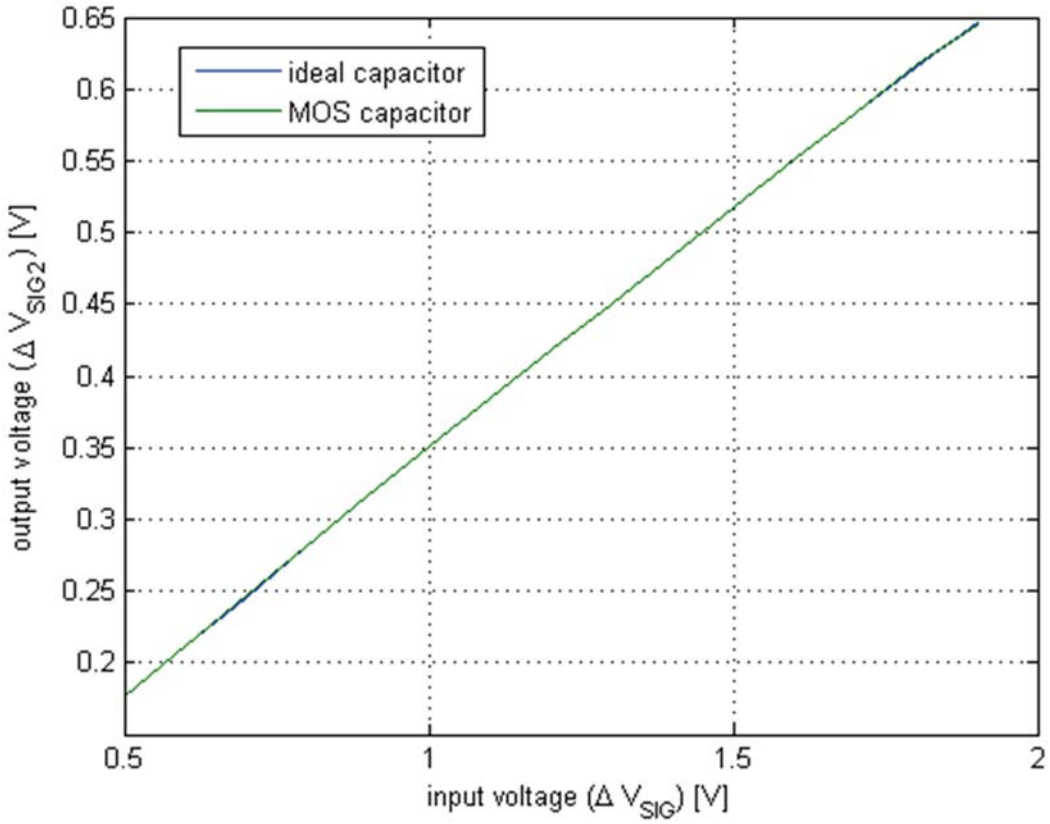

Figure 3-24: Output voltage comparison between ideal capacitor and MOS capacitor after Vt adjustment

3-5 Conclusion

In this chapter, an 8T global shutter pixel with $4.8\mu m$ pitch was developed. This architecture supports both the pipeline global shutter operation and the correlated double sampling. Based on the understanding of the pixel noise, a kTC noise model and a flicker noise model were constructed. According to these models, we estimated the pixel noise after CDS operation. Moreover, the pixel layout and operation voltage levels were carefully designed to optimize the pixel quantum efficiency, charge transfer and to decrease the dark current and noise level. Several simulation has been done to evaluate the pixel output swing, linearity and readout speed. By calculating the MOS device capacitors and extracting the pixel layout, we built the lumped RC model for the pixel array. With the help of these models, the row logic circuit was optimized and the offset, which is induced from the large RC delay, was reduced significantly.

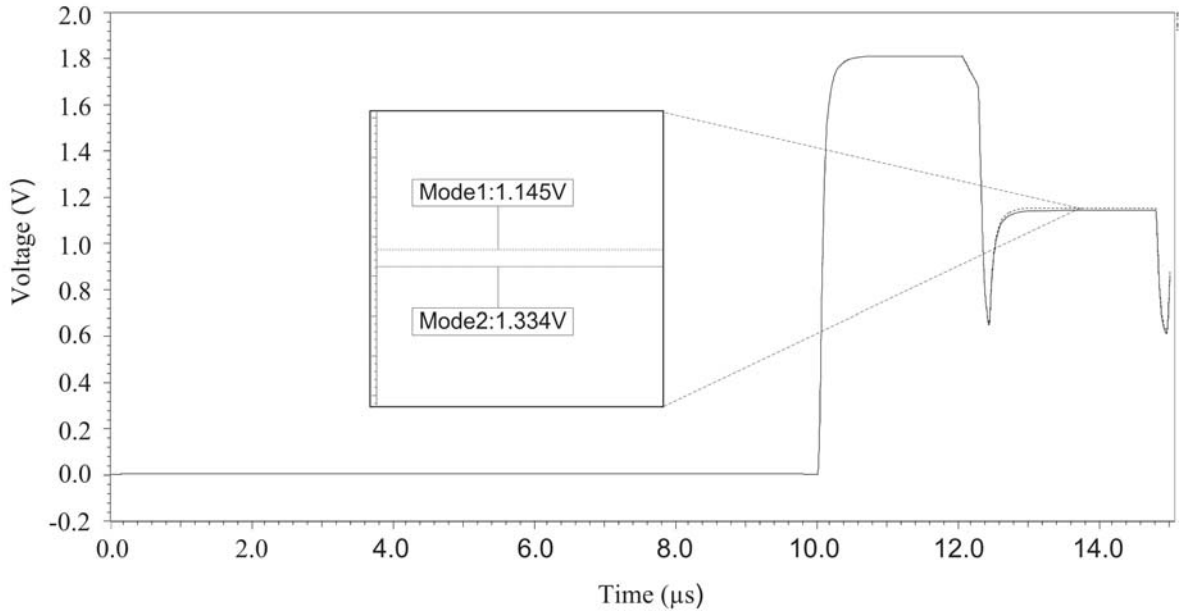

Figure 3-25: Output voltage comparison between Mode1 and Mode2

Table 3-5: Column and row bus estimated R and C

	MOS device cap (fF)	Extracted bus cap per pixel (fF)	Per-line cap (fF)	Per-line R (Ω)	Total cap (fF)	Total R (Ω)	RC (ns)
RST	0.422	1.076	1917.779	5939.200	1.963	5.8	11.390
PC	0.499	1.756	2886.906	5939.200	2.955	5.8	17.146
RS	0.437	1.556	2551.587	5939.200			15.154
S1	0.422	1.306	2212.256	5939.200	2.265	5.8	13.139
S2	0.422	1.338	2253.293	5939.200			13.383
TG	3.091	1.694	4900.289	4751.360	5.018	4.6	23.283
COL_OUT	0.207	1.457	1705.111	4751.360			8.102
VDD_H	1.557	1992.320	7372.800			14.690	
VDD_V	1.706	2183.206	1453.189			3.173	
VSS_H	1.982	3500.339	7372.800			25.807	
VSS_V	1.880	1925.530	1453.189			3.173	

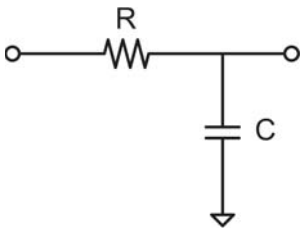

Figure 3-26: lumped RC model

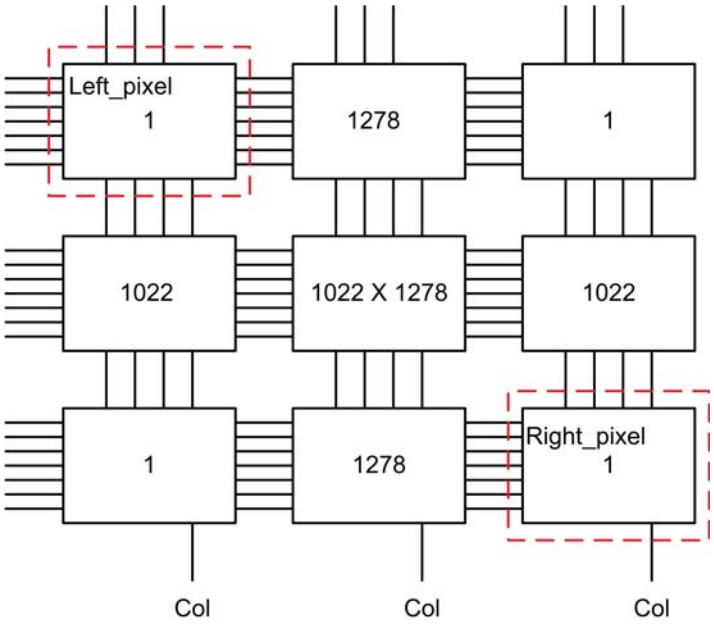

Figure 3-27: Complete pixel array simulation block with pixel and lumped RC model

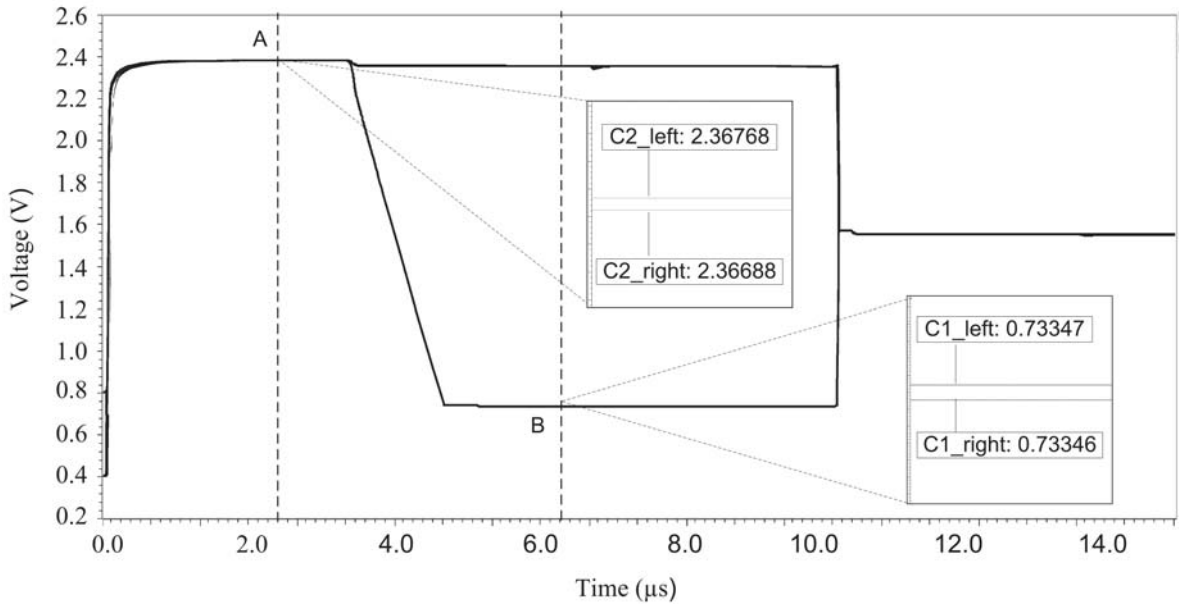

Figure 3-28: Offset for C1 and C2 storage voltage between Left_pixel and Right_pixel during FOT

Chapter 4

Readout chain

In previous chapter, the pixel implementation details have been presented, together with the comprehension of noise analysis, practical concerns for the pixel, and simulation analysis. For CMOS imagers, the readout of the signal from the pixel array also needs significant effort. In this chapter, we first present the whole readout chain architecture in Section 4.1. Next, in Section 4.2, the analog front end circuit operation and implementation will be explained. Finally, in Section 4.3, we present the LVDS output circuit with various issues.

4-1 Readout chain architecture

This project contains two different pixel architectures, implemented in two different chips, which are the 8T global shutter pixels and the HDR pixel (the details of HDR pixel implementation can be found in [44]) as we mentioned in Chapter 1. Both of them are built up from an array of 1280 pixel columns by 1024 pixel rows. From Figure 4-1, we can see that the readout functions of these two pixels are different. For the 8T pixel, the signal is readout only from the bottom side, while for the HDR pixel, the signal is readout from both top and bottom side. This is because the HDR pixel needs to readout two different reset and video signals in one Row Readout Time (ROT), thus, two channels for every column pixels are required. Although there is an extra readout channel for the HDR pixel and the speed specification for HDR pixel sensor is different from 8T global shutter pixel sensor, each readout circuit structure cell and its specifications of the two sensors are the same. We just implement one readout circuit and share it with two the sensors. This way eases the design effort and time.

In Chapter1, we have already given a general introduction about the whole sensor architecture and the function of each block. In this section, more details about the architecture of readout chain will be explained. The overview of the readout chain in this project is shown in Figure 4-2. The dash line in this figure separates the peripheral circuit of CMOS image sensor into three parts. The right two parts are the main readout circuit. Among them, the top part of which is the column parallel readout channels with the same pitch as pixels. They are intended

for processing the analog signals from the pixel and convert them into digital signals. The bottom part is the output part which serially transmits the digital signal from the ADCs. The left part of the figure is the support circuit. They generate the needed bias and reference signals to support the operation of the readout circuit.

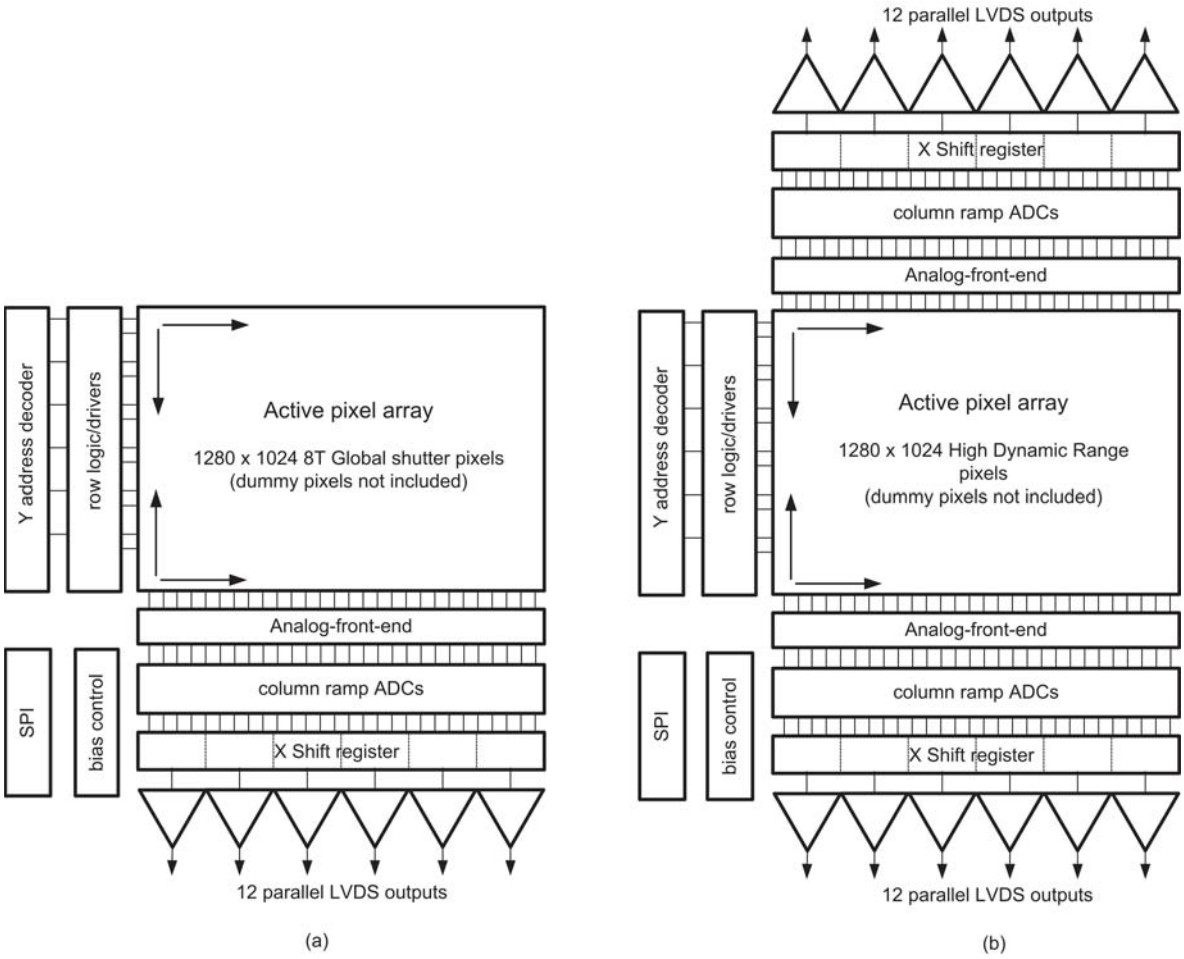

Figure 4-1: Basic sensor architecture (a) 8T global shutter pixel (b) High Dynamic Range pixel

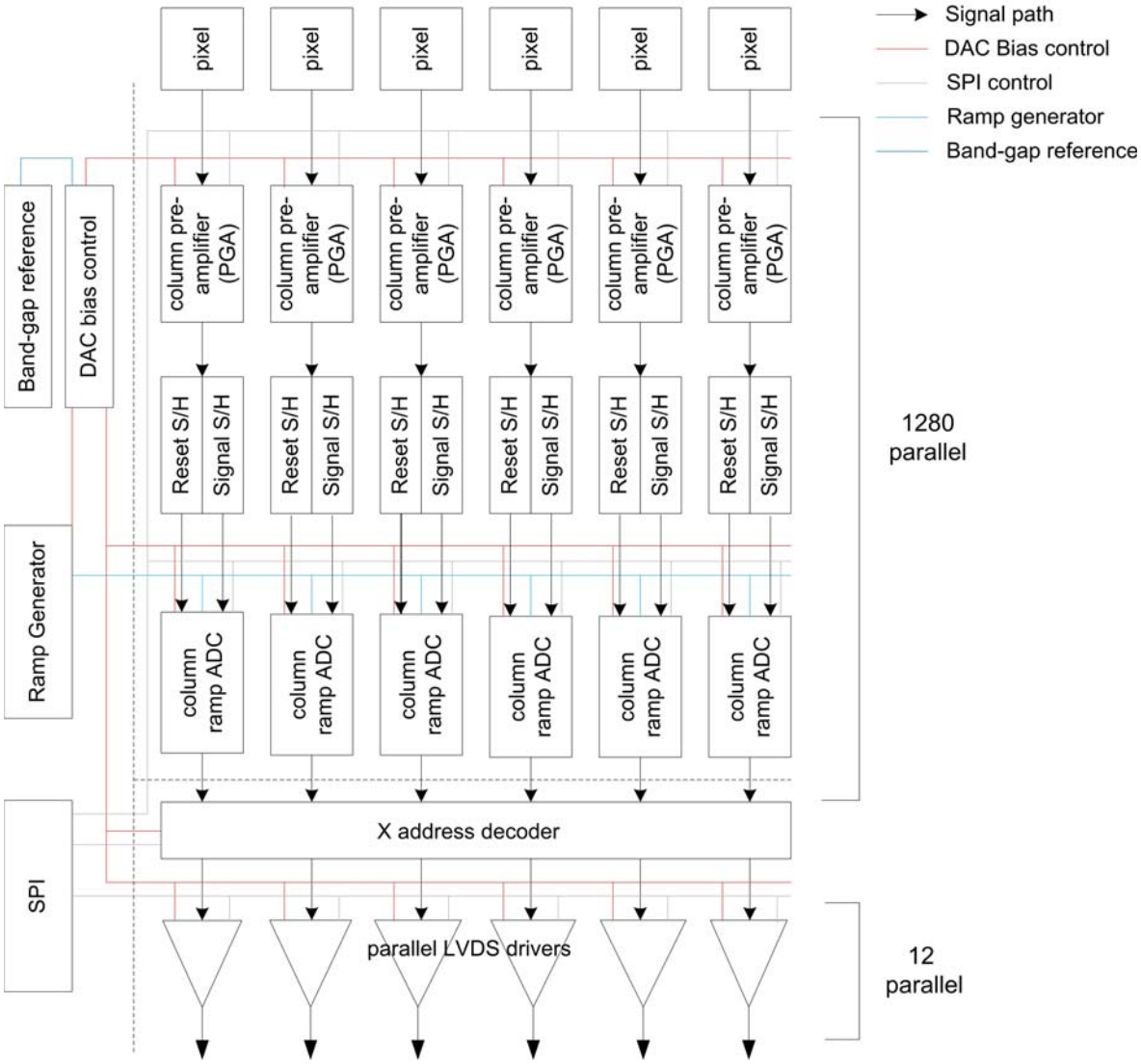

Figure 4-2: Architecture of readout chain

In the imager readout chain design, column AFEs contain a Programmable Gain Amplifier (PGA) and a Sample and Hold (S/H) circuit. During column parallel readout, the reset signal level V_{RESET} are subtracted from the 8T pixel readout video signal level $V_{SIGNAL2}$ (see Section 3-1-1), and meanwhile a programmable gain can be applied to this differential signal. Both the reference level $V_{reference,S/H}$ of the amplifier and the amplified signal level $V_{signal,S/H}$ are stored in analogue memories. The output for the AFE stage of one ROT is given by

$$V_{reference,S/H} = V_{CM} \tag{4-1}$$

$$V_{signal,S/H} = V_{CM} + A(V_{RESET} - V_{SIGNAL2}) \tag{4-2}$$

where V_{CM} is the common mode voltage of amplifier, A is the gain factor of this switched

capacitor amplifier.

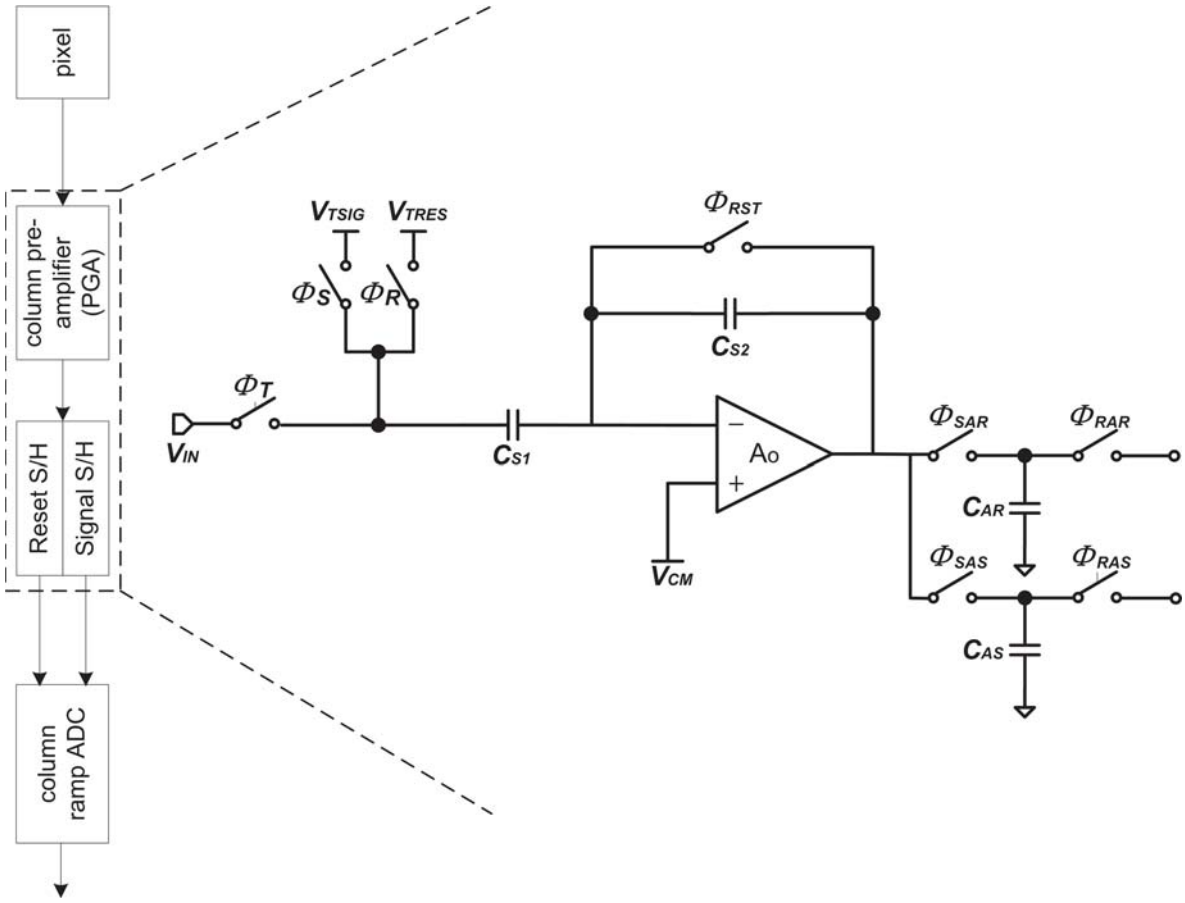

Figure 4-3: AFE block

As is shown in Figure 4-2,the column ADCs lies in the heart of the peripheral circuit. Together with ramp generator, the ADC converts the analog data, which stored on the sample and hold capacitors, into a digital number and subtract $V_{signal,S/H}$ from $V_{reference,S/H}$, the final result after the ADC is given by

$$V_{out,ADC} = V_{signal,S/H} - V_{reference,S/H} = A(V_{RESET} - V_{SIGNAL2}) = A\Delta V_{SIG2} \qquad (4\text{-}3)$$

where $V_{signal,S/H}$ is the amplified video signal stored on S/H stage, $V_{reference,S/H}$ is the reference level of the amplifier stored on S/H stage, A is the gain factor of the amplifier, V_{RESET} is the reset level of the pixel, $V_{SIGNAL2}$ is the readout video signal level of pixel and ΔV_{SIG2} is the voltage drop on C2. After that, this digital number is stored in a digital memory, until it is readout.

The block diagram of the column parallel ADC is shown in Figure 4-4. Each ADC cell consists of a comparator, a 12-bit counters and a 12-bit SRAM memories. The chip further contains a ramp generator that generates a ramp voltage of which the its slope can be defined by the

applied clock frequency. A simplified timing diagram in Figure 4-5 illustrates how the digital subtraction is implemented.

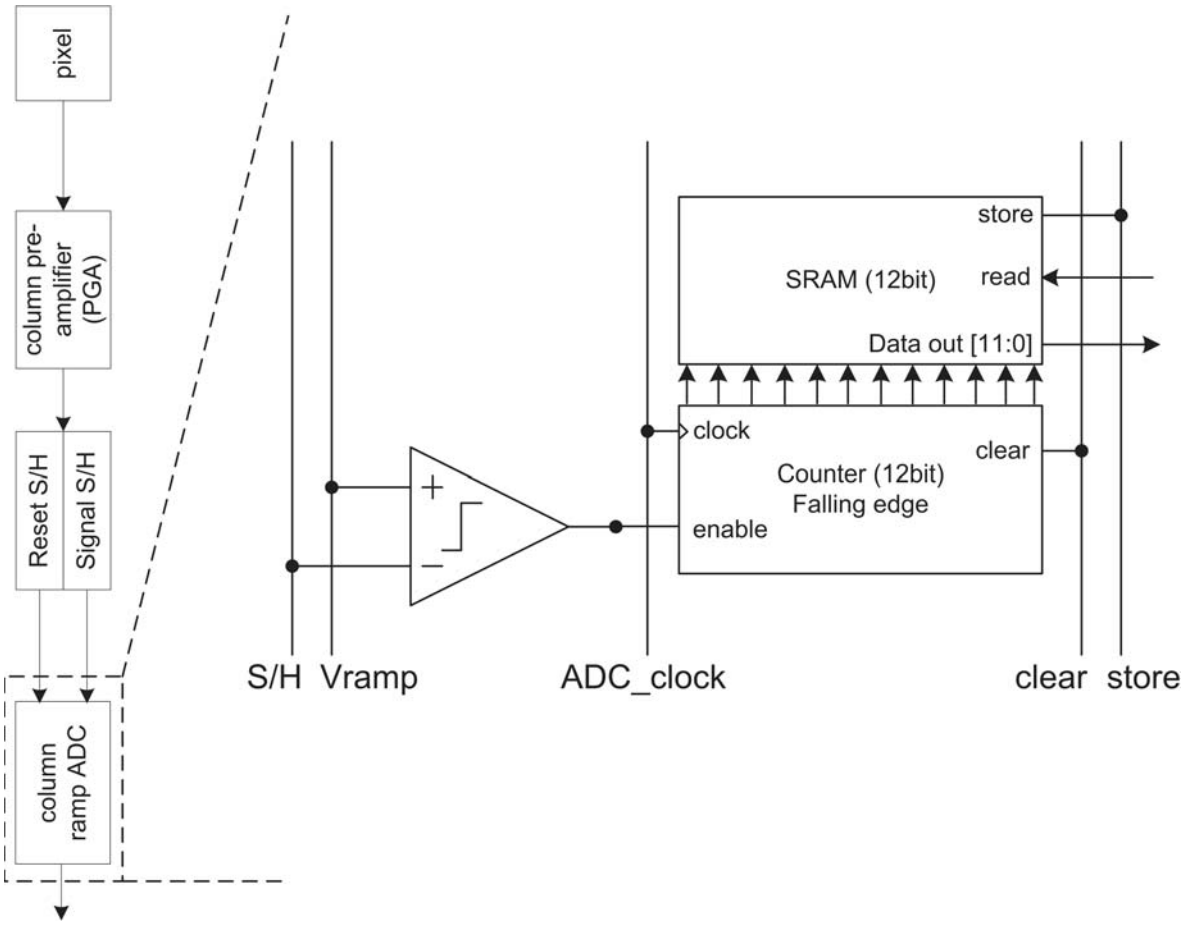

Figure 4-4: ADC block

At the start of the conversion phase, the previously stored values of the counters in the column are cleared. At T1, the reference level $V_{reference,S/H}$ is put on one input of the comparator. A positive slope from the ramp generator is applied to the other comparator input. Once the slope has crossed the reference level at T2, the comparator toggles and enables the counters. Until the end of the first ramp cycle at T3, the counters are disabled. At T4, the second ramp cycle starts, one input of the ADC is connected to the light-induced signal voltage $V_{signal,S/H}$ and the counter is enabled. Till the ramp signal crosses the signal level, the comparator toggles and the counter stops counting at T5, the then-reached value is stored in the counter. At the end of the conversion phase, the values from the counter are written into the SRAM memories of the column and are waiting for the readout.

After the ADC conversion, the digital signals are sent out through LVDS channels. This project adopts a parallel readout function which means a 12 bits signal is readout at one time, and one LVDS driver circuit is corresponding to one bit ADC output. As shown in

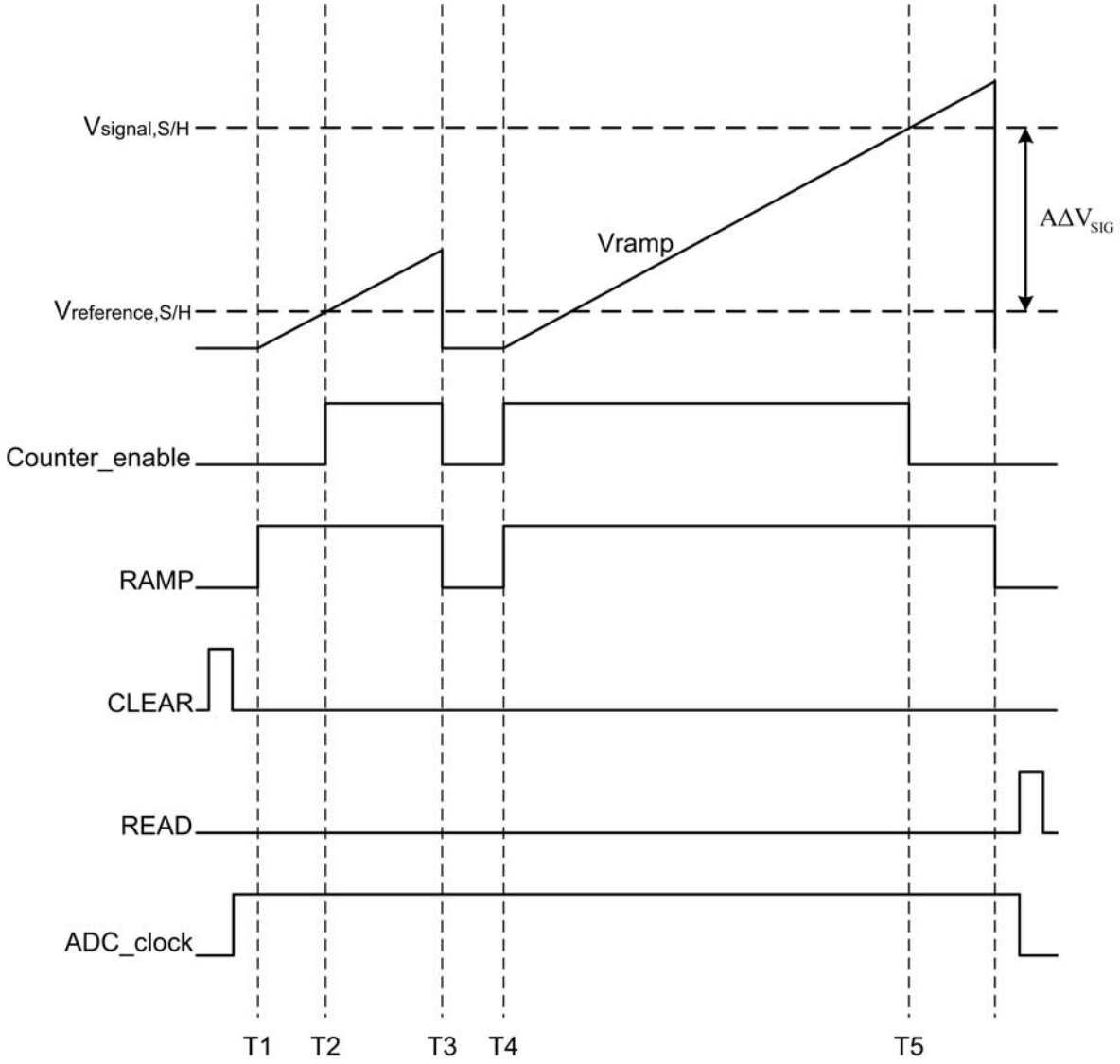

Figure 4-5: Timing diagram of ADC block

Figure 4-6, the X readout shift register selects the column chain and accesses the value from the ADC to the parallel LVDS drivers one by one. The LVDS drivers transform the 400Mbps bit stream to differential LVDS level signals and send them to LVDS receivers which are off-chip. The implementation details of LVDS drivers can be found in Section 4-3.

With the above three phases, the signals generated from pixels are processed and readout for further signal processing.

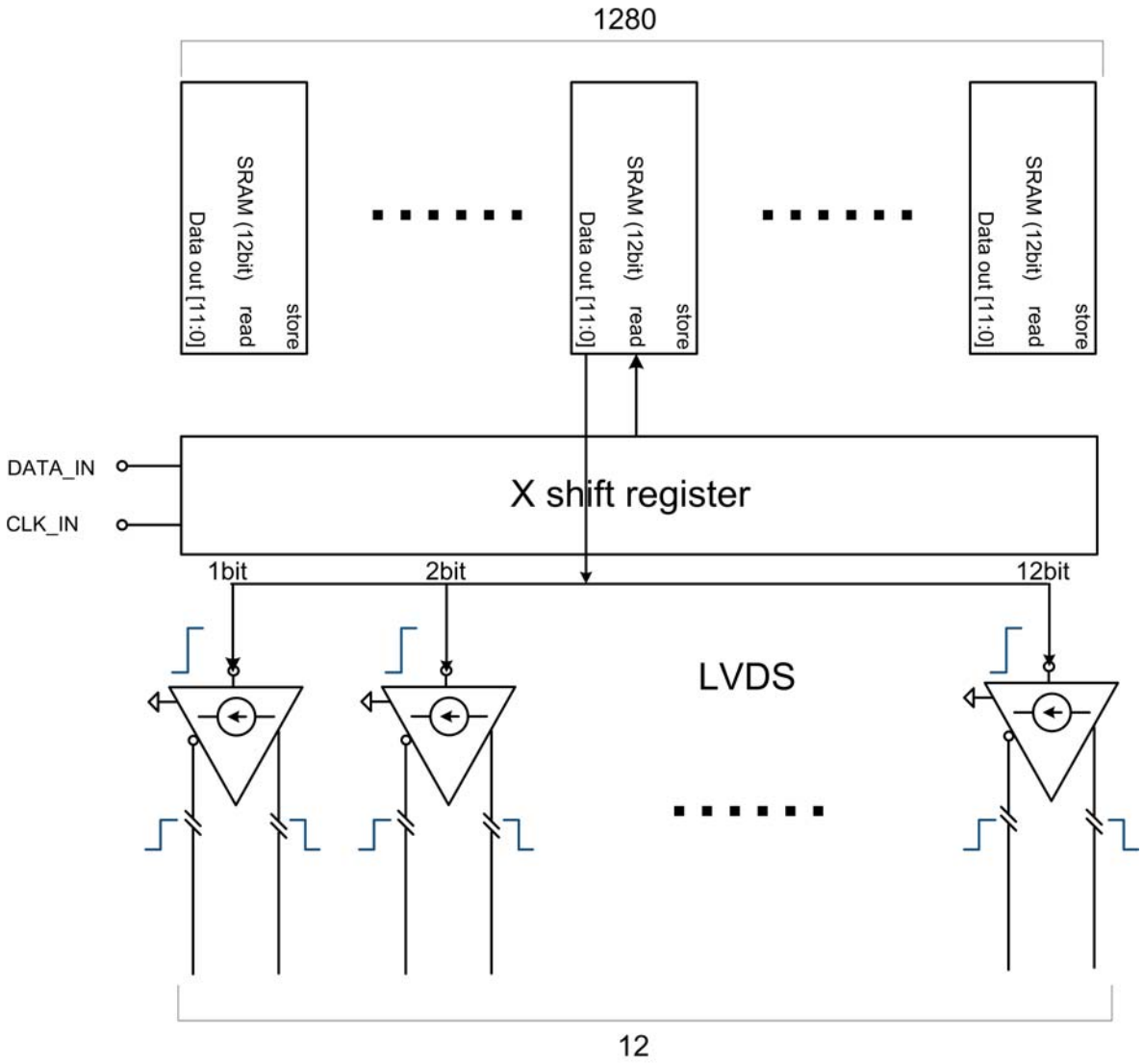

Figure 4-6: LVDS driver output block

4-2 Analog Front-End (AFE) column readout circuit

4-2-1 AFE circuit target specifications

As can be seen from Table 4-1, parts of the specifications of the 8T pixel and the HDR pixel are listed, from which, some AFE circuit target specification can be derived.

Since the AFE circuit serves as a preamplifier and its output signal is feed into the column parallel ADC, its output swing determines the gain of comparator in the ADC. For this design, assume the input range of the ADC as well as the output swing of the AFE is $V_{swing,AFE}$, and the resolution is 12bits, so the LSB is $V_{swing,AFE}/2^{12}$. To amplify LSB to 1.5V, the gain

Table 4-1: Specifications of 8T pixel and HDR pixel

Pixel type	8T global shutter pixel	HDR pixel [40]
Output swing	0.65V	High gain: 1.8V Low gain: 1.34V
Noise	Mode1 : $6.57e^-/339\mu V$ Mode2 : $8.69e^-/449\mu V$	Highgain : $3.1e^-/322.059\mu V$ Lowgain : $10.8e^-/321.084\mu V$

of comparator $A_{comp,ADC}$ should be:

$$A_{comp,ADC} > \frac{1.5 \times 2^{12}}{0.5 V_{swing,AFE}} \tag{4-4}$$

where $A_{comp,ADC}$ is the gain of comparator and $V_{swing,AFE}$ is the output swing of AFE circuit. After making a tradeoff between $A_{comp,ADC}$ and $V_{swing,AFE}$, the PGA output swing is chosen as 1.5V. From the output swing of the pixel in Table 4-1 we can see that the largest output swing is 1.8V for the HDR pixel in the high gain channel. It is also the largest input swing for the AFE circuit, thus, the smallest gain factor for the AFE is around 0.83. In this design, we choose 0.75 as a smallest gain for the amplifier. In order to ensure, in the environment of dark, the very small output swing from the pixel can be amplified to a large enough swing to support the ADC, the highest gain factor is chosen to be 8.

Apart from the gain of the amplifier, we also define a limit for the amplifier input referred noise. Generally, the input referred noise of the PGA at unity gain should be smaller than the pixel FD referred noise. For the 8T global shutter pixel, that is $v_{n,AFE} < 169.5\mu V$, and for the HDR pixel, that is $v_{n,AFE} < 321.084\mu V$. Here, we define that the input referred noise of the PGA at unity gain should be smaller than $160\mu V$. What's more, we determine the ROT time for the AFE is $5\mu s$ in this project.

4-2-2 Non-ideal effects in switches

The AFE structure is a switched-capacitor topology. This circuit is realized by using MOS switches which have the non-idealities of a non-zero and non-linear on-resistance. Thus, before we design the AFE circuit, we first analyze these non ideal effects [39].

Channel charge injection: Consider a simple sampling circuit as shown in Figure 4-7. Assuming $V_{in} \approx V_{out}$, the total charge stored in the inversion layer is

$$q_{inj} = WLC_{ox}(V_{CK} - V_{in} - V_{TH}) \tag{4-5}$$

where L and Wrepresents the transistor effective channel length and width, C_{ox} is the gate oxide capacitance per unit area, V_{CK} is the control signal switch M1, V_{TH} is the threshold voltage of M1, V_{in} and V_{out} are input voltage and output voltage. When the switch is off, q_{inj} still remains through the source and drain terminals. If the charge is injected to the capacitor, it will result in an error in the sampled output. As a worst-case estimation, we assume that all the charge is injected into the sampling capacitor, thus, the resulting error is:

$$\Delta V_{inj} = \frac{WLC_{ox}(V_{CK} - V_{in} - V_{TH})}{C_{CH}} = \frac{q_{inj}}{C_H} \tag{4-6}$$

Taking the body effect into account, the channel charge injection manifest three types of errors in MOS sampling circuit: gain error, DC offset and nonlinearity.

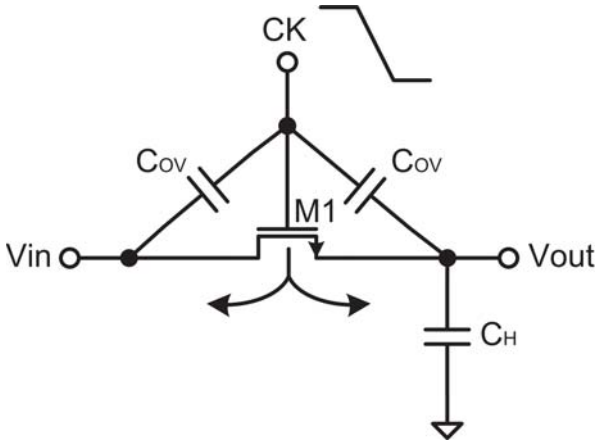

Figure 4-7: RC sampling circuit

Clock feed-through: The effect of a MOS switch coupling the clock transitions to the sampling capacitor through its gate-drain and gate-source overlap capacitance is referred to as clock feed-through. Like the channel charge injection, it also introduces an error in the voltage stored on C_H. Assuming the overlap capacitances are constant as shown in Figure 4-7, we have:

$$\Delta V_{clk} = \alpha V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H} \tag{4-7}$$

where C_{ov} is the overlap capacitance per unit width, α is the attenuation factor smaller, which accounts for a part of the total charge of $V_{CK}WC_{ox}$ flowing to the ground rather than the hold capacitor. The error ΔV is independent of V_{in}, exhibits itself as a constant offset between input and output.

kTC noise: Recall from Section 3-2 that a resistor charging a capacitor generates a rms voltage of $\sqrt{kT/C}$. In sampling circuits, this similar noise also occurs due to the same reason. The on-resistance of the switch introduces thermal noise at the output and along with the instantaneous value of the input voltage, this noise is stored on the capacitor when the switch is off. It also leads to an additional error on the stored output voltage, that is:

$$\Delta V_{kTC} = \sqrt{\frac{kT}{C_H}} \tag{4-8}$$

The total error ΔV in the sampled voltage across the hold capacitor is given by

$$\begin{aligned}\Delta V &= \Delta V_{inj} + \Delta V_{clk} + \Delta V_{kTC} \\ &= \frac{q_{inj}}{C_H} + \alpha V_{CK}\frac{WC_{ov}}{WC_{ov}+C_H} + \sqrt{\frac{kT}{C_H}}\end{aligned} \tag{4-9}$$

Since in most practical cases, the first term of Eq. (4-9) dominates, the voltage error ΔV can be simplified as $\Delta V = q_{inj}/C_H$ in the following discussions. What's more, it shall be noted that all contributions of the error voltage decrease if a larger hold capacitor is adopted. Thus, in this AFE circuit design, we set the sample and hold capacitor as 450fF.

4-2-3 Autozeroing technique to suppress the offset

In CMOS technology, due to the variation and uncertainties in fabrication, the input offset of typical differential amplifiers is as large as several milli-volt. As we mentioned in Section 4-1-1, the AFE circuit first samples the reference voltage on the S/H stage and then compares it with the ramp slope in the comparator. If this reference voltage severely fluctuates with this input offset, the range of ramp slope V_{ramp_ref}, which generated from ramp generator, is hard to cover this fluctuated reference voltage. It will lead to an error during the reference voltage ADC converting. Although this offset can be directly minimized by enlarging the transistor size, this readout chain needs to fit into the pixel pitch of $4.8\mu m$. Thus, it is impossible to increase the dimension of transistor without any limitation and we need autozeroing to reduce such an offset at AFE stage.

Similar to CDS, autozeroing is also a discrete-time sampling technique. In one clock phase, it samples the offset of the amplifier, and then in the next clock phase, the offset is subtracted from the input signal. There are three basic topologies for an autozeroing technique that can be distinguished: open-loop offset cancellation, closed-loop offset cancellation, and closed-loop offset cancellation with an auxiliary amplifier [45]. The disadvantage of the open-loop offset cancellation method is that the gain of the amplifier is limited in order to avoid the amplified offset voltage saturating the amplifier's output. Besides that, the closed-loop offset cancellation with an auxiliary amplifier method require an additional auxiliary amplifier placed in the feedback loop during offset cancellation. It consume a large area in the column chain. Considering the aspect of the high gain of the amplifier and the area reduction, the closed-loop offset cancellation would be the better solution.

Figure 4-8 shows the basic principle of the closed-loop offset cancellation technique. In the sampling phase, the output and input of the amplifier are shorted together by switches S2 and S3, placing the amplifier in a unity gain configuration. When the node voltage is settled, the voltage over the auto-zero capacitor is given by

$$V_C = \frac{A_o}{1+A_o}V_{OS} \tag{4-10}$$

where A_o is the voltage gain of the op-amp, V_{OS} is the offset of the amplifier, V_C is the voltage over the auto-zero capacitor C_C. Thus, the circuit reproduces the amplifier's offset at node X.

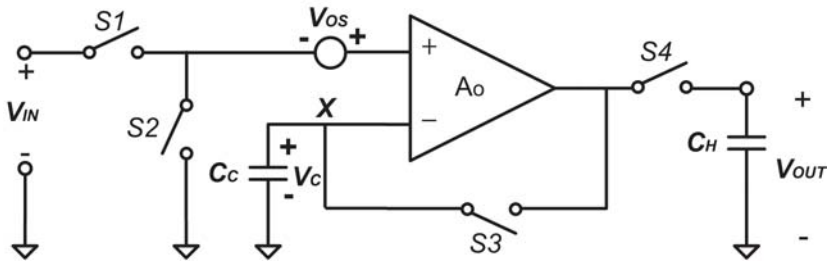

Figure 4-8: Autozeroed amplifier with closed loop offset storage [43]

During the signal phase, S2 and S3 are opened and S1 and S4 are closed. The output voltage can be expressed as:

$$V_{out} = A_o(V_{in} + V_{OS} - V_C) = A_o(V_{in} + \frac{1}{A_o + 1}V_{OS}) \tag{4-11}$$

where V_{in} and V_{out} are the input and output voltage of the amplifier. Thus, the input referred offset voltage of the overall circuit equals to $\frac{1}{A_o+1}V_{OS}$.

Except for the finite gain, the error of the output voltage caused by non-idealities of the MOS switch is another source of residual offset. Considering the same analysis above, the final offset is given by:

$$V_{OS,res} = \frac{1}{A_o + 1}V_{OS} + \frac{q_{inj}}{C_H} \tag{4-12}$$

where q_{inj}/C_H is the sampled voltage error caused by non-ideality in the switches as described in Section 4-2-1, C_H is the sample and hold capacitors and q_{inj} is the injected charge due to channel charge injection.

4-2-4 Operation principle of AFE circuit

The AFE readout circuit performs two functions for the signal processing: CDS and PGA. We choose the switch capacitor topology for the amplifier, because a resistive feedback needs a large area to implement on chip and suffers from gain inaccuracies. The basic AFE structure consists of: a test signal block, a column load, a CDS/PGA stage and a sample and hold stage. To make the story clear, we divide the AFE circuit operation into three phases:

Phase1: Offset cancellation

Figure 4-9 shows a circuit diagram of the AFE circuit exploiting the offset cancellation. During the autozeroing phase, the output and input is shorted, charges containing the offset information are stored on calibration capacitor C_C. In the signal phase, Φ_{C2} is open, Φ_{C1} is close, and the input referred offset is

$$V_{OS,res} = \frac{1}{A_o + 1}V_{OS} + \frac{q_{inj}}{C_C} \tag{4-13}$$

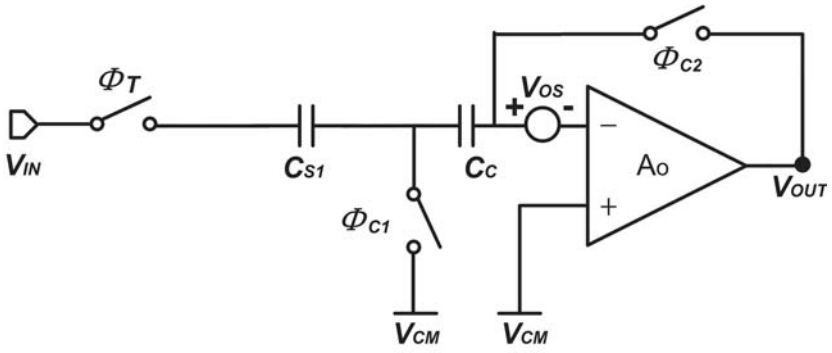

Figure 4-9: AFE operation in phase 1

as explained in Section 4-2-2, where A_o is the voltage gain of the op-amp, V_{OS} is the offset voltage of the amplifier and q_{inj}/C_C is the sampled voltage error caused by non-ideality in the switches.

Phase2: Sampling reference voltage

In phase two, when the reset level V_{RESET} comes from the column bus, the amplifier is first initialized by closing switch Φ_{RST} and Φ_{SAR}, it shorts the output to the negative input and places the amplifier in unity feedback (Figure 4-10). The voltage stored on C_{S1} is given by:

$$V_{C_{S1}} = V_{RESET} - V_{CM} \tag{4-14}$$

After that, the switch Φ_{RST} opens, followed by Φ_{SAR} open, thus, the reference voltage $V_{reference,S/H}$ is stored on C_{AR}.

Phase3: Amplifying and sampling the signal voltage

In this phase, as shown in Figure 4-11 the video level $V_{SIGNAL2}$ is readout, the voltage stored on C_{S1} now is expressed as:

$$V_{C_{S1}} = V_{SIGNAL2} - (V_{RESET} - V_{CM}) \tag{4-15}$$

This value is amplified with the gain of $A = C_{S1}/C_{S2}$ and the output is:

$$V_{signal,S/H} = V_{CM} + A(V_{RESET} - V_{SIGNAL2}) \tag{4-16}$$

With the switch Φ_{SAS} open, this value is sampled on C_{AS}.

Pipeline readout

For the purpose of readout the voltage more efficiently, we use the pipeline readout in our AFE design, which implying that the sampling and readout are able to happen simultaneous. The details of this pipeline readout circuit has been deleted due to the confidential reason. We just give the circuit block as shown in Figure 4-12.

The whole timing diagram of AFE circuit is as shown in Figure 4-13

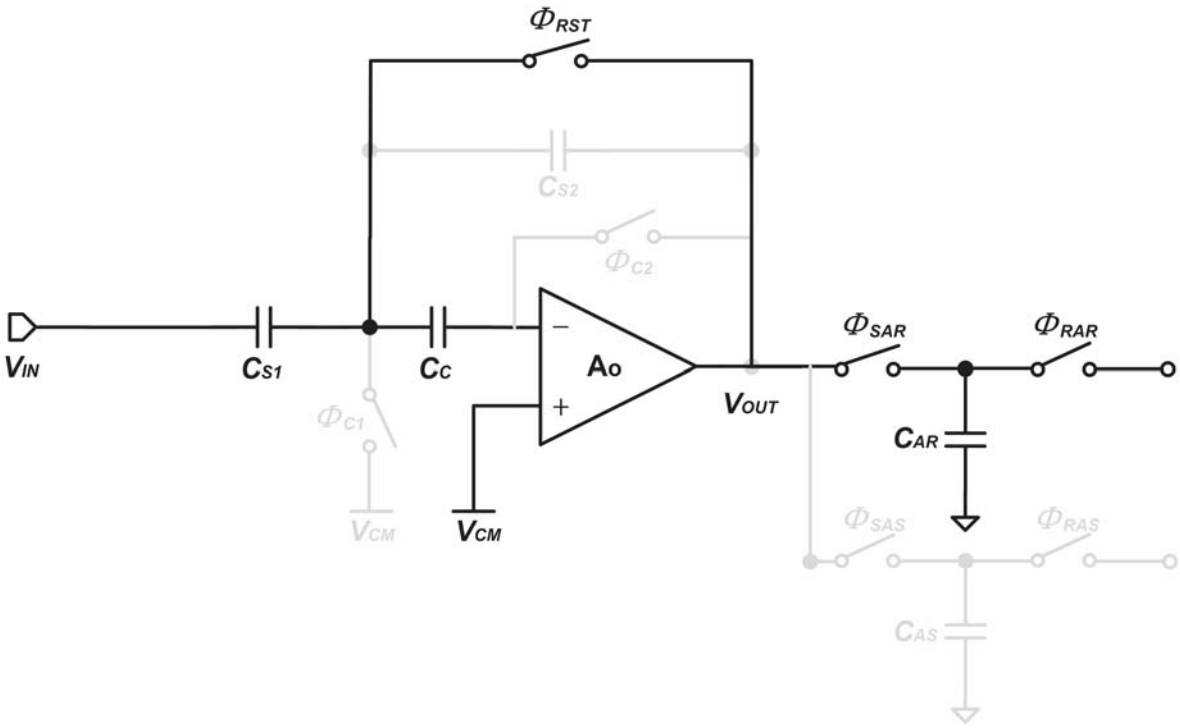

Figure 4-10: AFE operation in phase 2

4-2-5 Implementation of AFE circuit

Amplifier

Op-amp structure:

To make the area consumption efficient, we try to design the op-amp as simple as possible by starting with a single stage amplifier as shown in Figure 4-14. This amplifier adopts a differential pair with an active current mirror structure.

Op-amp common-mode voltage:

In the design of the op-amp, we first decide the input common-mode voltage V_{CM} of the circuit. For M4 to be saturated, the output voltage cannot be less than $V_{CM} - V_{TH4}$, where V_{TH4} is the threshold voltage of M4. Thus, to maximize the output swings, the input CM level should be as low as possible, with the minimum given by $V_{GS4} + V_{DS5,\min}$, where V_{GS4} is the gate-source voltage of M4 and $V_{DS5,\min}$ is the minimum overdrive voltage of M5. Suppose $V_{TH} = 0.7$V in this technology, and the overdrive voltage is around 0.2V, then the minimum common-mode voltage is $V_{CM,\min} = 1.1$V. Thus, in our design, we choose the common mode voltage as 1.1V.

Op-amp output swing:

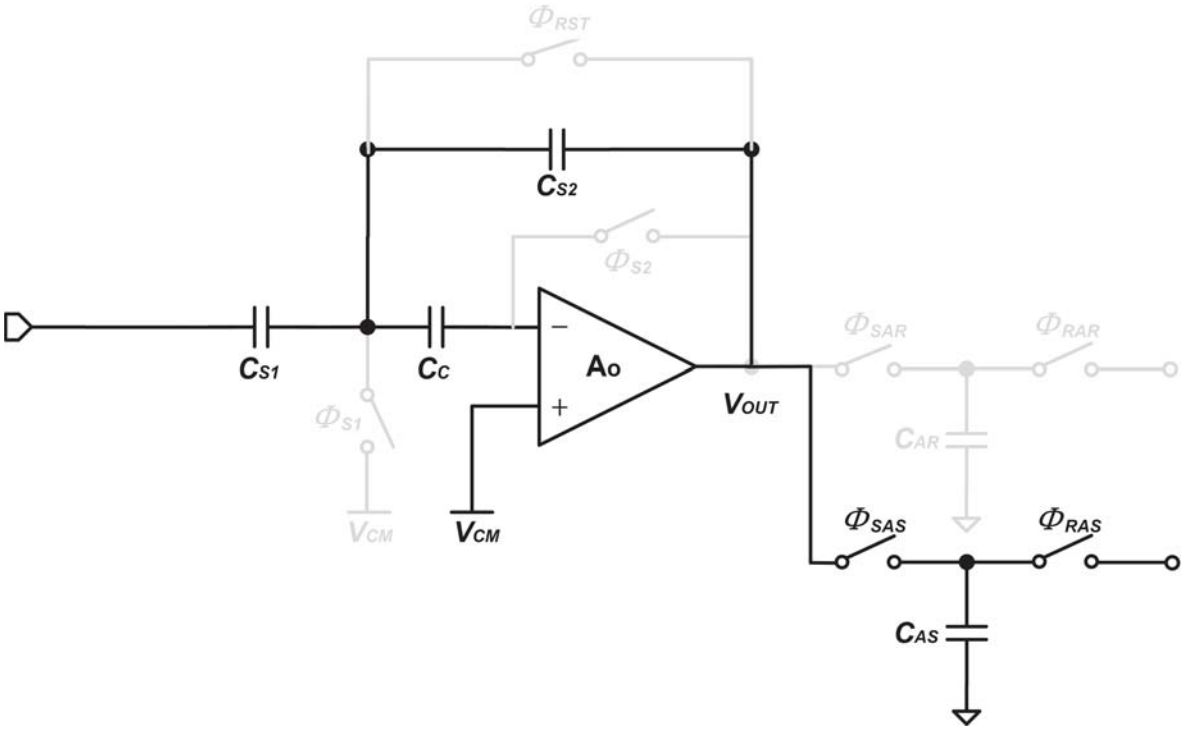

Figure 4-11: AFE operation in phase 3

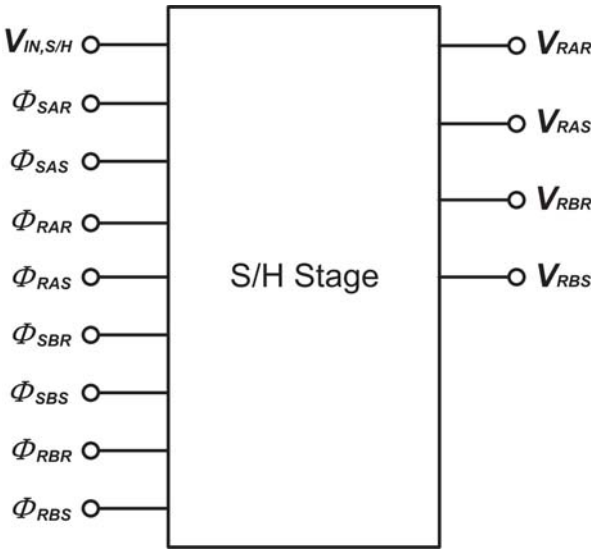

Figure 4-12: Pipeline readout block

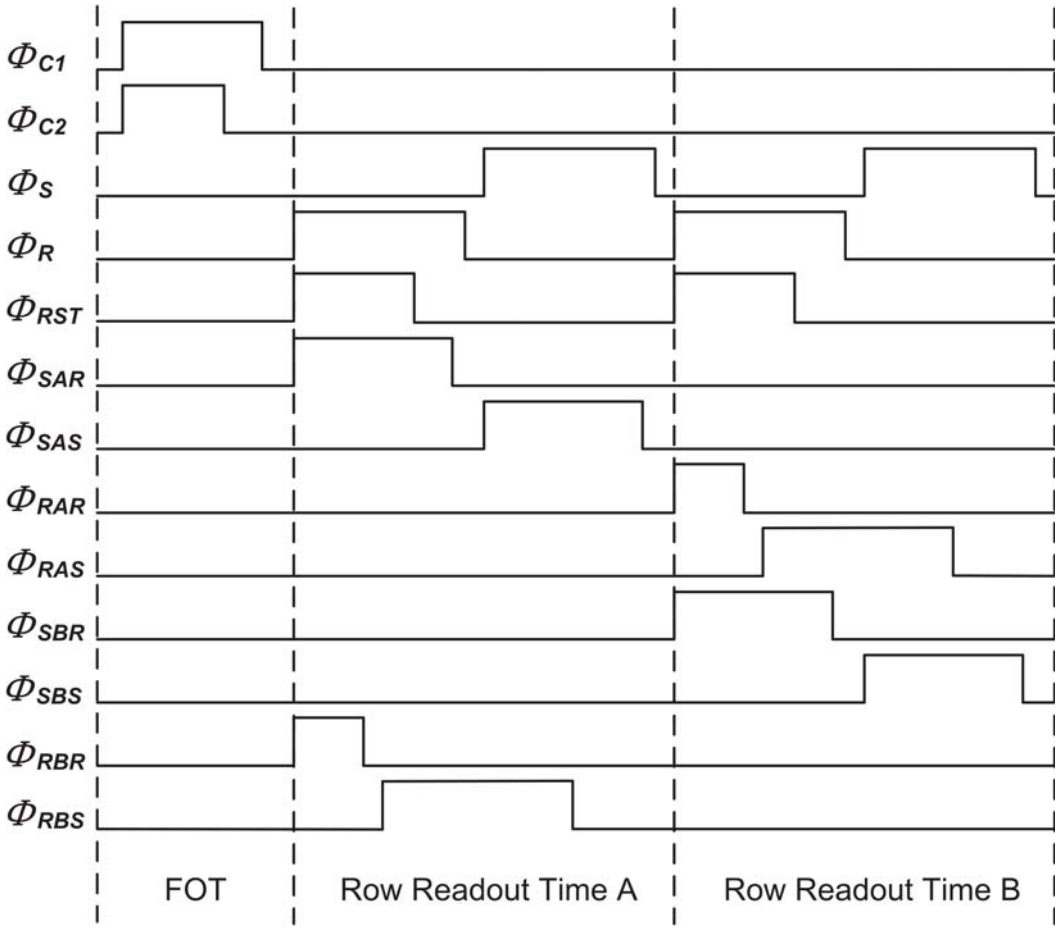

Figure 4-13: Timing diagram of AFE circuit

For the output swing, with the perfect symmetry, the minimum output is $V_{OUT,\min} = V_{DD} - |V_{GS2,\max}|$ when $V_{IN} = V_{CM}$, where V_{DD} is the supply voltage of the op-amp, and $V_{GS2,\max}$ is the maximum gate-source voltage of M2. The maximum output is $V_{OUT,\max} = V_{DD}$ when $|V_{IN} - V_{CM}|$ is sufficiently large.

Op-amp gain:

The gain of this amplifier is easily calculated, it is given by:

$$A_o = G_m R_{out} \tag{4-17}$$

where $G_m = g_{m4}$, and R_{out} is the parallel combination of the two output resistances $r_{DS1}//r_{DS3}$, r_{DS1} and r_{DS3} are the output resistance of M1 and M3.

Op-amp bandwidth:

The bandwidth is limited by the output capacitance and the same output resistance R_{out}:

$$f_{-3dB} = \frac{1}{2\pi R_{out} C_L} \tag{4-18}$$

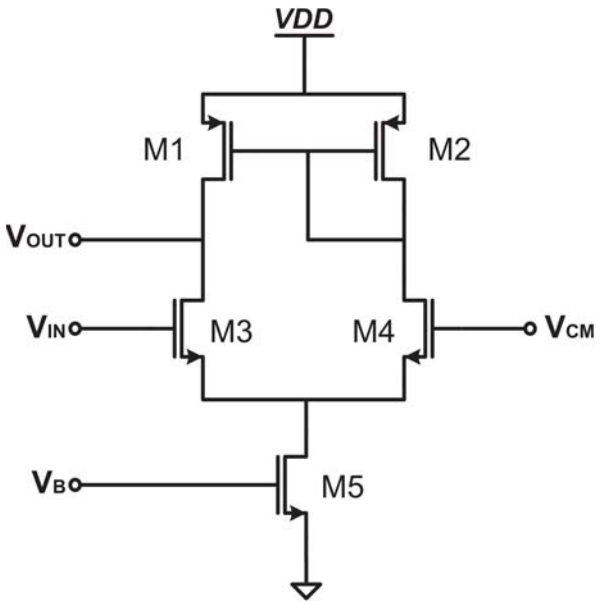

Figure 4-14: Op-amp used in the AFE

where C_L is the load capacitor at the value of $450fF$.

Op-amp gain-bandwidth:

The gain bandwidth of amplifier is:

$$GBW = A_o f_{-3dB} = \frac{G_m}{2\pi C_L} \tag{4-19}$$

To design the amplifier with a sufficient high gain- bandwidth, we use wider devices for M3 and M4 to obtain a sufficiently high G_m.

Figure 4-15 shows the op-amp voltage gain, bandwidth and gain-bandwidth under the condition of open loop. From this figure, we can see that the gain of this op-amp is 51.92dB, bandwidth is 30.76kHz, and the gain bandwidth is 7.86MHz. So this gain bandwidth is large enough for our design.

Op-amp noise:

The dominant noise source in this amplifier is the flicker noise and the thermal noise. The equivalent input referred noise can be expressed as [39]:

$$\overline{V_{n,in,tot}^2} = 8kT\left(\frac{2}{3g_{m4}} + \frac{1}{g_{m4}^2\left(r_{DS1}//r_{DS3}\right)}\right) + \frac{2K}{C_{ox}W_4L_4}\frac{1}{f} \tag{4-20}$$

where where L_4 and W_4 represents the effective channel length and width of M4, C_{ox} is the gate oxide capacitance per unit area, K is a process-dependent constant, f is the frequency, $k = 1.38 \times 10^{-23}$J/K is Boltzmann's constant, T is the temperature.

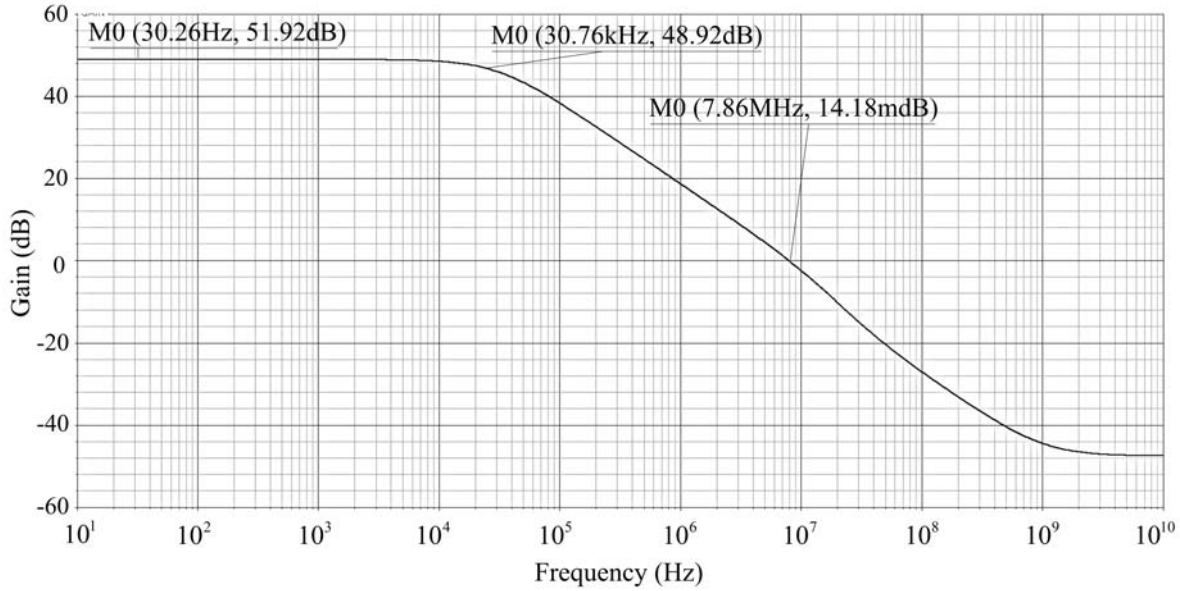

Figure 4-15: Open loop gain of amplifier

In order to understand in detail how the open-loop gain of the op-amp determines the precision of the feedback system, we have done some analysis by deriving the equations for it. For the purpose of simplicity, we ignore the autozero capacitor C_C.

Gain error of the amplifier:

Since $V_{out} = -A_o V_X$, we have

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{C_{s1}}{C_{s2} + (C_{s2} + C_{s1} + C_{in})/A_o} \tag{4-21}$$

where C_{in} is the finite input capacitance of the op-amp.

For a large value of A_o,

$$\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{C_{s1}}{C_{s2}}\left(1 - \frac{C_{s1} + C_{s2} + C_{in}}{C_{s2}}\frac{1}{A_o}\right) \tag{4-22}$$

The gain factor of this switched capacitor amplifier is:

$$\left|\frac{V_{out}}{V_{in}}\right| \approx \frac{C_{s1}}{C_{s2}} \tag{4-23}$$

And the amplifier suffers from a gain error which is given by:

$$gain\ error = \frac{C_{s2} + C_{s1} + C_{in}}{C_{s2} A_o} \tag{4-24}$$

From Eq. (4-24), we can see that in order to decrease the gain error, we need to set the voltage gain of op-amp as high as possible.

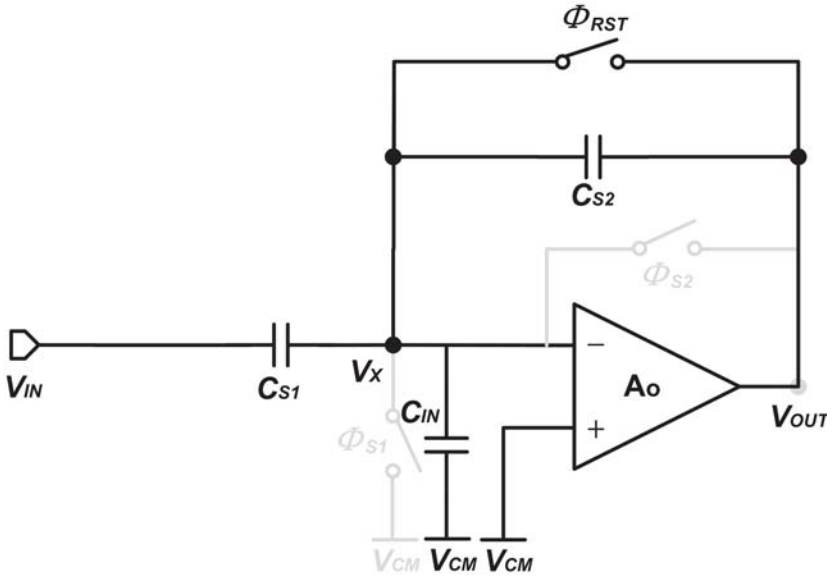

Figure 4-16: Equivalent circuit of the amplifier during amplification

Speed of the amplifier:

For this switched capacitor amplifier, the feedback factor is

$$\beta = \frac{C_{s2}}{C_{s1} + C_{in} + C_{s2}} \tag{4-25}$$

Thus, the closed loop gain bandwidth of the amplifier is approximately given by

$$f_{-3dB,CL} = \frac{C_{s2}}{C_{s1} + C_{in} + C_{s2}} \frac{G_m}{2\pi C_L} \tag{4-26}$$

The analysis of the time constant can be found in [39], here, we just rewrite the final result:

$$\tau = \frac{(C_{s1} + C_{in})C_{s2} + C_L\,(C_{s1} + C_{s2} + C_{in})}{G_m C_{s2}} \tag{4-27}$$

For a large signal, the speed of the amplifier is limited by either the bandwidth and the slew rate. Upon entering the amplification mode, the op-amp experiences a large step at the inverting input. The tail current of the op-amp's input differential pair is then steered to one side and its mirror current charges the capacitance seen at the output. Since M3 is off during slewing, the slew rate is approximately equal to I_{D5}/C_{out}, where I_{D5} is the drain current of M5 as shown in Figure 4-14, C_{out} is the total load capacitance of this amplifier. Since the amplifier is loading a sample and hold capacitor, hence, the output capacitance C_{out} can be estimated by the S/H capacitor, which has a value of 450fF, together with C_{DB3} and the Miller capacitance of C_{GD3}, C_{DB3} and C_{GD3} are the drain junction capacitor and the

gate-drain overlap capacitor of M4, both of them have the value of a few tens of femto-farad. As a result, the relatively small output capacitance, in conjunction with big supply current results in a big slew rate. Thus, the speed of amplifier is determined by the bandwidth.

Noise of the amplifier:

In this switched capacitor amplifier, the flicker noise can be suppressed by the CDS operation, as well as the flicker noise generated from pixel circuit. Except for the noise generated by the op-amp, two other noise source locations are also identified in this switched capacitor circuit: the gain stage and the sample and hold stage.

1. Gain stage: The capacitance used for the gain stage (C_{S1} and C_{S2}) have much less impact on the noise. The reason is that the correlated kTC noise generated on these capacitors is sampled on both the reference level storage capacitor and the video level storage capacitor in the sample and hold stage, thus, they can be cancelled by a second CDS operation which occurs in AD conversion.

2. S/H stage: The noise generated by this circuit is mainly determined by the kTC noise of the S/H capacitance. For one sample, this noise should be kT/C_L. Since two samples during one readout, kT/C_L should be multiplied by a factor of $\sqrt{2}$ in order to obtain the noise generated by the entire S/H operation.

Switchable Capacitors

So far, the switched capacitor amplifier is implemented with a fixed gain stage capacitor. In order to make our circuit to operate with different pixel types and illumination levels, as can be seen from Figure 4-17, we designed the feedback path with one switchable capacitor in parallel with one fixed capacitor, and designed the sampling path with two switchable capacitors in parallel with one fixed capacitor.

When choosing the capacitors value, the trade-off between mismatch and available area of the column pitch should be noticed. However, since there is no mismatch report by now, this factor is loosely considered now. From above analysis, we have known that the gain stage for this amplifier is from 0.75 to 8, we choose the following values for the capacitors:

$$\begin{aligned} C_{S1} &= 118\text{fF} \\ C_X &= 131\text{fF} \\ C_Y &= 303\text{fF} \\ C_{S2} &= 50\text{fF} \\ C_Z &= 95\text{fF} \end{aligned} \tag{4-28}$$

where C_{S1} and C_{S2} are fixed capacitors, and C_X, C_Y and C_Z are switchable capacitors. Therefore, we have eight gain combinations, from 0.75 to 8.

We use two switches with complementary control signals to select the capacitor of each path. Hence, when the capacitors are not selected, they do not load the feedback path of the amplifier, which further can leads to a bigger gain error of the whole circuit.

Switches

The content of this part has been removed for confidential reasons.

Test signal switch and bias control

On the input path, we add a test signal injection block, which can be replaced the pixel signal by an external voltage source. This allows full characterization of the readout path of the sensor.

What's more, in the above gain factor analysis, we ignored the autozero capacitor C_C. However, in fact, this autozero capacitor induces a larger gain error

$$\left(\frac{C_{in}+C_C}{C_C}\frac{C_{s1}+C_{s2}}{C_{s2}}+\frac{C_{in}}{C_{s2}}\right)\frac{1}{A_o} \tag{4-29}$$

In order to keep the flexibility to select the final result with autozeroing or without autozeroing, we also add a switch Φ_C for C_C.

As the exact pixel output level and output swing is currently unknown, the bias of theis amplifier is allowed to change by means of the reference voltage V_{CM} by a DAC bias control block, which implementation can be found in [40]. With this adjustable reference voltage, the reference level can be set to readout the signals in the most optimal way and designed for its full voltage range.

Figure 4-17 shows the complete circuit implementation of this switched capacitor amplifier.

4-2-6 Simulation results of AFE circuit

Some simulations with extracted parasitics from the layout (Appendix A) have been done to evaluate the AFE performance. The input referred noise of each gain stage is presented in Table 4-2. The noise for each gain stage is all smaller than 200μV, as we expected.

Table 4-2: Noise performance of AFE circuit

Gain	Output noise (μV)	Input referred noise (μV)
0.75	147.1	196
1.53	139.5	78.7
1.81	143.1	79.5
2.59	138.1	53.3
3.36	134.9	40.2
3.69	138.7	37.6
6.22	137.6	22.1
8.02	135.4	16.9

The linearity for the readout circuit mainly depends on the gain of the amplifier and the ramp generator. The linearity performances for the AFE circuit at the lowest gain and largest gain

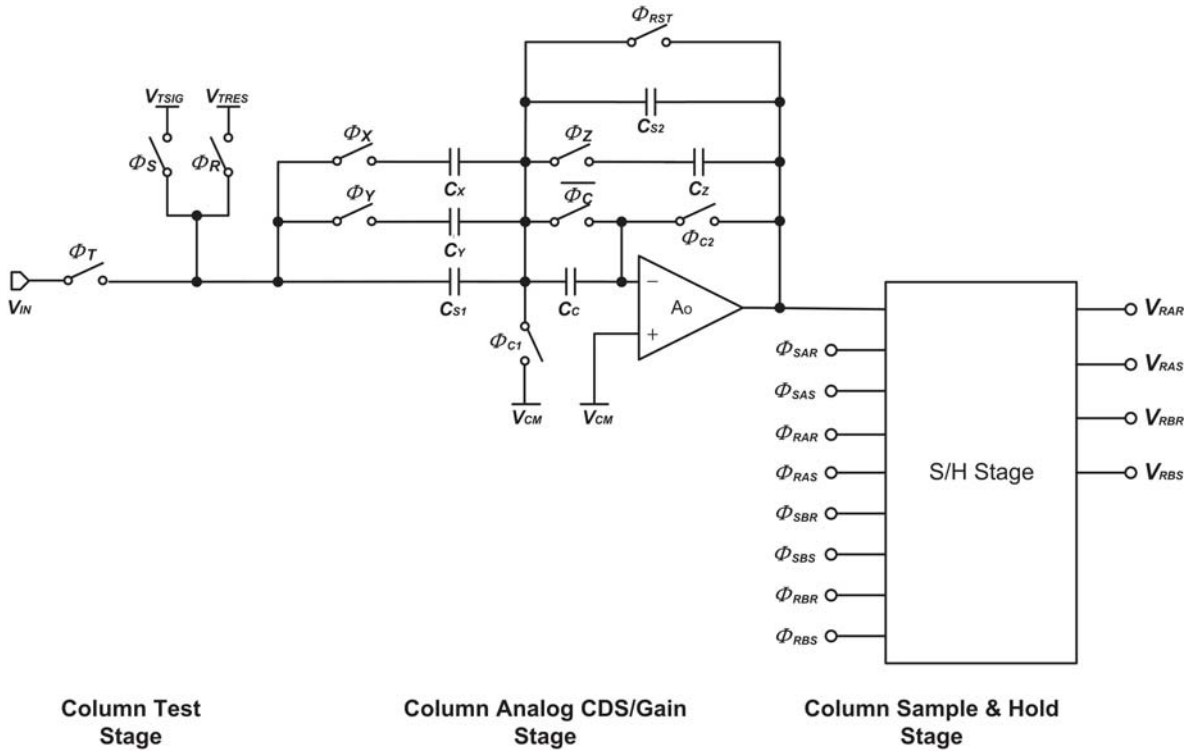

Figure 4-17: AFE circuit

stage are plotted in Figure 4-18 and Figure 4-19. From Figure 4-18 (a) vs. Figure 4-18 (b) and Figure 4-19 (a) vs. Figure 4-19 (b), we can see that the gain calculation from the signal at the output of S/H is a little larger than the one calculated from the output of the PGA. That is because the non-ideal effect of the MOS switches introduces an offset during the sampling and readout. Fortunately, in this design, this effect has no impact on the AFE linearity. The linearity gain error for this AFE circuit design is smaller than 0.1%.

In the pixel, we define the largest ΔV_{SIG} as a white signal, and the smallest ΔV_{SIG} as a black signal. In the switched capacitor amplifier, the capacitor charge and discharge have an effect on the sample speed and gain offset. In order to simulate the sample speed and the gain offset between the former signal and the latter signal. We set the input test-bench for this simulation as white-white-black-black to see the offset and charge and discharge speed, due to the fact that we use pipeline readout function. Figure 4-20 shows the output simulation result of switched capacitor amplifier at gain factor equals to 8 (the largest gain factor and the worst case of sampling speed). From this figure, we can see that the CDS operation can be completed within 5μs. And the charging (rising) offset is 70μV, the discharging (falling) offset is 10μV. These offset are much smaller than 1/2 LSB ($1.5/2^{13}$) of the comparator.

As we said before, the gain factor is different between with autozeroing and without autozeroing, Table 4-3 shows the final gain factor result of these two kinds of operation. From this table, we can see that the gain factor of amplifier with autozeroing operation is smaller than

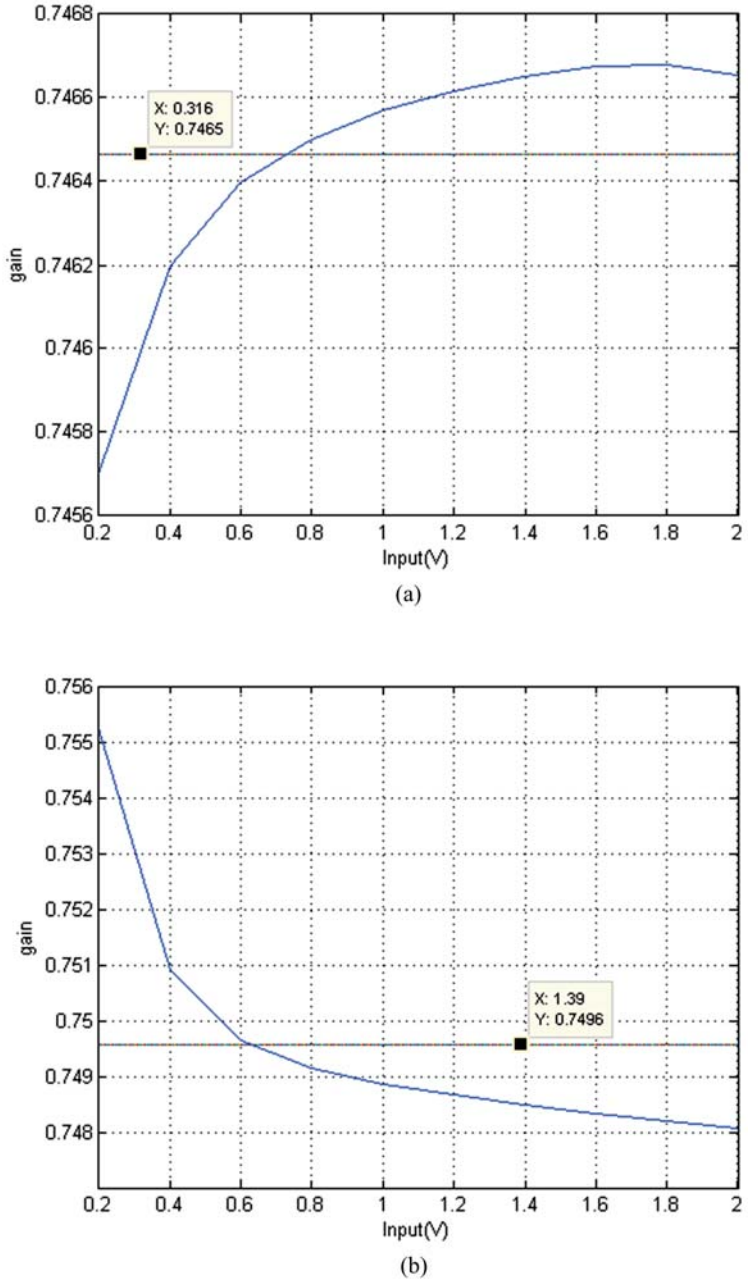

Figure 4-18: (a) Gain factor at 0.75 of the amplifier calculated from the signal at the output of the PGA. (b) Gain factor at 0.75 of the amplifier calculated from the signal at the storage capacitor.

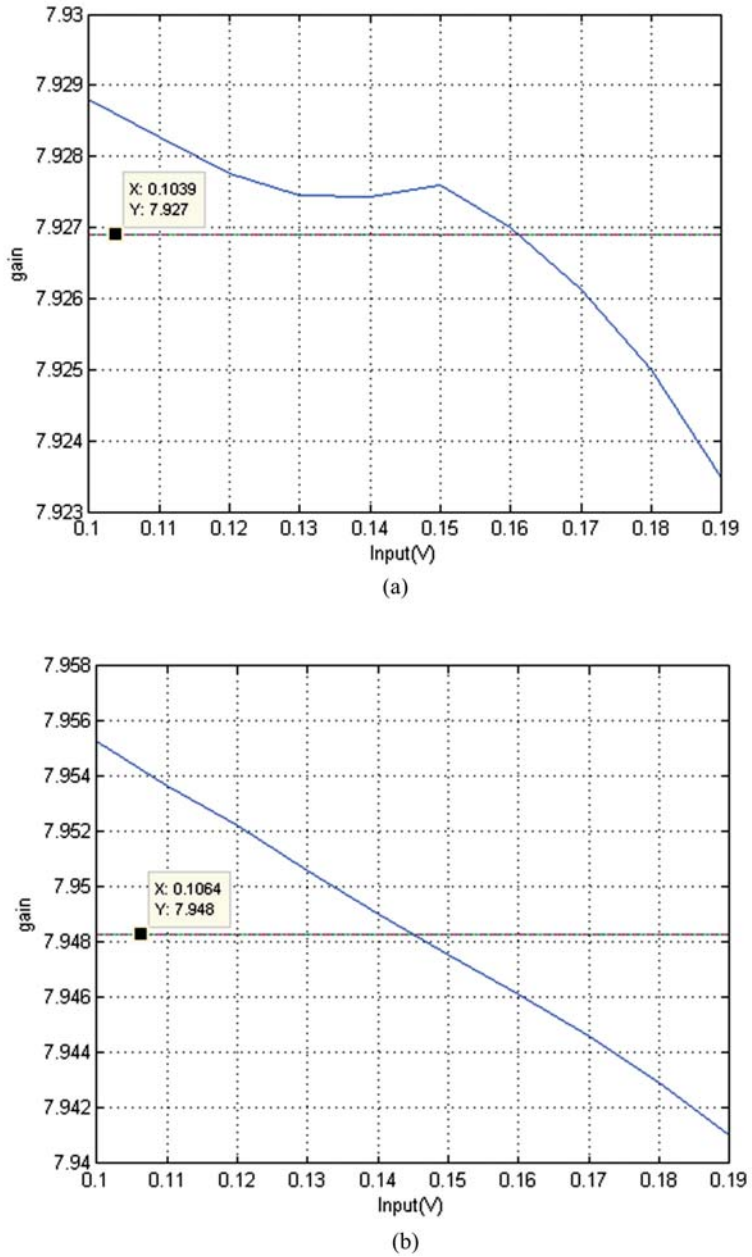

Figure 4-19: (a) Gain factor at 8 of the amplifier calculated from the signal at the output of the PGA. (b) Gain factor at 8 of amplifier calculated from the signal at the storage capacitor.

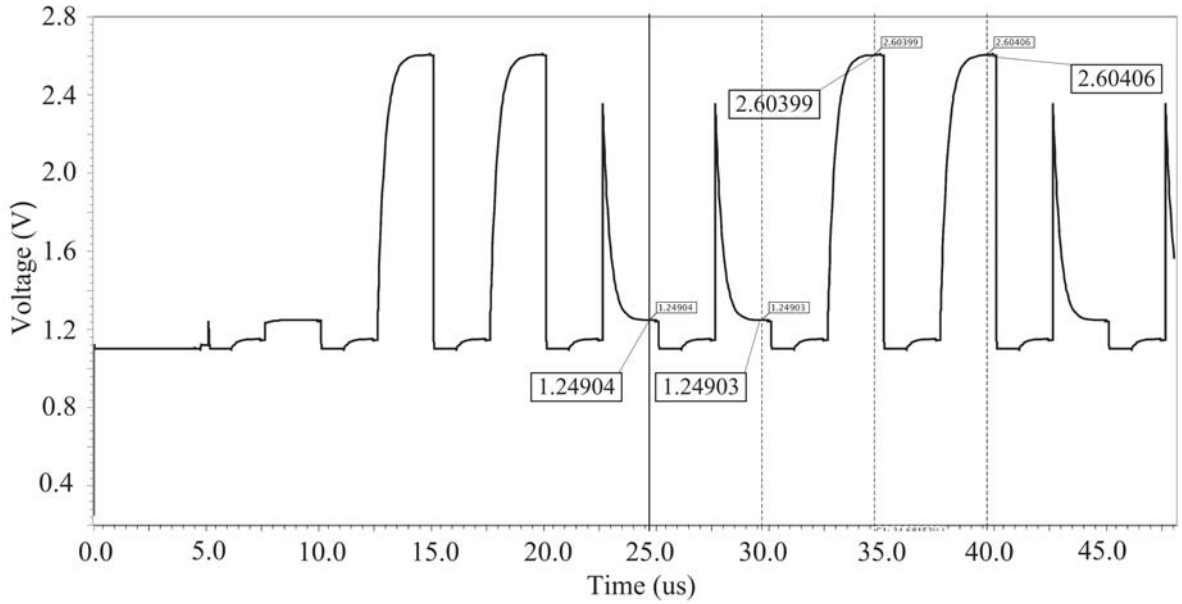

Figure 4-20: Output swing of AFE circuit

than the one with no autozeroing. This is due to the autozero capacitor C_C introduced a large gain error for the amplifier. However, this smaller gain factor is acceptable in our project.

Table 4-3: Gain factor of no autozero and autozero

	No autozeroing	Autozeroing
1	0.75	0.42
2	1.53	1.02
3	1.82	1.33
4	2.59	2.04
5	3.36	2.53
6	3.69	2.87
7	6.22	5.32
8	8.02	7.15

For the corner simulation, the typical (TT), slow (SS) and fast (FF) corners at 27 °C are simulated as well as the typical corner with different temperature (27 °C, 85 °C, −40 °C). Table 4-4 shows the corner analysis of the smallest and largest gain factor.

Table 4-5 gives all performance of the AFE circuit, all of them satisfied the design target.

Table 4-4: Output swing of pixel for corner simulation

Corner	TT 27 °C	FF 27 °C	SS 27 °C	TT 85 °C	TT −40 °C
0.75	0.751	0.735	0.754	0.745	0.747
8	8.02	7.57	8.18	7.86	7.94

Table 4-5: AFE circuit performance

Specification	Parameter	Unit
PGA Gain Setting	×0.75 ×1.53 ×1.82 ×2.59 ×3.36 ×3.69 ×6.22 ×8.02	
Power consumption	9.9	μW
Input referred noise	<200	μV
SNR	>74	dB
Nonlinearity	<0.1	%
Output swing	1.5	V
Max input signal level	2	V
Row sampling time	5	μs

4-3 LVDS driver circuit

4-3-1 LVDS design target specifications

Low Voltage Differential Signaling (LVDS) is a kind of process-technology-independent standard which developed for a low-power, low voltage and high speed I/O interface transmission. By means of a differential scheme, combined with a low voltage swing, it achieves a higher speed transmission and termination as well as a significant power saving [46].

Generally, the LVDS driver circuit, placed at a point (usually on chip) converts a digital logic signal into LVDS differential format. The LVDS receiver circuit placed at the other point (usually on the PCB) will convert this differential signal back into a single ended logic format. The target of this part of work is to design a LVDS driver circuit that can support a minimum of 400Mbps data rate with a 1.5V supply, while meeting all the requirement of the TIA/EIA standard [47]. The main set of specifications given for the current design is shown below.

Here, we give some explanation of short-to-ground current and short-together current. In order to ensure the driver circuit does not damage other parts of circuits and also include itself, we need to check the output circuits when short mutually and to ground.

When the driver terminals are short together to the ground, either current $|I_{SA}|$ or $|I_{SB}|$ should not exceed the specified value in the Table 4-6. The test circuit is as shown in Figure 4-21(a). When the driver terminals are short to each other, the current $|I_{SAB}|$ should not surpass 12mA as shown in Table 4-6. The test circuit is as shown in Figure 4-21(b).

Table 4-6: LVDS driver specifications from TIA/EIA standard [47]

Specification	Min.	Max.	Unit
V_{OD}(Differential voltage swing)	247	454	mV
V_{OS}(Common-mode voltage)	1.125	1.375	V
ΔV_{OD}(Acceptable mismatch on V_{OD})		50	mV
ΔV_{OS}(Acceptable mismatch on V_{OS})		50	mV
t_r,t_f (Rise and fall time)	0.26	1.2	ns
$\lvert I_{SA}\rvert$, $\lvert I_{SB}\rvert$(short-to-ground current)		24	mA
$\lvert I_{SAB}\rvert$(short-together current)		12	mA

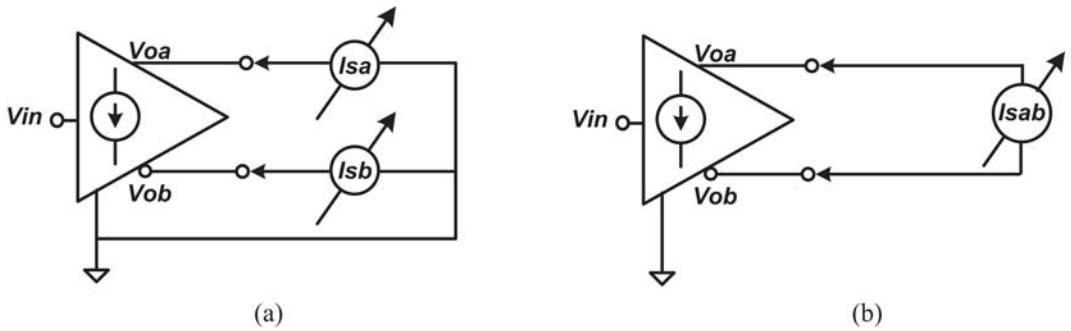

Figure 4-21: (a) Short-to-ground current test circuit (b) short-together current test circuit [47]

4-3-2 Operation principle of LVDS driver

Generally, as seen from Figure 4-22, the LVDS driver can be considered as a current source with a switched polarity for simplicity, whereas the receiver is treated as a comparator with hysteresis which is able to detect a voltage signal at the level of tens of milli-volt.

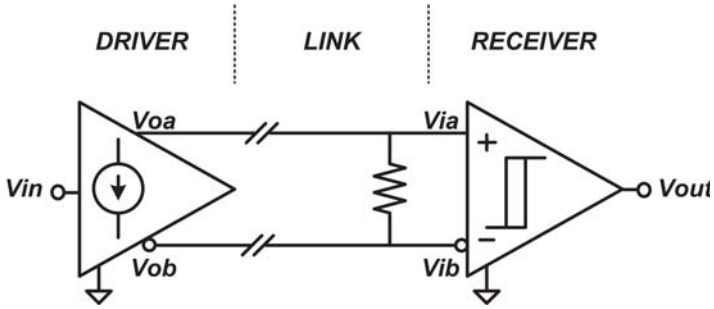

Figure 4-22: LVDS interface

The driver's output current flows through a differential pair lines and a termination resistor R_L. The receiver has a high DC input impedance so the majority of the driver's output current flow across R_L and generates a voltage swing at the receiver input, which can be detected as "one" or "zero" logic state according to the current flow direction.

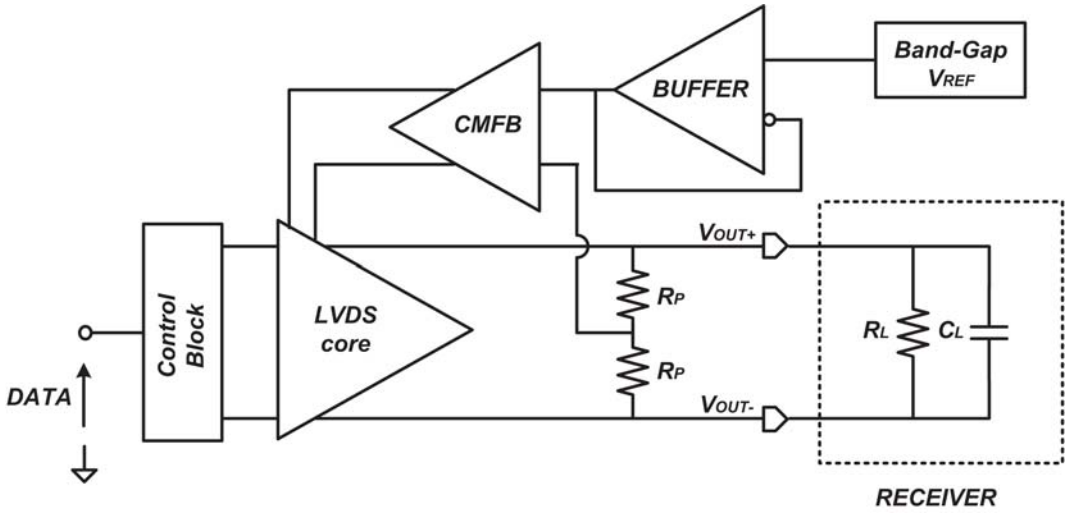

Figure 4-23: LVDS driver architecture

The following functional block can construct a stand-alone LVDS driver:

Control block: splits the signals, which come from the ADC, into two differential schemes and buffers them into the LVDS core.

LVDS core: a current source with switched polarity.

CMFB: the common mode feed back circuit stabilizes the driver's output common mode voltage $V_{CM,LVDS}$ always at the desired value, which is equal to V_{REF}, V_{REF} is the reference voltage generated from Band-gap reference circuit.

Band-gap reference circuit: generates a reference voltage V_{REF}, which should not depend on the temperature. The circuit implementation details can be found in [40].

Buffer: buffers the reference voltage V_{REF} into the CMFB circuit.

4-3-3 Circuit Implementation of LVDS driver

Single-end to differential conversion

Before the signals are feed into the LVDS driver, they should first being split as two aligned and complementary signals. As indicated in Figure 4-23, the input signal $V_{IN,LVDS}$ of LVDS (rising) is divided into two branches and applied to one inverter and one buffer, respectively. The size of the inverter and the buffer should be carefully designed to make the complementary edges aligned coarsely. A pair of cross-coupled inverters is used to synchronize the copies of

rising and falling edges. The output of this single-end to differential conversion circuit are V_{IN-} and V_{IN+}.

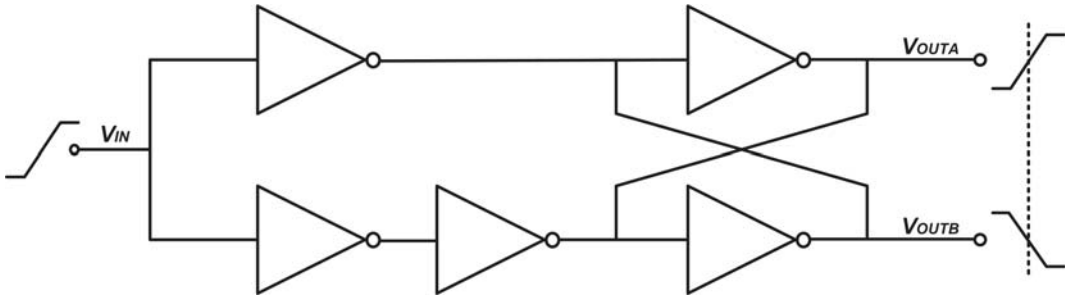

Figure 4-24: Single-end to differential conversion circuit (based on previous design)

Main driver

This project adopts a typical LVDS driver architecture which often is referred to as Bridged-Switched Current Sources (BSCS) architecture. It consists of two current sources M5 and M6 and four MOS switches M1 to M4 connected in bridge configuration as shown in Figure 4-25. Among them, gate M1-M3 and M2-M4 are shorted and controlled by the complementary signals V_{IN-} and V_{IN+}. Appling logic "1" to V_{IN+} and logic "0" to V_{IN-}, switches M2-M3 are on and M1-M4 are off. As a result, the polarity of the output current is positive together with the differential voltage, thus a logic "1" is transmitted.. On the contrary, when the polarity of the output current and voltage are reversed, a logic "0" is transmitted.

A differential load resistor R_L at the receiver end is used for the current-to-voltage conversion as well as to provides an optimum line matching at the same time. For an operation in the megabits-per-second range, an additional termination resistor R_T is usually placed at the driver end to suppress reflected waves caused by crosstalk or by imperfect termination, due to package parasitic and component tolerances [48].

In this design, we force the output common mode voltage to be directly equal to the output voltage of the band-gap reference circuit, which is $V_{CM} = V_{REF} = 1.19$V. Besides, we choose $V_{OD} = 400$mV as the differential voltage swing for this driver. In order to develop a 325mV voltage swing on the nominal 50Ω load resistance ($R_T//R_L$), the bridge must be biased at:

$$I_{BIASP} = I_{BIASN} = \frac{V_{OD}}{50\Omega} = 8\text{mA} \tag{4-30}$$

where I_{BIASP} and I_{BIASN} are the bias current for current source in the main driver.

CMFB

As can be seen from Figure 4-26, in order to achieve a higher precision and a lower circuit complexity, a simple low-power common-mode feedback control was implemented. The

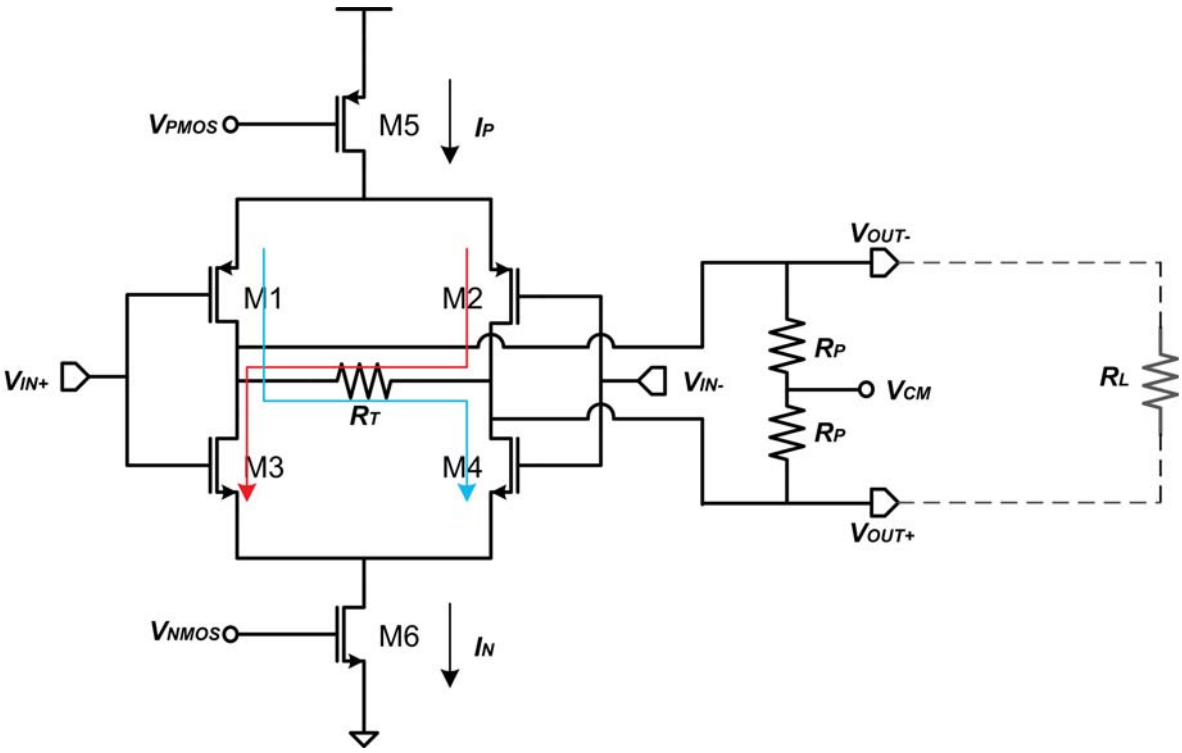

Figure 4-25: LVDS main driver

common-mode output voltage $V_{CM,LVDS}$ at the driver's output is sensed by means of a high resistive divider. The voltage between the two resistor is

$$V_{CM} = \frac{V_{OUT-} + V_{OUT+}}{2} \tag{4-31}$$

where V_{OUT-} and V_{OUT-} are the output of the LVDS main driver. This value is compared with reference voltage V_{REF} by the differential amplifier M7 to M10.

A cascode current mirror is employed in the CMFB circuit to suppress the effect of the channel-length modulation as well as to set the output LVDS driver's current at the desired value. If $V_{CM,LVDS} = V_{REF}$, the current flows through M8-M10 and M7-M9 branches of amplifier are equal. On the contrary, the unequal currents flowing across M9 and M10 are mirrored to the driver transistors M5 and M6 and forcing the $V_{CM,LVDS} = V_{REF}$.

In order to minimize the power consumption of the LVDS driver, we set I_{CMFB} equal to $I_{BIASN}/K = I_{BIASP}/K$, where K is the gain of current mirrors M10-M6 and M9-M5. However, if $I_{CMFB} << I_{BIASN} = I_{BIASP}$, the magnitude of the pole associated with the M10-M12 current mirror decreases as I_{CMFB} decreases. To illustrate this point, we will ignore all capacitors except the gate source capacitors for M10 and M12. Then the magnitude of the non-dominant pole associated with the current mirror is

$$p_{nd} = \frac{g_{m10}}{C_{gs12} + C_{gs10}} = \frac{2I_{D10}/V_{ov10}}{C_{gs12} + 2C_{ox}W_{10}L_{10}/3} \tag{4-32}$$

where g_{m10} is the transconductance of M10, C_{gs12} and C_{gs10} are the gate-source overlap capacitance, I_D10 and V_{ov10} are the drain current and overdrive voltage of M10, W_{10} and L_{10} are the width and length of transistor M10 and C_{ox} is the gate oxide capacitance per unit area.

If $I_{CMFB} = I_{D10}$ is scaled by a factor K, the pole magnitude decreases because the numerator scales by the factor K, but the denominator scales by a factor greater than K due to the constant C_{gs12} term in the denominator. This pole appears in the CMFB loop gain. Therefore, the phase margin of the CMFB loop decreases as this pole magnitude decreases as a result of I_{CMFB} reduction. In order to reduce this effect, we introduce a capacitor C_1 . This capacitor is connected in parallel with each sense resistor to introduce a left half plane zero in the CMFB loop and compensates the non-dominant pole p_{nd}. Figure 4-27 shows the stability performance of the CMFB circuit in the LVDS driver. From this figure, we can see that the phase margin is larger than 50°, which is satisfy the requirement of stability.

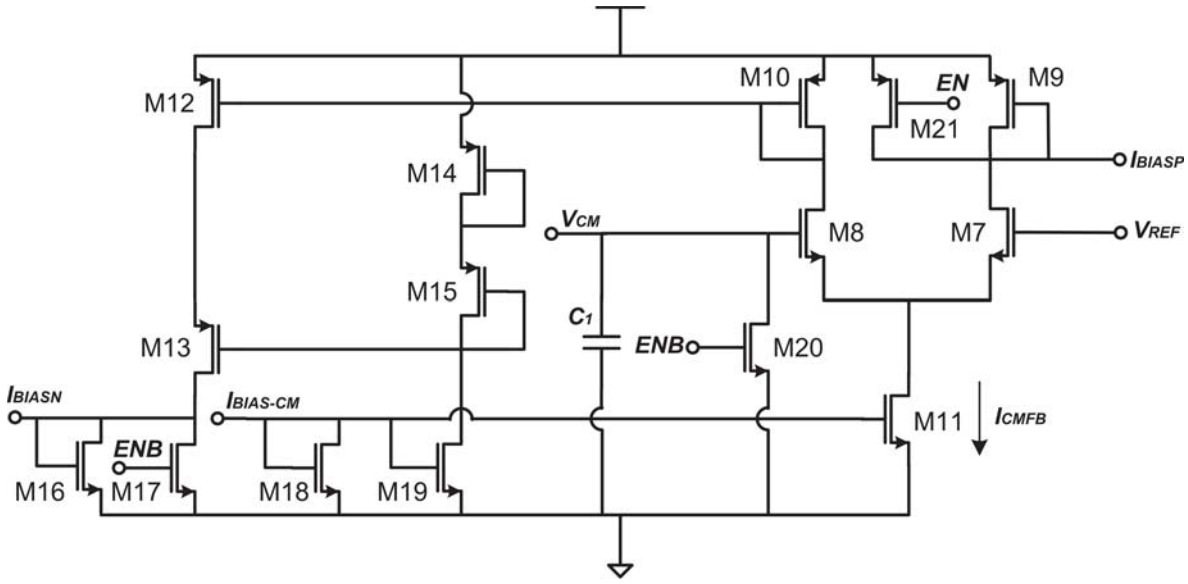

Figure 4-26: CMFB circuit (based on previous design)

4-3-4 Simulation result of LVDS driver

To verify the feasibility of a 400Mbps LVDS driver in the selected process and to get an idea of the power dissipation, the LVDS driver is simulated with the estimated parasitics as shown in Figure 4-28. As transmission line a $10cm$ long, micro strip line model with an impedance of 50Ω is used.

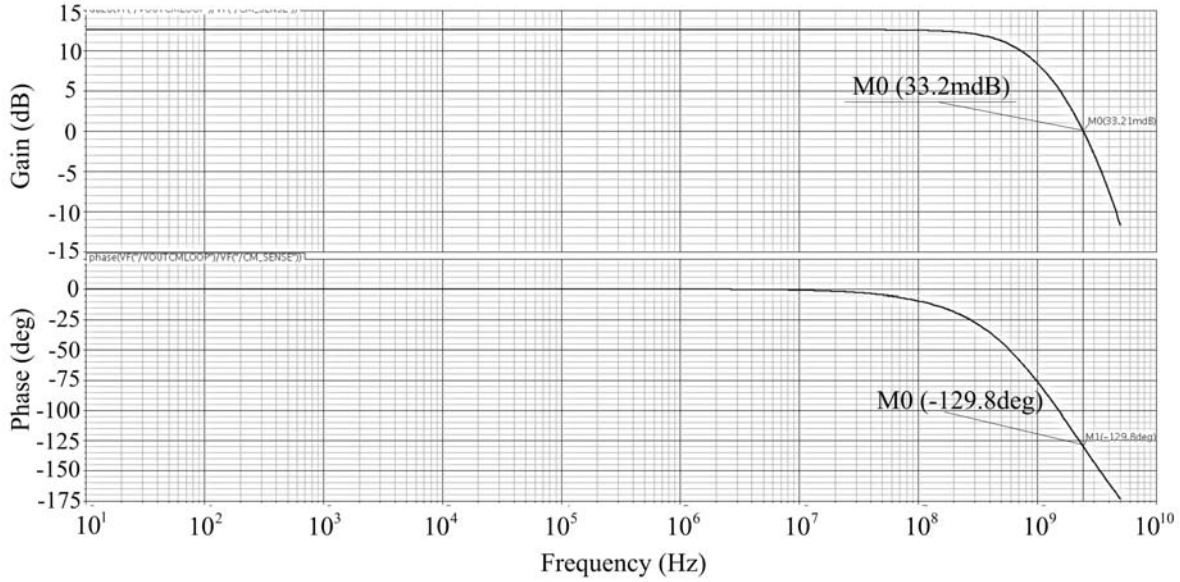

Figure 4-27: Stability analysis for LVDS main driver and CMFB circuit

Figure 4-29 and Figure 4-30 presents the output swing and differential output signal of the LVDS driver. From these figures we can see that the differential output swing is around $390mV$, which is satisfy the LVDS design specifications.

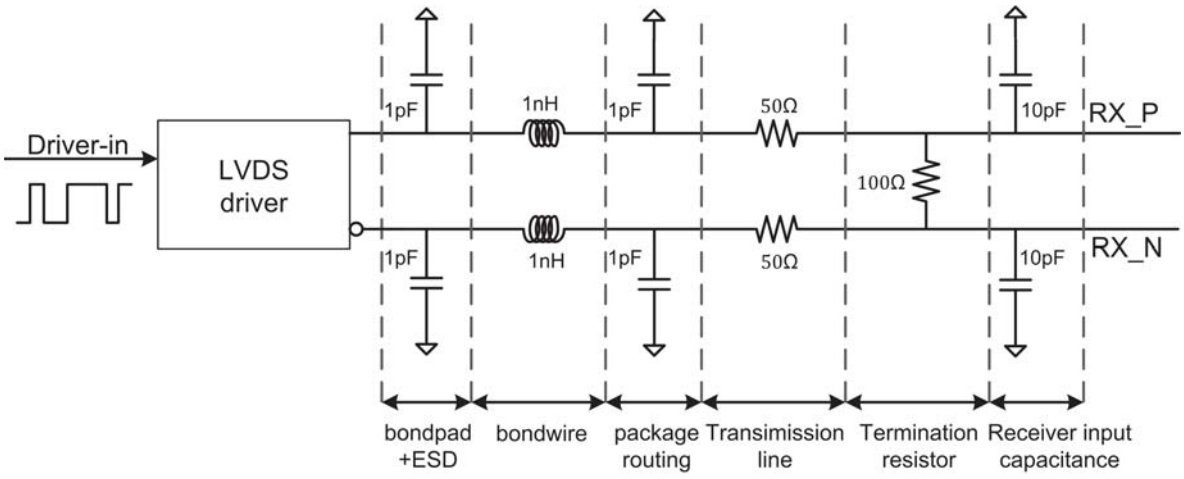

Figure 4-28: LVDS driver simulation model

Figure 4-31 shows the short-to-ground current $|I_{SA}|$ and $|I_{SB}|$. From this figure, we can see that the measured currents are smaller than $12mA$, the specified value. So they are satisfy

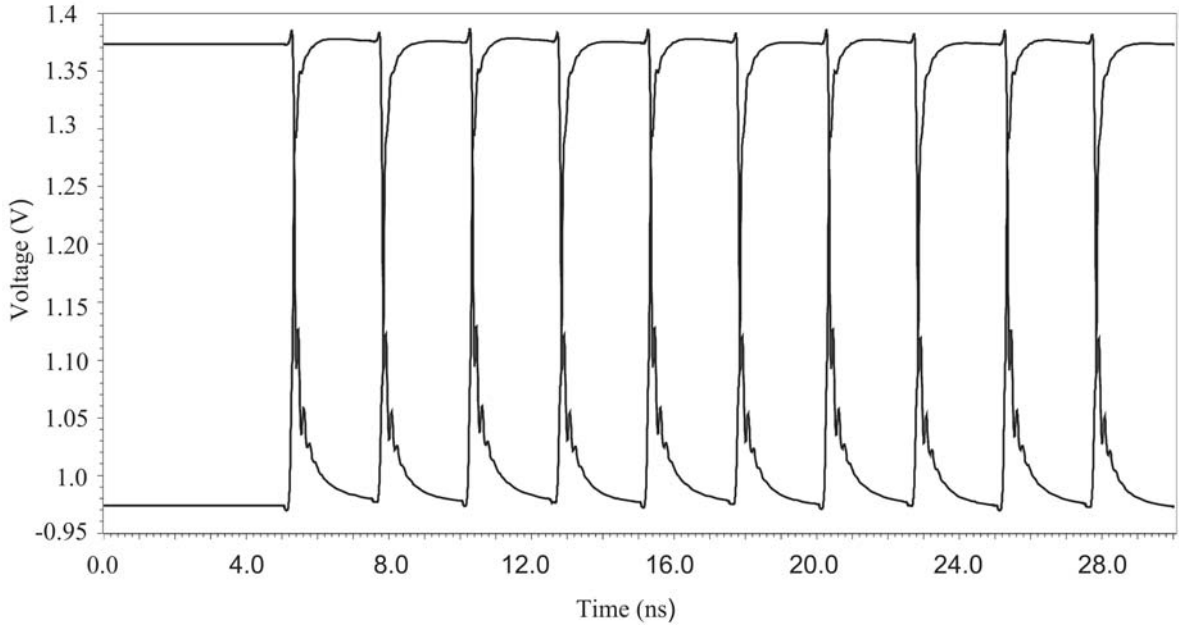

Figure 4-29: Output swing of the LVDS driver

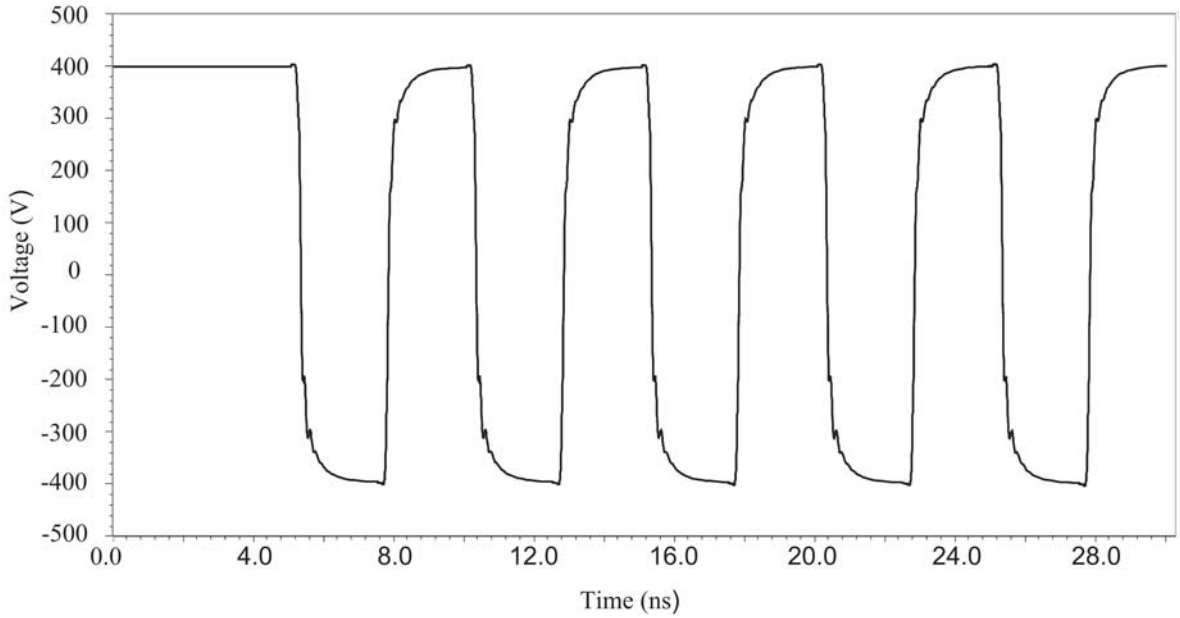

Figure 4-30: Differential swing of the LVDS driver

the standard. Figure 4-32 shows the short-together current $|I_{SAB}|$, the current here is much smaller than the specified Max. value, thus, it also meets our requirement.

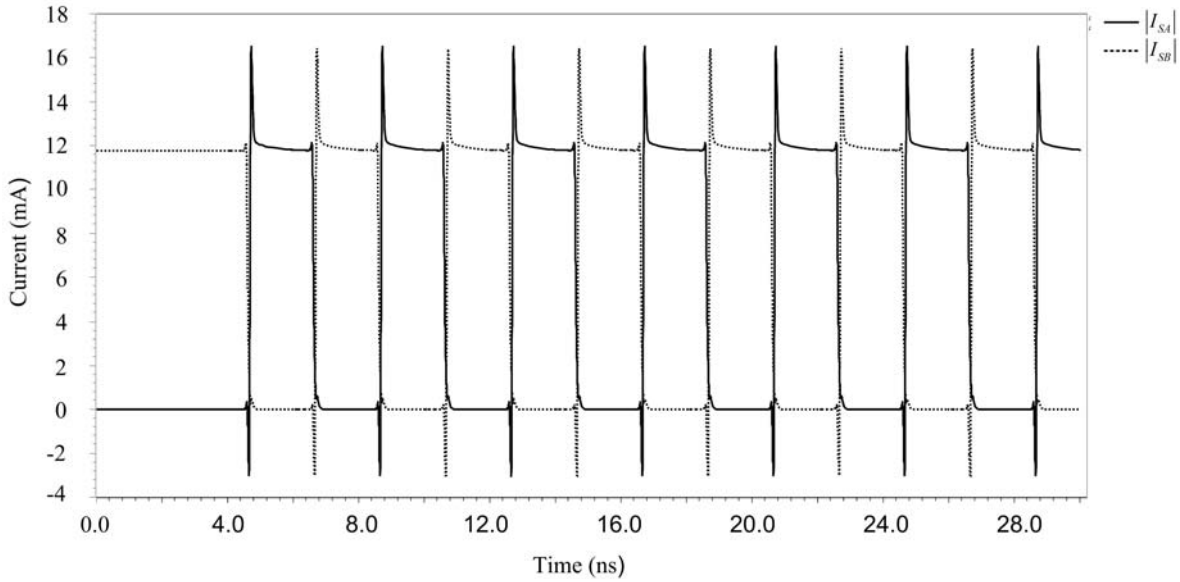

Figure 4-31: Short-to-ground current

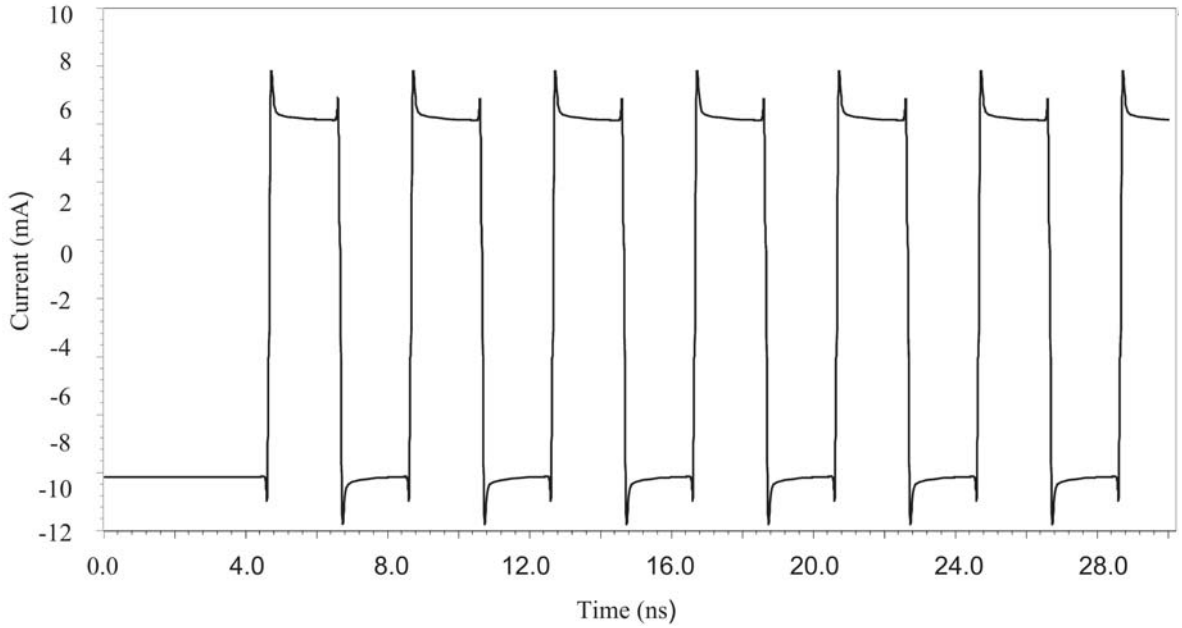

Figure 4-32: Short-together current

For the corner simulation, the typical (TT), slow (SS) and fast (FF) corners at 27 °C are simulated as well as the typical corner with different temperature (27 °C, 85 °C, −40 °C). Table 4-7shows the corner analysis of differential output swing of LVDS driver.

Table 4-7: Corner analysis of LVDS circuit

Corner	TT 27 °C	FF 27 °C	SS 27 °C	TT 85 °C	TT −40 °C
V_{OD}	390mV	417mV	352mV	379mV	414mV

Table 4-8 gives an overview of the performance parameters of the LVDS circuit. All of them meet the target specification which we given previously.

Table 4-8: LVDS driver performance

Specification	Parameter	Unit
Data rate	400 ($C_p = 10$pF)	Mbps
Common mode stability	Phase margin $> 50\circ$	
V_{OD} (Differential voltage swing)	390	mV
V_{CM} common mode voltage	1.19 (from band gap reference)	V
$\lvert I_{SA}\rvert, \lvert I_{SB}\rvert$	12	mA
$\lvert I_{SAB}\rvert$	6.5	mA
Static current consumption	8	mA
Static power consumption	12	mW
Rise/fall time	382/340	ps

4-4 Conclusion

In this chapter, we first introduced the whole readout chain architecture and their functions. Next, the analog front end circuit operation and implementation was explained and the transistor level implementations are presented in details. Then, the simulation results of the circuit level design have been analyzed which including signal amplitude, noise, linearity and SNR. We found that the simulated results all match well with the target specifications. Then, the description of the standard and the design of a stand-alone LVDS driver is presented. Due to the project requirements, the bridged switched current sources LVDS core's architecture was chosen. In this LVDS driver design, we also paid some attention on the stability of the common mode feedback and the LVDS core. In order to minimize the dynamic current consumption, the appropriate transistor scaling used in CMFB circuit is adopted.

Chapter 5

Conclusion

5-1 Contribution of this thesis

This work consists of the design of an 8T global shutter pixel, the analog front end circuit and the LVDS driver. The main contributions of this work are:

1. A pixel which consists of eight transistors with $4.8\mu m$ pitch was developed in this thesis. This architecture supports both the pipeline global shutter operation and the correlated double sampling. During the Frame Overhead Time (FOT), the pixel stores the reset level signal into one in-pixel capacitor, after the charge transfer, the video level signal is stored in another in-pixel capacitor with the same capacity as the former one. During CDS, the two storage levels are subtracted from each other and the correlated reset noise is eliminated. Thus, a higher frame rate can be obtained and the noise of the pixel is significantly reduced. Furthermore, since the voltage leak due to the Parasitic light sensitivity (PLS) on the two capacitors is the same, this undesired effect will also be subtracted during CDS. As a result, a high shutter efficiency can be achieved. In this thesis, various types of noise generated in the pixel were analyzed. For flicker noise and kTC noise, a noise model was constructed based on assuming the gain of source follower is unity and the switches are ideal. The pixel layout and operation voltage levels were optimized to increase the pixel quantum efficiency, charge transfer and to decrease the dark current and noise level. What's more, two current sources were implemented on the column bus, in order to keep a fast readout speed as well as a relatively large voltage swing. Some primitive pixel simulation results are also given in the thesis. From these results, we can coarsely estimate the voltage swing and readout speed of the pixel. By calculating the MOS device capacitors and extracting the pixel layout, we can build the lumped RC model for the pixel array. With the help of these models, the row logic circuit was optimized and the offset, which is induced from the large RC delay, can be reduced significantly.

2. The column analog front end circuit which contains the Programmable Gain Amplifier (PGA) and Sample and Hold (S/H) stage was implemented in this thesis. Studies

and analysis have been made at architecture level to investigate at first the design choice. Then, the circuit level implementations are presented in the thesis in detail. Considering the area efficiency, we use a simple differential amplifier to achieve the required performance. What's more, we have applied low leakage switches to improve the performance and switchable feedback capacitors to increase the design flexibility. The simulation results of the circuit level design have been analyzed in terms of signal amplitude, noise, linearity and SNR. We found that the simulated results all match well with target specifications.

3. The description of the standard and the design of a stand-alone LVDS driver, which is fully compatible with the IEEE specification, is presented. Due to the project requirements, the bridged switched current sources LVDS core's architecture was chosen. The attention was paid to the stability of the common mode feedback and the LVDS core. To minimize the static current consumption, the appropriate transistor scaling used in CMFB circuit is recommended. The designed LVDS driver is characterized by a static power dissipation of 8mW at the data rate 400Mb/s for capacitive load equal to 10pF.

5-2 Future work

There is always room for improvements and several things should be studied in the future. The expected future work can be categorized into four aspects:

1. The pixel noise aspect: It is worth to notice that in the scope of this thesis, the operation of the pixel has been separated in two modes: low noise mode which reads out the video level while keeping S2 on; and high noise mode which opens the switch S2 and holds the video level in C2 first and then reads out. In our noise analysis model, we simply consider that the thermal noise generated from the switch S2 is all presented in C2 for the high noise mode and no kTC noise is present on C2 for low noise mode. However, in theory, no matter whether switch S2 is on or off, if two in-pixel capacitors are completely equal, the kTC noise presented on both capacitors should be equal to 0.5kTC [49], which means two modes should have the same kTC noise. Yet, compared to previous measurements of the same pixel architecture in a 5.5μm pitch, the noise model described in this thesis, especially with respect to the low-noise mode is not accurate enough. Thus, further investigation and refinement needs to be done.

2. The AFE design aspect: In our design, although the op-amp structure used for the AFE design is very simple, it still consumes a relative large area. We can continue to optimize the op-amp structure and the layout to reduce its area in the future. What's more, the noise performance of the PGA is just enough to meet the specification (input referred noise of the amplifier is smaller than the pixel noise at unity gain). Further optimization can be adopted to the amplifier to reduce the noise such as decreasing the noise bandwidth. Regarding the sampling speed, in our design, the Row Readout Time (ROT) is about 5μs. As is known, the shorter sampling interval time, the lower the flicker noise. Thus, the speed for this AFE circuit can also be optimized. However, it should be noticed here, although the larger bandwidth improves the speed performance, it also enlarges the noise bandwidth at the same time which leads to a higher integrated

thermal noise. Thus, a much more careful tradeoff between speed and noise performance should get more attention.

3. The LVDS design aspect: The LVDS driver in this project is adopting the typical bridged switches structure. It is simple and only needs a minimum static current consumption to generate the required output signal swing. However, due to the finite on-resistance of the pMOS transistor switches and the large amount of current flowing through the switches, the headroom in VDD direction is very small and thus the pMOS current source transistors are very wide. Therefore, some other topologies like double current sources architecture [50], open drain architecture [51], and switchable current sources architecture [52] can also be an option for a future improved design.

4. The top level aspect: Due to the limited time, the top level circuit and layout has not been finished yet. For the pixel array, we just implemented a small 3×3 pixel array to do DRC, LVS and validation, it still waiting to be implemented in 1280×1024 array and protected by means of a guard ring. For the column readout chain circuits and their bias circuits, they still need to be put together to do the complete simulation and validation. The SPI and the X shift register also haven't been taken care of, they still require a significant effort to complete..

Appendix A

The Back of the Thesis

A-1 Analog Front-End (AFE) circuit layout

An example layout of 128-column the AFE circuit is illustrated in Figure A-1, the width is 614.4μm and the length is 560.5μm

A-2 Low Voltage Differential Signaling (LVDS) circuit layout

The layout of LVDS is shown in Figure A-2, which occupies an area of 161.656μm $\times$ 82.373 μm.

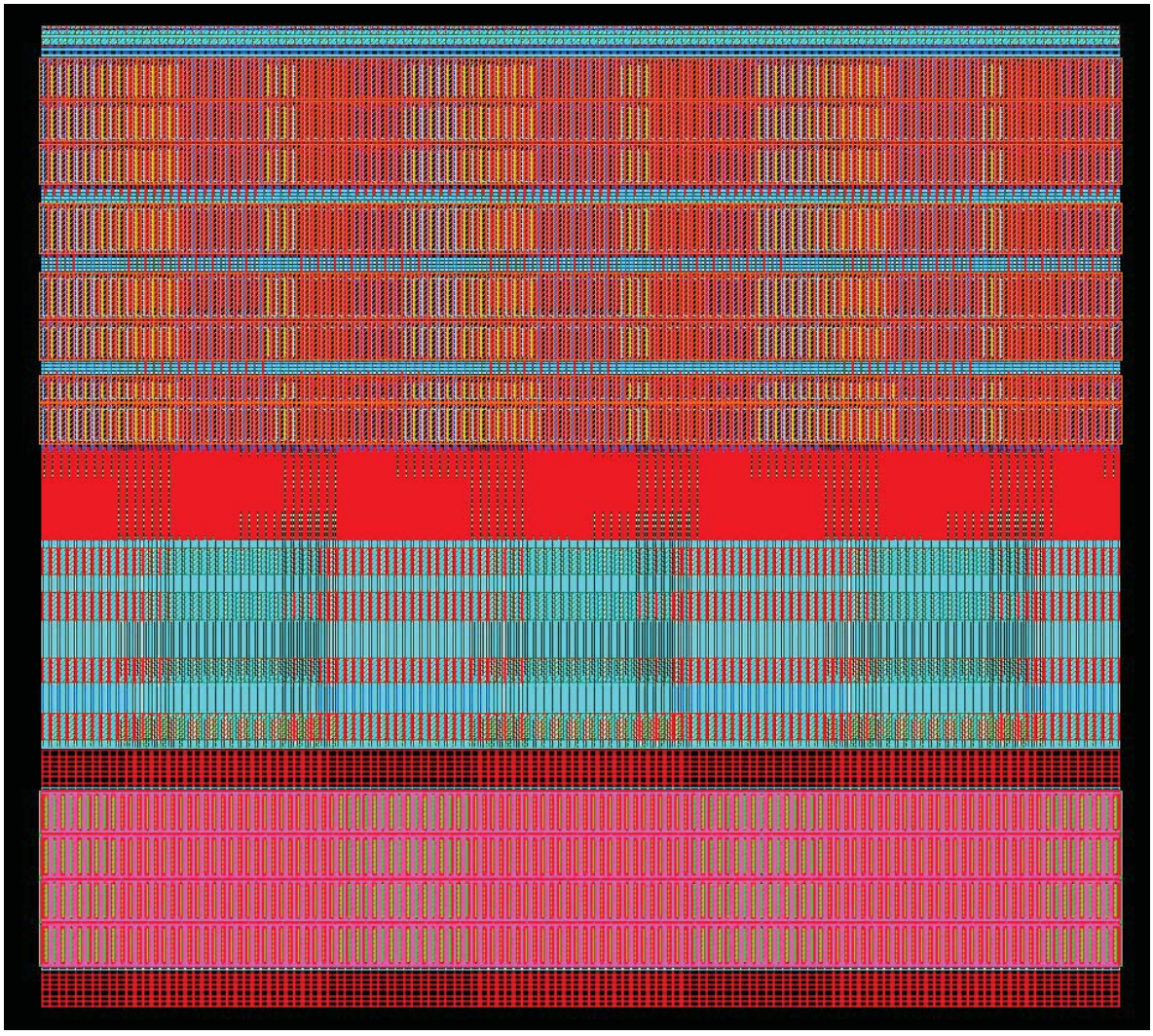

Figure A-1: Layout of the AFE circuit

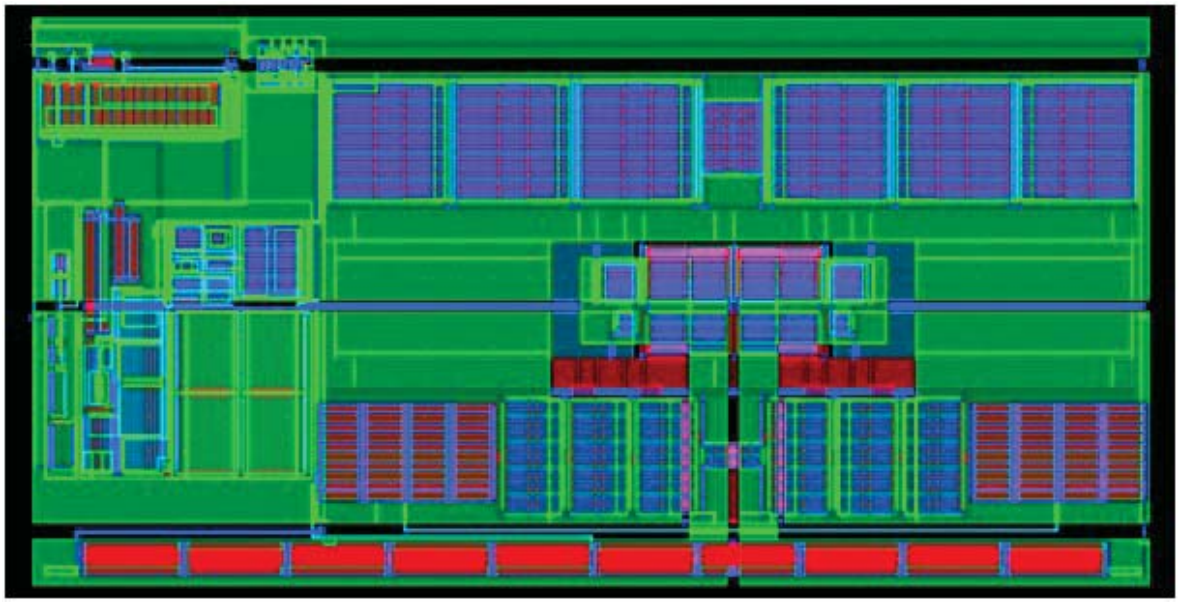

Figure A-2: Layout of the LVDS circuit

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Glossary

List of Acronyms

ADC	Analog-to-Digital Conversion
AFE	Analog Front-End
APS	Active Pixel Sensor
CAGR	Compound Annual Growth Rate
CCD	Charge-coupled Device
CDS	Correlated Double Sampling
CG	conversion gain
CMOS	Complementary Metal-Oxide-Semiconductor
DR	Dynamic Range
DS	Double Sampling
DSNU	Dark Signal Non-Uniformity
FD	Floating Diffusion
FOT	Frame Overhead Time
FPN	Fixed Pattern Noise
FWC	Full Well Capacity
GSE	Global shutter efficiency
HDR	High Dynamic Range
LVDS	Low Voltage Differential Signaling
PGA	Programmable Gain Amplifier

PLS	Parasitic light sensitivity
PPD	Pinned Photodiode
PPS	Passive Pixel Sensor
PRNU	Photo Response Non-Uniformity
PSD	Power Spectral Density
PWL	Piecewise Linear
QE	Quantum efficiency
RBT	Row Blanking Time
ROT	Row Readout Time
SCE	Short-Channel Effect
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
STI	Shallow Trench Isolation
S/H	Sample and Hold