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Modeling and Analysis of Aging Impact on SRAM PUFs for Advanced FinFET Technology Nodes

Shayesteh Masoumian[1], Roel Maes[2], Noemie Beringuier-Boher[2], Karthik Keni Yerriswamy[2], Geert-Jan Schrijen[2]
Said Hamdioui[1], Mottaqiallah Taouil[1]
[1]Delft University of Technology, Faculty of EE, Mathematics and CS, Delft, The Netherlands
[2]Synopsys Netherlands B.V., Eindhoven, The Netherlands

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***Abstract*—SRAM Physical Unclonable Functions (PUFs) serve as security primitives and can be used to generate random and unique identifiers, which makes their reliability crucial. The reliability is affected by aging and in particular Bias Temperature Instability (BTI), which in turn affects the PUF responses over time typically measured by the Hamming distance (HD). In this work, we model the BTI impact on SRAM PUF reliability for 14 nm FinFET technology and evaluate the reliability of SRAM PUFs using both simulation and silicon measurements. Additionally, we explore the effectiveness of an anti-aging technique on SRAM PUF reliability. Our simulation model and results (which include process variation and circuit noise) are validated with silicon measurements. From them we conclude the following: 1) there exists a direct correlation between BTI and the Hamming distance of an SRAM PUF, where its reliability decreases with 6% over a 6-month period due to aging, and 2) applying anti-aging patterns improves the Hamming distance and hence the reliability with 3% over a 6-month period.**

***Index Terms*—Anti-aging, BTI, FinFET, SRAM PUF.**

I. Introduction

PUFs are fundamental components in hardware security able to generate unique identifiers and keys due to their distinctive and unclonable properties [1, 2]. Among various PUF implementations, Static Random Access Memory (SRAM) PUFs are widely used. SRAM PUFs can be derived from existing SRAM devices by leveraging the inherent random start-up values. Technological advancements, such as the transition to FinFET technology, affect the SRAM PUF behavior both at enrollment and during lifetime. Hence, it is imperative to assess the security and reliability of SRAM PUFs while considering degradation such as Bias Temperature Instability (BTI) [3].

Although several studies have explored the BTI impact on SRAM cells for read/write operations [4–6], limited studies specifically looked at the impact on SRAM PUFs [7–12]. The impact of aging on SRAM PUFs is primarily researched for planar CMOS technologies. It is shown that Negative BTI (NBTI) causes gradual reliability degradation over time, with the fractional HD (FHD) remaining below 14% in 90nm and below 8% in 65nm after several years [7, 8, 11, 12]. To compensate for the BTI impact, anti-aging techniques were introduced in [9] by writing the inverse enrollment values to the SRAM cells. With respect to FinFET based PUFs, limited work has been published with most studies focusing on stability and reliability while not considering the impact of aging [13, 14]. However, the authors in [10] demonstrated that aging leads to bit shifts and decreased reliability in 28nm planar and 16nm FinFET SRAM PUF measurements, with a larger effect in the 16nm design [10]. Although previous works characterized PUFs using silicon measurements, they lack a proper simulation framework that can predict the impact of aging. Given the higher degradation in FinFET memories [5, 6], accurate simulation models are crucial for assessing long-term behavior and anti-aging patterns.

To the best of our knowledge, this is the first paper that provides an aging simulation framework for FinFET-based PUFs. Using our model, we are able to predict the reliability of SRAM PUFs for different conditions such as supply voltage, ramp-up time, temperature impact and technology node under the presence of circuit noise. The main contributions of this paper are: (1) development of a simulation model to assess aging and anti-aging effects on FinFET SRAM PUF in 14nm technology. (2) modeling of the impact of ramp-up time on FinFET SRAM PUF considering aging and anti-aging effects. (3) validation of the simulation model through comparison with corresponding silicon measurements.

The rest of the paper is organized as follows. Section II provides background on SRAM PUFs. Section III presents the simulation framework and results on the impact of anti-aging patterns on SRAM PUFs. Section IV discusses the silicon results and validates the simulation outcomes. Finally, Section V discusses the results and concludes this paper.

II. Background

In this section, we provide a background on SRAM PUFs, followed by sources that influence the start-up values (SUVs) and PUF evaluation metrics.

SRAM PUF: The SRAM PUF comprises six transistors two pFET pull-up, two nFET pull-down, and two nFET access transistors. The pFETs in cross-coupled inverters work with the nFETs to determine the SUV. During operation, only one transistor pairs remains active. However, at startup both sets experience competing currents which influence the final SUV.

Process variation: Due to process variation, each transistor has slightly different characteristics. The key affected parameters for FinFET devices are (i) fin height, (ii) channel length, (iii) oxide thickness, and (iv) gate work function [15]. Together

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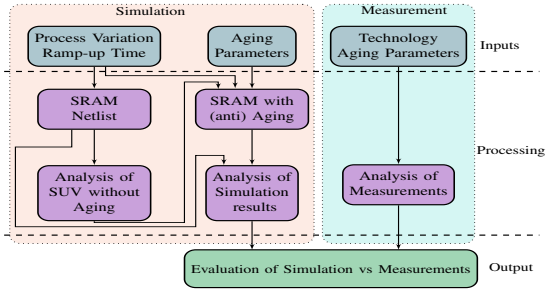

Fig. 1. Simulation Framework for the Validation Process

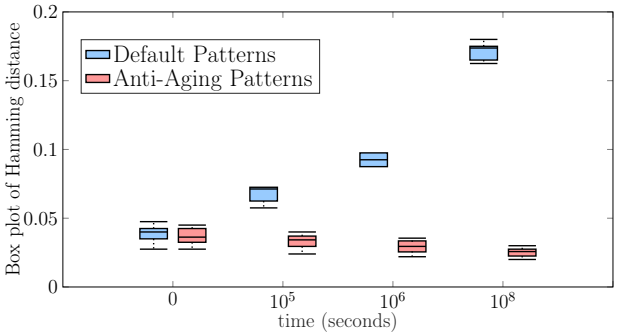

Fig. 2. FHD of Aged Cells With Default and Anti-Aging Patterns

they have an impact on the electrical behavior, e.g., on the V_{th} and drain current. An SRAM PUF utilizes these variations to create unique and physically unclonable sets of SUVs.

Environmental Noise: The repeatability of the SUVs is impacted by temperature, which impacts the transistor's performance and noise. Typical noise sources are the power supply and circuit; they impact mostly the weakly skewed cells. To deal with this, error correction codes (ECCs) are used.

Aging: Aging also impacts the SRAM PUF SUVs over time. In particular BTI, which is a dominant aging source that affects mostly PMOS transistors due to NBTI but also NMOS transistors due to Positive BTI (PTBI) [16, 17]. One of the main models to estimate BTI impact is the Atomistic Trap-Based BTI model [18]; it models NBTI/PBTI impact by modifying V_{th}. Aging due to BTI is accelerated with increased temperatures and supply voltages. The acceleration factor is calculated as follows [9]:

$$AF = (\frac{V_{stress}}{V_{nominal}})^{\frac{\alpha}{n}} \times exp(\frac{E_{aa}}{k} \times (\frac{1}{T_{stress}} - \frac{1}{T_{nominal}}) \times \frac{1}{n}) \quad (1)$$

where α=3.5 represents the gate voltage exponent, n=0.25 the time exponent, E_{aa}=$-0.02eV$ the apparent activation energy, and k=$8.62 \times 10^{-5} eV/K$ Boltzmann's constant.

Anti-Aging Patterns: Aging impacts the transistor's V_{th}, potentially affecting future SUVs after power-up. To counter this, reverse patterns are stored after each power cycle, weakening the transistor pair responsible for the complementary SUV and improving SUV reliability [9]. Although this counteracts the aging effects, some noise remains and ECC is still required.

Reliability metrics: To evaluate the reliability of the PUF, we use the Hamming distance (HD) and the cell skewness. We define the cell skewness based on the probability of an SUV being one or zero across varying conditions. Cells are strongly skewed if their SUV probability exceeds 80%, and otherwise weakly skewed. Weakly skewed cells could relatively easily be affected by noise. Finally, we use the Intra-PUF FHD [9] to measure the fractional HD between multiple evaluations for the same SRAM PUF device as compared to enrollment.

III. Simulation Results

In this section, we describe the simulation setup and results. The simulation framework and validation process are shown in Fig. 1. The PUF is based on a 6T SRAM cells with minimal dimensions. Our simulation model consists of 400 SRAM cells, incorporating the process variation and aging models described in Section II. Process variation is modeled by varying the four key physical parameters of the FinFETs, i.e., the channel length, fin thickness, oxide thickness, and gate work function. We modeled their variation using normal distributions with their nominal value as mean and standard deviations equal to 4% of the mean for the channel length L, fin thickness ($tfin$) and oxide thickness (tox), and 1.3% for gate work function (ϕ) [19]. The transistors are simulated using the PTM 14nm library [20].

With respect to aging, we consider BTI impact for two scenarios: applying (i) default and (ii) anti-aging patterns. In default patterns, cells retain their start-up value during aging. In anti-aging patterns, the inverted SUVs are stored instead. We use the BTI model described in Section II to evaluate both scenarios. For each transistor, we determine the aging activity factor (i.e., the duty cycle) based on the value each cell stores. Based on the SUV, the duty cycle is set to 0.99 for the transistor pair that is activated and 0.01 for the other pair. The junction temperature is set to 75°C (which is similar to the temperature used to accelerate aging for the silicon results). To simulate the start-up behavior of the SRAM PUF, the supply voltage is set to the nominal value. The default ramp-up time is considered to be 10 μs. We also performed experiments where the ramp-up time is varied between 1 μs and 50 μs. Finally, circuit noise is modeled using internal HSPICE and Spectre noise models. For each cell, we simulate 20 different noise samples per cell and measure for each of them the SUVs.

Impact of default and anti-aging patterns on HD: The results of the impact of aging on HD of the SRAM SUVs are shown in Fig. 2. From this figure, it can be concluded that with aging the HD of SUVs over time either improves or degrades depending on whether anti-aging patterns are applied or not. The lower the FHD, the more reliable the SUV of a cell is. The difference between the default and anti-aging patterns is significant. In case anti-aging patterns are applied, the ECC correction required for the PUF in this figure reduces from 17.5% of the cells to 4.5% of the cells.

Impact of aging on Strong cells: Fig. 3(a) shows the impact of aging on strongly skewed cells when default and anti-aging patterns are applied. Note that sometimes weakly skewed cells are removed from the PUF response to reduce the required amount of ECC [21]. The red and blue plots show the impact of default and anti-aging patterns respectively. When anti-aging patterns are applied, the number of strongly skewed

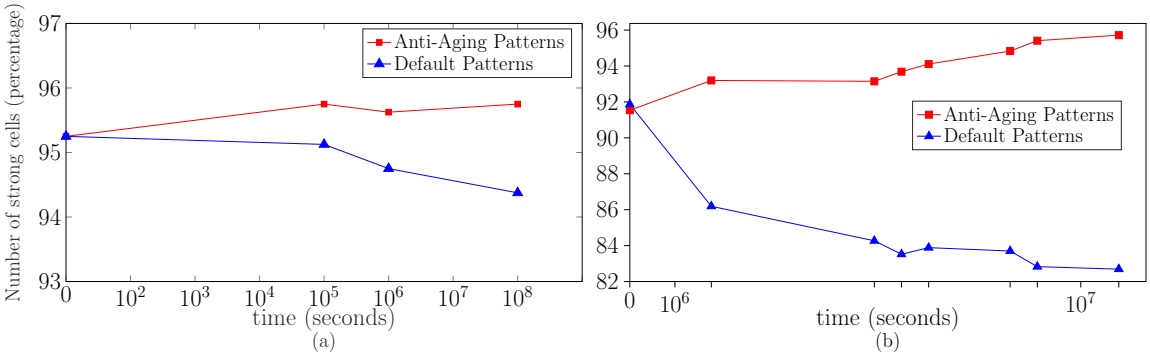

Fig. 3. Aging of Strong Cells With Default and Anti-Aging patterns using (a) simulation results (b) Silicon Measurements

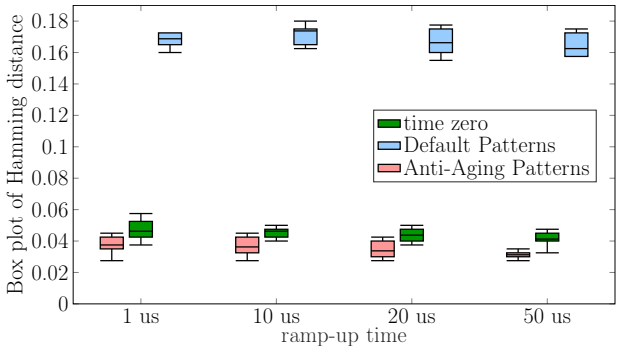

Fig. 4. Simulated Impact of Ramp-Up Time and Aging on HD

SRAM cells increases. This means that when we measure the SRAM PUF response multiple times, the SUVs tend to match better with the enrollment values (i.e., lower HD). When the default patterns are applied, the amount of strong cells reduces over time and hence more ECC is required, which can be explained again using the transistor pairs. The pair responsible for the SUV weakens over time and hence some strong cells (with a lot of skew) become weaker (i.e., less skewed).

Impact of Ramp-Up Time: Fig. 4 shows the impact of the ramp-up time (i.e., 1 us, 10 us, 20 us and 50us) for cells that are aged with the default and anti-aging patterns for a period of 3 years. Increasing the ramp-up time generally leads to a slightly lower FHD of SUVs compared to the enrollment SUVs, as it is less influenced by noise. This trend is consistent when both default and anti-aging patterns are applied. The impact is in general marginal and differences compared to time zero are mostly due to the aging pattern.

IV. Silicon Results

In this section, we present the silicon results for measurements of 14nm SRAM PUFs. We measured the impact of aging by applying both default and anti-aging patterns. We measure the PUF responses on two commercial boards [22], each containing two 14nm memories of which we have used 3KB for the experiments: On Chip RAM (OCRAM) and Tightly-Coupled Memory (TCM). We repeat 10 measurements per cell for each condition (e.g., different temperature). The goal of the measurements is to quantify the HD and number of strong bits at various stress times.

Before aging, the start-up values (SUVs) of the SRAM device are first measured as a reference mimicking the enrollment phase. To accelerate the aging impact, the temperature is raised to 75°C, and the SRAM retains its value for a specific duration. Thereafter, the SUVs are measured again at room temperature, i.e., 25°C. Given the above procedure and conditions, we can determine that AF equals to 1.56 for our experiments.

Impact of Default and Anti-Aging Patterns on Hamming Distance: The silicon measurement results for the HD relative to the enrollment measurement for the two boards each with two different memories are depicted in Fig. 5. The subfigures show for the different boards the FHD of the PUF responses for accelerated aging periods expressed in weeks. It is evident that the HD of all devices increases when default patterns are applied and decreases when anti-aging patterns are applied. This trend can be attributed to the change of V_{th} due to BTI in the stressed transistors of the cross-coupled inverters. Oppositely, when the anti-aging patterns are applied, the opposite transistors of the cross-coupled inverters are aged. This increases the skewness of the cells, lowers the HD, and hence, improves the reliability. At time zero, when no aging occurred there is of course no difference between applying both the default and anti-aging patterns. The small difference between their box-plots at time zero is a consequence of noise in the measurements.

Impact of aging on Strong cells: The silicon measurement results for the number of strong bits for chip 2/TCM, are shown in Fig. 3(b); we observed similar trends in all four sub-memories and hence only include the plot for this chip. The figure shows that the number of strong bits decreases over time when default patterns are applied due to decreasing asymmetry of the cells. Conversely, the number of strong bits increases when the anti-aging patterns are applied. The trends between simulation and measurements are quite similar although the simulation setup uses a different transistor model, noise models, aging model etc. as compared to the silicon result. Nevertheless, the trends are quite similar.

V. Discussion and Conclusion

This work analyzed the impact of aging on SRAM PUF in 14nm FinFET technology. To the best of our knowledge, this paper presents, for the first time in the literature a simulation model that analyzes the aging impact for FinFET-based SRAM PUFs. From the results, we conclude the following:

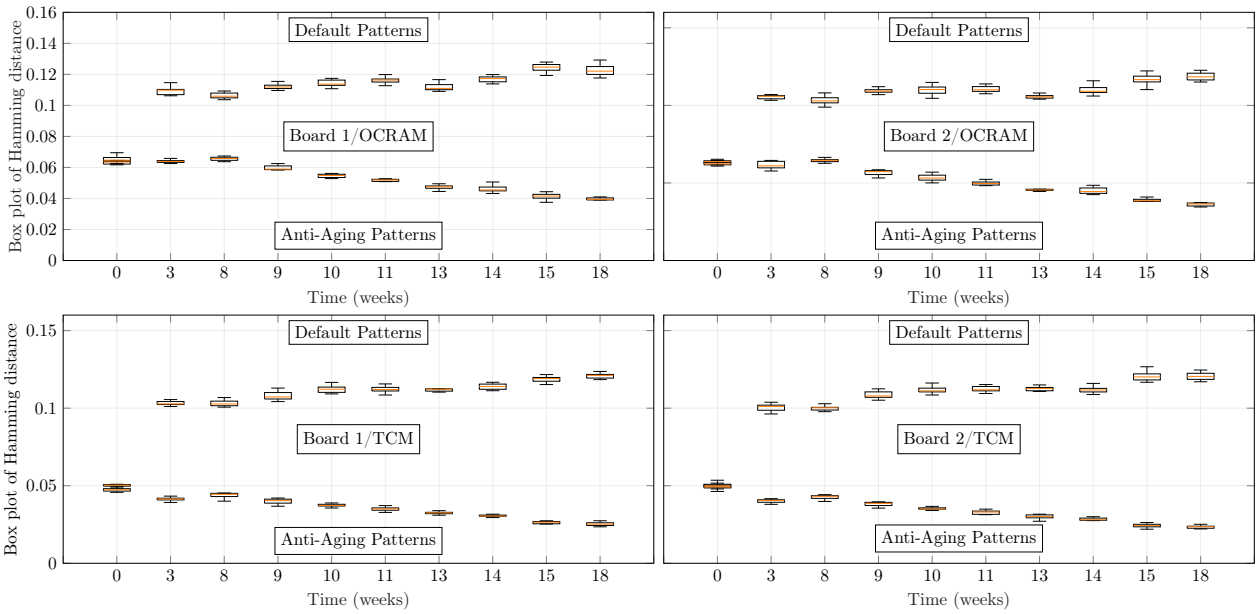

Fig. 5. Aging Impact on HD Using Default and Anti-Aging Patterns (Silicon Measurements)

Simulation vs. Silicon Measurements: Our simulation results demonstrated that the simulation model behaves similarly to the silicon measurements. However, there are small differences in the absolute values in terms of HD and number of strong cells. To improve the accuracy of the simulation model, commercial PDKs and libraries have to be used. The major benefit of a simulation model is to understand the behavior better prior to manufacturing and to measure parameters that are not possible or hard in actual silicon. For instance, in simulations, it is easy to see the effect of the ramp-up time. We could not measure this in the silicon experiments due to limitations of controlling the ramp-up time.

Impact of anti-aging on SRAM PUF in FinFET technology: Although known from previous results, it is extremely important to apply anti-aging patterns for SRAM-based PUFs as they improve the predictability of SUVs and significantly reduce the amount of ECC required. Hence, they reduce the overhead. For smaller technologies, this impact only gets bigger.

Impact of technology scaling on aging impact on SRAM PUF in FinFET technology: We showed that the HD in 14nm FinFET-based SRAM PUFs remains below 13% for the chip under consideration, even after 18 weeks of accelerated aging, which is equivalent to approximately 0.5 years of aging. The initial HD at time-zero ranges between 4% to 6% for different memories. Consequently, the monthly increase in HD due to aging falls within the range of 1% to 1.2%, which is equivalent to an increase of at least 36% over a period of 3 years when this data is extrapolated. Comparatively, older technologies exhibit lower HD increases over time. For instance, in [11], a monthly increase of 0.74% is reported.

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