Supplementary Power Controllers for Modern VSC-HVDC transmission links

Control design and advanced modelling methods for point-to-point and multi-terminal VSC-HVDC networks

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by

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For those that I have always loved
and I hope to hug one day.

Arcadio David PERILLA GUERRA

Contents

Summary

The increasing development of geographically close Voltage Source Converter based High Voltage DC links (i.e. VSC-HVDC links) is allowing to conceptualize their interconnection possibilities to form meshed VSC-HVDC networks. Ensuring the interoperability of a meshed (multi-terminal) VSC-HVDC network formed by the progressive expansion of VSC-HVDC links is a challenging task that requires a thorough analysis and understanding of different control aspects that affect the technical performance. Within this challenging task, the use of simulation models allowing to properly evaluate the level of stability support provided by an expanded point-to-point VSC-HVDC link (i.e. multi-terminal layout) towards an AC power system has a critical role. Furthermore, the simulation models for VSC-HVDC links are often modified to account for established grid code requirements. In view of this, an upgrade of a simulation model needed for analyzing the multi-terminal expansion of a modern point-to-point VSC-HVDC link remains an open challenge.

The upgrade of the VSC-HVDC link's simulation model is tackled in this dissertation by proposing several supplementary power controllers under a root-mean-square (RMS) simulation framework. The design of the proposed supplementary power controllers is done in DigSILENT PowerFactory 2019, and it is oriented to modify the reactive or the active power regulation of a VSC-HVDC link based on the stability phenomenon to be studied. Thus, the reactive power regulation is modified to provide quasi-stationary or dynamic voltage stability support, based on a dynamic power factor control or a (polynomial-based) reactive current injection control, respectively. The active power regulation is modified to provide primary frequency response based on a power-line communication-based controller, a post-fault active power recovery control, and an open-loop-based frequency control.

Besides above-mentioned VSC-HVDC link modelling upgrades, key aspects of performance assessment and control are also addressed. Firstly, a tool is developed for the assessment of the level of quasi-stationary voltage support provided by the reactive power controllers of a VSC-HVDC unit. The assessment was carried out by proposing a directional derivative-based method (DDBM). The DDBM allows to determine (without performing time domain simulations), the most suitable reactive power control to be used during different power flow and AC network (strength) conditions. Secondly, a dynamically adjustable fault impedance (DAFI) concept is proposed. DAFI facilitates the active and reactive power response of a VSC-HVDC link during the fault-ride-through (FRT) and post-FRT periods.

The main conclusion of this dissertation is that the multi-terminal expansion of a point-to-point VSC-HVDC link does affect its active and reactive power response

and its interplay with an AC power system in steady-state and dynamic stability performances. Particularly, during the design process of the supplementary power controllers, the dynamic power factor regulation in a VSC-HVDC unit can cause up to a 3% of AC voltage deviation, when an active power reversal event occurs. Moreover, the assessment of the DDBM determined that the dynamic power factor control is the less attractive option for supporting the quasi-stationary voltage stability in most of the operating conditions analyzed for the studied test AC network. Additionally, DAFI demonstrated that it is possible to emulate the inductive characteristics of a power system (during post-fault conditions) by designing a control system based on a first-order dynamic response. This can entail an enhanced performance of the supplementary power controllers defining the FRT and the post-fault active power recovery process.

Thirdly, a power-line communication-based controller is proposed from the point of view of a harmonic amplitude modulation strategy for embedded point-to-point VSC-HVDC links. The deployment of the controller for providing primary frequency support is illustrated and demonstrated. The proposed controller allows to reduce the rate-of-change-of-frequency and the maximum frequency deviation (e.g. Nadir) occurring in AC networks experiencing an AC network split event. Next, an open loop frequency controller is also proposed to adjust the active power reference and the active power gradient of a point-to-point VSC-HVDC link. The goal is to provide primary frequency support under severe active power imbalances. Numerical simulations show that the obtained frequency responses of two asynchronous AC networks can be selectively coordinated to effectively reduce either the rate-of-change of frequency or the steady-state frequency deviation, e.g. due to a sudden event concerning with a 18% load disconnection.

Finally, it is elucidated that the multi-terminal expansion of a point-to-point VSC-HVDC link would require a transient DC voltage modification of the VSC-HVDC units to effectively regulate the post-fault active power recovery process. To address this aspect, a multi-terminal DC voltage controller is proposed by considering an exponential function, which enables a suitable transient DC voltage regulation during the post-fault active power recovery period. Numerical simulations illustrate that, if the transient DC voltage modification is not possible, it would be necessary to include DC choppers to avoid DC over-voltage issues across the multi-terminal (i.e. expanded point-to-point) VSC-HVDC link. Additionally, it is also demonstrated that the proposed controller can use the power dissipation capabilities of DC choppers to support the multi-terminal DC power balancing during the FRT activation of a VSC-HVDC unit. The coordination of the DC choppers and the transient DC voltage regulation is found useful to reduce, for instance, up to 80% of the AC/DC power imbalance introduced during the FRT activation, while restoring the active power within 200 ms.

Samenvatting

De toenemende ontwikkeling van geografisch dichtbij gelegen, Voltage Source Converter gebaseerde HVDC-verbindingen (VSC-HVDC-verbindingen) maakt het mogelijk om de verbindingsmogelijkheden om vermaasde VSC-HVDC-netwerken te vormen te conceptualiseren. Het waarborgen van de interoperabiliteit van een vermaasd (Multi-Terminal) VSC-HVDC-netwerk gevormd door de geleidelijke uitbreiding van VSC-HVDC-verbindingen, is een uitdagende taak die een grondige analyse en begrip vereist van verschillende besturingsaspecten die van invloed zijn op de technische prestaties. Binnen deze uitdagende taak speelt het gebruik van simulatiemodellen die het mogelijk maken om het niveau van stabiliteitsondersteuning die wordt geboden door een Multi-Terminal-uitgebreide Point-to-Point VSC-HVDC-verbinding aan een AC-systeem, een cruciale rol. Bovendien worden de simulatiemodellen voor VSC-HVDC-verbindingen vaak aangepast om rekening te houden met de vastgestelde vereisten van de netcode. Met het oog hierop blijft een upgrade van een simulatiemodel dat nodig is voor het analyseren van de Multi-Terminal uitbreiding van een moderne Point-to-Point VSC-HVDC-verbinding een openstaande uitdaging.

De upgrade van het simulatiemodel van de VSC-HVDC-verbinding wordt in dit proefschrift aangepakt door verschillende aanvullende vermogensregelaars voor te stellen onder een Root-Mean-Square- (RMS)-simulatieraamwerk. Het ontwerp van de voorgestelde aanvullende vermogensregelaars is gedaan in DigSILENT PowerFactory 2019 en is gericht op het wijzigen van de reactieve of actieve vermogensniveaus van een VSC-HVDC-verbinding op basis van het te bestuderen stabiliteitsfenomeen. Het reactiefvermogensniveau wordt dus aangepast om quasi-stationaire of dynamische spanningsstabiliteitsondersteuning te bieden, gebaseerd op respectievelijk een dynamische vermogensfactorregeling of een (op polynomen gebaseerde) reactievestroominjectieregeling. Bovendien wordt het niveau van actief vermogen aangepast om inertie-, of primaire frequentierespons te bieden op basis van een op communicatie via de hoogspanningsverbinding gebaseerde regelaar, een regeling voor herstel van actief vermogen na een storing en een open-lus-gebaseerde frequentieregeling.

Naast de bijdrage voor verbeterde modellering van VSC-HVDC-verbindingen, zijn ook drie aanvullende methodologieën ontwikkeld. De eerste methodologie betreft de beoordeling van het niveau van quasi-stationaire spanningsondersteuning geleverd door de reactiefvermogensregelaars van een VSC-HVDC-eenheid. De beoordeling werd uitgevoerd door een Directional Derivative-Based Method (DDBM) voor te stellen. Met de DDBM kan worden bepaald (zonder tijdsdomeinsimulaties uit te voeren) wat de meest geschikte blindvermogensregeling is die moet

worden gebruikt tijdens verschillende vermogensstroom- en AC-netwerk(sterkte)-omstandigheden. De tweede methodologie bestaat uit het ontwerp van een Dynamic Adjustable Fault Impedance (DAFI) die de actieve en reactieve vermogensrespons van een VSC-HVDC-verbinding tijdens de FRT-periode (Fault-Ride-Through) en post-FRT-periodes vergemakkelijkt.

De belangrijkste conclusie van dit proefschrift is dat de Multi-Terminal-uitbreiding van een Point-to-Point VSC-HVDC-verbinding de actieve en reactieve vermogensrespons beïnvloedt tijdens de stationaire en dynamische stabiliteitsanalyse van een AC-systeem. Met name tijdens het ontwerpproces van de aanvullende vermogensregelaars kan de dynamische vermogensfactorregeling in een VSC-HVDC-eenheid tot 3% van de AC-spanningsafwijking produceren wanneer er om een omkering van het actief vermogen wordt verzocht. Bovendien heeft de beoordeling van de DDBM vastgesteld dat de dynamische vermogensfactorregeling de minder aantrekkelijke optie is voor het ondersteunen van de quasi-stationaire spanningsstabiliteit in de meeste geanalyseerde AC-netwerkomstandigheden. Bovendien toonde de DAFI aan dat het mogelijk is om de inductieve kenmerken van een elektriciteitssysteem na te bootsen (tijdens post-foutcondities) door een besturingssysteem te ontwerpen dat is gebaseerd op een eerste-orde dynamische respons. Dit om de prestaties te analyseren van de aanvullende vermogensregelaars die de FRT uitvoeren, en het herstelproces van actief vermogen na een fout.

Het ontwerp van een op communicatie via hoogspanningsverbindingen gebaseerde controller op basis van een harmonische amplitudemodulatiestrategie voor Embedded Point-to-Point VSC-HVDC-verbindingen die primaire frequentieondersteuning bieden, is gedemonstreerd. De voorgestelde strategie maakte het mogelijk om de Rate-of-Change-of-Frequency en de Frequency Nadir te verminderen die optreden in AC-netwerken die een AC-netwerksplitsing ervaren. Vervolgens werd ook een open-lus frequentieregelaar voorgesteld die de referentie van het actieve vermogen en de gradiënt van het actieve vermogen van een Point-to-Point VSC-HVDC-verbinding aanpast om primaire frequentieondersteuning te bieden bij ernstige verstoringen van het actief vermogen. Het resultaat toonde aan dat de verkregen frequentieresponsen van twee asynchrone AC-netwerken kunnen worden gecoördineerd om ofwel de Rate-of-Change-of-Frequency ofwel de stationaire frequentieafwijking te verminderen na een ontkoppeling van de belasting van 18%.

Ten slotte werd aangetoond dat de Multi-Terminal uitbreiding van een Point-to-Point VSC-HVDC-verbinding een transiënte DC-spanningsaanpassing van de VSC-HVDC-units zou vereisen om het herstelproces van actief vermogen na een storing te regelen. Bijgevolg werd een Multi-Terminal DC-spanningsregelaar ontworpen door een exponentiële functie te beschouwen die in staat is om de transiënte DC-spanningsregeling te leveren tijdens de herstelperiode van actief vermogen na een storing. Bovendien werd gezien dat als de transiënte DC-spanningswijziging niet mogelijk is, het nodig zou zijn om DC-choppers op te nemen om DC overspanningsproblemen over de Multi-Terminal uitgebreide Point-to-Point VSC-HVDC-verbinding

te voorkomen. Bovendien werd ook aangetoond dat de voorgestelde controller de vermogensdissipatiemogelijkheden van DC-choppers kan gebruiken om de Multi-Terminal DC-vermogensbalans te ondersteunen tijdens de FRT-activering van een VSC-HVDC-eenheid. De coördinatie van de DC-choppers en de transiënte DC-spanningsregeling bleken nuttig om tot 80% van de AC/DC-vermogensonbalans te verminderen die tijdens de FRT-activering werd geïntroduceerd, terwijl het actieve vermogen binnen 200 ms werd hersteld.

1

Introduction

The clean energy transition targets defined by the European Commission in its *European Green Deal*, have established the need for a no net emissions of greenhouses gases by 2050. These ambitious targets have direct implications for the power systems sector which will need to be progressively largely based on renewable energy sources [1]. In that sense, the High Voltage DC transmission links based on Voltage Sources Converter technology (i.e. VSC-HVDC links) are becoming one of the preferred solutions for the achievement of such targets since they present two important characteristics. The first one is their ability for allowing the integration of offshore wind power into the power systems, and the second one is their ability for allowing the electricity markets coupling between countries long distance separated (e.g. the 623km NordLink HVDC link). These two characteristics and the accelerated large-scale deployment of offshore wind turbines foreseen for the North Sea, are fostering the creation of a multi-terminal VSC-HVDC network based on the progressive expansion of existing point-to-point VSC-HVDC links [2, 3]. In Europe, the first point-to-point VSC-HVDC link that envisaged this concept is the COBRAcable project, which is a 700MW symmetrical monopole link interconnecting the Endrup region in Denmark with the Eemshaven region in The Netherlands [4].

Theoretically, the expansion of a point-to-point VSC-HVDC link towards multi-terminal operation is expected to allow higher integration of renewable energy, while offering a high degree of controllability to the power transmitted between the onshore and offshore AC networks [5]. In addition, several major technical aspects, required to ensure the robust operation of an expandable VSC-HVDC link, need to be investigated in terms of its underlying steady-state and dynamic performances. These aspects are especially critical in weak AC networks, in which stability issues can be of high concern [6]. Modelling upgrades and new control strategies should be designed to properly study and effectively provide stability support by multi-terminal expanded point-to-point VSC-HVDC links.

1

1.1. Research Problem Definition

High voltage DC (HVDC) technology has become an attractive technical and economical solution for transmitting power across long distances when compared to conventional AC transmission systems. The use of HVDC over HVAC transmission systems is considered techno-economically feasible for offshore networks when the distance between the corresponding offshore and onshore converter stations is above 60-75km [7]. Above these distances, the installation costs associated with the reactive power compensation units (needed to correct the power factor level of the corresponding AC transmission submarine cables) become economically impractical.

The benefits of utilizing an HVDC transmission system over an HVAC transmission system are also characterized by the type of power electronic semiconductor technology (thyristor or an insulated-gate bipolar transistor - IGBT) utilized by the corresponding HVDC converter stations. Each of these two types of power electronics semiconductors has its own advantages and disadvantages. For instance, a thyristor-based HVDC converter unit (also known as a line-commutated converter - LCC) can be used for ultra-high voltage DC (UHVDC) applications (e.g. 800kV) where power transmission across very long distances (above 1300km) is required [8]. However, a converter unit based on IGBT power semiconductors (also known as a voltage source converter (VSC)) can currently be used for DC power transmission up to 525kV HVDC applications. On the other hand, an LCC-based HVDC system is prone to experience commutation failures when voltage disturbances (caused by AC faults) occur [9]. Nevertheless, a converter station based on IGBT power semiconductors (i.e. VSC unit), can provide dynamic voltage support during an AC fault event occurring at the AC network [10].

Furthermore, the indicated benefits offered by LCC and VSC HVDC transmission systems can be simultaneously obtained if hybrid LCC-VSC HVDC grids are developed. However, the development of hybrid LCC-VSC-HVDC grids is limited by specific geographical conditions and by the additional integration of (per-pole) series-connected VSC units [11]. These restrictions would increase the investments needed and the complexity of implementing such hybrid LCC-VSC HVDC grids within the current European offshore energy transition targets for the North Sea. On the other hand, the multi-terminal expansion of point-to-point VSC-HVDC links represents nowadays a transmission system operator (TSO) requirement enabling the multi-purpose interconnector (MPI) functionality of such links [12].

The COBRAcable project is the first MPI point-to-point VSC-HVDC link between the TSOs from the Netherlands and Denmark (i.e. Energinet and TenneT). Therefore, the COBRAcable research project was created as an industrial-academic project meant to tackle the technical challenges associated with such multi-terminal expansion from an AC side and a DC side point of view. Within this context, the Dutch (Delft University of Technology) and the Danish (Aalborg University) research institutions were the academic entities of the COBRAcable research project. The analysis

of the influence of the multi-terminal expansion over the AC networks connected to the original point-to-point HVDC link (e.g. fault-ride through, post-fault active power recovery, etc) was tackled by the Delft University of Technology (this thesis). The analysis of the influence of the multi-terminal expansion over the original DC network (e.g. DC power regulation, DC protection, etc) was done by Aalborg University.

Certainly, the multi-terminal expansion of a point-to-point VSC-HVDC link is expected to support the stability of AC networks with the same or a higher level of effectiveness than the latest point-to-point links. This essentially challenges the control functionalities for active (P) power and the reactive (Q) power at the AC sides of the VSC units, without neglecting the interplay with the power management between AC and DC sides of the multi-terminal DC. Furthermore, the challenges become larger when different types of AC networks' contingencies (e.g. AC voltage drops or AC network splits) are considered within the planning studies of an expandable point-to-point VSC-HVDC link. In view of this, this dissertation focuses on the following challenges:

Accurate modelling of expandable point-to-point VSC-HVDC links

The current modelling approach utilized to represent the standard control functions of the point-to-point VSC-HVDC links is mainly focused to the DC voltage, the AC voltage, the active power control, and the reactive power control [13]. However, modern VSC-HVDC links are required to incorporate supplementary control functions, which go beyond the standard control functionalities in order to support the frequency and voltage stability of weak AC networks [14]. These supplementary control functions shall allow new modulation forms of the active and the reactive power flows transferred to the AC networks during steady-state or dynamic conditions. Moreover, there is a lack of knowledge on the design, performance, and tuning of the supplementary control functions within the context of an expandable point-to-point VSC-HVDC link. Consequently, an upgrade of the standard models for point-to-point VSC-HVDC links needs to be performed by adding such supplementary control functions. In this dissertation, the focus is on the design and tuning of functions for power factor control, fault ride-through control, frequency control, and post-fault active power recovery control.

Generally speaking, the regulation of power factor constitutes one of the control options for reactive power-voltage support in transmission or distribution networks. Nevertheless, it is predominantly deployed in distribution networks due to the higher exposure to voltage fluctuations, which are often attributed to variable inductive loads. In the context of distribution networks, the design of power factor control is done under the assumption of unidirectional reactive power exchange between, for example, capacitor banks and the surrounding electrical network. By contrast, there are no experience nor design criteria for the deployment of power factor control in transmission networks. The open challenge for expandable point-to-point VSC-HVDC links is to simultaneously tackle the possibility of dealing with

bi-directional active and reactive power exchanges and the risk of collateral implications of the power flow control over the AC voltage profile.

Furthermore, the dynamic support capability of a VSC-HVDC link under low or high AC voltage conditions involves a higher interplay between two supplementary control functionalities: the fault-ride through (FRT) and the post-fault active power recovery. The FRT function is essentially a supplementary control that adjusts the level of reactive current supplied by a VSC unit during a fault event in the AC network. Literature has shown that the reactive current adjustment generated by the FRT is determined by reference curves (typically defined by electricity grid codes [15]), which consist of piecewise functions [16]. Namely, the design process of these piecewise functions entails the use of fault detection systems (FDS) and switching algorithms that can produce an oscillatory AC voltage profile [17]. These oscillations typically occur when the AC voltage drop coincides with the limits associated with the activation of the FDS, or, with the expected reactive current injection principle used by the FRT control mode.

On the other hand, the control design of the post-fault active power recovery function has been tackled in existing literature so far by considering two approaches. The first approach alters (reset) the value of the state variables of the integral controllers utilized to regulate the active power level provided by a VSC unit when a fault event occurs at AC network in which it is connected [18, 19]. The second approach proposes a fast post-fault active power response where the affected VSC unit, restores its pre-fault active power with a recovery rate of 5 p.u./s [20]. These approaches have been mainly designed to cope with eventual DC over-voltages that occur in point-to-point VSC-HVDC links when transferring offshore wind power to onshore networks. Nevertheless, point-to-point VSC-HVDC links can also be utilized to transfer power between different synchronous AC networks, where the DC under-voltages can occur depending on the location of the fault event [21].

The stability analysis of power systems including VSC-HVDC links experiencing short circuit events has been usually carried out by considering modelling approaches based on a root-mean-square (RMS) simulation framework [22]. These RMS simulations typically simplify the representation of the dynamic response concerning with the AC voltage restoration process after a fault event [23], to increase the speed of the RMS simulation process. However, this simplification limits the numerical accuracy of the obtained results needed to properly study the short-circuit contribution provided by a VSC-HVDC unit when a fault event occurs at the AC network.

The frequency control of power systems by using VSC-HVDC links has received more and more attention due to the projected increment in the level of rate-of–change-of-frequency (RoCoF) and the magnitude of the maximum frequency deviation - MFD (also known as Nadir in case of under-frequency, or Zenith in case of over-frequency) within the period of primary frequency control. These projected

increments occur due to the replacement of conventional generation units [24, 25], by inverter-based renewable energy sources unable to supply the same level of inertia's constants to those power systems. In current literature, several methods like the inertial frequency response [26], and the derivative-based frequency control [27] propose different solutions for reducing levels of RoCoF and MFD. However, these methods are designed considering closed-loop control systems which strongly and continuously depend on the quality of the processing of the frequency measurement signal [28]. Furthermore, the complexity of integrating these types of methods within expandable point-to-point VSC-HVDC links constitutes a major challenge, considering the "black box" characteristics of the control systems associated with real VSC-HVDC projects. Therefore, the need for a method capable of enabling the effective tuning of the frequency regulation functionality of VSC-HVDC links, supporting low inertia AC networks is still an open challenge. A key aspect is to find the best control settings, without modifying the controller structure.

Assessment of the quasi-stationary AC voltage support by expandable point-to-point VSC-HVDC links

In the existing literature, the analysis of the quasi-stationary voltage support provided by VSC units has been usually tackled by using two main methodologies: the PV - QV curve analysis [29, 30], and the Jacobian sensitivity matrix [31, 32]. These methodologies require the development of simulation routines in which the change in the quasi-stationary voltage profile (generated by the operation of the reactive or active power control modes in the VSC unit) is examined, based on the corresponding power system's characteristics (e.g. voltage level, network impedance). However, none of these methods allow an integrated approach to examine the way in which the power system's characteristics and the power control modes of a VSC unit interact to modify the quasi-stationary voltage profile in the AC network. This interaction analysis would be beneficial, for example, to compare the effectiveness or limitations that the power factor control mode (PFmode) could provide to the transmission AC network without the need of performing consecutive (computationally expensive) load flow calculations. Furthermore, the current methods have not yet analyzed the implications that the power flow management of an expandable HVDC point-to-point link would generate for the level of support provided by its VSC units in terms of the quasi-stationary AC voltage support. This is especially relevant considering that the multi-terminal expansion of a point-to-point VSC-HVDC link can be developed by adding offshore wind power resources.

Power line communication concept for AC-DC-AC Power management by point-to-point VSC-HVDC links to support frequency stability.

In current literature, several methods have been proposed to use the active power regulation capabilities of the VSC-HVDC links to support the primary frequency response of low inertia power systems experiencing a severe (i.e. 20%) load imbalance. These methods (e.g. the inertial frequency response [26], derivative-based control [27], virtual synchronous power [14]) are subjected to the reliability of conventional communication methods (e.g. fiber optics) utilized by the VSC-HVDC link. By contrast, new frequency control strategies have been recently proposed, where

the DC voltage regulation represents a fundamental aspect for enabling alternative communication methods. Such emerging methods are based on the power-line communication principle and they can be classified into two main strategies: strategies based on non-periodic controlled signals (NPCS) [33–38] and based on periodic controlled signals (PCS) [39, 40]. On one hand, the NPCS attempts to proportionally change the DC voltage level of the VSC-HVDC link based on the frequency deviations in the affected power system. On the other hand, the PCS strategies consider the addition of very small (i.e. less than 2%) AC voltage waveforms (with variable frequency) as part of the DC voltage reference. However, introducing such type of frequency-modulated AC voltage waveform within the HVDC cable can lead to a resonance phenomenon within the VSC-HVDC link, which can potentially affect the stability of the HVDC/HVAC power transmission process [41].

Post-fault active power recovery of expandable VSC-HVDC links

The post-fault active power recovery (PFAPR) constitutes a control mode for regulating the response of the active power provided by the VSC unit after a voltage dip (caused by a fault event) occurs in the AC network. Typically, this control mode needs to be coordinated with the fault-ride-through function to balance the amount of reactive and active power provided by the VSC unit while keeping its AC current's magnitude with the allowed technical limits. To date, the PFAPR has been studied in the literature by considering the unidirectional power flow condition associated to point-to-point VSC-HVDC links connecting offshore wind farms [42]. In this power flow condition, DC choppers are normally utilized for reducing DC over-voltage phenomena experienced when a voltage drop affects the AC side of the onshore VSC unit while transmitting offshore power towards the onshore AC network. However, as the multi-terminal expansion might be developed from a point-to-point VSC-HVDC link interconnecting two onshore AC networks, the PFAPR design would need to be carried out by considering the likelihood of occurrence of DC under-voltages issues [21].

In current literature, DC under-voltages have been tackled in a point-to-point or a multi-terminal VSC-HVDC link by considering either the voltage margin method [43–45] or by utilizing a distributed DC voltage regulation approach for the multi-terminal network (e.g. droop control) [46–49]. Recently, the feasibility of balancing the DC power in the multi-terminal VSC-HVDC network by coordinating the operation of DC choppers and the DC voltage regulation methods has been discussed in [50]. Nevertheless, a design strategy focused on the PFAPR management by considering the simultaneous operation of DC choppers, and the DC voltage regulation methods within the multi-terminal expansion of a point-to-point VSC-HVDC link is still an urgent topic that needs to be investigated.

Optimal adjustment of frequency control parameters for point-to-point VSC-HVDC links

In current literature, the active power gradient (APG) of point-to-point VSC-HVDC links has been identified as one of the key parameters for reducing the RoCoF and MFD in low inertia power systems [51]. However, considering that the VSC-HVDC

links are capable of interconnecting AC networks that can be synchronously decoupled, a situation-dependent optimal tuning of the APG currently represents an open research challenge. The challenge resides in the lack of criteria for the adjustment of the frequency support action that a point-to-point VSC-HVDC link needs to provide when a severe power imbalance occurs at one of the AC networks connected with the link. The selection of the APG while preventing undesired (adverse) conflicting control reactions between the resources involved in primary frequency in the AC networks should be properly understood. The optimal adjustment of APG is also one of the urgent-to-solve research topics, considering the progressive increase of the transmission capacity foreseen for the point-to-point VSC-HVDC links in Europe, as well as the expected role of VSC-HVDC transmission to effectively and quickly support primary frequency control [52].

1.2. Research goal and questions

The research goal of this thesis concerns the design of supplementary control functions for expandable point-to-point VSC-HVDC links capable of providing frequency and voltage stability support to power systems during steady-state and dynamic conditions. In view of this, the following five research questions have been formulated:

1. - What modelling developments (upgrades) are needed to properly capture the active and reactive power grid support by expandable VSC-HVDC units?

2. - How can different reactive power control schemes of a modern VSC-HVDC unit for providing quasi-stationary AC voltage support be comprehensively and computationally efficiently compared and selected?

3. - What kind of supplementary power control should be used to provide primary frequency support to a power imbalanced AC network, if the PtP-VSC-HVDC link (demanding power from the imbalanced AC network) is requested to operate even during the loss of the communication interface between its converter stations??

4. - How to upgrade the post-fault active power recovery functionality of a point-to-point VSC-HVDC link when it expands towards a multi-terminal network, in order to effectively mitigate active power imbalances induced by AC voltage dips?

5. - How to calibrate the parameters of the upgraded VSC-HVDC model to optimally support the frequency stability of decoupled low inertia AC networks affected by severe active power imbalances?

1

1.3. Methodological approach

The design of supplementary active and reactive power controllers for an expandable point-to-point VSC-HVDC link is developed based on the requirements described by the European HVDC grid code in [14]. These requirements establish the need of VSC-HVDC links providing power factor (PF) control, fault ride-through (FRT) control, post-fault active power recovery control, frequency control, and constitute themselves the actual supplementary active and reactive power controllers.

The design process of these supplementary power controllers starts by implementing the standard modelling approach (presented in [13]) for point-to-point VSC-HVDC links in the Dynamic Simulation Language (DSL) of the commercial software package DIgSILENT PowerFactory 2018. This implementation is carried out under a root-mean-square (RMS) simulation framework which allows to evaluate the level of voltage and frequency support provided by the VSC-HVDC link to power systems under different steady-state and dynamic conditions. Furthermore, the multi-terminal expansion of the point-to-point VSC-HVDC link studied in this dissertation concerns with the addition of an offshore VSC unit integrating offshore wind power into the multi-terminal HVDC network. The analysis of the influence of the level of steady-state and dynamic stability support provided by the proposed supplementary power controllers is evaluated by firstly considering the point-to-point operation of the VSC-HVDC link and subsequently considering its offshore (three-terminal) expansion. Furthermore, several optimization routines have been developed in Python (version 3.7) to automatize the management of DIgSILENT PowerFactory 2018, in order to analyze the overall system performance and to execute the adjustment of the parameters utilized by the proposed supplementary power controllers.

1.4. Thesis outline

The outline of this thesis is graphically described in Figure 1.1.

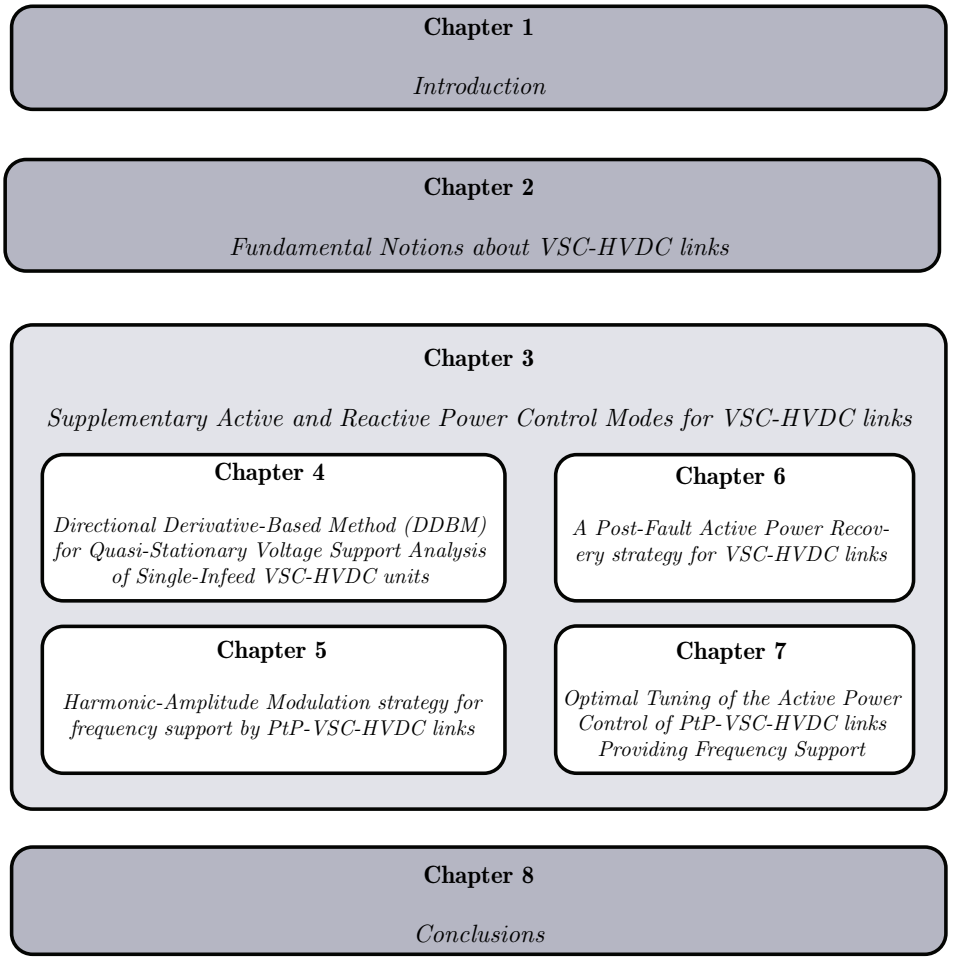

Figure 1.1: Layout of the dissertation.

Chapter 2 provides a summary of the fundamental notions that are needed to classify the operation and configurations of VSC-HVDC links. Moreover, Chapter 2 also provides a description of the modelling characteristics that are needed to generate a dynamic model of the expandable VSC-HVDC unit based on modular multi-level converter technology.

Chapter 3 presents the design process of the supplementary reactive and active power controllers that are incorporated into the modelling approach used for representing the expandable point-to-point VSC-HVDC model described in Chapter 2

during steady state, power imbalance and fault conditions in its corresponding AC networks.

In Chapter 4, a method for assessing the level of quasi-stationary voltage support provided by the reactive power control modes of a VSC-HVDC unit is proposed. The method is based on the directional derivative concept, and it is studied considering an expandable VSC-HVDC link operating in either a point-to-point or a multi-terminal scenario while assuming different AC network strength conditions.

Chapter 5 concerns with the development of a control system based on the power line communication principle applied to point-to-point VSC-VHDC links, which is used to provide frequency support to AC networks affected by severe active power imbalanced events (i.e. network split or power outer events).

Chapter 6, concerns with the analysis of the post-fault active power recovery characteristics of an expandable VSC-HVDC link operating in either a point-to-point or a multi-terminal scenario when a three-phase fault causes a voltage dip in the AC network. This analysis is based on the design of a non-linear DC voltage controller which coordinates the adjustment of the DC voltage reference of the VSC-HVDC units and the DC choppers activation strategy.

Chapter 7, the methodology for the adjustment of the active power gradient of a point-to-point VSC-HVDC link providing frequency support to synchronously decoupled low inertia power systems is proposed based on the mean-variance optimization approach.

Finally, Chapter 8 presents the conclusions and the answers concerning the research questions of this dissertation.

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2

Fundamental notions of VSC-HVDC links

This chapter describes the definitions, classifications and modelling assumptions of voltage source converters (VSC) HVDC links based on modular multilevel converter (MMC) technology. The methodology is developed by formulating a mathematical description utilized for explaining the AC/DC and DC/AC energy conversion process in a VSC unit. Additionally, the control modes enabling the operation of a VSC unit under normal conditions are described within the context of a point-to-point (PtP) HVDC network and a multi-terminal (MT) HVDC network.

2.1. Definitions and Classifications

A High Voltage DC (HVDC) link based on Voltage Source Converter technology (i.e. VSC-HVDC link) is an electrical system in which an AC/DC and DC/AC energy conversion process is developed. Moreover, the VSC-HVDC link is comprised of essentially DC cables, transformers, and VSC units which are utilized for interconnecting synchronous or asynchronous transmission networks. Furthermore, as shown in Figure 2.1, a VSC-HVDC link can be classified from an AC side point of view, as a non-embedded (i.e. AC networks synchronously decoupled c.f. Figure 2.1a) or as an embedded (i.e. AC networks synchronously coupled c.f. Figure 2.1b) interconnector [1].

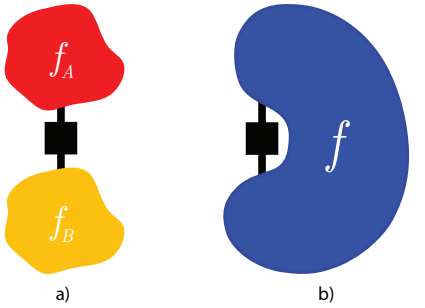

Figure 2.1: AC transmission networks (represented by the red, the orange and the blue shapes) linked by a VSC-HVDC system (represented in black) working as: a) non-embedded interconnector. b) embedded interconnector. Here, f represents the electrical frequency of the corresponding AC network.

On the other hand, from a DC side point of view, a VSC-HVDC link can be classified as a point-to-point (PtP) or a multi-terminal (MT) DC network [2, 3]. Moreover, these two types of DC side classifications can be further extended based on the possible configurations existing for VSC-HVDC links as for example, the ones presented in Figure 2.2, Figure 2.3 and Figure 2.4.

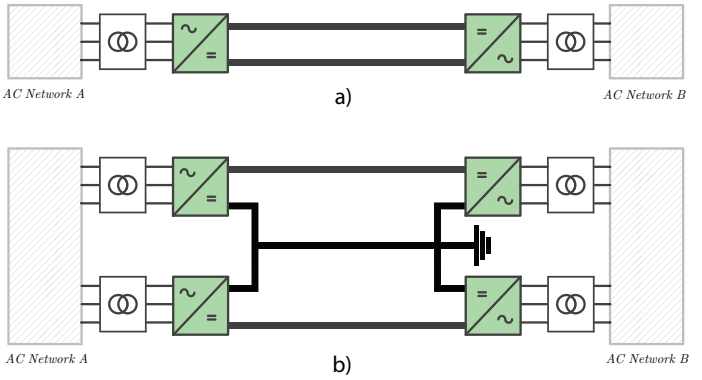

Figure 2.2: Example of Point-to-Point (PtP) HVDC links based on VSC units (highlighted in green) forming a two terminal: a) symmetrical monopole system. b) bipolar system with a grounded metallic return.

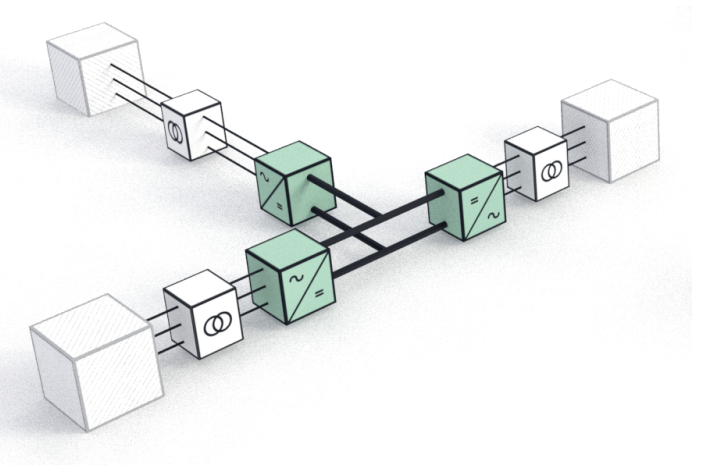

Figure 2.3: Example of a Multi-terminal (MT) HVDC link consisting of three VSC units (highlighted in green) forming a three terminals symmetrical monopole system.

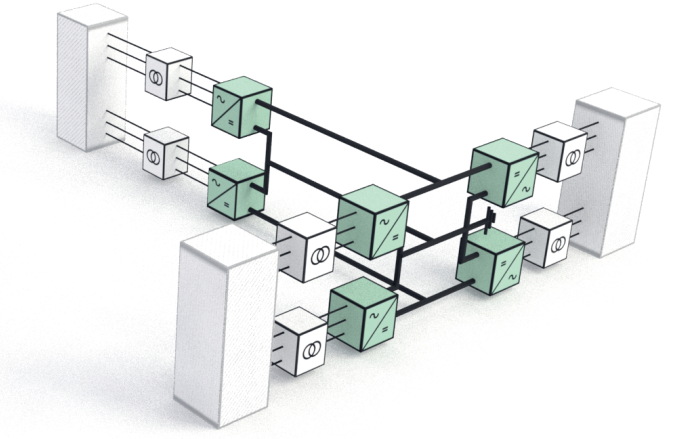

Figure 2.4: Example of a Multi-terminal (MT) HVDC link consisting of six VSC units (highlighted in green) forming a three terminals bipolar system with a grounded metallic return.

Independently of the classification utilized, the DC/AC or AC/DC energy conversion process is essentially carried out by the VSC units which have the role of generating the necessary DC and AC voltage waveforms in the corresponding DC or AC networks. The generation of these DC and AC voltage waveforms in a VSC unit is established by means of several control systems which are designed to regulate the power flow between the electrical networks (coupled by the HVDC link) during energization, normal, and fault conditions [4].

The design and the adjustment of such control systems are strongly influenced by the electrical properties of the HVDC link and by the AC network characteristics of the coupled power systems. These characteristics and properties are usually represented (for evaluating and adjusting the performance of the VSC's control systems) in a phasor's based (i.e. root means square (RMS)) simulation environment [5], or a differential equations based (i.e. electromagnetic transient (EMT)) simulation environment [6, 7]. Thus, the analysis of the energy conversion process requires the implementation of EMT or RMS models capable of expressing the interplay between the AC and DC networks, from a dynamic response and a steady-state operational point of view.

2.2. Modelling a VSC-HVDC unit based on MMC technology

The implementation of an EMT or RMS model of a VSC-HVDC link represents the process of describing the mathematical relationships that govern the dynamic response of the currents and voltages defining the power transfer between the AC and DC networks. In that sense, it is first necessary to describe the basic elements that constitute a VSC unit which is nowadays (for high-power transmission system applications below 1300km, [8])here are moment in life in which mainly based on Modular Multi-level Converter (MMC) technology.

2.2.1. System Description

As seen in Figure 2.5, a VSC unit based on MMC technology is essentially formed by six reactors (L_{MMC}) and six structures called valves (a.k.a. "arms") which are comprised of hundreds of sub-modules [9, 10]. Within each of these sub-modules, an arrangement of semiconductors (typically IGBTs) is managed in order to control the moment in which the sub-module's capacitor C is excluded or inserted into the corresponding (internal) current loop (i.e. i_{up} or i_{low}) presented in Figure 2.5. It is worth pointing out that the i_{up} or i_{low} currents are comprised of DC and AC components which simultaneously flow within the MMC unit (i.e. DC and AC currents simultaneously flow through the inserted capacitors within the valves) [11].

Essentially, the insertions or the exclusions of the capacitors within a single valve, are a consequence of two regulation processes. The first (outer) regulation process defines the *number* of capacitors that must be inserted in order to produce the desired voltage waveform across the corresponding valve (e.g. $v^{(+)}_{valve_x}$), [12]. It is relevant to clarify that the first regulation process is developed by considering that the second (inner) regulation process (a.k.a. *capacitor voltage balancing*) is properly executed [13]. The second (inner) regulation process determines and defines *which* of the capacitors must be inserted (or excluded) in order to maintain (as identical as possible) the same voltage level across all the capacitors within the same valve, at all time [14, 15]. The successful development of the *capacitor voltage balancing* (i.e. the second regulation process) allows managing the MMC unit as a power electronic device where a series of identical *time-variant* voltage

sources (located within each valve) are inserted between the DC and AC networks.

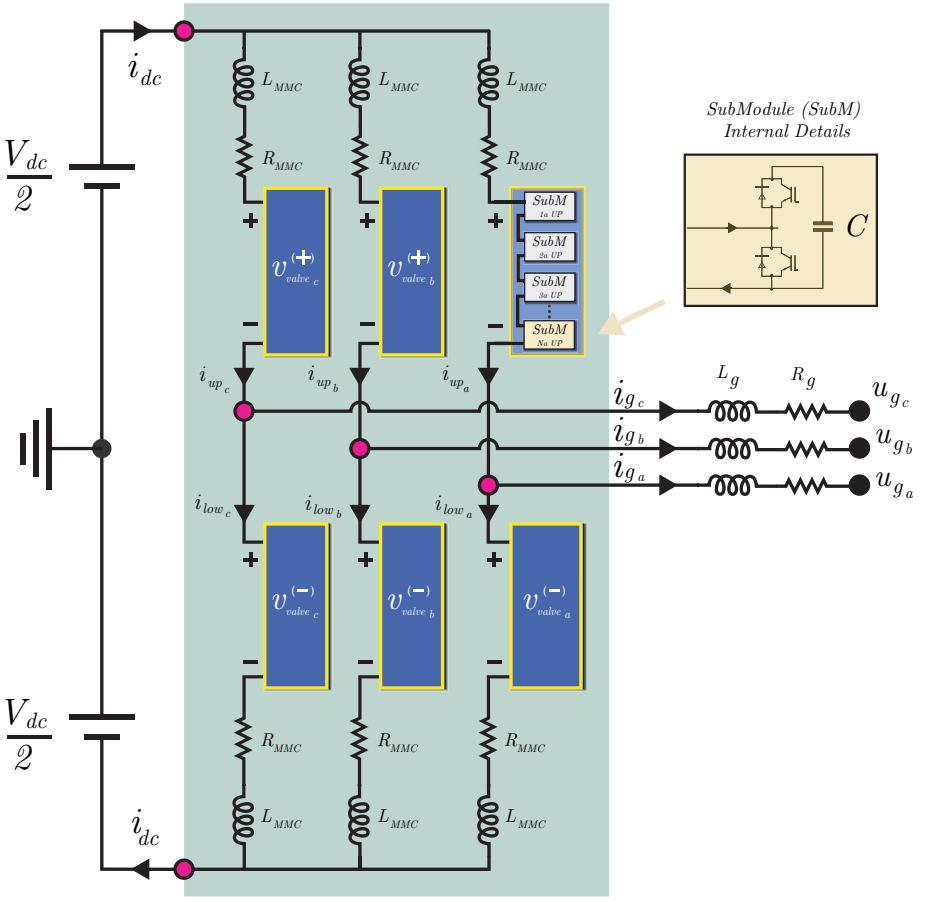

Figure 2.5: General description of a VSC (MMC-based) unit, as presented in, [16].

As shown in Figure 2.5, if a reduced representation of the AC and DC network is considered [16], it is possible to simplify the description of the differential equations defining the interplay between the currents and the voltages generated by the valves of the MMC unit as expressed by 2.1, 2.2 and 2.3.

$$i_{up_x} = i_{g_x} + i_{low_x} \tag{2.1}$$

$$\frac{-V_{dc}}{2} + L_{MMC}\frac{di_{up_x}}{dt} + R_{MMC}i_{up_x} + v^{(+)}_{valve_x} + L_g\frac{di_{g_x}}{dt} + R_g i_{g_x} + u_{g_x} = 0 \tag{2.2}$$

$$\frac{V_{dc}}{2} - L_{MMC}\frac{di_{low_x}}{dt} - R_{MMC}i_{low_x} - v^{(-)}_{valve_x} + L_g\frac{di_{g_x}}{dt} + R_g i_{g_x} + u_{g_x} = 0 \tag{2.3}$$

By defining the term $\frac{v_{valve_x}^{(-)} - v_{valve_x}^{(+)}}{2}$ as e_{g_x}, the term $\frac{v_{valve_x}^{(+)} + v_{valve_x}^{(-)}}{2}$ as v_{circ_x} (i.e. *circulating voltage*), and the term $\frac{i_{up_x} + i_{low_x}}{2}$ as i_{circ_x} (i.e. *circulating current*), it is possible to obtain the mathematical expressions presented in 2.4 and 2.5, when 2.2 and 2.3 are respectively added and subtracted as in [17].

$$(\frac{L_{MMC}}{2} + L_g)\frac{di_{g_x}}{dt} + (\frac{R_{MMC}}{2} + R_g)i_{g_x} - e_{g_x} + u_{g_x} = 0 \tag{2.4}$$

$$-V_{dc} + 2L_{MMC}\frac{di_{circ_x}}{dt} + 2R_{MMC}i_{circ_x} + 2v_{circ_x} = 0 \tag{2.5}$$

The mathematical expressions shown in 2.4 and 2.5 reveals that the MMC unit can be studied as a dynamic system represented by two electrical circuits in which the e_{g_x} and the v_{circ_x} terms define, the corresponding AC and DC currents generated by the converter. Hereafter, this representation will be referred as the *Kirchhoff's based approach* of the MMC unit and its corresponding circuit diagram can be seen in Figure 2.6. The analysis of the DC circuit model given by the *Kirchhoff's based approach* (c.f. Figure 2.6) indicates that the defined *circulating voltage* (i.e. v_{circ_x}) is formed by DC and AC components instantaneously establishing the characteristics of the *circulating current* (i.e. i_{circ_x}).

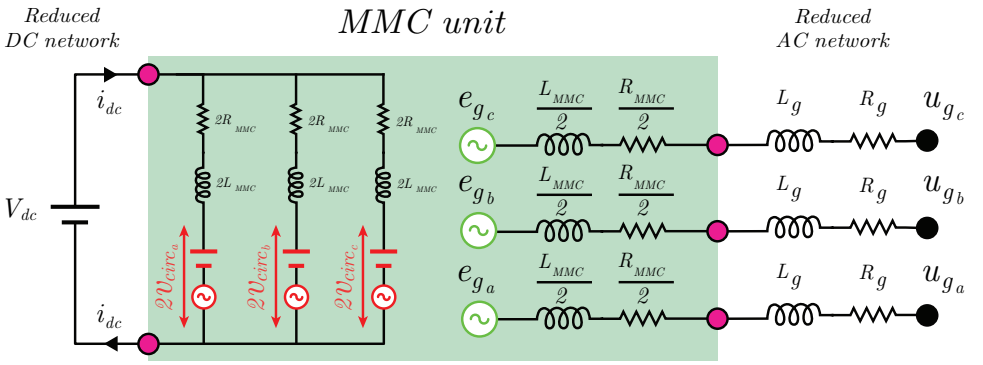

Figure 2.6: Electrical circuit model of the MMC unit (shown in Figure 2.5) considering a *Kirchhoff laws-based approach* for an EMT simulation framework.

In terms of i_{circ_x}, several scientific works have already indicated that a DC and a double frequency oscillation pattern $2w$ (i.e. double w.r.t. the oscillation pattern w of i_g) represent the main current components of i_{circ_x} (e.g. [18–22]). Moreover, the DC and the $2w$ components presented in each of the i_{circ_x} are balanced during steady-state conditions [20]. This means that the sum of the $2w$ currents becomes zero at the corresponding DC bus and additionally, the DC component in each i_{circ_x}, represents one-third of the DC current in Figure 2.6. On the other hand, the analysis of the AC circuit presented in Figure 2.6 shows that the defined voltages e_{g_x} instantaneously determines the characteristics of the grid currents i_{g_x}. Furthermore, the need of introducing a particular i_{g_x} current into the AC network

can be understood as a mathematical (instantaneous) restriction for the *per phase* currents i_{up} and i_{low} based on the equality shown in 2.1. These currents restrictions directly influence the terms e_{g_x} (shown in Figure 2.6) which means that the relationship established between $v^{(+)_{valve_x}}$ and $v^{(-)_{valve_x}}$ generating e_{g_x}, also gets bounded. However, the precise description of the corresponding currents i_{up_x} and i_{low_x} is completed as soon as the circulating current i_{circ_x} is defined. Similarly to the i_{g_x} current, the generation of a particular i_{circ_x} current also impose restrictions to the corresponding i_{up_x} and i_{low_x} currents which will also be reflected as boundaries for the $v^{(+)}_{valve_x}$ and $v^{(-)}_{valve_x}$ voltages. Thus, considering [13], a mathematical and graphical representation of these relationships (based on the definitions previously described for v_{circ_x} and i_{circ_x}) can be given in 2.6, 2.7 and illustrated in Figure 2.7.

$$\begin{pmatrix} i_{up_x} \\ i_{low_x} \end{pmatrix} = \begin{bmatrix} \frac{1}{2} & 1 \\ -\frac{1}{2} & 1 \end{bmatrix} \cdot \begin{pmatrix} i_{g_x} \\ i_{circ_x} \end{pmatrix} \tag{2.6}$$

$$\begin{pmatrix} v^{(+)}_{valve_x} \\ v^{(-)}_{valve_x} \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \cdot \begin{pmatrix} v_{circ_x} \\ e_{g_x} \end{pmatrix} \tag{2.7}$$

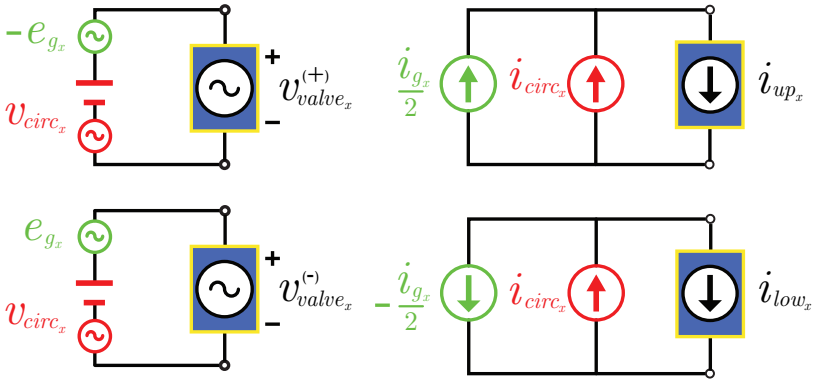

Figure 2.7: Electrical circuit representations of the current and voltage dependencies for each $valve$ (shown in Figure 2.5) considering the *Kirchhoff's approach* presented in Figure 2.6.

Figure 2.7 clearly shows that the corresponding voltages $v^{(+)}_{valve_x}$, $v^{(-)}_{valve_x}$, and currents i_{up_x} and i_{low_x} (across all the valves within an MMC unit) can only be known when all the i_{g_x}, i_{circ_x}, e_{g_x} and v_{circ_x} are clearly established. Usually, the criterion utilized (during normal operating conditions) to generate the references of the i_{g_x} currents is determined by control systems defining the amount of active and reactive power to be provided by the MMC unit to the AC network. On the other hand, several criteria that have been proposed (e.g. [23–25]), to define the DC and the AC references of the i_{circ_x} currents shown in Figure 2.6. For instance, it can seen in Figure 2.6 that if the AC current components in i_{circ_x} are minimized then, the associated losses within the MMC unit can be consequently reduced (i.e.

$\sum_a^c (i_{circ_x}^2 \cdot 2R_{MMC_x})$ can be reduced by minimizing the AC components of i_{circ_x}). This reduction is handled by a regulation system called *circulation current suppression controller* (CCSC) which utilizes a double frequency park's transformation [11] in order to reduce the main harmonic component (i.e. $2w$) within i_{circ_x}. Furthermore, it is also relevant to mention that most of the existing criteria defining the DC component in i_{circ_x} aim for regulating the balance between the DC power and the three-phase active power flowing through the MMC unit. One way of performing such a balance is by adjusting the reference of the DC component in i_{circ_x}, based on the ratio between the MMC's measured DC voltage, and the measured (average) active power provided by the converter to the AC network [24, 25].

Another way for establishing the reference of the DC component of i_{circ_x} is by utilizing a modelling approach based on the energy conservation principle. The energy conservation principle (proposed by G. Leibniz [26] several centuries ago) is utilized to formulate a power-balance mathematical description for representing the electrical circuit of an MMC unit (e.g. [7, 13, 24, 27–32]). In this *energy-based* approach, the simultaneous (and instantaneous) interactions between the powers input, the powers output, and the internal powers of the MMC unit are studied by using the relationships presented in 2.8 and 2.9. In short, the rates of change of the energy within the MMC unit are examined by defining the instantaneous (*per phase*) internal powers P_x^{Σ} and P_x^{Δ} as shown in 2.8 and 2.9.

$$P_x^{\Sigma} = \frac{dw_x^{\Sigma}}{dt} = v_{valve_x}^{(+)} i_{up_x} + v_{valve_x}^{(-)} i_{low_x} = -e_{g_x} i_{g_x} + 2v_{circ_x} i_{circ_x} \tag{2.8}$$

$$P_x^{\Delta} = \frac{dw_x^{\Delta}}{dt} = v_{valve_x}^{(+)} i_{up_x} - v_{valve_x}^{(-)} i_{low_x} = -2e_{g_x} i_{circ_x} + v_{circ_x} i_{g_x} \tag{2.9}$$

The power-balance relationships presented in 2.8 and 2.9 constitute the bases for designing dedicated control systems aiming for regulating the *per phase* energy level (i.e. w_x^{Σ} control) and the distribution of such energy (i.e. w_x^{Δ} control) between the *per phase* valves of the MMC [33]. Essentially, these energy control systems define the DC and AC references of i_{circ_x} in order to regulate the rate of change of w_x^{Σ} (c.f. 2.8) by typically assuming that the AC network power (described by $-e_{g_x} i_{g_x}$ in 2.8) is already established [25].

On the other hand, the w_x^{Δ} energy controllers are commonly used during abnormal power conditions in the AC network (e.g. a single phase fault event), to regulate the energy distribution between the upper and lower valves (c.f. 2.9) of the MMC unit [34]. This regulation process has been reported to be particularly useful to avoid the transferring of double frequency power fluctuations into the HVDC network [23]. Furthermore, the blocking of these power fluctuations has been observed by developing EMT simulation experiments which have highlighted the dynamic *energy-buffer* characteristics of the MMC technology [23, 35].

Nevertheless, the *energy-buffer* (or *energy-based*) modelling approach is not entirely aligned with the RMS type of simulation framework in which the instantaneous sinusoidal nature of the currents and voltages, as well as the harmonic analysis, are not directly considered. Consequently, and recalling that this thesis has an AC side (power system) focus, the phasor (RMS) model proposed in [36] is used for describing the energy conversion process in the MMC unit. In [36], the *Kirchhoff's based approach* is utilized and the representations of the electrostatic elements within the MMC unit are considered by including an equivalent capacitor C_{eq} in the DC side of the electrical circuit model. Moreover, the *CCSC* is assumed to completely eliminate the $2w$ component in i_{circ_x} simplifying in that way, the electrical circuit model of the MMC as shown in Figure 2.8.

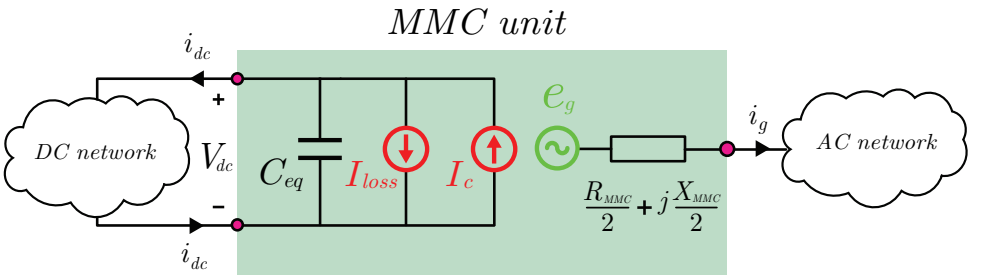

Figure 2.8: Electrical circuit model of an MMC unit based on the RMS approach proposed by [36].

In the phasor model proposed in [36], the DC side representation of the MMC unit (shown in Figure 2.6) is transformed into a Norton equivalent DC current source Ic. Additionally, the power-dissipating elements associated with the Norton transformation are replaced by another DC current source I_{loss} to represent the corresponding losses of the converter unit. Lastly, the C_{eq} term is calculated based on the number of submodules per valve N and the corresponding submodule's capacitance value C (c.f. Figure 2.5) multiplied by the number of valves (i.e. $C_{eq} = \frac{6C}{N}$).

2.2.2. Basic Regulation Schemes

Accordingly to [36], the control system's modelling of a MMC unit can be divided in two main sections (i.e. control layers) which are presented in Figure 2.9. As shown in Figure 2.9 each of these two sections (i.e. upper and lower-level control layers) are formed by several control blocks having specific regulation targets. For instance, the lower-level control layer generates the IGBT switching pulses for directly inserting (or excluding) the submodules' capacitors based on the *capacitor voltage balancing* and the $CCSC$ described in section 2.2.1.

Furthermore, the upper-level control layer is divided into two parts, the non-island control block, and the island control block. The island control block is typically utilized when an HVDC converter should self-generate the three-phase AC voltage waveform serving as the voltage reference for those networks mainly consisting of power electronic interfaced generation units (e.g. an offshore wind farm). On the

other hand, the non-island control block is mainly used in those HVDC converters which are connected to power systems where the three-phase AC voltage waveform (i.e. voltage reference) is already established. Thus, in the non-island control block, a current-based power control method is utilized by the MMC unit, considering several mathematical formulations which give a geometrical perspective to the energy conversion process.

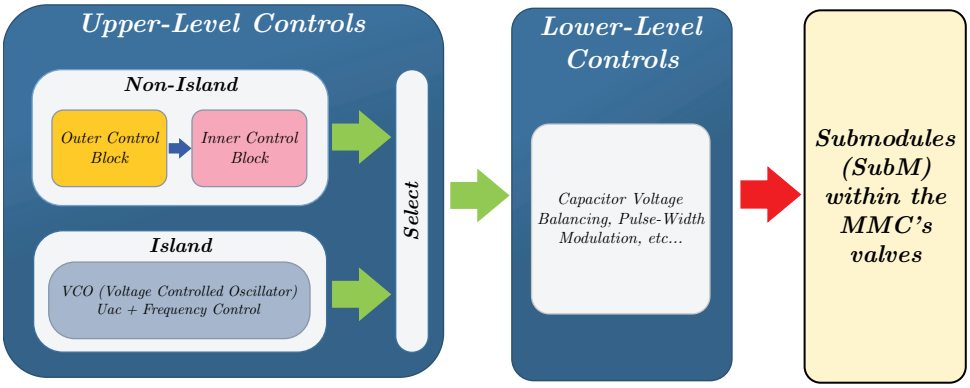

Figure 2.9: General description of the control layers of the MMC unit proposed by [36]. Green arrows representing the references of the voltage waveforms generated by the *Upper-Level Controls* section, and the red arrow representing the IGBT firing pulses generated by the *Lower-Level Controls* section.

In general, the geometrical perspective simplifies the design methodology of the AC power controllers in the MMC unit since it reduces the four-dimensional framework of the three-phase variables, into a two-dimensional framework (c.f. section 8.3.4). This simplification is obtained based on linear algebra transformations which combined with a phase-locked-loop (PLL) system, convert the three-phase AC network representation shown in Figure 2.8, in two virtually coupled DC circuits, ruled by the differential equations shown in 2.10 and 2.11.

$$\left(\frac{L_{MMC}}{2}+L_g\right)\frac{di_{gD}}{dt}=-\left(\frac{R_{MMC}}{2}+R_g\right)i_{gD}+w\left(\frac{L_{MMC}}{2}+L_g\right)i_{gQ}+e_{g_D}-u_{g_D} \quad (2.10)$$

$$\left(\frac{L_{MMC}}{2}+L_g\right)\frac{di_{gQ}}{dt}=-\left(\frac{R_{MMC}}{2}+R_g\right)i_{gQ}-w\left(\frac{L_{MMC}}{2}+L_g\right)i_{gD}+e_{g_Q}-u_{g_Q} \quad (2.11)$$

The PLL system used for all the RMS simulations carried out in this dissertation is based on a control block using an ideal *in-quadrature phase detector* approach which is inherently implemented in DiGSILENT PowerFactory 2018, and further described in [4]. Furthermore, the possibility of analyzing a three-phase network as two virtually coupled DC circuits, allows utilizing several controller design methods (e.g. space-state or frequency-response-based methods) for the establishment of the dynamic responses of the electrical currents i_D and i_Q [37]. Moreover, as the

voltage u_g is typically imposed by the power system, the control of the i_D and i_Q currents in the electrical DC circuits defined by 2.10 and 2.11 will determine the level of three-phase power supplied by the MMC unit to the AC network as shown in 2.12 and 2.13.

$$p = u_{g_D} i_{g_D} \tag{2.12}$$

$$q = -u_{g_D} i_{g_Q} \tag{2.13}$$

The relationships shown in 2.12 and 2.13 are obtained when the PLL system aligns the instantaneous-complex voltage vector (defined by the *instantaneous p-q theory* in [38]), with the synchronous reference frame as described in Appendix A. Furthermore, as shown in Figure 2.10, the structure of the current controllers is typically based on PI regulators which are usually calibrated to define the currents' time responses (for i_D and i_Q) considering a short millisecond time-frame (typically around 20ms, [39, 40]).

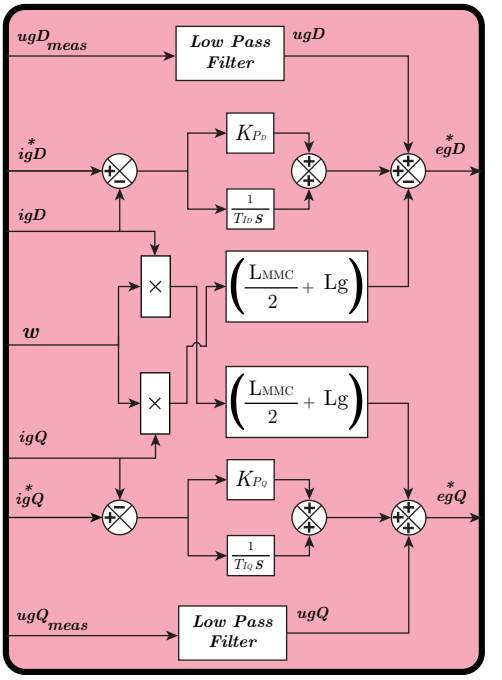

Figure 2.10: Internal structure of the *Inner Control* (Current) Block shown in Figure 2.9.

The calibration of the PI regulators of the current controllers is referred to the adjustment of their control gains (i.e. K_{P_D}, T_{I_D}, K_{P_Q}, and T_{I_Q} shown in Figure 2.10) in order to set up the corresponding voltage references $e^*_{g_D}$ and $e^*_{g_Q}$ based on the time-domain relationships presented in 2.14 and 2.15.

$$e^*_{gD} = u_{gD} - w\left(\frac{L_{MMC}}{2} + L_g\right)i_{gQ} + K_{P_D}(i^*_{gD_{Outer}} - i_{gD}) + \int \frac{(i^*_{gD_{Outer}} - i_{g_D})}{T_{I_D}}dt \quad (2.14)$$

$$e^*_{gQ} = u_{gQ} + w\left(\frac{L_{MMC}}{2} + L_g\right)i_{gD} + K_{P_Q}(i^*_{gQ_{Outer}} - i_{gQ}) + \int \frac{(i^*_{gQ_{Outer}} - i_{gQ})}{T_{IQ}}dt \quad (2.15)$$

The current controllers for i_D and i_Q belongs to the *Inner Control* block which receives the corresponding current references values (i.e. $i^*_{gD_{Outer}}$ and $i^*_{gQ_{Outer}}$ shown in 2.14 and 2.15) from the *Outer Control* block presented in Figure 2.9. As shown in Figure 2.11, the *Outer Control* block is essentially composed (in a VSC unit operating within a PtP-HVDC link) by four control modes which are responsible for managing the AC voltage level (i.e. U_{ACCtrl}), the DC voltage level, (i.e. $V_{dc_{Ctrl}}$), the reactive power level (i.e. Q_{Ctrl}), and the active power level (i.e. P_{Ctrl}), supplied by the converter (i.e. VSC unit).

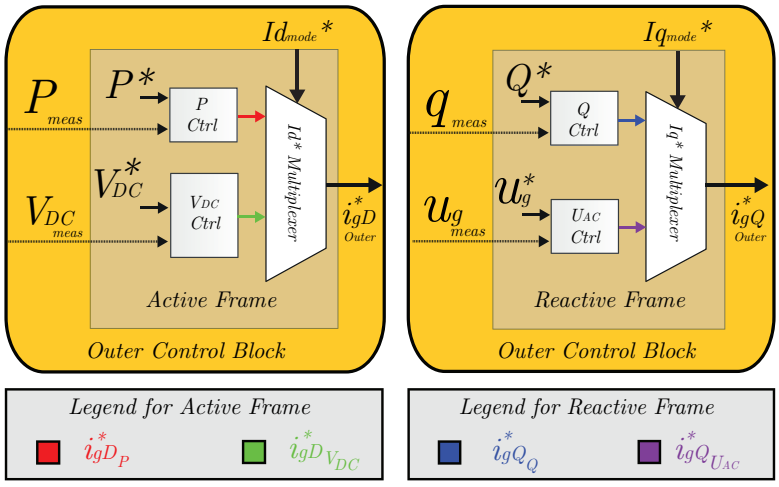

Figure 2.11: Control modes conforming the *Outer Control Block* shown in Figure 2.9.

Similarly to *Inner Control* block and as described in [36], the control modes within the *Outer Control* block utilize dedicated PI regulators which are meant to establish the dynamic responses of the corresponding variables (e.g. u_g, V_{dc}, q, or p), based on AC network requirements and the physical characteristics of the DC network. For instance, by neglecting the converter losses (i.e. $I_{loss} = 0$), the DC voltage V_{dc} in Figure 2.8, can be described through the currents balance equation shown in 2.16. Moreover, if the i_{dc} current is considered as an independent variable, the regulation process of the V_{dc} level will entirely depend on the I_c control.

$$C_{eq}\frac{dV_{dc}}{dt} = I_c - i_{dc} \quad (2.16)$$

Consequently, the design process of the PI regulator for V_{dc} can be developed by establishing a reference current I_c^* which depends on the i_{dc} current and the corresponding $K_{P_{DC}}$ and $T_{I_{DC}}$ gains as shown in 2.17.

$$I_c^* = i_{dc} + K_{P_{dc}}(V_{dc}^* - V_{dc}) + \int \frac{(V_{dc}^* - V_{dc})}{T_{I_{DC}}} dt \tag{2.17}$$

Additionally, it can be noticed that when multiplying 2.16 by V_{dc}, the resulting equation describes the power balance relationship between the AC and DC networks coupled by the MMC unit where the term $V_{dc}I_c$ represents (from a DC side perspective) the active power taken by the converter unit from the AC network. Moreover, it is convenient to remember that the active power p was already defined in 2.12 as a function of u_{g_D} and i_{g_D}. Hence, as the u_{g_D} term is typically known, the I_c^* adjustment is equivalent to the $i_{g_D}^*$ current adjustment as presented in 2.18. The absolute values shown in 2.18 just highlight the fact that special attention must be given to the sign conventions utilized for defining the power flow directions in the converter unit from a DC and an AC side perspectives.

$$|V_{dc}I_c^*| = |u_{g_D}i_{g_D}^*| \tag{2.18}$$

Furthermore, the adjustments of the PI regulators within the AC voltage (i.e. $U_{AC_{Ctrl}}$), active (i.e. P_{Ctrl}), and reactive power (i.e. Q_{Ctrl}) control blocks (shown in Figure 2.11) are developed by considering the characteristics of the AC network in which the VSC unit is connected to. Such characteristics are typically referred to the inertia level and the associated short circuit power capabilities of the AC network [41, 42]. Therefore, once these AC network characteristics are determined, several time-domain simulation experiments are typically performed in order to establish the adjustment of these PI regulators' parameters.

It is also worth mentioning that although the adjustment of the PI regulators associated with the *Outer Control* block uses the characteristics of the AC and DC networks to be performed, there are additional considerations that should also be taken into account. For instance, the need for avoiding adverse control interactions between the *Outer* and *Inner control* blocks is typically handled by establishing different bandwidth ranges (i.e. time scales) between these blocks [43]. On the other hand, it is suitable to utilize additional methodologies [44, 45], to optimize the selection of the control modes parameters (within the *Outer Control* block), to avoid an adverse interplay between a VSC unit and electrically close AC network control devices (e.g. power system stabilizers).

2.3. Power flow regulation process

Independently of the DC network topology, the power flow regulation process in a HVDC link is carried out by adjusting the DC voltage level between the VSC units within a HVDC network. However, depending on the HVDC network topology, the control strategies utilized for adjusting the DC voltage level can be different. For

that reason, it is convenient to describe for each HVDC network topology the control strategies utilized for adjusting the DC voltage across the HVDC network. For simplicity, this description will be developed by considering symmetrical monopole systems (c.f. Figure 2.2a) since so far [46–48], represents the most common type of VSC-HVDC link installation in the world.

2.3.1. Point-to-Point (PtP) VSC-HVDC links

In a symmetrical monopole PtP-VSC-HVDC link (c.f. Figure 2.2), the power flow within the HVDC network is typically managed by setting up one of the converter stations to control the DC voltage (by using DC_{Ctrl}), while the other converter station regulates the active power transferred to the AC network (by using P_{Ctrl}). In this way, the DC voltage is kept constant at the rectifier VSC unit of the HVDC link by absorbing active power from the adjacent AC network as described by the expression 2.15. On the other hand, in the inverter VSC unit, the active power control adjusts the $i^*_{g_D}$ value to define the amount of active power supplied to the adjacent AC network. This adjustment essentially induces a reduction of the DC voltage level at the DC terminals of the inverter VSC unit, and consequently, a DC current flow appears in the HVDC cable.

The DC power coordination process between the rectifier and the inverter VSC units of the PtP-VSC-HVDC link is typically known as the *master-slave* control [49] which is commonly described by utilizing a power vs voltage (i.e. P vs V_{dc}) *diagram* as shown in Figure 2.12, where the corresponding operational limits of the rectifier (VSC01) and inverter (VSC02) units within the PtP-VSC-HVDC link are defined.

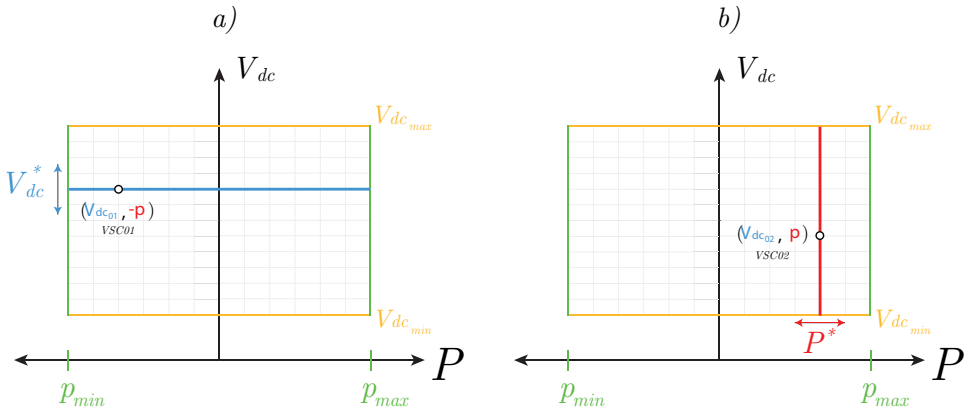

Figure 2.12: DC voltage and active power control characteristics of a point-to-point VSC-HVDC as shown in [50]. a) $V_{dc_{Ctrl}}$ representation within the Power vs DC Voltage diagram of a rectifier (VSC01) unit. b) P_{Ctrl} representation within the Power vs DC Voltage diagram of an inverter (VSC02) unit.

As each of the VSC units of the symmetrical monopole link (c.f. Figure 2.2) are connected through the point-to-point HVDC cables, the initial conditions (V_{dc_0},p_0) shown in Figure 2.12 (for each of the VSC units) are strongly correlated and defines

the steady-state DC power level transmitted through the HVDC link. The effects of this correlation can be better noticed as soon as one of the corresponding references (i.e. V_{dc}^{*} or P^{*}) in Figure 2.12 is modified. As an example, if in the rectifier VSC01 unit, the V_{dc}^{*} (represented by the horizontal blue line in Figure 2.12a) is increased (upward displacement), the steady-state operational condition (V_{dc},p) will be modified according to the V_{dc}^{*} displacement. Furthermore, the upward change of V_{dc}^{*} at the VSC01 unit will also induce an upward displacement of the steady-state operational voltage (i.e. V_{dc_0}) at the inverter VSC02 unit shown in Figure 2.12b. This induced V_{dc_0} upward displacement in VSC02 is generated since the active power control (i.e. P_{Ctrl}) of VSC02 kept constant the supplied active power level by adjusting the $i_{g_D}^{*}$ current which results in an increment of the V_{dc_0} value at VSC02.

On the other hand, if another example considering a modification of the active power reference (P^{*}) in VSC02 is studied, then it will be observed that a horizontal and a vertical displacement of the steady-state operational condition (V_{dc_0},p_0) shown in Figure 2.12b will occur. Conversely, to the previous V_{dc}^{*} modification example, the change of P^{*} in VSC02 will only induce a horizontal displacement of the steady-state operational condition of the VSC01 shown in Figure 2.12a since the V_{dc}^{*} is kept constant at VSC01.

It is worth pointing out that as the steady-state operational conditions (V_{dc_0},p_0) in Figure 2.12 are mutually dependent, special attention is needed when analyzing the potential effects of AC network disturbances in terms of undesirable displacements of the (V_{dc_0},p_0) steady-state operational conditions. These undesirable displacements would graphically represent that the (V_{dc_0},p_0) points would go beyond the regions defined by the power or voltage limits (i.e. $V_{dc_{max}}$,$V_{dc_{min}}$, p_{max} and p_{min}) shown in Figure 2.12. Consequently, a methodology for modifying the voltage and power references (i.e. V_{dc}^{*} and P^{*}) called *Voltage Margin* control is commonly considered to avoid exceeding the power and DC voltage limits within the HVDC network [51–53].

2.3.2. Multi-Terminal (MT) VSC-HVDC links

As mentioned in [54], the DC voltage adjustment of the VSC units is the most relevant process in terms of the regulation of the DC power flows within a MT-VSC-HVDC network. In that sense, a control strategy known as the *Droop* control represents one of the most studied methods for distributing the regulation of the DC voltage control (i.e. establishing the power sharing) across the VSC units of the MT-VSC-HVDC network [50, 55–57]. Similarly to the master-slave control mentioned in section 2.3.1, the *Droop* control (i.e. $Droop_{Ctrl}$) can also be represented within the P vs V_{dc} *diagram* as illustrated in Figure 2.13

In essence, the $Droop$ control typically utilizes local measurements [55] for altering either the DC voltage reference (i.e. V_{dc}^{*}), or the reference of the active power (i.e. P^{*}), in a converter unit based on the proportional factor K_{Droop} as

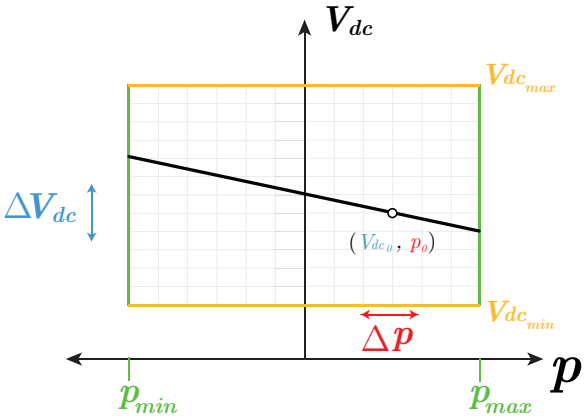

Figure 2.13: $Droop_{Ctrl}$ representation within the Power vs DC Voltage diagram of a VSC unit, as presented in [50].

shown in 2.19 and 2.20.

$$V_{dc}^{*} = V_{dc_0} - K_{Droop_{dc}}(P_{meas} - p_0) \tag{2.19}$$

$$P^{*} = p_0 - K_{Droop_p}(V_{DC_{meas}} - V_{dc_0}) \tag{2.20}$$

It is interesting to notice that if in 2.19, the $K_{Droop_{dc}}$ factor is zero, the resulting relationship would describe the steady-state condition expected from the $V_{dc_{Ctrl}}$ presented in Figure 2.12a. This implies that the role of the $K_{Droop_{dc}}$ factor is to define the influence of the measured active power (i.e. P_{meas}) in a VSC unit, over its DC voltage reference (i.e. V_{dc}^{*}). On the other hand, the relationship 2.20 indicates that similarly to 2.19, the K_{Droop_p} factor is used to define the influence of the measured DC voltage (i.e. $V_{dc_{meas}}$) in a VSC unit over its active power reference (i.e. P^{*}). Consequently, the nullification of the K_{Droop_p} in 2.20, will lead to describe the steady-state condition expected from the P_{Ctrl} presented in Figure 2.12b.

It is also convenient to clarify that the VSC units forming a multi-terminal HVDC network, can also utilize the power flow control methods described in section 2.3.1. However, the determination of the type of control modes to be used in a multi-terminal HVDC network depends on several aspects. These aspects are in general referred to the number of VSC units forming the MT-VSC-HVDC link [58], the types of contingencies to be considered (e.g. outage of a converter station) [59], and the expected requirements associated to the dynamic responses of the active power and DC voltage under fault events [53].

2.3.3. Expandable PtP-VSC-HVDC links

The *expandability* of a PtP-VSC-HVDC link has been defined in [60] as the ability to add one or more VSC stations to the existing point-to-point HVDC link in order

to form a multi-terminal VSC-HVDC network capable of operating as such during energization, steady-state, and fault conditions. In that sense, an example of such *expandability* is observed in Figure 2.14, where a PtP-VSC-HVDC link is planned to be *expanded* as a multi-terminal (adding a third terminal) offshore VSC-HVDC link.

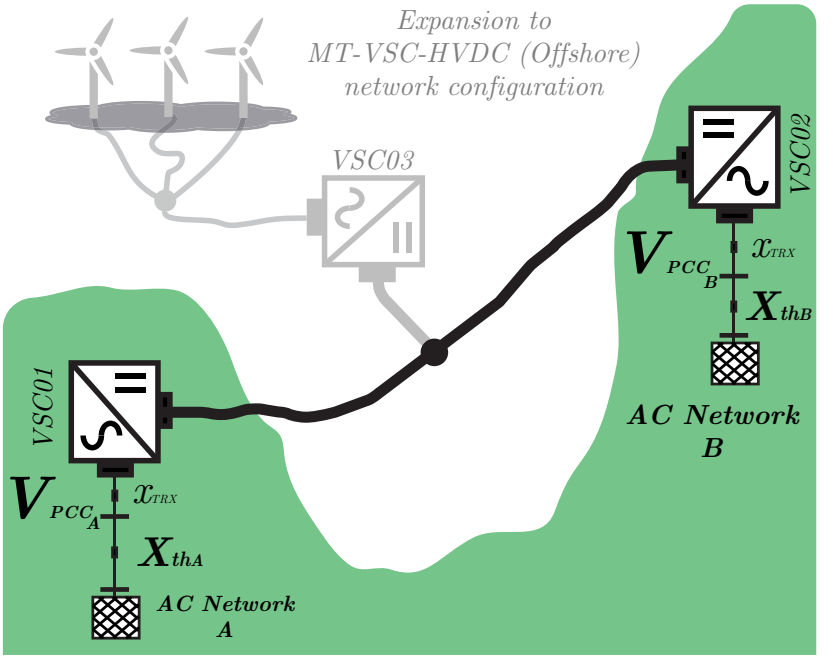

Figure 2.14: Example of a multi-terminal expanded PtP-VSC-HVDC link. The PtP-VSC-HVDC link represented by the elements highlighted in black colour is expanded to form a multi-terminal (three-terminals) VSC-HVDC link by adding the elements highlighted in grey colour.

Recently, the *expandability* of an HVDC link has received more attention from an academic and industrial perspective due to the increasing proliferation of VSC-HVDC links [61]. As discussed in [62], the *expandability* of the HVDC links constitutes a challenge, in terms of technical interoperability, especially if the VSC units belong to different converters manufacturers (i.e. multi-vendor scheme for HVDC links). For that reason, definitions [62], and methodologies [63–68] are currently being discussed for evaluating those technical aspects ensuring suitable levels of voltage control, power quality, and security of supply of the multi-terminal VSC-HVDC links.

In this regard, one of the most important functions that needs to be considered for the expansion of a PtP-VSC-HVDC link is the DC power flow regulation. As indicated in [69], the ability to regulate such DC power can be theoretically achieved, if the access for modifying the DC voltage reference of the VSC units is ensured. However, if the access for modifying the DC voltage reference is not ensured, then, modifications in the VSC units' control systems and/or the addition of HVDC network

elements (e.g. DC choppers) should be envisaged to ensure the multi-terminal (MT) operation of an expandable PtP-VSC-HVDC link.

In this connection, a solution for developing a multi-vendor DC power flow regulation in a VSC-HVDC link (based on the design of a primary control interface) has been presented in [69]. The primary control interface is used as a medium to provide the reference of the DC voltages, based on a *Droop Line Tracking* (DLT) method. The full description of the DLT method is explained in further detail in [70], but in short, its mathematical formulation can be expressed as shown in 2.21. Here, the term e, represents a non-linear multi-variable scalar function depending on the p_{meas}, the $V_{dc_{meas}}$ and two additional terms contained within a predefined (and adjustable) trajectory, located over the P vs V_{dc} *diagram* of the controlled VSC unit.

$$V_{dc}^{*} = V_{dc_{meas}} + e \tag{2.21}$$

It is interesting to notice in 2.21 that, if the non-linear multi-variable scalar function e is designed to be: $e = V_{dc_{Nominal}} - V_{dc_{meas}}$; the obtained relationship would describe the trajectory associated to the $V_{dc_{Ctrl}}$ shown in Figure 2.12a. Here, $V_{dc_{Nominal}}$ represents the constant value associated to the nominal DC voltage of the VSC-HVDC link. This description suggests that in general, the trajectories presented in Figure 2.12 and Figure 2.13 associated with the P_{Ctrl} and the $Droop_{Ctrl}$ (or even more complex piecewise trajectories as in [58, 71]) can also be obtained for a VSC unit, depending on the e value provided by DLT method.

In this connection, the applicability of the DLT-based DC power flow regulation depends on three fundamental aspects (requirements). The first aspect is the access to the regulation of the DC voltage references in those VSC units meant to define the power flow distribution within the *expandable* HVDC link. Here, it is relevant to consider that, as presented in [72], the regulation of the DC voltage response in a VSC (MMC) offers more consistent transient behavior when the zero sequence (DC) component of the circulating current is directly adjusted. This would imply that the internal energy level of the MMC unit (i.e. w_x^{Σ} in 2.8) must be regulated through the adjustment of the $i_{g_D}^{*}$ current shown in 2.10. Consequently, the applicability of the DLT method for carrying out the DC voltage regulation will depend on the internal energy balance strategy utilized by an MMC unit.

The second aspect is the access to the real-time (instantaneous) information of the measured DC voltage level (i.e. $V_{dc_{meas}}$) and the measured DC power level (i.e. p_{meas}) of those VSC units described in the first aspect. Here, the methodologies for reducing the delays associated with the transmission of the corresponding measurements and reference orders for the DC voltages of the VSC units will need to be defined (at least) considering the associated time constants of the HVDC network.

The third aspect is the establishment of the trajectory over the P vs V_{dc} *diagram* that needs to be used by the DLT method. The establishment of this trajectory rep-

resents the desired behavior in terms of DC the voltage and the DC power response of a particular VSC unit within the *expandable* HVDC network. Consequently, as the DC and AC networks can experience disturbances affecting the AC/DC power balance, the criterion for establishing such a trajectory is a process that depends on extensive power flows distribution and contingency analysis of the *expandable* HVDC link. In that sense, Chapter 6 of this thesis, proposes a method for the compliance of the post-fault active power recovery requirements (presented in [73]) in a VSC unit affected by an electrically close balanced AC fault. The proposed method utilizes the DC voltage level and the active power level of the affected VSC unit to redefine its DC voltage reference, providing in that way a solution to be considered for the formulation of a possible trajectory to be evaluated during the contingency analysis of *expandable* VSC-HVDC links.

2.4. Challenges for expandable PtP-VSC-HVDC links

The power flow regulation process (discussed in section 2.3) is a relevant aspect of the multi-terminal expansion of a point-to-point VSC-HVDC link, there are other relevant aspects to consider when a point-to-point HVDC link is planned to be expanded for multi-terminal operation. These aspects are related to the protection philosophy (i.e. type of strategies and technologies) to be used by the protecting elements within the multi-terminal DC network, (e.g., High Voltage DC circuit breakers (DCCB)). Another aspect to be taken into account, it's the type of devices needed for establishing the DC side connection of point-to-point VSC-HVDC links operating at different DC voltage levels (e.g. DC/DC transformers), and the coordination of such devices with the actual power flow regulation process.

The VSC units' interaction analysis following the connection between point-to-point links manufactured by different vendors also represents an aspect of concern, due to the lack of standardization for the development of multi-terminal multi-vendor VSC-HVDC networks. All these aspects constitute relevant DC-side challenges for the implementation of expandable PtP-VSC-HVDC links that are beyond the scope of work of this dissertation. This dissertation tackles the AC-side type of challenges for expandable PtP-VSC-HVDC links described in section 1.1 of this dissertation.

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3

Supplementary active and reactive power controllers for VSC-HVDC links

In this chapter supplementary control blocks are incorporated as part of the regulation schemes of the RMS model presented for VSC-HVDC links in Chapter 2. Additionally, the methodology for the implementation of such supplementary control blocks is described in detail as well as their corresponding implications in terms of the support provided to the AC network during disturbance and steady-state conditions.

The results presented in this chapter have been published in:

A. Perilla, J. L. Rueda Torres, E. Rakhshani, R. Irnawan, F. Faria da Silva, M. van der Meijden, C. L. Bak, A. Alefragkis, and A. Lindefelt, *Directional derivative-based method for quasi-stationary voltage support analysis of single-infeed VSC-HVDC units*, High Voltage 5, 511 (2020).

A. Perilla, J. L. Rueda Torres, A. A. van der Meer, M. van der Meijden, and A. Alefgrakis, *Influence of Active Power Gradient Control of an MMC-HVDC Link on Long-Term Frequency Stability*, in 2017 IEEE Power and Energy Society General Meeting (PESGM) (2017).

A. Karaolanis, A. Perilla, J. L. Rueda Torres, M. van der Meijden, and A. Alefragkis, *Generic model of a VSC-based HVDC link for RMS simulations in PSS/E*, in 2018 10th IFAC Symposium on Control of Powerand Energy Systems (CPES) 2018.

3.1. Description of the supplementary control modes

The European HVDC grid code [1] established in 2016 that besides the basic regulation schemes described in 2.2.2, the HVDC systems should be capable of providing additional (supplementary) support functions for the stability of the European Power Systems. These additional support functions are carried out by supplementary control modes which need to be developed and incorporated into the generic RMS model described in [2]. In that way, the performance of such supplementary controllers can be analyzed to ensure the stability of the power system by examining the operation of the VSC-HVDC link during steady-state and/or fault conditions. A summary of the differences between the basics and the supplementary control modes indicated in [1] (in terms of the active or reactive power management), are presented in Table 3.1.

Table 3.1: Basic and supplementary control modes demanded for VSC-HVDC links in Europe [1].

Control Modes	Affecting Reactive Power (Voltage) Management	Affecting AC/DC Power Management
Basic [2]	$U_{AC_{Ctrl}}$ Q_{Ctrl}	$V_{dc_{Ctrl}}$ P_{Ctrl}
Supplementary [1]	PF FRT	f_{Ctrl} $PFAPR$

Table 3.1 shows that the supplementary control modes can be classified depending on their influence over the management of the active and reactive power supplied by a VSC-HVDC link. As indicated in [1], the frequency control (f_{Ctrl}) and the post-fault active power recovery ($PFAPR$) affect the AC/DC power balance in a VSC-HVDC link. On the other hand, the power factor (PF) and the fault ride through (FRT) control modes are essentially designed to adjust the level of reactive power supplied to the power system depending on the AC network conditions.

On the other hand, there are more supplementary control functions demanded in the current European HVDC grid code [1]. However, the focus of this thesis is limited to the supplementary control modes indicated in Table 3.1. Therefore, the design criteria and the implementation of the supplementary control modes shown in Table 3.1 are developed in section 3.2, section 3.4, section 3.3, chapter 5, and chapter 6 respectively.

3.2. Power Factor control mode for VSC-HVDC units

3.2.1. Power Factor definition and the *P/Q capability diagram*

For three-phase systems under sinusoidal and balance conditions, the IEEE has defined the PF in [3] as a non-linear mathematical relationship between the active power (P) and the apparent power (S), as described in 3.1 and 3.2.

$$PF = \frac{P}{|S|} \tag{3.1}$$

$$|S| = \sqrt{P^2 + Q^2} \tag{3.2}$$

The relationships presented in 3.1 and 3.2 show that the PF is a non-linear function that depends on the active (P) and reactive (Q) power. Consequently, the proposed dynamic PF control (i.e. PF_{Ctrl}) is designed here by considering the IEEE PF definition, and the power limits of a VSC-HVDC unit.

As described in [4], the *P/Q capability diagram* indicates the power limits of a VSC-HVDC unit as shown in Figure 3.1. Furthermore, the *P/Q capability diagram* is also utilized to define the steady-state operational region (blue coloured in Figure 3.1) of a VSC-HVDC unit.

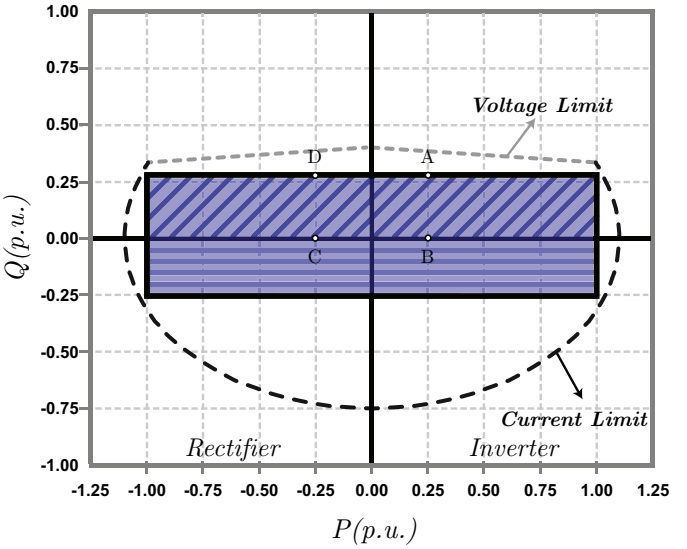

Figure 3.1: Example of *P/Q capability diagram* of a VSC-HVDC unit [4].

As the steady-state power conditions of a VSC-HVDC unit are indicated by the *P/Q capability diagram*, such conditions can be used by the expression 3.1 and 3.2, to identify the associated steady-state limits of the PF as described in section 3.2.2.

3.2.2. Defining a *P/PF capability diagram*

The determination of the PF steady-state limits in a VSC-HVDC unit represents a necessary step for the design of the PF_{Ctrl}. This step can be done by proposing a *P/PF capability diagram* as shown in Figure 3.2. In Figure 3.2, the positive and negative values of the PF are referred to the capacitive and inductive reactive power supplied by the VSC-HVDC unit respectively. For the sake of illustration, the ABCD points shown in Figure 3.1 are projected into the in Figure 3.2 to appreciate the relationship between both operational regions.

It is interesting to realize in Figure 3.2 that the inductive or the capacitive quad-

rants of the PF are not connected with each other, except when the PF and the active power are simultaneously null. This particular condition is created by the mathematical definition of the PF (c.f. 3.1 and 3.2) that reveals the fact that independently of the reactive power supplied, the PF will always be zero if the active power transmitted by the VSC-HVDC is null. The associated problem (in terms of the PF_{Ctrl} design) to this particular condition can be easily understood if the direction of the active power in a VSC-HVDC unit changes. As an example, the unity power factor defined by the segment BC (in Figure 3.2) cannot be maintained when the level of the active power in a VSC-HVDC unit goes to zero (c.f. expressions 3.1). Therefore, the design process of a PF_{Ctrl} must be developed considering this particular condition, especially for those VSC-HVDC units foreseen to transmit active power in a bidirectional way (i.e. positive and negative active power) to an AC network.

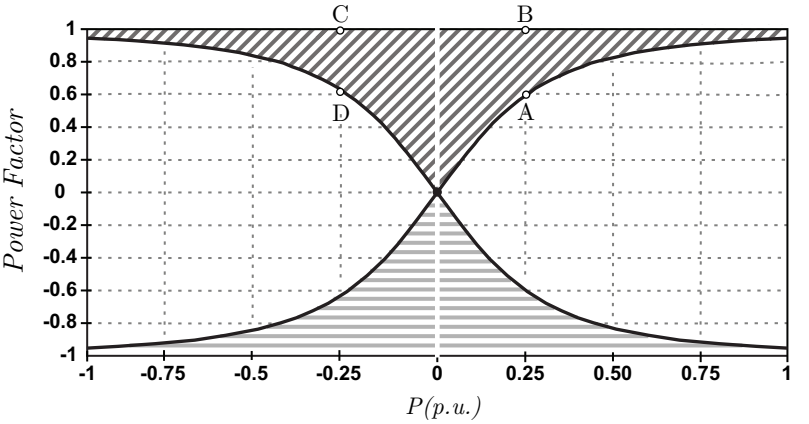

Figure 3.2: *PF-P diagram* of a VSC-HVDC unit. The shape of the *PF-P diagram* is a consequence of the non-linear PF definition established by the IEEE, and the steady-state VSC-HVDC unit's power limits.

3.2.3. Designing and Implementing a PF_{Ctrl}

The mathematical description indicated in 3.1 and 3.2 revealed that the PF can be controlled by either adjusting the active power level or by either adjusting the reactive power level supplied by a VSC-HVDC unit. Therefore, as the active power is usually established as part of the primary objectives of the electricity markets, the reactive power represents the most feasible variable to perform the PF regulation.

Accordingly with [1], the PF shall be controlled to a specific target at the connection point of the VSC-HVDC unit. On the other hand, as the active power level provided by the VSC-HVDC unit might change, the reactive power level must be accordingly adjusted, to keep the desired PF target. Additionally, as described in section 3.2.2, the PF_{Ctrl} faces a challenge when the PF level must be kept during an active power reversal order in a VSC-HVDC unit. However, this challenge can be overcome if, within the design process of the PF_{Ctrl}, an additional parameter

(requirement) is incorporated. Essentially, this additional parameter represents an *active power deadband* (i.e. $P_{deadband}$) that needs to be defined in order to relax the regulation of the PF during the transition (reversal) period of the active power. This parameter will facilitate the utilization of a conventional PI regulator to perform the adjustment of the PF without altering the reactive power level during the reversal period of the active power in a VSC-HVDC unit. Consequently, the PF_{Ctrl} can be added within the reactive frame of the *Outer Control* block presented in section 2.2.2 as shown in Figure 3.3a.

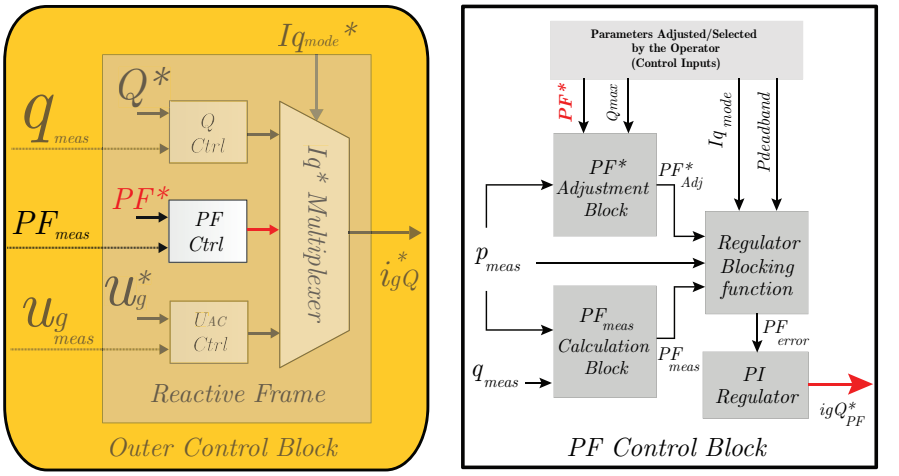

Figure 3.3: Description of the PF Control Block. a) Showing the proposed PF_{Ctrl} as a new control block introduced within the *Reactive Frame* of the *Outer Control Block*. b) Showing the control blocks located within the proposed PF_{Ctrl}.

As seen in Figure 3.3, the proposed PF_{Ctrl} is compounded by five control blocks. The first control block is the one providing those inputs signals for the PF_{Ctrl} such as: the reference of the PF (i.e. PF^*), the maximum reactive power that the converter can supply (i.e. $Qmax$), the signal defining the used reactive control mode (i.e. Iq_{mode}), and $P_{deadband}$. The second control block (PF^* *Adjustment Block* in Figure 3.3) utilizes the measurement of the active power (i.e. p_{meas}) and the PF^* defined by the operator (positive for capacitive and negative for inductive), in order to generate an adjusted PF reference (i.e. PF^*_{Adj}). The PF^*_{Adj} reference is generated based on the mathematical relationships presented in 3.3 and 3.4.

$$PF^*_{Adj\_Cap} = \begin{cases} PF^*_{Cap} & \text{if } PF^*_{Cap} \geq \frac{|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} \\ \frac{|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} & \text{if } PF^*_{Cap} < \frac{|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} \end{cases} \tag{3.3}$$

$$PF^*_{Adj\_Ind} = \begin{cases} PF^*_{Ind} & \text{if } PF^*_{Ind} \leq \frac{-|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} \\ \frac{-|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} & \text{if } PF^*_{Ind} > \frac{-|p_{meas}|}{\sqrt{p^2_{meas}+Q^2_{max}}} \end{cases} \tag{3.4}$$

As shown in Figure 3.3b, the third block is the one responsible for computing the actual capacitive or inductive value of the PF (c.f. 3.1 and 3.2), based on the measurements of the active and reactive power (i.e. p_{meas} and q_{meas}) supplied by the VSC-HVSC unit. The forth block is essentially a *regulator blocking function* (RBF) which provides the corresponding PF error signal (i.e. PF_{error}) to the fifth block (i.e. PI regulator in Figure 3.3b). The PF_{error} signal provided by RBF will be null if the PF_{Ctrl} has not been selected to operate (i.e. Iq_{mode} state is zero), and if the modulus of the actual active power transmitted by the VSC-HVDC unit is lower than the $P_{deadband}$. Hence, the mathematical relationship between the PF_{error} and the $P_{deadband}$ is shown in 3.5.

$$PF_{error} = \begin{cases} PF^{*}_{Adj} - PF_{meas} & \text{if } |p_{meas}| > P_{deadband} \\ 0 & \text{if } |p_{meas}| \leq P_{deadband} \end{cases} \tag{3.5}$$

As seen in Figure 3.3b, the PI regulator of the proposed PF_{Ctrl}, generates the reactive current reference signal (i.e. igQ^{*}_{PF}) for the current control block presented in Figure 2.10, based on the PF_{error} described in 3.5. Moreover, it is interesting to notice that, the regulation of the PF essentially leads to a link between the rate of change of reactive power or reactive power gradient (RPG) and the rate of change of active power or active power gradient (APG). This link can be scaled up (or down) depending on the λ parameter as defined in 3.6.

$$|RPG| = |\lambda| \cdot |APG| \tag{3.6}$$

The relationship presented in 3.6 is obtained as soon as the implication of having a PF_{Ctrl} capable of maintaining a constant PF is formulated by nullifying the rate of change of the PF (i.e. $\frac{dPF}{dt} = 0$) linked to 3.1. Additionally, the term λ in 3.6 represents the PF value (defined by PF^{*}) to be kept constant by the PF_{Ctrl}. On the other hand, the relationship presented in 3.6 is only applicable for those active power levels outside of the $P_{deadband}$ range. Consequently, as the PF regulation (i.e. adjustment of the reactive power) depends on the relationship presented in 3.6, and also in the established value for $P_{deadband}$, it is recommended to utilize relatively low values (e.g. less than 5% of the nominal VSC-HVDC active power) for $P_{deadband}$. This recommendation will prevent an abrupt change in the igQ^{*}_{PF} (i.e. the state variable output of the PI regulator), during an active power reversal.

3.2.4. Simulation setup and numerical results of the PF_{Ctrl}

The analysis of the performance associated with the proposed PF_{Ctrl} is developed by proposing simulation experiments where a three-area (PST16 benchmark) power system (containing high voltage tie-lines as described in [5]) is considered. In the proposed simulation experiment, the tie-line connecting the areas B and C has been replaced by a 700MW±230MVAr PtP-VSC-HVDC link (represented by a dash line) mimicking the power flow conditions associated with the replaced tie-line presented in Figure 3.4.

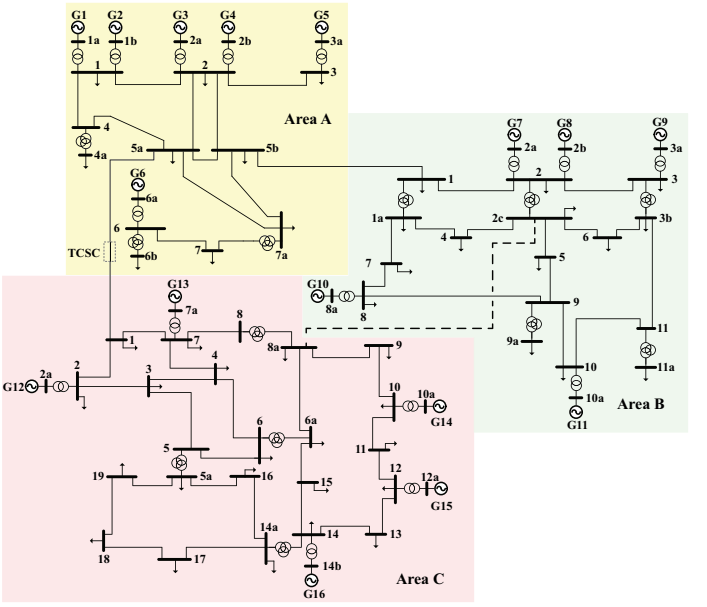

Figure 3.4: PST16 benchmark system from [5, 6] including the PtP-VSC-HVDC link (represented as a dashed line) between terminals B2c and C8a.

This tie-line replacement is done to study the effects of an active power reversal event in terms of the reactive power management associated with the proposed PF_{Ctrl}. The PtP-VSC-HVDC link incorporates the proposed PF_{Ctrl} as presented in Figure 3.3, and its corresponding modelling parameters are further described in [5, 6].

The developed simulation experiments consisted of two case studies. The first case study provides a comparison between the dynamic response of the proposed PF_{Ctrl} against the dynamic response of a (field tested) PF_{Ctrl} for a utility-scale PV power plant [7]. Furthermore, in the second study case, the influence over the AC voltage's magnitude and the reactive power deployment (associated with the proposed PF_{Ctrl}) is analyzed, during an active power reversal action in the PtP-VSC-HVDC link.

Fist study case (Step Change Analysis)

The comparison process of the PF_{Ctrl} against the work developed in [7], starts by matching the active and reactive power set points in one of the converter stations of the PtP-VSC-HVDC link (c.f Figure 3.4) w.r.t. the power levels indicated in [7]. The matching process of active and reactive power is made in converter station VSC02 (located in area C) to be aligned in terms of the power flow direction. The active and the reactive power are set up to −206.84MW and 42MVAr respectively (negative active power reference at station VSC02 implies DC power flowing from Area C to Area B). In that way, the (capacitive) PF provided by the converter station

VSC02 results 0.98.

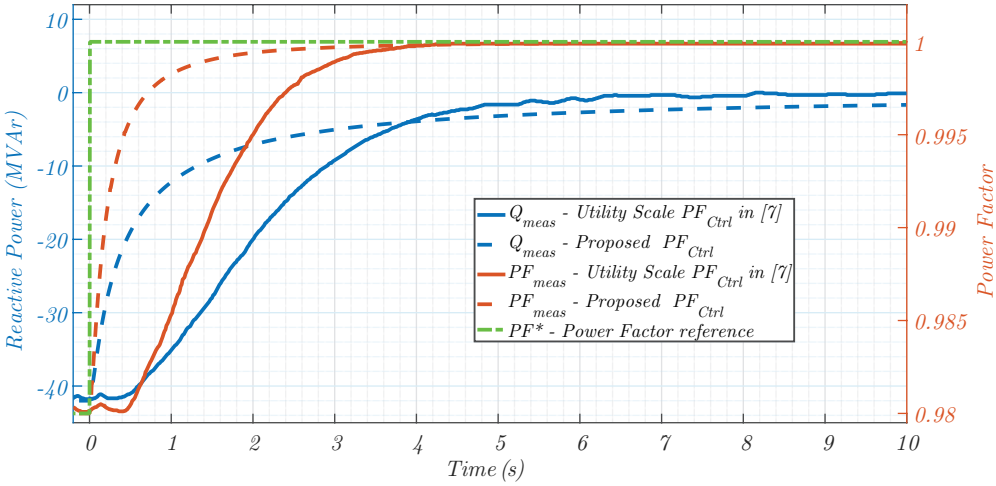

Figure 3.5: Comparison of a field test dynamic power factor controller shown in [7] (continuous lines), vs the proposed PF_{Ctrl} (dashed lines).

The PF controller's response is assessed by increasing the PF^* (from 0.98 to 1.0) as shown in Figure 3.5. As described in [7], with the utility-scale PV power plant, the rise time (i.e., the time needed to reach 90% of the steady state value) provided by the PF_{Ctrl} was around 3.2s, and it is presented Figure 3.5. However, with the proposed PF_{Ctrl}, it is observed a reduction of the rise time (around 1s of enhancement), providing in that way a faster PF regulation as seen in Figure 3.5.

Second study case (Power Reversal Analysis)

In this study case, the active and reactive power set-points of the converter station VSC02 were set to 150MW and -180MVAr respectively. These power level conditions were established in order to evaluate the performance of PF_{Ctrl} during an active power reversal event while operating with a particularly low (0.64) PF (inductive) value. Moreover, the corresponding APG (c.f. 3.6) has been set up to 999MW/min, which constitutes the maximum APG value allowed (during normal operating conditions) for the COBRAcable HVDC link. The simulation experiments corresponding to the second study case are presented in Figure 3.6, Figure 3.7, and Figure 3.8.

As shown in Figure 3.6, the active power level provided by the HVDC link starts to be modified at t=20s stabilizing at -500MW in approximately t=60s. The change in the active power direction in the PtP-VSC-HVDC link (i.e. VSC02) influences the PF_{Ctrl} response through the *regulator blocking function* accordingly to the relationship shown in 3.5. This entails that as soon as the active power level goes into the region defined by $P_{deadband}$ (i.e. ±35MW or 5% of HVDC link nominal active power), the reactive power level supplied by VSC02 is kept constant. This behaviour

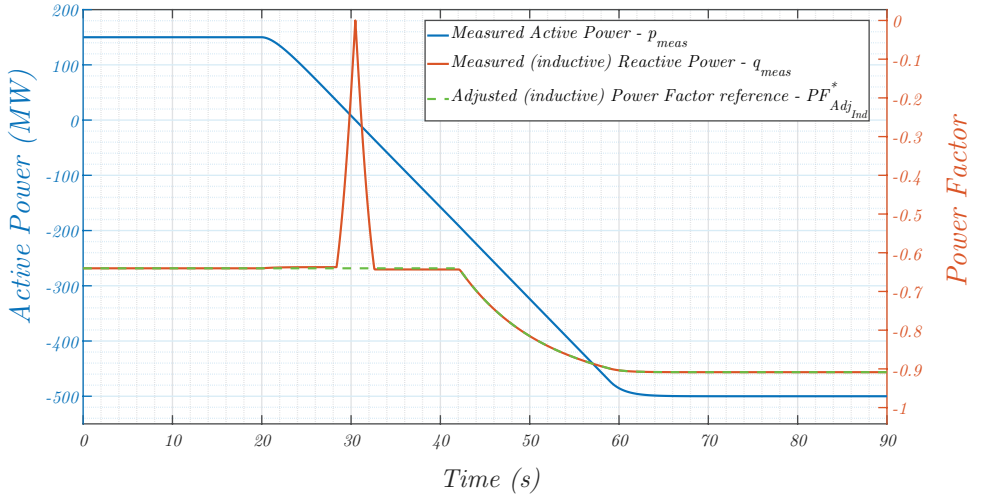

Figure 3.6: Performance of the proposed PF_{Ctrl} in VSC02 (i.e. area B) during an active power reversal event. The PF is kept constant outside the active power range defined by the $P_{deadband}$ (i.e., ±35MW). On the other hand, after t = 42s, the PF level is not kept constant since the reactive power limit (i.e., 230MVAr) shown in Figure 3.7 is not exceeded.

can be verified through Figure 3.7 where the reactive power remains unchanged (while the active power reversal is having place) only within $P_{deadband}$.

The linear behaviour of the reactive power response shown in Figure 3.7 (i.e. RPG) can also be computed based on the relationship presented in 3.6. As the APG has been previously defined (i.e. 999MW/min), the initial conditions associated with the reactive and active power supplied by VSC02 (i.e. Q_0 and P_0) must be known for determining λ (i.e. $\lambda = \frac{Q_0}{P_0}$). Consequently, λ factor represents the reactive and active power ratio that the PF_{Ctrl} must be kept after the PF^* is reached out. Furthermore, in the proposed PF_{Ctrl}, the PF^* is adjusted in order not to exceed the maximum reactive power capabilities (i.e. ±230MVAr) of the VSC unit. The PF^* level adjustment (i.e. $PF^*_{Adj_{Ind}}$) is represented by the green dash lines shown in Figure 3.6 and Figure 3.7, where it can be seen that PF_{meas} and $PF^*_{Adj_{Ind}}$ deviate each other within the active power region defined by $P_{deadband}$ (i.e. ±35MW).

On the other hand, the changes in the active and reactive power presented in Figure 3.6 and Figure 3.7 can also induce changes in the AC voltages magnitude of those buses electrically close to VSC02 unit. Ergo, the magnitude of the closest AC bus voltage to VSC02 unit (i.e. 8a Bus in Figure 3.4) is studied in Figure 3.8, by considering the Q_{Ctrl} and the proposed PF_{Ctrl}, under the same steady-state Q_0 and P_0 power conditions (i.e. 150MW and -180MVAr respectively).

Once the active power reversal event starts, it can be notice in Figure 3.8 that there is a clear difference between the evolution of the AC voltage magnitude when

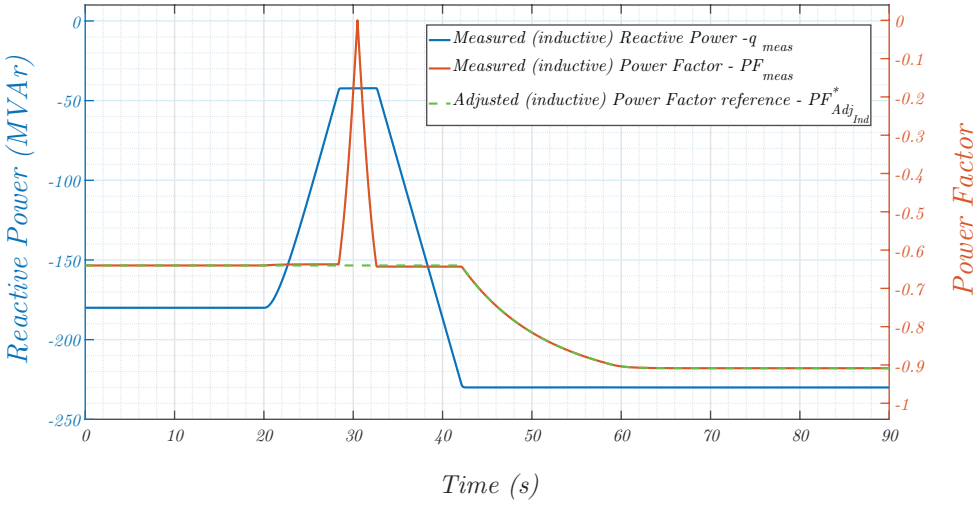

Figure 3.7: Performance of the proposed PF_{Ctrl} in VSC02 (i.e. area B) during an active power reversal event. It can be seen that the level of reactive power starts to be modified as soon as as the active power reversal event shown in Figure 3.6 beings. The modification of teh reactive power level provided by VSC02 is done in order to maintain a constant PF value. Furthermore, it can also be seen that the reactive power is kept constant within the $P_{deadband}$. Finally, the proposed PF_{Ctrl} does not exceed the -230MVAr reactive power limit once it is achieved.

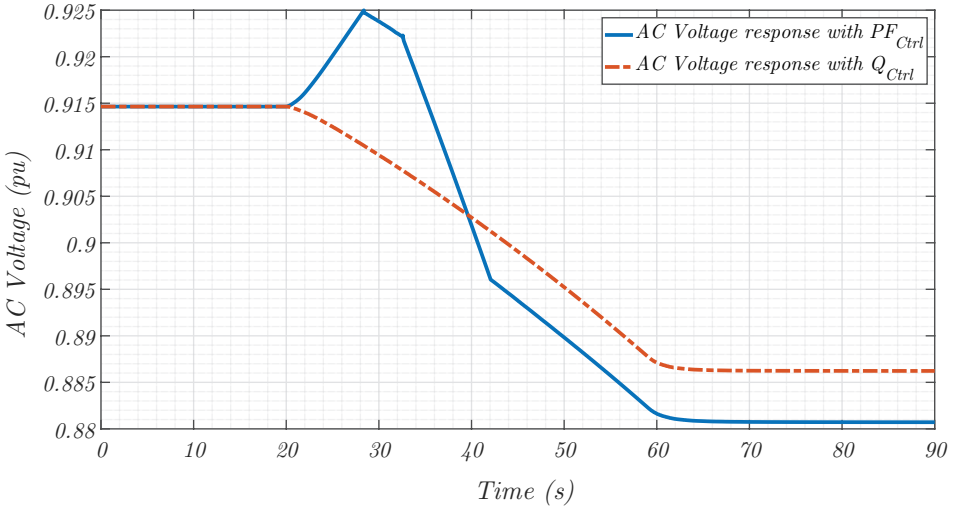

Figure 3.8: Comparison between the quasi-stationary AC voltage response generated by the proposed PF_{Ctrl} (continuous line) and the Q_{Ctrl} (dashed line) during the active power reversal event.

using the Q_{Ctrl} and when using the proposed PF_{Ctrl}. In terms of the Q_{Ctrl}, it is observed that by keeping the Q_0 steady-state condition (i.e. -180MVAr) during the active power reversal, the AC voltage magnitude in 8a Bus experience a contin-

uous reduction of the AC voltage magnitude (dash lines in Figure 3.8). On the other hand, when using the proposed PF_{Ctrl}, the analysis becomes more elaborated since it cannot be directly described as a continuous increment or reduction of the AC voltage magnitude.

Initially, the PF_{Ctrl} starts to decrease the level of (inductive) reactive power in order to maintain a constant level of PF supplied by VSC02 (c.f. Figure 3.7). This reduction in the reactive power level generates a momentary increment of the AC voltage magnitude (from t=20s to approximately t=28s) w.r.t. the response generated by the Q_{Ctrl}. Later (as shown in Figure 3.7), the active power level enters into the $P_{deadband}$ region and then, the reactive power level is kept constant for approximately 4s. During this short time period, the Bus 8a presents a slight reduction in the AC voltage magnitude having a very similar shape when it's compared against the magnitude's evolution generated when using the Q_{Ctrl} as shown in Figure 3.8.

Once the active power level goes out of the $P_{deadband}$ region (i.e. at t≈33s), the PF_{Ctrl} modifies again, the reactive power value supplied in order to keep constant the inductive PF level provided by VSC02 (from t≈33s to t=42s) as shown in Figure 3.7. During such a time period, a 3% reduction of the AC voltage magnitude (w.r.t. the initial steady-state voltage level) is generated by the proposed PF_{Ctrl}as shown in Figure 3.8. This deeper reduction (w.r.t. the one generated by the Q_{Ctrl} mode) indicates that the PF_{Ctrl} is the less attractive option for providing quasi-stationary AC voltage support. However, it is relevant to point out that the evolution of the AC voltage magnitude also depends on the network (short circuit) impedance seen from the bus where the PF is being controlled (i.e. Bus 8a in Figure 3.4). Consequently, a geometrical methodology to analyze in detail the level of quasi-stationary AC voltage support provided by different reactive power control modes (i.e. AC_{Ctrl}, Q_{Ctrl}, and PF_{Ctrl}) under different network impedances conditions, is proposed in chapter 4.

3.3. Frequency control for PtP-VSC-HVDC links

3.3.1. Basic conceptualization and f_{Ctrl} proposal

As indicated in [1], the role of a frequency control (f_{Ctrl}) is to modulate the active power of a VSC-HVDC link depending on the electrical frequencies of the AC networks connected to the link. Additionally, the active power gradient (ramp rate) represents a relevant feature (parameter) for the modulation of the active power, since it allows a fast active power deployment into an AC network during a short time period (e.g. 60GW/min accordingly to [8]). This fast active power deployment has been considered specially relevant for low inertia power systems in which the rate of change of frequency (i.e. RoCoF) is particularly pronounced [9]. For that reason, the development of a f_{Ctrl} needs to examine the influence of the adjustment of the active power gradient (APG) over the frequency response of AC networks considering low inertia levels. In this connection, it is proposed a f_{Ctrl} capable of modifying the set-point of the active power reference (i.e. P^*) and the

APG level utilized by a VSC-HVDC link as illustrated in Figure 3.9.

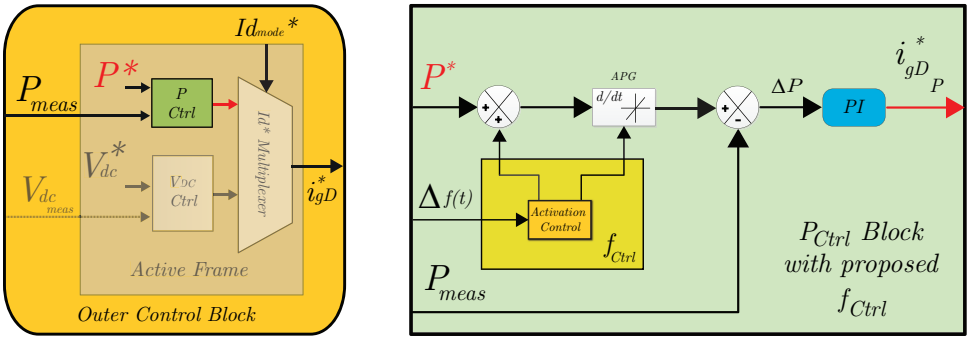

Figure 3.9: Schematic of the supplementary f_{Ctrl} control altering the APG level and the set-point of the active power reference P^* of the P_{Ctrl} presented in Figure 2.11.

In Figure 3.9, it can be seen that the f_{Ctrl} is represented by an activation control (yellow) block which depending on the frequency deviation ($\Delta f(t)$) occurring at the affected AC network, will generate the changes for the active power reference (i.e. P^*) and the APG (rate limiter) level of the VSC-HVDC link. It is worth pointing out that the $\Delta f(t)$ signal is transmitted through a communication based (e.g. fiber optic) system, ensuring in that way the frequency support even to the AC network connected to the rectifier station of the VSC-HVDC link.

Once the $\Delta f(t)$ signal is detected, it goes to a filter differentiator which determines its associated RoCoF in order to identify if the power imbalance generates a $\Delta f(t)$ signal surpassing a defined RoCoF threshold (e.g. ±500mHz/s) and if so, the f_{Ctrl} will modify P^* and the APG level based on a predefined set of values within approximately 500ms time window. The selection of these predefined values depends on specific characteristics such as the inertia levels, generator s' dispatches, and the available generation units providing frequency containment reserve (FCR) services for the AC networks coupled by the VSC-HVDC link. Consequently, a representative case study is utilized to demonstrate the relevance of the selection of these predefined values in a VSC-HVDC link during a power imbalance event in one of the AC networks connected to the link.

3.3.2. Representative case study

The power system illustrated in Figure 3.10 is an adaptation of the benchmark low inertia two-areas (four-machines) power system presented in [10], where the transmission lines (i.e. electromagnetic coupling) between the AC networks have been replaced by a VSC-HVDC link modelled as described in section 2.2.1. Additionally, the synchronous machines have been modelled by using a 6^{th} order generator model and the power flow interchanged between both AC networks is identical to the one described in [10] (i.e. 400MW sent from AC network A to AC network B).

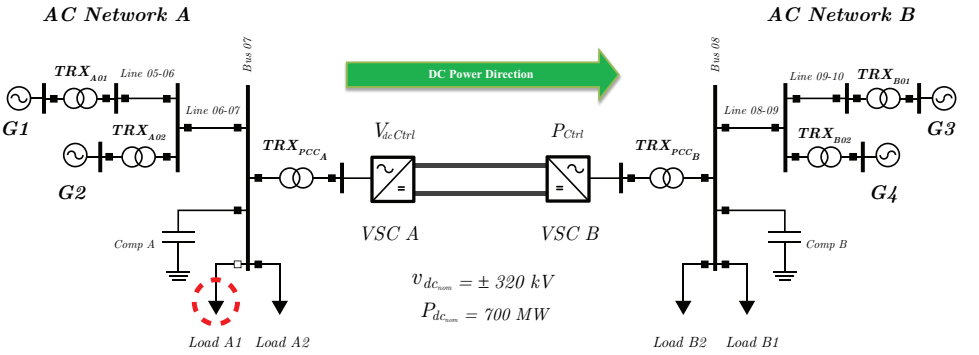

Figure 3.10: Modified benchmark two area power system derived from [10].

In that sense, the frequency support analysis provided by the VSC-HVDC link in Figure 3.10 is carried out by considering a power imbalance generated in AC network A. This power imbalance is produced by a load shedding event occurring at Load A1 in AC network A. This load shedding will generate a 18% power imbalance in AC network A shown in Figure 3.10 which is aligned with the 20% criterion used in [11] to analyze the stability of a power system considering over-frequency conditions. Furthermore, the inertia constant and the associated power flow condition for each of the generators and loads presented in Figure 3.10 are given in Table 3.2. Likewise, the equivalent inertia constant per AC network is computed as described in [12] (e.g. 6,5s for AC Network A and 6,175s for AC network B).

It is interesting to notice that the inertia levels, and the load flow conditions shown in Table 3.2, indicates that the VSC-HVDC link shown in Figure 3.10 could be used as a medium facilitating the participation of the primary frequency resources of AC network B into the frequency deviation occurring at AC network A. This observation can be confirmed as soon as the results associated to the Load A1 shedding are analyzed as presented in section 3.3.3.

3.3.3. Simulations results

Original benchmark two area power system response

The evaluation of the frequency response of the adapted benchmark power system presented in Figure 3.10 was done by first considering the same power imbalance event (i.e. load shedding) in the AC network A, which is created by disconnecting the Load A1 (cf. Figure 3.10) at t = 1s. In the original version of the benchmark system shown in [10], the two AC networks are connected through two parallel AC tie-lines as shown in Figure 3.11. Furthermore, Figure 3.12a and Figure 3.12b present the dynamic response of the generators' rotor speed and the electrical power of all turbines shown in Figure 3.11, respectively.

Figure 3.12a shows that the disconnection of Load A1 entails that the genera-

Table 3.2: VSC units and AC networks data

Power Balance	Network Element	Load Flow Conditions (MW)	Inherent Inertia (s)
Generation on AC Network A	G1	700	6.5
	G2	700	6.5
Demand on AC Network A	Load A1	250	N.A.
	Load A2	717	N.A.
	VSC A	400	N.A.
Generation on AC Network B	G3	719	6.175
	G4	700	6.175
	VSC B	381.6	N.A.
Demand on AC Network B	Load B1	250	N.A.
	Load B2	1517	N.A.

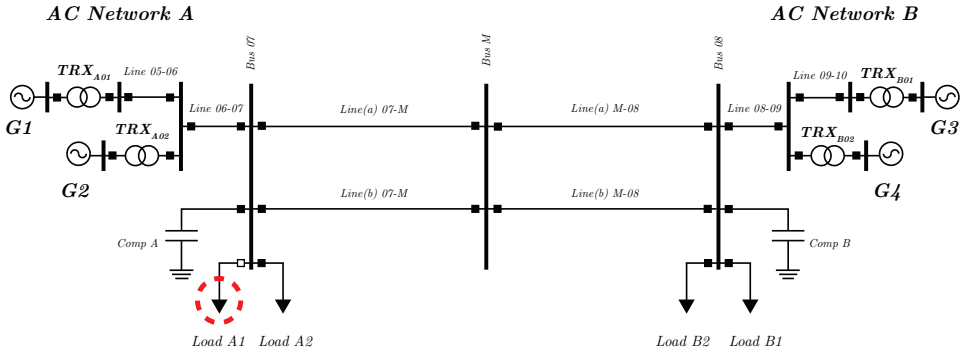

Figure 3.11: Original benchmark two area power system from [10].

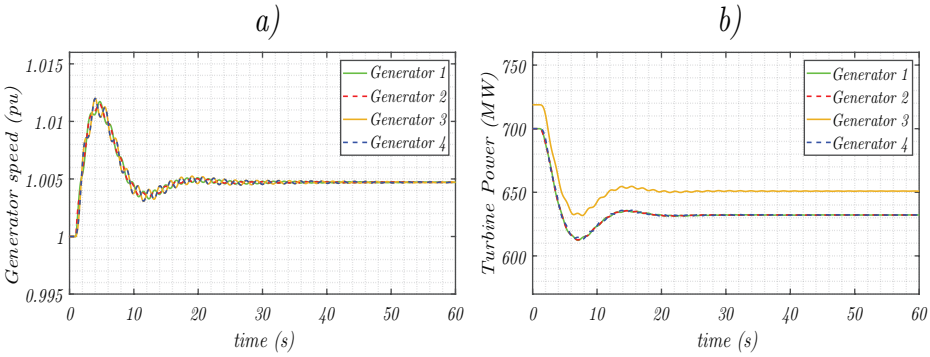

Figure 3.12: Rotational speed (frequency) and turbine power responses of the generator units presented in Figure 3.18.

tor's rotor speed reach a steady-state condition of approximately 1.005 pu. Moreover, Figure 3.12a also shows that the electrical frequency zenith (i.e. peak value

of the generators' rotor speed) is approximately 1.012 pu. Note also in Figure 3.12a that although some inter-area oscillations are observed (as a consequence of the power imbalance occurring at AC network A), all generators kept synchronized which means that their rotational speeds present a practically indistinguishable alignment during the dynamic and steady-state periods after the fault. Furthermore, the inter-area oscillations effects are also observable in the turbines' powers during the dynamic period (i.e. from t = 1 s to t = 30 s) shown in Figure 3.12b.

Adapted benchmark system considering the f_{Ctrl} function

As it was described in section 3.3.1, the activation of the f_{Ctrl} depends on the RoCoF value (obtained from $\Delta f(t)$) which is computed within 500ms from the time of occurrence of the power imbalance. The following criterion is used to enable frequency support by the corresponding VSC station: if the computed RoCoF value of $\Delta f(t)$ (measured by VSC A in Figure 3.10) is higher than a predefined threshold (e.g. 500mHz/s was used in this case study), the active power control shown in Figure 3.9, will increase the ΔP and the APG level to 250MW and 60GW/min respectively. The selection of this APG value (i.e. 60GW/min) has been adopted since it represents a typical adjustment used for VSC-HVDC links during severe (emergency) power imbalance conditions [8]. On the other hand, the 250MW value used for increasing P^* has been selected to show that compensating the load-shedding event with the same level of power imbalance, doesn't necessarily lead to a dynamic response similar to the one obtained in the original benchmark system as shown in Figure 3.13.

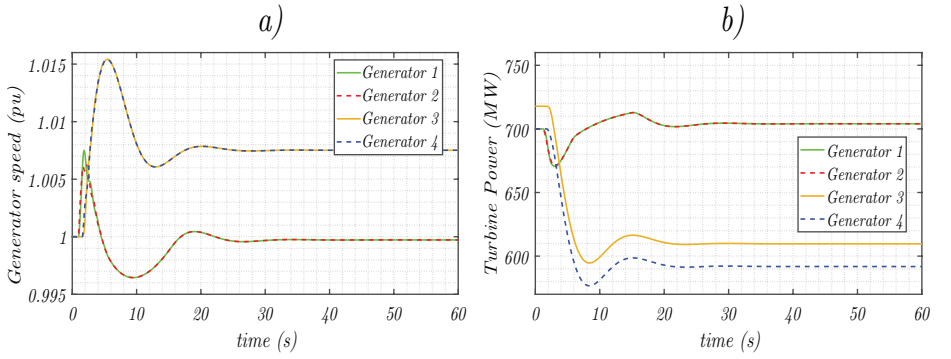

Figure 3.13: Rotational speed (frequency) and turbine power responses of the generator units shown in Figure 3.10 when the APG value of the PtP-VSC-HVDC link is set up to 60GW/min.

It can be seen from Figure 3.13a that by utilizing these APG and ΔP adjustments, the generators' rotor speeds deviations (peak value and steady-state) belonging to the AC network B result comparatively higher than the ones shown in Figure 3.12a. On the other hand, it is also observed in Figure 3.13a that the steady-state frequency response obtained in AC network A has been effectively improved. This implies that the VSC-HVDC link has detected the frequency deviation at AC network A and consequently, has modified the active power supplied to AC network B in

order to generate a fast increment of the load levels in AC network A. Likewise, it can be noticed that due to the electromagnetic decoupling between AC network A and AC network B, the inter-area oscillatory modes present in Figure 3.12a are not observed in Figure 3.13a. Furthermore, it is seen that the steady-state (power) deviation shown in Figure 3.13b for the generators of AC network B (i.e. G3 and G4) results comparatively bigger, when it is compared against the one shown for AC network A in Figure 3.13b (i.e. G1 and G2). The difference between these steady-state deviations also indicates that the VSC-HVDC link has facilitated the participation of the primary frequency resources of AC network B into the frequency deviation occurring at AC network A. In other words, from the point of view of the AC network A, the VSC-HVDC link has effectively contributed to support its frequency stability. Conversely, the VSC-HVDC link has abruptly modified the power flow conditions in AC network B, creating in that way a response of its primary frequency reserves, that is to say, a change in the synchronous machines' active power levels.

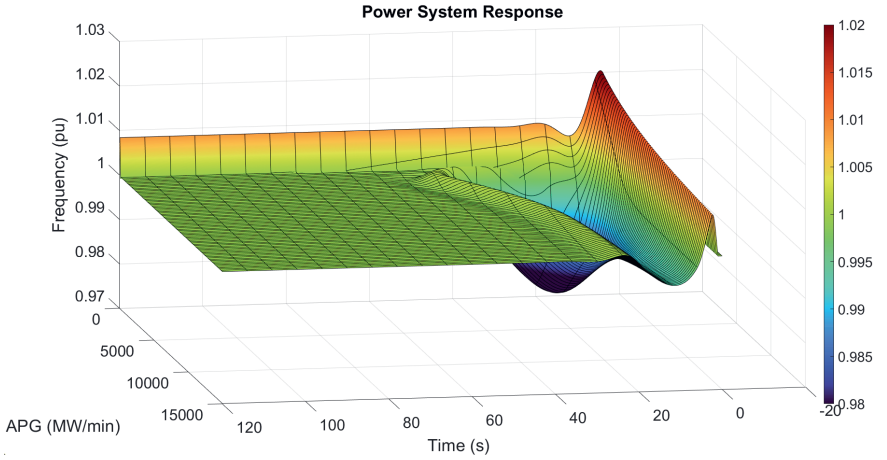

Figure 3.14: Frequency response of the affected power system (i.e. AC network A in Figure 3.10) considering a progressive increment of the APG level in the proposed f_{Ctrl} for the PtP-VSC-HVDC link.

The simulation experiment carried out in Figure 3.13, essentially demonstrate that a reduction of the steady-state frequency deviation and the zenith levels generated by a load shedding in AC network A is generated by the f_{Ctrl} when the same active power imbalance and the maximum (emergency) APG value are utilized. However, it is possible to examine in more detail, the corresponding evolution of the frequency and generator's power responses in AC network A, based on the progressive increment of the APG level for f_{Ctrl} as shown in Figure 3.15.

The progressive increment of the APG level shown in Figure 3.15 indicates that when higher (i.e. higher than 600000 MW/min) APG values are used in the test system, there is a substantial reduction of the zenith levels against the ones observed when there is not modification in the active power transmitted by the VSC-HVDC

link (i.e. APG = 0). On the other hand, it is interesting to notice that frequency drop events are observed in AC network A, if the APG is setup to utilize values lower than 10000 MW/min.

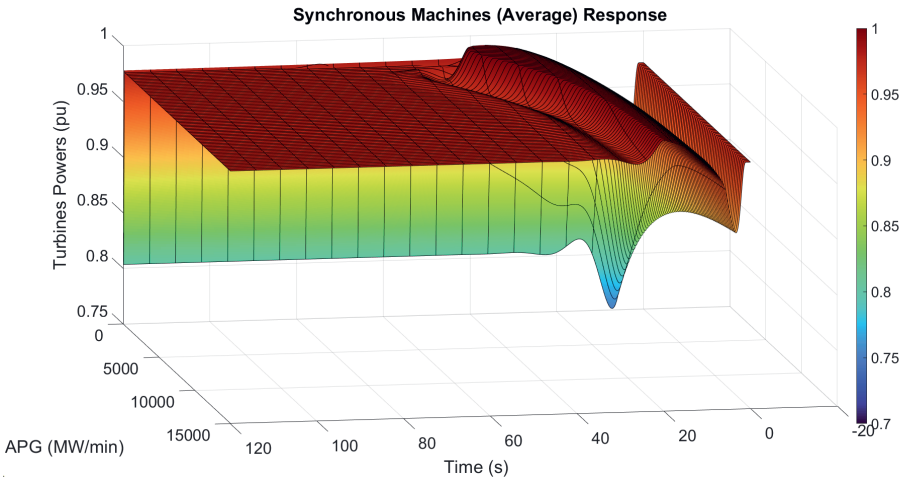

Figure 3.15: Turbines powers response of the synchronous machines within the affected power system (i.e. AC network A in Figure 3.10) considering a progressive increment of the APG level in the proposed f_{Ctrl} for the PtP-VSC-HVDC link.

These frequency drop events are a consequence of the interplay occurring between the control actions developed by the generators' governor systems and the electrical power change generated by the APG. Here, it is relevant to remember that the generators' governor systems support the frequency stability in a power system, based on a proportional control action known as the speed (or frequency) droop. This proportional action is not meant to restore the frequency to the nominal level, but instead to provide the necessary primary frequency response during a severe power imbalance to contain the frequency excursion. Furthermore, Figure 3.15a shows that initially the APG gives the possibility of restoring the nominal level of the electrical frequency in AC network A but later, the increment of the APG is not aligned with the active power recovery function developed by the generators' governor systems as shown in Figure 3.15b. In other words, the balance between management of the mechanical (i.e. governor system's action) and the electrical power (i.e. driven by the APG) expressed within each generators' swing equation, becomes adversely affected. This adverse effect creates a negative accelerating power leading to a pronounced frequency drop (almost 2% of deviation) when the APG level is below 5000 MW/min as shown in Figure 3.15a.

The obtained results for this case study indicates that the criterion utilized for selecting the predefined values for the APG level and ΔP (to develop the frequency support) generates an unequal participation of the primary frequency resources between the AC networks shown in Figure 3.10. Consequently, a more elaborated

criterion allowing a balanced deployment of the primary frequency resources of both AC networks will be presented in Chapter 7.

3.4. FRT and Post-Fault Active Power Recovery

In the European HVDC grid code [1] the fault ride through (FRT) capability is described as *the ability of a VSC-HVDC link for staying connected (during fault conditions) to the affected AC network and continuing stable operation after the power system has recovered following the fault clearance*. In this connection, the short circuit contribution during fault conditions, the prioritization of the active power vs the reactive power during fault conditions, and the post-fault active power recovery, represents associated aspects that are demanded in [1] as part of the FRT capability.

The connection between these aspects (requirements) and the FRT capability can be better understood as soon as the AC current (supplied to the faulted AC network) by the VSC-HVDC unit (i.e. i_{VSC}) is presented as a function of the reactive and active currents (i.e. i_{gQ} and i_{gD}) as shown in 3.7.

$$i_{VSC}^2 = i_{gQ}^2 + i_{gD}^2 \tag{3.7}$$

The short circuit level of a VSC-HVDC unit represents the amount of current provided to an AC network during a fault event, and as indicated in 3.7 this amount depends on its active i_{gD} and reactive i_{gQ} currents levels. As discussed in section 2.2.2, the current references for $i^*_{gD_{Outer}}$ and $i^*_{gQ_{Outer}}$ (c.f 2.14 and 2.15) are generated by different control modes (within the *Outer Control Block*) which define the active and the reactive power supplied by a VSC-HVDC unit during steady-state (normal) operation conditions. On the other hand, the generation of the i_{gD} and i_{gQ} current references during fault conditions needs to be created based on the physical constrains of the affected VSC-HVDC unit and its feasibility of boosting the magnitude of the dropped AC voltage.

3.4.1. FRT criterion based on a polynomial reference

Description

The criterion for the short circuit level provided by a VSC-HVDC unit (or a modern wind farm) during an AC fault event is typically given as a reactive current injection that has to be introduced into the faulted AC network [13]. This reactive current injection depends on the voltage drop experienced at the point of common coupling (i.e. V_{PCC} bus) as described in [14] and presented in Figure 3.16. Moreover, the modification of the reactive current injected during an AC voltage drop (fault event), also leads to a modification in terms of the reactive power supplied by the VSC-HVDC unit as indicated by the expression 2.13. This reactive power modification starts to takes place if the AC voltage at the V_{PCC} bus drops below 85% of its nominal value as shown in Figure 3.16. In other words, the 85% limit represents the condition in which the reactive power supplied by the VSC-HVDC unit starts to become more relevant than the active power transmission provided by the VSC-HVDC link (i.e. prioritizing i_{gQ} over i_{gD} for providing AC voltage support). Ad-

ditionally, this 85% limit is established to avoid a modification of the active power transmitted by the VSC-HVDC link during normal operating conditions.

More precisely, Figure 3.16 indicates that a linear increment of the i_{gQ} current is expected in the VSC-HVDC unit when an AC voltage drop in V_{PCC} (between 50% and 85% w.r.t. nominal voltage network value) occurs. On the other hand, the reactive current injected will be equal to the nominal AC converter current (i.e. I_n) when the drop in V_{PCC} goes beyond 50%. This implies that the level of AC voltage drops in the V_{PCC} bus defines the level of prioritization of the active and reactive power supplied by the VSC-HVDC unit.

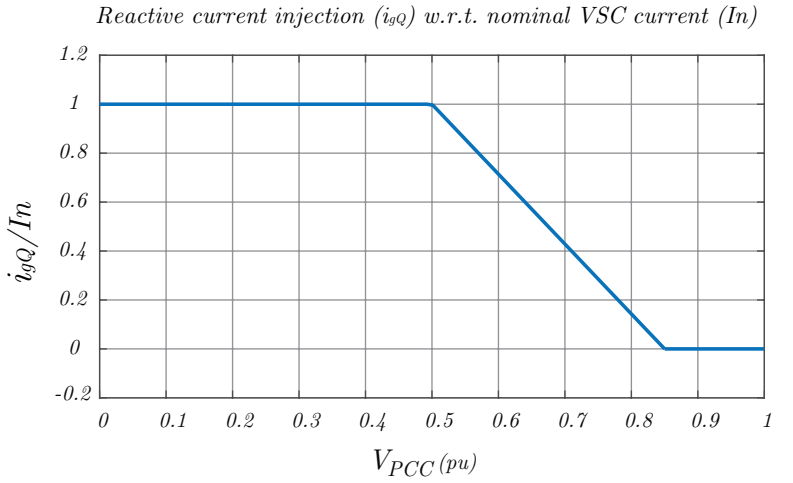

Figure 3.16: Reactive current injection profile of VSC units under balance AC fault conditions [14].

The reactive current injection indicated in Figure 3.16 represents a challenge in terms of the i_{gQ} regulation since it must continuously examine the V_{PCC} level for adapting the reference of i_{gQ} (i.e. i^*_{gQ}) based on a piecewise graphical description. Consequently, it is proposed to utilize a non-linear function capable of generating the i^*_{gQ} value based on the piecewise graphical description shown in Figure 3.16. The non-linear function generates the i^*_{gQ} value depending on the V_{PCC} level and the parameter α_{FRT} as indicated in the expression 3.8.

$$i^*_{gQ_{Fault}} = \frac{12}{7} - \frac{\sqrt{5}\sqrt{20V_{PCC}^2 - 20V_{PCC} + 28\alpha_{FRT} + 5}}{7} - \frac{10V_{PCC}}{7} \tag{3.8}$$

The continuous function indicated by the expression 3.8 is obtained by noticing that the piecewise nature of the reactive current injection profile shown in Figure 3.16 can be avoided when adding two mathematical functions. These two functions are described by the expressions 3.9 and 3.10.

$$V_{PCC} = \frac{1}{20}(17 - 7(i_{gQ}/I_n)) \tag{3.9}$$

$$V_{PCC} = -\frac{\alpha_{FRT}}{(1 - (i_{gQ}/I_n))} \tag{3.10}$$

The expression 3.9 represents the expected linear increment in the reactive current injection when the voltage drop in V_{PCC} value is within 0.5pu and 0.85pu range shown in Figure 3.16. On the other hand, expression 3.10 represents an asymptotic function that converges to negative infinite when the i_{gQ}/I_n value is close to one. This convergence does not imply a concern for the control reference since the minimum physically possible value for the magnitude of the V_{PCC} voltage is zero. Moreover, the expression 3.10 does also have the parameter α_{FRT} which essentially is a proposed mitigation factor used to nullify the value of the asymptotic function when the voltage drop in V_{PCC} value is within 0.5pu and 0.85pu range. This nullification can be obtained if α_{FRT} is set to be nearly zero (e.g. α_{FRT} = 0.0001) Thus, the expression 3.8 is the inverse function of the addition of two mathematical functions presented in 3.9 and 3.10.

The expression 3.8 is utilized to directly provide the reference of i_{gQ}^* as soon as the V_{PCC} drops below 85%, which is the starting point indicated in Figure 3.16 for developing the modification of i_{gQ}. Thus, the implementation for providing the i_{gQ}^* based on a piecewise function can be simplified by utilizing the single non-linear function (as shown in Figure 3.17) where the parameter α_{FRT} is used to define the curvature level in 3.8 between the linear increment and the fixed i_{gQ} level to be provided by the VSC-HVDC unit under low AC voltage conditions at V_{PCC}.

Implementation

The reactive current injection utilizing the polynomial reference presented in 3.8 is implemented as part of a (FRT) control block added between the *Outer Control Block* and the *Inner Control Block* as shown in Figure 3.18. This FRT control block acts as a selector which defines the currents references i_{gD}^* and i_{gQ}^* (used by the *Inner Control Block*) depending on the AC voltage drop at the V_{PCC} bus as shown in Figure 3.18.

As indicated in Figure 3.17, once the V_{PCC} voltage drops below 85%, the FRT control block shown in Figure 3.18 will get activated. Consequently, the output signal i_{gQ}^* in Figure 3.18b will be equal to $i_{gQ_{Fault}}^*$. On the other hand, when the FRT control block gets deactivated the output signal i_{gQ}^* will be equal to the reactive current reference signal provided by the *Outer Control Block* (i.e. $i_{gQ_{Outer}}^*$). The reactive current injection supplied by VSC-HVDC unit the during a fault event in the AC network must be carried out by considering its physical (current) limits.

For this reason, the reactive current injected will potentially induce a reduction of the active current i_{gD} in order to keep i_{VSC} within the AC current limits of the VSC-HVDC unit. The relationship between the reference of the active current (i.e.

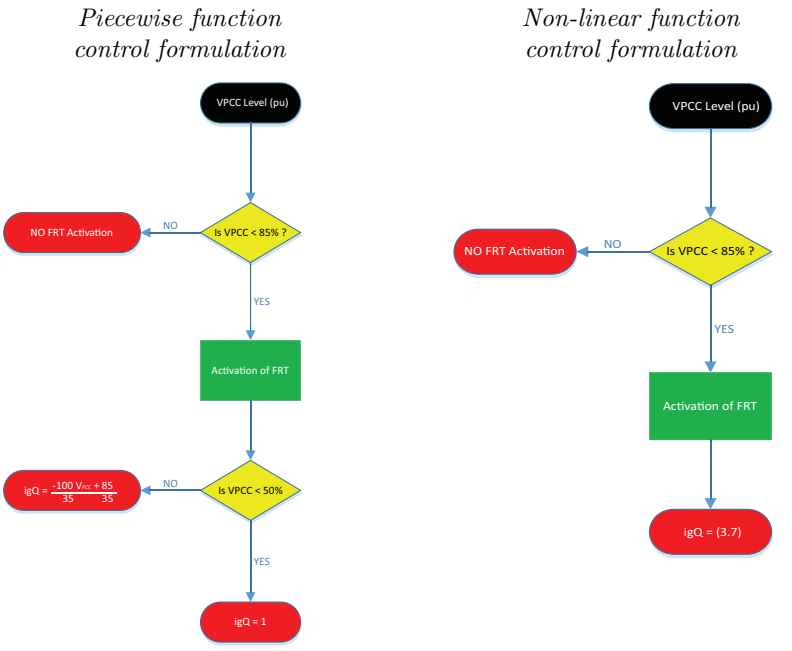

Figure 3.17: Flowchart comparison of the piecewise function, and the proposed non-linear (polynomial) control formulation.

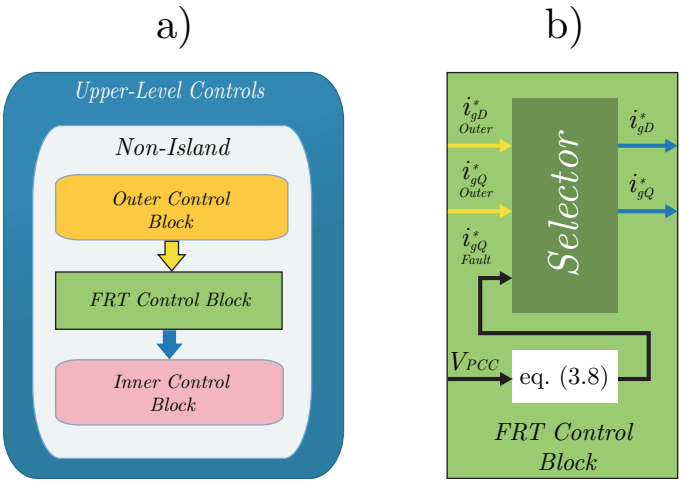

Figure 3.18: a) Hierarchy between the *Outer Control Block*, the *FRT Control Block* and the *Inner Control Block* based on Figure 2.9. b) The *FRT Control Block* is only activated in the VSC unit that detects the voltage drop at its AC side network bus.

i^*_{gD}) and the reactive current injected during a fault event (i.e. $i^*_{gQ_{Fault}}$) is defined as presented in [15], and illustrated by the limiter block shown in Figure 3.19. At

this point, it can be seen that as the amount of reactive current injected $i^*_{gQ_{Fault}}$ depends on the level of voltage drop experienced by V_{PCC} (c.f. expression 3.8), then the amount of active current is also implicitly affected by the voltage drop in V_{PCC}.

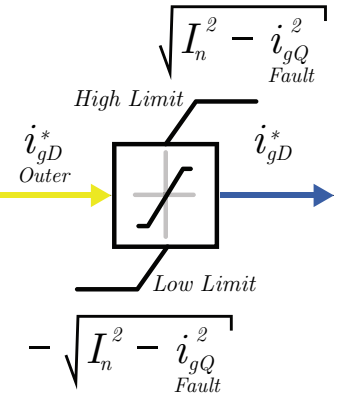

Figure 3.19: Limiter block defining the i^*_{gD} output signal for the *Inner Control Block* during a voltage drop in V_{PCC} based on the relationship shown in [15]

3.4.2. Enhancement of the Active Power Controller for Post-Fault Active Power Recovery Compliance

Another point for attention regarding the $i^*_{gD_{Outer}}$ management is the tendency of the active power's PI regulator to increase the $i^*_{gD_{Outer}}$ value during the AC fault period. The increment in $i^*_{gD_{Outer}}$ shown in Figure 3.19 is generated due to the accumulative error created by the integral term of the PI regulator which is also know as the windup effect. This PI regulator's windup effect occurs since the drop in V_{PCC} negatively affects the level of active power supplied by the VSC-HVDC unit, creating in that way a prolonged active power error, which induce an continuous increment of the integral block's output. For that reason, an Anti-Windup strategy has been designed, and it is presented as shown in Figure 3.20.

As shown in Figure 3.20, the active power error signal ΔP represents the input signal for the integral and the proportional blocks (highlighted in yellow) of the active power controller. The corresponding output signal of the entire block is the $i^*_{gD_P}$ and represents one of the input signals of the *Inner Control* block shown in Figure 2.10. As soon as the FRT function is enabled it activates a nor gate that nullifies the ΔP (input) signal for the integral (yellow) block, and a second PI controller is activated and incorporated into the anti-windup control loops as shown in Figure 3.20. Unlike other methods for anti-windup control, in which the limits for saturation blocks need to be established [16], the use of the proposed second PI controller excludes the need for such saturation blocks, simplifying the criterion for regulating the state-variable value of the integrator block. This second PI controller

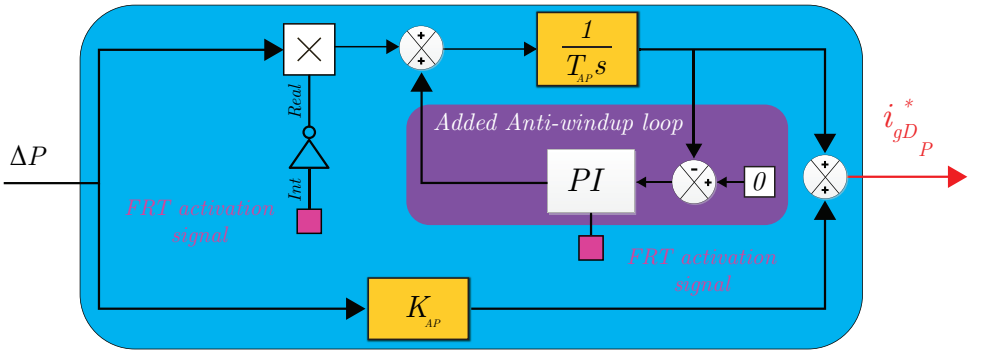

Figure 3.20: The highlighted purple section showing the added anti-windup dependent FRT control loop. The added loop consists of a PI controller regulating the state variable value of the integrator within the P_{Ctrl} block (c.f. Figure 2.11), during the AC fault period. The highlighted blue section corresponds to the one illustrated in Figure 3.9.

essentially nullifies the output signal of the integral term which means that during the fault period, the $i^*_{gD_{Outer}}$ is exclusively defined by the K_{AP} output, and this feature will allow establishing certain active power transmission by the VSC-HVDC unit during high impedance faults. Furthermore, as soon as the FRT function is disabled, the ΔP signal is reestablished as input for the integral term, and simultaneously the second PI controller is reset and excluded from the control loop as shown in Figure 3.20. Here, it is recommended to perform the adjustment of the second PI controller by considering a settling time equal to 20 ms, and considering the pole location method for second-order systems presented in [16]. This settling time is recommended in order to accelerate the integration action of the active power's PI controller after the end of the post-fault period, generating in that way a faster restoration process of the pre-fault active power set point in the inverter station of the PtP-VSC-HVDC link.

Simulation results

The performance of the FRT block is assessed by considering a PtP-VSC-HVDC link connecting two synchronous areas in which three fault scenarios are studied. In all the studied scenarios, a 100 ms high impedance three phase balanced fault occur at the V_{PCC} bus of the inverter unit while 680 MW are transmitted to the affected AC network. The difference between these faulted scenarios lies on the amount of residual voltage established during the fault period which is observed as shown in Figure 3.21a.

The residual voltages shown in Figure 3.21 appear after the fault inception occurring at t=1 s, and they lead to a modification of the reactive and active current as shown in Figure 3.21c and Figure 3.21d respectively. It can be seen that the lowest V_{PCC} voltage drops (first scenario) generates the maximum and the minimum amount of i_{gQ} and i_{gD} values injected by the VSC-HVDC unit respectively. Furthermore, as the active current goes to zero during the 40% drop in V_{PCC}, the

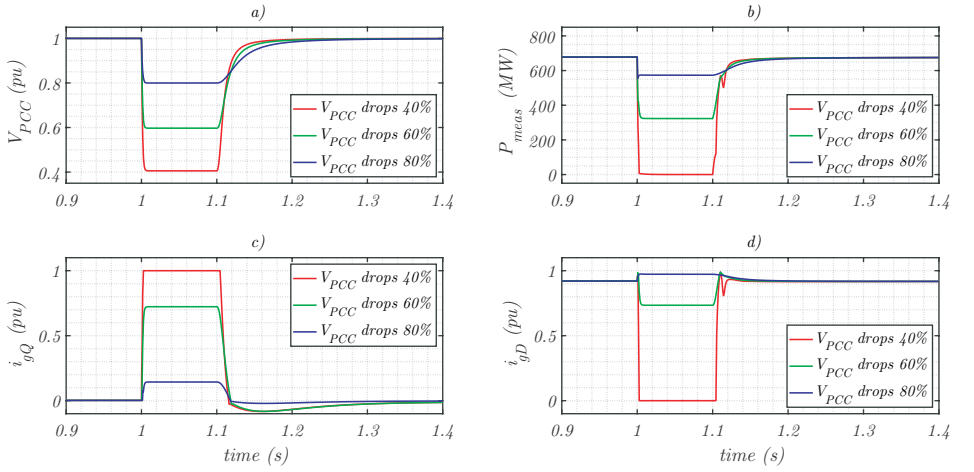

Figure 3.21: Active power response of an inverter VSC-HVDC unit using the proposed anti-windup loop experiencing different levels of AC voltage drops. Figure 3.21a showing different AC voltage drops caused by the high impedance AC network faults. Figure 3.21b presenting the active power of the FRT activated VSC-HVDC unit. Figure 3.21c showing the reactive current injected by the FRT activated VSC-HVDC unit (c.f. expression 3.8). Figure 3.21d showing the active current injected into the AC network based on the limiter block shown in Figure 3.19.

active power supplied by the VSC-HVDC unit is also nullified as shown in Figure 3.21b. On the other hand, in the second scenario (i.e. 60% drop in V_{PCC}), the amount of i_{gQ} injected during the fault period is comparatively lower than in the first scenario. This allows to induce a less pronounce reduction in i_{gD} in Figure 3.21d which results in an active power supplying of approximately 320 MW during the fault period as presented in Figure 3.21b. Lastly, the third scenario (i.e. 80% drop in V_{PCC}), leads to the lowest reactive current i_{gQ} injection as shown in Figure 3.21c and slight increment of the active current i_{gD} supplied by the VSC-HVDC unit during the fault period. This increment in i_{gD} occurs since the $i^*_{gD_{Outer}}$ attempts to maintain the active power supplied by the VSC-HVDC unit within the boundaries established by the limiter block shown in Figure 3.19. In other words, during the fault period of the third scenario, the injected reactive current i_{gQ} is not imposing a restriction as severe as for the first and the second scenarios in the limiter block shown in Figure 3.19. Consequently, the values of the limits of the limiter block for the third scenario allow more active participation of the regulation function of $i^*_{gD_{Outer}}$ which helps to maintain the active power level during the fault condition closer to its pre-fault condition in comparison with the other two scenarios. 6.3.3

3.4.3. Dynamically Adjustable Fault Impedance for PFAPR

The post-fault active power recovery mentioned in [1], is a requirement defining the conditions in which the active power supplied by a VSC-HVDC unit should be restored to the affected AC network when an AC fault is cleared. In terms of a RMS simulation framework (this thesis), the evolution of the variables under a post-fault

condition (e.g. DC voltage, and AC currents) is obtained based on the numerical interaction between algebraic equations (usually AC network) and differential equations (usually DC network) as shown in Figure 3.22. It is worth mentioning that, in order to establish that the RMS model is adequate to perform a post-fault type of analysis, a comparison process against a more detailed electromagnetic transient (EMT) model of the transmission AC network needs to be carried out.

The description of the characteristics of an RMS simulation for the analysis of a post-fault active power recovery (PFAPR) process can be simplified when the AC network representation is reduced to an infinite bus system as shown in Figure 3.22. In a classical RMS simulation framework, a three-phase fault affecting the V_{PCC} bus can be expressed by the addition of a fault impedance, which will instantaneously generate a change in the V_{PCC} profile due to the algebraic system of equations used to compute the variables of the transmission AC network. This instantaneous change in the V_{PCC} profile will also influence the AC/DC power balance of the VSC-HVDC link abruptly affecting the performance of the controllers managing the PFAPR process in a RMS simulation framework.

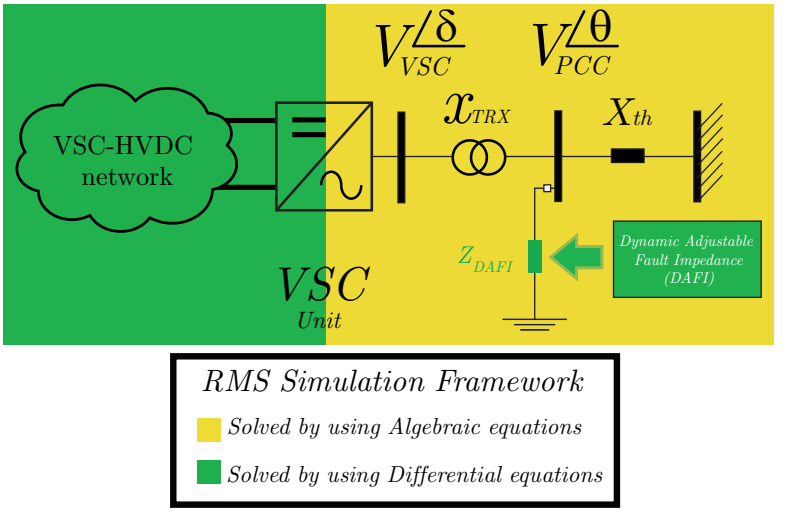

Figure 3.22: The RMS simulation framework shows the elements utilizing differential (green) and algebraic (yellow) equations. 8.3.4

Consequently, it is proposed an independent control system capable of performing a dynamic adjustment of the fault impedance (Z_{DAFI}) magnitude's value based on a first-order dynamic response defined by the time constant T_{DACI} and the input u_{IPFC} (which Initiates the Post-Fault Condition) as defined by 3.11.

$$\frac{dZ_{DAFI}(t)}{dt} = -\frac{Z_{DAFI}(t)}{T_{DAFI}} + Z_{value}\frac{u_{IPFC}(t)}{T_{DAFI}} \tag{3.11}$$

From Figure 3.22, it can be inferred that the Z_{DAFI} is essentially a shunt impedance

that is connected to the corresponding V_{PCC} busbar through an AC circuit breaker which is opened during normal operating conditions. The AC fault event is then generated by closing the AC breaker and the corresponding impedance values of the Z_{DAFI} are described in Figure 3.23.

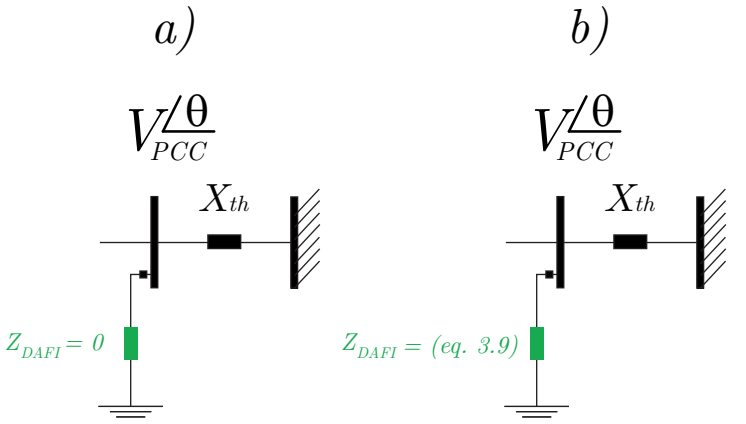

Figure 3.23: Response of the dynamically adjustable fault impedance (green) during a) the fault period, and b) the post-fault period.

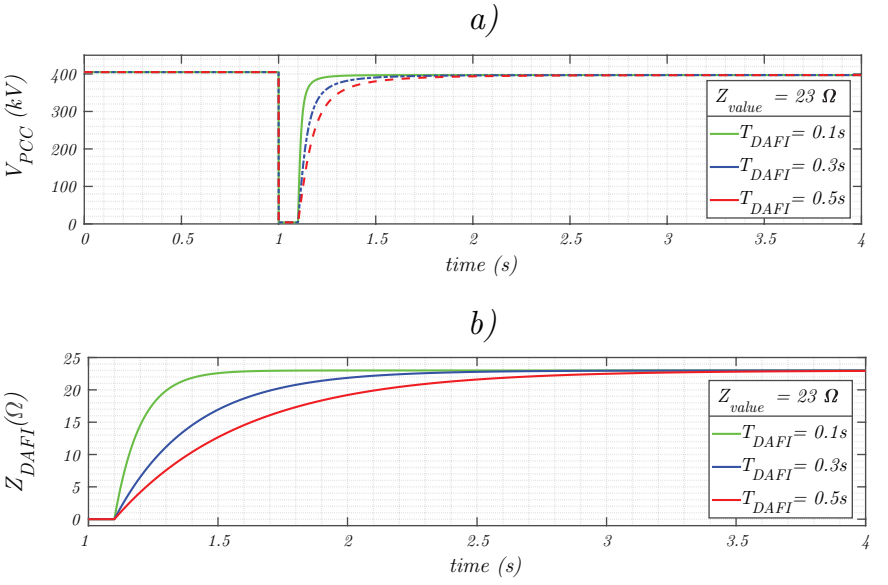

Figure 3.24: a) Evolution of the AC voltage profile considering different T_{DAFI} values. b) Evolution of the dynamic adjustable fault impedance Z_{DAFI} considering several T_{DAFI} values.

The inclusion of a differential equation defining the value of Z_{DAFI} will influence

the evolution of V_{PCC}'s profile since the control system indirectly defines the fault current flowing through Z_{DAFI} only during the post-fault period by progressively increasing the Z_{DAFI} magnitude's value. Furthermore, the criterion for determining the associated value of Z_{value} (c.f. 3.11) needs to be defined for establishing a minimum post-fault current which is intended to progressively be reduced until the complete clearance of Z_{DAFI}. Moreover, the first-order dynamic system is considered since it is assumed that the evolution of V_{PCC} during a post-fault condition is mainly driven by the inductive characteristics of the transmission AC network represented by X_{th} in Figure 3.22. Ergo, the adjustment of the magnitude's value Z_{DAFI} is developed under the assumption that the impedance Z_{DAFI} shown Figure 3.23 in is purely inductive.

Figure 3.24 shows that the selection of the time constant T_{DAFI} (defined by the expression 3.11) affects the post-fault profile of V_{PCC}. As an example, in Figure 3.24a a 100ms three-phase fault to ground occurring at t = 1s is developed by means of the fault impedance Z_{DAFI} shown in Figure 3.23. It can be seen in Figure 3.24b that the time constant value T_{DAFI} shown in 3.11 defines the time response of the Z_{DAFI} and consequently, it does influence the V_{PCC} profile during the post fault period (i.e. t > 1.1 s). On the other hand, the selection of the Z_{value} (in this case Z_{value} = 23 Ω) determines the desired level of post-fault current flowing through Z_{DAFI} depending on the network impedance value as shown in Figure 3.23.

3.5. Conclusions

The fundamental challenges associated with the regulation of power factor by a VSC-HVDC link were discussed and solved through the design of a power factor controller PF_{Ctrl}. The proposed PF_{Ctrl} demonstrated its superior regulation capabilities in terms of rising and settling times responses when compared against other available power factor regulation systems. Moreover, for the first time, the challenges associated with the power factor regulation during active power reversal events in VSC-HVDC links were solved by proposing an adjustable PF_{Ctrl} operational range defined by an active power deadband (i.e. $Pdeadband$). On the other hand, it was observed that when comparing the voltage support provided by the proposed PF_{Ctrl} versus the voltage support provided by a reactive power control Q_{Ctrl} certain level of voltage boosting was obtained for a short period of time during an active power reversal event. Furthermore, a lower performance of the PF_{Ctrl} with respect to the Q_{Ctrl} was observed when an inductive power factor is used during an active power reversal event. These findings suggest that a more elaborated methodology needs to be developed to determine the conditions in which the power factor regulation provides superior performance (in terms of voltage support) when compared against other reactive power control modes.

The development of a fault ride-through (FRT) control strategy regulating the reactive current injection during voltage drop conditions in the AC network was carried out by proposing a polynomial reference-based approach. The polynomial reference was proposed based on an AC voltage-reactive current profile which helps to establish the level of active and reactive current prioritization that a VSC-HVDC unit needs to establish during a voltage dip in an AC network. On the other hand, a modification of the active power's PI regulator was carried out in order to maintain affected as less as possible the supply of active power, and to avoid the generation of windup effects (i.e. anti-windup control) in the active power's PI regulator during voltage drops on the AC network. Furthermore, the obtained results indicated that the injected reactive current complies with the requirements associated with the expected levels of reactive current to be introduced as a function of the level of AC voltage drop in the AC network.

Additionally, the results regarding the supplying of active power during a fault event indicated that a direct relationship between the AC voltage drop and the active power reduction is established by the proposed anti-windup control, that is to say, a slight drop in the AC voltage will induce a slight reduction in the active power provided by the VSC-HVDC unit. The direct relationship between the level of AC voltage drop and the level of active power reduction represents a relevant feature contributing to the support of the AC/DC power balance during high impedance faults (slight voltage drop levels) events in the AC network. Moreover, a dynamic adjustable fault impedance (i.e. DAFI) was proposed as an additional concept to improve the voltage recovery representation (in a RMS simulation environment) of the post-fault conditions in an AC network. The improved representation of the AC voltage profile during a post-fault condition is also a convenient characteristic that

enhances the description of the active power recovery profile and consequently the AC/DC power balance response in the VSC-HVDC unit.

Last but not least, a frequency support control strategy for low inertia AC networks connected through a point-to-point VSC-HVDC link was proposed, considering a predefined adjustment of its active power reference and its active power gradient value (i.e. a predefined ramp-rate setting). The obtained frequency results demonstrated that by using the proposed control strategy, a frequency disturbance caused by a power imbalance event in one of the AC networks connected by the VSC-HVDC link, can be mitigated in terms of the zenith values and the steady-state frequency level obtained after the disturbance. This demonstrates that by utilizing the control strategy proposed, the VSC-HVDC link can certainly serve as a medium for enabling the participation of the primary frequency resources of a non-disturbed AC network when a power unbalance event affects the frequency profile of the other AC network connected by the VSC-HVDC.

References

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4

Directional Derivative-Based Method for Quasi-Stationary Voltage Support Analysis of Single-Infeed VSC-HVDC units

In this chapter an analytical method based on the directional derivative concept is developed to quantify the sensitivities of an AC bus voltage with respect to the reactive power control modes of a VSC unit. It is shown that the developed method applies to VSC units that are part of VSC-HVDC links, which can operate in a point-to-point or multi-terminal configuration. Time-domain simulations are performed to verify the findings from the application of the analytical method on a reduced size power system.

The results presented in this chapter have been published in:

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4.1. Generic AC/DC system representation

The analysis of the quasi-stationary AC voltage support, generated by each of the reactive power control (RPC) modes in a VSC unit, is developed by considering the system configuration presented in Figure 4.1.

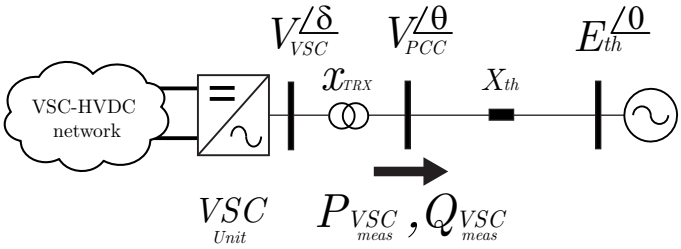


Figure 4.1: Single-infeed VSC-HVDC system model.

In Figure 4.1, the system configuration shows a reduced HVAC network represented by an ideal AC voltage source, the E_{th} and V_{PCC} buses, and the pure inductive transmission line X_{th}. Furthermore, a VSC-HVDC network representation is also shown as part of the system configuration in Figure 4.1, where a VSC unit, the X_{TRX} transformer, and the V_{VSC} bus constitute the elements linking the HVDC and HVAC networks. The VSC-HVDC network represents a generalization which can represent either a meshed HVDC grid (multi-terminal VSC system) or a simple HVDC grid (point-to-point VSC system). Please also notice that, the VSC unit regulates the active power P_{VSC} and reactive power Q_{VSC} at the point of common coupling (i.e. V_{PCC} bus). Additionally, it is assumed that the VSC unit is based on modular multi-level technology, which means that a filter representation (for harmonic compensation) is not required as mentioned in [1].

4.2. Analytical formulation for quasi-stationary AC voltage support

4.2.1. Steady-state power and voltage equations

The mathematical descriptions of the RPCs and the power system are formulated here, to highlight the interplay between the regulation of the RPC's modes with the quasi-stationary voltage analysis. First of all, the steady-state equations for the power system shown in Figure 4.1 are presented in 4.1 and 4.2.

$$P_{VSC} = \frac{|V_{PCC}||E_{th}|sin(\theta)}{X_{th}} \tag{4.1}$$

$$Q_{VSC} = \frac{|V_{PCC}|^2}{X_{th}} - \frac{|V_{PCC}||E_{th}|cos(\theta)}{X_{th}} \tag{4.2}$$

If the power system variables X_{th} and E_{th} are assumed to be constant, then, it is possible to describe the V_{PCC} voltage in terms of P_{VSC} and Q_{VSC} as shown in 4.3.

$$V_{PCC}(P_{VSC}, Q_{VSC}) = \sqrt{\frac{|E_{th}|^2}{2} + X_{th}Q_{VSC} + \sqrt{\frac{|E_{th}|^4}{4} + |E_{th}|^2 X_{th}Q_{VSC} - X_{th}^2 P_{VSC}^2}} \tag{4.3}$$

It is clear then, that the V_{PCC} profile will be influenced by the control schemes used to modulate the active and reactive power produced by the VSC unit. Furthermore, these power modulations can be appreciated as the corresponding paths generated by the control modes within the PQ capability diagram (limits) of the VSC unit, as shown in Figure 4.2.

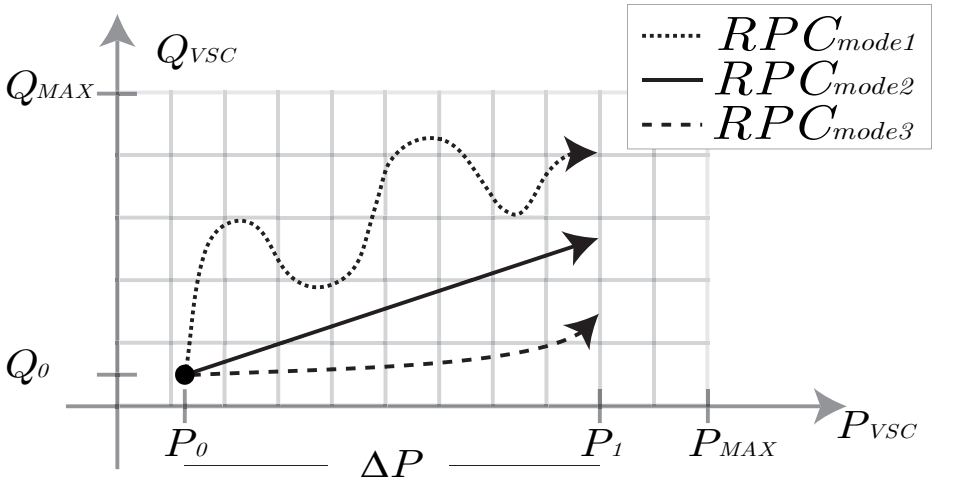


Figure 4.2: Examples of the trajectory generated by the RPC modes over a section of the VSC unit's PQ capability diagram. The evolution of the trajectories is created following a ΔP change from the Po, Qo steady-state power conditions.

Thus, the study of the quasi-stationary AC voltage's profile support by means of a VSC unit, can be tackled as a power-trajectories analysis problem. The development of this analysis will start by proposing in section 4.2.2, a mathematical formulation for the regulation targets of each RPC mode, which will be later used by the directional derivative-based method (DDBM) in section 4.3.

4.2.2. Mathematical description of the VSC's RPC modes operation

The mathematical formulation for each RPC mode can be defined to express their regulation targets as presented in 4.4, 4.5, and 4.6.

$$Q_{Ctrl} \Rightarrow \frac{Q^* - Q_{meas}}{\Delta t} = \frac{\Delta Q_{VSC}(t)}{\Delta t} = 0 \tag{4.4}$$

$$PF_{Ctrl} \Rightarrow \frac{PF^* - PF_{meas}}{\Delta t} = \frac{\Delta PF_{VSC}(t)}{\Delta t} = 0 \tag{4.5}$$

$$U_{ACCtrl} \Rightarrow \frac{V^*_{PCC} - V_{PCC_{meas}}}{\Delta t} = \frac{\Delta V_{PCC}(t)}{\Delta t} = 0 \tag{4.6}$$

Here, it is assumed that PI regulators are used in each RPC mode. If other types of regulators (e.g. only proportional controllers) are considered, the mathematical formulations in 4.4, 4.5 and 4.6 do not hold and the analysis of power-trajectories should be performed by executing time domain simulations which can be very computationally expensive. Therefore, by considering PI regulators, it is assumed that they can ensure that for any $\Delta t > 0$, in 4.4, 4.5 and 4.6, each mathematical relationship can be satisfied. In this way, several implications of the use of each RPC mode, can be analyzed. First, if the Q_{Ctrl} is chosen, the V_{PCC} profile deviation will depend exclusively on the active power changes as shown in 4.3. Second, if the PF_{Ctrl} is chosen, the magnitudes of the active power gradient (APG) and the reactive power gradient (RPG), of the VSC unit, will be related as shown in 4.7. Thus the PF_{Ctrl} will generate a dependence between the Q_{VSC} and the P_{VSC} variables presented in 4.3 by means of a proportional constant, the λ factor. This factor represents the steady-state power ratio $\left|\frac{Q_{oVSC}}{P_{oVSC}}\right|$ to be maintained by the PF_{Ctrl}.

$$RPG = \lambda * APG \tag{4.7}$$

The third deduction is referred to the U_{ACCtrl} mode analysis. The mathematical relationship presented in 4.6 can be perceived as the rate of change of the V_{PCC} w.r.t. time. Consequently, the analysis V_{PCC} profile defined by 4.6 can be tackled by means of the description of two main elements: the partial derivatives of 4.3 and the description of the rate of changes of P_{VSC} and Q_{VSC} respectively. This analysis will allow to illustrate, the power-trajectory description for each RPC mode 4.4-4.6 using the DDBM presented in section 4.3.

4.3. DDBM for VSC unit power-trajectory description

4.3.1. Definition and Interpretation of dynamic vectors

The deployment of the DDBM for quasi-stationary voltage support analysis of a single infeed VSC unit will start by defining the vector spaces represented by the two diagrams shown in Figure 4.3. In this work, the first diagram (presented in Figure 4.3) represents the vector space that contains, the directional vector $\overrightarrow{PRR}$ (or the power ramp-rate vector of the VSC unit). As seen in Figure 4.3a, the directional $\overrightarrow{PRR}$ vector is comprised by the APG vector magnitude (i.e. $\frac{dP_{VSC}(t)}{dt}$ value), and the RPG vector magnitude (i.e. $\frac{dQ_{VSC}(t)}{dt}$ value). As the control modes of the VSC unit regulate the P_{VSC} and the Q_{VSC} provided to the power system, the rate of changes of the P_{VSC} and Q_{VSC} (i.e., APG and RPG) are also established by the control modes used by the VSC unit.

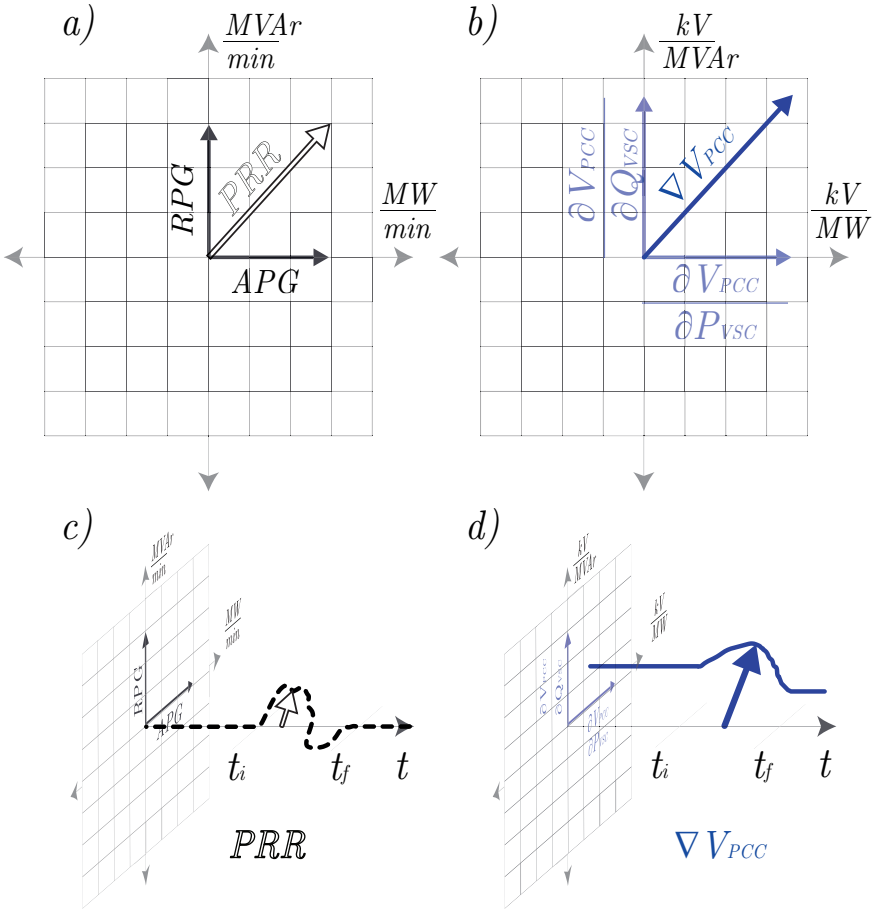


Figure 4.3: VSC power ramp-rate diagram shown in a) and voltage's gradient diagram shown in b). The dynamic vectors trajectories (in dash and solid lines) of the $\overrightarrow{PRR}$ and $\overrightarrow{\nabla V_{PCC}}$ are shown in c) and d) respectively.

Ergo, the directional $\overrightarrow{PRR}$ vector (in Figure 4.3a) and its corresponding trajectory (in Figure 4.3c) are $shaped$ by the control systems used by the VSC unit. For instance, during steady-state time periods, the norm of the $\overrightarrow{PRR}$ vector is null since the APG and the RPG vectors (in Figure 4.3a and Figure 4.3c) have zero magnitudes during these time frames. The second diagram (presented in Figure 4.3b) represents the vector space in which, the gradient vector field of the V_{PCC} function (shown in 4.3), is exhibit, that is to say, $\overrightarrow{\nabla V_{PCC}}$ vector. As shown in Figure 4.3b and Figure 4.3d, the $\overrightarrow{\nabla V_{PCC}}$ vector is comprised by the partial derivatives $\frac{\partial V_{PCC}}{\partial P_{VSC}}$ and $\frac{\partial V_{PCC}}{\partial Q_{VSC}}$, which are mainly defined by the power systems parameters, X_{th} and E_{th} expressed in 4.3. Consequently, the $shape$ of the trajectory exhibited by the $\overrightarrow{\nabla V_{PCC}}$ vector (in Figure 4.3d) is fundamentally determined by these power system param-

eters.

As the trajectories shown by the $\overrightarrow{\nabla V_{PCC}}$ vector (in Figure 4.3d) and the $\overrightarrow{PRR}$ vector (in Figure 4.3c) evolve in a time frame axis, $\overrightarrow{\nabla V_{PCC}}$ and $\overrightarrow{PRR}$ represent indeed, dynamic vectors. This dynamic vectors perspective allows to expose in a graphical and individual manner, the two main characteristics for the quasi-stationary V_{PCC} support. On one hand, the power system features such as the X_{th} and the E_{th} (exhibited by the $\overrightarrow{\nabla V_{PCC}}$ trajectory) and on the other hand, the power modulation executed by the control modes used by the VSC unit (exhibited by the $\overrightarrow{PRR}$ trajectory). The interaction analysis of the dynamic vectors trajectories will lead in to the formulation of an instantaneous voltage sensitivity factor (IVSF) as mathematically expressed in 4.8.

$$IVSF = \overrightarrow{\nabla V_{PCC}} \bullet \overrightarrow{PRR} \tag{4.8}$$

The IVSF is defined as the scalar product between the dynamic vectors $\overrightarrow{\nabla V_{PCC}}$ and $\overrightarrow{PRR}$. This scalar product defines the interaction between $\overrightarrow{PRR}$ (VSC's control modes) with $\overrightarrow{\nabla V_{PCC}}$ (AC network strength) and constitutes, the formulation of the directional derivative method as a way to describe the rate of change of V_{PCC} in Figure 4.1.

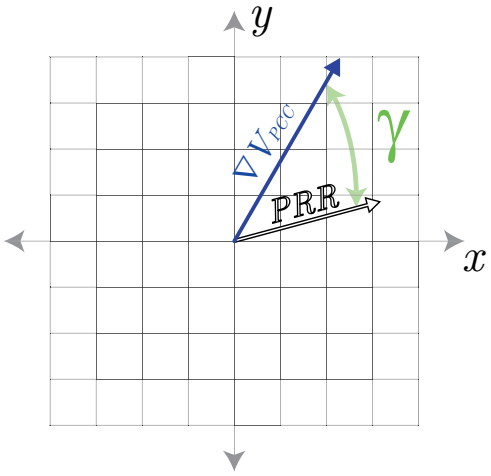


Figure 4.4: The γ angle (in green) representing the angular difference between the ∇V_{PCC} and PRR dynamic vectors shown in Figure 4.3c and Figure 4.3d.

If $\overrightarrow{PRR}$ and $\overrightarrow{\nabla V_{PCC}}$ are projected over the same Cartesian coordinate system (as shown in Figure 4.4), the angle γ between them can be defined as shown in 4.9.

$$\gamma = atan\left(\frac{\frac{\partial V_{PCC}}{\partial Q_{VSC}}}{\frac{\partial V_{PCC}}{\partial P_{VSC}}}\right) - atan\left(\frac{RPG}{APG}\right) \tag{4.9}$$

The mathematical formulations 4.8 and 4.9, depend on two main factors: the explicit knowledge of the vector field of V_{PCC} (i.e. $\overrightarrow{\nabla V_{PCC}}$), and the APG and RPG modulations executed by each control mode. The explicit knowledge of the vector field of the V_{PCC} is known since, the function of V_{PCC} has been explicitly defined in 4.3. Now, the $\overrightarrow{PRR}$ formulation can be elaborated based on the RPC mode formulations established in 4.4-4.6 and will be described from section 4.3.2 to section 4.3.5 to define the power-trajectories shown in section 4.4.

4.3.2. U_{ACCtrl} mode analysis based on DDBM

The regulation target of the U_{ACCtrl} mode can be expressed in terms of the DDBM, by imposing to the $IVSF$, the mathematical restriction stated in 4.6. This can be done by obtaining the partial derivatives of 4.3 and by defining the magnitude of the RPG vector (illustrated in Figure Figure 4.3a) as expressed in 4.10.

$$RPG = -APG\frac{\frac{\partial V_{PCC}}{\partial P_{VSC}}}{\frac{\partial V_{PCC}}{\partial Q_{VSC}}} \tag{4.10}$$

When 4.10 is substituted in 4.9, the γ angle (in Figure 4.4) becomes $\pm\frac{\pi}{2}$. This means that, from the DDBM point of view, the role of the U_{ACCtrl} mode is to modulate the RPG vector magnitude such that, the $\overrightarrow{PRR}$'s trajectory be orthogonal to the $\overrightarrow{\nabla V_{PCC}}$'s trajectory while a change in P_{VSC} is executed.

4.3.3. PF_{Ctrl} mode analysis based on DDBM

The regulation target of the PF_{Ctrl} mode can be expressed in terms of the DDBM, by evaluating the condition presented in 4.7 into the DDBM formulation shown in 4.9. If the partial derivative $\frac{\partial V_{PCC}}{\partial P_{VSC}}$ (which is a function of X_{th} as mentioned in section 4.1) is assumed to be very low (which is a valid assumption for low impedance networks), the γ angle can be expressed as presented in 4.11.

$$\gamma_{PF_{Ctrl}} \approx \pm\frac{\pi}{2} - atan(\lambda) \tag{4.11}$$

Now, if the magnitude of the IVSF in 4.8 is computed by considering the linear relationship presented in 4.7, the voltage deviation experienced by V_{PCC}, (as a consequence of having the VSC unit in Figure 4.1, operating in PF_{Ctrl} mode), will be defined by 4.12.

$$\left|IVSF_{PF}\right| = \left|\nabla V_{PCC}\right|\left|APG\left|\sqrt{1+\lambda^2}\right|cos(\gamma_{PF_{Ctrl}})\right| \tag{4.12}$$

It can be seen from 4.12 that, the magnitude of the IVSF gets amplified depending on the steady-state power ratio, λ value. Therefore, it is (in general) advisable to decrease the λ ratio for the operation of the PF_{Ctrl} mode by setting up in the PF_{Ctrl}, a PF reference value (PF^*) close to the unity.

4.3.4. Q_{Ctrl} mode analysis based on DDBM

Similar to the previous two RPC modes analysis, the regulation target of the Q_{Ctrl} mode will start by integrating the mathematical condition presented in 4.4 into the DDBM formulation shown in 4.8 and 4.9. If again, the partial derivative $\frac{\partial V_{PCC}}{\partial P_{VSC}}$ is assumed to be very low, then, the associated IVSF's magnitude and γ angle (for the Q_{Ctrl} mode DDBM analysis) can be described by 4.13 and 4.14.

$$\gamma_{Q_{Ctrl}} \approx \pm\frac{\pi}{2} \tag{4.13}$$

$$\left|IVSF_{Q}\right| = \left|\nabla V_{PCC}\right|\left|APG\right|\left|cos(\gamma_{Q_{Ctrl}})\right| \tag{4.14}$$

If the same steady-state power conditions P_{oVSC}, Q_{oVSC} and $|APG|$ are considered for 4.12 and 4.14, the comparison of the IVSF's magnitudes will be determined by the constant $\sqrt{1+\lambda^2}$ and the corresponding γ angles values presented in 4.11 and 4.13. In general, these two equations would lead to conclude that the PF_{Ctrl} is always the less attractive option for voltage support if it is compared against the Q_{Ctrl}. This conclusion has been also verified by performing specific field tests in [2]. However, the influence of $\frac{\partial V_{PCC}}{\partial P_{VSC}}$ on the γ magnitude, has not been so far considered for analyzing the quasi-stationary voltage support provided by a single-infeed VSC unit. In other words, the equations 4.11 and 4.13 have been obtained based on the assumption of having a very low value for the partial derivative $\frac{\partial V_{PCC}}{\partial P_{VSC}}$. Hence, if this assumption is not considered anymore (i.e., power system having high impedance network conditions), the magnitude of the γ angles will be entirely determined by the evolution of the $\overrightarrow{\nabla V_{PCC}}$ vector components (Figure 4.3b). Thus, depending on the steady-state power conditions (P_{oVSC} and Q_{oVSC}) and, the X_{th} value, the PF_{Ctrl} mode might provide a better voltage support if it is compared to the voltage support provided by the Q_{Ctrl} mode. This statement will be thoroughly analyzed in section 4.4.

4.3.5. APG vector's magnitude formulation and VSC-HVDC network configuration

The analysis of the active frame control modes, in terms of the DDBM, can be tackled by describing the implications of each regulation target (P_{Ctrl}, U_{DCCtrl}, or $Droop_{Ctrl}$) over the APG vector magnitude. Typically, the APG value is a constant parameter specified by the owner of an embedded PtP-VSC-HVDC system (c.f. section 2.1). Hence, if the active power balance is ensured within the HVDC network, the active power changes in one VSC unit (operating in P_{Ctrl}) will be reflected into the other VSC unit (operating in U_{DCCtrl}). Thus, the APG vector magnitude in a PtP-VSC-HVDC system operation, will be equivalent for both VSC units as described in 4.15.

$$PtP_{Op} \Rightarrow \left|APG_{U_{DCCtrl}}\right| = \left|APG_{P_{Ctrl}}\right| \tag{4.15}$$

On the other hand, in an MT-VSC-HVDC system, the active power balance regulation usually involves additional control strategies like the $Droop_{Ctrl}$ mode. This strategy allows to disseminate the regulation of the DC voltage within the MT-VSC-HVDC network, by distributing the DC power flow between the VSC units accordingly to a proportional constant, the K_{Droop}. Since the MT-VSC-HVDC systems are prone to include renewable energy sources (RES), the resulting APG values of the VSC units belonging to the MT-VSC-HVDC network, might not be constant. Therefore, a proportional factor (η) is defined to simultaneously consider the effects of the DC power flow strategies utilized by all VSC units within an HVDC network. Concretely, the factor η will allow to express the APG value for each VSC unit within the MT-VSC-HVDC network as defined in 4.16.

$$MT_{Op} \Rightarrow \left|APG_{VSC_i}\right| = \eta_{VSC_i}\left|APG_{RES}\right| \tag{4.16}$$

As seen in 4.16, the APG value of a particular VSC unit i (e.g. APG_{VSC_i}), depends on the active power gradient associated to the RES (e.g. APG_{RES}) included within the VSC-HVDC network. The range of η_{VSC_i} in 4.16 goes from a non-influence of the APG_{RES} (e.g. $\eta_{VSC_i} = 0$) to a maximum influence of the APG_{RES} (e.g. $\eta_{VSC_i} = 1$). The utilization of the η_{VSC_i} factor will be exemplified by considering a three-terminal (MT-VSC-HVDC) system described in section 4.5.

4.4. Graphical description of the DDBM for RPC's power-trajectories analysis

The mathematical formulations described in section 4.3 have geometrical implications that will be elaborated in this section. The orthogonality condition mentioned in section 4.3.2 for the $\overrightarrow{PRR}$ dynamic vector, can be illustrated by determining the vector field of V_{PCC} (i.e. $\overrightarrow{\nabla V_{PCC}}$) and project it over the *PQ capability diagrams* as shown in Figure 4.5. The vector field of V_{PCC} can be computed from the relationship presented in 4.3 if the power system features (X_{th} and E_{th} in Figure 4.1), and the power limits (P_{MAX}, Q_{MAX}) of the VSC unit are known. Therefore, the features of the power system and the VSC unit characteristics presented in [3] (summarized in Table 4.1) are utilized to develop the graphical description of the DDBM.

Table 4.1: VSC unit and power system features data

S_{Base}	P_{MAX}	Q_{MAX}	E_{th}	$X_{th_{low}}$	$X_{th_{high}}$
700 MVA	1 pu	0.3286 pu	405 kV	0.0196 pu	0.1225 pu

Once the vector field of V_{PCC} is known, the VSC-HVDC network configuration needs to be determined. For a PtP-VSC-HVDC system, the APG vector's magnitude is assumed to be constant as discussed in section 4.3.5. Consequently, the orthogonality condition produced by the U_{ACCtrl} mode 4.10, will generate the PRR's vector fields as the ones presented in Figure 4.5a, and Figure 4.5b. The dash lines shown

in Figure 4.5 represent the power trajectories in which, the regulation target of the U_{ACCtrl} mode is achieved 4.6. In other words (and from the DDBM point of view), the power-trajectories in which the scalar product of the $\overrightarrow{\nabla V_{PCC}}$ and the $\overrightarrow{PRR}$ is null.

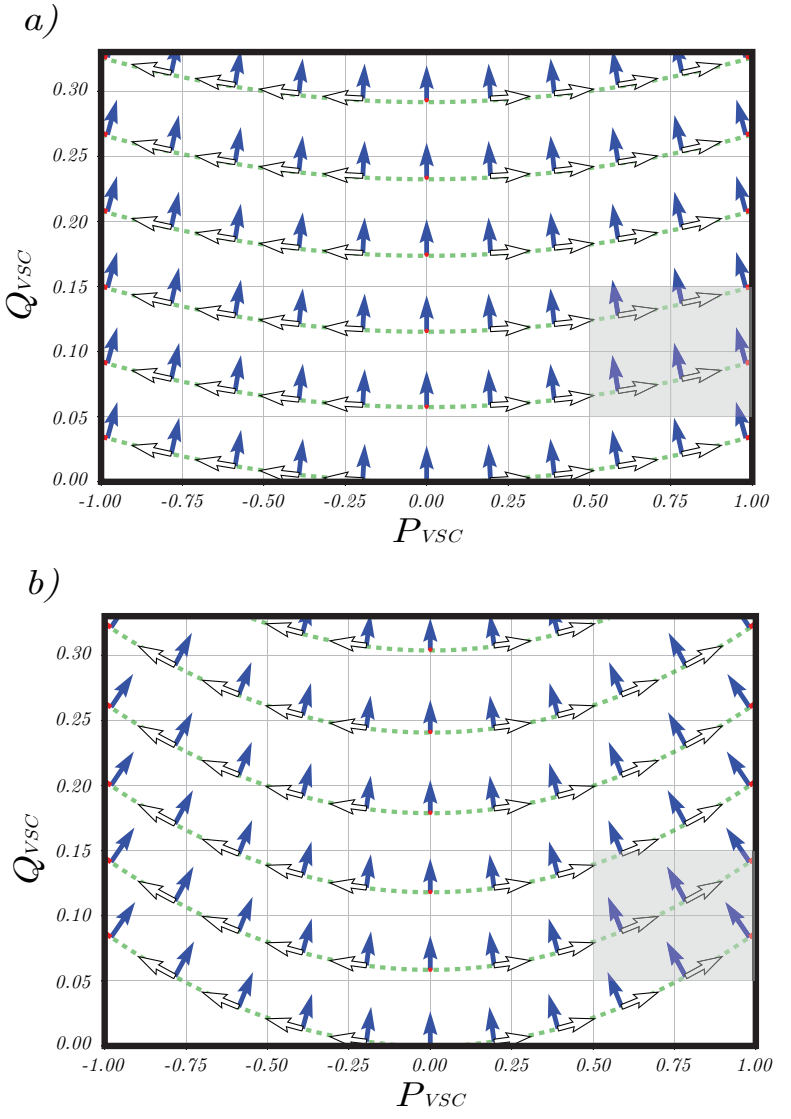


Figure 4.5: The orthogonality condition between $\overrightarrow{PRR}$ and $\overrightarrow{\nabla V_{PCC}}$ creating the power-trajectories of the $U_{AC_{Ctrl}}$ (dotted-green lines) for different the X_{th} conditions presented in Table 4.1. (a) The vectors fields of $\overrightarrow{PRR}$ and $\overrightarrow{\nabla V_{PCC}}$ projected over the *PQ capability diagram* of a VSC unit connected to a low impedance network ($X_{th_{low}}$), (b) The vectors fields of $\overrightarrow{PRR}$ and $\overrightarrow{\nabla V_{PCC}}$ projected over the *PQ capability diagram* of a VSC unit connected to a high impedance network ($X_{th_{high}}$)

Moreover, these dash lines, exhibit different curvature ratios, which are a consequence of the difference between the X_{th} network conditions in Table z4.1. Thus, it can be seen that the evolution of the RPG vector magnitude (i.e., the rate of change of reactive power in Figure 4.3a) for a high impedance network (Figure 4.5b), is prone to be higher than the one observed for the low impedance network (Figure 4.5a) case. Therefore, the quasi-stationary voltage support of a VSC unit, for a high-impedance network, is conditioned by its capability of providing fast reactive power modulation while an active power changes occur. This condition might constitute a challenge in terms of the VSC unit design and VSC unit's coordination with other voltage support systems (e.g., transformer tap changers) [4].

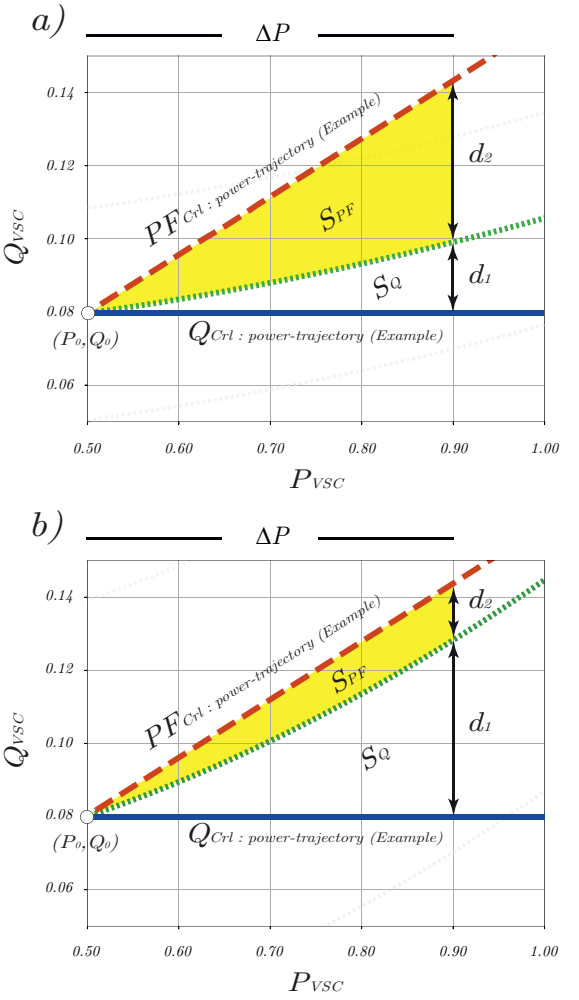


Figure 4.6: The power-trajectories for each RPC mode are presented within the sections of the PQ capability diagrams presented in Figure 4.5. The Figure 4.6a and Figure 4.6b, are representing the X_{th_A} and the X_{th_B} cases respectively.

Conversely, in Figure 4.5a, the associated $\overrightarrow{PRR}$ vector field is not prone to evolve (increase their RPG magnitude, c.f. Figure 4.3a) as fast as the $\overrightarrow{PRR}$ vector field, presented for the high impedance network case (i.e. Figure 4.5b). Hence, the Q_{Ctrl} mode might be considered as $a\ good\ option$ for providing quasi-stationary voltage support in V_{PCC} during low impedance network conditions. However, in order to illustrate the meaning of $a\ good\ option$ for the quasi-stationary voltage support (in either high or low impedance networks), a comparative assessment, based on a euclidean-distance criterion is proposed.

The euclidean-distance criteria will depend on the explicit knowledge of the points belonging to the power trajectories generated by each RPC mode. Thus, the determination of these points is a necessary step for the comparison process between the different quasi-stationary voltage support strategies of a VSC unit. The power-trajectories generated by the U_{ACCtrl} mode (shown as dash lines in 4.5), can be obtained by computing the level set curves from 4.3. On the other hand, the power-trajectories generated by the Q_{Ctrl} and the PF_{Ctrl} mode are based on the operational ranges, specified by the VSC unit operator and, will be illustrated by using the Figure 4.6. Please notice that Figure 4.6a and Figure 4.6b, constitute a zooming of the highlighted gray sections, presented in the PQ capability diagram of Figure 4.5a and Figure 4.5b respectively.

The formulations presented in 4.4 and 4.7, automatically define the behavior of the RPG magnitude vector (Figure 4.5a) for the Q_{Ctrl} mode and the PF_{Ctrl} modes, for any technically feasible APG value (or VSC-HVDC network configuration, c.f. section 4.3.5). These formulations would indicate that the points which belong to the power trajectories generated by either the Q_{Ctrl} or the PF_{Ctrl} mode, can be represented by means of a straight line or a sloped line as shown in Figure 4.6a and Figure 4.6b. Consequently, the Euclidean distances between the points belonging to each power trajectory can be used, to define the S factors (Riemann's sums) presented in 4.17.

$$S_Q = \sum_{i=0}^{n} |d_1(P_i)||\Delta P_i| \qquad S_{PF} = \sum_{i=0}^{n} |d_2(P_i)||\Delta P_i| \tag{4.17}$$

As it can be seen in Figure 4.6a and Figure 4.6b, the $d1$ and $d2$ values, represent the distances between the power-trajectories produced by the Q_{Ctrl} and PF_{Ctrl} modes w.r.t. the U_{ACCtrl} power-trajectory respectively. Please notice that the distance values depend on the active power level provided by the VSC unit, and the impedance network condition X_{th}. In 4.17(17), the S_Q and S_{PF} factors (respectively, the white and yellow areas in Figure 4.6) represent, the equivalent areas generated when an active power change (ΔP) occurs in the VSC unit, from its initial steady-state power conditions P_{oVSC} and Q_{oVSC}, (i.e. (P_o, Q_o) in Figure 4.6). Then, if the S_Q

and the S_{PF} factors values are compared, the one that possesses the minimum value (minimum area), will be closest to the U_{ACCtrl} power-trajectory. In other words, the minimum S factor identifies the RPC control mode, which produces the smallest quasi-stationary voltage deviation during an active power change in the VSC unit. From Figure 4.6a, it can be noticed that for the $X_{th_{low}}$ case, the area represented by the S_Q factor is smaller than the area represented by the S_{PF} factor. This means that, the Q_{Ctrl} mode can be considered as $a\ good\ option$ for the quasi-stationary voltage support of V_{PCC} if, it is compared against the PF_{Ctrl} mode for the same initial steady-state power conditions P_o, Q_o. However, in Figure 4.6b, the curvature ratio associated to the U_{ACCtrl} power-trajectory is shorter, which means that, the distance d_2 will also be shorter if it is compared against the one presented in Figure 4.6a. Thus, for this particular example, the area represented by the S_{PF} factor is smaller, than the one represented by the S_Q factor. Consequently, the PF_{Ctrl} mode can be considered as $a\ good\ option$ for quasi-stationary voltage support of V_{PCC} if, it is compared against the Q_{Ctrl} mode, for the same initial P_o, Q_o steady-state power conditions. Thus, the explicit determination of the power-trajectories, the selection of the steady-state power condition (P_o, Q_o), and the descriptions of the $\overrightarrow{\nabla V_{PCC}}$ and the $\overrightarrow{PRR}$ dynamic vectors represent the bases for the quasi-stationary voltage support analysis (of a single-infeed VSC unit), provided by DDBM.

The graphical methodology based on the S factors constitutes a first step to quickly provide a comparative assessment between the Q_{Ctrl} and the PF_{Ctrl} modes w.r.t. an ideal U_{ACCtrl} mode. However, some questions might appear, especially when the values of the S_{PF} and S_Q are quite similar. For these cases, it is necessary to introduce a second (more precise) comparative criteria in which the values of each $d_1(P_i)$ and $d_2(P_i)$ (belonging to a specific power-trajectories analysis) are contrasted. This more precise comparative criteria basically provides two main features. Firstly, it allows a substantial increase in the degree of accuracy for comparing the level of quasi-stationary voltage support for each RPC mode (e.g. Q_{Ctrl} and PF_{Ctrl}). Secondly, it allows determining the steady-state power conditions (e.g. P_o, Q_o), in which, the Q_{Ctrl} mode or the PF_{Ctrl} mode presents a superior performance (one respect to the other) for quasi-stationary voltage support.

The implementation of the second comparative criteria was developed as a MATLAB code in which all the possible steady-state points and power trajectories for the three RPC modes of the VSC unit were considered. Finally, the execution of the MATLAB code produced the areas presented in Figure 4.7a and Figure 4.7b respectively. The dotted (grey) regions in Figure 4.7a and Figure 4.7b define the steady-state power conditions in which the Q_{Ctrl} will exhibit better performance in terms of quasi-stationary voltage support rather than the PF_{Ctrl} mode.

Conversely, the solid (red) regions in Figure 4.7a and Figure 4.7b define the steady-state power conditions in which the PF_{Ctrl} will exhibit better performance in terms of quasi-stationary voltage support rather than the Q_{Ctrl}. Lastly, the white areas in Fig. 9a and Fig. 9b represent the steady-state power conditions in which

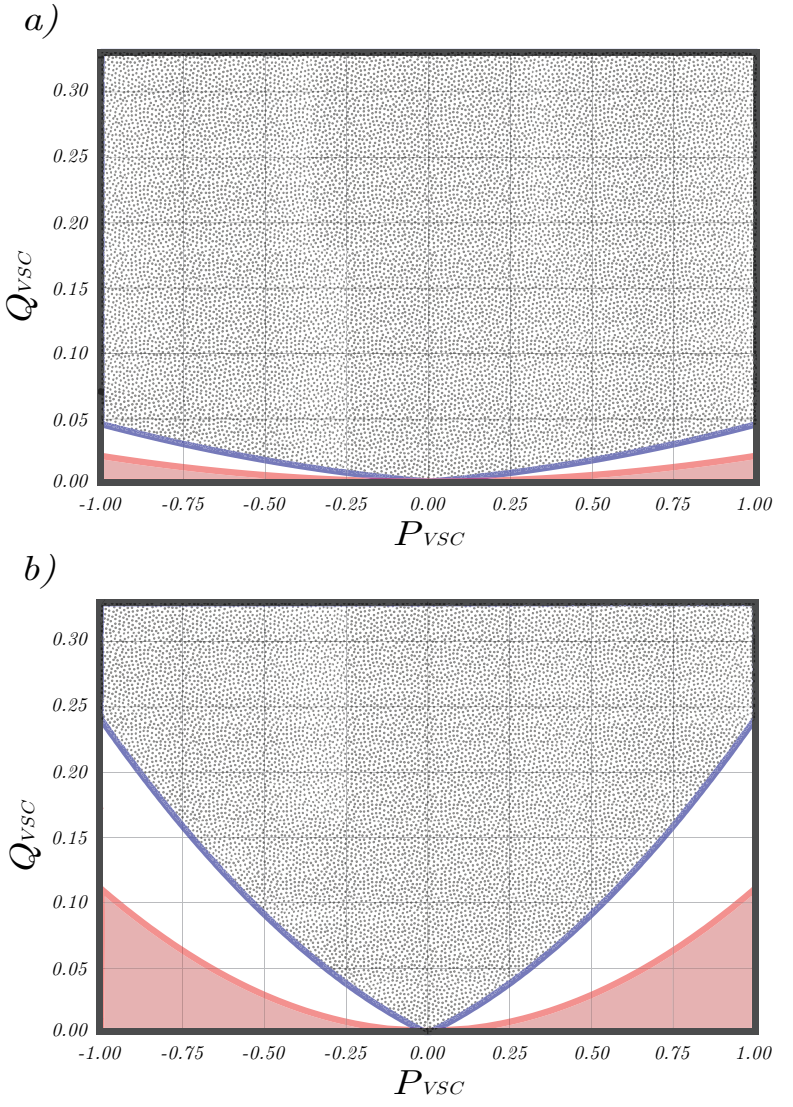


Figure 4.7: PQ capability diagram of one VSC unit connected to a low impedance network X_{th_A} (Figure 4.7a) and to a high impedance network X_{th_B} (Figure 4.7b). The regions within each PQ diagram represent the steady-state power conditions (Po, Qo) in which the Q_{Ctrl} (dotted gray area) and the PF_{Ctrl} (solid red area) can be used, as the second best option, for providing quasi-stationary voltage support.

the second-best option for quasi-stationary voltage support cannot be entirely attributed to a single RPC mode, that is to say, the PF_{Ctrl} or the Q_{Ctrl}. In the white areas, the level of quasi-stationary voltage support obtained will also depend on the

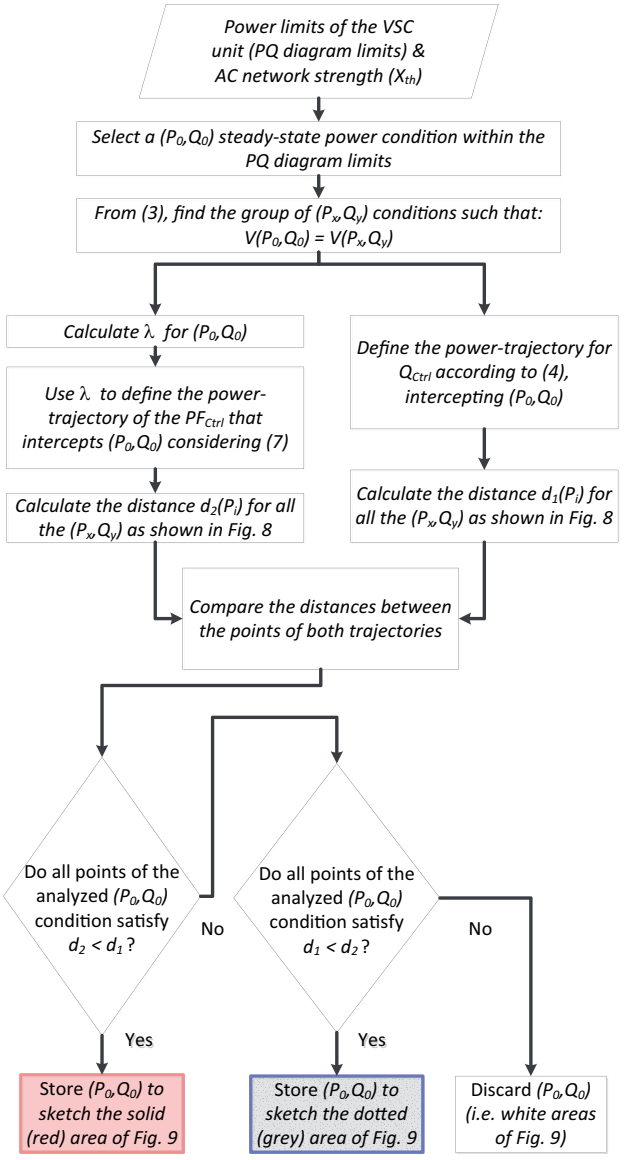


Figure 4.8: Flowchart of the MATLAB code showing the analytical process for determining if one steady-state power condition (P_o,Q_o) can be considered to generate the (red) solid, the (grey) dotted or the white area.

amount of active power change (increment or decrement) experienced by the VSC unit studied. The corresponding flowchart of the MATLAB code executed is shown in Figure 4.8.

It can also be noticed that the sizes of each region in Figure 4.7a and Figure 4.7b are comparatively different. This means that the evolution of the impedance network (i.e., from $X_{th_{low}}$ to $X_{th_{high}}$) will alter the conditions (i.e., Figure 4.7 areas) in which an RPC mode can be considered as an attractive option for providing quasi-stationary voltage support. In that sense, the DDBM provides a way to graphically compare the performance of the Q_{Ctrl} vs PF_{Ctrl} by simultaneously considering different AC network strength levels. For instance, using the Q_{Ctrl} in Figure 4.7a for a steady-state power condition equal to $Q_o = 0.15$ and $P_o = 0.50$ will create less V_{PCC} deviations than using PF_{Ctrl} for the same (P_o,Q_o) conditions. However, using the Q_{Ctrl} for a steady-state power condition equal to $Q_o = 0.05$ and $P_o = 0.75$ in Figure 4.7b, will generate a bigger V_{PCC} deviation if it's compared against the one generated by the PF_{Ctrl} mode. This does mean that by assuming an ideal U_{ACCtrl} mode (i.e. the most suitable quasi-stationary voltage control), the DDBM provides a fast way to illustrate which RPC mode is the second most attractive and the less attractive option for providing quasi-stationary voltage support based on the comparison of the distances (i.e., d_1 and d_2) obtained. It is worth remembering that, the graphical DDBM analysis conducted so far, has been based on the constant APG vector magnitude assumption for each RPC mode. However, the variable nature of the APG (most likely expected for a VSC unit belonging to an MT-VSC-HVDC network) will be covered in section 6. This analysis will be carried out by executing simulation experiments using a quasi-stationary phasor (or RMS) model for an expandable PtP-VSC-HVDC network, described in section 4.5.

4.5. Overall Description of the Test System

4.5.1. Simulation Setup for the expandable VSC-HVDC link

The simulation setup presented in this section has been developed in DIgSILENT PowerFactory 2018 by utilizing an expandable HVDC link (c.f. section 2.3.3) operating under a point-to-point and a multi-terminal DC network configuration as shown in Figure 4.7. Additionally, the simulation model used for the expandable PtP-VSC-HVDC link, and the AC networks utilized in this work have been obtained from the references [3, 5, 6] respectively. For the sake of illustration, it is assumed that the expansion of the PtP-VSC-HVDC link to MT-VSC-HVDC network concerns with the integration of an offshore wind farm (OWF) through a third terminal (VSC03 unit) as shown in Figure 4.9. It can also be noticed that the system data presented in Figure 4.9 is linked with the information provided in Table 4.1. Therefore, the vector fields shown in Figure 4.5a and Figure 4.5b, represent the ones associated with the onshore AC networks and the VSC units, VSC01 and VSC02 (shown in Figure 4.9), respectively. The islanded control scheme described in [7] has been implemented for the VSC03 unit to provide, the corresponding AC voltage reference to the OWF's network. The control schemes for the OWF units have been implemented based on the modelling work presented in [8]. Additionally, the wind power generation profile associated with the OWF units was defined, based on real wind power generation data obtained from a European transmission system operator in [9].

As described in [10], the DC power flow regulation in an expandable VSC-HVDC link can be carried out by utilizing the Droop Line Tracking (DLT) method if the access to the DC voltage reference's regulation is guaranteed in those selected VSC units within the multi-terminal HVDC network configuration. This means that if the onshore converters (VSC01 and VSC02) are selected to use DC voltage control (i.e., Udc_{Ctrl}), then the DLT method will modify their DC voltage references to establish the power flow regulation within the multi-terminal HVDC network based on 2.21 as discussed in section 2.3.3. Furthermore, it is worth remembering that several types of DC voltage control strategies (e.g., master-slave, single slope droop, or even multi-slope droop DC voltage control) can be set up in the DLT method for establishing the DC power flow profile in a multi-terminal HVDC network [10].

Notwithstanding, the simulations developed for the multi-terminal configuration of the expandable VSC-HVDC link are exclusively based on the single slope droop (DC voltage) control in this work. This consideration allows to simplify the analysis of the quasi-stationary voltage support, provided by each onshore VSC unit, in Figure 4.9. Moreover, the use of the single slope droop also allows to define a constant value for the η factor (described in section 4.3.5). In this connection, the quasi-stationary voltage support of a VSC unit belonging to a MT-VSC-HVDC system is analyzed by considering two single slope droops cases. The first case has been defined such that the output power profile of the OWF is identically distributed between the onshore VSC units VSC01 and VSC02. In other words, η = 0.5 for both onshore VSC units. The second case is defined such that the output power profile of the OWF is distributed in different proportions, between the onshore VSC units as presented in Table 4.2.

Table 4.2: Multi-terminal DC power flow cases for the expandable HVDC link (shown in Figure 4.9).

η	η_{VSC01}	η_{VSC02}	η_{VSC03}
Case 1	0.5	0.5	1
Case 2	0.02	0.98	1

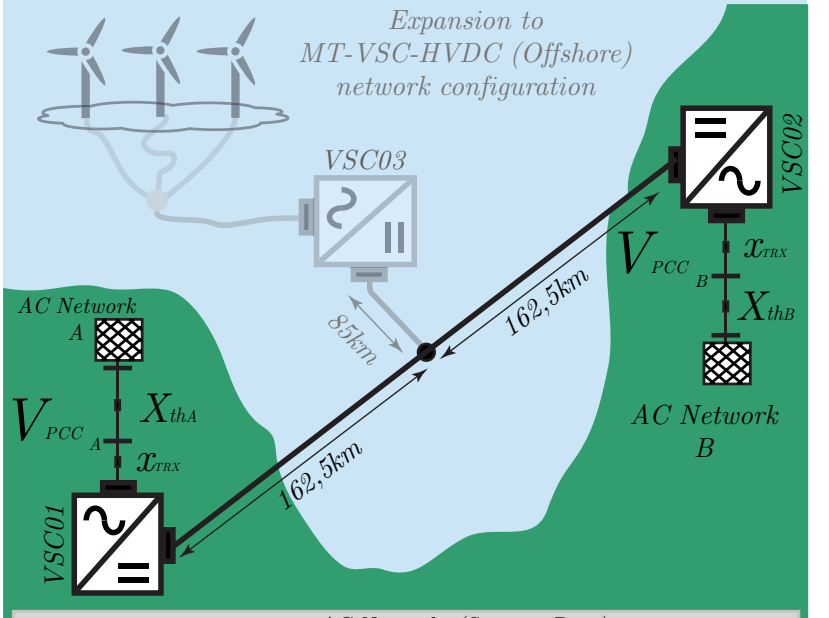
The different η proportions have been selected to expose the influence of a variable APG magnitude in the quasi-stationary voltage support for the different AC networks presented in Figure 4.9.

4.6. Simulation Results

4.6.1. Quasi-stationary voltage support in point-to-point configuration

The simulation experiments executed for the point-to-point operation of the expandable HVDC link are presented in Figure 4.10. It is shown in Figure 4.10a, that, the VSC01 unit is subjected to a change in its steady-state active power condition at t = 10s. This reduction (from 560MW to 50MW) in the active power transmitted between VSC01 and VSC02, induces different reactive power responses as shown in

Expandable PtP-VSC-HVDC (System Data)			
Functional Specification	PtP-VSC-HVDC (Onshore) [3]		Expansion to MT-VSC-HVDC (Offshore) [6]
	VSC01	VSC02	VSC03
Active Power (MW)	±700		+800
DC Voltage (kV)	±320		±320
Reactive Power (MVAr)	±230		N/A



AC Networks (Systems Data)			
AC Network Parameters	AC Network (Onshore) [3]		AC Network (Offshore) [6]
	X_{thA}	X_{thB}	
Equivalent Network Impedance (W)	4,58	28,77	Based on the AC network layout shown in [3] and the Wind Turbine (RMS) model in [8].
AC Voltage (kV)	405		

Figure 4.9: Expandable PtP-VSC-HVDC network. The PtP-VSC-HVDC network configuration is represented by the elements highlighted in black color and the MT-VSC-HVDC expansion is represented by the elements highlighted in gray color.

the left side of Figure 4.10b and Figure 4.10c. These reactive power responses depend on the RPC mode utilized and the associated AC network strength (impedance levels) to which the VSC units are connected to.

As described in 4.7, the PF_{Ctrl} leads to a linear relationship between the APG and the RPG which is scaled up by the steady-state power ration factor, $\lambda = \frac{50MVAr}{560MW}$.

Additionally, the deployment of the reactive power executed by the U_{ACCtrl} mode of VSC01 in Figure 4.10b, is comparatively smaller than the one produced by the same RPC mode in the VSC02 unit as shown in the left side of Figure 4.10c. These reactive power deployments from each VSC unit will guarantee, a constant steady-state voltage magnitude for V_{PCC_A} and V_{PCC_B} as shown in the right side of the Figure 4.10b and the Figure 4.10c, respectively. This non voltage deviation presented in (the right side of) Figure 4.10b and Figure 4.10c (for the ΔV_{PCC} responses), is completely aligned with the implications observed when projecting the vector field of the $\overrightarrow{PRR}$ (described in section 4.3.1) over the PQ diagrams as shown in Figure 4.5. That is to say, the faster reactive power deployment produced by the U_{ACCtrl} mode in the left side of Figure 4.10c, is a consequence of having a shorter curvature ratio in Figure 4.5b in comparison to the one exhibited by Figure 4.5. This demonstrates that the reduction of the short circuit impedance in a power system (caused by the decommissioning of conventional power plants) will lead to increase the RPG capabilities of the VSC units to provide quasi-stationary voltage support at transmission levels.

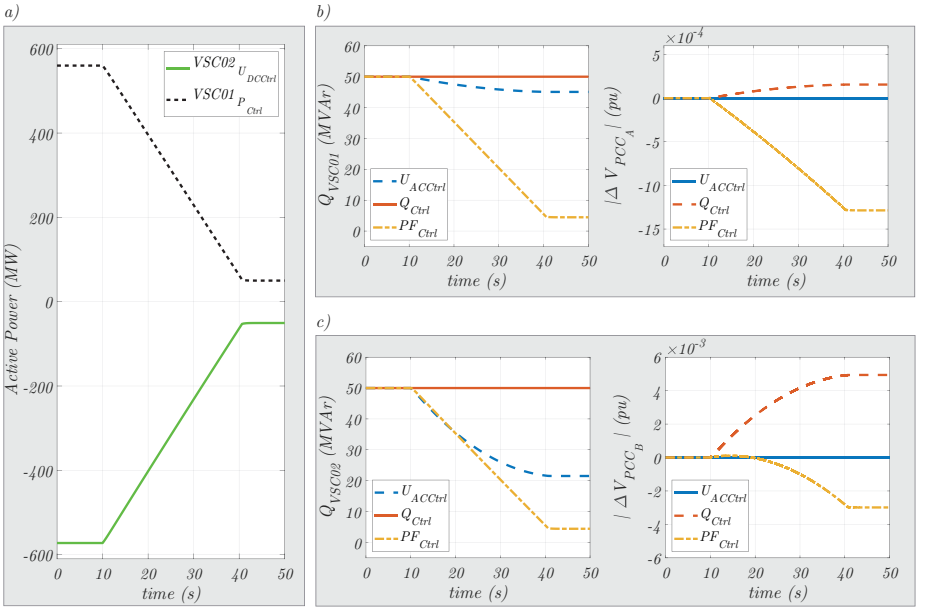


Figure 4.10: The expandable HVDC link operating under a PtP-VSC-HVDC network configuration (i.e., the grey elements in Figure 4.9 are not presented). Figure 4.10a presents the linear decrement in the active power transferred through the onshore VSC units. The left sides of Figure 4.10b and Figure 4.10c show the deployment of the reactive power executed by each RPC mode during the active power decrement event. The right sides of Figure 4.10b and Figure 4.10c show the corresponding quasi-stationary voltage deviation experienced by ΔV_{PCC} in each AC network.

The deviations of the steady-steady voltages V_{PCC_A} and V_{PCC_B} produced by the Q_{Ctrl} mode and the PF_{Ctrl} mode are also observed in the right side of Figure 4.10b and Figure 4.10c. If all the ΔV_{PCC} responses in Figure 4.10b and Figure 4.10c are

examined, it is clear that the U_{ACCtrl} mode is the one that provides the best quasi-stationary voltage support since it does not generate quasi-stationary (steady-state) voltage deviations (ΔV_{PCC}) in each AC network. However, the second best alternative for providing quasi-stationary voltage support is determined based on the ΔV_{PCC} deviations produced by the Q_{Ctrl} and the PF_{Ctrl} w.r.t. the one generated by the U_{ACCtrl}. It can be seen in (the right side of) Figure 4.10b, that the steady-state deviation experienced by the V_{PCC_A} voltage (i.e., ΔV_{PCC_A}) is lower when the Q_{Ctrl} mode is utilized. Conversely, in (the right side of) Figure 4.10c, the PF_{Ctrl} is the RPC mode which generates the smaller steady-state voltage deviation ΔV_{PCC_B}. The difference in these two results can be explained based on two factors: the AC network strength of each network (X_{th_A} and X_{th_B} in Figure 4.9) and the P_{oVSC} and Q_{oVSC} conditions of each VSC unit. These two factors are simultaneously considered within the areas presented in Figure 4.7a and Figure 4.7b respectively. Ergo, Figure 4.7 represents a way to graphically identify (depending on the AC network strength), the second best and the last RPC mode option to be considered for providing quasi-stationary voltage support depending on the steady-state power conditions (P_o,Q_o) of the VSC unit analyzed. Additionally, Figure 4.7 is independent of the variability associated with the APG magnitude which is associated with the type of VSC-HVDC network (point-to-point or multi-terminal) in which the onshore VSC unit can be connected to. This statement will be studied in Section 4.6.2 by enabling the multi-terminal expansion of the PtP-VSC-HVDC system (used in this simulation experiment) as described in section 4.5.1.

4.6.2. Quasi-stationary voltage support in multi-terminal configuration (Case 1)

The simulation results concerning case 1 presented in Table 4.2, for the MT-VSC-HVDC operation of the expandable PtP-VSC-HVDC system are presented in Figure 4.12. It can be seen in Figure 4.12a, that the wind power profile injected into the VSC-HVDC network by the VSC03 unit (shown in Figure 4.9), has been equally distributed between the onshore VSC units, as indicated by the η_{VSC01} and η_{VSC02} factors in Table 4.2. The steady-state power conditions analyzed for case 1 are shown in Figure 4.12a, and in the left side of Figure 4.12b and Figure 4.12c respectively. Concretely, the steady-steady power conditions are: Q_{oVSC01} = 2MVAr, P_{oVSC01} = 280MW, Q_{oVSC02} = 14MVAr and $P_{oVSC02} \approx$ 280MW. These steady-state power conditions have been selected to asses the feasibility of enabling the simultaneous operation of the PF_{Ctrl} in the VSC onshore units of the MT-VSC-HVDC network configuration shown in Figure 4.9.

In the left side of Figure 4.12b and Figure 4.12c, the reactive power deployments of each onshore VSC unit are shown. It can be seen (in the left side of) Figure 4.12b and Figure 4.12c that the deployments of the reactive power executed by the PF_{Ctrl} and the U_{ACCtrl} are quite similar. These reactive power similarities also derive in smaller quasi-stationary voltage deviations (ΔV_{PCC} responses) as the ones presented in the right side of Figure 4.12b and Figure 4.12c. In other words, the PF_{Ctrl} exhibits for both onshore VSC units a higher level of quasi-stationary voltage

support (less ΔV_{PCC} deviation), if it is compared against the ΔV_{PCC} deviations generated by the Q_{Ctrl} mode observed in the right side of Figure 4.12b and Figure 4.12c. However, it is relevant to clarify that for this case, the steady-state power ratio of VSC01 is: λ_{VSC01} = 0,007$\frac{MVAr}{MW}$. This means that the corresponding reference of the PF_{Ctrl} for VSC01 is respectively: PF^{*}_{VSC01} = 0.9999. In other words, the feasibility of using the PF_{Ctrl} mode in a VSC unit connected to a low impedance network (e.g. X_{th_A} in Figure 4.9) would require, a high precision measurement system to consider (at least) a 4 decimals resolution for the PF_{Ctrl} mode. This high precision measurement requirement and the level of quasi-stationary voltage support achieved by the PF_{Ctrl} in Figure 4.12b makes impractical its implementation for a low impedance network.

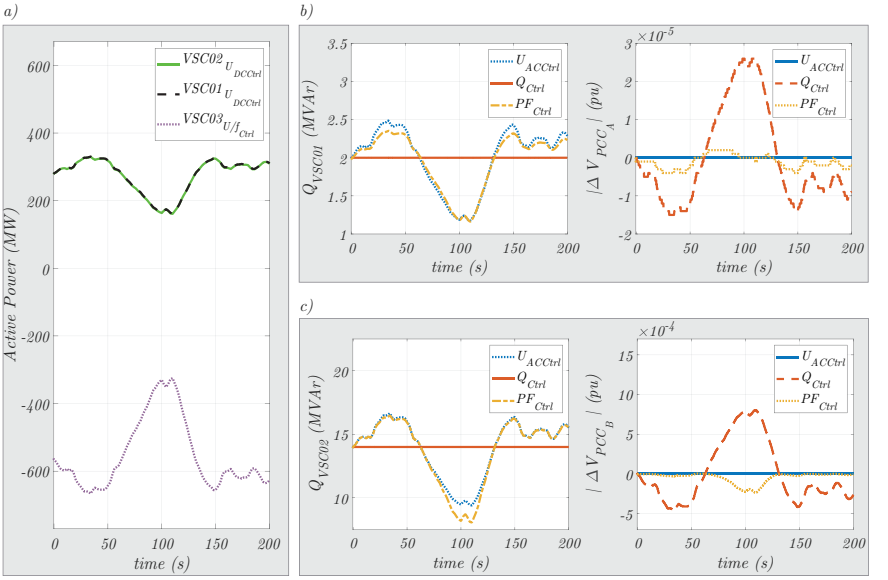


Figure 4.11: The Expandable PtP-VSC-HVDC system operating under the MT-VSC-HVDC network configuration shown in Figure 4.9. In Figure 4.12a, the wind power provided by VSC03 and its distribution (in the onshore VSC units) is shown accordingly to the case 1 shown in Table 4.2. In the left sides of Figure 4.12b and Figure 4.12c, it is shown the deployment of the reactive power executed by each RPC mode in each onshore VSC unit. In the right sides of Figure 4.12b and Figure 4.12c, the RPC modes are compared in terms of the steady-state voltage deviation (ΔV_{PCC}) produced in the reduced AC networks representation shown in Figure 4.9.

On the other hand, the steady-state power ratio associated with the VSC02 unit is λ_{VSC02} = 0,05$\frac{MVAr}{MW}$. This means that the PF_{Ctrl} reference for VSC02 is PF^{*}_{VSC02} = 0.9987. Thus, it can be seen that, the increment in the impedance network (e.g., X_{th_B} in Figure 4.9) can lead to a slightly less precise (or more flexible) resolution for the utilization of the PF_{Ctrl} mode. However, the utilization of the PF_{Ctrl} mode will just lead to superior quasi-stationary voltage support if it is compared against the one provided by the Q_{Ctrl} mode as shown in this simulation experiment. Thus, the quasi-stationary voltage support information presented by Figure

4.7 has been verified considering, an identical distribution of the wind power, between the onshore VSC units of the expandable PtP-VSC-HVDC system operating under a MT-VSC-HVDC network configuration.

4.6.3. Quasi-stationary voltage support in multi-terminal configuration (Case 2)

The simulation results concerning case 2 presented in Table 4.2, for the MT-VSC-HVDC operation of the expandable PtP-VSC-HVDC system are presented in Figure 4.12. In Figure 4.12a, it can be seen that the wind power profile provided by the VSC03 unit, has been unequally distributed between the onshore VSC units. As shown in Figure 4.12a, almost the entire wind profile ($\eta_{2_{VSC02}} \approx 0.98$) is been captured by the VSC02 unit. This means that most of the wind power will be provided to the high impedance network X_{th_B} (as shown in Figure 4.9).

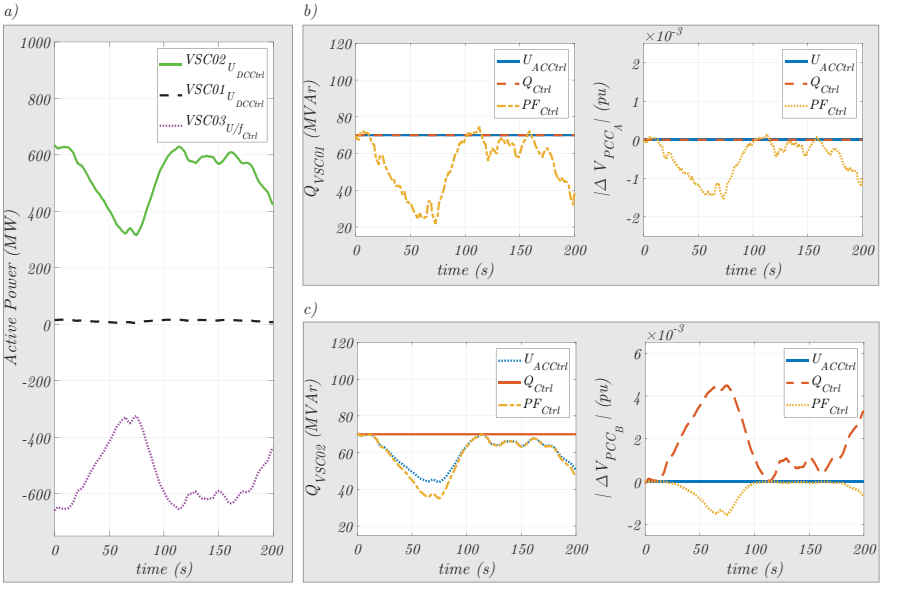


Figure 4.12: The Expandable PtP-VSC-HVDC system operating under the MT-VSC-HVDC network configuration shown in Figure 4.9. In Figure 4.12a, the wind power provided by VSC03 and its distribution (in the onshore VSC units) is shown accordingly to case 2 (i.e., η_{VSC_i} description) shown in Table 4.2. In the left sides of Figure 4.12b and Figure 4.12c, it is shown the deployment of the reactive power executed by each RPC mode in each onshore VSC unit. In the right sides of Figure 4.12b and Figure 4.12c, the RPC modes are compared in terms of the steady-state voltage deviation (ΔV_{PCC}) produced in the reduced AC networks representation shown in Figure 4.9.

Accordingly to Figure 4.7b, the selection of the PF_{Ctrl} as the second best option for providing quasi-stationary voltage support in a high impedance network, is slightly more suitable than in a low impedance network condition (Figure 4.7a). Thus, if the steady-state reactive power conditions are examined in the left side of Figure 4.12b and Figure 4.12c (i.e., Q_{oVSC01} = Q_{oVSC02} = 70MVAr), the steady-stated

power ratios can be determined: λ_{VSC01} = 4.441$\frac{MVAr}{MW}$ and λ_{VSC02} = 0.111$\frac{MVAr}{MW}$. These steady-stated power ratios automatically define the references utilized for the PF_{Ctrl} in each VSC onshore unit, that is to say: PF^{*}_{VSC01} = 0.2197 and PF^{*}_{VSC02} = 0.9939. Then, if the reactive power deployment for each RPC is observed in the left side of Figure 4.12b, it is found that the Q_{Ctrl} and the AC_{Ctrl} exhibit almost an identical behavior. This means that the steady-state power conditions considered for the VSC01 unit and its AC network strength value (i.e., X_{th_B} in Figure 4.9) generate a $\gamma_{Q_{Ctrl}} \approx \frac{\pi}{2}$ as indicated in section 4.3.4. Consequently, the quasi-stationary voltage deviation (i.e. ΔV_{PCC_A}) induced by the PF_{Ctrl} is comparatively higher w.r.t. the ones produced by other RPC modes as shown in the right side of Figure 4.12b.

The deviation induced by the PF_{Ctrl} is an expected result since, it depends on the λ_{VSC01} value selection as explained in section 4.3.3 and section 4.3.4. The quasi-stationary voltage deviations of V_{PCC} in the AC network B (i.e., ΔV_{PCC_B} in Figure 4.9) associated with the different reactive power modulation executed by each RPC mode in the VSC02 unit, are shown in the right side of Figure 4.12c. Here, it is shown that the utilization of the Q_{Ctrl} mode leads to the worst quasi-stationary voltage support if it is compared against the other RPC modes. These results demonstrate that the regions obtained in Figure 4.7 (based on the DDBM analysis), can effectively classify the level of quasi-stationary voltage support provided by each RPC mode in a single-infeed VSC unit independently of the APG characteristics (i.e., variable of constant) associated to the VSC-HVDC network configuration. Additionally, it can be seen that the influence of the unequal wind power distribution (between the onshore VSC units) over the quasi-stationary voltage support level, is again determined, by mainly two factors. First, the evolution of the power trajectories associated with each RPC mode, and second, the steady-state power conditions in which the Q_{Ctrl} and the PF_{Ctrl} operate under different AC network strength levels.

4.7. Conclusions

This chapter presented an analytical method based on directional derivatives to assess the level of quasi-stationary voltage support provided by a single-infeed VSC unit operating within a point-to-point or a multi-terminal VSC-HVDC system. The assessment was performed by proposing a set of mathematical formulations for describing the active and reactive power control (RPC) modes, during the quasi-stationary operation of a VSC unit. The formulations proposed allowed to define dynamic vectors which were used to separately analyze the control actions of a VSC unit and the AC network features (i.e. AC network strength) of a reduced power system representation. The analysis of the interaction of the dynamic vectors led to define an instantaneous voltage sensitivity factor (IVSF) which provides the necessary geometrical insight to determine the power trajectories for each RPC mode considered. The determination of these power-trajectories allowed to develop a quantitative criteria based on Riemann's sums (S factors) and Euclidean distances. This quantitative criteria produced a graphical representation in which, the conditions defining the first, the second, and the third best RPC option for providing quasi-stationary voltage support (under different AC network strength conditions) were obtained.

The graphical representation was derived by implementing a MATLAB code in which, the vector fields of the PRR and V_{PCC} vectors were obtained and projected over the PQ diagram of the VSC unit. These projections facilitate the assessment of the level of quasi-stationary voltage support provided by each RPC mode, as a function of the AC network strength and the steady-state power conditions associated with the VSC unit. It was revealed that in some cases, the power factor control (PF_{Ctrl}) can lead to better quasi-stationary voltage support if it is compared against the reactive power control (Q_{Ctrl}) under the same high impedance network and the same (and very specific) steady-state power conditions. Additionally, it was also discussed that the implementation of such RPC mode (i.e., PF_{Ctrl}) in a VSC unit might result very challenging due to its high precision measurement requirements. These conclusions were verified by performing simulation experiments in DIgSILENT PowerFactory 2018 by considering an expandable point-to-point VSC-HVDC system operating in a multi-terminal and a point-to-point configuration. The different VSC-HVDC Network configurations analyzed revealed that the influence of the active power gradient (APG) over the quasi-stationary voltage support is modulated by mainly two factors: the evolution of the power-trajectories associated with each RPC mode and, the steady-state power conditions in which the Q_{Ctrl} and the PF_{Ctrl} operate for different AC network impedance levels.

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5

Harmonic-Amplitude Modulation (HAM) strategy for frequency support by PtP-VSC-HVDC links

In this chapter, a Harmonic-Amplitude Modulation (HAM) strategy for PtP-VSC-HVDC links is developed as a way of providing frequency support to those power systems affected by a power unbalance event. The HAM strategy is developed by means of control systems that utilize the existing HVDC cable for transmitting the corresponding command for adjusting the supplied active power level in order to support the frequency deviation phenomena occurring at the affected power system.

5.1. HAM for non-embedded PtP-VSC-HVDC links

The description of the HAM control starts by recalling section 2.2.1, where the circulating currents i_{circ_x} of the converter unit were described as the electrical currents that are flowing at each branch of the DC circuit shown in Figure 2.6 (c.f. section 2.2.1). Additionally, i_{circ_x} is formed by the combination of a third of the DC current (i.e. i_{dc}) and a harmonic (balanced) current (i.e. i_{hbal_x}) as shown in 5.1. Interestingly, the additional term i_{HAM_x} presented in 5.1 represents a harmonic amplitude modulated current (i.e. i_{HAM_x}) which is not cancelled at the DC buses (i.e. DC side black dots) presented in Figure 2.6 of section 2.2.1.

$$i_{cc_x} = \frac{i_{dc}}{3} + i_{hbal_x} + \frac{i_{HAM_x}}{3} \tag{5.1}$$

This implies that the first and the third terms presented in the right side of the equality in 5.1 are introduced within the DC cables of the non-embedded HVDC link shown in Figure 5.1. The introduction of a HAM current is developed as a way of transmitting a signal (through the DC cables) carrying out the necessary data for adjusting the active power reference of the HVDC link. This adjustment is designed to be executed when a power unbalance event jeopardize the frequency profile in Network A shown in Figure 5.1. Furthermore, the signal transmission process is developed under the assumption that a dedicated communication channel (e.g. fiber optic cable) is not available at the HVDC link shown in Figure 5.1.

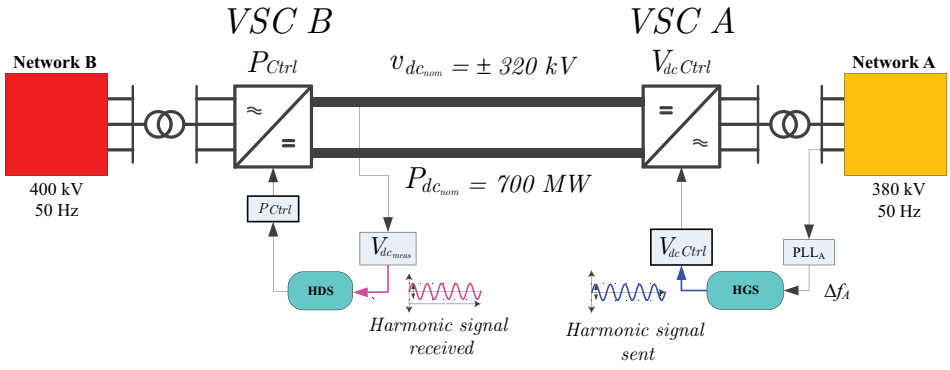

Figure 5.1: Non-embedded HVDC link including the proposed HAM control strategy based on the Harmonic Generation System (HGS) and the Harmonic Detection System (HDS).

The frequency support methods that consider the absence of dedicated communication channels (sometimes called *communication-free* frequency support methods c.f. [1–6]) usually modify the power flow in HVDC links by typically introducing non-oscillatory changes in the DC voltage levels across the HVDC network (e.g. [7, 8]). Nevertheless, the introduction of oscillatory changes for transmitting information across high-power conductors has been historically developed for HVAC networks (also known as power-line communication strategies) where the transmission lines are used as the medium for simultaneously transferring data and electrical

power.

On the other hand, the introduction of harmonic currents within DC cables enabling the transmission process of data between HVDC converter stations based on modular multi-level technology is essentially proposed in this chapter by means of two control systems as shown in Figure 5.1. These two control systems are in charge of detecting (receiving) and generating (sending) the harmonic signal having the adjustment of the active power reference of the HVDC link.

Consequently, the explanation of the control structures regarding the harmonic generation system (HGS) and the harmonic detection system (HDS) shown in Figure 5.1 are further elaborated in section 5.1.1 and section 5.1.2 respectively. It is worth mentioning that the electrical characteristics of the DC cables shown in Figure 5.1 would influence the speed of the propagation (i.e. propagation delay) of the introduced harmonic signals. The propagation delay can be calculated when these electrical characteristics are known, by utilizing a transfer function representation for the DC cables. In that sense, the total resistance (R_T), inductance (L_T), and capacitance (C_T) values associated with the DC cables shown in Figure 5.1 are 11Ω, 80mH, and 200μF, respectively. Next, the proposed transfer function describing the frequency response of the DC cables (located between VSC A and VSC B units) is shown in the expression 5.2.

$$\frac{V_B(s)}{V_A(s)} = \frac{1}{L_T C_T s^2 + R_T C_T s + 1} \tag{5.2}$$

When the R_T, L_T, and C_T are substituted in the expression 5.2, the magnitude of the first coefficient (i.e., $L_T C_T$) is comparatively (140 times) much lower than the second coefficient in 5.2 (i.e., $R_T C_T$). This difference helps to generate a first-order approximation of the expression 5.2. By doing so, the corresponding propagation delay affecting the introduced harmonic signals within the DC cable will be defined by the time constant ($R_T C_T$) of the generated first-order transfer function (i.e., 2,2ms).

5.1.1. Generating the harmonic oscillatory signal

In the proposed HAM strategy, the generation of the harmonic signal into the HVDC cables is developed by the HGS block (initially shown in Figure 5.1 and expanded in Figure 5.2). In short, the PLL system of VSC A (i.e. the rectifier VSC station) is utilized for providing the input signal (i.e. the measured electrical frequency of the Network A) for the HGS block.

The electrical frequency Δf_A signal is then passed through a deadband block and a proportional gain K which amplifies such a Network A signal. The amplified Δf_A signal is sent to detector blocks (c.f. Figure 5.2) that are used to identify if the nature of the frequency disturbance corresponds to an over-frequency or an under-frequency issue. The identification process in the detectors blocks is carried out by determining the properties (i.e. positive or negative sign) of the amplified

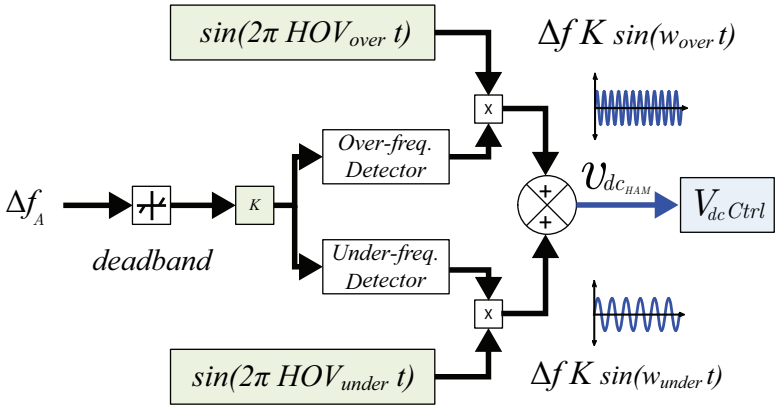

Figure 5.2: Harmonic Generation System (HGS) of Figure 5.1.

Δf_A signal. If the Δf_A signal is positive, the output of the *Under-frequency Detector* block will be automatically set to zero and the output of the *Over-frequency Detector* block will be equal to the amplified Δf_A signal. On the other hand, if the Δf_A signal is negative the output of the *Over-frequency Detector* block will be automatically set to zero and the output of the *Under-frequency Detector* block will be equal to the amplified Δf_A signal. Thus, the signal $v_{dc_{HAM}}$ presented in Figure 5.2 can be described as shown in 5.3.

$$v_{dc_{HAM}} = K\Delta f_A(t)sin(2\pi HOVt) \tag{5.3}$$

Notice that in 5.3, the $v_{dc_{HAM}}$ signal depends on the harmonic oscillatory values (HOV_{under} or HOV_{over}) generated by the oscillatory blocks shown in Figure 5.2, which means that the nature of the frequency disturbance occurring in Network A is directly reflected in the harmonic frequency of $v_{dc_{HAM}}$. On the other hand, the amplitude of the harmonic $v_{dc_{HAM}}$ signal is defined by the amplification factor K and the severity of the power unbalance affecting Δf_A. Ergo, it can be seen that the generated $v_{dc_{HAM}}$ signal simultaneously contains the information regarding the level of frequency deviation (amplitude of $v_{dc_{HAM}}$), and the over or under-frequency nature (HOV of $v_{dc_{HAM}}$) of the disturbance occurring in Network A.

It can be noticed from 5.3 that Δf_A essentially modulates the amplitude of the harmonic $v_{dc_{HAM}}$ signal as well as the K proportional factor. However, the selection of the K value needs to be carefully considered to prevent unwanted instabilities across the HVDC network. These instabilities can be prevented by adjusting the HGS' parameters based on a frequency domain (i.e. harmonic stability or selective modal) analysis or a time domain-based sensitivity study to ensure a stable response of the HVDC network. Furthermore, in a DC network comprised by VSC units (exclusively based on 2 levels technology), the introduction of harmonic signals have been recently explored in [9], where the maximum harmonic amplitude considered is lower than 1% of the nominal DC network voltage.

On the other hand, the selection of the HOVs utilized by $v_{dc_{HAM}}$ is another aspect that needs to be carefully considered to prevent a detriment of the efficiency (and/or the power balance) of the modular multilevel based VSC unit. As discussed in section 2.2.1, the efficiency (i.e. internal losses) of a (MMC based) VSC unit is regulated through the utilization of a double frequency park's transformation for reducing the double frequency (harmonic) component in i_{cc}. Consequently, the HOVs utilized for the i_{HAM_x} current within i_{cc_x} (c.f. 5.1) must be considerably lower (at least five times) than the double frequency component associated with i_{hbal_x}. This HOV consideration is needed in order to reduce the influence of the introduction of the harmonic i_{HAM} current over the CCSC performance in the VSC unit avoiding in that way the efficiency detrimental of the VSC unit. Thus, the K and HOV parameters utilized to the HGS block are defined as presented in Table 5.1.

Table 5.1: HGS controller's parameters

Parameters	Units
K	1,25 pu
HOV_{under}	5 Hz
HOV_{over}	20 Hz

Finally, once the harmonic $v_{dc_{HAM}}$ signal is generated, it's transmitted to the DC_{Ctrl} to influence the DC voltage profile at the rectifier station (i.e. VSC A unit shown in Figure 5.2) based on the relationship shown in 5.4.

$$v_{dc_{ref}} = v_{dc_{nom}} + v_{dc_{HAM}} \tag{5.4}$$

As presented in 5.4, the HGS system essentially alters the reference of the DC voltage at the rectifier VSC unit of the non-embedded PtP-VSC-HVDC link inducing in that way, the flow of the harmonic i_{HAM} current into the HVDC cables shown in Figure 5.1.

5.1.2. Detecting the harmonic oscillatory signal

Once the harmonic i_{HAM} current flows through the HVDC cables of Figure 5.1, the modification of the active power reference at the inverter (P_{Ctrl} mode) VSC unit is carried out in two steps. The first step represents the detection (amplification) at the inverter unit of the introduced harmonic signal, and the second step is referred to the processing of the information contained within the harmonic signal. In the first step of the HDS, the methodology for detecting the harmonic signal within the HVDC cable is based on a control system specifically designed to amplify those harmonic signals generated by HGS. As shown in the upper side of Figure 5.3, the first section of the amplification loop of HDS is referred to the measurement of the DC voltage level (i.e. $V_{dc_{meas}}$) at the inverter (P_{Ctrl} mode) VSC unit presented in Figure 5.1.

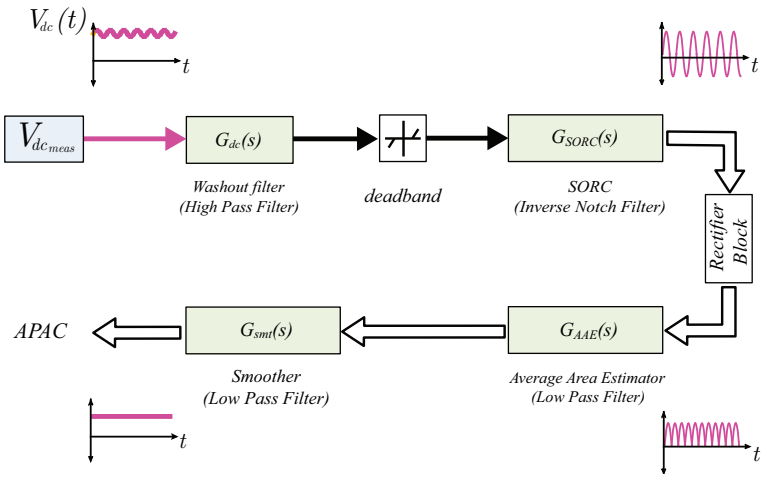

Figure 5.3: Harmonic Detection System (HDS) of Figure 5.1.

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Next, a high pass filter is utilized (i.e. $G_{dc}(s)$) to get rid of the constant component (associated with the DC voltage measurement), keeping in that way the harmonic content present in the measured signal. The structure of the $G_{dc}(s)$ block is based on a filter differentiator (a.k.a. washout filter) as presented in 5.5 and defined by the parameters K_{dc} and T_{dc}.

$$G_{dc}(s) = \frac{K_{dc}s}{1 + T_{dc}s} \tag{5.5}$$

Furthermore, the harmonic content (previously filtered by $G_{dc}(s)$) is then passed through a deadband block to reduce the undesired harmonic components present in the harmonic signal measured. This reduction is based on the assumption than the harmonic i_{HAM} current generates the highest harmonic voltage component measured by $V_{dc_{meas}}$ in Figure 5.3. Later, an additional block (i.e. G_{SORC}) is utilized to filter out the signal sent by the deadband block. Basically, the G_{SORC} block contains two inverse notch filters working as second-order resonant controllers which are set up to exclusively and individually amplify the HOVs generated by HGS as shown by the Bode Diagram in Figure 5.4. This means that the output of the G_{SORC} block represents a *signals' vector* having an individual loop (path) for each harmonic signal, i.e. one loop for the HOV_{under} signal and another loop for the HOV_{over} signal.

Moreover, the associated shapes of the curves of the G_{SORC} filters shown in Figure 5.4 are determined by the transfer function presented in 5.7 and characterized by the parameters K_{SORC}, α, β and ρ which are tuned based on the pole placement technique (to define the desired controller bandwidth), and based on time domain simulations (to verify the desired controller time response).

$$G_{SORC}(s) = \frac{K_{SORC}\rho s}{\alpha s^2 + \beta s + \rho^2} \tag{5.6}$$

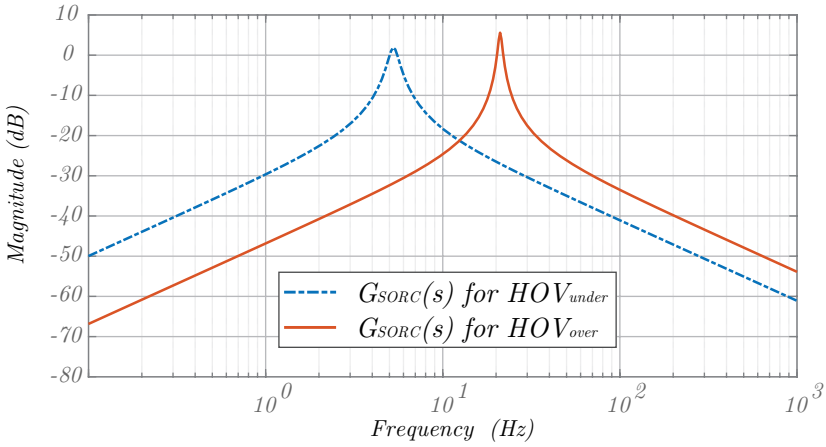

Figure 5.4: Bode analysis of the proposed $G_{SORC}(s)$ for two examples of HOV.

It is relevant to point out that the output signals given by $G_{SORC}(s)$ represent amplitude-modulated sinusoidal waveforms directly related to the frequency deviation occurring in network A as described in 5.3. Thus, the processing of the information of those output signals determines the active power adjustment command (i.e. APAC in Figure 5.3) to be sent to the P_{Ctrl} at the inverter (VSC B) unit shown in Figure 5.1. The methodology for processing the amplitude-modulated harmonic signals provided by $G_{SORC}(s)$ can be understood by considering the mathematical approach proposed by the Green Theorem. In short, the Green Theorem can be used to determine the area D of a parameterized (simple) closed curve $\overrightarrow{C(t)}$ (as shown in 5.7) when a vector field $\vec{F}$ (i.e. F_1 and F_2) is defined as $\vec{F} = (-\frac{y}{2}, \frac{x}{2})$.

$$Area(D) = \frac{1}{2}\oint_{C(t)} xdy - ydx \tag{5.7}$$

If one of the amplitude-modulated harmonic signals provided by $G_{SORC}(s)$ is utilized to define the components of the parameterized (simple) closed curve $\overrightarrow{C(t)}$, then, the processing of the information within the harmonic signal becomes an area determination problem as shown in 5.7. As an example, one of the components in 5.8 represents one of the output signals given by G_{SORC}, while the other component of $\overrightarrow{C(t)}$ represents the same signal $\frac{\pi}{2}$ phase shifted. Consequently, the $\overrightarrow{C(t)}$ shown in 5.8 will illustrate a circle with a radius depending on the frequency disturbance occurring at Network A in Figure 5.1 i.e. $\gamma\Delta f(t)$. Furthermore, the γ term in 5.8 represents the damping effect corresponding to the frequency-spectrum characteristics of the HVDC cable associated with the specific HOV introduced by the HGS.

$$\overrightarrow{C(t)} = \frac{\sqrt{2}}{2}\gamma\Delta f(t)(cos(2\pi HOVt), sin(2\pi HOVt)) \tag{5.8}$$

The equations 5.7 and 5.8 essentially point out that the computation of the area

associated with the output signals given by G_{SORC} can be utilized as a methodology for defining the APAC (c.f. Figure 5.3) generated by the HDS. Consequently, the development of a control system capable of providing a measure of the associated area of the output signals given by G_{SORC} is proposed as the second step of the HDS (i.e. the processing of the harmonic information).

In the second step of the HDS, a full-wave rectification system is applied to each of the outputs of G_{SORC} in order to develop the computation of its corresponding areas. This rectification system is designed by utilizing an absolute value operator presented as the *Rectifier Block* in Figure 5.3. Later, the full-wave rectified signal is passed through two consecutive low pass filters (i.e. $G_{AAE}(s)$ and $G_{smt}(s)$ in Figure 5.3) in order to generate the APAC (c.f. Figure 5.1). The low pass filters $G_{AAE}(s)$ and $G_{smt}(s)$ are characterized by the first order transfer function shown in 5.9 where the parameters K_i and T_i represent the proportional gain and the time constant utilized by each block to completely filter out the oscillatory components extracting in that way, the average value of the full-wave rectified signal.

$$G_{smt}(s) = G_{AAE}(s) = \frac{K_i}{T_i s + 1} \tag{5.9}$$

Next, the APAC (i.e. output of $G_{smt}(s)$) is sent to the P_{Ctrl} as shown in Figure 5.1 to modify the DC power flowing through the HVDC link. Here, it is convenient to highlight that APAC is a signals' vector having the areas' value of the harmonic signal HOV_{under} and the harmonic signal HOV_{over}. Consequently, the APAC can be understood as two individual signals (i.e. $APAC_{under}$ and $APAC_{over}$) generating the active power deviation when a frequency deviation occurs at Network A as defined in 5.10.

$$APAC = APAC_{over} - APAC_{under} \tag{5.10}$$

Please notice that it is not physically possible that the $APAC_{over}$ and the $APAC_{under}$ signals simultaneously exist since each of them reveal a different frequency deviation issue at Network A. On the other hand, and similarly to the HGS block, the adjustment of the parameters of the HDS block can be developed by carrying out a frequency domain (i.e. harmonic stability or selective modal) study or a time domain-based sensitivity analysis. For the sake of simplicity, the time domain-based sensitivity analysis was developed, and the parameter values obtained for the HDS block are presented in Table 5.2.

5.2. Extension of HAM for an embedded PtP-VSC-HVDC link

As mentioned in section 2.1 the AC networks can be connected through embedded or non-embedded PtP-VSC-HVDC links. Furthermore, section 5.1 presented a strategy for enabling the participation of non-embedded PtP-VSC-HVDC links (without using a dedicated communication (e.g. fiber optic) channel) to provide frequency

Table 5.2: Parameters of the second-order blocks of HDS

Transfer Functions	*First Order*			*Second Order*	
Parameters	$G_{dc}(s)$	$G_{AAE}(s)$	$G_{smth}(s)$	HOV_{under}	HOV_{over}
K	15000	0,02	0,1	0,16	0,09
ρ	N/A	N/A	N/A	31,42	125,66
α	N/A	N/A	N/A	0,9	0,9
β	N/A	N/A	N/A	4	6
T	0,02	0,05	0,05	N/A	N/A

support. On the other hand, it is also relevant to mention that synchronously coupled AC networks can sometimes suffer an extreme power unbalance producing a network split event (i.e. permanent loss of their synchronous coupling) as the ones registered in [10], and [11]. In this connection, this section develops a frequency support strategy for embedded PtP-VSC-HVDC links operating within AC networks having a network split (i.e. synchronous decoupling) event.

5.2.1. Coordination and adjustment of the active power

The strategy for developing the network support during frequency splits events is based on the addition of two (green) control blocks named Generic Frequency Control (GFC), and a synchronous Coupling Detector (SCD), to the strategy described in section 5.1, as illustrated in Figure 5.5. As shown in Figure 5.5, the frequency measurement of Network B (i.e. Δf_B) is developed by PLL_B and given to the GFC block which is based on the *generic frequency control scheme* (for PtP-VSC-HVDC links) presented in [12]. In short, the GFC will generate the adjustment of the active power level transmitted by the PtP-VSC-HVDC link based on Δf_B signal's value.

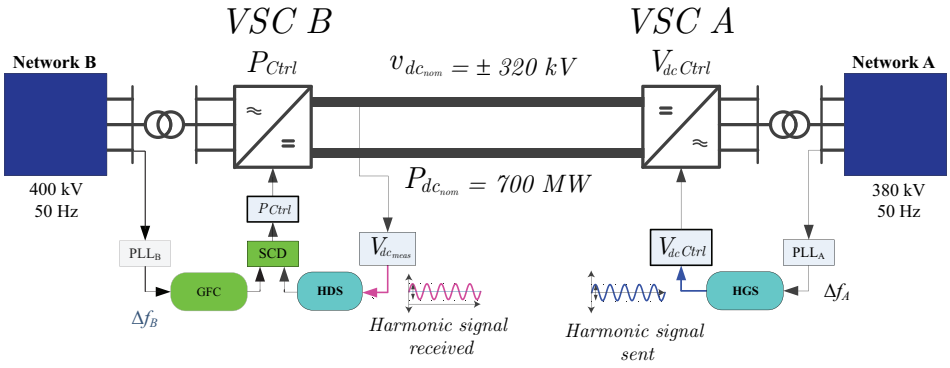

Figure 5.5: Embedded HVDC link including the proposed HAM control strategy (with SCD) based on the Harmonic Generation System (HGS) and the Harmonic Detection System (HDS) described in section 5.1.

It is relevant to mention that in an embedded PtP-VSC-HVDC link, Δf_A and Δf_B in Figure 5.5 are identical (during normal operation conditions) because of the syn-

chronous coupling existing between Network A and Network B. However, during an AC Network split event, it is expected that Δf_A and Δf_B are fundamentally different. Consequently, during an AC Network split event, the GFC block and the HDS block will simultaneously produce the corresponding signals for adjusting of the active power level of the PtP-VSC-HVDC link. Therefore, the Synchronous Coupling Detector (SCD) block presented in Figure 5.5 is introduced in order to generate the active power modification of the PtP-VSC-HVDC link based on the output signals provided by generic frequency control (GFC) block and the harmonic detection system (HDS) block. It is worth mentioning that if a power imbalance occurs within the AC network in which the PtP-VSC-HVDC link is embedded, the Δf_A and Δf_B can be different with respect to the case when the electrical nodes are electrically far away. Nevertheless, even in this circumstance, the SCD can help to mitigate such Δf differences by developing a comparative process.

Essentially, the SCD develops a comparative process between the output signals provided by the GFC and HDS blocks where all the possible states of Δf_A and Δf_B are shown in Table 5.3. It is important to mention that Table 5.3 is developed under the assumption that the DC power in the PtP-VSC-HVDC link (shown in Figure 5.5) always flows from the rectifier station (V_{dcCtrl}) to the inverter station (P_{Ctrl}).

Table 5.3: Truth table of the SCD block considering a Network Split Event in Figure 5.5

Variables & Cases	Possible States of Δf_A and Δf_B							
	A	B	C	D	E	F	G	H
Δf_A (HDS)	+	+	-	-	0	0	+	-
Δf_B (GFC)	+	-	+	-	+	-	0	0
ΔP	0	↑	↓	0	↓	↑	↑	↓

In Table 5.3, the phrase *"Possible States of* Δf_A *and* Δf_B*"* is referred to the conditions associated to the electrical frequency measured at each AC Network in Figure 5.5. In Table 5.3, symbol "+" indicates an *over-frequency* issue, symbol "-" indicates an *under-frequency* issue, and symbol "0" indicates no frequency deviation registered. Moreover, the active power adjustment ΔP (processed by SCD) will depend on the particular case shown in Table 5.3 and will be expressed as either an increment "↑", or a reduction "↓" of the DC power transmitted by the PtP-VSC-HVDC link. For instance, in Table 5.3, Cases *A* and D, represent conditions where the AC Networks in Figure 5.5 are affected by a power unbalance leading to a common over-frequency or under-frequency issue respectively. In these cases, the SCD will not execute any modification of the DC power flow transmitted by the PtP-VSC-HVDC link since it assumes that both AC networks (c.f Figure 5.5) are still synchronously coupled. On the other hand, Cases *B* and C represent conditions where the AC Networks in Figure 5.5 experience a power unbalance generating a simultaneous under-frequency issue in one AC network, and an over-frequency issue in the other AC network. These conditions (i.e. Cases *B* and C) are interpreted by the SCD as a loss of the synchronous coupling between Network A and Network

B, and will consequently lead to a modification of the DC power transmitted by the PtP-VSC-HVDC link. It is interesting to notice that if the first four Cases presented in Table 5.3, are analyzed using a methodology based on digital logic, the implementation required to obtain the corresponding ΔP output can be easily obtained by using a XOR gate.

Furthermore, Cases *E, F, G,* and H are referred to conditions where the AC Networks in Figure 5.5 experience a power unbalance where only one of the AC networks connected to the PtP-VSC-HVDC link results affected. These particular conditions can occur if the inertia levels in one of the corresponding AC Network are sufficiently robust to handle the power unbalance while insufficient in the other AC Network. However, the frequency deviations measurements obtained from the last European AC Network split events reported in [10] and [11], indicate that the Cases *E, F, G,* and H are not the main area of concern during AC Network splits events, specially in AC networks where the integration of power electronics interfaced generators units is progressively increasing. Therefore, the simulation experiments carried out in this chapter are selected based on the first four Cases defined in Table 5.3.

5.3. Simulations setup and results

5.3.1. Systems and Scenarios Description

The numerical simulation experiments developed in this chapter have been carried out in a quasi-stationary (or RMS simulation) time frame in DIgSILENT PowerFactory 2019. Moreover, the PtP-VSC-HVDC link is implemented based on the regulations schemes described in section 2.2.2, and additionally, the implemented AC network corresponds with the synthetic power system model described in [13]. In short, the synthetic power system model shown in Figure 5.6, constitutes a reduced representation of the Danish, the Dutch and the German AC networks in which a 700 MW PtP-VSC-HVDC link is utilized for connecting the north part of the Dutch high voltage AC network, with the south-west part of the Danish high voltage AC network as illustrated in Figure 5.6. Additionally, it is established that for all the simulations experiments carried out in this chapter, the PtP-VSC-HVDC link will be transmitting 350MW to the Danish AC network, this entails that the rectifier and the inverter stations of the HVDC link are located in the Dutch and the Danish AC networks respectively.

Furthermore, the synthetic power system model shown in Figure 5.6 has been selected since it can be used to recreate an electromagnetic decoupling (i.e. AC network splitting) event, such as the one reported by [10], when the (red) transmission lines highlighted in Figure 5.6 get disconnected. On the other hand, this synthetic power system model can also allow the performance's analysis of the HAM strategy under a severe power unbalance (i.e power plant outage in DE) affecting the frequency response of all the synchronously coupled AC networks. Thus, these two power unbalance events (i.e. Ac network split and the power plant outage) are

utilized for the analysis of the proposed HAM strategy in the embedded PtP-VSC-HVDC link shown in Figure 5.6.

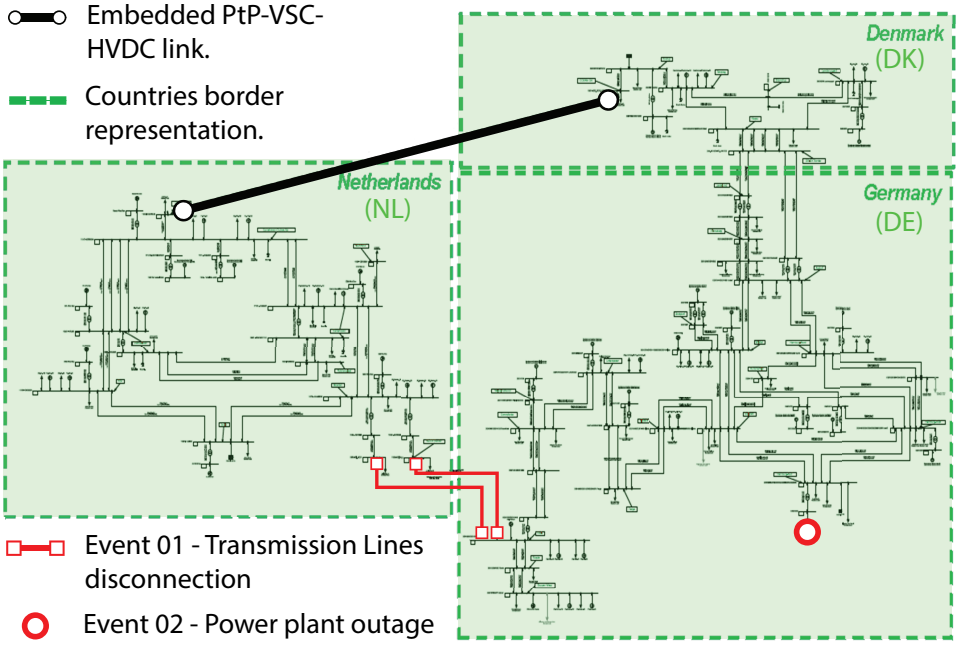

Figure 5.6: A PtP-VSC-HVSC link embedded in the synchronously coupled synthetic power system model described in [13].

First of all, the disconnection of the (red) transmission lines (i.e. first event) will entail a loss of 760MW imported from the German (DE) Network to the Dutch (NL) Network, leading to a drop of the electrical frequency in the isolated NL power system. In this connection, as the synthetic power system model shown in Figure 5.6 only considers a partial section of the Dutch transmission network [13], the inertial response of the modelled Dutch AC network is limited to the generator units present in Figure 5.6. Thus, in order to assess the frequency support provided by PtP-VSC-HVDC link (using the HAM strategy) during the AC network split event, three scenarios (SC01, SC02, & SC03) are proposed. The SC01 demonstrates the natural inertial and primary frequency response of the AC networks when the disconnection of the (red) transmission lines in Figure 5.6 take place. The SC02 demonstrates the level of frequency support provided by the HAM strategy when 350MW are received by the Danish network through the PtP-VSC-HVDC link which utilizes 1GW / min as active power gradient (APG) setup. Last, the SC03 scenario is almost identical to SC02 except for the fact that the associated (APG) has been increased to 10GW/min.

Secondly, the simulation experiment regarding the second power unbalance event (i.e. second event) is developed by disconnecting a generation power plant

in the German network supplying 1500MW while the DC power transmission in the PtP-VSC-HVDC link is identical to the scenarios SC02 and SC03. The loss of this power generation will induce a drop on the electrical frequency of the synchronously coupled AC networks In Figure 5.6 which will be measured by the PtP-VSC-HVDC link through the PLL_A and PLL_B blocks as shown in Figure 5.5.

5.3.2. Event 01: AC network split

The simulation results regarding the scenarios SC1, SC2, and SC3 (described in section 5.3.1), starts by disconnecting the (red) transmission lines at t = 10 s. Furthermore, the analysis of the HAM strategy considers the response of the PtP-VSC-HVDC link and the AC networks in terms of the DC voltage profiles, the electrical frequencies Δf, and the DC (active) power provided by the link, (during the disconnection of the transmission lines) as shown in Figure 5.7 and Figure 5.8. As shown in Figure 5.7, it can be seen that, the DC voltage profile of the HVDC network is not affected in the scenario SC1 (i.e. Figure 5.7a) and consequently, the active (DC) power transferred through the PtP-VSC-HVDC link is not modified (as shown by the thicker dashed lines illustrated in Figure 5.8a) during the disconnection of the (red) transmission lines in Figure 5.6. Likewise, as the active power in the PtP-VSC-HVDC remains unchanged, the frequency responses associated with SC1 (expressed by the thicker dashed lines in Figure 5.8), present the largest steady-state frequency deviations (50,6 Hz and 49 Hz in Figure 5.8b) and the most pronounced frequency nadir (47,8 Hz) in the Dutch network.

For the second scenario (SC2), two differences w.r.t. SC1 can be highlighted. The first difference is the introduction of the harmonic signal (i.e. activation of the HAM strategy) which produces a non-linear modification of the DC voltage level of both VSC units as presented in Figure 5.7. The second difference is the setting of the APG parameter to 1 GW/min [14]. These two differences essentially determine the active power response in the HVDC link as illustrated by the thin dashed lines shown in Figure 5.8a, where the active power level is reduced to 230 MW from its initial 350 MW steady-state level. This helps to slightly enhance the steady-state frequency deviations obtained when comparing against the SC1 shown in Figure 5.8b. Additionally, it can be seen that the resulting Nadir value in the Dutch network is slightly improved (as shown by the thin dashed lines in Figure 5.8b) when compared against the SC1's Nadir value obtained. However, the selection of the typical limit value for the APG (i.e. 1GW/min) generates a lineal active power deployment during the transmission lines' disconnection, which delays the frequency support provided by the HVDC link. This causes a reduction of the active power until -200 MW within the first 15 seconds after the transmission lines get disconnected in the AC network (cf. thin dashed lines in Figure 5.8a). Fortunately, this delay on the frequency support provided by the HVDC link can be reduced if the P_{Ctrl} is adjusted to use emergency power control settings (i.e. increase the APG limit value) like the ones indicated in [14].

Hence, for the third scenario (SC3), the APG set-point has been further increased

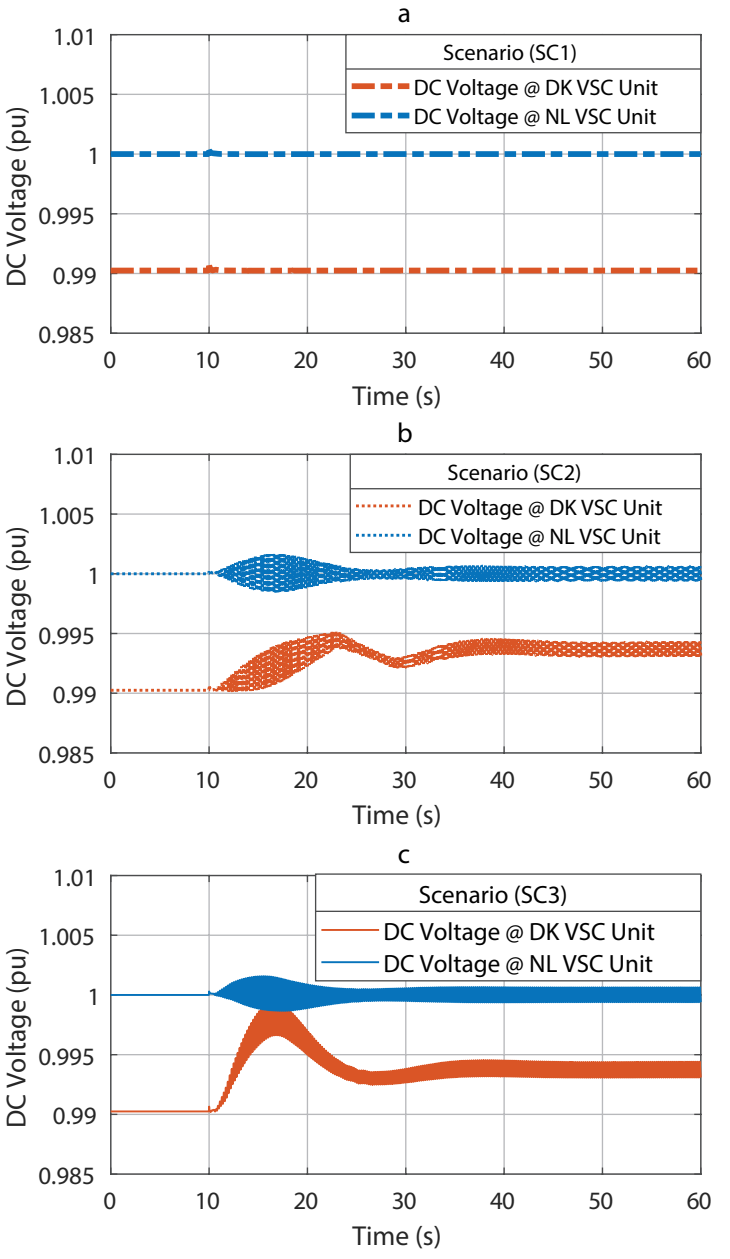

Figure 5.7: DC voltage responses of the embedded point-to-point VSC-HVDC link associated to the Event 01 shown in Figure 5.6 considering a) the scenario 01 (SC1), b) the scenario 02 (SC2), and c) the scenario (SC3).

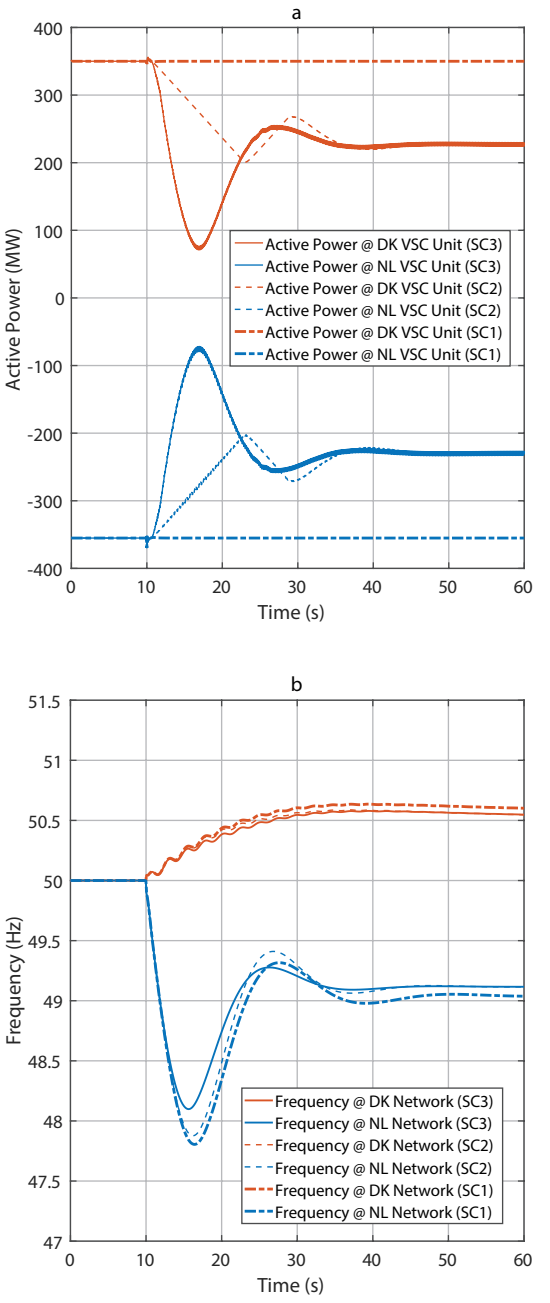

Figure 5.8: a) Active power responses for each of the DC voltage responses shown in Figure 5.7. b) frequencies responses measured at each VSC-HVDC unit for each of the DC voltage shown in Figure 5.7.

to 10 GW/min for examining the effects of accelerating the deployment of the active power when the HAM control is utilized when an AC network split (i.e. emergency or extreme) event occurs in the AC network. The increment of the APG set-point for SC3 allows to generate a more pronounced reduction of the active power (until -78MW) within the first 15 seconds after the transmission lines' disconnection occurs as shown by the solid lines presented in Figure 5.8a. Likewise, the increment in the APG set-point allows accelerating the active power deployment generated by the HAM strategy, reducing in that way the nadir level obtained in the Dutch network for the SC3 in a more significant way than the reduction obtained in SC2 as shown in Figure 5.8b.

During the steady-state period achieved after the fault, the active power (i.e. Figure 5.8a) and DC voltage responses (i.e. Figure 5.7b and Figure 5.7c) obtained are identical. This effect occurs since the harmonic amplitude presented (8) remains constant because the Δf stabilizes at the same level during the steady-state period after the disturbance occurs (i.e. Figure 5.8b). On the other hand, due to the superior performance observed in terms of the Nadir level obtained by SC3, it is worth pointing out that having an APG set-point of 10 GW/min allows achieving the best mitigation of the maximum frequency deviation experienced during an extreme contingency by using the HAM strategy.

5.3.3. Event 02: Power plant outage

Similar to section 5.3.2, the simulation results regarding the power plant outage event (described in section 5.3.1), starts by disconnecting the power plant shown in Figure 5.6 at t = 10s. Furthermore, the performance of the HAM strategy is studied here by considering the DC voltage profiles, the electrical frequencies Δf (measured by each PLL block in Figure 5.5), and the transmitted active power between the Dutch and the Danish AC networks.

In this connection, Figure 5.9a indicates that during the power plant outage event, an identical drop in the electrical frequency is observed as a consequence of the existing synchronous coupling between the German, the Dutch, and the Danish AC networks. Furthermore, it is also noticed Figure 5.9 that during the first seconds of the frequency drop, the DC power and the DC voltage of the PtP-VSC-HVDC link are slightly modified for a short period of time. This slight modification of the active power occurs due to the time needed for generating the output signal of the GFC block and the time needed for generating the output signal of the HDS block shown in Figure 5.5. Namely, as the output signal of the HDS block depends on the output signal of the HGS block, the GFC's output signal arrives comparatively faster to the SCD block w.r.t. the output signal of the HDS block. Therefore, at the beginning of the power plant event, the SCD detects an under-frequency problem in Δf_B (i.e. Danish AC network) and proceed to increment the active power transmitted by the HVDC link as shown in Case F of Table 5.3. Later, the HDS signals arrives indicating an under-frequency problem in Δf_A (i.e. Dutch AC network) creating in that way a change in the operation of the SCD block from Case F to Case D and consequently,

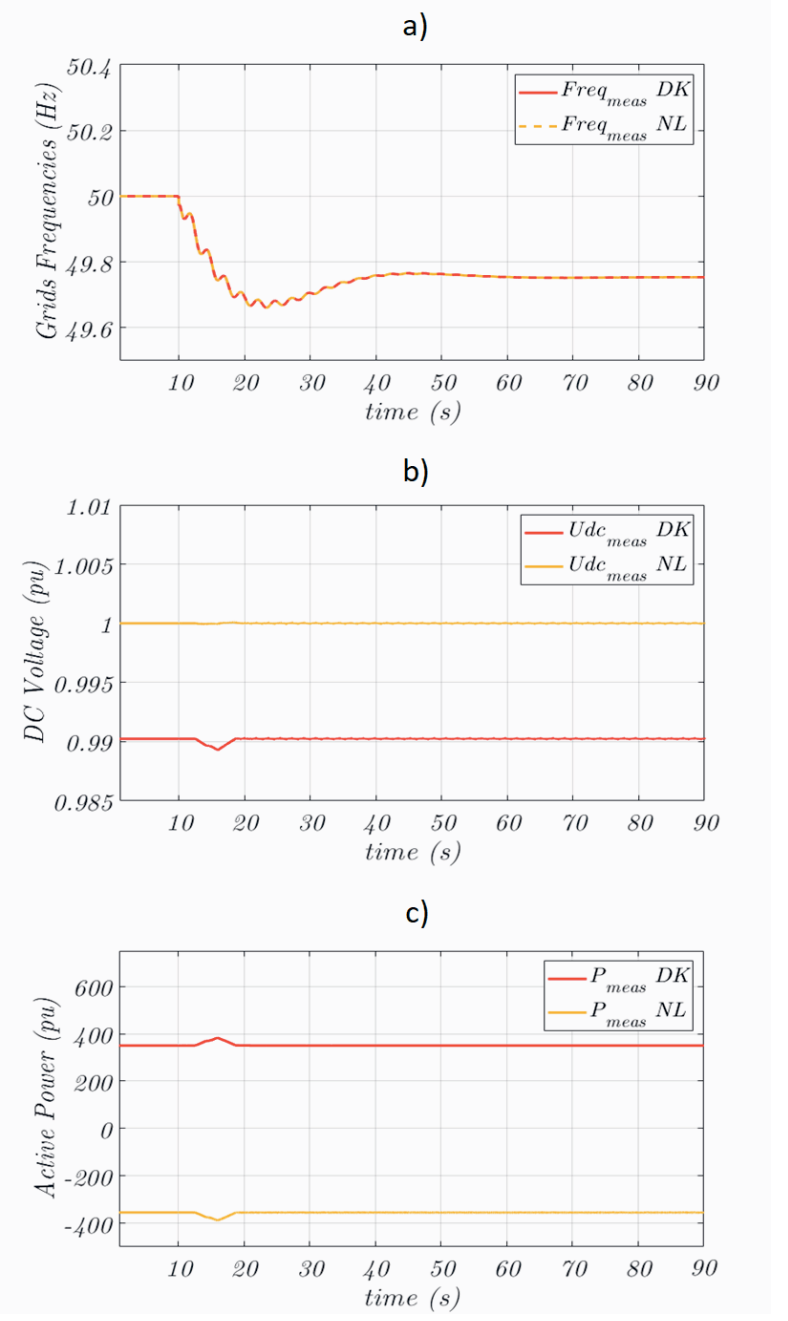

Figure 5.9: Results associated to the Event 02 shown in Figure 5.6. a) Frequencies responses b) DC voltage response and, c) active power response of the VSC-HVDC units of the point-to-point link.

the modification of active power (initiated by the GFC output signal) disappears.

5.4. Conclusions

In this chapter, a frequency support method by PtP-VSC-HVDC links was presented, based on the generation of a harmonic amplitude modulation (HAM) strategy. The proposed HAM strategy is integrated in the active power and DC voltage control schemes of a modular multilevel technology based PtP-VSC-HVDC link. Fundamentally, the introduction of the harmonic signal within the HVDC link represents an additional zero-sequence component included in the circulating current of the VSC unit, and it does not compromise the operation of the PtP-VSC-HVDC link. Numerical simulations were performed to evaluate the effects of the HAM control on the frequency support provided by an embedded PtP-VSC-HVDC link during two severe events, an AC network split and a power plant outage.

It was shown that by using the proposed control schemes i.e. harmonic generation system (HGS), the harmonic detection system (HDS) and the synchronous coupling detector (SCD), the HAM control can effectively perform the transmission and the reception of the required active power adjustment command (APAC) based on the frequency deviations of the affected AC networks. For most of the conducted numerical simulations, it was found that the HAM control contributes to improve the Nadir and the steady-state frequency response levels obtained after an AC network split event occurs in the power system. On the other hand, it was shown that during a power plant outage event, the HAM strategy helps to keep unchanged the active power transmission levels in an embedded PtP-VSC-HVDC link allowing in that way the deployment of the inherent inertial and primary frequency resources of the affected power system. On the other hand, it was also found that the active power gradient (APG) settings of the HVDC link (i.e. active power ramp-rate settings) also influence the level of support provided by the HAM control. This analysis was developed by comparing the performance of the HAM control under different APG conditions.

The results obtained suggest that the selection of sufficiently separated HOVs, guarantee an adequate operation of the second order resonant controllers used in the HDS. Otherwise, it will be necessary to reduce even further the considered bandwidth. This could be done by using a more sophisticated filter strategy. Based on the simulation results obtained, it is also recommended to select HOVs lower (at least five times less) than the main harmonic component of the circulating current, to avoid in that way a detrimental of the dynamic performance regarding the internal energy control of the VSC unit. Finally, future research shall also be devoted to investigate the performance of the HAM control when applied in multi-terminal VSC-HVDC networks analyzed under an electromagnetic-transients (EMT) simulation environment.

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6

Methods for Post-Fault Active Power Recovery in VSC-HVDC links

In this chapter an exponential function-based DC voltage control is proposed for regulating the post-fault active power recovery (PFAPR) process in a VSC-HVDC link. The proposed control is effective to prevent a DC voltage collapse during the activation of the fault ride-through function, while ensuring the compliance of the PFAPR requirements. Additionally, the effectiveness of this control is tested in an expandable VSC-HVDC link, considering its operation as a point-to-point or a multi-terminal VSC-HVDC network. The tests also consider the application of droop or constant DC voltage control, and the need of coordination when a DC chopper is required under significant DC power imbalances.

6.1. PFAPR requirements for VSC-HVDC links

The regulation of the active power during post-fault conditions at the AC network has been defined by transmission system operators, as one of the fundamental requirements that modern VSC-HVDC links must comply [1]. Typically, this active power regulation process is referred as the *post-fault active power recovery* (PFAPR) function, and it is characterized by two main aspects. The first aspect concerns with the time period in which the pre-fault active power level is expected to be restored, and the second aspect concerns with the AC voltage level in which the active power is expected to be restored [2].

Figure 6.1 shows two different responses (represented by the green and blue dashed lines, respectively) concerning with the active power evolution of the VSC-HVDC unit before, during and after an AC fault occurs. As an example, a VSC-HVDC unit transmits 300MW during steady-state operation (i.e., Δt_0) as shown in Figure 6.1. Next, a three-phase fault to ground event occurs at its AC terminals, and the resulting (RMS) AC voltage drop is observed during the Δt_1 period, as shown in Figure 6.1.

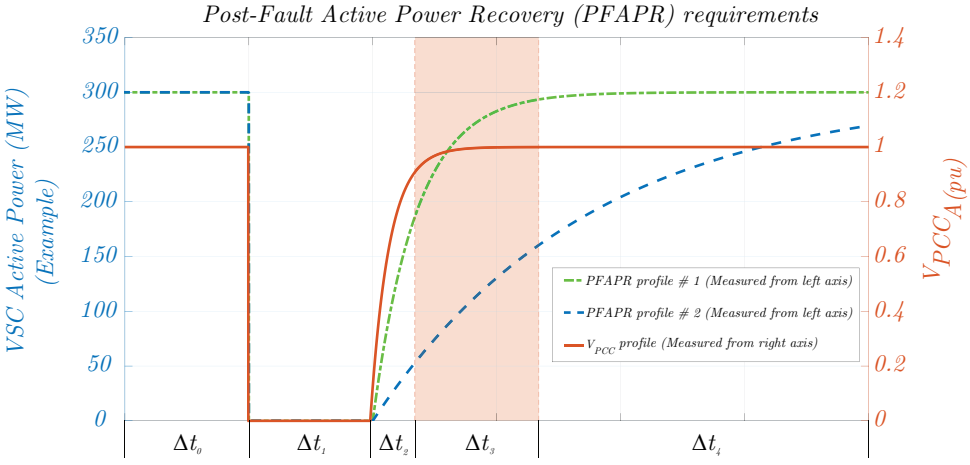

Figure 6.1: The active power and V_{PCC} voltage responses of a VSC-HVDC unit (during a fault condition) transmitting 300MW. The evolution of the fault event is divided by the pre-fault (Δt_0), fault (Δt_1),and post-fault (Δt_2, Δt_3, Δt_4) time periods. The activation of the FRT function occurs at beginning of Δt_1, and its deactivation occurs at the end of Δt_2 period. In this example, 90 % of the pre-fault active power condition of PFAPR #1 is restored within the time window defined by Δt_3 complying with the PFAPR requirement. Conversely, The PFAPR #2 does not comply with the PFAPR requirement. Typically, Δt_3 = 200ms as indicated in [2].

Note that five different time periods are shown in Figure 6.1: i) the time period Δt_0 where the pre-fault conditions are presented, ii) the time period Δt_1 associated with the fault duration, iii) the time period Δt_2 in which 90% of the pre-fault AC voltage level is achieved, iv) the time period Δt_3 in which at least 90% of the pre-

fault active power level is restored, and v) the time period Δt_4 in which the active power should be restored.Note also in Figure 6.1 that the active power response represented by the blue-dashed line is not properly restored within the time period associated with Δt_3. By contrast, the active power response represented by the green-dashed line is restored within the time period defined by Δt_3, complying in that way with the PFAPR demands indicated in [2].

6.2. Structure of the PFAPR Analysis for Expandable VSC-HVDC links

As described in section 2.3.3, an expandable PtP-VSC-HVDC link must be capable of operating under a point-to-point or a multi-terminal network configuration. The control design process for the PFAPR regulation is explained considering each of these two network configurations in sections 6.3 and 6.4, respectively. The structure of the performed PFAPR analysis is summarized in Table 6.1.

Table 6.1: Structure of the PFAPR analysis for the expandable VSC-HVDC links analyzed in this dissertation

VSC-HVDC link Operation	Fault Location at	Associated Issues	Proposal	Key take away
Point-to-Point (DC Voltage Control & P Control)	AC network connected Rectifier Station (Controlling DC Voltage)	DC Voltage Collapse and Ineffective PFAPR	Exponential function-based DC Voltage control (c.f. section 6.3.2)	(1) Non-linear based DC voltage support method can stabilize the DC voltage within safe limits without the need of an active communication channel between the converter stations.
	AC network connected Inverter Station (Controlling DC Voltage)	Ineffective PFAPR under high impedance fault conditions	Enhanced Active Power Control (c.f. section 3.4.2)	(2) Enhanced Active Power Control capable of restoring the active power level in less than 200ms without abrupt change in the active power during the PFAPR period.

Continued on next page

Table 6.1: Structure of the PFAPR analysis for the expandable VSC-HVDC links analyzed in this dissertation (Continued)

Multi-terminal (Droop Control at Onshore Stations)	AC network connected to one of the Onshore Stations	Droop control unable of effectively processing PFAPR	Adapting the non-linear based DC voltage support method for MTDC operation	(3) The multi-terminal DC grid controller can perform the PFAPR process by utilizing the memorized Pre-fault levels of the Active Power and DC Voltage of the affected VSC unit without the need of an active communication channel between the converter stations. (4) The use of the adapted non-linear-based DC voltage support method is better for regulating the PFAPR process when compared to the classic Droop control method.
		Abrupt power transfer increase towards any onshore VSC unit due to FRT activation	Dynamically Adjustable Chopper Impedance (DACI)	(5) The use of DACI allows to mitigate the sudden change in the DC power across the MTDC network up to a 90% and to prevent undesirable harmonic distortion introduced by conventional DC choppers during their operation within a MTDC network.

Continued on next page

Table 6.1: Structure of the PFAPR analysis for the expandable VSC-HVDC links analyzed in this dissertation (Continued)

Multi-terminal (DC Voltage Control & P Control at Onshore Stations)	AC network connected to Inverter Station (Controlling P)	Abrupt power transfer at Rectifier station		DACI	c.f. (5) above
	AC network connected to Rectifier Station (Controlling DC Voltage)	Depending on the Active Power Level provided by Offshore Station	(a) if supplied OWF Power is > Inverter Power Demand: DC overvoltage risk and ineffective PFAPR	DACI	c.f. (5) above
			(b) if supplied OWF Power is < Inverter Power Demand: DC voltage collapse and ineffective PFAPR	Enhanced Active Power Control (c.f. section 3.4.2)	c.f. (2) above

6.3. PFAPR during Point-to-Point Operation

6.3.1. Power Flow Characterization

The analysis of the PFAPR process starts by defining the power flow characteristics concerning the studied point-to-point VSC-HVDC link. As shown in Figure 6.2 a point-to-point VSC-HVDC link can be used to transmit active power between two AC networks (c.f. section 2.1). In an onshore-to-onshore, point-to-point VSC-HVDC link, the active power can be transmitted from Onshore Network A towards Onshore Network B, or vice versa. On the other hand, a point-to-point VSC-HVDC link can also be utilized to transmit active power between an Offshore AC Network and an Onshore AC Network as shown in Figure 6.3. Unlike the onshore-to-onshore case, the offshore-to-onshore, point-to-point VSC-HVDC link, the active power can only be transmitted (during steady-state operation) from Offshore Network towards the Onshore Network A shown in Figure 6.3.

If the active power can only be transmitted in one direction, and there is an event that blocks the capabilities of *VSC A* unit for transferring active power towards the

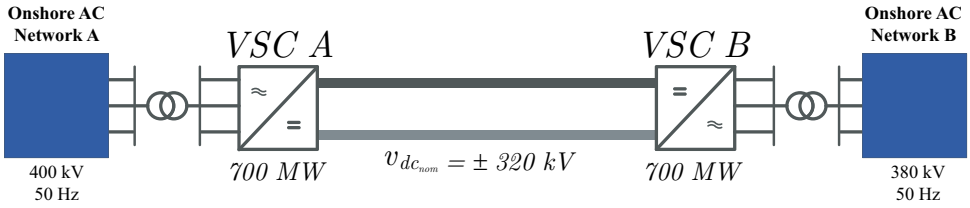

Figure 6.2: Expandable PtP-VSC-HVDC link interconnecting two onshore AC networks. Here, the active power can be transmitted between the Onshore AC Networks in both directions (i.e. from *VSC A* unit towards *VSC B* unit, or vice versa).

Onshore Network A, the HVDC link will experience a DC voltage rise. The DC voltage rise will occur since the Offshore Network supplies power into the point-to-point HVDC link during the blocking event increasing in that way the electrostatic energy of the HVDC cables. Consequently, the DC Chopper (shown in red in Figure 6.3) is typically included in this type of offshore-to-onshore, point-to-point VSC-HVDC links.

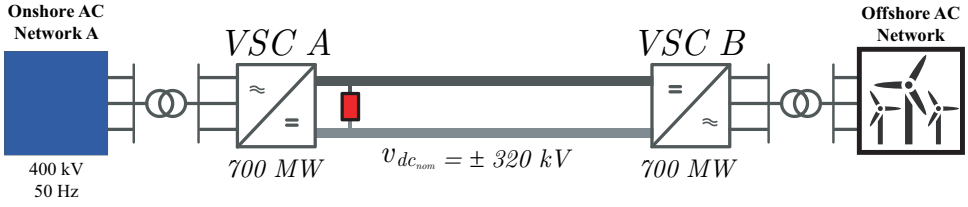

Figure 6.3: Expandable PtP-VSC-HVDC link interconnecting one Offshore AC Network with an Onshore AC Network. Here, a DC Chopper (red box) is usually included to reduce the DC over-voltages experienced by the HVDC link when the active power cannot be transmitted towards the Onshore Network A by *VSC A* unit.

The DC Chopper is designed by the HVDC manufacturers to temporarily dissipate the power supplied by the Offshore Network, while *VSC A* attempts to restore its AC/DC power balance. The dissipation of the power is carried out by regulating the insertion and extraction of a resistor within the HVDC network, without violating its thermal limits. The potential use of the power dissipation capabilities of the DC Chopper during the multi-terminal expansion of a point-to-point VSC-HVDC link (within the PFAPR context) is discussed in section 6.4.3.

6.3.2. AC Network Fault at the Rectifier Station (Onshore-to-Onshore HVDC link)

The PFAPR process is studied in this section by considering a three-phase fault event occurring at the AC network side of either the inverter or the rectifier unit of an (Onshore-to-Onshore) Point-to-Point VSC-HVDC link. In this regard, Figure 6.4 shows a point-to-point VSC-HVDC link in which the DC power is transmitted from the rectifier unit *VSC A*, towards the inverter unit *VSC B*. Next, Figure 6.4 also indicates the presence of a fault at V_{PCC_A} bus which will affect the power balance

at *VSC A* unit.

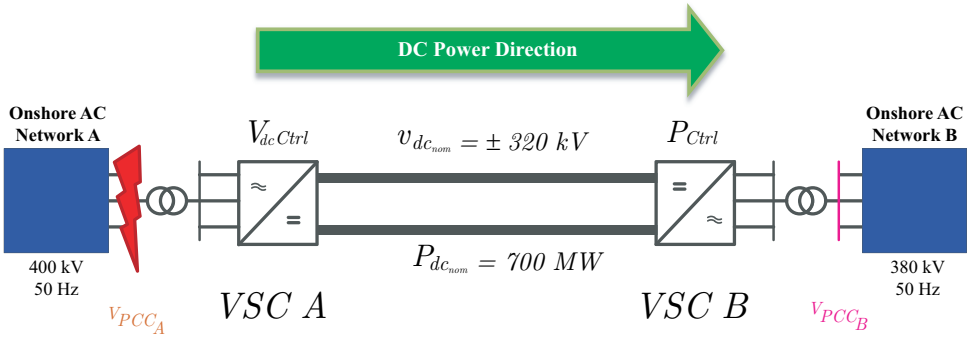

Figure 6.4: Expandable (Onshore-to-Onshore) PtP-VSC-HVDC link (under steady-state point-to-point operation) experiencing a sudden three phase fault at V_{PCC_A}.

As indicated in section 3.4.1, the voltage drop at the AC network A (i.e., fault at V_{PCC_A} bus), will lead to the activation of the FRT control function at the rectifier *VSC A* unit. This activation will modify the priority level given to the active and the reactive currents of *VSC A*, jeopardizing in that way the regulation process of the DC voltage during the fault event at AC network A. At this point, it can be inferred from Figure 6.4 that if the DC voltage regulation is blocked in *VSC A* unit, and the inverter *VSC B* unit keeps subtracting power from the point-to-point network, the DC voltage level across the entire link will start to drop. Consequently, if the DC voltage level drops beyond its low limit value (i.e. a DC voltage collapse), then, the VSC-HVDC link will no longer be able to develop the PFAPR process in case the fault at the AC network A is cleared.

Typically, for this type of fault condition, a communication interface detects the blocking condition of *VSC A*, and then, a reduction of the active power level demanded by *VSC B* is developed to avoid the DC voltage collapse across the link. The dependency between the active power reduction and the DC voltage level is called the *voltage-margin method*, and it has been already implemented and tested in some HVDC projects [3]. As discussed in [3], the *voltage-margin method* can provide benefits for multi-terminal HVDC applications. However, its actual implementation is based on a control structure where the operation of several limiters and switching control blocks must be carefully coordinated.

On the other hand, if the communication interface is not available during the blocking of *VSC A*, then a more sophisticated active power reduction strategy must be designed. Until now, most of the active power reduction strategies within the *voltage-margin method*, have been developed by using a complex arrangement of frequency domain controllers that follow piecewise linear characteristics through the modification of their corresponding inner state variables [4]. However, unlike

the complex arrangement of frequency domain controllers presented in the current literature, the proposed active power reduction strategy proposed in this dissertation is based on a simple non-linear active current modulation. This active current modulation will essentially generate a non-linear DC voltage support whose rationale is explained at the end of this section.

The non-linear active current modulation is implemented at the inverter unit shown in Figure 6.4, and it essentially generates a dependency between the amount of DC power subtracted by *VSC B*, and the voltage level at its DC terminals based on the expressions 6.1 and 6.2.

$$i^*_{gD} = \lambda_{MOD} \cdot i^*_{gD_P} \tag{6.1}$$

$$\lambda_{MOD} = 1 - e^{-\alpha(DC_{meas} - LVT)} \tag{6.2}$$

The signal i^*_{gD} represents the input to the *Inner Control* block which is generated through the non-linear modulation of the active current reference (i.e. $i^*_{gD_P}$) generated by the active power controller (i.e., P_{Ctrl}) of *VSC B*. The non-linear modulation is developed through the term λ_{MOD}, and a visual representation of its influence over the control systems of *VSC B* is provided in Figure 6.5.

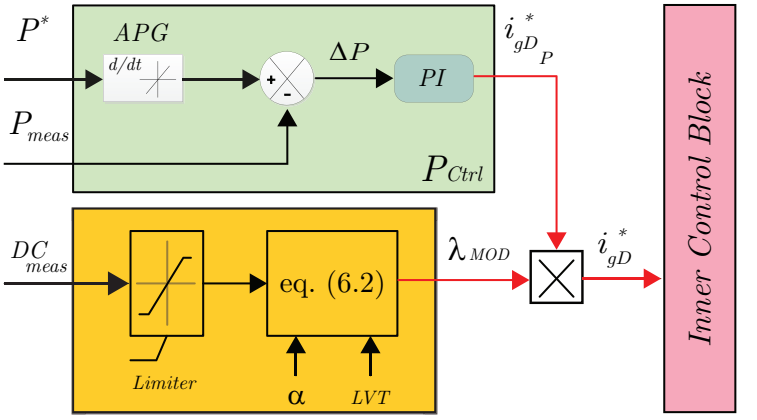

Figure 6.5: Graphical description of the proposed non-linear modulation method. Here, it is shown that the modulation action essentially modifies the output of the $PCtrl$ block which represents the input of the *Inner Control* block (as illustrated in Figure 2.9).

The expression 6.2 shows that the term λ_{MOD} consists of an exponential function which depends on the DC voltage level measured (DC_{meas}) at the DC terminals of *VSC B*, a constant low voltage threshold (*LVT*), and the gain α. The parameter *LVT* of 6.2 represents the constant value defining the *minimum steady-state DC voltage level* in which a converter unit is expected to operate without saturating its modulation index. For example, a *LVT* = 0.97pu is referred to a VSC-HVDC unit capable of

operating 3% below its nominal DC voltage value, during steady-state conditions. Next, it can be seen in 6.2 that the difference between the DC_{meas} and the *LVT* constant is amplified by the term $alpha$. This amplification term is used to control the rate of change of the term λ_{MOD}, when the DC voltage level at the DC terminals of *VSC B* (i.e., DC_{meas}) gets close to the *LVT* constant value as presented in Figure 6.6.

It is very important to notice that if the difference between the DC_{meas} and the *LVT* becomes negative, the λ_{MOD} term will also become negative (c.f. 6.2). The change in the λ_{MOD} term sign will induce an active power reversal event at *VSC B* that will help to boost the DC voltage during the blocking period of *VSC A* unit. Thus, the difference between the DC_{meas} and the *LVT* needs to be controlled by limiting the DC_{meas} level that can be used by the expression 6.2. This limitation is developed by introducing a limiter block (as shown in Figure 6.5). The calibration of the *low limit* value of the limiter block will depend on the desired level of active power reversal during the blocking period of the rectifier *VSC A* unit. For example, if during the blocking period of *VSC A*, the maximum level of active power reversal is setup to 50%, then, a *low limit* value of 0.9698pu can be used, when the *LVT* is equal to 0.97pu, and the α gain is equal to 2000.

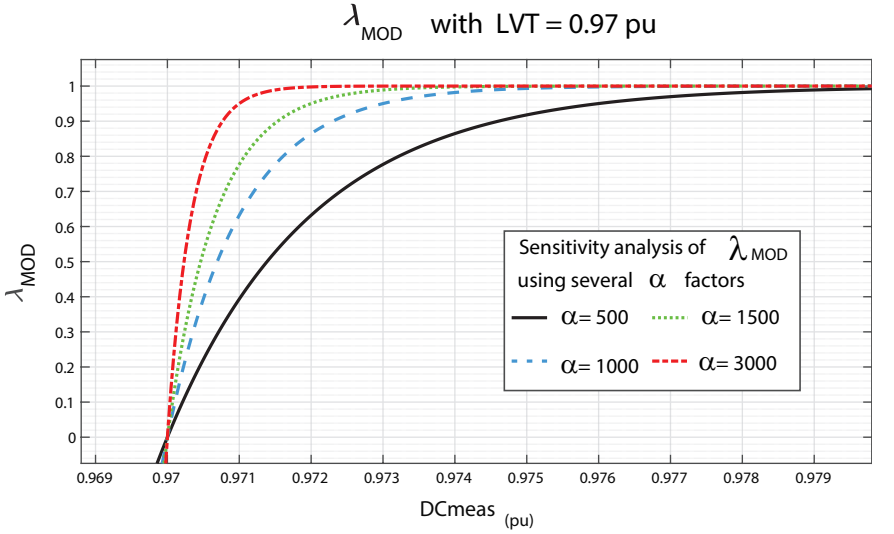

Figure 6.6: Non-linear dependency (c.f. relationship 6.2) between λ_{MOD} and the DC voltage level at VSC B unit showing different α values. Notice that the assumed LVT value is 0.97 and the λ_{MOD} becomes negative when the $DC_{meas_{LIM}}$ value is lower than LVT.

The fast active power reduction during a critical DC voltage drop is a desirable characteristic for supporting the DC voltage profile of the HVDC link shown in Figure 6.4. Nevertheless, the consequences of using higher α values (e.g. above 3000) in a real power electronic converter application would require the use of real-time processors able to compute the non-linear function λ_{MOD} in a time frame smaller

than 1 ms. Besides, the use of lower α values (e.g. below 500) is not recommended since its decrement can seriously affect the performance of the PtP-VSC-HVDC system during its steady-state operation.

It is worth pointing out that the development of the non-linear DC voltage support method (provided by *VSC B*) is a fundamental step to enable the PFAPR process by the *VSC A* unit. Consequently, once the electrical fault has been cleared, and the AC voltage at V_{PCC_A} level starts to recover, there will be a change in the prioritisation of the active and reactive current at the rectifier station *VSC A*. Consequently, the *VSC A* unit will start to progressively restore the DC voltage level across the HVDC link increasing the DC_{meas} value used 6.2. Thus, it is ensured that the non-linear DC voltage support provided by the *VSC B* unit will not interfere with the DC voltage boosting process developed by the *VSC A* unit. Instead, it will progressively restore the demand of active power (i.e. PFAPR) accordingly to the DC voltage profile evolution based on 6.2.

Rationale behind the non-linear DC Voltage support

The rationale behind the non-linear mathematical expression shown in 6.2 has been inspired based on the need of adjusting the level of active power demanded by the inverter VSC unit of a point-to-point HVDC link during an AC side fault in the rectifier VSC unit. In steady-state conditions, the modulation of the active power does not occur. However, the modulation of the active power should start as soon as the DC voltage drops below a defined LVT value (i.e. low DC voltage condition), and should nullify the active power level if necessary. Therefore, these two requirements can be expressed by a mathematical function. For DC voltage magnitudes around nominal conditions, the function inhibits the active power modulation action (i.e. $\lambda_{MOD} = 1$). For very low DC voltage conditions, the function nullifies the active power demanded by the inverter VSC unit (i.e. $\lambda_{MOD} = 0$). During the transition between normal and low DC voltage conditions, the mathematical function should have a value that progressively transitions between 1 and 0. There are several mathematical functions that can comply with these requirements but from a control point of view, these two requirements match with the temporal response of a first-order transfer function. From a frequency domain perspective, the time response of a first-order transfer function can be seen as the inverse transformation of Laplace shown in 6.3. It can be seen that in 6.3, the inverse transformation of Laplace is defined by the exponential term α, which essentially determines the shape of the temporal evolution associated with the first-order dynamic system.

$$f(t) = (1 - e^{-\alpha t}) = \mathcal{L}^{-1}\left\{\frac{1}{s}\frac{\alpha}{(s+\alpha)}\right\} \qquad \forall t > 0 \tag{6.3}$$

The fundamental difference between the approach presented in 6.2 with respect to the inverse transformation of Laplace in 6.3, is the type of domain of the corresponding functions. The time domain dependency represents the one utilized by the Laplace transformation, while the DC voltage level represents the domain of the proposed approach shown in 6.2. Thus, the proposed approach could also

be interpreted as a way to develop a transient non-linear active power modification to provide DC voltage support based on the well-known dynamic response of a first-order transfer function when it is excited by a Heaviside's step function.

6.3.3. AC Network Fault at the Inverter Station (Onshore-to-Onshore HVDC link)

If during the (Onshore-to-Onshore) Point-to-Point operation, the three-phase fault event occurs at the V_{PCC_B} bus (as shown at Figure 6.7), the AC/DC power balance at *VSC B* unit will be immediately affected. This sudden change in the AC/DC power balance will be reflected at the DC terminals of *VSC B*, and consequently the DC power introduced by the rectifier station will also be altered at the rectifier *VSC A* unit. Once the AC voltage drop is generated in V_{PCC_B}, the FRT control function will be activated as described in section 3.4.1. However, the regulation of the active power level during the fault period becomes a challenge especially if the AC voltage drop is studied under the assumption of having a high-impedance fault element.

The fundamental problem lies in the accumulative error that takes place in the integrator block of the active power controller. This accumulative error essentially causes an undesired dynamic response of the active power that degrades the PFAPR performance.

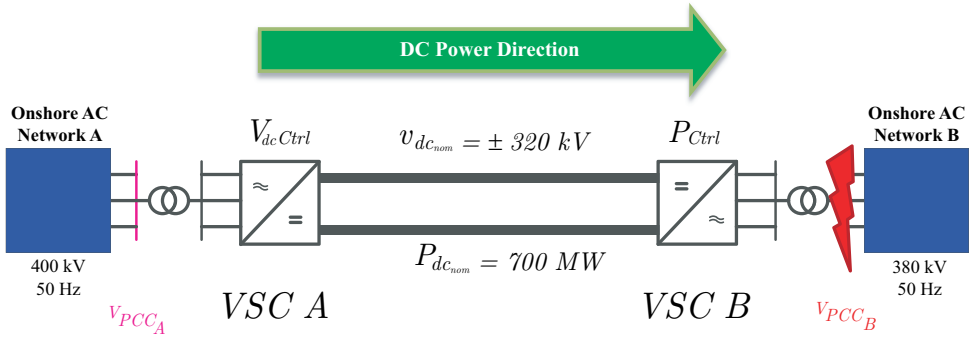

Figure 6.7: Expandable (Onshore-to-Onshore) PtP-VSC-HVDC link (under steady-state point-to-point operation) experiencing a sudden three phase fault at V_{PCC_B}.

Consequently, an enhancement of the original active power control (i.e., P_{Ctrl}) described in [5], was developed in section 3.4.2 as part of the proposed FRT design methodology. As shown in Figure 3.20, this enhancement was carried out based on the introduction of an (FRT activated) anti-windup loop which consists of an added PI controller. The (FRT activated) anti-windup loop is capable of regulating the state-variable value of the integral part of the PI controller of P_{Ctrl} during the activation period of the FRT function.

6.3.4. AC Network Fault at the Inverter Station (Offshore-to-Onshore HVDC link)

As mentioned in section 6.3.1, a point-to-point VSC-HVDC link can also be utilized to transmit active power from offshore AC networks to onshore AC Networks. This particular active power flow condition eliminates the issue concerning the DC voltage collapse (described in section 6.3.2), but leads into a potential DC over-voltage problem when an AC fault occurs as shown in Figure 6.8.

Essentially, the DC voltage across the HVDC link will experience a rise since the *VSC A* unit in Figure 6.8 will initiate its reactive current support (i.e. FRT will get activated), when the AC voltage level in V_{PCC_A} bus drops as described in section 3.4.1. The activation of the FRT in *VSC A* will block (jeopardize) the regulation of the DC voltage across the HVDC link, and as the *VSC B* unit keeps providing offshore power into the link, the electrostatic energy associated to the HVDC cables will increase. Therefore, a DC Chopper (red box in Figure 6.8) is normally included for these types of offshore-to-onshore links. The DC chopper will temporarily dissipate the provided power given by the offshore AC network keeping in that way the DC voltage level within predefined (between 1.05pu and 1.10pu) ranges [6, 7].

The PFAPR complexity associated with the VSC-HVDC condition shown in Figure 6.8 consists of the need of stabilizing the DC voltage level across the HVDC link when the fault clearing process at V_{PCC_A} starts. As shown in Figure 6.9, this complexity is tackled by utilizing the same anti-windup control strategy as proposed for the enhancement of the active power response during the post-fault period described in section 3.4.2.

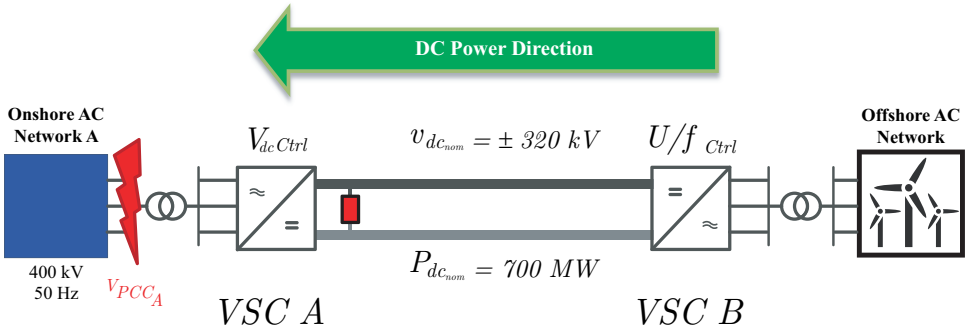

Figure 6.8: Expandable (Offshore-to-Onshore) PtP-VSC-HVDC link (under steady-state point-to-point operation) experiencing a sudden three phase fault at V_{PCC_A}.

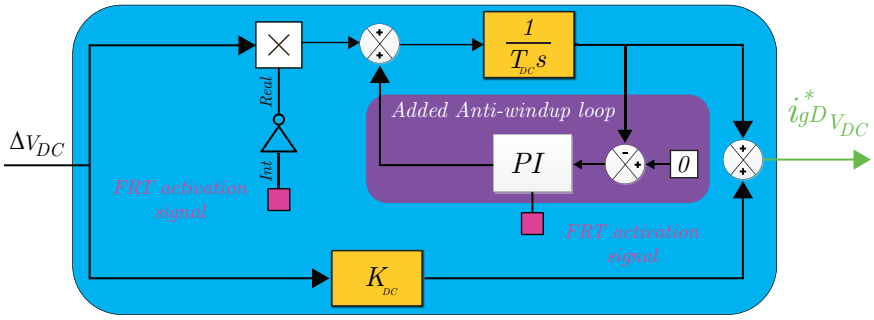

Figure 6.9: The highlighted purple section shows the added anti-windup dependent FRT control loop. The added loop consists of a PI controller regulating the state variable value of the integrator within the $V_{DC_{Ctrl}}$ (c.f. Figure 2.11), during the AC fault period.

6.4. PFAPR during Multi-Terminal Operation

6.4.1. Onshore-to-Onshore (Ons-Ons) Point-to-Point VSC-HVDC Expansion

Similar to section 4.5.1, the multi-terminal expansion shown in Figure 6.10 is done by connecting an 800MW offshore VSC unit, an offshore AC network, and additional DC cables to the point-to-point VSC-HVDC link shown in Figure 6.2. The offshore *VSC C* unit basically provides the AC voltage, and the electrical frequency references needed for the operation of wind turbines located within the offshore AC network in Figure 6.10. The AC voltages and the electrical frequency generated by *VSC C* are created by using the U/f control mode as described in [5].

The development of the PFAPR analysis is carried out by assuming that the steady-state power flow conditions of the multi-terminal expanded point-to-point VSC-HVDC link shown in Figure 6.10 are already established. This means that corresponding sequences associated with the energization process of the multi-terminal expanded network are out of the scope of this study. As mentioned in section 2.3.3, the DC power flow regulation of an expandable PtP-VSC-HVDC link operating in a multi-terminal network configuration can be developed considering two different scenarios. In the first scenario, the access for modifying the DC voltage references in the multi-terminal expanded point-to-point link is ensured, while in the second scenario, it is not ensured.

The PFAPR for the multi-terminal expanded onshore-to-onshore point-to-point link shown in Figure 6.10 is further elaborated in section 6.4.4 by considering the first scenario characteristics. Thus, the access for regulating the DC voltage references of the onshore VSC units shown in Figure 6.10 is ensured, enabling in that way the development of an Multi-Terminal DC Voltage Controller. From a RMS simulation environment perspective, the DC voltage regulation access is relatively simple to generate. It is relatively simple since, the associated communication interfaces (transferring the new DC voltage set-points between the Multi-terminal DC (MTDC)

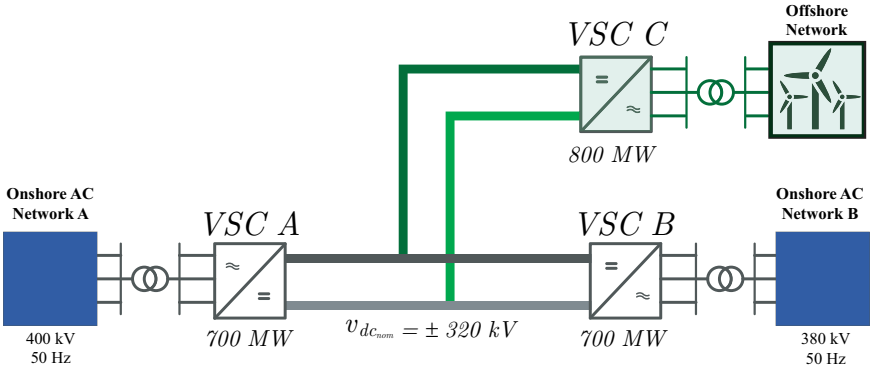

Figure 6.10: The Onshore-to-Onshore PtP-VSC-HVDC link shown in Figure 6.2 has been multi-terminal expanded by adding the green highlighted *VSC C* unit, and the corresponding offshore network.

Voltage Controller, and the onshore VSC units) are already integrated within the simulation software. However, the access for adjusting the DC voltage references in real VSC-HVDC stations would need to be explicitly requested by the corresponding owners of the multi-terminal link. This requirement is a fundamental step for ensuring that the DC power flow regulation can be developed through an external MTDC Voltage Controller. Additionally, the characteristics (e.g. time delays) of the communication interfaces to be used for ensuring the compliance of the PFAPR (especially) in a multi-terminal multi-vendor VSC-HVDC link context will also need to be discussed.

6.4.2. Offshore-to-Onshore (Off-Ons) Point-to-Point VSC-HVDC Expansion with DC Chopper

Unlike section 6.4.1, the multi-terminal expansion shown in Figure 6.11 consist of the addition of an 800MW onshore VSC unit, a DC Chopper, an onshore AC network, and additional DC cables to the point-to-point VSC-HVDC link shown in Figure 6.3.

A new DC chopper is added as part of the expansion in Figure 6.11 to mitigate the risk of having a DC over-voltage event across the HVDC network when the offshore power is fully transmitted towards the Onshore AC Network C. Concretely, the potential risk of having a DC over-voltage would occur if the *VSC C* unit experiences an AC/DC power imbalance event, while the *VSC A* unit is (for instance) out for maintenance. Moreover, for this particular type of multi-terminal expansion, the two DC power regulation scenarios described in section 6.4.1, are considered.

For the first scenario, it is assumed that the onshore VSC-HVDC units utilize the $Droop_{Ctrl}$ (similar to section 6.4.1), and that the access for modifying the DC voltage reference in both of them is ensured. Furthermore, the Multi-Terminal DC Voltage Controller is designed to transiently modify the DC voltage references of the onshore VSC-HVDC units and to activate the DC choppers (if needed) as further

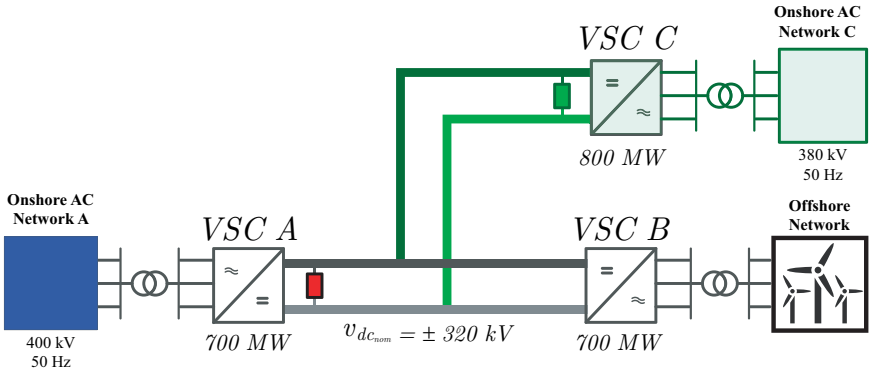

Figure 6.11: The Offshore-to-Onshore PtP-VSC-HVDC link shown in Figure 6.3 has been multi-terminal expanded by adding the green highlighted DC chopper, *VSC C* unit, DC cables, and the corresponding Onshore AC Network.

described in section 6.4.3.

For the second scenario, it is assumed that the access for regulating the DC voltage is not ensured for the Off-Ons point-to-point expansion shown in Figure 6.11. Therefore, the steady-state DC power management is mainly developed by considering the use of the DC Voltage (i.e. DC_{Ctrl}), and the active power (i.e., P_{Ctrl}) regulation at the *VSC A* and *VSC C* units. Furthermore, the role of the Multi-Terminal DC Voltage Controller for this particular scenario is further discussed in section 6.4.6.

6.4.3. Dynamically Adjustable Chopper Impedance

As indicated in section 6.3.4, the DC chopper (represented as a red box in Figure 6.3) is responsible for absorbing the wind power provided by the offshore network during a short period of time. From a physical point of view, this implies that the DC chopper works as a controllable DC power consumption element, which is activated when a DC over-voltage phenomenon occurs within the point-to-point VSC-HVDC link. Similarly, in the multi-terminal (MT) expanded point-to-point HVDC link shown in Figure 6.11, the DC choppers can be used to mitigate DC over-voltages occurring within the MT network. On the other hand, it is worth pointing out that the risks of having a DC over-voltage issue within the MT network can be reduced, depending on the power control modes used by the *VSC A* and *VSC C* units shown in Figure 6.11. This reduction occurs since the electrostatic energy corresponding to the DC over voltage is distributed (by the control modes), between the corresponding *VSC A* and *VSC C* units. Therefore, if for example, the FRT function of the *VSC A* unit is activated (due to a transient AC fault at Onshore Network A), then, the wind power supplied by the Offshore Network can be transiently and fully transmitted towards the *VSC C* unit. However, this transient modification of the steady-state power flow conditions of the VSC C unit could be potentially avoided, if the DC power consumption characteristics of the DC chopper were coordinated by the MT

DC Voltage Controller.

Typically, the DC chopper consists of a resistor which is inserted and excluded into the HVDC network creating in that way a DC voltage ripple phenomenon across the HVDC link. However, based on the dynamically adjustable fault impedance (DAFI) concept proposed in section 3.4.3, and considering the latest developments in DC choppers technology [8, 9], the dynamically adjustable chopper impedance (DACI) concept is proposed here. As indicated in [8, 9] the new developments in DC chopper technology enable the smooth regulation of the DC current flowing through the DC chopper's resistors based on a power electronic IGBT arrangement. Therefore the proposed DACI concept is characterized by the RMS representation of the DC chopper's impedance (within the RMS simulation framework) as a controllable current source which is governed by the proposed control system shown in Figure 6.12.

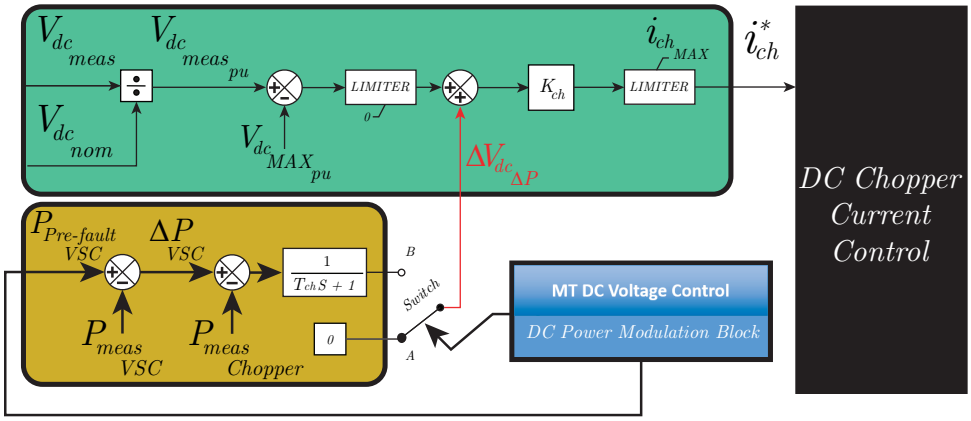

Figure 6.12: Proposed voltage and power modulation for the DACI of the DC Chopper.

The control system presented in Figure 6.12 is divided by two main control loops (the green one and the brown one) which define the amount of DC current that flows through the controllable current source (i.e. the DC chopper).

The green loop shown in Figure 6.12 represents the loop used to enable the power dissipation of the DC chopper when a DC over-voltage issue is detected. In general, the DC chopper current reference i^*_{ch} generated by the green loop utilizes a proportional controller which consists of the gain K_{ch}. Within the green control loop, K_{ch} amplifies the difference between the measured DC voltage across the DC chopper (i.e. $V_{dc_{meas_{pu}}}$), and the maximum DC voltage level (i.e. $V_{dc_{MAX_{pu}}}$) which is a constant value (e.g. 1.05pu). Furthermore, the deactivation of the DC chopper during normal operating conditions in the HVDC link is obtained through the use of the limiter (low-limit) block shown in Figure 6.12. Finally, the output signal generated by the gain K_{ch} is limited by a second limiter block which is used to define the

maximum current capabilities of the DC Chopper (i.e. $i_{ch_{MAX}}$) within the proposed control loop.

The brown loop shown in Figure 6.12 is designed to modify the input signal of K_{ch} based on the addition of the $\Delta V_{dc_{\Delta P}}$ signal. The $\Delta V_{dc_{\Delta P}}$ signal is essentially an active power-based DC voltage error. The generation of the $\Delta V_{dc_{\Delta P}}$ starts by subtracting two signals. The first signal $P_{Pre-Fault}$, represents the pre-fault active power level of an FRT-activated VSC-HVDC unit. The second signal $P_{meas_{VSC}}$, represents the measured active power level of such FRT-activated VSC-HVDC unit. The $P_{Pre-Fault}$ is a constant signal provided by the MT DC Voltage Controller. As explained in section 6.4.4, the MT DC Voltage Controller should be capable of recording the pre-fault active power level of the FRT-activated VSC-HVDC unit. This implies that unlike, the DC power modulation strategies for DC Choppers shown in [10], the proposed DACI concept in this dissertation is coordinated with the transient DC voltage regulation developed by the MT DC Voltage controller. The MT DC Voltage Controller sends the $P_{Pre-Fault}$ signal and simultaneously changes the *State* of the DC Power Modulation switch shown in Figure 6.12. Once the switch goes from *State A* (normal condition) to *State B* (FRT condition), the brawn loop will introduce the $\Delta V_{dc_{\Delta P}}$ signal, and then, the DC power-based dynamic adjustment of the DC chopper will start. Thus, the brown loop is designed to operate during i) the FRT activation of an onshore VSC-HVDC unit (c.f. Figure 6.11), and ii) during the following PFAPR period (c.f. Figure 6.1). Ergo, the $\Delta V_{dc_{\Delta P}}$ signal generated by the brown loop in Figure 6.12 has the role of transiently balancing the multi-terminal DC power flow during the FRT and the PFAPR period of an onshore FRT activated VSC-HVDC unit.

Furthermore, the difference between $P_{Pre-Fault}$ and $P_{meas_{VSC}}$ (i.e., ΔP_{VSC}) is used as the reference signal defining the power to be consumed by the DC chopper. The ΔP_{VSC} signal, and the measurement of the DC power consumed by the DC chopper (i.e., $P_{meas_{Chopper}}$) are subtracted to generate an error signal which is sent to a first-order transfer function defined by the time constant T_{ch}. The time constant T_{ch} represents the associated delay needed by the control system to actually process the required DC Power level of the DC chopper and its setup for a 10ms time range. Finally, the coordination process is designed to be aligned with the PFAPR requirements (c.f. section 6.1) while, reducing DC power imbalance levels within the MT HVDC network caused by an FRT-activated VSC-HVDC unit, as described in sections 6.4.5 and 6.4.6.

6.4.4. Expanded Ons-Ons link with Droop Control

For this particular point-to-point (Ons-Ons) expansion (c.f. Figure 6.10), it is assumed that the DC power regulation at each onshore station (during steady-state operation) is characterized by the $Droop_{Ctrl}$ (c.f section 2.3.2). As mentioned in section 6.4.1, it is also assumed that the access for modifying the DC voltage reference in the onshore VSC units (by means of a Multi-Terminal Voltage Controller) is ensured. As described in section 2.3.2, the $Droop_{Ctrl}$ represents a regulation

mechanism that modifies the DC voltage level in one particular VSC-HVDC unit depending on the amount of DC power that is transmitted through this unit. Thus, in Figure 6.10, the $Droop_{Ctrl}$ at each onshore station will modify the DC voltage references at the onshore stations, when the amount of offshore (wind) power supplied by *VSC C* unit (c.f. Figure 6.10) changes.

PFAPR for Ons-Ons Expansion (with Droop Control) using a Multi-Terminal DC Voltage Controller

As the access for modifying the DC voltage reference in the onshore stations is ensured, it is possible to design a Multi-Terminal DC Voltage Controller capable of generating the DC voltage modulation term ($V_{dc_{MOD}}$) as shown in Figure 6.13. The modulation term $V_{dc_{MOD}}$ is generated to modify the DC voltage reference of the FRT-activated VSC-HVDC unit as described in 6.4. Notice that in Figure 6.13, the MTDC Voltage controller also obtains data from each onshore VSC unit concerning their DC voltage level $V_{dc_{meas}}$, their active power level P_{meas}, and their FRT status FRT_{Act}.

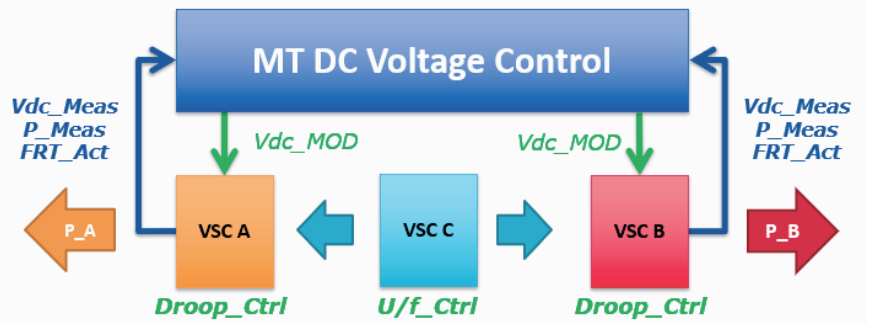

Figure 6.13: Control Hierarchy of the multi-terminal expansion shown in Figure 6.10 with access to modify the DC voltage references of the onshore VSC units ($V_{dc_{MOD}}$).

$$V_{dc}^{*} = V_{dc_0} - K_{Droop_{dc}} \Delta P - V_{dc_{MOD}} \tag{6.4}$$

Within the simulation software utilized (i.e. DigSilent PowerFactory 2019), the transmission, and the reception of the data associated with the MTDC Voltage Controller do not constitute a major issue. This is because its implementation has been developed utilizing the same Dynamic Simulation Language (DSL) used to implement the basic and the supplementary controllers of the expandable VSC-HVDC link described in Chapter 3. On the other hand, the transmission and the reception of the data concerning a MTDC Voltage controller regulating the PFAPR process for real HVDC projects would need to be defined and developed by considering several technical aspects. These technical aspects are referred (for example), to the characteristics of the communication interfaces (e.g. associated time delays) utilized by the onshore VSC units. Moreover, the corresponding data to be interchanged must be clearly defined by the corresponding VSC-HVDC owners. For example, the FRT_{Act} signal (shown in Figure 6.13) is used as a triggering signal which notifies

about the moment in which the three-phase AC fault event starts and ends at the affected AC network. The processing of other signals like converter blocking, DC cable fault, and saturation of the modulation index might also represent a relevant step for developing a more sophisticated criterion for the DC power flow regulation performed by the MTDC Voltage Controller in larger multi-terminal networks. However, the analysis of this criterion is out of the scope of the PFAPR process studied in this dissertation, and it is suggested as a future research topic.

The expressions 6.5 and 6.6 are used to describe the piecewise mathematical formulation defining $V_{dc_{Mod}}$.

$$V_{dc_{MOD}} = \begin{cases} 0 & \text{before the post-fault period,} \\ \Delta V_{dc_{MEM}}(1 - e^{-\alpha(P_{Pre-Fault} - P_{meas})}) & \text{during post-fault period} \end{cases} \quad (6.5)$$

$$\Delta V_{dc_{MEM}} = |V_{dc_{meas}} - V_{dc_{PreFault}}| \quad (6.6)$$

It can be noticed in 6.5 that the value of the $V_{dc_{MOD}}$ term depends on the fault, and post-fault periods shown in Figure 6.1 (c.f. section 6.1). Next, the non-linear (exponential) nature of the $V_{dc_{MOD}}$ modulation has been inspired based on the DC voltage support method described by the expressions 6.1 and 6.2 in section 6.3.2. Furthermore, it can be seen in 6.5 that during the post-fault period, the $V_{dc_{MOD}}$ is also defined by the term $\Delta V_{dc_{MEM}}$.

As shown in 6.6, the $\Delta V_{dc_{MEM}}$ represents the absolute value of the difference between the $V_{dc_{meas}}$ of the affected VSC-HVDC unit and its pre-fault DC voltage level $V_{dc_{PreFault}}$. Finally, the rate of change of the exponential function depends on the gain α, and the difference between the active power of the affected VSC-HVDC unit P_{meas}, and its pre-fault active power level $P_{Pre-Fault}$. The $V_{dc_{PreFault}}$ and the $P_{Pre_{Fault}}$ are memorized by the MTDC Voltage Controller and established as constant values which are taken based on the instant before the FRT function is activated. Thus, these constant values are used to set up the equation 6.5 during the post-fault period.

As shown in Figure 6.13 the information associated with the $V_{dc_{PreFault}}$ and the $P_{Pre-Fault}$ terms is obtained from the data provided by each onshore VSC unit as shown in Figure 6.13. Basically, the variables $V_{dc_{meas}}$ and P_{meas} are used by the MTDC Voltage Controller to generate the $V_{dc_{PreFault}}$ and the $P_{Pre-Fault}$ terms, once the FRT activation signal has been sent to it. It is important to clarify that the MTDC Voltage Controller modifies the DC voltage reference only in the affected onshore VSC-HVDC unit during the post-fault period as indicated in 6.4. This consideration implies that the role of the proposed MTDC Voltage Controller is to guarantee an effective PFAPR response at the affected VSC-HVDC unit based on the requirements described in section 6.1.

Rationale behind the (Ons-Ons Expansion with Droop Control) MTDC Voltage Controller

If an AC fault occurs at one of the V_{PCC} buses shown in Figure 6.10, the active power reduction in the affected VSC-HVDC unit will generate a transient rise in its DC voltage terminals. The DC voltage rise occurs since it is assumed that under the $Droop_{Ctrl}$ (implemented within each onshore VSC unit), the DC power in the multi-terminal link will always flow from the offshore VSC unit towards the onshore VSC units. Therefore, if the AC fault event is cleared from the affected AC network, the DC voltage in the affected VSC unit should ideally be reduced to its pre-fault level, to reestablish its corresponding pre-fault active power level. Thus, the $\Delta V_{dc_{MEM}}$ term represents the DC voltage error needed to obtain the pre-fault DC voltage level (i.e., $V_{dc_{PreFault}}$) in the affected VSC unit during the post-fault period.

At the beginning of the post-fault period, the difference between the actual active power level (i.e. P_{meas}), and the pre-fault active power level $P_{Pre-Fault}$ (c.f expression 6.5) is maximum, and consequently: $V_{dc_{Mod}} \approx |V_{dc_{meas}} - V_{dc_{PreFault}}|$. Thus, the $V_{dc_{Mod}}$ will initially place the $V_{dc_{PreFault}}$ term within the expression 6.4, creating in that way an additional support for the $Droop_{Ctrl}$ to bring down the DC voltage level in the affected VSC unit during the PFAPR period. Next, as soon as the DC voltage level start to be reduced, the restoration of the pre-fault active power level (i.e. $P_{Pre-Fault}$) will start to be developed. It is also worth remembering that the DC voltage regulation of the affected VSC-HVDC unit is progressively restored during the PFAPR period since its FRT function progressively restores the active current regulation as soon as the AC voltage's magnitude is above 50% of its nominal level (c.f. section 3.4.1). Consequently, during the beginning of the PFAPR period, a proportional control action (c.f. Figure 6.9) develops the restoration process of the DC voltage at the affected VSC-HVDC unit.

The progressive restoration process of the active power during the post-fault period does also influence the exponential term in the expression 6.5, which will generate a reduction of the $V_{dc_{Mod}}$ value over the V_{dc}^{*} reference in 6.4. Thus, the exponential modulation concerning the $V_{dc_{Mod}}$ term, acts as a DC voltage support method that dynamically change the V_{dc}^{*} value. Additionally, the exponential modulation is progressive mitigated in V_{dc}^{*} as a consequence of continuous restoration process of the pre-fault active power level at the affected VSC-HVDC unit during post-fault period. Finally, the dynamic change of V_{dc}^{*} can also be understood as a transient modification of the P-V_{dc} trajectory (c.f. Figure 2.13) defined by the expression 6.4, for ensuring the compliance of the PFAPR requirements discussed in section 6.1.

It can also be noticed in Figure 6.13 that the data concerning the P_{meas}, the $V_{dc_{meas}}$, and the FRT_{Act} is only exchanged between the corresponding VSC-HVDC unit and the MTDC Voltage controller. In other words, for the proposed PFAPR, there is no need of having a direct communication channel between the VSC-HVDC units, since they are part of a hierarchical structure exclusively governed by the

MTDC Voltage controller. This hierarchical approach does simplify the design of a MTDC Voltage controller. It gets simplified since it concentrates the efforts to individually align the communication interfaces used between the MTDC Voltage controller, and each of the onshore VSC-HVDC units shown in Figure 6.10. These individual alignments will represent a methodological procedure that can potentially be used to facilitate the design of a MTDC Voltage Controller within a multi-terminal multi-vendor context.

6.4.5. Expanded Off-Ons link with Droop Control

Similar to section 6.4.4, it is assumed that the access for modifying the DC voltage reference in the onshore VSC-HVDC units shown in Figure 6.11 (by means of a Multi-Terminal Voltage Controller) is ensured. Furthermore, it is also assumed that both onshore VSC-HVDC units utilize the $Droop_{Ctrl}$ to regulate the steady-state DC power flow across the multi-terminal network presented in 6.11. Additionally, the offshore power generated by the wind turbines in Figure 6.11 is always distributed between the onshore VSC-HVDC, which means that there is no DC power interchanged between the onshore AC networks.

Considering the assumptions described in the previous paragraph, and the presence of the DC Choppers, the design of the Multi-Terminal DC Voltage Controller shown in Figure 6.13 is adapted as shown in Figure 6.14.

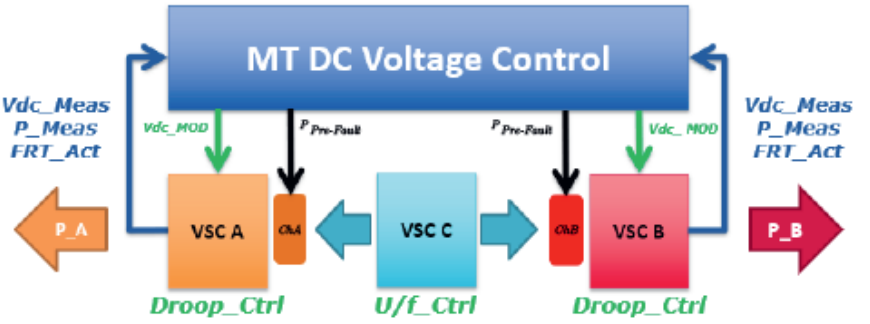

Figure 6.14: Control Hierarchy of the multi-terminal expansion shown in Figure 6.11 with access to modify the DC voltage references of the onshore VSC units ($V_{dc_{MOD}}$) and DC Choppers Control.

PFAPR for Off-Ons Expansion (with Droop Control) using a Multi-Terminal DC Voltage Controller

The adaptation of the Multi-Terminal DC Voltage Controller shown in Figure 6.14 consists of the addition of the output signals $P_{Pre-Fault}$. The addition of these two new output signals does not represent a major modification of the mathematical functions defining the transient DC voltage regulation shown in section 6.4.4. Instead, it utilizes the data associated with the activation of the FRT (FRT_{Act}), and the pre-fault active power level $P_{Pre-Fault}$ (of the FRT activated VSC-HVDC unit),

to activate the DC power dissipation capabilities of the DC chopper.

The activation of the DC power dissipation capabilities of the DC chopper is developed to prevent the AC/DC power imbalance (caused by the FRT-activated VSC-HVDC unit) spread across the multi-terminal system shown in Figure 6.11. The $V_{dc_{MOD}}$ signal modulates the DC voltage reference during the post-fault period of the FRT-activated VSC-HVDC unit (as in Figure 6.13) by using the expressions 6.4 and 6.5. Next, the FRT_{Act} signal and the P_{meas} value are used to determine the $P_{Pre-Fault}$ value which is sent to the control system of the DC chopper (c.f. Figure 6.12) to temporarily absorb DC power from the multi-terminal network.

Essentially, the Multi-terminal DC Voltage Controller detects the change in the status of the FRT_{Act} signal (active or inactive) and it memorizes the corresponding P_{meas} value just before the FRT_{Act} is changed. Thus, the memorized value of the active power before the FRT activation represents the $P_{Pre-Fault}$ which is used by the DC Chopper. Hence, the disturbance caused by an AC fault in one of the onshore networks would not necessarily lead to a sudden redistribution of the DC power across the multi-terminal HVDC network. This is because the DC power dissipated by the DC Chopper is coordinated with the level of power provided by the FRT-activated VSC-HVDC units during the fault and the post-fault periods.

Rationale behind the (Off-Ons Expansion with Droop Control) MTDC Voltage Controller

The activation of the DC power dissipation capabilities of the DC chopper by means of the MT DC Voltage Controller is designed to avoid unnecessary changes in the DC power across the multi-terminal network. On the other hand, the activation of the DC power dissipation capabilities of the DC chopper by means of the MT DC Voltage Controller must be bounded by the thermal limits associated with the DC chopper. However, the thermal analysis of the DC chopper has not been considered, since the focus of this chapter is the design of a PFAPR controller capable of supporting the dynamic stability of the multi-terminal HVDC networks. Basically, the dynamic stability of the multi-terminal network during the fault and the post-fault period is tackled by adapting the Multi-terminal DC Voltage Controller to coordinate two control functions. These two control functions are: i) the transient DC voltage modulation of the FRT-activated onshore VSC-HVDC unit, and ii) the DC power dissipation control system of the DC chopper. The simulation results associated with this Off-Ons point-to-point expansion are shown in section 6.5.4 and section 6.5.5.

6.4.6. Expanded Off-Ons link with DC Voltage and Active Power Control

In this section (unlike section 6.4.5, the expansion of the Off-Ons point-to-point link shown in Figure 6.11 does not foresee that the access for regulating the DC voltage of the Onshore VSC-HVDC units is ensured. Consequently, the Onshore VSC-HVDC unit of the point-to-point link (i.e. *VSC A* in Figure 6.11) keeps controlling the DC

voltage of the multi-terminal network. On the other hand, the *VSC B* is set up to control the active power across the multi-terminal expanded Off-Ons point-to-point link.

For this particular Off-Ons expansion, it is convenient to clarify that although the DC voltage of the Onshore VSC-HVDC units cannot be modified, the Multi-terminal DC Voltage Controller will be able to command the DC choppers as shown in Figure 6.15.

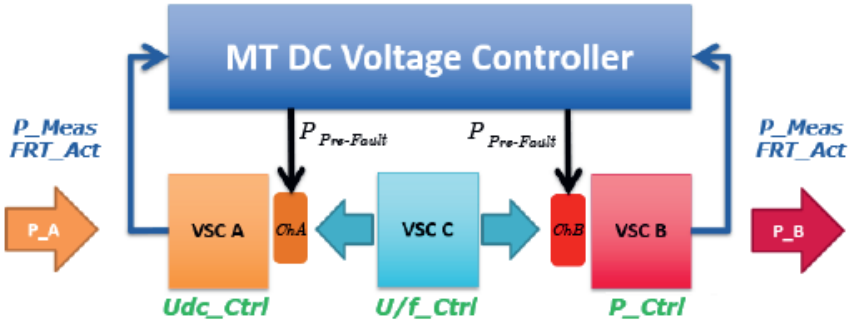

Figure 6.15: Control Hierarchy of the multi-terminal expansion shown in Figure 6.11 without access to modifying the DC voltage references of the Onshore *VSC A* unit. Conversely, the DC Choppers Control is ensured.

The command of the DC choppers is referred to the control of their DC power dissipation capabilities. It can also be noticed from Figure 6.15 that the Multi-terminal DC Voltage Controller will need to use the corresponding status of the FRT_{Act} signal, and the active power level of the corresponding VSC-HVDC units to properly command the DC choppers.

Rationale behind the (Off-Ons Expansion with DC Voltage and Active Power Control) MTDC Voltage Controller

It can be noticed from Figure 6.11, that the DC power flow across the multi-terminal network is now conditioned by the level of offshore wind power provided by the *VSC C* unit, and by the level of active power established by the *VSC B* unit. This condition can also lead to a DC power flow distribution in which the *VSC A* unit provides power from the Onshore AC network A towards the multi-terminal HVDC network. Consequently, if an AC/DC power imbalance occurs at one of the onshore VSC-HVDC units, the PFAPR process will depend essentially on two aspects. The first aspect is the control mode used by the FRT-activated onshore VSC-HVDC unit, and the second aspect depends on the steady-state ratio between the supplied power by *VSC C* and the demanded power established by *VSC B*.

The evolution of the DC Voltage response across the multi-terminal network (during the activation of the FRT function in one of the onshore VSC-HVDC units),

will also depend on the two aspects mentioned in the previous paragraph. Thus, the two aspects might lead to either DC over-voltage or either a DC voltage collapse issue in the multi-terminal network as shown in section 6.5.5.

6.5. Simulation Setup and Results

The analysis of the expandable PtP-VSC-HVDC links discussed in sections 6.3.1 and 6.4 is carried out by performing simulation experiments under a quasi-stationary (or RMS) simulation time frame in DIgSILENT PowerFactory 2019. The modelling assumptions described in [5] for the outer controllers of a VSC unit are used, and the supplementary controllers indicated in sections 3.4, 6.3.2, 6.3.4, 6.4.3, and 6.4.4 are also included. Additionally, the implementation of the offshore AC network is developed by considering the layout described in [11].

The analysis of the non-linear modulation strategy for the PFAPR compliance starts by considering a 200 ms three-phase onshore fault for each of the simulation-based experiments developed for the point-to-point and multi-terminal configuration of the expandable HVDC link shown by the Figures 6.4, 6.7, 6.10, and 6.11. Based on real PtP-VSC-HVDC requirements [12] and national HVDC grid codes [2], it is assumed that the time limit for reestablishing the pre-fault active power levels (i.e. Δt_3 in Figure 6.1) is 200 ms after 90% of the pre-fault network voltage level has been restored.

6.5.1. Point-to-Point Operation: AC Network Fault at the Rectifier Station (Ons-Ons HVDC link)

During the steady-state operation of Figure 6.16, the *VSC A* unit regulates the DC voltage level across the HVDC link, while the *VSC B* station provides 600 MW to the Onshore AC network B. Next, a three-phase fault occurs at the AC network terminals of the *VSC A* unit (i.e. V_{PCC_A}) creating in that way a 600MW AC/DC power imbalance. The parameter values associated with α and the LVT (indicated by the expression 6.2) are 1500 and 0.97 respectively. The three-phase fault experienced by the AC network A at t = 0.2s presented in Figure 6.17a generates a 600MW AC/DC power imbalance across the HVDC link as shown in Figure 6.17b. During the fault period, the FRT function gets activated at *VSC A* unit prioritizing its reactive current injection (i.e. I_q) over the active current injection (i.e. I_d) as presented in Figure 6.17c. The prioritization of the reactive current during the fault period directly jeopardizes the operation of the DC voltage control developed by the *VSC A* unit, causing in that way a critical reduction of the DC voltage as shown in Figure 6.17d. The reduction of the DC voltage is caused by the demand of power generated by the *VSC B* unit. Furthermore, the control system shown in Figure 6.5 is implemented for *VSC B* unit, creating in that way a transient DC voltage support in the HVDC link during the fault period.

As soon as the DC voltage in the DC terminals of the *VSC B* unit gets close to the LVT level, the proposed non-linear DC power modulation strategy generates

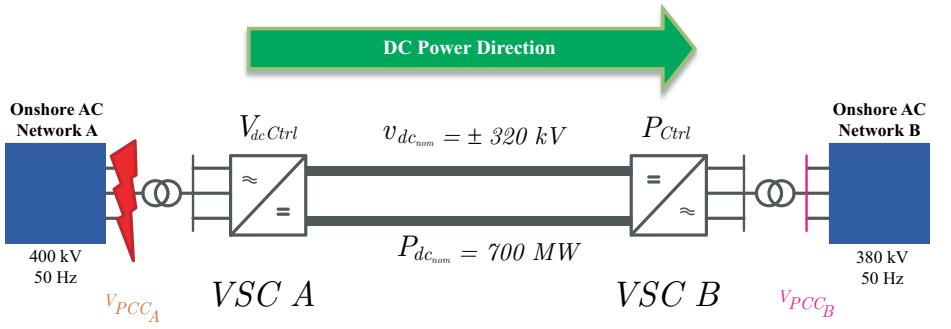

Figure 6.16: Expandable (Onshore-to-Onshore) PtP-VSC-HVDC link (under steady-state point-to-point operation) experiencing a sudden three phase fault at V_{PCC_A}.

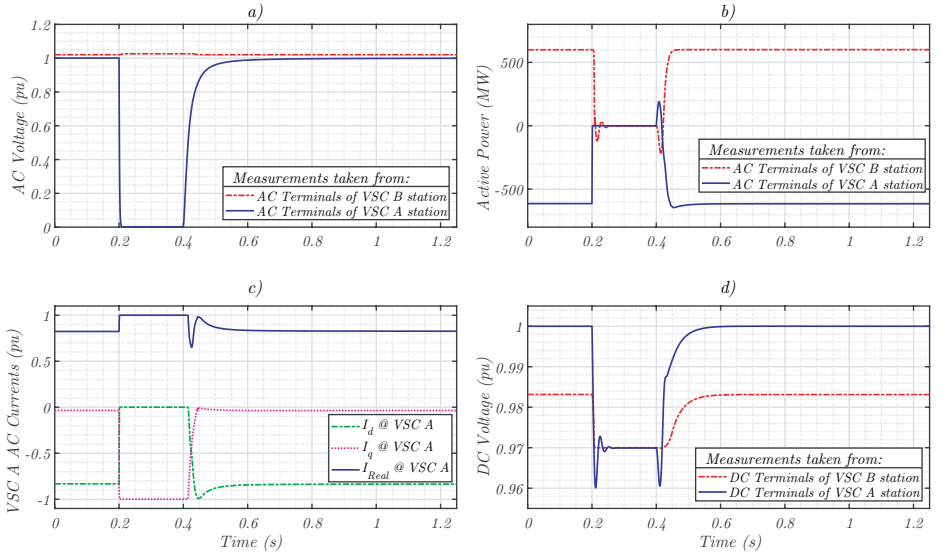

Figure 6.17: The Ons-Ons Point-to-point HVDC link having a three-phase AC fault (at t = 0.2s) at its rectifier (*VSC A*) unit. The associated onshore networks' AC voltage is shown in 6.17a. The active powers of the VSC units are shown in Figure 6.17b. The injection of reactive current at *VSC A* unit during the fault period is presented in Figure 6.17c. Finally, the DC voltages are shown in Figure 6.17d.

a reduction of the active power demanded by the *VSC B* unit in Figure 6.4. The reduction of the active power demanded by the *VSC B* helps to stabilize the DC voltage in the HVDC link, and it also produces a boosting action in the DC voltage by generating a change in the direction of the active power flow demanded. The change in the active power flow direction is a consequence of the negative values generated by the expression 6.2 when the DC voltage at the DC terminals of the VSC B unit goes to levels below the LVT as observed in Figure 6.6. As shown in Figure 6.17d, the non-linear DC power modulation strategy allows stabilizing the DC voltage in the entire HVDC system during the fault period which means that the

forfeit of the DC voltage regulation in the *VSC A* unit does not lead into the collapse of the stability of the HVDC link as shown in Figure 6.16.

As seen in Figure 6.17a, the voltage at V_{PCC_A} starts to recover at t = 0.4s. Consequently, the priority of the active current over the reactive current in VSC A is progressively given back, as soon as the AC voltage level surpasses 50% of the pre-fault voltage level in the Onshore AC network A (c.f. Figure 6.16). This post-fault FRT reactive current criteria implies that, during the recovering process of the AC voltage, the difference between the DC and AC voltage magnitudes at the *VSC A* terminals will induce a transfer of active power towards the AC network A. However, as indicated by the reactive current injection (FRT) requirements shown Figure 3.16 of section 3.4.1, once the AC voltage level surpasses 50%, the injected active current starts to progressively increase (c.f. Figure 6.17c) following the proportional response associated to the design of the anti-windup loop shown in Figure 6.9. Thus, the DC voltage control in *VSC A* begins to be restored increasing the level of DC voltage to its pre-fault condition as shown in Figure 6.17d.

As the DC voltage regulation action is progressively restored at the *VSC A* unit, the DC current in the HVDC link starts to increase, producing in that way an increment in the power (DC current) transferred towards the *VSC B* unit. Moreover, due to the electrostatic energy storage characteristics of the HVDC cable, the increment of the DC current (during the post-fault period) also generates a boosting of the voltage level at the DC terminals of the *VSC B* unit (c.f. Figure 6.17d). The progressive DC voltage recovery in the DC terminals of *VSC B* unit, increments the λ_{MOD} value (c.f. expression 2.2) of the *VSC B* unit, creating in that way gradual reestablishment of its "normal" active power regulation process. In this context, the "normal" active power regulation is referred to λ_{MOD} = 1. Finally, the results shown by Figure 6.17 demonstrates that the coordination between the recovery process of the DC voltage level (developed by the DC_{Ctrl} in VSC A), and the non-linear (exponential) DC power modulation strategy (developed by *VSC B*) are aligned with the PFAPR needs. Additionally, it has also been demonstrated that the DC voltage restoration process and the PFAPR process in Ons-Ons point-to-point link can be performed without having a dedicated communication infrastructure between the VSC units during the fault and post-fault periods described in Figure 6.1.

6.5.2. Point-to-Point Operation: AC Network Fault at the Inverter Station (Ons-Ons HVDC link)

The simulation experiments corresponding to Figure 6.18 were already discussed in section 3.4.2 and are repeated (for the sake of illustration) in Figure 6.19. In section 3.4.2, the analysis was focused on the dynamic response of the active power generated by the proposed anti-windup loop, considering different levels of (high impedance) AC faults. The different high impedance AC faults levels produces different levels of AC voltage drops at the Onshore AC Network B as indicated in Figure 6.18. Consequently, the reactive and the active current injection developed by the *VSC B* unit is adjusted accordingly to the FRT polynomial reference and the

enhanced active power controller described in section 3.4.

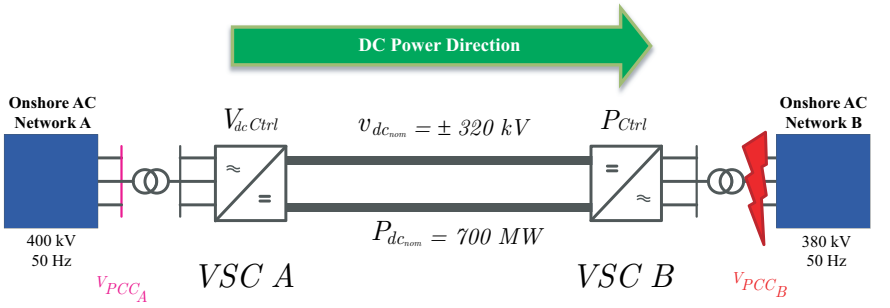

Figure 6.18: Expandable (Onshore-to-Onshore) PtP-VSC-HVDC link (under steady-state point-to-point operation) experiencing a sudden three phase fault at V_{PCC_B}.

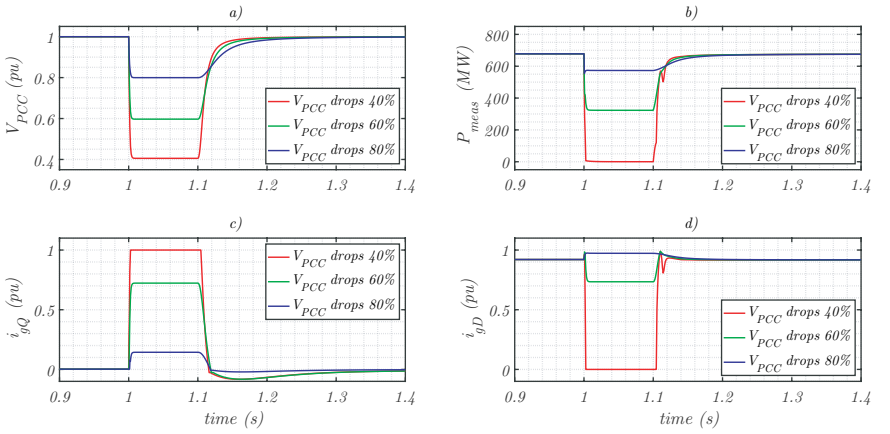

Figure 6.19: Active power, reactive current, active current responses of the *VSC B* unit, experiencing different levels of AC voltage drops (c.f. section 3.4.2).

6.5.3. Multi-Terminal Operation: Ons-Ons Point-to-Point VSC-HVDC Expansion with Droop Control

As described in section 6.4.1, the multi-terminal expansion of an Ons-Ons PtP-VSC-HVDC link is developed by adding an 800MW offshore VSC unit connecting an offshore AC network (network characteristics in [11]) providing wind power as shown in Figure 6.10. On the other hand, the steady-state power conditions considered for the simulation experiment concerning this multi-terminal expansion are presented in Figure 6.20. Moreover, Figure 6.21, shows the simulation experiments concerning Figure 6.20. It can be notice in Figure 6.21 that there is a 200ms three-phase fault occurring at the V_{PCC_B} bus (at t = 0.2s), when the *VSC B* unit (operating with $Droop_{Ctrl}$) transmits approximately 500MW towards the Onshore AC Network B. Furthermore, the 500MW are obtained from the 700MW provided by the Offshore

AC Network, and consequently, *VSC A* transmits approximately 200MW towards the Onshore AC Network A.

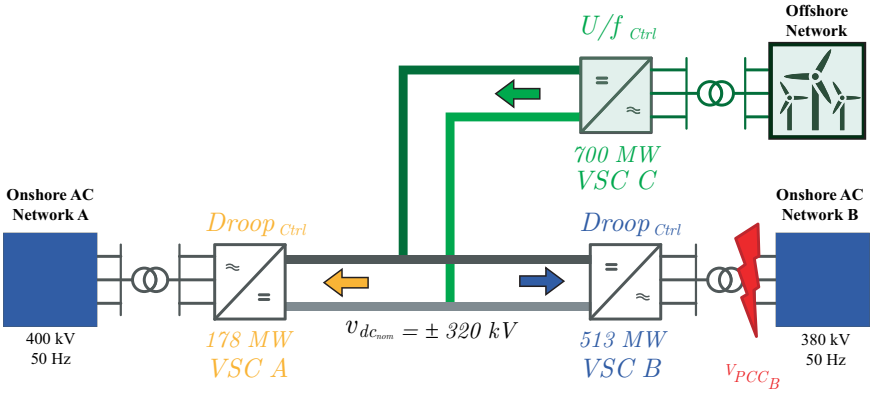

Figure 6.20: Steady-state DC power distribution with the coloured arrows, and the AC fault at V_{PCC_B} for the multi-terminal expanded Ons-Ons point-to-point VSC-HVDC link described in Figure 6.2.

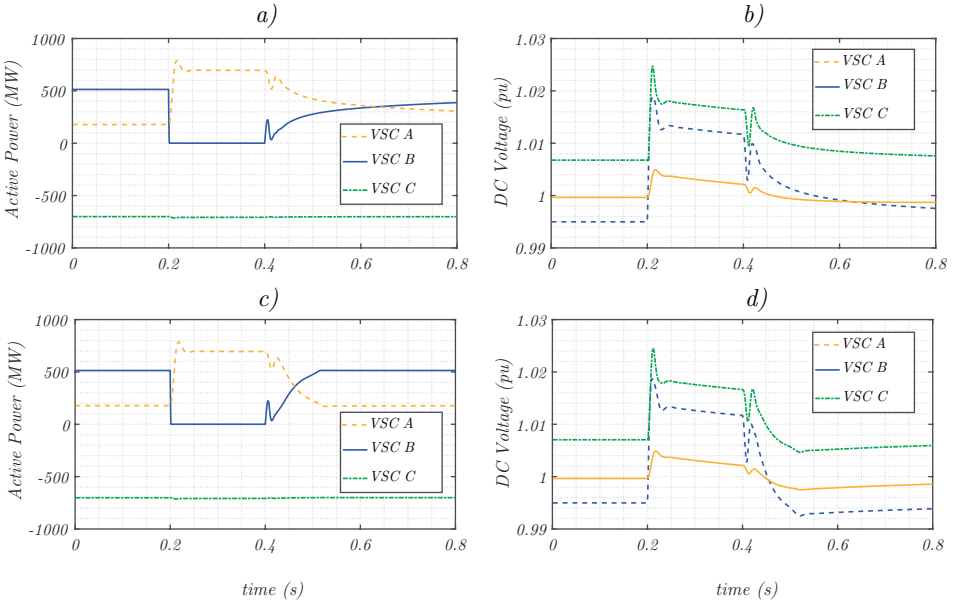

Figure 6.21: Multi-terminal expanded Ons-Ons PtP-VSC-HVDC link (c.f. Figure 6.10) experiencing an AC fault (at t = 0.2 s) at *VSC B* unit working with $Droop_{Ctrl}$ at 5%. The Case A1 presents the response of the active powers and the DC voltage responses in the VSC units utilizing a conventional $Droop_{Ctrl}$ in Figure 6.21a and Figure 6.21b respectively. The Case A2 presenting the response of the active powers and the DC voltage responses in the VSC units utilizing the proposed non-linear modulation (c.f. 6.4) in Figure 6.21c and Figure 6.21d respectively.

The simulation experiments for Figure 6.20 are divided into two cases (i.e. Case A1 and CaseA2). In Case A1, the active power and DC voltage responses of the multi-terminal network are analyzed by using the DC power flow regulation method associated with the conventional $Droop_{Ctrl}$ method described in section 2.3.2. In Case A2, the active power and DC voltage responses of the multi-terminal network are analyzed by using the proposed exponential modulation of the DC Voltage reference at the FRT-activated onshore VSC-HVDC unit described in section 6.4.4. Thus, both cases (Case A1 and Case A2) are compared to demonstrate the superior performance of the proposed exponential modulation within the PFAPR context. The unequal DC power distribution shown in Figure 6.20 and Figure 6.21 is generated since different $Droop$ gains (i.e. cf. K_{Droop} in 6.4) have been utilized for each VSC unit as indicated in Figure 6.21.

For the *VSC A* unit a K_{Droop} = 0.01 (i.e. 1% of $Droop_{Ctrl}$) has been used, and for the *VSC B* unit a K_{Droop} = 0.05 (i.e. 5% of $Droop_{Ctrl}$) has been used. The active power responses of all the VSC-HVDC units for Case A1 and Case A2 are shown in Figure 6.21a and Figure 6.21b, respectively. Additionally, the DC voltage responses for the Case A1 and Case A2 are shown in Figure 6.21b and Figure 6.21d, respectively. It can be seen that the active power the level during the fault period (i.e. from t = 0.2s until t=0.4s) at the *VSC B* unit drops to zero for Case A1 and for Case A2 as shown in Figure 6.21a and Figure 6.21c. Next, the active power distribution (during the fault period) is modified within the HVDC link, creating an approximately 500MW boosting (i.e. *VSC A* unit transmitting 688MW) of the active power transferred towards the Onshore AC Network A (c.f. Figure 6.21a., and Figure 6.21c). This active power boosting occurs due to the power balance characteristics associated to the $Droop_{Ctrl}$ (i.e. $K_{droop_{dc}}$ = 0.01) of the *VSC A* unit. Moreover, as the FRT function is activated at the *VSC B* unit, the DC voltage levels in the HVDC link increases w.r.t. the DC voltage levels of *VSC A* unit (during the fault period), as shown in Figure 6.21b and Figure 6.21d.

On the other hand, during the post-fault period (i.e. from t = 0.4 s) relevant differences between the Case A1 and Case A2 can be noticed. Firstly, the active power level in Figure 6.21a is restored after t = 0.8s, exceeding in that way the 200 ms limit for the PFAPR period which was defined in section 6.1. This PFAPR delay in Case A1 occurs because of the inability of the proportional gain of the $Droop_{Ctrl}$ to restore the pre-fault DC voltage level of the *VSC B* unit, as shown in Figure 6.21b. Nevertheless, the non-linear (exponential) DC power modulation (represented by the addition of the $V_{DC_{MOD}}$ shown in by the expression 6.3), can bring back the pre-fault active power level in *VSC B* unit as shown in Figure 6.21c. The restoration of the pre-fault active power $P_{Pre-Fault}$ level in *VSC B* unit is a consequence of the DC voltage reference adjustment driven by $V_{DC_{MOD}}$ (c.f. expression 6.4), which accelerates the DC voltage restoration process as shown in Figure 6.21d. The faster restoration of the DC voltage in *VSC B* unit can be physically understood as the temporal addition of a DC voltage source which contributes to develop the PFPR process during the post-fault period.

6.5.4. Multi-Terminal Operation: Off-Ons Point-to-Point VSC-HVDC Expansion with Droop Control

As described in section 6.11, the multi-terminal expansion of the Off-Ons PtP-VSC-HVDC link is developed by adding an 800MW onshore VSC unit, a DC Chopper, and an onshore AC network. On the other hand, the steady-state power conditions considered for the simulation experiment of this Off-Ons expansion coincides with the DC power flow distribution described in section 6.5.3 as shown in Figure 6.22.

It is relevant to mention that for this particular expansion the Multi-Terminal DC Voltage Controller can modify the DC voltage reference of the onshore VSC-HVDC units, and can provide the $P_{Pre-Fault}$ signals (c.f. section 6.4.3) for the DC choppers in Figure 6.22. Furthermore, the values for the DC power flow controllers (i.e., $K_{droop_{dc}}$) of the *VSC A,* and the *VSC B* units are set to 1% and 5% (as in section 6.5.3), respectively. These DC power flow distributions, and $Droop_{Ctrl}$ characteristics for the multi-terminal expansion of the Off-Ons point-to-point (shown in Figure 6.22) have been considered to assess the DC power chopper controller (i.e. DACi) shown in section 6.4.3. In that respect, the AC voltages, the active power, the DC voltages, and the current through the DC Choppers (described in section 6.4.3) are presented in Figure 6.23.

It can be seen in Figure 6.23b indicates that the AC fault event show in Figure 6.22, occurs at t = 0.2s and it creates an abrupt active power drop at the *VSC C* unit as shown in Figure 6.23a. Unlike, the Ons-Ons expansion of the point-to-point VSC-HVDC link discussed in section 6.5.3, here the MT DC voltage controller can utilize the DC power dissipation capabilities during the fault period (i.e. t = 0.2s to t = 0.4s). If the active power response of the *VSC A* unit in Figure 6.23a is compared against the one in Figure 6.21a (or Figure 6.21c), it can be seen that *VSC A* unit power consumption during the fault period increased approx., 70MW (i.e. *VSC A* unit power consumption = 252MW) during the fault period. This active power level represents a 85% reduction w.r.t. the 500MW increment (i.e. 688MW) generated by the same active power imbalance shown in Figure 6.21a or Figure 6.21c.

The substantial active power reduction occurs since the DC chopper's current (c.f. section 6.4.3) is increased during the fault period as shown in Figure 6.23c. The increment in the DC chopper's current generates a transient DC power consumption within the multi-terminal network that transiently balances the DC power flow distribution as indicated in Figure 6.23a. Besides, the same increment in the DC chopper's current generates a DC voltage decrement in *VSC B* and *VSC C* (c.f. Figure 6.23b), when they are compared with the ones presented in Figure 6.21b. From a physical point of view, the DC voltage decrement occurs since the DC current increment in the activated DC chopper helps to extract the excess of electrostatic charge accumulated in the HVDC cable capacitors during the fault period. By doing so, the electric field within the HVDC cable is reduced and consequently, its associated DC voltage level.

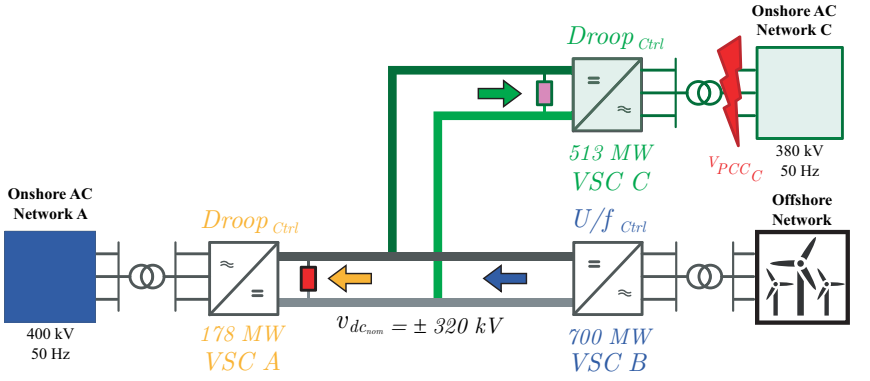

Figure 6.22: The multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.11 describing the steady-state DC power distribution with the coloured arrows and the AC fault at V_{PCC_B}. A DC under-voltage phenomenon is expected if no control actions are executed.

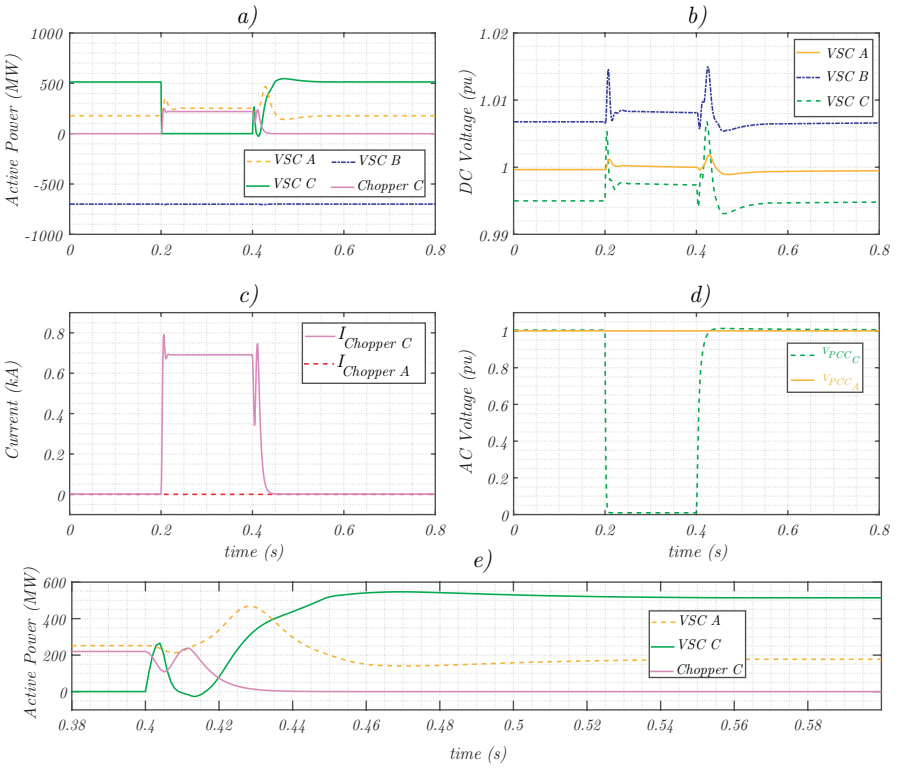

Figure 6.23: Multi-terminal expanded Ons-Ons PtP-VSC-HVDC link shown in Figure 6.22 experiencing an AC fault (t = 0.2 s) at V_{PCC_C} while *VSC C* unit working with $Droop_{Ctrl}$ at 5%. MT DC Voltage Controller using DC Chopper (from *VSC C* unit) to dissipate power during the fault period (c.f. section 6.4.3, and 6.4.5 section).

Interestingly, during the PFAPR period, the pre-fault active power level transmitted towards the Onshore AC Network C is restored within 200ms as shown in Figure 6.23a, and (in more detail) in Figure 6.23e. At the beginning of the post-fault period (i.e. t = 0.4s), the active power regulation of the *VSC C* unit is bounded by the active and reactive current prioritization discussed in section 3.4. Consequently, the DC Chopper of the *VSC C* unit attempts to compensate the change in the active power of the *VSC C* unit. This active power compensation is performed with certain delay (as seen in Figure 6.23e) mainly due to the time constant T_{ch} (c.f. section 6.4.3). It can be seen that from t = 0.41s, the DC chopper power dissipation starts to decrease, while the active power provided to the onshore AC network C is progressively increased. Furthermore, the active power transmitted towards the onshore AC network A is also increased during the same time period as shown in Figure 6.23e. During 20ms (i.e., from t = 0.42 to t = 0.44), the amount of active power transmitted towards both onshore networks exceeds the power introduced by *VSC B* unit. This occurs since the electrostatic energy accumulated within the multi-terminal network, needs to be reduced to restore the pre-fault DC voltage levels across the VSC-HVDC link. Hence, the $Droop_{Ctrl}$ at *VSC A* unit progressively adjust the amount of active power sent to onshore network A while the MT DC voltage controller use the $V_{dc_{MOD}}$ to progressively restore the active power transmitted towards the onshore network C.

6.5.5. Multi-Terminal Operation: Off-Ons Point-to-Point VSC-HVDC Expansion with DC Voltage and Active Power Control

Alike section 6.5.4, the steady-state power conditions presented in Figure 6.24 are referred to the multi-terminal expanded Ofs-Ons point-to-point system shown in Figure 6.11. However, it is relevant to remember that for this particular Ofs-Ons point-to-point expansion, the Multi-Terminal DC Voltage Controller cannot modify the DC voltage references of any of the onshore VSC-HVDC units. Consequently, the *VSC A* unit keeps controlling the DC voltage across the HVDC link, while the added *VSC C* unit is setup to regulate the active power level transmitted towards the Onshore AC Network C as shown in Figure 6.24. Thus, the analysis of the multi-terminal expanded Ofs-Ons point-to-point VSC-HVDC link will be developed by considering two DC power flow scenarios. The first scenario will be described as *Case 1*, and the second scenario will be described as *Case 2*.

Case 1

Figure 6.24 presents the first power flow scenario in which 600MW are transmitted by the *VSC C* unit towards the Onshore AC Network C. At the same time, the offshore *VSC B* unit supplies 450MW, while the *VSC A* unit absorb approximately 150MW form the Onshore AC Network A, to maintain the DC Voltage level (i.e. DC power balance) across the multi-terminal HVDC network. The particular DC power flow scenario shown in Figure 6.24 has been chosen to demonstrate the potential risk of having a DC collapse problem when a three-phase fault occurs at the Onshore AC Network A. Nevertheless, due to the exponential function (c.f. section 6.3.2)

implemented within the P_{Ctrl} of the *VSC C* unit, the AC/DC power imbalance at *VSC A* unit can be mitigated as shown by Figure 6.25.

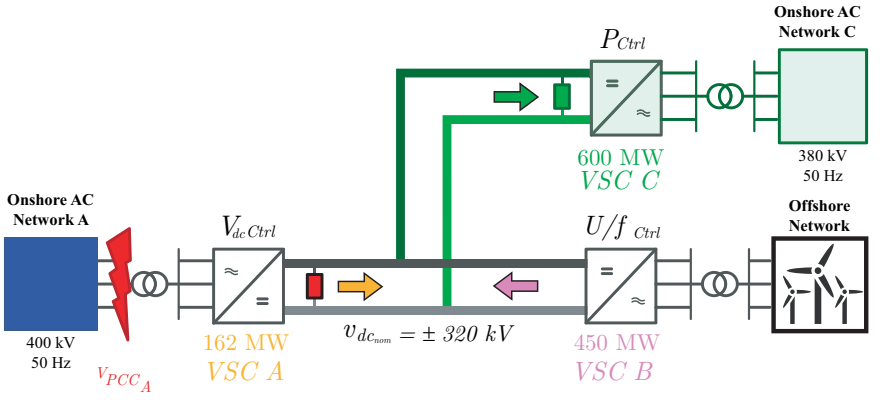

Figure 6.24: Steady-state DC power distribution for the multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.11 experiencing an AC fault at V_{PCC_A}. Risk of DC under-voltage (collapse) if non-control actions developed.

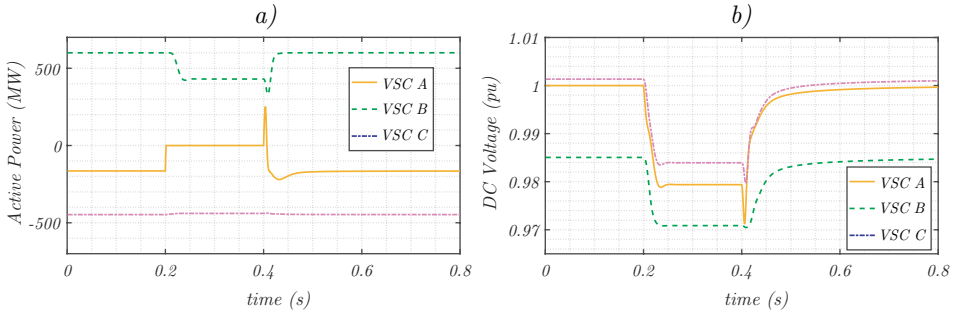

Figure 6.25: Multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.24 experiencing an AC fault (t = 0.2 s) at V_{PCC_A} while *VSC A* unit working with Vdc_{Ctrl}. The DC voltage collapse is avoided by the *VSC C* unit based on the exponential control described in section 6.3.2.

First, the drop in the active power (c.f. Figure 6.25a) leads to the FRT activation at *VSC A* unit, blocking in that way its DC voltage regulation function. Next, the blocking of the DC voltage regulation function, generates a drop in the DC voltage across the multi-terminal VSC-HVDC system. Consequently, the mitigation of the AC/DC power imbalance is generated by the adjustment of the active power transmitted towards the Onshore AC Network C.

The active power adjustment is performed by the modulation term λ_{MOD} of the P_{Ctrl} in *VSC C*, and then, it stabilizes the DC voltage (c.f. Figure 6.25b) at the LVT value (i.e. 0.97 pu) as described in section 6.3.2. It can be noticed that, during the fault period, (i.e. from t= 0.2s to t=0.4s), the active power reduction at the *VSC*

C unit closely coincides with the one provided by the offshore *VSC B* unit, demonstrating a full DC power redistribution between them. This redistribution effectively demonstrates that the proposed exponential function can be utilized in an expanded Ofs-Ons point-to-point HVDC link to support the DC voltage and (consequently) balance the DC power flow without using frequency domain controllers.

On the other hand, it is convenient to remember, that the active power modulation induced by the exponential function is designed to avoid the collapse of the DC voltage in a HVDC link. However, depending on the type of control mode used by the affected VSC-HVDC unit, and the (pre-fault) multi-terminal steady-state DC power flow conditions across the link, it might be possible to observe a DC over-voltage phenomenon.

Case 2

Figure 6.26 presents the second power flow scenario in which 200MW are transmitted by the *VSC C* unit towards the onshore AC network C. Additionally, the offshore *VSC B* unit supplies 450MW to the multi-terminal HVDC network. Furthermore, the *VSC A* unit (using $V_{dc_{Ctrl}}$) balance the DC power flow in the multi-terminal HVDC network by transmitting 246MW towards the Onshore AC Network A. If (as indicated in Figure 6.27d) a 200ms three-phase fault occurs at V_{PCC_A} then, an AC/DC power imbalance at the *VSC A* unit will occur as shown in Figure 6.27a. The AC/DC power imbalance occurs at t = 0.2s, and it will cause a rise in the DC voltage since the exponential function implemented in the P_{Ctrl} of the *VSC C* unit has only been designed to reduce the active power transmission towards the Onshore AC Network C when a DC Voltage drop occurs. However, the DC Chopper electrically close to the *VSC A* unit operates generating the DC voltage ripples across the multi-terminal network as shown in Figure 6.27b. The DC voltage ripples appears since for this DC over-voltage simulation experiment, the DC chopper is modelled using the DC chopper control approach indicated in [7], where the insertion and the extraction of the DC chopper's resistor are developed based on a piecewise function. The activation DC voltage limits of the piecewise function were setup to 1.03pu and 1.05 respectively.

It can be notice that although the DC voltage is certainly bounded within the DC voltage limits defined by the piecewise function, the active power level is maintained constant at the *VSC C* unit. Consequently, the DC power fluctuations associated to the DC voltage ripples are dissipated in the DC chopper. On the other hand, it can also be seen that during the post-fault period (i.e. t > 0.4s) the active power at the *VSC A* unit is restored in approximately 100ms (c.f. Figure 6.27a).

The DC current waveform of the DC chopper is shown in Figure 6.27c, and it is generated by the switching actions defined by the piecewise function in [7]. By contrast, Figure 6.28 shows the same simulation experiment but considering the DACI concept (proposed in section 6.4.3) instead of the approach presented in [7]. It can be seen that the DC voltage ripples in Figure 6.27b generated by the control

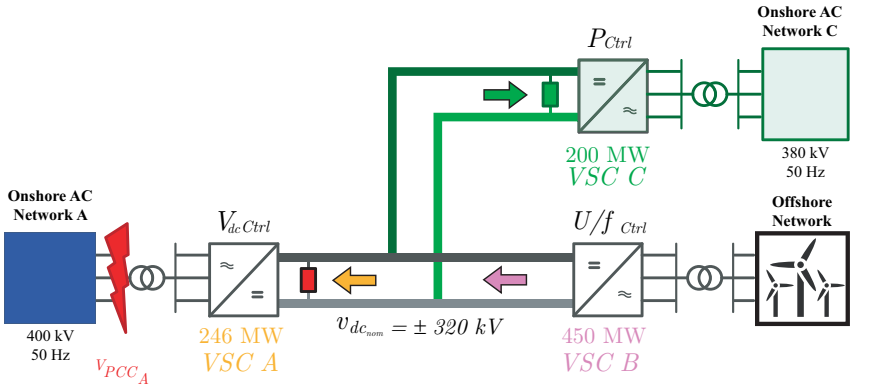

Figure 6.26: Steady-state DC power distribution for the multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.11 experiencing an AC fault at V_{PCC_A}. Risk of DC Over-voltage if non-control actions developed.

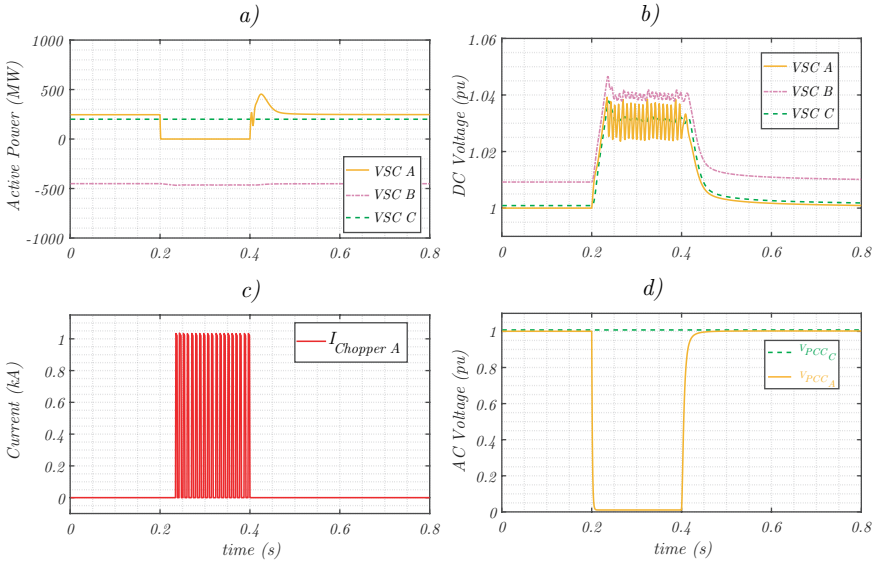

Figure 6.27: Multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.26 experiencing an AC fault (t = 0.2 s) at V_{PCC_A} while *VSC A* unit working with Vdc_{Ctrl}. The DC over voltage issue is tackled by utilizing a DC chopper based on the control approach defined in [7].

concept in [7], can be eliminated if the DC chopper based on the DACI concept is implemented. It can be seen that the proposed DACI concept generates a lower and more smoother DC current profile for the DC Chopper (c.f. Figure 6.27c), and consequently, the DC voltage ripples disappear in the multi-terminal expanded Off-Ons point-to-point systems presented in Figure 6.26. The enhancement in the DC voltage profile across the multi-terminal network is an interesting feature that can

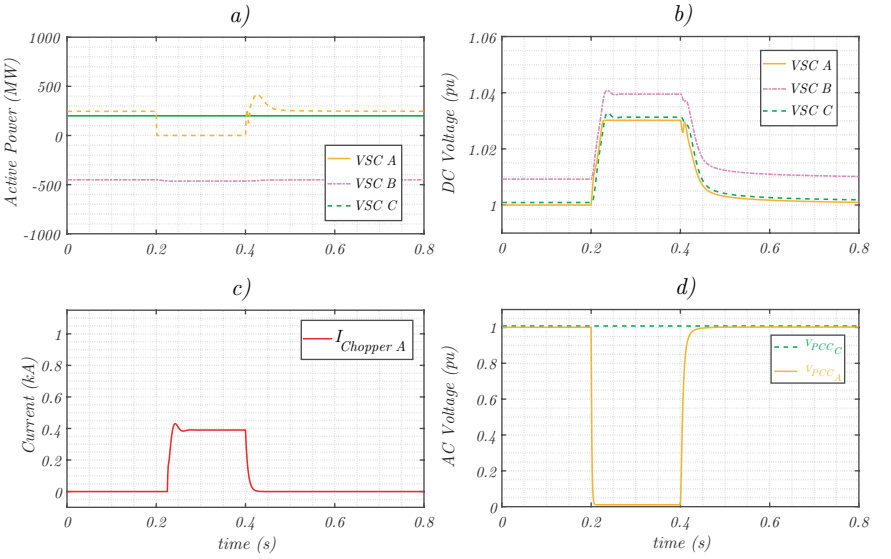

Figure 6.28: Multi-terminal expanded Off-Ons PtP-VSC-HVDC link shown in Figure 6.26 experiencing an AC fault (t = 0.2 s) at V_{PCC_A} while *VSC A* unit working with Vdc_{Ctrl}. The DC over voltage issue is tackled by utilizing a DC chopper based on the proposed DACI concept presented in section 6.4.3.

be potentially used in multi-vendor multi-terminal HVDC links to facilitate the DC power flow regulation under AC/DC power imbalance events.

6.6. Conclusions

In this chapter, several post-fault active power recovery (PFAPR) methods for a multi-terminal expandable point-to-point (PtP) VSC-HVDC link have been proposed based on a non-linear DC power modulation strategy. The strategy is aligned to cooperatively work with the low voltage (fault) ride through (FRT) function and it is also aligned with the national PFAPR European requirements for VSC-HVDC links. The implications of expanding a PtP-VSC-HVDC link are discussed to give insight into the ways in which the non-linear DC power modulation strategy can be implemented when the modification of the DC voltage reference (in the VSC units conforming to the expandable system) is enabled or not. Moreover, it has been found that for the PtP-VSC-HVDC links, the strategy proposed effectively alters the DC power flow in order to maintain (within an acceptable LVT 3% range) the DC voltage levels in the HVDC link, even if the DC_{Ctrl} mode is blocked (in the rectifier VSC unit) during the activation of the FRT function.

In terms of the multi-terminal expanded VSC-HVDC links (allowing the modification of its DC voltage references), the non-linear DC power modulation strategy exhibits a superior performance in terms of the PFAPR requirements when it is compared against a conventional $Droop_{Ctrl}$ method. However, when the multi-terminal expansion of point-to-point VSC-HVDC links does not contemplate the modification of the DC voltage references of their VSC units, the effectiveness of the non-linear DC power modulation strategy is subjected to the power flow conditions in the HVDC system before the three-phase fault occurs. This power flow dependency constitutes a limitation of the proposed exponential method (that occurs only if the modification of the DC voltage reference is not allowed), which can be easily overcome if a DC chopper is installed to protect the HVDC system against potential over voltages risks. Nevertheless, the installation of a DC chopper constitutes a costly solution that partially limits the increment in the DC voltage level in the HVDC system during the fault period. Consequently, a transient boosting in the active power transmitted by the affected VSC unit is generated during the post-fault period in order to comply with the time restrictions associated to the PFAPR requirements. The extension of the exponential DC power modulation strategy for tackling overvoltage risks during fault periods in the VSC-HVDC system is suggested for a future work.

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7

Optimal Tuning of the Active Power Control of PtP-VSC-HVDC links Providing Frequency Support

This chapter describes a tuning criterion, based on several mathematical formulations utilized by an optimization algorithm for establishing the predefined APG and active power reference values in a PtP-VSC-HVDC link. The tuning criterion will help to demonstrate the feasibility of enabling a balanced participation of the primary frequency resources between synchronous decoupled AC networks connected through a PtP-VSC-HVDC link during a power imbalance event in one AC network. The proposed mathematical formulations are evaluated in terms of (1) their applicability, (2) their effectiveness based on the availability of active power reserve, (3) their optimization convergence rate and the suitability of the frequency response obtained after performing a series of RMS simulations on a modified low-inertia two area benchmark system utilizng DIgSILENT PowerFactory coupled with a Python-based optimization solver that uses the mean variance mapping optimization (MVMO) algorithm.

7.1. Frequency Control in PtP-VSC-HVDC Links

A PtP-VSC-HVDC link is capable of providing frequency support to low inertia AC networks experiencing a power imbalance, when the proposed frequency control (f_{Ctrl}) described in section 3.3 is implemented as part of the supplementary controls of a VSC-HVDC link. The idea behind the proposed f_{Ctrl} is to utilize a triggering signal to set off the deployment of active power in a VSC-HVDC link based on a predefined selection of the amount of active power to be changed, and the active power gradient (APG) value to be used by the PtP-VSC-HVDC link during a frequency disturbance. In that sense, the proposed f_{Ctrl} was implemented in a PtP-VSC-HVDC link located within the modified version of the two-area, four-machine benchmark system (illustrated in Figure 7.1), under the operating conditions presented in Table 7.1.

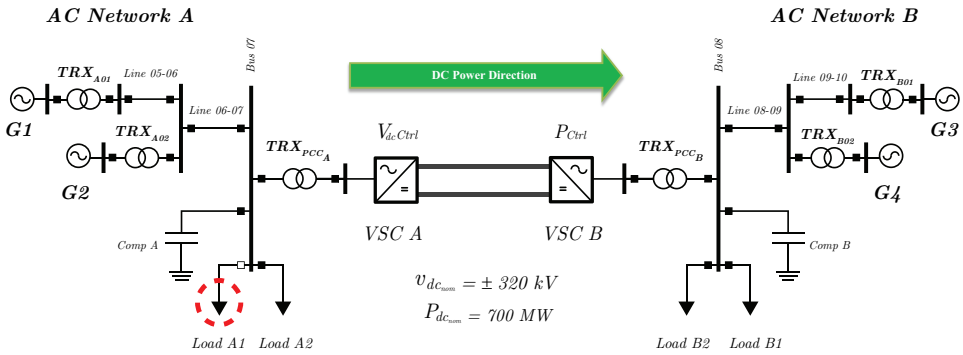

Figure 7.1: Modified benchmark two area power system derived from [1].

Table 7.1: VSC unit and AC networks data

Power Balance	Network Element	Load Flow Conditions (MW)	Inherent Inertia (s)
Generation on AC Network A	G1	700	6.5
	G2	700	6.5
Demand on AC Network A	Load A1	250	N.A.
	Load A2	717	N.A.
	VSC A	400	N.A.
Generation on AC Network B	G3	719	6.175
	G4	700	6.175
	VSC B	381.6	N.A.
Demand on AC Network B	Load B1	250	N.A.
	Load B2	1517	N.A.

Furthermore, Figure 7.1 shows that the PtP-VSC-HVDC link establishes a connection between the synchronously decoupled AC networks. As described in [1], these AC networks are prone to appreciable frequency deviations due to the re-

duced amount of sources of kinetic energy and the weak coupling associated with the initially long AC transmission line connecting both AC networks. Figure 7.1 also shows that a sudden load disconnection (i.e., in Load A1) occurs in AC network A. As shown in Table 7.1, the disconnection of Load A1 represents an 18% power imbalance in AC network A, which is within the 20% criterion utilized in [2] to perform frequency stability analysis in the context of an RMS simulation. On the other hand, as the inertia levels of the AC networks are approximately the same, modifying the active power in the PtP-VSC-HVDC link during the power imbalance will influence the extent of participation of the primary frequency resources of both AC networks. Consequently, a criterion for determining the level of adjustment needed for the proposed f_{Ctrl} (c.f. section 3.3) must be formulated to enable a balanced participation of the primary frequency resources of the AC networks coupled by a PtP-VSC-HVDC link, during power imbalance conditions.

7.2. Optimal Tuning of f_{Ctrl} Parameters

The parameters adjustment criterion for the proposed f_{Ctrl} consist on formulating two independent cost functions and assessing them through an optimization methodology implemented in Python 3.6. The formulation of these two independent cost functions is defined in such a way as to balance the participation of the primary frequency resources of both AC networks, as discussed in section 7.2.1 and section 7.2.2 respectively.

7.2.1. Problem Formulation 1

The occurrence of an active power imbalance triggers the dynamic behaviour of the synchronous generators in operation, and this leads to a variation of the electrical frequency within the synchronous area to which the generators belong. However, as Figure 7.1 shows, AC networks A and B are connected by a PtP-VSC-HVDC link, which means that there is no electromagnetic coupling between them. For that reason, the first problem formulation proposes a cost function A (i.e. CFA) which seeks to establish a *virtual electromagnetic coupling* between AC networks A and B, by adjusting the active power reference and the APG level of the PtP-VSC-HVDC link. This, *virtual electromagnetic coupling* is achieved by performing simulation experiments under an RMS simulation framework in DIgSILENT PowerFactory 2019, where the difference between the areas associated to the square of the electrical frequencies is minimized. Therefore, the optimization problem for CFA is defined as shown in 7.1.

Minimize:

$$CFA(\mathbf{x}^{CFA}) = \int_0^{\tau} \left[\rho_1 \left((yi(\mathbf{x}^{CFA}) - y_{1_{ref}} \right)^2 + \cdots + \rho_n \left((y_n(\mathbf{x}^{CFA}) - y_{n_{ref}} \right)^2 \right] dt \quad (7.1)$$

Subject to:

$$\mathbf{x}_{min}^{CFA} \leq \mathbf{x}^{CFA} \leq \mathbf{x}_{max}^{CFA} \tag{7.2}$$

Where ρ_i is a weight factor (assumed to be 1 in 7.1 due to the fact that all controlled generators of the studied test system have similar parameters). Moreover, y_i constitutes the instantaneous frequency on the AC side of the VSC station with the APG functionality activated, and y_{ref} is defined as the nominal frequency value of the synchronous area. The optimization vector $\mathbf{x}^{CFA}$ is defined in 7.3, and its elements (i.e., the optimization variables) are named APG_{VSC} and ΔP_{VSC}.

$$\mathbf{x}^{CFA} = [APG_{VSC}, \Delta P_{VSC}] \tag{7.3}$$

The bounds of the optimization variables are taken from [3] and are presented in 7.4 and 7.5

$$1\frac{MW}{min} \leq APG_{VSC} \leq 60\frac{MW}{min} \tag{7.4}$$

$$0 \leq \Delta P_{VSC} \leq P_{VSC_{Rated}} \tag{7.5}$$

The expression in 7.1 constitutes an attempt to equalize the change in the rotational energy of the synchronous generators of AC network A and B, shown in Figure 7.1 when an active power imbalance occurs. Concretely, once the active power imbalance generated by the disconnection of Load A1 in Figure 7.1 occurs, the adjustment of optimization vector $\mathbf{x}^{CFA}$ will influence the evolution of the electrical frequency from both AC networks. In that sense, Problem Formulation CFA constitutes a tool for assessing the frequency stability of two AC networks coupled by a PtP-VSC-HVDC link.

7.2.2. Problem Formulation 2

The second problem formulation utilizes a geometrical approach based on the instantaneous frequency responses (i.e. w_i) of each AC network connected to the PtP-VSC-HVDC link as described by expression 7.6.

$$A(t) = w_1(t) \cdot w_2(t) \tag{7.6}$$

During steady-state operation, the instantaneous area $A(t)$ shown in 7.6, is assumed to be constant. On the other hand, during a power imbalance event, the changes associated to $A(t)$ can be mathematically described based on 7.7.

$$\frac{dA(t)}{dt} = w_1(t) \cdot \frac{dw_2(t)}{dt} + w_2(t) \cdot \frac{dw_1(t)}{dt} \tag{7.7}$$

In electromagnetically coupled AC networks, the electrical frequencies w_i shown in 7.6 and 7.7 are synchronized. This implies that the instantaneous area $A(t)$ describes a symmetrical four-sided polygon (i.e. a square) for electromagnetically coupled AC networks. However, when AC networks are not electromagnetically synchronized, and one of them is affected by an active power imbalance, the change

in the dimensions of the four-sided polygon (described by $A(t)$) will not necessarily be symmetrical. Consequently, a cost function B (i.e. CFB) capable of minimizing the changes in the dimensions of the four-sided polygon is described as shown in 7.8.

$$CFB(\mathbf{x}^{CFB}) = \frac{dA(t)}{dt} \tag{7.8}$$

The minimization process for CFB is also intended to balance the changes in the dimensions of the four-sided polygon subjected to 7.9 and 7.10.

$$\frac{dw_1(t)}{dt} = \frac{dw_2(t)}{dt} \tag{7.9}$$

$$\mathbf{x}_{min}^{CFB} \leq \mathbf{x}^{CFB} \leq \mathbf{x}_{max}^{CFB} \tag{7.10}$$

The optimization vector for $\mathbf{x}^{CFB}$ is formed by the variables APG_{VSC} and ΔP_{VSC} (i.e. $\mathbf{x}^{CFB} = \mathbf{x}^{CFA}$, c.f. 7.3), and utilizes the same boundary conditions described in 7.4 and 7.5.

7.3. Optimization Process: Description of the MVMO Algorithm

The methodology for obtaining the optimization variables (i.e. minimizing the cost functions) presented in section 7.2 (i.e. APG_{VSC} and ΔP) is based on the mean-variance mapping optimization (MVMO) algorithm. The MVMO algorithm has been selected due to the high convergence rate and the high-quality results it has achieved in other complex optimization problems concerning electrical power systems [4, 5]. In this connection, a graphical representation of the influence of the MVMO algorithm over the frequency control strategy presented in section 3.3.1 is shown in Figure 7.2. The resolution of the optimization problems formulated in section 7.2 implies the use of the application program interface of DIgSILENT PowerFactory 2018 which enables the integration of Python 3.6 for automating the management of the simulation experiments.

Thus, a Python script was written to gather and process, information regarding the dynamic responses of the electrical frequencies of the AC networks shown in Figure 7.1 under the conditions described in Table 7.1. The Python script is also responsible of automatically executing the RMS simulation experiments with the modified APG_{VSC} and ΔP values, which are generated by a dedicated Python MVMO Library. A complete flowchart of the routines followed by the MVMO algorithm is shown in Figure 7.3.

Basically, the MVMO algorithm generates an evolving offspring solution by performing a series of iterations based on the best parent solution achieved throughout the process, and on the statistical data representing the evolutionary direction of

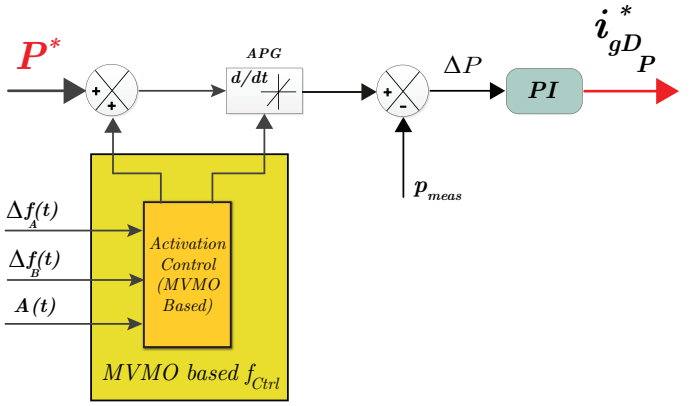

Figure 7.2: Optimization block altering the active power reference P^*, and the APG level of the active power controller P_{Ctrl} of a point-to-point VSC-HVDC link.

the optimum solution used by a mapping function for each of the mutated optimization variables. Initially, it performs the first iteration based on an initial optimization vector **x0**, either provided by the user or randomly calculated within the algorithm. Then, the candidate optimization variables are applied in the corresponding elements in DigSILENT 2018, and an RMS simulation is executed to obtain the frequency time series of interest.

The results of this simulation are stored in a comma-separated value (csv) file, in a Python-readable format, and are used to perform the fitness evaluation. Then, several iterations are performed, with the solution vector evolving based on the candidate vectors that have achieved the best fitness evaluations, and the guidelines of a mapping function until the termination criterion are thus fulfilled. For this purpose, an file with a constant size stores the best optimization vectors, along with the statistical data, for each of the optimization variables. Also, the algorithm generates the offspring solutions in a normalized [0,1] range, thus always respecting the boundaries of the optimization variables and avoiding penalties and modifications at a later stage [4]. In this analysis, the termination criterion selected corresponds to a number of 200 fitness evaluations.

7.4. Numerical Results

As indicated in Chapter 3 (section 3.3.2), the frequency support provided by the PtP-VSC-HVDC link shown in Figure 7.1, is studied considering a modified version of the two-area four machine benchmark system presented in [1], where a load shedding event occurs, generating an 18% power imbalance in AC network A.

In the original two-area, four machine benchmark system (presented in section 3.3.3), it was shown that due to the existing electromagnetic coupling (tie-lines) between both AC networks, the generators units were able to stay synchronized

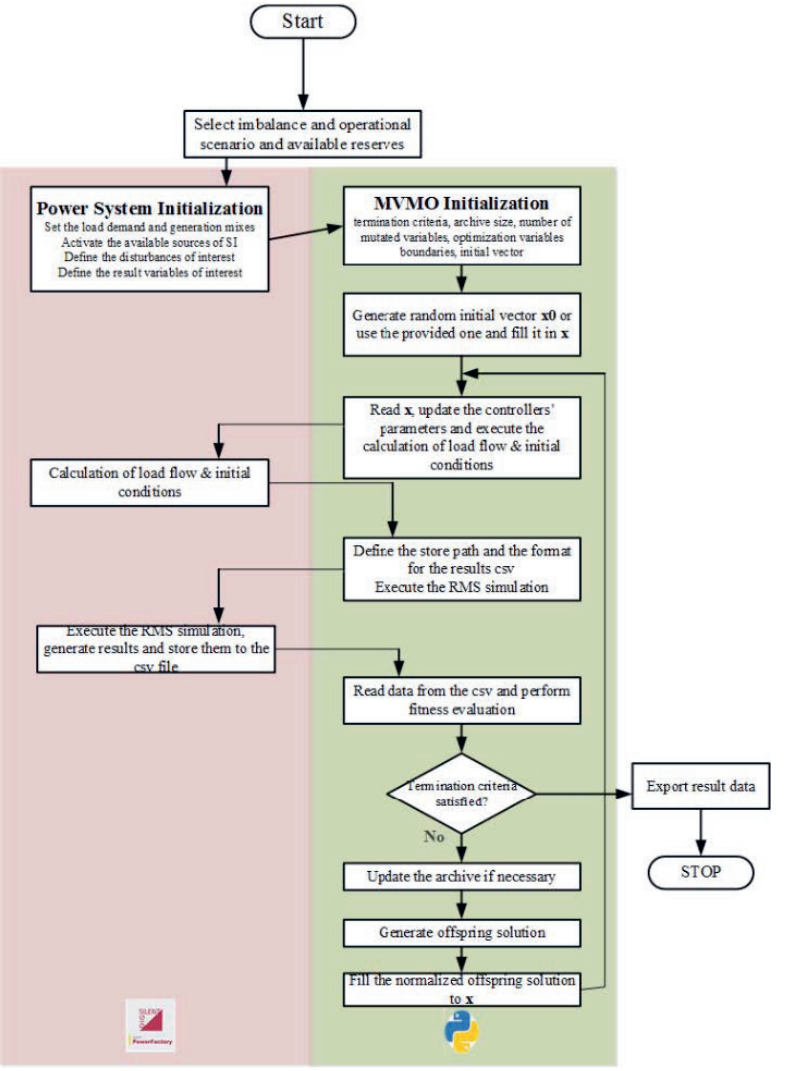

Figure 7.3: The mean variance mapping optimization (MVMO) algorithm process.

and to react simultaneously to the power imbalance generated by the disconnection of Load A1 at t = 1 s. The reaction of the AC networks was characterized by a homogeneous response from the primary frequency resources (i.e. governors systems) of the generator units, leading to a reduction in their corresponding active power levels.

Furthermore, as the replacement of the tie-lines with the PtP-VSC-HVDC link shown in Figure 7.1 leads to the loss of the electromagnetic coupling between the AC networks, the deployment of their primary frequency resources might not be

homogeneous during a power imbalance event. For that reason, as described in section 3.3.3, the selection of the ΔP and APG_{VSC} values would strongly influence the participation of the primary frequency resources of both AC networks during the power imbalance event. As shown in Figure 7.4, if the APG_{VSC} is set to an emergency value (e.g. 60 GW/min c.f. [3]) and the ΔP value is identically set to the power imbalance generated in AC network A (i.e. 250 MW), neither the electrical frequencies nor the deployment of the primary frequency resources of both AC networks would be balanced.

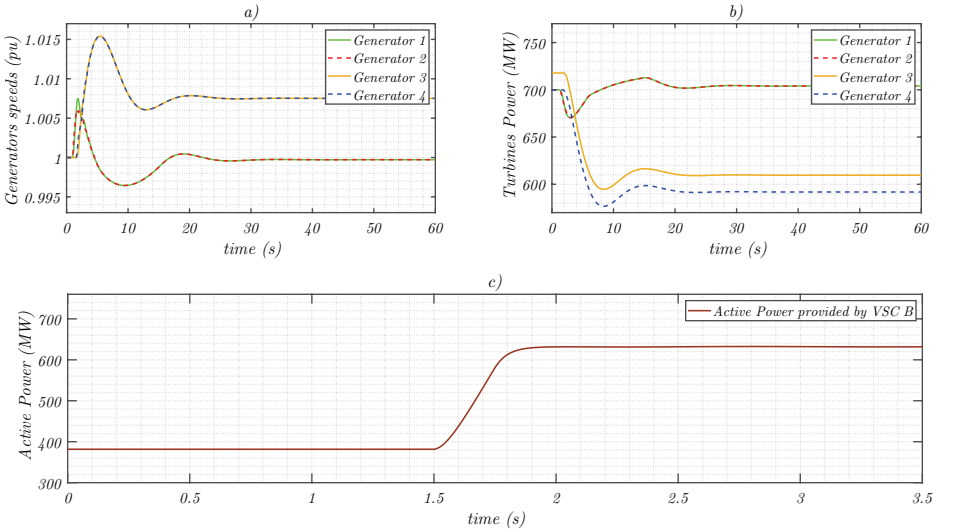

Figure 7.4: Simulation experiment corresponding to the f_{Ctrl} described in section 3.3 when the 18% load outage shown in Figure 7.1 occurs. a) Generators speeds after the VSC-HVDC link provides 250MW at 60GW/min. b) Generators active power deployment after the VSC-HVDC link provides 250MW at 60GW/min. c) Active power of the VSC-HVDC link provided after 500ms of the power imbalance event.

On the other hand, when the optimization algorithm (i.e. MVMO) is used to solve the problem formulation expressed by cost function A (i.e. CFA in section 7.2), the electrical frequency responses and the deployment of the primary frequency resources by both AC networks are substantially different, as presented in Figure 7.5. Figure 7.5 shows that the responses associated to the electrical frequencies, as well as the active power produced by the synchronous generators, are identical during the steady-state condition reached after the power imbalance. Moreover, it is interesting to notice that amount of ΔP is relatively shorter (i.e. 134 MW) when compared with the 250 MW used for the previous simulation experiment. A similar finding was observed when comparing the APG_{VSC} value obtained for this simulation experiment (i.e. approx. 28GW/min c.f. Figure 7.5) against the previously used emergency APG_{VSC} value (i.e. 60 GW/min). Thus, it is noticed that, by utilizing the MVMO algorithm, the generators' powers and the electrical frequencies of the AC networks present a more homogeneous response which is a consequence

of a balanced deployment of the primary frequency resources by both AC networks.

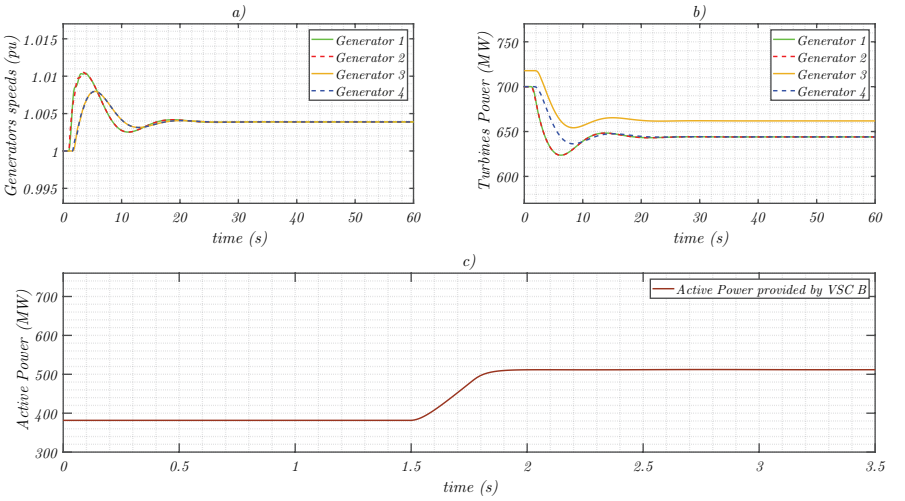

Figure 7.5: Simulation experiment corresponding to the MVMO based f_{Ctrl} using the problem formulation 1 described in section 7.2.1. a) Generators speeds after the VSC-HVDC link provides 134MW at 28GW/min. b) Generators active power deployment after the VSC-HVDC link provides 134MW at 28GW/min. c) Active power of the VSC-HVDC link provided after 500ms of the power imbalance event.

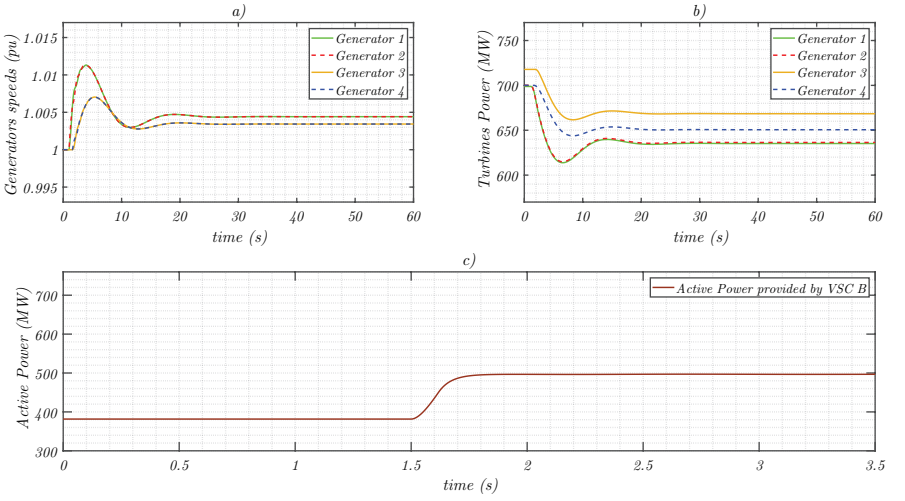

Figure 7.6: Simulation experiment corresponding to the MVMO based f_{Ctrl} using the problem formulation 2 described in section 7.2.2. a) Generators speeds after the VSC-HVDC link provides 115MW at 57,5GW/min. b) Generators active power deployment after the VSC-HVDC link provides 115MW at 57,5GW/min. c) Active power of the VSC-HVDC link provided after 500ms of the power imbalance event.

Interestingly, the results shown in Figure 7.5 constitute the time response asso-

ciated to the solution of the minimization process of CFA (that is, the total average change in the rotational energy of both AC networks generated by the shedding of Load A1). Hence, cost function B (CFB), described in section 7.2.2, incorporates the characteristics of the RoCoF of both AC networks as a boundary condition for the equalization of the response of the electrical frequencies during the deployment of the primary frequency responses, instead of the minimization of the total average change in rotational energy, as was done in CFA. Thus, the results obtained by the optimization process for CFB are 58,5 MW/min and 115 MW for the APG_{VSC} and ΔP respectively, and the associated time responses are presented in Figure 7.6.

Furthermore, Figure 7.6 shows that the dynamic responses of the synchronous generators in terms of the electrical frequency (i.e., the speed of the generators) and of the power supplied are essentially different compared them against the results presented in Figure 7.5. More precisely, during the dynamic period (i.e. from t = 1 s to t = 20 s), the speed reponses from the generators in AC networks A and B (shown in Figure 7.6) present a closer alignment pattern in relation to one another, instead of the one shown in Figure 7.5. The initial differences observed between the speeds of the generators in AC networks A and B (shown in Figure 7.6a), essentially occurs due to the delay associated to the execution of the frequency support strategy described in section 3.3.3. On the other hand, during the steady-state period, the generators' speeds, shown in Figure 7.5a, present a closer alignment pattern in relation to one another, instead of the one shown in Figure 7.6a.

These results indicate that the use of the proposed cost functions CFA and CFB can produce sufficiently close alignment patterns for the speeds of the generators in AC networks A and B, as to mimic the dynamic response observed when both AC networks are connected by transmission lines as shown in section 3.3.3. This analysis also entails that, depending on whether the CFA or the CFB formulation is used, either the steady-state or the dynamic *virtual electromagnetic coupling* characteristics can be obtained for the frequency support of AC networks coupled through a PtP-VSC-HVDC link, during a power imbalance event. Furthermore, the selection of the cost function must be established based on several factors associated to the particular characteristics of each AC network, such as the inertia levels, the maximum allowed RoCoF, the availability of primary frequency resources, the congestion levels in the transmission network, and the time constants associated to the speed control (i.e. governor system) of the synchronous generators.

7.5. Conclusions

This chapter, described an optimal tuning of the active power control of a PtP-VSC-HVDC link providing frequency support to low inertia AC networks. The optimal tuning process proposes two different cost functions based on the rate of change of frequency, and the total average change of the rotational (kinetic) energy corresponding to the synchronous generators in each AC network. Furthermore, the mean-variance mapping optimization (MVMO) algorithm was utilized to solve the

proposed cost functions, considering an optimization vector formed by the active power deviation and the active power gradient needed when a disturbance producing an 18% active power imbalance occurs at one of the AC networks connected by the PtP-VSC-HVDC link.

In general, the results obtained indicated that the adjustment of the active power control variables in the optimization vector leads to an homogeneous participation of the primary frequency resources (within the AC networks coupled by the HVDC link), similar to the one observed between electromagnetically coupled AC networks which are affected by the same type of power imbalance event. Thus, the optimal active power control tuning can be perceived as a method that allows the establishment of a *virtual electromagnetic coupling* between AC networks connected by a PtP-VSC-HVDC link. More precisely, the level of *virtual electromagnetic coupling* achieved is analyzed by examining the alignment characteristics of the generators' speeds (i.e. the electrical frequencies of both AC networks) during and after the power imbalance. In that sense, the solutions obtained for the proposed cost functions produced different types of alignment characteristics between the electrical frequencies of the AC networks (connected by the PtP-VSC-HVDC link), which were mainly noticed in either the dynamic period or the steady-state period following the power imbalance event. This entails that a PtP-VSC-HVDC link can support (by considering the formulated cost functions) the frequency stability of the asynchronous AC networks connected to it, by acting as transmission line in which a *virtual electromagnetic coupling* is developed by inducing a dynamic or steady-state alignment between the generators' speeds at each AC network. On the other hand, further research is devoted to the applicability of this method for the frequency stability assessment of low inertia power system connected by multiple PtP-VSC-HVDC links and considering different AC network scenarios.

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8

Conclusions

This thesis proposes modelling upgrades of the active and the reactive power controllers of symmetrical monopole VSC-HVDC links represented within a RMS simulation framework. Additionally, new control principles are proposed to support the active power recovery process, and the quasi-stationary voltage response of VSC-HVDC links operating under a point-to-point or a three-terminal (multi-terminal expanded) network configuration. The focus of the analysis is on the performance during steady-state and faulted operating conditions. Furthermore, two new primary frequency support methodologies for point-to-point VSC-HVDC links are presented based on two perspectives: the optimization of the parameters of the active power control, and the integration of the power line communication principle.

8.1. Answer to Research Questions

The answers for the research questions presented in Chapter 1 are given below.

What modelling developments (upgrades) are needed to properly capture the active and reactive power grid support by expandable VSC-HVDC units?

Three essential upgrades were proposed and analyzed in Chapter 3. The first upgrade is shown in Chapter 3.2, and it is concerned with the addition of a supplementary reactive power control mode that enables the dynamic regulation of the power factor (PF) performed by a VSC-HVDC unit. The dynamic regulation was studied by proposing a PF-P diagram in which the non-linear characteristics of the power factor control were defined as a function of the desired power factor reference and the P-Q power limits of a VSC-HVDC unit during steady-state operation. Moreover, numerical simulations showed that the quasi-stationary AC voltage support provided by the power factor control is negligible when the supplied active power is lower than a low bound (e.g. 5%) of the nominal power of the VSC-

HVDC unit. Therefore, the PF-P diagram can be utilized to define an active power dead-band, where the PF control is disabled by keeping the level of reactive power supplied by the VSC unit constant. Lastly, the obtained results indicate that the use of particularly low (e.g. 0.64) inductive power factor set-point can collaterally lead to an undesirable drop (e.g. higher than 3% of the nominal voltage) in the quasi-stationary voltage profile in the surrounding bus bars of the AC network. The latter finding is especially critical when an active power reversal action (i.e. by following a linear adjustment of the active power) is carried out by the VSC-HVDC unit.

The second VSC-HVDC modelling upgrade focused on the design of a frequency control f_{Ctrl} mode capable of providing frequency support during severe power imbalances (i.e. 18% power system's load shedding) was proposed as described in Chapter 3.3. Essentially, the f_{Ctrl} mode is based on a control logic that defines the slope of the active power gradient (APG), and the set-point of the active power reference in the active power controller in a point-to-point (PtP) VSC-HVDC link. Besides, it was considered that the PtP-VSC-HDC link is used to interconnect two electrical areas of a modified benchmark power system, which are characterized by low equivalent inertia constants (i.e. H<7s), and similar power generation levels (i.e. approximately 700MW per synchronous machine). During the computer-aided RMS simulation of an 18% load shedding event in one of the areas, the control logic of the proposed f_{Ctrl} mode is activated considering a 500mHz/s threshold. Next, as a challenging example to illustrate the effectiveness of the controller under large active power imbalances, the selection of the set-point of the active power reference was defined to be equal to the level of power imbalance generated by the load shedding event, to concentrate the study of the proposed f_{Ctrl} on the APG adjustment of the PtP-VSC-HDC link.

The study of the APG was carried out by performing a sensitivity analysis which showed that the load-shedding event generates a frequency zenith (i.e., an over-frequency issue) of 1.02pu and a steady-state frequency deviation of 1.008pu in the affected area when the APG value is defined as 0 MW/min. On the other hand, if an emergency APG value (i.e. 60000MW/min) is used, the frequency response in the affected area experiences an effective reduction (i.e. 50%) in the zenith level (i.e. 1.01pu), and, additionally, the steady-state frequency deviation is eliminated. The improvement in the frequency response of the affected area comes at the expense of (collaterally) deteriorating the frequency response of the non-affected area. When the APG is equal to 60000MW/min, the non-affected area experiences zenith and steady-state frequency deviation issues close to the ones previously described for the case of APG = 0MW/min (i.e. 1.02pu and 1.008pu). Thus, the trade-off between desired improvement vs collateral implications due to the action of the f_{Ctrl} mode (when utilizing the maximum APG level) constitutes a key challenge for the effective cooperative frequency support of both areas. This challenge is further investigated in Chapter 7 from an optimization point of view.

In Chapter 3.3, the effect of different settings of the APG in the affected area

was investigated more closely by increasing the number of considered APG values (between the corresponding 0MW/min and 60000MW/min range) in order to determine the level of interaction between the primary frequency resources (i.e. governor systems) in the affected area, and the action of the APG attached to the PtP-VSC-HVDC link. Numerical results showed that although the frequency zenith and steady-state frequency deviations can be certainly reduced when the APG values are higher than 0MW/min, an undesired deterioration of the frequency Nadir (e.g., an under frequency around 0.975pu) can be generated in the affected area when the APG value of the PtP-VSC-HVDC link is higher than 900MW/min and lower than 9000MW/min. The undesired deterioration of the frequency Nadir is generated because an adverse interaction occurs between the reaction of the governor systems of the affected area and the speed of the deployment of the APG attached to the PtP-VSC-HDC.

More precisely, the fast adjustment of the power absorption level associated with the APG in the affected AC network contrasts significantly with the slow adjustment of the mechanical power of the synchronous machines (i.e. governor systems' response). Such contrast impacts the variation of accelerating power over time, causing undesired or unprecedented forms of frequency deviations. These results highlight the relevance of defining a suitable criterion for the adjustment of the APG's value of a VSC-HVDC link within a low inertia power system (c.f. Chapter 7). Furthermore, it is suggested to perform future frequency support studies considering other possible forms of interplay between the APG of PtP-VSC-HDC and the dynamic response of the governor systems under severe power imbalance events.

The third modelling upgrade tackles the dynamic voltage support and the post-fault active power recovery process, based on three developed supplementary controllers, which were presented in Chapter 3.4.

The first development concerns with a modification of the active power control's structure for enhancing the regulation of the time response of the post-fault active power recovery process. The proposed modification alters the active current reference by inserting an additional control loop in parallel with the integrator block of the PI regulator within the active power control. The simulation results showed that the insertion of the additional control loop generates an anti-windup response during a three-phase fault period. The anti-windup response enables the active power recovery process in less than 200ms for all studied events that could cause AC voltage dips. Additionally, it was observed that the only action of the proportional gain of the active power controller during the fault period, stabilizes the AC/DC power imbalance in the VSC-HVDC unit for all the studied forms of AC voltage dips.

The stabilization of the AC/DC power imbalance was possible since the management of the active current is coordinated with the second developed supplementary control, which essentially concerns with the design of a (square root characteristic-

based) polynomial function for the adjustment of the reactive current reference provided by the FRT function during a three-phase fault event. The results illustrated that the proposed polynomial adjustment of the reactive current is maximum when the voltage dip in the considered AC network is higher than 50% of the nominal network's voltage level, and it is minimum when the voltage dip is lower than 15%. Moreover, a parametric sensitivity analysis considering high impedance fault conditions unveiled that an indirectly caused AC/DC power imbalance is less pronounced in the VSC-HVDC unit when the polynomial reference of the reactive current adjustment is used to compensate small (e.g. lower than 40%) voltage dips in the AC network.

Finally, the third development consists of an upgrade in the RMS model representation of the AC fault element utilized to study the dynamic voltage response and the active power recovery profile of a VSC-HVDC unit during a fault event. Unlike the current abrupt voltage step-wise characteristics shown in most of the software packages used to conduct RMS simulations for three-phase short circuit experiments, the proposed modelling upgrade allows a realistic continuous representation of the inherent inductive transient characteristic of the network during a post-fault event. This realistic representation is obtained through a control block consisting of a fist order transfer function which defines the time-varying value of the fault impedance during the post-fault period.

Furthermore, the parameters of the first order's control block are based on a time constant and a proportional gain which are used to define the rise and the settling time of the AC voltage recovery process. For instance, the time constant could be chosen by the user to be close to zero if the purpose of the analysis on the post-fault active power recovery on the step-wise change of the voltage magnitude. By contrast, a time constant value around 1s could be considered when the purpose is on having a continuous representation of the post-fault ride through like in an electromagnetic transient (EMT) simulation. The proportional gain should be selected to reflect the dynamic response of the AC network current magnitude at the fault location. Future studies could consider the combination of EMT simulation and optimization to define the proportional gain and time constant depending on the dynamic properties of the system under study.

How can different reactive power control schemes of a modern VSC-HVDC unit for providing quasi-stationary AC voltage support be comprehensively and computationally efficiently compared and selected?

The replacement of conventional synchronous generators by power electronics interface generation is affecting the AC network strength and consequently, the response of the quasi-stationary AC voltage profile across transmission networks. The currently deployed analytic methods for assessing quasi-stationary AC voltage profiles do not capture the simultaneous influence of the active and reactive power provided by a VSC-HVDC unit when a point-to-point VSC-HVDC network expansion

(into a multi-terminal configuration) is foreseen. For this reason, in Chapter 4, the level of quasi-stationary AC voltage support provided by the reactive power control schemes of a modern VSC-HVDC unit was analyzed by proposing a directional derivative-based method (DDBM).

The proposed DDBM essentially avoided the need of performing computationally expensive time domain simulations to quantify the level of provided quasi-stationary AC voltage support. Instead, it offers a graphical description for determining the VSC-HVDC unit's power conditions in which a particular reactive power control mode offers the most suitable level of quasi-stationary AC voltage support. Additionally, unlike other analytic methods for the assessment of quasi-stationary voltage support, the proposed DDBM introduced the concept of an instantaneous voltage sensitivity factor which provides insight into the way in which the expansion of a point-to-point VSC-HVDC link, and the use of a particular reactive power control mode will affect the magnitude of the AC voltage in the surrounding AC transmission network.

The obtained results illustrated that the quasi-stationary AC voltage support of a VSC-HVDC unit under high impedance (e.g. 25Ω) network conditions requires higher reactive power gradient capabilities of the converter unit in order to keep the deviations of the AC voltage profile within an acceptable range (e.g. ±5% around the nominal value). Moreover, it was also shown that the degree of effectiveness of a particular reactive power control mode mainly depends on the AC network strength conditions, and the steady-state power levels in which the VSC-HVDC unit operates. Lastly, it was shown that the power factor control mode is the less attractive option for providing quasi-stationary AC voltage support in strong AC transmission networks conditions (i.e. 12GVA short circuit power). However, it was shown that depending on the steady-state reactive power level provided by the VSC-HVDC unit under weak AC network conditions, the power factor can provide a better level of quasi-stationary AC voltage support than the reactive power control mode.

What kind of supplementary power control should be used to provide primary frequency support to a power imbalanced AC network, if the PtP-VSC-HVDC link (demanding power from the imbalanced AC network) is requested to operate even during the loss of the communication interface between its converter stations?

Chapter 5 presents a frequency support methodology that is designed based on a power line communication principle applied to point-to-point VSC-HVDC links connecting two asynchronous AC networks. The power line communication principle is used to enable a point-to-point VSC- HVDC cable to act as an auxiliary communication channel in which a carrier signal containing the frequency deviation is introduced. Unlike other methods where the frequency of the carrier signal is modulated (increasing in that way the risk of harmonic instabilities in the HVDC network), the proposed method demonstrates that introducing a harmonic amplitude modu-

lated (HAM) carrier signal into the HVDC network makes possible to generate the necessary modification in the DC power flow of the point-to-point VSC-HVDC link without collateral harmonic resonances. The modification of the DC power flow is demonstrated by executing off-line RMS simulation experiments in a test system, which shows that the proposed HAM method helps to reduce the frequency Nadir (in approximately 0,3Hz) and to reduce the steady-state frequency deviation (in approximately 0,07Hz) generated in a synchronously coupled power system experiencing an emergency operating state (e.g. AC network split).

How to upgrade the post-fault active power recovery functionality of a point-to-point VSC-HVDC link when it expands towards a multi-terminal network, in order to effectively mitigate active power imbalances induced by AC voltage dips?

The analysis of the post-fault active power recovery process of an expandable point-to-point VSC-HVDC link was developed based on the proposal of a dynamic DC voltage regulation strategy as shown in Chapter 6. The dynamic DC voltage regulation strategy consists of a non-linear (exponential) function that modulates (in a point-to-point VSC-HVDC link) the active current at the inverter unit when a fault event occurs at the AC side of the rectifier unit. Additionally, it was also shown that the proposed non-linear function can be also utilized by a multi-terminal DC grid controller to ensure the post-fault active power recovery process in a three-terminal VSC-HVDC link allowing a post-fault active recovery time faster than 200ms and a DC voltage restoration within the same time range. Finally, it was also shown that if DC choppers are included within the expansion of the point-to-point VSC-HVDC link, the proposed non-linear DC voltage regulation strategy can also be deployed to enlarge the balancing support function capability, which could, for instance, suppress up to 85% of the DC power imbalance generated in a multi-terminal HVDC network due to faults occurring in the surrounding AC networks.

How to calibrate the parameters of the proposed frequency control mode of point-to-point VSC-HVDC links to optimally support the frequency stability of decoupled low inertia AC networks affected by severe active power imbalances?

In Chapter 3.3, it was shown that the maximum frequency deviation (e.g. frequency Zenith in case of over-frequency) within the containment period and the steady-state frequency deviations (generated by a severe (e.g. 20%) power imbalance in a low inertia AC network) can be effectively reduced by the proposed f_{Ctrl} mode. Nevertheless, if the point-to-point VSC-HVDC link is used to interconnect two separated AC networks with similarly low equivalent inertia constants (i.e. H< 7s), then, the improvement of the frequency stability in one AC network will come at the expense of the deterioration of the frequency stability of the non-disturbed AC network. Hence, Chapter 7 provides a method for defining how to harmonize the frequency response of the two (electromagnetically) decoupled AC networks

after a severe power imbalance occurs in one of them. The method considers the fact that an optimization problem can be conveniently defined depending on the targeted coordinated control actions. For the sake of illustration, the formulations of two cost functions were proposed and solved by using a mean-variance optimization (MVMO) algorithm, which generates near-to-optimal values of the parameters defining the adjustment of the proposed f_{ctrl} (i.e. active power gradient (APG) and the active power reference's set-point) through an off-line iterative RMS simulation process.

The obtained results indicated that the proposed cost functions allow to generate a frequency support function (between the two interconnected AC networks), which is characterized by two main aspects. The first aspect focuses on a mutual alignment between the rate of change of frequencies (RoCoF) of the AC networks. In this example, the best values of the APG and the set-point of the active power reference were, for instance, 961MW/s and 115MW, respectively. By contrast, the second aspect gives priority to the mutual alignment observed in the steady-state frequency deviation between the AC networks. In this example, the best values of the APG and the set-point of the active power reference were, for instance, 466MW/s and 134MW, respectively. Both examples indicate that depending on the operational needs (e.g. reducing RoCoF levels after an active power imbalance event) in a power system, the proposed f_{ctrl} mode, can be utilized to optimally deploy the primary frequency resources of two (decoupled) AC networks. In this way, the optimal deployment is done according to the underlying virtual electro-magnetic coupling that is associated with the obtained net effect of an APG-controlled point-to-point VSC-HVDC link.

8.2. Scientific Contributions

The research questions presented in section 1.2 of this dissertation led to the following scientific contributions:

1. An extended root mean square (RMS) generic model for studying the integration of VSC-HVDC links interconnecting synchronous transmission networks. The extended RMS model is based on the European HVDC grid code, and it is upgraded to include several advanced control functions: i) a dynamic regulation of the power factor (c.f. Chapter 3.2) for bidirectional active power exchange; ii) a post-fault active power recovery control (c.f. Chapter 3.4 and Chapter 6) that, based on the dynamic evolution of the AC voltage, reduces the impact on the active power balance, even in cases of high impedance network faults; and, iii) a situation dependent-emergency active power scheduling that modifies the amount and speed of active power response of the active power controller in a point-to-point VSC-HVDC link (c.f. Chapter 3.3 and Chapter 7).

2. An analytical method to directly quantify the level of quasi-stationary AC voltage support provided by different reactive power controllers of VSC-HVDC units within a point-to-point or a multi-terminal network (c.f. Chapter 4). The method

performs a directional-derivative-based analysis to determine (without the need of executing computationally expensive load flow calculations, or time domain simulation routines) the most effective reactive power control to be used by a VSC-HVDC unit to provide quasi-stationary AC voltage support, under different AC network strength levels.

3. A power line communication-based primary frequency control method for point-to-point VSC-HVDC links (interconnecting two synchronous AC networks) is proposed in Chapter 5. The method allows to modify the transferred DC power without the need of having dedicated communication channels be- tween the converter stations. The DC power modification is used to mitigate the power system's frequency excursions during emergency operating conditions (e.g., network split) through a proposed synchronous coupling detector concept. Unlike other approaches from the literature, it does not excite resonance phenomena within the HVDC network.

4. A method for post-fault active power adjustment of point-to-point or multi-terminal (i.e., point-to-point expanded) VSC-HVDC links is proposed in Chapter 6. The proposed method is based on a non-linear DC voltage modulation technique. The method allows to effectively restore the active power level in a point-to-point VSC-HVDC link after a fault event occurs at one of its connected AC networks, without the need for communication interfaces within a VSC-HVDC link. For the expanded VSC-HVDC link, the concept of a Dynamically Adjustable Chopper Impedance (DACI) is introduced, and together with the proposed DC voltage modulation, it is shown that the transfer of power imbalances across the multi-terminal network is significantly reduced while keeping the DC voltage limits within the required safety margins.

5. Two formulations for optimal tuning of the control parameters involved in the situation dependent-emergency active power scheduling for VSC-HVDC links are presented in Chapter 7. The selection of the formulation depends on the desired frequency response in an AC network affected by a severe active power imbalance: priority on steady-state (secondary) frequency performance between asynchronous areas interacting through a point-to-point VSC-HVDC link, or priority on the containment of the maximum frequency deviation during the primary frequency response.

8.3. Suggestions for Further Research

The design methodologies for the supplementary active and reactive power controllers presented in this work, where essentially established for a point-to-point VSC-HVDC link capable of being expanded up to a three-terminal VSC-HVDC network. In this connection, the analysis of the limitations of the proposed control principles under a multi-terminal network with a higher number of VSC-HVDC units and a different network topology represents a relevant research topic within future studies of the HVAC/HVDC network stability.

8.3.1. HAM method

The implications of using the proposed harmonic amplitude modulation (HAM) method under the context of a multi-terminal network, would require a harmonic stability analysis of the entire HVDC network. The use of a real-time simulation platform would help to increase the details concerning the electrical noise generated by the switching patterns of the converter units over the DC voltage.

8.3.2. PFAPR methods

The coordination between the energy dissipation capabilities of the DC choppers and the active power reduction characteristics of the offshore wind turbines represents a relevant research area for the enhancement of the proposed post-fault active power recovery (PFAPR) methods. Additionally, the analysis of the impact of the delays associated with the communication protocols used by the DC Grid controller would also be an important aspect to consider for the stability of the multi-terminal VSC-HVDC network.

8.3.3. DDB method

The utilization of the proposed directional derivative-based method (DDBM) for the converter interaction analysis of a VSC-HVDC unit with other AC voltage support systems represents an additional research area for the quasi-stationary AC voltage analysis of AC networks with high penetration of power electronic devices. The frequency support analysis of several AC networks interconnected by point-to-point VSC-HVDC links, having the proposed emergency power (frequency) control, it's also a very relevant topic for the coordination of the primary frequency resources of AC networks with different inertia levels.

8.3.4. APC tuning methods

The optimal tuning methods of the active power control (APC) proposed in this dissertation could be further enhanced by including other types of power electronic (driven) devices such as batteries, electrolyzers, solar or even wind turbine generation units. It is also suggested to extend the scope of the proposed cost functions to be applicable for multi-terminal VSC-HVDC links interconnecting several AC networks.

Appendix A

The energy conversion process in a VSC-HVDC unit starts by defining the *space-time vector* of the voltage $\overrightarrow{stv_v}$, and the *space-time vector* of the current $\overrightarrow{stv_i}$. In general, the *space-time vector* of the voltage $\overrightarrow{stv_v}$, is essentially a vector formed by each of the phase AC voltages as shown in the next four equations (identical approach is used to generate the $\overrightarrow{stv_i}$).

$$\overrightarrow{stv_v} = \begin{bmatrix} v_a(t) & v_b(t) & v_c(t) \end{bmatrix}^{\mathsf{T}}$$

$$v_a(t) = \sqrt{2} V_{rms} \sin(2wt + \phi)$$

$$v_b(t) = \sqrt{2} V_{rms} \sin(2wt + \phi - \frac{2\pi}{3})$$

$$v_b(t) = \sqrt{2} V_{rms} \sin(2wt + \phi - \frac{4\pi}{3})$$

As shown in Figure 8.1, during purely sinusoidal voltage conditions, the $\overrightarrow{stv_v}$ will be moving (within a three dimensional space) at constant speed, describing a circular trajectory. The constant speed is determined by the frequency of the electrical power system.

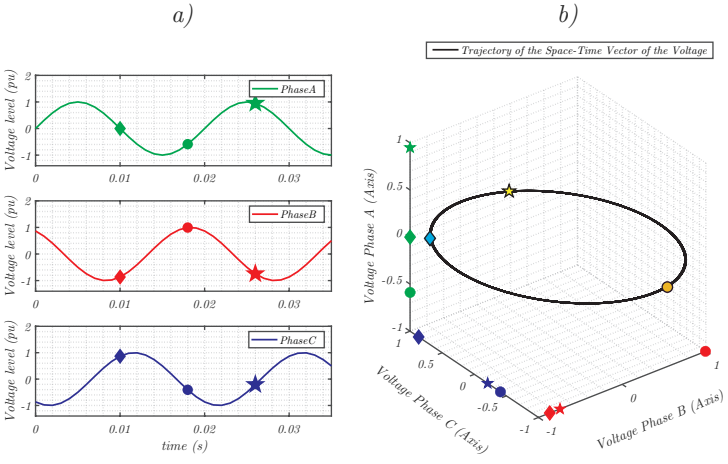

Figure 8.1: a) The three-phase voltages showing three different moments represented by three different symbols (a diamond, a circle and a start symbol). b) The $\overrightarrow{stv_v}$ moving in the three dimensional space formed by $v_a(t)$, $v_b(t)$, and $v_c(t)$.

Once it is understood that the three-phase voltages are now used to instantaneously describe the $\overrightarrow{stv}_v$ (which moves in a three dimensional space), then the four dimensional nature of the $\overrightarrow{stv}_v$ can be reduced by applying linear algebra transformations. The first linear algebra transformation to be applied is the Clarke transformation T_{Clarke}, and it is represented by the below matrix.

$$T_{Clarke} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}$$

The T_{Clarke} transformation is used to project the circular trajectory described by the $\overrightarrow{stv}_v$ (shown in Figure 8.1b) over a plane which is defined as the $\alpha\beta$ plane. This projection is done by multiplying the T_{Clarke}, and the $\overrightarrow{stv}_v$ as shown in the below equation.

$$v_{\alpha\beta} = T_{Clarke} \cdot \overrightarrow{stv}_v$$

The obtained $v_{\alpha\beta}$ vector represents the projection of the $\overrightarrow{stv}_v$ into the $\alpha\beta$ plane. Here, the $v_{\alpha\beta}$ vector rotates over the $\alpha\beta$ plane at the same speed of the $\overrightarrow{stv}_v$. Next, the second linear algebra transformation is the rotation matrix transformation $R_{\theta(t)}$, and it is represented by the below matrix.

$$R_{\theta(t)} = \begin{pmatrix} \cos\theta(t) & \sin\theta(t) & 0 \\ -\sin\theta(t) & \cos\theta(t) & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

The $R_{\theta(t)}$ transformation generates a rotation of the $\alpha\beta$ plane with an speed determined by $\theta(t)$. The rotational speed of the $\alpha\beta$ plane is adjusted by the *phase-locked-loop* control system to be equal to the rotational speed of the $\overrightarrow{stv}_v$. Thus, as the rotational speed of the new *rotating* DQ plane is identical to the rotational speed of the $v_{\alpha\beta}$ vector, the relative rotational speed between both of them will be null. Therefore, the $v_{\alpha\beta}$ vector "will look like" as *non-rotational* vector which is defined as the v_{DQ} vector as shown in the next equation.

$$v_{DQ} = R_{\theta} \cdot T_{Clarke} \cdot \overrightarrow{stv}_v$$

Additionally, the rotational speed of the DQ plane can be adjusted to align the v_{DQ} vector with one of the axis of the new DQ plane. This alignments process of the v_{DQ} vector is done to simplify the definition of the active and reactive power in this new geometrical framework as described by the two next equations.

$$P = v_D \cdot i_D + v_Q \cdot i_Q$$

$$Q = -v_D \cdot i_Q + v_Q \cdot i_D$$

There are several approaches to obtain the above active and reactive power equations. One of the most used relies on the use of the Fortescue transformation. Essentially, the $\overrightarrow{stv_v}$ and the positive sequence vector of the Fortescue transformation are multiplied to define the instantaneous complex $\overrightarrow{v_{\alpha\beta}}(t)$ and $\overrightarrow{i_{\alpha\beta}}(t)$ vectors as shown in the below equations.

$$\overrightarrow{v_{\alpha\beta}}(t) = v_\alpha(t) + jv_\beta(t) = \sqrt{\frac{2}{3}}\begin{bmatrix}1 & \alpha & \alpha^2\end{bmatrix} \cdot \overrightarrow{stv_v}$$

$$\overrightarrow{i_{\alpha\beta}}(t) = i_\alpha(t) + ji_\beta(t) = \sqrt{\frac{2}{3}}\begin{bmatrix}1 & \alpha & \alpha^2\end{bmatrix} \cdot \overrightarrow{stv_i}$$

Consequently, the instantaneous complex power $\overrightarrow{S_{\alpha\beta}}(t)$ can be defined by multiplying the instantaneous complex $\overrightarrow{v_{\alpha\beta}}(t)$ vector and the conjugate of the $\overrightarrow{i_{\alpha\beta}}(t)$ vector as shown in the equation below.

$$\overrightarrow{S_{\alpha\beta}}(t) = P + jQ = v_{\alpha\beta}(t) \cdot i_{\alpha\beta}(t)^*$$

Nomenclature

List of Abbreviations

APAC	Active power adjustment command.
APG	Active power gradient.
CCSC	Circulating current suppression controller.
CFA	Cost function A.
CFB	Cost function B.
DACI	Dynamic adjustable chopper impedance.
DAFI	Dynamic adjustable fault impedance.
DDBM	Directional derivative-based method
DLT	Droop line tracking.
DSL	Dynamic simulation language.
EMT	Electromagnetic transient
FDS	Fault detection system.
FRT	Fault ride through.
GFC	Generic frequency control.
HAM	Harmonic amplitude modulation.
HDS	Harmonic detection system.
HGS	Harmonic generation system.
HOV	Harmonic oscillatory value.
HVDC	High Voltage DC
IVSF	Instantaneous voltage sensitivity factor
LVT	Low voltage threshold.
MFD	Maximum frequency deviation.
MMC	Modular multi-level converter.
MT	Multi-Terminal.
NPCS	Non-periodic controlled signal.
PCC	Point of common coupling.
PCS	Periodic controlled signal.
PF	Power Factor.
PFAPR	Post-Fault active power recovery.
PLL	Phase-locked loop.
PtP	Point-to-Point.
RMS	Root-Mean-Square.
RoCoF	Rate-of-Change-of-Frequency.
RPG	Reactive power gradient.
SCD	Synchronous coupling detector.
VSC	Voltage source converter.

List of Symbols

Chapter 2

i_{up_x}	Current flowing through the $v_{valve}^{(+)}$ located in phase x.
i_{low_x}	Current flowing through the $v_{valve}^{(-)}$ located in phase x.
i_{g_x}	AC network current in phase x.
v_{g_x}	AC network voltage in phase x.
e_{g_x}	MMC AC side voltage generated in phase x.
v_{circ_x}	MMC voltage generating the i_{circ} current in DC branch x.
i_{circ_x}	Circulating current flowing in DC branch x.
L_{MMC}	Reactor (inductance) of the MMC.
L_g	MMC's transformer reactor (inductance) representation.
R_{MMC}	Resistance (losses) of the MMC.
R_g	MMC's transformer resistance (losses) representation.
$v_{valve}^{(+)}$	Positive pole valve of the MMC.
$v_{valve}^{(-)}$	Negative pole valve of the MMC.
C_{eq}	Equivalent MMC total capacitance.
I_{loss}	DC side current source representing MMC losses.
N	Number of submodules per valve.
I_c	DC side current source representing DC side MMC dynamics.
C	Capacitance of a Submodule.
P_x^{Σ}	Instantaneous Σ Power of the MMC in phase x.
P_x^{Δ}	Instantaneous Δ Power of the MMC in phase x.
w_x^{Σ}	Instantaneous Σ Energy of the MMC in phase x.
w_x^{Δ}	Instantaneous Δ Energy of the MMC in phase x.
i_{gD}	Direct Axis current of i_g.
i_{gQ}	Quadrature Axis current of i_g.
u_{gD}	Direct Axis current of u_g.
u_{gQ}	Quadrature Axis current of u_g.
e_{gD}	Direct Axis current of e_g.
e_{gQ}	Quadrature Axis current of e_g.
e_{gD}^*	Control generated reference for e_{g_D}.
e_{gQ}^*	Control generated reference for e_{g_Q}.
$i_{gD_{Outer}}^*$	Control generated reference for i_{g_D}.
$i_{gQ_{Outer}}^*$	Control generated reference for i_{g_Q}.
K_{P_D}	Proportional gain of the PI controller of the P_{Ctrl}.
T_{I_D}	Integral time constant of the PI controller of the P_{Ctrl}.
K_{P_Q}	Proportional gain of the PI controller of the Q_{Ctrl}.
T_{I_Q}	Integral time constant of the PI controller of the Q_{Ctrl}.
$K_{P_{dc}}$	Proportional gain of the PI controller of the $V_{dc_{Ctrl}}$.
$T_{I_{DC}}$	Integral time constant of the PI controller of the $V_{dc_{Ctrl}}$.
$V_{dc_{Ctrl}}$	DC Voltage Control of the MMC.
P_{Ctrl}	Active Power Control of the MMC.
Q_{Ctrl}	Reactive Power Control of the MMC.

U_{ACCtrl}	AC Voltage Control of the MMC.
$Droop_{Ctrl}$	Droop Control of the MMC.
I_c^*	Reference of I_c.
i_{dc}	DC current of the MMC unit (RMS model).
v_{dc}	DC voltage of the MMC unit (RMS model).
V_{dc}^*	Reference of the DC voltage of the MMC unit (RMS model).
$v_{dc_{max}}$	Maximum steady-state operational DC voltage of the MMC.
$v_{dc_{min}}$	Minimum steady-state operational DC voltage of the MMC.
P_{max}	Maximum steady-state operational active power of the MMC.
P_{min}	Minimum steady-state operational active power of the MMC.
P_{meas}	Measured active power of the MMC.
$V_{dc_{meas}}$	Measured DC voltage of the MMC.
$V_{dc_{Nominal}}$	Nominal DC voltage for the MMC.
e	Generated DLT error.
P^*	Reference of the active power for a MMC.
$K_{Droop_{dc}}$	Proportional DC voltage Droop gain for MT power flow control.
K_{Droop_P}	Proportional DC power Droop gain for MT power flow control.

Chapter 3

PF	Power Factor.
PF^*	Power Factor reference.
PF_{error}	PF error in the PF_{Ctrl}.
PF_{meas}	Power Factor measurement.
PF_{Ctrl}	Power Factor Control.
Q_{max}	Maximum Reactive power of the MMC.
S	Apparent power.
f_{Ctrl}	Frequency control.
$PF^*_{Adj\_Cap}$	Reference for the capacitive adjustment of the PF_{Ctrl}.
$PF^*_{Adj\_Ind}$	Reference for the inductive adjustment of the PF_{Ctrl}.
$P_{deadband}$	Active power deadband for PF_{Ctrl}.
APG	Active power gradient.
RPG	Reactive power gradient.
λ	Steady-state power ratio for the PF_{Ctrl}.
ΔP	Active power deviation in the f_{Ctrl}.
Δf	Frequency deviation in the f_{Ctrl}.
$i^*_{gD_P}$	Reference generated by the P_{Ctrl}.
i_{VSC}	AC current supplied by the VSC unit.
$i^*_{gQ_{Fault}}$	Reactive current reference generated by the FRT control.
α_{FRT}	Parameter (smoother factor) for the FRT polynomial reference.
V_{PCC}	AC voltage at the PCC bus.
$i^*_{gD_{Outer}}$	Active current reference for FRT control block.
K_{AP}	Proportional gain of the PI controller of the P_{Ctrl}.
T_{AP}	Integral time constant of the PI controller of the P_{Ctrl}.
Z_{DAFI}	Dynamic adjustable fault impedance.

T_{DAFI}	Time constant of the DAFI.
Z_{value}	Impedance final value of the DAFI.
u_{IPFC}	Input (step) signal initiating DAFI.
x_{TRX}	Reactance of the VSC (MMC) converter.
X_{th}	Thévenin reactance of the AC network.

Chapter 4

E_{th}	Thévenin voltage of the AC network.
X_{th}	Thévenin voltage of the AC network.
δ	Angle of the VSC unit with respect to E_{th}.
θ	Angle of the PCC bus with respect to E_{th}.
P_{VSC}	Active power supplied by the VSC unit.
Q_{VSC}	Reactive power supplied by the VSC unit.
λ	Steady-state power ratio for the PF_{Ctrl}.
APG	Active power gradient.
RPG	Reactive power gradient.
$\overrightarrow{PRR}$	Power ramp-rate vector for the DDBM.
$\overrightarrow{\nabla V_{PCC}}$	Gradient vector of V_{PCC}.
γ	Angle between $\overrightarrow{\nabla V_{PCC}}$ and $\overrightarrow{PRR}$.
$\gamma_{PF_{Ctrl}}$	γ angle associated to PF_{Ctrl}.
$\gamma_{Q_{Ctrl}}$	γ angle associated to Q_{Ctrl}.
$IVSF_{PF}$	IVSF of the PF_{Ctrl}.
$IVSF_{Q}$	IVSF of the Q_{Ctrl}.
APG_{VSC_i}	APG generated by VSC unit i.
$APG_{U_{DCCtrl}}$	APG generated by $V_{dc_{Ctrl}}$.
$APG_{P_{Ctrl}}$	APG generated by P_{Ctrl}.
PtP_{Op}	Point-to-point Operation.
MT_{Op}	Multi-terminal Operation.
η_{VSC_i}	Power distribution factor.
$X_{th_{low}}$	Low level reactance.
$X_{th_{high}}$	High level reactance.
d	Distance vector.
S_{PF}	Area generated by PF_{Ctrl}.
S_Q	Area generated by Q_{Ctrl}.

Chapter 5

i_{dc}	DC current of the MMC.
i_{cc_x}	Circulating current per DC branch of the MMC.
i_{hbal_x}	Harmonic balanced current per DC branch of the MMC.
i_{HAM_x}	HAM current per DC branch of the MMC.
K	Proportional Gain of the HGS.
Δf_x	Frequency deviation in the AC network x.
$v_{dc_{nom}}$	Nominal DC voltage.
$v_{dc_{HAM}}$	HAM DC voltage.

HOV_{over} HOV corresponding to the over-frequency issue.
HOV_{under} HOV corresponding to the unde-frequency issue.
$G_{dc}(s)$ Filter differentiator.
K_{dc} Proportional gain of $G_{dc}(s)$.
T_{dc} Time constant of $G_{dc}(s)$.
$G_{SORC}(s)$ Second order resonant controller (inverse notch filter).
K_{SORC} Proportional gain of transfer function $G_{SORC}(s)$.
α Parameter of transfer function $G_{SORC}(s)$.
β Parameter of transfer function $G_{SORC}(s)$.
ρ Parameter of transfer function $G_{SORC}(s)$.
$\overrightarrow{C(t)}$ Parameter of transfer function.
γ Parameter defining ratio of $\overrightarrow{C(t)}$.
$G_{AAE}(s)$ Average Area Estimator (Low Pass Filter).
K_{AAE} Proportional gain of $G_{AAE}(s)$.
T_{AA} Time constant of $G_{AAE}(s)$.
$G_{smt}(s)$ Smoother (Low Pass Filter).
K_{smt} Proportional gain of $G_{smt}(s)$.
T_{smt} Time constant of $G_{smt}(s)$.
HOV_{under} HOV signal for an under-frequency issue.
HOV_{over} HOV signal for an over-frequency issue.
$APAC_{over}$ APAC signal for an over-frequency issue.
$APAC_{under}$ APAC signal for an under-frequency issue.

Chapter 6

λ_{MOD} Exponential based modulation term.
DC_{meas} DC Voltage measurement of the VSC unit.
LVT Low voltage (DC) threshold.
α Exponential term for λ_{MOD}.
i^*_{ch} DC current reference value for the DC Chopper.
$i^*_{ch_{MAX}}$ Maximum value for the DC Chopper current.
$V_{dc_{nom}}$ Nominal DC voltage of the VSC unit.
$V_{dc_{MAX_{pu}}}$ Value for the DC Chopper over-voltage activation.
$P_{Pre-fault_{VSC}}$ Active power pre-fault value of VSC unit.
$P_{meas_{VSC}}$ Active power (measured value) of VSC unit.
$P_{meas_{Chopper}}$ Active power (measured value) of DC Chopper.
K_{ch} Proportional gain for the DC chopper control.
T_{ch} Time constant of the DC power based DC chopper control.
V^*_{dc} DC voltage reference for VSC unit.
$K_{Droop_{dc}}$ DC voltage based droop constant.
$V_{dc_{MOD}}$ Modulated DC Voltage term.
$V_{dc_{Pre-fault}}$ DC voltage level at the pre-fault condition.
$\Delta V_{dc_{MEM}}$ DC Voltage term for $V_{dc_{MOD}}$.
P_{Ctrl} Active power control.
$Droop_{Ctrl}$ Droop control.

U/f_{Ctrl}	AC voltage / frequency control.
FRT_Act	FRT activation signal.
Ch_x	DC Chopper unit of VSC unit x.
V_{PCC_x}	AC voltage at PCC busbar of VSC unit x.

Chapter 7

$\mathbf{x}^{CFA}$	Optimization vector for the cost function CFA.
$\mathbf{x}^{CFA}_{min}$	Vector defining the lowest limits for $\mathbf{x}^{CFA}$.
$\mathbf{x}^{CFA}_{max}$	Vector defining the highest limits for $\mathbf{x}^{CFA}$.
$\mathbf{x}^{CFB}$	Optimization vector for the cost function CFB.
$\mathbf{x}^{CFB}_{min}$	Vector defining the lowest limits for $\mathbf{x}^{CFB}$.
$\mathbf{x}^{CFB}_{max}$	Vector defining the highest limits for $\mathbf{x}^{CFB}$.
APG_{VSC}	Active power gradient of the VSC unit.
ΔP_{VSC}	Active power deviation of the VSC unit.
Δf_x	Frequency deviation of the AC network x.
$A(t)$	Instantaneous area for the optimization process of $\mathbf{x}^{CFB}$.
τ	Term defining integration range.
ρ_n	Weight for the frequency deviation response n.

List of Figures

8

List of Tables

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List of Publications

Journal Papers (First Author)

[A] **A. Perilla**, J. L. Rueda Torres, E. Rakhshani, R. Irnawan, F. Faria da Silva, M. van der Meijden, C. L. Bak, A. Alefragkis, and A. Lindefelt, *Directional derivative-based method for quasi-stationary voltage support analysis of single-infeed VSC-HVDC units*, High Voltage 5, 511 (2020).

[B] **A. Perilla**, J. L. Rueda Torres, S. Papadakis, E. Rakhshani, M. van der Meijden, and F. Gonzalez-Longatt, *Power-Angle Modulation Controller to Support Transient Stability of Power Systems Dominated by Power Electronic Interfaced Wind Generation*, in Energies 2020, 13, 3178.

[C] **A. Perilla**, S. Papadakis, J. L. Rueda Torres, M. van der Meijden, P. Palensky, and F. Gonzalez-Longatt, *Transient Stability Performance of Power Systems with High Share of Wind Generators Equipped with Power-Angle Modulation Controllers or Fast Local Voltage Controllers*, in Energies 2020, 13, 4205.

Other Journal Papers

[A] E. Rakhshani, **A. Perilla**, J. L. Rueda Torres, F. M. Gonzalez-Longatt, T. B. Soeiro, and M. A. M. M. Van Der Meijden, *FAPI Controller for Frequency Support in Low-Inertia Power Systems*, in IEEE Open Access Journal of Power and Energy, vol. 7, pp. 276-286, 2020.

[B] S. Ganesh, **A. Perilla**, J. L. Rueda Torres, P. Palensky, A. Leki´c, and M.A.M.M van der Meijden, *Generic EMT Model for Real-Time Simulation of Large Disturbances in 2 GW Offshore HVAC-HVDC Renewable Energy Hubs*, in Energies, vol. 14, 2021.

[C] S. Ganesh, **A. Perilla**, J. L. Rueda Torres, P. Palensky, and M.A.M.M van der Meijden, *Validation of EMT Digital Twin Models for Dynamic Voltage Performance Assessment of 66 kV Offshore Transmission Network*, in Applied Science, vol. 11, 2021.

[D] G. Giannakopoulos, **A. Perilla**, J. L. Rueda Torres, P. Palensky, F. Gonzalez-Longatt, *Coordinated tuning of MMC-HVDC interconnection links and PEM electrolyzers for fast frequency support in a multiarea electrical power system*, in Academic Press, 2023.

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frequency ancillary services in future multi-energy sustainable power systems, in Heliyon, vol. 5, 2019.

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Conference Papers (First Author)

[A] **A. Perilla**, J. L. Rueda Torres, A. A. van der Meer, M. A. M. M. van der Meijden and A. Alefragkis, *Influence of active power gradient control of an MMC-HVDC link on long-term frequency stability*, in IEEE Power & Energy Society General Meeting, Chicago, IL, USA, 2017.

[B] **A. Perilla**, J. L. Rueda Torres, M.A.M.M. van der Meijden, A. Alefragkis and A. M. Lindefelt, *Analysis of a power factor regulation strategy for an embedded point-to-point MMC-HVDC system*, in IEEE International Energy Conference (ENERGYCON), Limassol, Cyprus, 2018.

[C] **A. Perilla**, D. Gusain, J. L. Rueda Torres, P. Palensky, M.A.M.M. van der Meijden and F. Gonzalez-Longatt, *Optimal Tuning of Active Power Gradient Control for Frequency Support in Multi-Energy Systems*, in IEEE PES Innovative Smart Grid (ISGT-Europe), The Hague, Netherlands, 2020.

Other Conference Papers

[A] R. Irnawan, **A. Perilla**, F.F. Da Silva, C. Leth Bak, J. L. Rueda Torres, M.A.M.M. van Der Meijden, A. M. Lindefelt, A. Alefragkis *Operation strategy of a multi-terminal HVDC-connected wind farm against a highly fluctuating condition*, in 15th IET International Conference on AC and DC Power Transmission (ACDC 2019), 2019.

[B] R. Irnawan, **A. Perilla**, F.F. Miguel Faria da Silva, C. Leth Bak, J. L. Rueda Torres, M.A.A.M. van der Meijden, N. Qin, A.M. Lindefelt, A. Alefragkis *Preparing the expansion of a point-to-point VSC link into a multi-terminal HVDC transmission system: a COBRAcable research project*, in CIGRE Symposium Aalborg, 2019.

[C] G. Giannakopoulos, **A. Perilla**, J. R. Torres and P. Palensky, *A New Formulation for Optimal Tuning of Fast Frequency Support in Multi-Energy Systems*, 2022 IEEE Power & Energy Society General Meeting (PESGM), Denver, CO, USA, 2022.

[D] J. L. Rueda Torres, **A. Perilla**, E. Rakhshani, P. Palensky, M.A.A.M. van der Meijden, A. Alefragkis, *MVMO-based tuning of Active Power Gradient Control of VSC-HVDC links for Frequency Support*, in 2nd International Conference on Smart Grid and Renewable Energy (SGRE), Doha, Qatar, 2019.

[E] Z. Ahmad, S. Papadakis, **A. Perilla**, J. L. Rueda Torres, M.A.M.M. van der Meijden *Hardware-in-the-loop based testing of wind turbine controllers for transient stability enhancement*, in IEEE 29th International Symposium on Industrial Electronics (ISIE), Delft, Netherlands, 2020.

[F] A. Torres Acosta, **A. Perilla**, E. Rakhshani, J. L. Rueda Torres and M.A.M.M. van der Meijden, *Impact Assessment of Power Electronic-based Generation Units on Harmonic Response of Power Systems Using SVD based Method*, in IEEE Power Energy Society General Meeting (PESGM), Montreal, QC, Canada, 2020.

[G] A. Karaolanis, **A. Perilla**, J. L. Rueda Torres, M.A.A.M. van der Meijden, and A. Alefragkis, *Generic model of a VSC-based HVDC link for RMS simulations in PSS/E*, in 10th IFAC Symposium on Control of Power and Energy Systems (CPES), Tokyo, Japan, 2018.

[H] J. Mola-Jimenez, J. L. Rueda Torres, **A. Perilla**, W. Da, P. Palensky, M.A.M.M van der Meijden, *PowerFactory-Python based assessment of frequency and transient stability in power systems dominated by power electronic interfaced generation* in Workshop on Modeling and Simulation of Cyber-Physical Energy Systems (MSCPES), Porto, Portugal, 2018.

[I] D. Wang, J. L. Rueda Torres, **A. Perilla**, E. Rakhshani, P. Palensky, M.A.A.M. van der Meijden *Enhancement of transient stability in power systems with high penetration level of wind power plants*, in IEEE Milan PowerTech, Milan, Italy, 2019.

Curriculum Vitæ

Arcadio Perilla was born in Venezuela in 1987. During his last high school year (2003-2004), He designed and manufactured a magnetic levitation train (as part of his high school thesis) winning the first national prize at the Asociacion Venezolana para el Avance de la Ciencia. After that prize, He decided to study Electrical Power Engineering at Universidad Simón Bolívar, to become an expert on drives' design for magnetic-field control. Simultaneously, He did started his music composition studies at the Instituto Universitario de Estudios Musicales (IUDEM). Additionally, during the same time period, He did started (and concluded) his studies at the Unidad Profesional de Enseñanza Technologica (UPET) focusing on Industrial Electronics and Microcontrollers programming. His bachelor's degree internship was done at the Centro de Investigaciones Aplicadas (CIAP) Edelca, developing governor's system modelling for aero-derivative gas turbines for the Siderurgica del Orinoco (SIDOR) in Puerto Ordaz, Venezuela.

After receiving his B.Sc degree from Universidad Simón Bolívar, He had several jobs on automation and distribution systems design at Caracas, Venezuela. Next, He decided to continue his studies on Power Electronic by doing the M.Sc. degree on Electrical Engineering for Sustainable Development (E2SD) offered by the Université Lille 1 - Sciences et Technologies, Villeneuve-d'Ascq in France. During his master studies He did program the master micro-controller unit (MCU) for a lab mock up of a Modular Multi-Level Converter (MMC) half bridge, at the Laboratoire d'Électrotechnique et d'Électronique de Puissance de Lille. For his master thesis, He did develop an space-state representation analysis, focusing on the mathematical description of the participation factor theory for enhancing MMC's dynamic performance. After receiving his M.Sc. degree in 2015, Arcadio started his PhD studies as a part of the research program of the COBRAcable Project with the Delft University of Technology in The Netherlands. During his PhD studies, He has been a guest PhD student with SINTEF Energy Research, Trondheim, Norway, and with the Department of Energy Technology, Aalborg University, Denmark. Since 2020, Arcadio joint to the Transmission System Operator of the Netherlands (TenneT TSO B.V.) as an HVDC technologist working on several multi-terminal high-voltage dc (HVDC) projects such as the North Sea Wind Power Hub Project, the 2GW Program, and the interOPERA project. His research interests include modeling and control of power electronics interfaced generation for power systems dynamic stability assessment, MMC applications for power systems, and operation, control, and protection of multi-terminal HVDC networks.