Power Flow Control Converter

for Meshed LVDC Grid

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Technische Universiteit Delft

TU Delft Delft University of Technology

Challenge the future

Power Flow Control Converter

for Meshed LVDC Grid

by

R. A. Prakoso

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Thursday August 31, 2017 at 10:00 AM.

Student number:	4512529	
Project duration:	November 1, 2016 – August 31, 2017	
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This thesis is confidential and cannot be made public until August 31, 2018.

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Abstract

Meshed LVDC distribution grid is considered to be more efficient and reliable than AC distribution network. This applies in particular when there is a significant portion of DC sources, storage, and loads in the grid. Its optimal operation, however, is not inherent. The power flow in distribution network can suffer from congestion due to the line impedance of the system. Thus, a device that can regulate the power flow is regarded important. Several works have proposed DC-DC transformer and series voltage source type of power flow control device for HVDC application. DC-DC transformer, however, needs to be rated at full grid power. Meanwhile, series voltage source type for HVDC requires an additional connection to either nearby AC network or other lines. This thesis presents a function and requirements validation of a novel power flow control converter (PFCC) which only requires partial power rating with respect to the grid rating, needs no additional connection to other lines, and can regulate power flow in four V-I quadrants. The proposed topology able to performs power regulation with a fraction of grid power in all of the quadrants both in simulation and experiment.

Keywords: power flow control, power flow converter, meshed LVDC, DC distribution grid.

Acknowledgement

This thesis was carried out at the DC Systems, Energy Conversion & Storage of TU Delft. I take this opportunity to extend a warm hand of gratitude to all the people who have supported me to complete my studies and this work.

First and foremost, praises and thanks to Allah, the Almighty, for His showers of blessing throughout my studies and thesis work.

My gratitude goes to my supervisors, Prof. Pavol Bauer and Dr. Laura Ramirez Elizondo. It is an honor and a pleasure to have these great people as my supervisors. I am grateful for their generosity to share their deep understanding on scientific work.

It is also a huge privilege to have Pavel Purgat and Laurens Mackay as daily supervisors. They have laid the foundation and supported me in uncertain times, and been there for me when I had questions and in need of help. Without them, this work would not have reached this point.

I would like to also express my gratitude to Indonesia Endowment Fund for Education (LPDP) for supporting my two-year studies.

Finally, I wish to deeply thank my parents Mrs. Irawati Handayani and Mr. Imrony Hidayat, my sister Dinda Mutiara Savitri, my brother Bobby Rayhan Yusuf, and my fiancee Muthia Szami Naffisah, for their constant support and encouragement during the process of this thesis work. I thank all my friends for their support and memorable two years.

R. A. Prakoso
Delft, August 2017

Contents

1 Introduction

Chapter 1 discusses the basis of this thesis. A brief overview that leads to the discussion of the meshed DC distribution grid is presented in section 1.1. A more detailed motivation, problem definition, and scope of this thesis is described in section 1.2. These formulations are summarized in 1.3 as questions that need to be addressed by the end of this report. The path to answer those questions is summarized in 1.4. Finally, the structure of this report is presented in 1.5.

1.1. Research Background

Power network infrastructure faces challenges due to diminishing conventional energy resources, and environmental issues amid emerging sustainable technology, e.g. Distributed Generation (DG), Electric Vehicle (EV), and Energy Storage System (ESS). Global electricity demand will double in the 2060 and the per capita energy will peak before 2030 [39]. Meanwhile, generation of electricity and heat contributes to 41% of CO_2 emission [36]. To meet the electricity demand while reducing the emission, changes are needed in the global power infrastructure. Development of electrical grid was slow for the last decade in terms of energy generation and distribution. Most electric powers are generated centrally and distributed with the top-down approach. Power plants are typically built close to the main resource of the energy, e.g. hydro and geothermal. The generated energy must flow through long AC transmission system resulting in line losses. One of the reasons AC network was preferred a century ago was due to the absence of DC transformer. The non-existent of this technology meant DC power must be transmitted with a high value of current that leads to even greater losses compared to AC system. Nowadays, DG challenges the status quo of power distribution. A more sustainable power generating device such as photovoltaic and wind turbine can be deployed in a decentralized manner enabling the option of bi-directional power flow. It means an opportunity regarding generation capacity to supply the ever-increasing demand while still complies with environmental requirements. Distributed generation, however, along with energy storage system and electric vehicle, have several integration challenges to AC system. Moreover, the advancement of power electronics technology allows the use of potentially more efficient DC system. These facts raise a discussion over the evolution path of distribution grid infrastructure, AC or DC system.

The discussion over AC and DC distribution grid is largely influenced by the rise of DC load and sources in the network [34]. A significant portion of residential load today is DC, e.g. computer and monitors. The existing AC system necessitates the use of AC-DC conversion to supply these loads. Even AC load such as AC machines use variable speed drives that utilize AC-DC-AC conversion. The extra conversion steps and associated losses compared to an equivalent DC system creates an opportunity cost. This, among other development, initiates the discussion to change distribution grid into DC system. The ideal and expected course of a more sustainable technology in the form of DGs, EVs, and ESS fuels this discussion further as issues arise in AC environment. Synchronization, voltage stability, and efficiency are among many difficulties in the combination of AC system and DC nodes. Thus, if the DC sources and loads grow more dominantly in distribution grid, DC network can provide more benefits. Despite of that, there are challenges as well as opportunities ahead of DC network implementation. Lack of the unity in the voltage standard, the protection strategies, market integration, control and communication, and instability due to constant power loads are several problems that must be addressed [23]. One interesting opportunity that could not be done in AC distribution grid is

the possibility to use meshed architecture. The use of this amid the proliferation of DG and microgrids potentially increase network reliability and effectiveness. Thus, in the middle of direction uncertainty of DC distribution grid development, increasing DC loads and sources would arguably be benefited from the use of DC with mesh architecture.

Meshed DC Distribution grid comes with opportunities and challenges. It provides more efficient power transfer path in the low-voltage level. Without the topology, power has to traverse through higher voltage network to support other parts of the grid even in the nearby area [21]. This direct path offers a faster and more efficient grid support in terms of power availability and reliability. In a meshed network, however, optimal power flow is not inherent. One distribution line might be overloaded and limiting other cables to transfer requested power from the load. This line overload issue can also happen in the case of fault where power does not have anywhere to go but to the overloaded path. This imposes a risk to cable thermal limit and efficient operation of the grid. In a DC grid, there are many power electronic interface in the form of voltage source converter to the loads and DG. These converters can provide node voltage control that in the end regulates power flow on the lines. However, line power control through this method cannot be done independently to the grid stability [29]. Although the level of independence that can be achieved varies to the complexity of the network, a solution to control power flow in the lines without significant change in node voltage is necessary to tackle the apparent challenge of power regulation in meshed DC distribution grid.

1.2. Thesis Motivation

Suboptimal operation issue in meshed LVDC has been touched upon in the previous section. In order to gain a clearer vision of the problem, figure 1.1 is presented. The network is connecting three nodes composed of one link to a higher AC grid and two active loads in the form of EV charging station and DC house with PV. Suppose that there is an absence of car in the charging station and all the line resistances are equal, the resistance in the path of I_{L1} and I_{L2} is double the one of I_{L3}. This could lead to an overloading of L_3 while L_1 and L_2 are still 50% of its rated value. This imposes an unnecessary limit to the power transfer rating. This phenomenon could happen, of course, in many other mesh DC grid cases. This is the problem that needs to be addressed in meshed DC grid and shall be referred to as an over-current issue. The second issue that could arise in a meshed grid is unacceptable voltage-drop. Under the scenario described in figure 1.1, this could happen when the number of EV that needs to be charged increases dramatically such that the current flowing through L_1 creates a large voltage drop although other infrastructure ratings can still allow it to happen. These two issues need an ancillary solution in order to have a cost-effective infrastructure while keeping the power quality high.

Fundamentally, the over-current and voltage-drop issue can be solved in two ways. The first solution is to employ droop voltage control on the VSCs of N1 to N3. In the scenario of EV absence in the charging station, this would help prevent the over-current but not necessarily increase the utilization of the line to its maximum capability. In other cases where all the active loads are present, the over-current prevention using the droop control could be in conflict with the effort to maintain the stability of the grid where the node voltage is a critical parameter. Regulating voltage drop through droop control can also become tricky due to the node actual form as interface converter which frequently behaves as Constant Power Load [18]. Thus, it beneficial for the stability of the grid to have another dimension of controllability. Line variables can have the potential to provide this room to regulate its power flow and solve the over-current issue without significant influence to the grid stability.

DC power flow control is defined as devices that regulate the power flow in DC line [32]. It works by manipulating line variables instead of nodes. As nodes voltage in DC grid is expected to be maintained with minimum variation, power flow is overseen from line current. This left two other variables to be controlled to regulate power flow, i.e. line voltage and resistance. Several devices have been listed and categorized in [32]. Among the published works in DCPFC, there are very few dedicated to DC distribution grid and more research is required to explore the alternatives further.

Research on DCPFC is currently done mainly for HVDC[4] [35] [2]. They can be categorized based on device type and line connection type. Based on the component type, it can be divided into three division. The first device is DC transformer where it separates network nodes using full grid rated DC-DC converter with isolation. The second type utilizes lossy variable series resistor. The third category provides energy exchange links to insert a series voltage to the line; hence called Series Voltage Source. This type of device comes with different topology and can be done in partially rated manner. The partly rated version of Series Voltage Source is considered to be the best solution in terms of cost, efficiency, and controllability by [32].

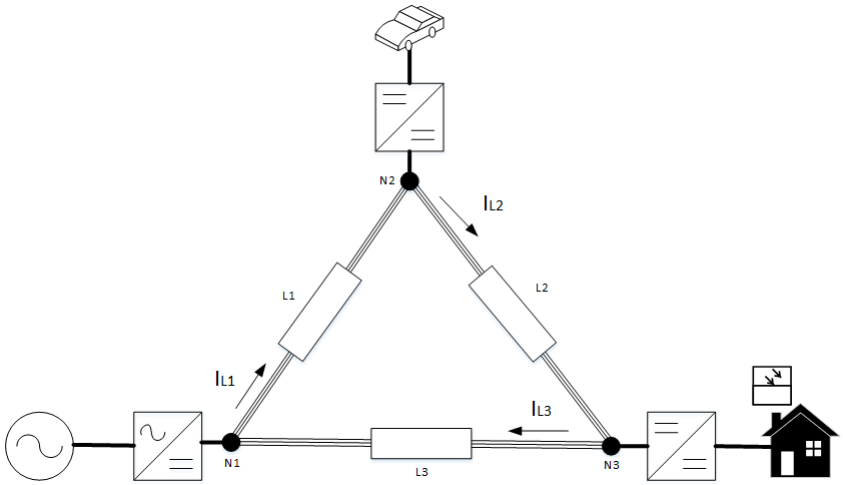

Figure 1.1: *Meshed Bipolar DC Distribution Grid with three nodes where overloading current and unacceptable voltage-drop can occur.*

Regarding the line connection, the energy exchange links can be provided from external AC sides or other DC lines. In the low voltage level, only one paper discusses a power flow control device [29]. None of the fully developed solutions, however, offers DCPFC with a partial rating and dedicated to be used in meshed DC distribution grid.

In [21], the author offered a glimpse of how partially rated converter for DC distribution grid would be. It proposed a topology utilizing isolated DC-DC converter with a parallel connection to the line on one side and a series one on the other side. This way it can reduce the power rating requirement of the converter into approximately 10% of the grid. Thus, it would reduce cost and loss of the converter. It also discusses, in a limited manner, how should it be operated when the DCPFC is not required to operate and the response time needed for the dynamic control. This limited discussion requires a more thorough exploration and evaluation regarding topology, device-level control, simulation and experimental test.

1.3. Thesis Questions

The goal of this thesis is to design a partially rated power flow control converter to enable more line controllability for meshed DC distribution grid. According to this, the research question of this thesis are as follow:

"How should a partially rated power flow control converter be designed to enable more line controllability for meshed LVDC distribution grid?"

The following subquestions will be answered to get the final outcome:

1. What are the important functions and requirements of partially rated power flow control device that woud be suitable for meshed LVDC distribution grid?
2. Which converter topology of the partially rated power flow control device can be used to satisfy the selected functions and requirements?
3. What device-level control of the partially rated power flow control device can be used to satisfy the selected functions and requirement?

1.4. Methodology

In this research, the development and evaluation of PFCC are done through literature review, simulation, and experimental test. Firstly, suitable PFCC functions and requirements for meshed DC distribution grid are determined through literature review. Secondly, topology and device-level control alternatives for both the DC-DC with isolation segment and four quadrant part are also done through literature review. Thirdly, a suitable topology is then selected and modeled to pursue simulation validation. Fourthly, a hardware prototype

dedicated as a proof of concept is built. Finally, evaluation and possible future improvement of the evaluated topology and device-level control shall be presented.

1.5. Report Outline

This report consists of six chapters. The organization is as follow

- Chapter 1 introduced the research by discussing its context, motivation and question that must solved
- Chapter 2 composed of literature review on LVDC distribution grid and DC power flow control devices. These knowledge is used to determine a proper functions and requirements.
- Chapter 3 presents the simulation of the proposed converter. Circuit alternatives that can be used for the isolation stage and output regulator segment are discussed along with the modeling. Afterwards, the simulation results are presented.
- Chapter 4 discusses the development of hardware prototype. The choice for each part of the implementation is discussed. The construction was mainly done for the full-bridge segment. Thus, the selection of the switches, passive components and its implementation on the PCB are discussed.
- Chapter 5 presents the analysis of the experiment results. The efficiency of the prototype was first measured. Afterwards, its functionality and one of its requirement was demonstrated.
- Chapter 6 concludes the thesis by summarizing key takeaways and offer future works that needs to be done

2

Low Voltage Direct Current Power Distribution Grid and DC Power Flow Control

This chapter focus on reviewing literature of DC distribution grid and DC power flow control to determine appropriate functions and requirements for the power flow control converter. Section 2.1 discusses the opportunities and challenges of LVDC. Section 2.2 summarizes [32] to gain a fundamental understanding of DC power flow control devices in general and its behavior on the grid. Section 2.3 presents examples of DC power flow control devices in HVDC and LVDC. Finally, section 2.4 analyzes literature both from LVDC grid and the power flow control device point of view to determine functions and requirements of DC power flow control converter.

2.1. LVDC Distribution Grid

Factors that drive the use of DC grid in the utility network keeps increasing albeit there are few challenges ahead. At first, the efficiency of High Voltage Direct Current (HVDC) transmission line attracts the use of DC. The absence of the reactive power allows pure active power transfer without the inconvenience of cable capacitance, and this is especially beneficial for sea cable [37] [23]. The advancement of high power electronics made this application possible. Today, the steep increase in global power demand [8] and the risk of environmental issue pushes the use of sustainable technologies which employ more DC link such as Photovoltaics (PV) and Electric Vehicle (EV). These renewable sources and DC loads are distributed in the distribution grid. LVDC offers features that match the needs to maximize the use of these emerging technologies. Despite that, there are fundamental challenges that must be addressed in this early stage of LVDC development. One of interesting potential in LVDC is the possibility to mesh the network which is not preferred in Low Voltage Alternating Current (LVAC) grid. This grid topology could unlock a better reliability and efficiency of the grid[21]. Its development, however, is also facing challenges that must be addressed.

LVDC distribution grid has two important opportunities and challenges. There are features of LVDC that made it attractive but most of them are narrowed down to two opportunities that must be grabbed. The first one is increased efficiency. There is a number of reason behind lower losses in LVDC. These include the absence of reactive power and lower amount of conversion stages. The second one is DC source, storage, and load compatibility. In fact, the advantages of LVDC are mainly dictated by the portion of these DC nodes on the grid [34]. In secondary customer today, however, most of the loads are in DC. In order to utilize these opportunities, two significant challenges must first be solved. The first one is standardization [22]. As a technology that tries to break the status quo without a collective voice, it is difficult to have an unequivocally accepted standard across different institutes and companies. The second challenge is protection [22]. The absence of zero voltage crossing which is available on AC grids and the low inertia of the sources make the protection difficult [3]. The two opportunities and challenges can be discussed further based on the cause that creates it and the consequence of it.

A quantitative value of how significant the efficiency of LVDC varies between applications and implementations has been reviewed by [38]. In order to analyze the energy saving, [38] has divided the analysis

into four categories of the system. The first category is a residential system. In this category, there is a range of energy savings between 2% and 14%. The differences in the studies are due to assumptions made for converter efficiencies and the complexity of the system. The second category is data centers. In this category, there can be energy saving between 1% to 15%. The differences between studies are due to a different efficiency of UPS and converter used. The third category focuses more on the implementation of a portion of DC in a large system. In this category, one study that incorporates Distributed Generations (DG) shows an energy saving of 40%. Meanwhile another study which does not use it only gain 1% at best. The last category is other implementations and applications. [38] discusses, however, two studies that incorporate changes on conversion stages on the residential load used for this category. The modification of the conversion stages does save energy for a certain load. This removal of conversion stage in DC grid can be observed from figure 2.1. One takeaway from the study is that the energy saving comparison between LVDC and LVAC depends significantly on the efficiency of power electronics, the complexity of the system and portion of DC loads and sources connected to the system [38][34]. Thus, the primary driver of the efficiency of LVDC is the reduced conversion stage. On top of that, another reason that LVDC has higher efficiency is due to a negligible reactive component. Although the driver of efficiency does not automatically put LVDC as a more efficient system than LVAC, the review of different LVDC and LVAC energy saving comparison shows that increased efficiency is possible in LVDC distribution grid [38].

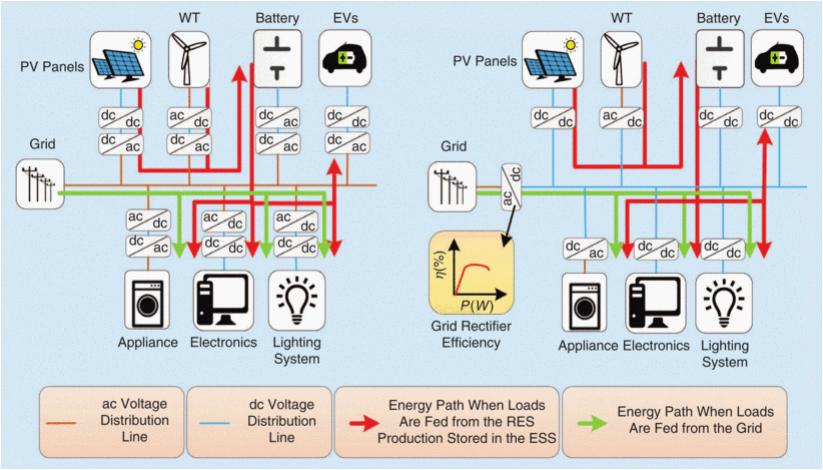

Figure 2.1: *Reduced conversion stages on LVDC distribution grid. The network on the right side employs LVDC distribution line and many dc/ac conversion stage can be eliminated. [34]*

Another opportunity of LVDC is its compatibility to DC loads and sources. This advantage does not only include the less conversion stages involved but as well as how the power is flowing and shared on the grid. The proliferation of DGs and the increasing demand of power would be benefited by power distribution system upgrade to allow multi-directional power flow [3]. Unlike LVAC, DC grid has less issue with DGs in terms of harmonic compare to its AC counterparts. This would allow the concept of prosumers in which an electric utility customer is allowed to produce energy and feed it to the grid. It means that power capacity of the grid no longer relies solely on the construction of large centralized power plants. This taps a huge potential of additional energy sources which has not been possible before. In multidirectional power flow implementation, DC grid is a better equipped solution compared to the AC side [3]. This is due the complexity of AC grid which depends on the difference of phase angle in controlling the direction of power flow. LVAC grid is also rarely implemented as mesh network due to protection issues [3]. Short circuits and faults happens frequently in the AC distribution grid. Thus, it is important to have a topology that can isolate the fault from propagating to different direction of the grid. The ease of fault isolation in radial grid is especially true when the power flowing in one direction from centralized power plants [21]. Due to the simplicity of LVDC , mesh network has a better advantage to be implemented. In a system where DGs are significant, mesh topology can increased reliability and efficiency of the grid as energy exchange path is shorter. A study of the advantage of multi-terminal network on EV charging is presented in [31]. This shows that mesh network can allow a better power sharing in terms of EV charging and more EV can be incorporated to the grid. All of this shows that in a system where a significant portion of DC loads and sources are present, LVDC can increase its reliability and

efficiency through reduction of conversion stages, multi-direction power flow and mesh network.

Despite of the opportunities LVDC distribution grid offers, it has a tough challenge in terms of standardization. This issue is significant to the adoption of LVDC as distribution grid as it is the closest network to the consumers and loads. It means that a change in this part of the grid would influence the equipments and loads consumer used as well. This includes a plethora of consumer electronics which needs to adapt to the new grid suppose that it is implemented [34]. This changes requires a common standard to take place. In LVDC, however, there is still no widely accepted voltage level standard. figure 2.2 shows the different codes, standard and application define its voltage level. There is, however, a growing opinion that voltage standard between 350V to 400V is going to be used. This is because the discussion of voltage standard must also include the distribution grid architecture that shall be used. figure 2.3 shows one attractive option. The architecture presented is a bipolar voltage grid. In this alternatives multiple pole can be connected to different loads with respect to a neutral according to the voltage required by the application. This is beneficial considering the number of local DC grid application that has been developed in different voltage level and mature faster than the distribution grid itself. This would allow minimum changes to those application and its best practice and its integration to the new grid more seamlessly. The standardization challenge is an imperative issue to be tackled on for LVDC distribution grid to be adopted. There are already engineering alternatives to solve the issue but the challenge also requires institution and companies to accelerate the progress to a more widely accepted standard.

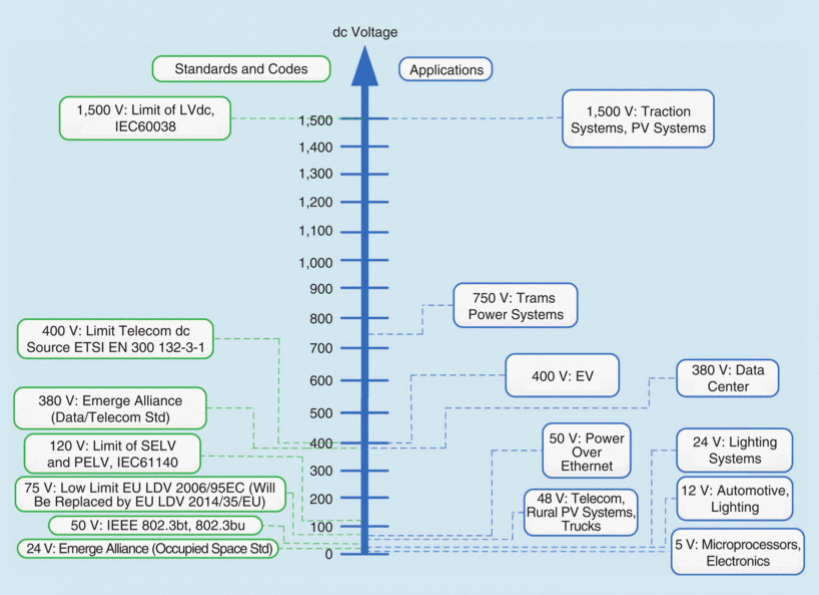

Figure 2.2: *List of standards and application of LVDC. SELV: Separated extra LV; PELV: Protected extra LV. [34]*

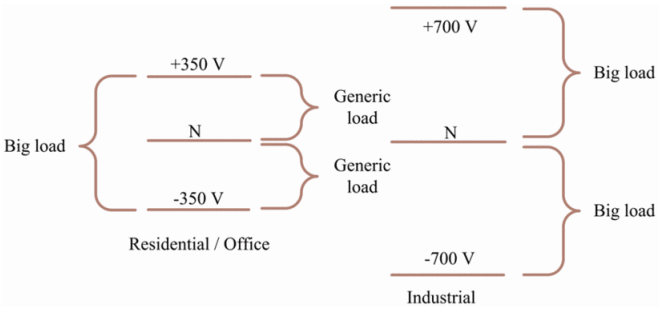

Figure 2.3: *Bipolar LVDC voltage level and different node connection [23]*

Protection is another important challenge that must be addressed in LVDC distribution grid. It is difficult mainly due to the absence of zero current crossing and the low inertia of the system [15] [22]. The best practice to clear out short circuit in LVAC is to utilize the zero current crossing of AC waveforms. This is, of course, not available in DC waveform. AC circuit breakers can be used for DC implementation but this would need and overrating of the device [22] which would be expensive. Another practice in HVDC is to isolate the fault by disconnecting from the AC side. This, however, is more impractical in LVDC distribution grid. The low inertia of the system made this issue more challenging. This low value is due to the the absence of reactance in DC cable as well as the use of power electronic interface and PV. It means that a DC faults require fast coordinated protection in the scale of less than few milliseconds [15]. Protection which use DC Circuit Breakers (CB) that requires communication would need to transmit the information in a fraction of the that time scale. The use of DC-DC converter with isolation would help isolate the fault without needing any communication. In a mesh grid, however, this solution would be to complex to implement especially in a large and sophisticated mesh network[22]. Solid state breakers can offers a faster disconnection albeit its on-resistance and switching losses [22]. A hybrid between mechanical and solid state breaker is another promising solution for this issue and would need further research to mature. Other issue of protection such as over-current due to network congestion and under-voltage due to high voltage drop requires more attention especially in mesh network where optimal operation is not inherent. This is illustrated by [21] with scenario given in figure 2.4. Suppose that node 2 is disconnected due to a fault and all cables have the same resistance, the current flowing through line 3 would be double than the one on the two lines. When high power close to the rating of the cable is transferred during the fault, line 3 would suffer an over-current. Paper [21] offers a solution to solve this issue by limiting the current using a device that insert series voltage on the line. This type of device is called a DC power flow control. It offers more controllability to solve these issue of over-current and high voltage drop. However, most of the work has only been done for multi-terminal DC and there are only few which covers distribution grid.

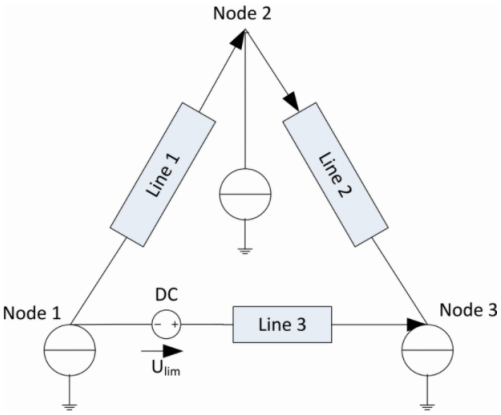

Figure 2.4: *Case study of over-current due to disconnected faulty node in [21]*

Opportunites and challenges of LVDC distribution grid has been discussed. It offers two prominent opportunities, possibility of higher efficiency than LVAC and a better compatibility to DC sources and loads which includes DGs, EVs and ESS. This efficiency, however, does not come automatically but depends largely on the portion of DC sources and loads in the grid as well as efficiency of power converters. LVDC would maximize the potential of sustainable technologies such as DGs, EVs and ESS with its bidirectional power flow and mesh network. Despite of that, it faces two significant challenges in the form of standardization and protection. There is currently no widely accepted voltage and grid architecture standard for LVDC. This issue requires a better communication between stakeholders of distribution grid. The low inertia of the system and the absence of zero crossing made the grid protection requires more work to mature. The use of solid state and hybrid breaker might offset the disconnection time needed in an efficient and inexpensive manner. The use of protective device like DC power flow would help tackle this issue by offering more controllability and safety. In order to maximize the opportunity and tackle the challenges a more work has to be done to provide more solution and ideas which creates a domino effect in increasing the LVDC distribution grid time of adoption.

2.2. DC Power Flow Control Principle

In an meshed system, optimal power flow is not inherent due to Kirchoff's Law. Unregulated power flow would result in lightly loaded or overloaded path which leads to losses, underutilized infrastructure or even fault. AC grids have dealt with this issue for decades with many different methods and devices such as transformer tap settings, capacitor bank connection and other AC power flow control techniques. Most approaches used in AC grid controls the power flow through reactance. In DC however, current flow is entirely governed by DC resistance of the conductor while transmission path inductance influence insignificantly. Devices that can regulate power flow in DC grid is called DC Power Flow Control (DCPFC). This section discuss the principle of the devices and its behavior on the grid by summarizing paper by Mu et al. (2012) [32] [7]. Power flow control in DC grid can be done mainly using three types of devices; DC Transformer, Variable Series Resistor (VSR), and Series Voltage Source (SVS) [32]. Each type has different characteristic to each other and determines its suitability to a certain application. It is necessary to understand how these types works and its characteristics.

DC Transformers are used to build multiple DC voltage levels for the purpose of increased flexibility of power transfer and enhanced overall economic operation. It is composed of DC/AC converter, AC transformer, and AC/DC converter. The AC transformer provides voltage level conversion and isolation between the two converters. An equivalent model to describe its operation is depicted in figure 2.5. The primary side is modeled with a current source I_1 and a parallel equivalent capacitor C_E while the secondary side is modelled with a voltage source U_2 and a series equivalent inductor L_E. The relation of voltage and current between the two sides can be presented as in equation 2.1 and 2.2. It is dependent on the turn ratio of the AC transformer n and modulation index of both AC/DC converters m_1 and m_2. The current can then be controlled to a desired value by manipulating these indexes. In addition of controlling power flow, DC transformer can also acts as voltage stepping and DC fault current interruption. However, DC transformer has high construction cost due to its full rating capability, comparatively large power losses and low reliability for high power application compared to AC transformer.

$$U_2 = kU_1 \tag{2.1}$$

$$I_2 = -I_1(\frac{1}{k}) \tag{2.2}$$

$$k = n(\frac{m1}{m2}) \tag{2.3}$$

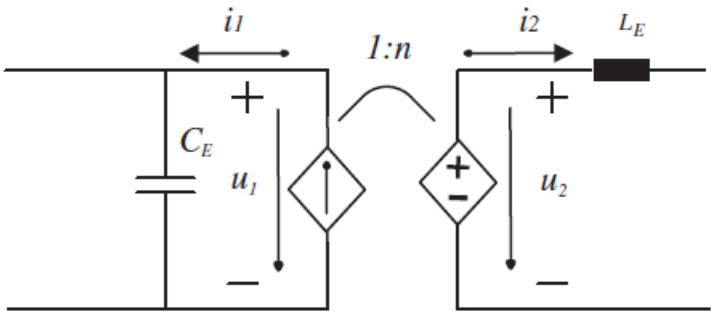

Figure 2.5: *DC Transformer Equivalent Model [32]*

Variable series resistor works by simply inserting additional resistance in series to DC line. Figure 2.6 shows one of VSR implementation using IGBTs and diodes. The resistance introduced to the line is proportional to the duty cycle of IGBTs with maximum inserted resistance of R as presented in equation 2.4. The duty cycle D is the percentage of one period T in which IGBT is on. VSR can also regulates active power in which the VSR is not located but connected to line. However, the controllability of this device depends on the current flowing to the line connected to it. Moreover, the main disadvantage is the large losses due to introduced resistance which require large cooling. Despite of that, its small rating due to its series connection to line brings advantage of low investment.

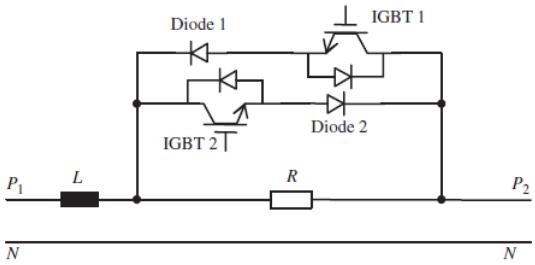

Figure 2.6: *Variable Series Resistor Diagram [32]*

$$R_{ave} = \frac{T_{off}R}{T} = (1-D)R \tag{2.4}$$

Series Voltage Source use power exchange between lines to insert a series voltage which will control the power flow. The device acts as a controllable voltage source with a fraction of grid rating. This concept can be implemented with different methods and devices. The first method is to introduce a series voltage through an external AC link. This method requires at least one AC tranformer, AC/DC converter, and DC/DC converter. The AC transformer is used to isolate the AC and DC grid while providing a voltage step down option. The AC/DC converter, on the other hand, convert the AC voltage to a constant DC value which in DC/DC converter will be chopped to a required value which in the end regulate power flow in DC line. The main disadvantage of this method, however, is the requirement to use AC transformer which must be rated to the full AC system. One example of topology which uses this method is depicted in figure 2.7. The second approach is inserting a series voltage without AC link. One of the topology to achieve this is presented in figure 2.8. In this example, two H-bridges are connected to two different lines which has the same common DC voltage or ground. One H-bridge is controlled to maintain the voltage U_C while the other H-Bridge is used to chop that voltage into a required ΔU_2. The relationship for the power control is $\Delta U_2.I_2 = \Delta U_3.I_3$. This approach eliminates the need of full grid rated devices such as AC transformer.

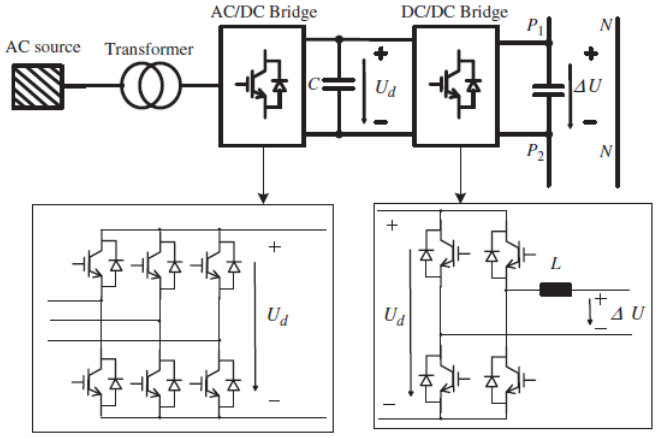

Figure 2.7: *Series Voltage Source with AC Link [32]*

In general, the three types of PFCC devices above can be modeled as a voltage series to the line which can be elaborated to compare its control sensitivity as done in [32]. SVS works directly by inserting series voltage which can be positive or negative. Meanwhile, VSR inserts a series voltage through resistance which is then dependent on line current. On the other hand, DC Transformer can significantly influence the power flow by changing the voltage ratio of the two sides complying to $U_{insert} = (k-1)U_1$. By elaborating this model to small signal model, paper [32] has compared the three devices in terms of control flexibility, power rating and power losses. Figure 2.9 shows the comparison in terms of control characteristics. The Y axis represents the control

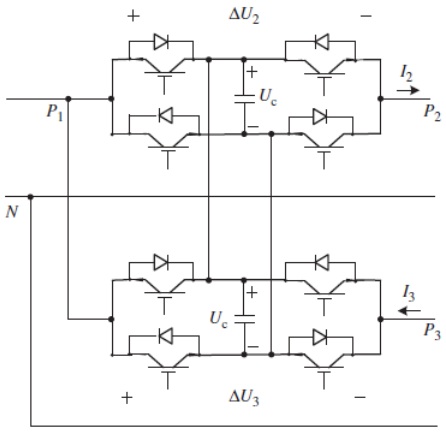

Figure 2.8: *Series Voltage Source without AC link [32]*

variable needed to be changed by the devices with 100% showing the device limits while the X axis is the line current which is presented as percentage of the rated current. It can be seen that VSR is the only power control device type which has a limited control range as the current decrease. It also cannot change the current more than its rated current. This is not the case for DC transformer and SVS. The DC transformer, however, requires less change in its control variable to change the same amount of current compared to SVS. Despite of that, DC transformer requires full rating of the DC system. This creates high amount of loss compared to VSR and SVS. VSR losses is around 5-10% of the entire losses of the DC system while DC transformer could accounts for 14-15% [32]. On the other hand, the losses in SVS only includes limited switching loss of the converter and few percentage of conduction loss. This shows the superiority of SVS in terms of control flexibility, power rating, and power loss compared to the other two devices.

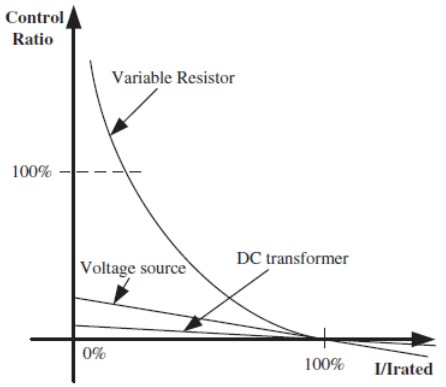

Figure 2.9: *Control characteristics of three power flow control devices [32]*

2.3. Examples of Direct Current Power Flow Control

Development of power flow control devices in HVDC is ahead of the progress done in LVDC. Several topologies and control algorithm have been published. Thus, it is beneficial to take a look and gain inspiration from these progresses before moving on to LVDC power flow control devices. It is more efficient, however, to focus directly to SVS type of devices which has been concluded as the best power flow control devices type in previous section. Thus, one example of each SVS type with external AC link and the one without AC link shall be discussed. A work on LVDC DCPFC is also summarized. The discussion covers its topology, operating principle, and its control.

2.3.1. HVDC DCPFC

An SVS device which uses the same topology as figure 2.7 is proposed in [2] as an IGBT based converter. The device bridge a connection between AC side and DC side of the grid allowing power transfer between the two. It means that any additional or required power will be exchanged between AC and DC side to gain control of the power flow. The power flow controller is composed of three segments as depicted in figure 2.10; an AC transformer, a 3-phase 2-level Voltage Source Converter as AC/DC conversion device, and a 4-quadrant chopper in the form of H-Bridge. V_{PFC} is the series voltage to be inserted to the line in a value complies to equation 2.5 and 2.6 with D as duty cycle of the four quadrant chopper.

$$V_{PFC} = (2D-1)V_c \tag{2.5}$$

$$-V_c <= V_{PFC} <= V_c \tag{2.6}$$

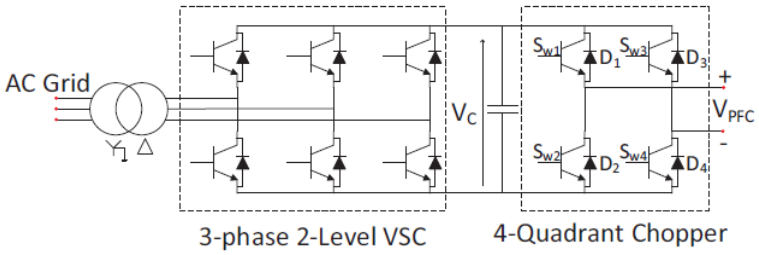

Figure 2.10: *Series Voltage Source Device Type with AC Link [2]*

The DC chopper is controlled using unipolar voltage switching. The control scheme and the output series voltage depends on the current flowing through the converter. When the current is going out from the positive side of V_{PFC} and going back in through its negative side, the inserted voltage remains zero if either SW1 or SW4 is off and the other one is on. If both SW1 and SW4 are on then the inserted voltage is positive and it will be negative when both are off. For the current in the reverse direction, the series voltage value depends on SW2 and SW3 with the same scheme.

The two converter segments, VSC and H-Bridge, are controlled with control scheme described in figure 2.11 and 2.12 respectively. The 3-phase 2-level converter is controlled with inner current control loops and outer DC capacitor voltage and reactive power controller. The inner current loop is based on dq reference frame to regulate AC current components by giving out modulation signals through dq to abc reference frame transformation. The DC capacitor voltage controller sets a DC side current reference value while the reactive power controller sets reference value of the q-component of AC side current. The inner current controller is tuned to gain a fast dynamic response and linked to the slower outer loop. The H-Bridge, on the other hand, is controlled using control block diagram depicted in figure 2.12. It contained a voltage control as its inner loop and current control as the outer loop. It gives out the duty cycle of each leg with value between 0 to 1.

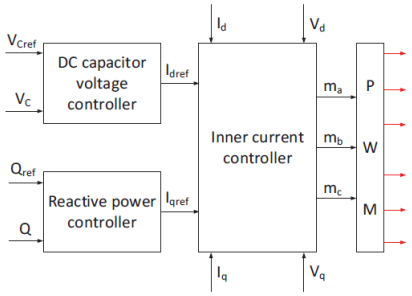

Figure 2.11: *Series Voltage Source Device Type with AC Link VSC Control [2]*

The absence of AC link offers a significant advantage in terms of power rating and losses which is demonstrated by [4]. The paper proposes a novel power flow control devices which works by exchanging power

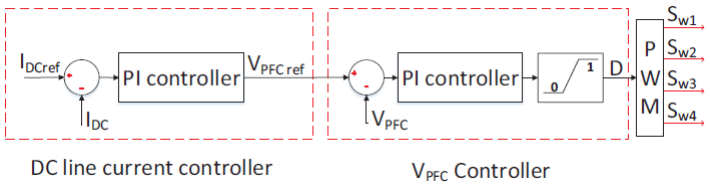

Figure 2.12: *Series Voltage Source Device Type with AC Link H-Bridge Control [2]*

between two DC lines using a topology and connection as depicted in figure 2.13. The topology is exactly the same as depicted in figure 2.8 but presented in a 3-terminal Modular Multilevel Converter (MMC)-based HVDC grid.

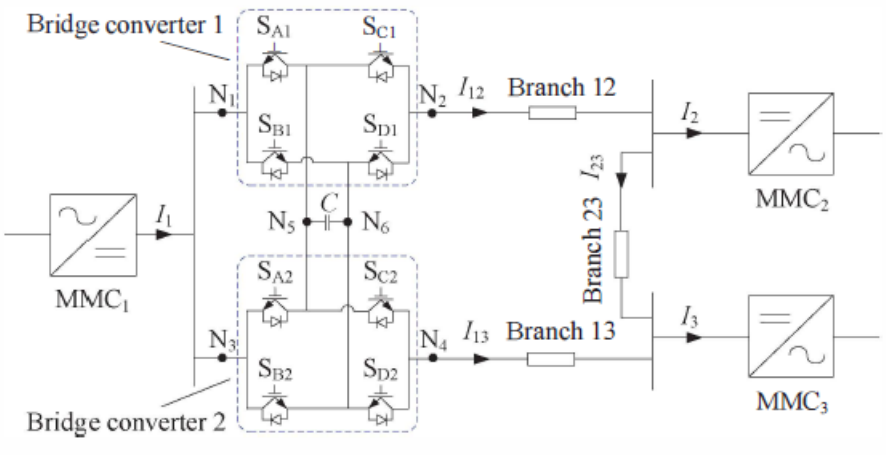

Figure 2.13: *Series Voltage Source Device Type Without AC Link [4]*

The topology is composed of two identical full-bridge DC-DC converter with a capacitor in the middle. Each full-bridge can be seen as two leg pairs with SA and SB form one leg and SC and SD composed the other leg. SA and SB are switched complementary to each other and so does the other leg. By doing so, there are three state of capacitor exist. The first one is charged state where SA and SD are off. Discharged is the second state where both SB and SC are on. The last state is bypass state where either SA and SC are on or SB and SD are on. This states are used such that energy is transferred through charged capacitor from Branch 12 to Branch 13.

One may notice that the use of the capacitor in the middle means that in a DC system this capacitor voltage must be stable under steady-state condition. This is because under such state the power exchange between the two lines must be balanced. This can be clearly seen from equation 2.7. It implies that not only the branch current needs to be regulated but also the capacitor voltage. Therefore, one full-bridge converter is employed to regulate the active power flow while the other one maintain the capacitor voltage.

In order to simplify the control algorithm analysis, duty cycle of SA and SB are set fixed to 0.5 and duty cycle of SC1 and SC2 is used to control the line current and capacitor voltage. Figure 2.14 shows how the device control its branch current by using the difference of duty cycle between SA and SC1. When the difference is positive, the capacitor will be charged and current I_{12} is reduced. This difference is controlled by means of negative feedback between the measured current and the reference value. A similar approached is used for the other leg to control the capacitor voltage as described in figure 2.15. Aside from the control during operational term, one remarks must also be made during the start-up phase. The device requires a certain amount of capacitor voltage to regulate the power flow. Thus, one must make sure such that the start-up condition enables the capacitor to be charged and a new steady state condition of the capacitor is reached.

$$P_c = 0 = \frac{d(W_c)}{dt} = \frac{d(\frac{1}{2}CV_c^2)}{dt} \tag{2.7}$$

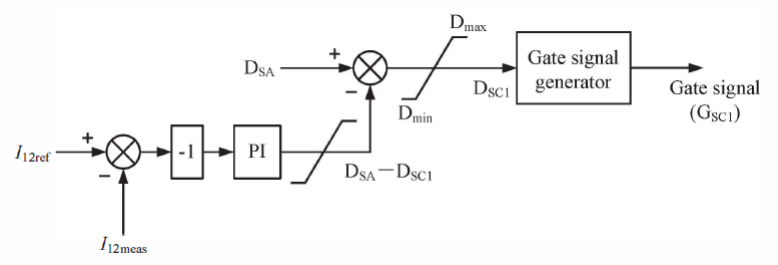

Figure 2.14: *SVS without AC link current control [4]*

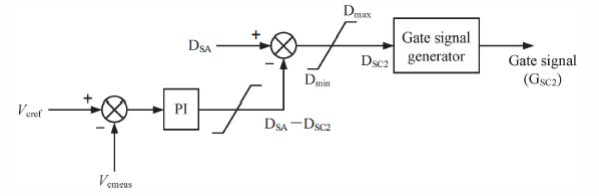

Figure 2.15: *SVS without AC link capacitor voltage control [4]*

2.3.2. LVDC DCPFC

There are not many DC power flow control which has been done in LVDC distribution grid. Paper [29] are among the few work which can be found. It present its case to solve the issue of independent link power control in a mesh network. This is due to the fact that local voltage is the only controllable parameters in DC distribution network and regulating the power of a DC cable using the node voltage would mean changes in power flow of other line as well. Moreover, DC node voltage is expected to be kept close to constant. It proposed a converter depicted in figure 2.16 to do the power flow control on the line. The principle of the converter and its relevant experimental result is discussed.

The converter proposed is made of two sets of two-quadrant chopper in back-to back connection with an inter-stage capacitor [29]. The converter port connected to the line has voltage of V_a and V_b is not on the same node with the grid node voltage as it is separated by line resistance. It works by inserting a series voltage across the line defined by V_link. The relation between V_link and V_a as well as V_b is determined by equation 2.8 and 2.9. The two voltage is controlled by the ratio of the duty cycle of the two legs as shown in equation 2.10. Thus, one value of V_a or V_b can be achieved by two sets of duty cycle. The control is done by clamping the duty cycle of the legs which would have higher dutcy cyle to 1. This way one leg is shorted and the other leg is switching. The paper has proof that this control method is able to regulate the power bidirectionally. The converter is proven in an experimental setup that it can regulate the power in the cable independent the the node voltage.

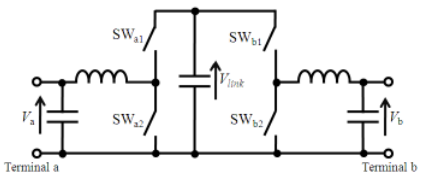

Figure 2.16: *A bidirectional Buck-Boost converter for LVDC power flow control in paper [29]*

$$V_{link} = V_a / D_a \tag{2.8}$$

$$V_b = D_b V_{link} \tag{2.9}$$

$$V_b = V_a D_b / D_a \tag{2.10}$$

2.4. DC Power Flow Control Converter Functions and Requirements in LVDC

Functions and requirements of a DCPFC device must sufficiently solve a defined problem in DC Distribution Grid. Although the main function of DCPFC is clearly impressed in its name, the level of power regulation needed determines its design. The function term power regulation includes a wide level of control. It could interpreted as defining the direction and magnitude of flowing power on the full grid rating. Its definition could also include only changing current to negative direction. Thus, for devices that can only reduce current, its function is limited as power limiter. Power regulation function is reserved for device that can control power in four V-I quadrants. Requirements, on the other hand, means a characteristic of the device that would allow it to behave as expected in its intended environment, e.g. partially rated. In order to determine the functions and requirements, it is beneficial to briefly discuss the meshed DC distribution grid as its environment and a specific problem that needs to be solved.

Due to more benefits offered by meshed DC grid in urban distribution network, it is used as the environment in which the functions and requirements of PFCC is evaluated. Urban distribution grid is expected to have more DC sources and loads including DGs as its power nodes. This coincides with the fact that meshed grid offers lower losses in DC distribution grid compared to other topologies and the losses is decreasing along with increasing number of DGs [20]. Those sources and other nodes are expected to exchange power bidirectionally. The distance between nodes are closer to each other than in rural area. Thus, it is more cost effective to create additional line for meshing network [21]. It must be noted, however, that urban distribution grid usually covers wide area. It has the possibility of having most nodes placed far from higher hierarchical voltage level whether it is DC or AC. It also open the chance that power can flow through the network longest path and creating a high voltage drop. In a particular or developing city, the highly dense population and limited space would create a complex network which needs compact and easily installed electrical infrastructure. These characteristics of urban distribution grid impose constraint to the development of PFCC in terms of its topology and operation.

There are several challenges of meshed urban DC distribution grid but PFCC must have functions that focus on solving problem that it can contribute best. Table 2.1 shows a summary of several DC power flow control paper both for HVDC and LVDC. One issue that these works consistently offer to solve is the line overloading in meshed DC network. This shows that the issue is critical to solve and power flow control can contribute best to ease the problem. Thus, line overloading prevention is a must have function for PFCC. An increase in one line can results in reduction of other line which also serves for this function. Therefore, this function is not limited to reduction of current in a cable. The ability to perform power regulation in four V-I quadrants could also be beneficial in reducing grid losses although all cables operate under its rating. Another issue which can be clearly spotted in discussion of urban DC distribution grid is the probable high voltage drop. PFCC might able to help solve this problem but it is not as critical as the network congestion issue. Thus, it is considered as a "nice to have" function of PFCC. With these two functions, SVS as the best form of power flow control is the most suitable option for PFCC. The converter should serve this two functions in a meshed urban DC distribution grid through inserting series voltage to a cable.

In order for the PFCC to suits urban DC distribution grid characteristic, a number requirements must be determined. One feature that certainly there in meshed LVDC network is bidirectional power flow. This is one of the most interesting benefits of meshed DC distribution grid as it increases reliability and best utilized the DGs and active loads. It was also discussed that the line overloading prevention is not limited to reduction of current. Thus, the first requirement of PFCC is that it must be able to operate in all four voltage and current (V-I) quadrants. Another thing that is expected from every converter is low power loss. This can be gained by designing a topology that has rating significantly lower than the DC grid itself. This partially rated feature is one characteristic of SVS and is included as the second requirement. Lastly, it was discussed that urban DC distribution usually covers a wide area far from higher hierarchical voltage level and can create complex network in a densely populated area with limited space. It means that external AC link is not an option. Furthermore, any link requirements to other cable would unnecessarily limit where the PFCC can be placed. Thus, the last requirement is the PFCC should not require any connection to other cable apart from the one it controls.

Table 2.1: Functions and Requirements of several series voltage source DC power flow control paper

No	Paper Title	Author	Functions	Requirements
1	Flexible Control of Power Flow in Multiterminal DC Grids Using DC–DC Converter	K. Rouzbehi et al.	Power limiter and regulator	Maintain stability of the grid
2	A modular bidirectional DC power flow controller with fault blocking capability for DC networks	Kish, Gregory J; Lehn, Peter W.	Power flow regulation and DC fault blocking	Modular and resistant to uncontrolled propagation due to external DC faults
3	Multiterminal HVDC With Thyristor Power-Flow Controller	Veilleux, Etienne; Ooi, Boon-Teck	Power flow regulator	Partially rated
4	A DC Current Flow Controller for Meshed Modular Multilevel Converter Multiterminal HVDC Grids	N. Deng et al.	Power Limiter	Accurate control of line current with low power loss
5	A multiport power-flow controller for DC transmission grids	Ranjram, Mike; Lehn, Peter W.	Power flow regulation	Partially rated and no external AC link
6	An IGBT based series power flow controller for multi-terminal HVDC transmission	S. Balasubramaniam et al.	Power Limiter	Partially rated
7	Flexible power flow control for next-generation multi-terminal DC power network	K. Natori et al.	Power flow regulation	No link to any other cable
8	Decentralized current limiting in meshed DC distribution grids	L. Mackay et al.	Power Limiter	partially rated

2.5. Summary of Chapter 2

Literature review has been done on LVDC distribution grid and DC power flow control device. Two main opportunities and challenges of LVDC has been discussed. Possibility of higher grid efficiency and better compatibility to DC sources and loads are the two opportunities that drives the research and use of LVDC distribution grid. Two critical challenges, however, needs to be solved for faster time to adaption of LVDC grid. Standardization is vital as stakeholders of changes in LVDC are not only the utility and customer but also the consumer electronic company. The lack of availability of day to day devices compatible to LVDC would hamper its development. On the other side, protection is an important aspect of the grid which needs to be developed more as it has not mature enough to provide fast and inexpensive protection. DC power flow control device is regarded as a component that can increase the attractiveness of LVDC by providing more controllability to the grid and help protect the cable from over-current. Principle and examples of this device on HVDC and LVDC has been discussed. It is thought that Series Voltage Source type of the device is the most lucrative option as it offer good range of control, low cost, and low grid losses.

Based on the studies, a function and three requirements have been decided to develop a new LVDC power flow control device:

Function

- Power flow regulation

Requirements

- Four V-I quadrants operation
- Partially rated
- Connection to other cable is not required

3

Power Flow Control Converter

This chapter demonstrates the needs of power regulation in LVDC mesh network and develops a simulation of its solution in the form of Power Flow Control Converter (PFCC). Firstly, a system level simulation is developed to present the problem that is trying to be solved by power control. The problems are congested line and high voltage drop. Secondly, a partially rated power flow control converter is introduced based on work on [21]. Thirdly, model for this converter is slowly developed starting from the Full-Bridge stage to the isolation stage and its incorporation to the grid model. Lastly, the simulation results are shown to show that the proposed converter can regulate power on congested line and compensate voltage drop over a long DC line in all four V-I quadrants.

3.1. Meshed LVDC Network Congestion and Voltage Drop

As discussed in chapter 2, meshed network for LVDC distribution grid is an attractive proposition to increase grid strength and utilization. Optimal operation of mesh network, however, does not come naturally. The overloading limit of power electronic converters, intermittent sources and abrupt changes of loads are few things that can create congestion on LVDC network. This issue can lead to suboptimal utilization of distribution line and even breakdown of infrastructure due to thermal limit of cable. Another issue that could occur is an unacceptable voltage drop due to high power demand in a long cable. This could happened in a large city with long network path on a peak hour. This two issues are in need of solution to increase the possibility of mesh LVDC network implementation in the future.

A simple hypothetical mesh grid with three nodes and lines is illustrated in figure 3.1 to describe the two issues clearer. It is safe to assume that DC load and sources can be connected to a voltage source converter (VSC) as a power electronic interface. This VSCs acts as the node in the mesh network which are depicted as DC1, DC2 and DC3. The line resistance 2 and 3 are the same (0.82Ω) while line 1 has resistance of 0.70Ω. At the beginning, both DC1 and DC3 are transferring power to DC2. Due to a disturbance, however, source DC3 is disconnected from the network. Assuming DC1 has enough power, this force DC1 to increase its power transfer to DC2. The current is divided into two path where the same value of current flows through R2 and R3 and the rest flows through R1. Due to Kirchoff's law and difference in line resistance, most of the current flow through R1. Ideally, 175A has to travel through line 1 and another 75A on line 2. The thermal limit of the cable, however, hits its maximum at 100A. Due to this, only 70% of the cable can be utilized while at the same time breaking down the cable, moreover, the power demand cannot be met. At the same instant, the voltage drop across the line is higher than the tolerated value. This voltage drop can disturb the grid as local variable that needs to be maintained on DC grid is node voltage. Suppose that there is a device that can regulate the line current, the cable life would not be threatened by the overheating due to line over-current, the utilization of the cable can be increased, and the voltage drop can be compensated.

In developing a device to solve the meshed LVDC issues, it is important to have sufficient model of the grid. The present condition, however, is that real world implementation of meshed LVDC distribution network is very limited. There is also a void of widely accepted standard for this grid. As discussed previously, there are several voltage standards and network configuration that are discussed in academic society. One interesting proposal is a bipolar network which is composed of poles with voltage in multiple of 350V. Using this concept, the network can be connected to generic and large load easier. This idea can be kept in mind as

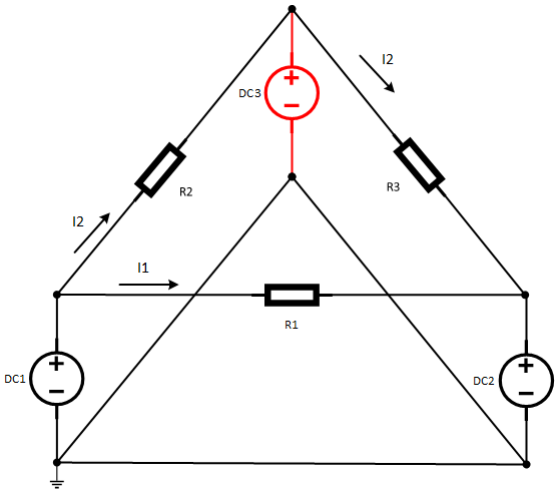

Figure 3.1: *An illustration of unipolar meshed network with VSC as nodes to demonstrate the issue of current congestion and voltage drop*

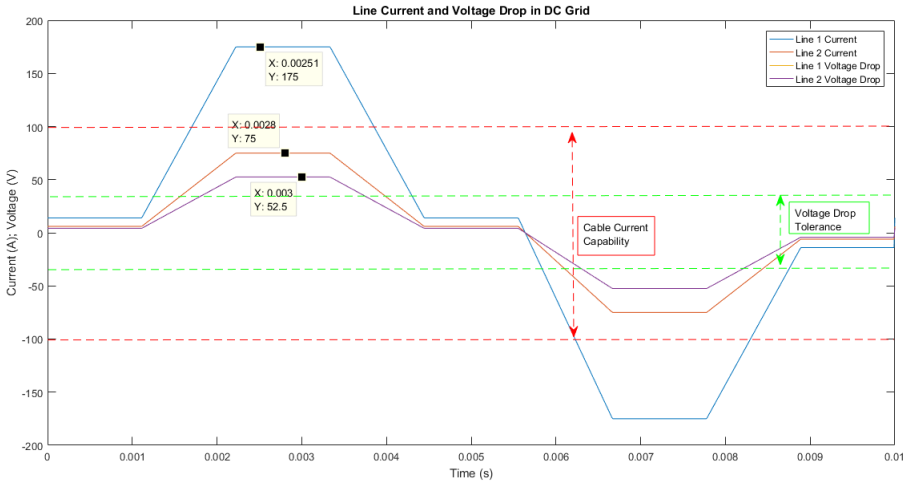

Figure 3.2: *A demonstration of network congestion and voltage drop based on illustration on figure 3.1. Ratio of R1:(R2+R3) is (1:2.3).*

a thought-basis to test the proposed solution in the future.

This thesis focus on the basic functionality analysis of possible solution to the power regulation issue in the form of new converter topology. The proposed solution should work on one pole by inserting a voltage series to the line to control power flow. Thus, at this early stage, it is unnecessary to develop complex meshed bipolar LVDC network. It is expected that if the converter works on a unipolar network, two of it can be connected to each pole of bipolar network and can still perform the same functionality. In order to validate the converter power flow control feature, it is thought that network with three nodes of voltage sources is sufficient. The line is enough to be modeled simply with resistance and inductance. The line capacitance in DC cables are usually small and can be neglected. The analysis of the basic functionality is done on the steady-state.

Issues of network congestion and voltage drop has been illustrated in this section along with the basic idea of the how the appropriate grid model should be. Congestion can be caused by several causes and creates a suboptimal operation of mesh LVDC network. A cable can be overheated and underutilized, threatening not only continuity of power transfer but also the protection of distribution infrastructure. With or without the congestion, a large voltage drop can also occur which endanger the stability of the grid as it is the local

variable that must be maintained. A basic idea of grid model is discussed to be used as a test environment for potential converter solution to these problem. Amid the uncertainty of standard and best practice of LVDC, a unipolar grid with three nodes and lines modeled as series resistance and inductance is considered to be sufficient for grid model. This is because the main purpose it to validate the basic functionality and analyze the performance on steady state.

3.2. PFCC Topology and Simulation Model

Paper [21] briefly presented one possible converter solution to the issues described in the preceding section. It has advantage of having fraction power rating of the grid which leads to an inexpensive and low losses solution. On top of that, it is only connected one line as oppose to SVS converter that needs additional link to AC sides or other cable. The proposed device uses a Dual Active Bridge (DAB) and a diode H-bridge to perform a series voltage insertion to the line. An improved version of the proposed solution is depicted in figure 3.3. All of the switches are realized using MOSFETs and its internal diode. This improved version is capable of performing power flow control in all four V-I quadrants. The basic idea, however, remains the same. One of its side is connected parallel to the line while the other side series to the line. The parallel side is defined as the input of the converter and the series part is the output. The parallel connected side is the isolation segment realized as DAB. Without this part, the converter would create a short circuit on a return path it creates between the positive of its input and output port. The isolation also acts as a voltage step down which allows the partial rating characteristic. Dual Active Bridge is chosen mainly due to its ability to have this high transformer ratio compared to other bidirectional DC-DC with isolation. Other reasons are that it has a lower number of switching devices for high power application [33]. This segment is connected to the Full-Bridge through a parallel capacitor to decouple the dynamic between the two cascaded segments and ease the control. The Full-Bridge is defined as the output regulator segment where it controls the series voltage to the line. The voltage across the decoupling capacitor C_{out} is always positive and acts as the input of the Full-Bridge. This way the output regulator segment can gives out both positive and negative series voltage regardless of the current direction on the line.

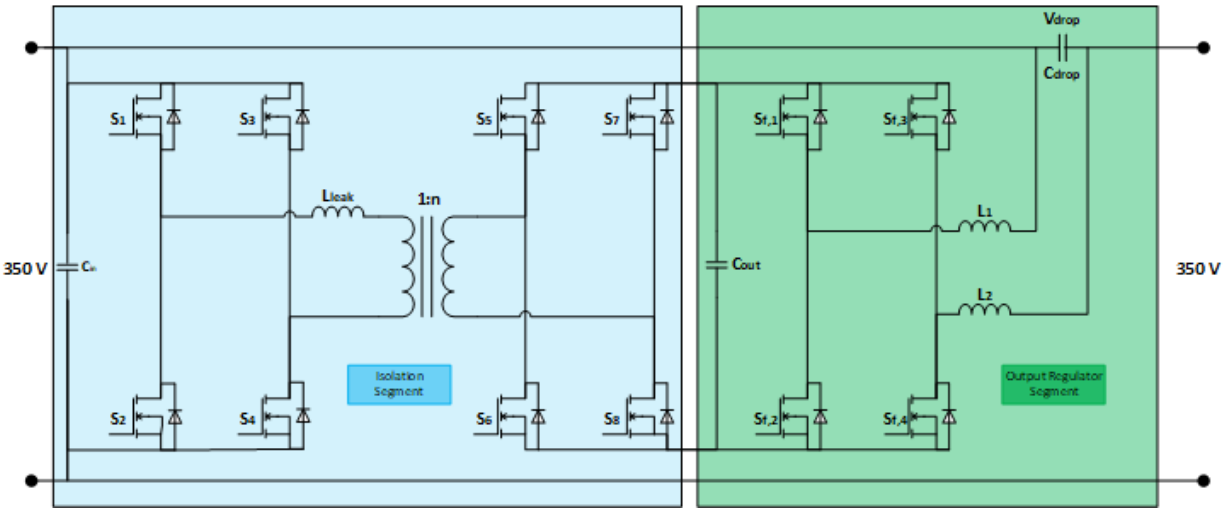

Figure 3.3: *An improved version of partially rated power flow control device. The isolation segment prevents short circuit connection between the positive of parallel connected side of the converter and the positive side of the series connected side. The output regulator segment receive a constant positive voltage from isolation segment and perform line power control in all four V-I quadrants.*

In terms of how the proposed converter regulate power, it behaves in a similar way as Series Voltage Source (SVS) described in chapter 2. In order to illustrate the power regulation principle with PFCC, a two nodes connected through one line is depicted in figure 3.4. Suppose that there is PFCC, DC power flow from VSC1 to VSC2 complies equation 3.1. PFCC influences this power flow by introducing a series voltage on the line. This changes the sum of potential difference between the two VSCs without changing the node voltage. This is important because the voltage of the VSC is maintained to be constant to ensure a stable grid. Using PFCC, the power flow can be controlled by complying to equation 3.2.

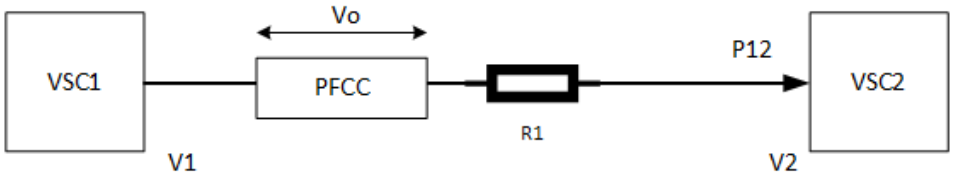

Figure 3.4: *An illustration of DC power transmission with series voltage insertion using PFCC. The series voltage allows control of power flowing through the line without changing the VSC node voltage which is important to maintain stability of the grid*

$$P_{12} = V_2 \frac{(V_1 - V_2)}{R_1} \tag{3.1}$$

$$P_{12} = V_2 \frac{(V_1 - V_2 - V_O)}{R_1} \tag{3.2}$$

In order to validate the capability of PFCC on controlling the power flow as wel as compensating the voltage drop, a simulation model must be built and tested. The first step is to develop the output regulator segment. This part is the key in controlling the power flow in four V-I quadrants. A sufficient model and control is developed based on PWM and PI controller. The isolation segment mainly acts to prevent the short circuit path between input and output port of the converter. Therefore, basically, all bidirectional DC-DC converter with isolation and high power ratio can do the job. As paper [21] uses DAB, the model of DAB is built to implement the isolation segment. The DAB controller use single phase shift control to gives out constant voltage as its output and complying with the current direction.

3.2.1. Synchronous Full-Bridge

This section discusses the topology used for output regulator segment and its modeling. The reason behind selection of synchronous full-bridge as this segment is first discussed. Afterwards, it is important to briefly discuss its operating principle before creating the model. There are few decision made in its operation principle that influence the modeling. Eventually, the specification of synchronous full-bridge circuit model is explained. The under-lying assumptions used are focused on estimating the functional validity of the PFCC. The control block used in the modeling is then explained.

The main objective of output regulator segment is to control the series voltage inserted to the grid. It receives an approximately constant voltage from isolation segment and step it down to a certain value that would change the line current. This must works in all four V-I quadrants to ensure full voltage control in bidirectional power. It is also the interface between the controlled grid line and PFCC. Current passing through the cable would pass via PFCC secondary side. Thus, it is important to have passive component that minimize the ripple created by PFCC switching operation. The two inductors minimize the current ripple on the line. Meanwhile, the capacitor smooth out the inserted series voltage. There are only few converter topology alternatives that can regulate the series voltage in four V-I quadrants that is capable of seamless integration to the grid.

Two full-bridge circuits are the few alternatives considered for this segment. Synchronous and non-synchronous full-bridge buck converter. Other step-down converters and half-bridge configuration cannot satisfy the four V-I quadrants requirement. The main difference between synchronous and non-synchronous full-brige lies on the use of external diode. Synchronous full-bridge uses its MOSFET internal body diode. This way the switch works bidirectionally. Meanwhile, non-synchronous full-bridge requires a diode parallel to its MOSFET. This leads to extra voltage drop for non-synchronous full-bridge. Intuitively, this would result in higher efficiency for synchronous full-bridge. This, however, is not always the case. Non-synchronous buck converter can outperform its synchronous counterpart at light load and high duty cycle [30]. This is due to the performance of MOSFET internal body diode which is not always better than external diode in terms of reverse recovery current. Thus, it increases switching loss for synchronous full-bridge. In PFCC application, high current is expected to pass through the switches as the grid current must flow via PFCC secondary side. Another advantage of the synchronous type, however, is a lower part count. This would result in a better reliability. Thus, synchronous full-bridge is choses as the output regulator segment due to its fewer component

counts.

The synchronous full-bridge works as a buck-converter in all four V-I quadrants. Equation 3.3 shows the duty cycle influence to the ratio of input and output voltage. PFCC inserts a positive series voltage to the grid when the duty cycle is more than 0.5 and a negative one when it is less than 0.5. The ability to control the output voltage to zero is also important when PFCC is not needed to control the power flow. It can let the energy in the passive component to be discharged before PFCC can be bypassed. The off-state of PFCC, however, is not the scope of this thesis. The dynamic to switched off the PFCC along with what would happen to the energy stored in the passive component during the turn off is left out for future works. Meanwhile, the passive component acts as a buffer to smooth out the ripple coming out of PFCC. The sizing of the inductor and capacitor depends significantly to the switching mode used.

$$V_O = (2D-1)V_{IN} \tag{3.3}$$

There are two options of switching mode which can be used for the synchronous full-bridge, unipolar and bipolar voltage switching. The main difference between the two is how each leg of the full-bridge is controlled. Unipolar voltage switching treated the legs as pairs. Switches in each pair are switched on and off simultaneously using one control voltage to be compared to a triangular waveform. Meanwhile, bipolar voltage switching treated the two legs independently using two different control voltage. Switching mode influences the required inductance and capacitance value because it defines the effective switching frequency of the inductor current and ouput voltage. Unipolar voltage switching offers better output voltage waveform and frequency response. This is due to its effective frequency which is double to the bipolar voltage switching. Implementation of unipolar voltage switching in practice, however, is more difficult than its bipolar counterpart. Thus, the normal switching frequency shall be used to determine the value of inductance and capacitance. Type of voltage switching, however, does not influence input and output voltage relation with regards to duty cycle. In conclusion, due to easier practical hardware implementation, unipolar voltage switching is used in synchronous full-bridge model.

The main objective of Synchronous Full-Bridge modeling is to validate the four quadrant operation given the topology. Thus, non-idealities and high accuracy of model specification is not the utmost priority. Influence of dead-band absence, switching losses, capacitor ESR, and winding resistance are neglected. Only MOSFET on-resistance is included. The model is expected to work at input voltage of 35V and output range of at least ± 20V. The current flowing through this stage is expected to be between 50A to 100A. The output voltage ripple must not exceed 1% of the maximum output voltage and the inductor current peak to peak ripple must not exceed 10%. A high switching frequency is preferred to reduce the size passive component and its losses.

Passive component values for the model is calculated. Peak to peak ripple current (ΔI_L) is determined by the sum value of the single inductance value (L), switching frequency (f_s), duty cycle (D), and input voltage. The maximum ripple current occurs when duty cyle is 0.5. Utilizing both equation 3.4 and capacitor voltage ripple (ΔV_C) formula 3.5, a set of single inductance value is traversed through a matlab program to determine possible pair of passive component values. The result is depicted in figure 3.5. It shows that pair of capacitance value higher than 26 μF and single inductance value more than 15μH will limit the peak to peak ripple current to 5A and voltage ripple of 2V. This value is sufficient for a 350V and 100A LVDC distribution grid model.

$$\Delta I_L = \frac{D(V_{IN} - V_O)}{2Lf_S} \tag{3.4}$$

$$\Delta V_C = \frac{\Delta I_L}{8Cf_S} \tag{3.5}$$

The model is controlled using control block depicted in figure 3.6. A negative feedback system is implemented with a duty cycle feed-forward. In the real application, a command for reference voltage is expected to be received by PFCC from a network-level control algorithm. In this simulation, however, an arbitrary value is given to demonstrate PFCC capability to regulate power flow. The reference value is compared to measured output voltage value across the synchronous full-bridge capacitor which passed through a low pass filter (LPF). The error is feed into a PI controller. The PI gained is tuned using the good-gain method to get a good transient characteristic. It is desired to have a dynamic that contains minimum overshoot and low steady-state error. The output of the PI controller is added to a 0.5 constant. This helps stabilize the control

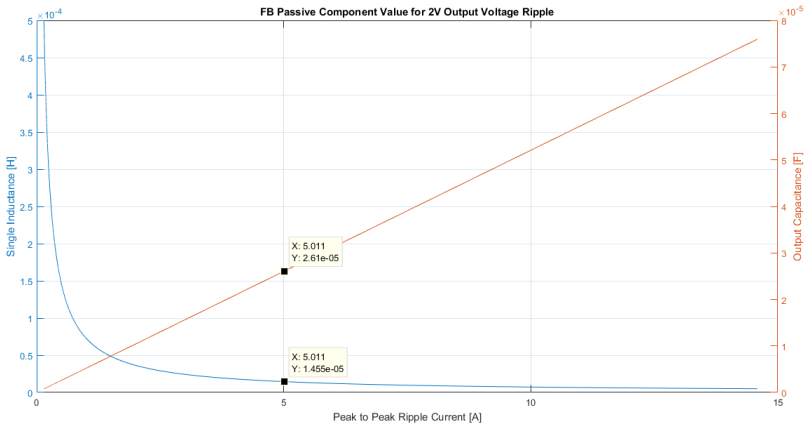

Figure 3.5: *Fullbridge passive component set of pairs for 1% grid voltage ripple with respect to corresponding peak to peak ripple current.*

as 0.5 duty cycle gives out 0V. The resulting duty cycle is then limited to a value between zero to one. This value is processed inside the Pulse Width Modulation (PWM) block to switch the MOSFET on and off.

An output regulator segment model has been developed. The selected circuit must be able to insert series voltage to the line grid in four V-I quadrants. Synchronous full-bridge topology satisfy that requirements and chosen due to its comparatively low conduction loss and minimum part counts. Its output voltage is controlled by its duty cycle where 0.5 marks 0V and the rest of the region gives out a stepped down positive and negative value. The ability to insert 0V helps the PFCC when power regulation is not required by the grid. The off-state implementation, however, is not the scope of this thesis. The synchronous full-bridge is controlled using bipolar voltage switching due to its easy hardware implementation. Based on this mode, a model was developed. Non-idealities such as switching loss, capacitor ESR, winding resistance and dead-band are neglected. The model was designed to perform on 100A and 350V grid model. In order to limit its influence to the grid current ripple and its output voltage ripple, total inductance of 30 μH and capacitance of 15 μF are used. A negative feedback control model is used to regulate the output voltage to a reference value. A model of synchronous full-bridge has been developed to estimate the operation of PFCC in controlling power flow in a DC grid.

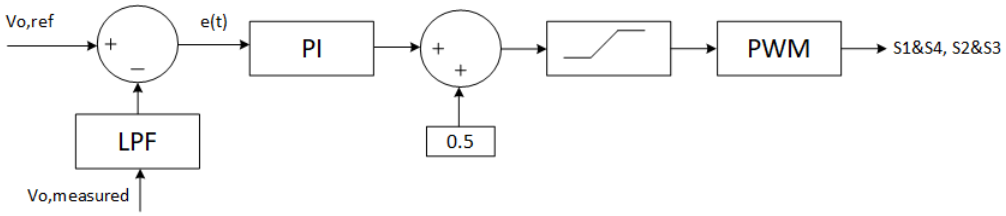

Figure 3.6: *Fullbridge Control Schematic*

3.2.2. Dual Active Bridge

This section discusses the topology used for isolation segment and its model for the simulation. The reason behind selection of Dual Active Bridge (DAB) for this simulation is explained. There a couple of converter topologies which can perform as an isolated bidirectional DC/DC converter. Two alternatives, however, stands out of the rest. It is A brief overview of LLC resonant converter and DAB is presented. Afterwards, a comparison between the two is discussed. Based on the selection, a model and its control was developed. The overview of circuit topology selected for DAB helped understand the PFCC and its modeling.

There are two converters which can be a good candidate to perform isolation segment role. This stage of the converter has two main functions. It has to isolate the connection between the input and output port. Otherwise, it would create a short circuit. On top of that, it should provide a constant ratio between its out-

put and input. This is imperative to create the converter partial power characteristic. Isolated bidirectional DC/DC converter topologies are the category suitable to perform these roles. In [40], the author compares those topologies with respect to DAB. Most of it, however, is inferior to DAB in high power application [40]. Moreover, DAB offers ease of realizing soft-switching. There is, however, a topology which offers a similar qualities to DAB, LLC resonant converter. As far as functionality is concern, DAB and LLC resonant converter can fulfill the role of isolation segment. It is important for future work, however, to understand the operation and comparison of DAB and LLC resonant converter.

An LLC resonant converter distinguished itself to other isolated bidirectional DC/DC converter by having a capacitor series to its high frequency transformer. This capacitance forms a resonant tank with the transformer leakage and magnetizing inductance. A full-bridge generates a square-wave to excite this resonant tank which will gives out a sinusoidal signal on the transformer secondary side. This waveform is then rectified and filtered by another full-bridge circuit. The converter voltage gain is defined by transformer ratio and its resonant tank gain. When the converter operates above its resonant frequency, the input voltage from the primary side will receive a boost from the resonant tank gain. The other way around happened when it operates below its resonant frequency, the input voltage will be stepped down by the resonant tank gain. The gain magnitude, however, is influenced by the level of the LLC resonant converter load. The topology can perform soft switching. Zero voltage switching (ZVS) is preferred because it is achieved in its inductive region. In capacitive region, the current leads the voltage. This means that the switch current is reversed before the MOSFET is turned off. After the MOSFET switched off, this current will force the body diode into a hard commutation once the other MOSFET is turned on. This would result in reverse recovery loss and high current spike. Overall, LLC resonant converter is a suitable topology for isolation segment with the capability of ZVS at its inductive region.

Dual active bridge works based on two full-bridge circuits connected its high frequency transformer. The full-bridge typically use MOSFETs as its switches. This way, it has bidirectional power capability. The switches can be modulated with in a variety of ways. The simplest one, however, is single phase shift control. The power transmission characteristic of this modulation technique is presented in figure 3.7. The power is regulated by controlling duty cycle on one of the full-bridge. The D and P_{SPS} represents the duty cycle of one MOSFETs in the full-bridge and the power transferred through the DAB respectively. When the duty cycle is positive or negative 0.5, maximum power is transferred. The power goes into the positive direction when the duty cycle is positive and vice versa. The power is defined by equation 3.6. The duty cycle is equal to ϕ/π with ϕ is the phase angle in radian. The DAB is also able to perform soft-switching using the leakage inductance of the transformer. However, the ZVS can be lost at light load. A DAB can be designed to perform ZVS at an extended range of loads. This is done at the expense of more reactive current which would result in higher conduction loss. In conclusion, a DAB modulated by single phase shift control is sufficient to act as the isolation segment.

$$P = \frac{nV_{primary}V_{secondary}}{2\pi^2 f_s L}\phi(\pi - \phi) \tag{3.6}$$

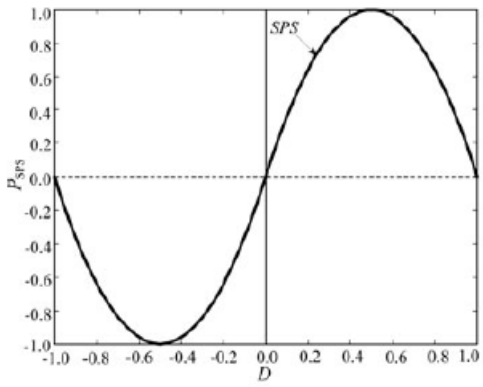

Figure 3.7: *Dual Active Bridge phase shift to power magnitude relation [40]*

The main differences between DAB and LLC resonant converter are its efficiency characteristic. Paper [13] compare the two topologies. The difference in efficiency is due to the characteristic of its ZVS. LLC resonant

converter can perform ZVS at wider load range as long as it is in its inductive region. This is achieved, however, at the expense of higher conduction loss due to more energy is circulating in LLC resonant tank. DAB has lower conduction loss but the range of ZVS is more limited. At high power application such as distribution grid converter, conduction loss could be a more significant concern than ZVS range. Thus, it is possible that DAB is a better choice for PFCC isolation segment.

The purpose of DAB model is to act as the isolation segment in the figure 3.3 and help estimate the power regulation function of PFCC. The DAB must be able to demonstrate its ability to isolate the connection between input and output port as well as providing a step-down ratio. Thus, similar assumptions to synchronous full-bridge is also used for DAB model. Apart from the switches, there are three components in the DAB model. The two of them are capacitor at the input and output of DAB. The role of these capacitors are to decouple the DAB ripples from the synchronous full-bridge and the grid. Thus, a sufficiently large value of 100 μF is used for both capacitors. The transformer is rated for 10kVA and 200kHz with transformer ratio of 7:1.

The model is controlled using SPS modulation and PI block as depicted in figure 3.8. An output voltage reference is set to a constant value of 35V. It is compared to the measured and filtered value of the output voltage. The error is fed into a PI block and limited to a value between zero and one. The resulting duty cycle is converter to a phase shift value to create a delay between the primary and secondary side. This way the magnitude and direction of the power transferred through the DAB is controlled.

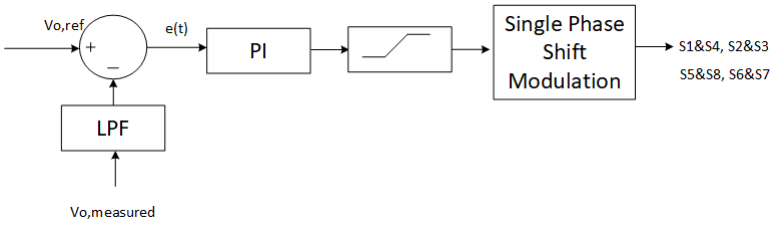

Figure 3.8: *Dual Active Bidge Single Phase Shift Control Schematic*

A topology for isolation segment has been selected and modeled. DAB and LLC are good candidate for this part of PFCC. The efficiency characteristic of DAB, however, is more suitable to a high power application such as PFCC as it has lower conduction loss. A model of DAB was developed. It is modulated by single phase shift technique and controlled through a negative feedback system and PI controller.

3.3. Simulation Results of PFCC Operation on Meshed LVDC Network

DC grid has been modeled in figure 3.9 and 3.13 for validating PFCC function. Although the proposed converter has the potential to be implemented in bipolar DC distribution grid, a unipolar grid is used for the sake of simplicity. This is considered as a sufficient model as the first step in validating the converter function. Further research on its implementation on bipolar grid, however, is necessary. As the power flow might influence the current flowing in the neutral of bipolar gid. In the meantime, figure 3.9 is use to show the power regulation function of PFCC. This model contains three nodes of DC sources. The network is congested and requires a power flow regulator action. The second model in figure 3.13 is made to resembles the experimental configuration used. The network is a simplification of the scenario shown in figure 3.1 where one out of three DC sources is turned off. This leaves the two DC nodes connected through two lines. Simulation with this model is used to show the four V-I quadrant operations and partial power characteristic of PFCC.

3.3.1. Simulation of PFCC Power Flow Regulator Function

A meshed distribution grid with three DC nodes depicted in figure 3.9 is used to simulate power flow regulator function of PFCC under a congested network condition. The three nodes are composed of one DC source (DC_1) and two active loads (DC_2 & DC_3). The DC nodes are modeled with simulation block depicted in figure 3.10. The source capacitance (C_1)is defined as 1mF while the internal resistance (R_1) is 0.1 Ω. The DC source (DC_1) is set as constant voltage value while the two active loads (DC_2 & DC_3) are set to value between 300V to 400V. Three lines of equal length of 1 km are connecting the three nodes. Each line has resistance of 0.188 Ω per km and inductance of 358 μH per km. The cable has current limit of 100A. Several measurement for the test scenario in this grid model is presented to show the power regulation function.

There are eight measurements needed to be displayed to clearly show the ability of PFCC to regulate power flow. The first three parameters are the voltage of DC nodes. These values determines the power flowing in the grid with respect to the resistance. Reference values for the sources as VDC depicted in figure 3.10. Thus, the source voltage that is impose to the grid can be higher or lower due to the its internal resistance R_1. The change in a source voltage is influenced by the dynamic introduced by its capacitance C_1. The other three parameters are the line currents. The DC node voltage is expected to varies close to its steady state value. Meanwhile, the change of power flow is represented by the current flowing through the DC cables. The other two parameters represent the action of PFCC in regulating the power flow. The series voltage inserted to the line is measured as V_o. This value is controlled by setting a reference value and minimizing the error to the measured value using a PI control block. $PFCC_{Vo}$ is shown, however, to observe the influence of PFCC to the grid better.

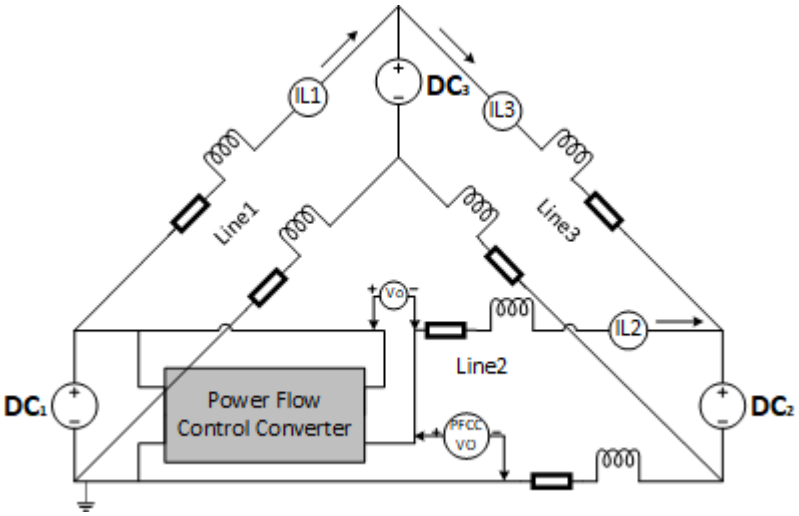

Figure 3.9: *Meshed LVDC grid model with three nodes to simulate PFCC power regulation function*

The result of a congested network scenario is presented in figure 3.11 and 3.12 to show ability of PFCC to control the line current. Prior to the simulation, the current in line 2 has increased to more than 100A and exceeding its rating. At first, each DC node has its own constant value dictating the value of the current

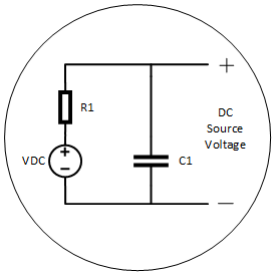

Figure 3.10: *DC source used in grid model of figure 3.9*

flowing in the grid. $PFCC_{Vo}$ shows a same voltage value with DC_1. In order to reduce the line current in line 2, the PFCC inserts a 12V series voltage to the grid. $PFCC_{Vo}$ decreased to 368V due to this inserted voltage. As a result, the current in line 2 is decreased to an acceptable value. This is done at the expense of an increased in both I_{Line1} and I_{Line2}. The series voltage can be seen as an additional voltage source that adds positive current to both of the increased currents. Another thing that is interesting to observe is the change in DC_2 voltage. Ideally, it is desired for the node voltage to maintain its value when PFCC perform power regulation function. From this simulation, it can be seen that the node voltage changes due to voltage drop across its internal resistance. It shifts slowly to a lower value because of the high capacitance value of DC source capacitor. This shows that PFCC power regulation action can influence the stability of node voltage depending on the value of the node capacitance, resistance and the current flowing in the grid. The change in node voltage, however, is less than 5V in this case. Thus, the simulation shows that the PFCC can relieve the congestion in the network by inserting a series voltage on the line it is connected.

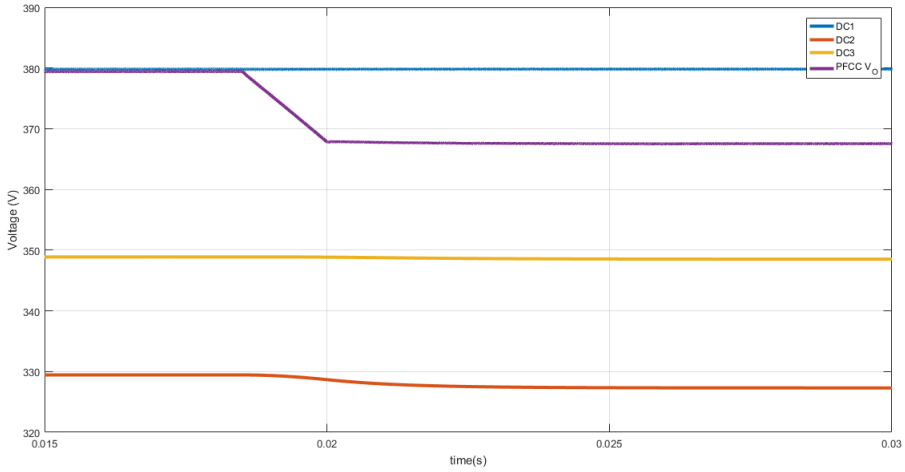

Figure 3.11: *Voltage value of nodes of figure 3.9 and the potential difference between PFCC output and ground (PFCC V_o). These values mean the current flows from DC1 to DC2 through line 2 as well as line 1 and 3.*

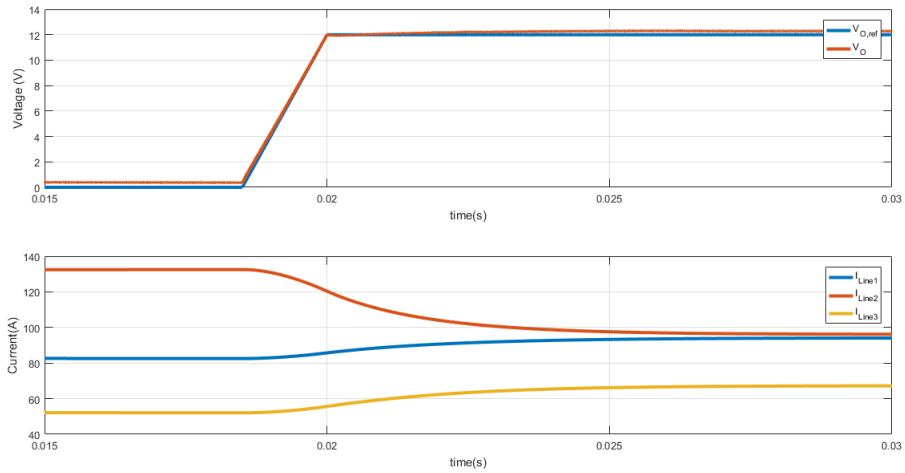

Figure 3.12: *Simulation of PFCC power regulation function. This graph shows that the inserted series voltage to the line reduces the line current*

3.3.2. PFCC Partial Power and Four V-I Quadrants Operation

Another simulation is made to show the ability of PFCC to regulate current in both direction and change its power. The simulation model is shown in figure 3.13. It is basically demonstrating the event on figure 3.1 but as the $DC3$ is disconnected that leaves two voltage source connected through two lines. DC1 and DC2 is allowed to change between 300V to 400V. R_s are series resistance of the sources which has value of one over eight of $RL1$. Meanwhile, $RL2$ is two times larger than the the sum value of line resistance one $RL1$. The value of $RL1$ is 1.88 Ω. The two load resistance are 5.3 Ω. Two scenarios are simulated two show the four quadrant operations of PFCC. In the first scenario, DC1 is set to be 380V while DC2 is 330V. The current measured in i_L1 is flowing towards DC2 showing a negative value. The second scenario is set to be the other way around where DC2 is higher than DC1. On both cases, PFCC is set to give out $\pm 10V$. The result of first scenario is presented in figure 3.14 while the second one is on figure 3.15. The power processed inside PFCC is also shown in figure 3.16. These figures shows the partial power and four V-I quadrants requirement of PFCC.

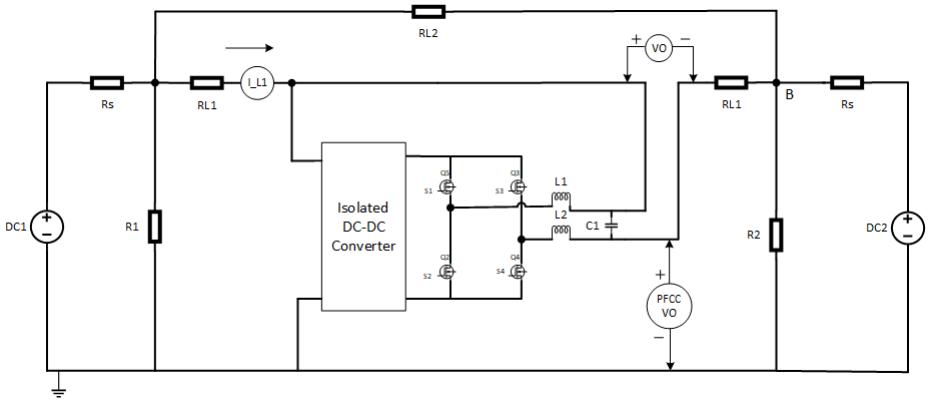

Figure 3.13: *Two nodes LVDC grid model to simulate four V-I quadrants operation of PFCC and the partial power processed in it.*

The result on figure 3.14 and 3.15 are analyzed. PFCC inserts $\pm 10V$ in the two scenarios with negligible steady state error. In figure 3.14, this voltage is inserted into a positive line current. Meanwhile, a negative current is flowing in figure 3.15 while the PFCC outputs $\pm 10V$. The current flowing is also regulated in response to the inserted series voltage. These shows that PFCC has successfully regulate power flow in all the four V-I quadrants. There are, however, a notable difference between its operation in positive and negative current direction. There is a difference in the value of current flowing in the grid line. The maximum value of current is 20A higher when it is flowing in negative direction than when it is positive. The cause of this might be found by analyzing $PFCC_{VO}$. This value is 10V higher when $DC2$ voltage acts as the main source with voltage higher than $DC1$. This is due to the fact that PFCC topology is not symmetrical from the source point of view. Overall, the PFCC has shown that it is capable of regulating power flow in all four V-I quadrants.

Figure 3.16 shows the comparison of the power flowing through the line PFCC is installed and the power processed at the output side of PFCC. The line power is calculated with current measured at the point of I_{L1} in figure 3.13 and the voltage across R1. On the other hand, the PFCC power is calculated at its output using the current flowing through RL1 and the absolute value of its output voltage (VO). The figure shows that the power processed at the output of PFCC is approximately the ratio between the grid voltage interfaced with PFCC input port and the value of series voltage inserted by PFCC to the line. When negative 10V is inserted, the power ratio is 1/45. Meanwhile, the positive 10V results in 1/38 power ratio. This difference is due to the value current flowing into the input port of PFCC where the current measured at I_{L1} is the sum of PFCC input current and the current flowing through RL1. To conclude, it is shown that PFCC is processing only a fraction of the power flowing through the grid with a ratio between the inserted series voltage and the grid voltage.

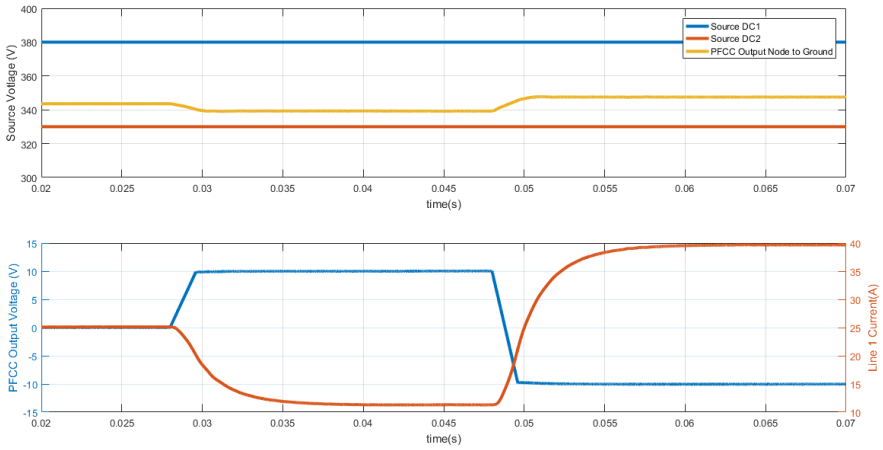

Figure 3.14: *PFCC operating in two V-I quadrants, a positive and negative output voltage in a positive current flow.*

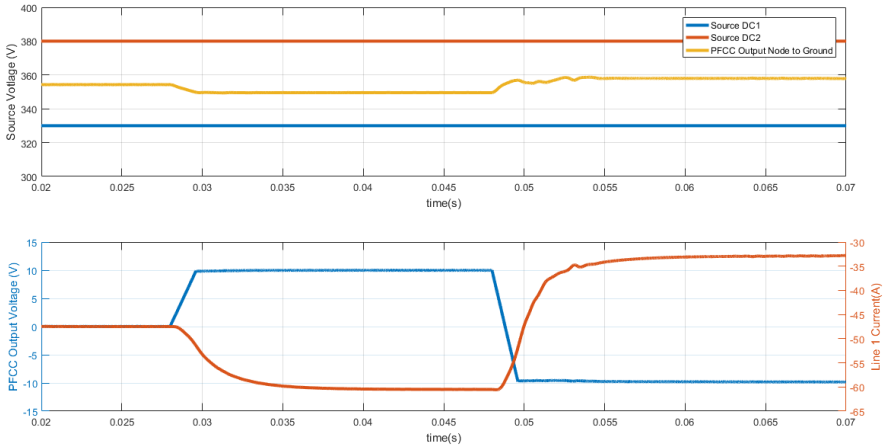

Figure 3.15: *PFCC operating in two V-I quadrants, a positive and negative output voltage in a negative current flow.*

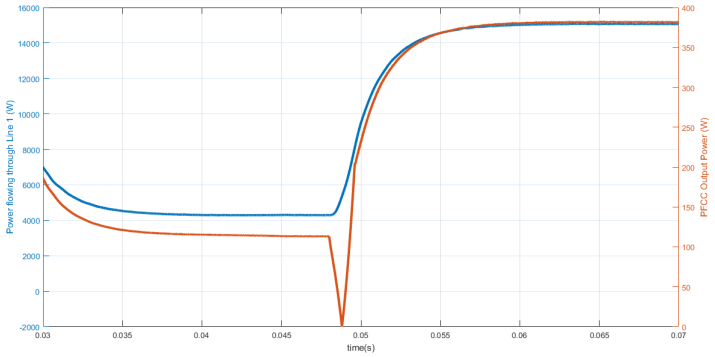

Figure 3.16: *Comparison between the power flowing through the line grid and the power processed at the output port of PFCC. The proposed converter only processed a fraction of the grid line power.*

3.4. Summary of Chapter 3

In this chapter, a model has been developed to simulate the power regulation function and its requirement for four V-I quadrants operation and partial power. In the first section of this chapter, the problem that needs to be solved by PFCC is defined. Meshed LVDC network could face an issue of network congestion. This would result in suboptimal operation of the grid. A proposed topology for PFCC and its model is discussed in section 2. The converter is composed of two segments, the isolation segment and the output regulator segment. Few alternatives for these stages have been briefly discussed. Although the selection is has not been proven to be the best option for each stage, it is decided that Dual Active Bridge is modeled for the isolation segment and a synchronous full-bridge for the output regulator stage. The Dual Active Brige is suitable with higher power application due to its lower conduction loss compared to LLC resonant converter. On the other hand, synchronous full-bridge is chosen because of its lower part count compared to non-synchronous full-bridge. Both models are controlled using a separate PI block. The Dual Active Bridge is modulated using Single Phase Shift modulation. In the third section, PFCC power flow regulation function and its requirement is simulated. It is shown that PFCC can regulate power flow in a unipolar meshed grid with three nodes by inserting a series voltage to the line it is installed to. Four V-I quadrants operation has been successfully simulated. The power processed in the converter is shown to be fractions of the power flowing through the line with an approximate ratio between PFCC output voltage and the grid voltage at the input of PFCC.

4

Prototype Design

In this chapter, a hardware prototype is designed as PFCC proof concept. First, a requirement for the prototype is defined as well as the method to develop it. Afterwards, the design is presented starting from the isolation stage, the full-bridge and its passive component, the control and measurement realization, thermal management, up to PCB design. The components selected are also outlined in each respective sections.

4.1. Prototype Specification

Experimental validation is imperative to prove the concept of PFCC. Simulation has shown promising results which are aligned with the function and requirements. It shows that the topology proposed can regulate power flow in four quadrants with partial rating operation and does not require connection to any other line apart from the one it is installed to. Voltage drop compensation function is implicitly aligned with the power flow regulation. This is because the PFCC works by inserting a voltage drop/gain to the line. The simulation results, however, does not necessarily prove the concept due to simplification of the model. Thus, power flow regulation function along with its requirement must be validated in a lab scale experiment. In order to do so, it is important to understand the available resources in the laboratory, the experiment focus and develop a specification for the prototype.

The prototype is built around the specification of DC sources available in the laboratory by considering several constraints such as time. The highest power DC supply available is N5772A Agilent Technologies with 1.56kW nominal power, 600V and 2.6A. There are four of this power supply which can be set in a master-slave configuration. At least two nodes are needed to do the experiment. Suppose that 350V is used to represent the unipolar grid, the power supply can be paralleled to increase the current rating to 5.2A. None of the power supply can be a sinking source. Thus, the power circulating can be increased up to 1.82kW. It is important to note, however, that in the middle of the thesis, a larger power supply was thought to be available. In the real application, one would go for 10% of the grid to show the partial rating but the converter would operate in partial power based on the voltage ratio of the isolation segment regardless of the rating of the converter. Thus, it is beneficial to protect the prototype from unintended failure by increasing the rating. This would help in complying with the time constraint of the thesis. The parts that are required to be built also need to be adjusted due to constraints. Building the two segments as a separate converter without prior experience would require a large amount of time and support. As there are modules for DC-DC converter with isolation and it is necessary to build the inductor in-house, it is decided to only build the full-bridge stage.

The specification of the prototype is listed on table 4.1. The power rating is based mainly on the grid voltage and the expectation of the PFCC prototype maximum power value between 25% to 50% of the DC source nominal power. The nominal voltage of the test grid is defined as 350V and it is reasonable to allow voltage swing in the range of ± 5% to 10%. The maximum input voltage is set to 385V. The output voltage of PFCC is the potential difference inserted in series to a line. It has a probability to modify the voltage value experienced in the input voltage. Thus, it is limited between ± 25V. High frequency of 120kHz is used to keep the passive component in a reasonable dimension.

Table 4.1: PFCC prototype specification

Parameter	Value
Maximum Power	525 [W]
Maximum Input Voltage	380 [V]
Voltage Output Range	± 25 [V]
Maximum Output Current	± 60 [A]
Switching Frequency	120 [kHz]
Output Voltage Ripple	1%
Output Current Ripple	15%

4.2. DC-DC Isolation Segment Module Selection

A module of DC-DC converter with isolation has two important roles to prevent short circuit on the return path and provide voltage ratio between the output and input port. Dual Active Bridge is one among few topology that can provide these two roles. Ready-made commercial Dual Active Bridge module, however, is expensive and has a large dimension. Thus, it is not preferred. LLC converter module, on the other hand, can be acquired with less cost and higher power density. Therefore, it is used for this prototype. Nonetheless, it is important to understand important parameters that would influence the design of full-bridge and to select a module that suits the experiment needs.

There are only a few considerations that need to be taken into account when incorporating an LLC resonant converter module. The difference between Dual Active Bridge and LLC resonant converter mainly lies on the characteristic of the losses [14]. Dual Active Bridge achieves Zero Voltage Switching (ZVS) using the energy stored in the transformer leakage inductance. It means the circulating energy in Dual Active Bridge is lower compared to LLC resonant converter which uses magnetizing inductance. This results in lower conduction losses in Dual Active Bridge. This advantage is gained at the expense of ZVS lost at light load. On the other hand, LLC resonant converter can achieve ZVS over the entire load range. Apart from that, LLC resonant converter would behave similarly to Dual Active bridge with respect to the load at its secondary side. In the PFCC case, the step-down transformer ratio would not only influence the voltage and current but also the capacitance value. Switching frequency on the secondary side would introduce current ripple to the full-bridge. This dynamic would influence with the separated control for full-bridge. However, LLC resonant converter in buck operation would have a higher frequency than its resonant frequency which would help ease the requirement on output filter and separating the dynamic of the two cascaded converters. Despite of that, the output filter of the LLC resonant converter and the influence of its dynamic to the control of the full-bridge needs to be dealt carefully.

The module used for PFCC prototype is VICOR BCM^{TM} with specification listed on table 4.2. The primary side voltage of the module would experience 350V which means with the ratio of the converter the output voltage would ideally be 43.75V. This means that it can handle secondary current up to 18A with an 800W load. The converter gain of 1/8 would mean that the power processed inside the PFCC prototype would be 12.5 % of the power circulating on the line it is controlled. The module has a requirement for maximum allowable output capacitance value due to its short circuit protection. The module only starts to work when the primary side voltage is 260V. An increase to that value within a short amount of time would trigger an unacceptable starting current if the output capacitance is more than 100 μF. It is important to note that the output capacitance of the full-bridge might influence this value as well. The primary side would experience a capacitance eight times the value on the secondary side. However, 100 μF should be more than enough to filter out ripple from both the module and full-bridge. With that, VICOR BCM^{TM} fulfills all the specification stated for the prototype.

4.3. Full-bridge MOSFET Selection

Synchronous fullbridge use MOSFETs to carry current in positive and negative direction by utilizing its internal diode and block a voltage only in one direction. Thus, the selection of MOSFET as well as its mounting type would influence the robustness and efficiency of the prototype. Among the fullbridge component, the switches are one the most prone to failures and mistakes in experimentation. Parameters such as forward current rating, voltage rating, dV/dt capability, and internal diode reverse recovery peak current are indicators for its robustness. Meanwhile, efficiency is mainly influenced by parameters such as its on-resistance, charge

Table 4.2: Specification of DC-DC converter with Isolation Module used. VICOR BCM380x475y800A3z.

Parameter	Value
Maximum Secondary Side Power	800 [W]
Primary Side Voltage	260 to 410 [V]
Secondary Side Voltage	32.5 to 51.3 [V]
Converter Gain	1/8
Switching Frequency	1.18[MHz]
Maximum Allowable Output Capacitance	100 [μ F]

stored in its gate-drain capacitance, and switching frequency. Thus, selection of the MOSFET was done by evaluating the mounting-type and parameters that influence robustness and efficiency of the prototype.

There are basically two MOSFET mounting alternatives. The first one is Through-Hole technology. It is installed to the board by using leads of an electrical component that is inserted into holes that are drilled on the Printed Circuit Board (PCB). This type provides strong mechanical bonds to the board. It is easy to install and remove the component. This mounting type, however, requires more space and usually more expensive. In the implementation of PFCC, the parasitic of Through-Hole can also increase its switching losses. The current in DC distribution grid can be more than 100A. The heating management typically depends mainly on its heat sink if there is no higher level cooling system. In the actual PFCC, it is expected that the converter uses SMDs and can handle the management only through passive cooling. Thus, although Through-Hole technology is a better option for prototyping, SMD is used.

Three SMD MOSFETs key specifications are listed on table 4.3. The drain source voltage and current rating were decided to be significantly higher than prototype specification due to the use of SMD and probable failure in assembly and experiment. Three other parameters are compared to gauge the MOSFET loss. The value of gate-drain capacitance determines the turn-on and turn-off time of MOSFET switching. Thus, it is an acceptable parameter to estimate the switching loss. Due to the complexity of gate-drain capacitance value, it is not stated as one particular value in the datasheet. However, its value is directly proportional to gate-drain charge. Internal diode voltage drop and drain-source on-resistance indicate the conduction loss of MOSFET. When positive current pass through a MOSFET, the drain-source on-resistance along with the magnitude of current defines its conduction loss. Internal diode voltage drop, on the other hand, define the conduction loss in the negative direction. Infineon IPB027N10N3 G was chosen due to its superiority on its conduction loss and only second to Fairchild MOSFET with a slight difference.

Table 4.3: Comparison of Full-bridge MOSFETs alternatives

Parameter	IPB027N10N3 G (Infineon)	FDB86135 (Fairchild)	BUK965R8-100E (NXP)
Maximum Drain Source Voltage [V]	100	100	100
Maximum Drain Source Current [A]	120	120	120
Gate-Drain Charge [nC]	27	25	51
Internal Diode Voltage Drop [V]	1.2	1.25	1.2
Drain-Source On-Resistance [m Ω]	2.7	3.5	5.8

4.4. Full-Bridge Passive Component Design

There are three passive components that need to be designed for full-bridge. At the output side of the full-bridge, value of capacitor and inductor is closely tied to each other in order to filter out AC component from influencing grid current ripple. Therefore, the value of both components is calculated first before proceeding to the determination of input capacitor and component selection.

The value of output capacitor and inductor are determined based on equation 4.1 and 4.2. First, the total inductance of two symmetric inductors is calculated based on the ripple current. This value would be maximum when the duty cycle is 0.5 which means the output voltage is zero. Using the ripple specified for the prototype, inductance and capacitance of full-bridge output filter were found. It is decided that the capacitance value must be more than 10 μ F and the inductance must be more than 30 μH.

$$L = (V_d - V_o) * (V_o + V_d) / (2 * V_d * F_s * I_{ripple}) \tag{4.1}$$

$$C = I_{ripple}/(8 * F_s * V_{ripple}) \tag{4.2}$$

4.4.1. Capacitor Component Selection

The output capacitor is connected in series to the line and parallel to the output of the fullbridge. It means that the capacitor must handle the grid ripple current and withstand the maximum output voltage of PFCC. It has to also serve to keep the output voltage ripple down. In chapter three, a range of capacitor value that can be chosen to keep the output voltage ripple less than 0.35V has been presented. As long as the single inductor is kept at a value above 32uH, the output voltage ripple can be pushed below 1.75V if the capacitor value is more than 10 μ F. The capacitor value is selected to be 30 μF.

CKG57NX7R2A106M500JH capacitor manufactured by TDK is selected. It is an X7R 10uF capacitor with 100V voltage rating. It has stable capacitance value across temperature rise up to 10 degree celcius and frequency range up to 1MHz. It also can kept its capacitance value above 77% of its nominal value with DC bias up to 35V. Under 100kHz switching frequency, RMS ripple current of 4A only takes a temperature rise of 1.8 degree celcius. Based on this facts, this capacitor is chosen.

The input capacitor decouples the two converter segment allowing ease of control implementation. Thus, a large value possible is preferred. It is important to note, however, that DC-DC isolation module impose a limit on maximum capacitance value on its secondary side due to its short circuit protection. The maximum capacitance value allowed in the secondary side of the module is 100uF. Simplifying the calculation to take into account the fullbridge output capacitor, maximum value that can be chosen is 70uF. Thus, 47uF is chosen to leave a room for reliability such that external capacitance on experiment setup would not interfere with DC-DC with isolation module. Value of the peak to peak ripple current flowing out of the isolation segment is the value of the grid current.

GRM31MR72A474KA35 capacitor manufactured by Murata is selected for the fullbridge input capacitor. It has 0.47uF capacitance value and 100V voltage rating. The datasheet shows that with 200kHz swiching frequency and 1A RMS current ripple the temperature can rise up to 10 degree celcius. It is expected, however, that with lower switching frequency, the temperature rise can increase exponentially with the same RMS current. Considering that the ESR on 100kHz is only 0.03Ω, 100 of this capacitor will be set in parallel to each other to form 47uF total input capacitance and withstanding 100A RMS ripple current.

4.4.2. Inductor Component Design

Two inductors with a value of 34uH each are required at the output of the full-bridge. An inductor design method based on core geometrical constant (K_g) [6]. This is best used when DC copper loss and winding resistance are the significant constraints. It is suitable for this prototype as DC is expected to flow through the inductors. Ferrite core is used due to the high switching frequency in modulating the full-bridge MOSFETs. A database of numerous ferrite core dimension and properties are used. Calculation of ferrite-based inductor parameters is done by first selecting a core which has a sufficient core geometrical constant and followed by computation of the required air gap, turns, and wire size.

Core geometrical constant is a measure of core magnetic size by taking into account significant parameters in four design constraints. In designing an inductor, the goal is to prevent it from saturation when a certain peak current passed through and to minimize losses. These goals are limited by design constraint. The first one is maximum flux density (B_{max}). This determines the peak current (I_{max}) that can flow through an inductor. The maximum flux density of the chosen core must be higher than the value of equation 4.3. The turns ratio (n) and air gap length (l_g) are unknown variables. The second constraint is the inductance value L itself. Equation 4.4 represents one symmetrical inductor. Core area (A_c) is an unknown variable. The third constraint is the winding area. This determines the maximum combined value of turns and cross sectional area of the conductor (A_W) used. It must fit in the core window area (W_A). Type of conductor, however, influence the area that is filled effectively. Thus, a fill factor (K_u) is used to indicate this. As Litz wire is going to be used due to the high switching frequency, a fill factor of 0.3 is used. The fourth constraint is winding resistance (R_L). This determines the copper loss of the inductor. Equation 4.5 represents the value of winding resistance. It is a function of conductor material resistivity (ρ), the number of turns, window area, and mean length per turn (MLT). Using these four constraints, unknowns variable are eliminated. This forms equation 4.6. The right side consists of variables from the specification and other known values while the left side is core geometric quantities. In order to satisfy inductor specification, the value of quantities on the left side referred as core geometrical constant (K_g), must be greater to those on the right side.

$$B_{max}\frac{nImax\mu_o}{l_g} \tag{4.3}$$

$$L=\frac{\mu_o A_c n^2}{l_g} \tag{4.4}$$

$$R_L=\frac{\rho n(MLT)}{A_w} \tag{4.5}$$

$$\frac{(A_c)^2 W_A}{(MLT)} \geq \frac{\rho L^2 (I_{max})^2}{(B_{max})^2 R K_u} \tag{4.6}$$

The calculation is done iteratively to find appropriate value of core factor based on equation 4.8 up to 4.12. Firstly, the air gap (l_g) is calculated based on the core cross sectional area (A_C) and its maximum flux density. Secondly, the number of turns is determined. Thirdly, based on the window fill factor, the number of turns and the core winding area (W_A) the maximum diameter of the wire D_{max} is found. In addition to that, skin depth (S_D) is also calculated to reduce copper AC losses. Thus, Litz wire is used. It means that a single Litz wire strand must not exceed S_D and the total diameter must not be more than D_{max}. Lastly, the power dissipation is calculated based on the core Mean Length per Turn (MLT).

$$K_{g(min)}=\frac{(L^2)(I_{max}^2)}{RK_U(B_{max}^2)}\rho 10^8 \tag{4.7}$$

$$l_g=\frac{\mu_{air}L(I_{max}^2)}{A_C(B_{max}^2)}10^4 \tag{4.8}$$

$$n=\frac{nLI_{max}}{B_{max}A_C}10^4 \tag{4.9}$$

$$D_{max}=\sqrt{\frac{K_U W_A}{\pi n}} \tag{4.10}$$

$$S_D=\sqrt{\frac{2\rho}{2\pi f_s \mu_{r,copper}\mu_{air}}} \tag{4.11}$$

$$P_{cu}=\frac{\rho nMLT(I_{max})^2}{W_A} \tag{4.12}$$

The result of inductor design is presented in table 4.4 but implementation requires few adjustment. With minimum core factor of 0.68, there are not many core options left that are available on the low volume market. Thus, a 3C90 core of ETD49 is chosen. In order to illustrate the size of this inductor, the core has a cross-sectional area of 2.11 cm^2 and window area of 2.71 cm^2. The 3C90 material can handle maximum flux density up to 250mT depending on the temperature it is operating. As Litz wire is used, the winding fill factor is chosen to be 0.3. This results in total air gap length of 0.43 cm. The ETD49 have an air gap on each of the three legs. Thus, around 0.15cm is used for each leg. The first adjustment on the implementation comes from the conductor as there is a limitation over the Litz wire that can be used. The options are limited because custom made Litz wire is expensive. Litz wire with 130 strands and diameter of 0.1007mm each is used. The second adjustment is made for the number of turns as leakage inductance and the precision of air gap influence the implementation. Both inductors used only 10 turns. The non-idealities in execution, as well as additional wire required to connect inductor to the board, made the value of inductance unequal. The realized values are 35.8 μH and 36.4 μH.

4.5. Gate Driver and Measurement Circuit

The full-bridge needs a unit that can support closed-loop feedback Pulse Width Modulation (PWM) control. A bipolar voltage switching with PFCC output voltage measurement to close the loop is sufficient to demonstrate the function of PFCC. Texas Instrument (TI) TMS320F28027F offers an efficient control unit with pulse width modulator and Analog to Digital Converter (ADC) for voltage measurement. PFCC control program along with control-related readings are flashed into this module.

Table 4.4: Single Inductor Parameters

Parameter	Acronym	Value
Single Inductance	L	34 [μH]
Minimum Core Factor	$K_{g(min)}$	0.68
Total Air Gap Length	l_g	0.43 [cm]
Number of Turns	n	15

4.5.1. Gate Driver Stage

In order to develop the control circuit, the full-bridge schematic is depicted in figure 4.1 for ease of explanation. The MOSFETs are controlled through four different gate signals with bipolar voltage switching. S1 and S3 are the high-side gate signal while S2 and S4 are the low-side ones. This gate is connected to PWM signals through half-bridge gate driver as depicted in figure 4.2. The output voltage is used as the feedback to the controller with control schematic as figure 3.6.

The MOSFETs are connected through gate resistor and LM5107 as its driver. The MOSFETs has its internal gate resistor but additional resistance is added to slow down the dv/dt of the switch which gives additional protection against internal latched up at the expense of switching loss. The top MOSFETs gate pin is connected to a bootstrap circuit. The floating high-side driver can handle rail voltage up to 100V. It is important to note that capacitor between HB and HS as well as VDD and VSS is required to ensure reliable operation against high peak currents from LO and HO.

The high-side and low-side PWM signal are coming directly from TI module. The TMS320F28027F has a dedicated pin for PWM. It is programmed based on the control block diagram presented in figure 3.6. On the real application, the voltage reference is expected to be given by system-level control mechanism. In this prototype, however, the voltage reference is flashed in the program without any feedback to change its reference value. Thus, the prototype always gives the same set of output unless the module is reprogrammed. The reference value is compared to a measured value which is already processed and filtered. The error is then amplified through a PI gain which has an internal saturation of -0.3 to 0.3. This limits the duty cycle to a range between 0.2 and 0.8. The switching signal is equipped with dead-band to prevent short circuit.

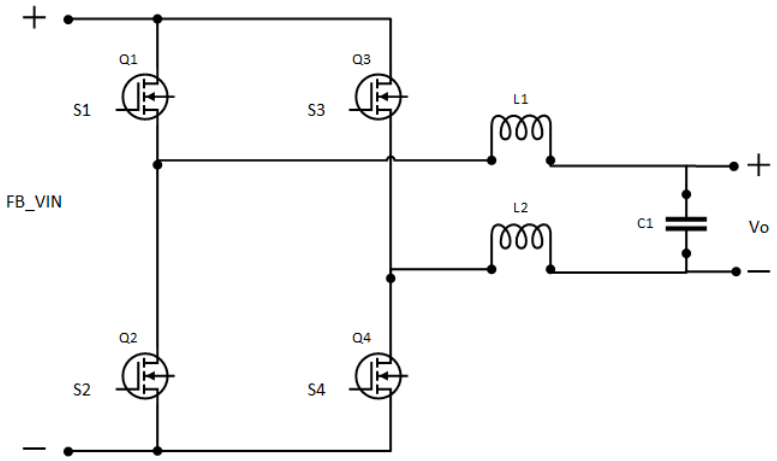

Figure 4.1: *Full-bridge Schematic*

4.5.2. Measurement Stage

A good output voltage measurement circuit is important to ensure reliable control. The measurement stage is divided into two parts, sensor and signal processor. The first part is made out of differential voltage divider and RC filter. The second part is signal processing inside the microcontroller. The first part is placed on the PCB while the second part is flashed into the control unit.

On the first part, The voltage divider ensures that the voltage coming into the microcontroller does not exceed its maximum value. On the other hand, RC filter eliminates high-frequency noises as the DC-DC isolated module is switching on MHz range.

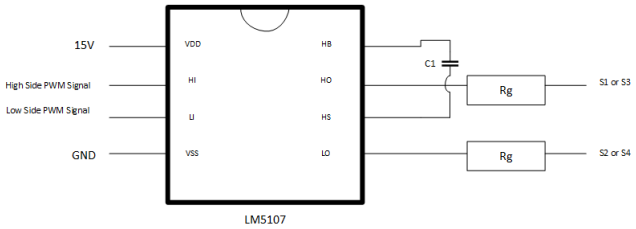

Figure 4.2: *Half bridge gate driver*

On the second part, the signal processing is composed of several blocks. The first block is the ADC. This block is important to manage the sampling rate and point which influence the quality of data measured. The digital signal then flows into delay block which averages out a certain amount of sample and acts as an additional filter. Afterwards, the data type is changed into single and a conversion gain must be made to compensate the voltage divider ratio as well as type conversion changes. Each measurement pole is processed through this block separately. Only after that, the differential is taken to ensure the quality of the measurement.

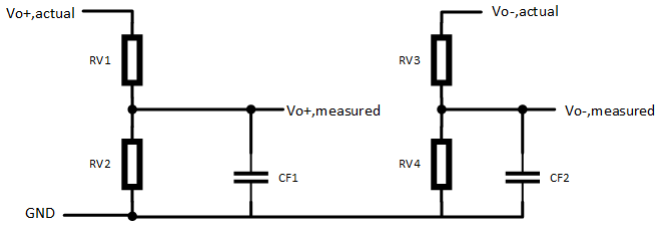

Figure 4.3: *Voltage Measurement Circuit*

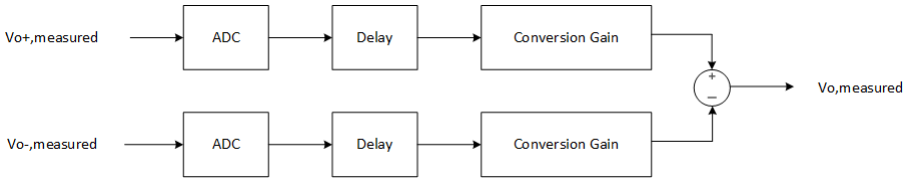

Figure 4.4: *Signal Processing Block for Output Voltage Measurement*

4.6. PCB Design

A proper PCB layout is necessary to gain stable switching waveform with minimum noise. PCB design starts with layer assignment and component placement. After all device's spot has been decided, the routing is done. In order to do this, one must first understand the current conduction paths, signal flows, and the pulsating area.

Figure 4.5 shows the current path on the power plane. The blue dashed line represents continuous current path while the dashed red line is the pulsating one. This switching current path includes the top and bottom MOSFETs and all other components under the red shaded area. This high di/dt path can lead to not only magnetic field radiation but also voltage ringing and spikes due to parasitic inductance (LP). In order to minimize this parasitic component, the distance between the two MOSFETs on each half-bridge must be reduced and must be connected with wide and short traces. Decoupling capacitance (CHF) is also necessary to minimize the influence of di/dt. In this prototype, the input capacitance can act as a decoupling capacitor. As this component is also in the hot loop di/dt area, the distance between the capacitor to each half bridge must also be as close as possible. One can also observe that the gate pin of the MOSFETs are close to the high

dv/dt node. These points are strong sources of EMI noise and rich of high-frequency noise components. Thus, it is important to have a proper layer assignment to minimize these interference.

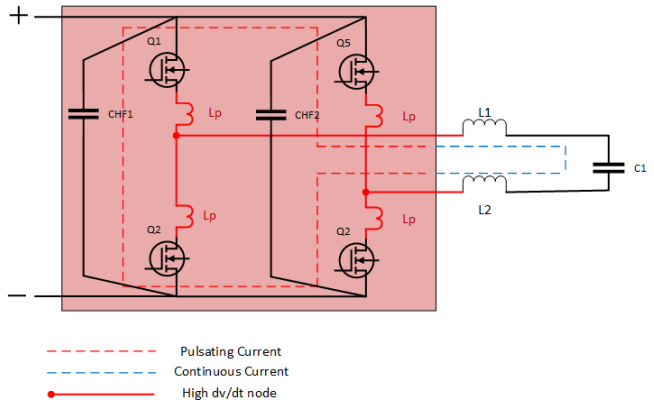

Figure 4.5: *PCB layers assignment*

Figure 4.6 shows the layer structure of the PCB. The top layer is assigned as the power plane where most of the power components and traces are placed onto. The second top layer is called Mid-Layer 1. This is where the ground plane is assigned to. The Mid-Layer 1 is separating the power plane and signal plane to provide additional shielding. On the signal plane, only gate and measurement signals are allowed to pass through. The last layer, Bottom Layer, is assigned as a limited power plane. This is made to add more path for high current traces to reduce line resistance. However, care is taken to place the traces on this layer such that it does not come in the proximity of the signal traces.

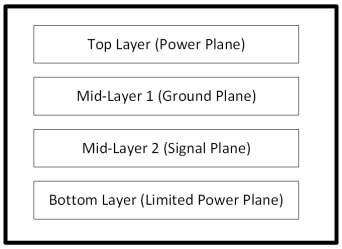

Figure 4.6: *PCB layers assignment*

Power components layout is presented in figure 4.7. As one can see from the layout, the input capacitor, MOSFETs, and its gate driver are placed in a close area to each other. The input capacitor act as decoupling capacitor that filters out high-frequency components from the pulsating current paths. The midpoint of MOSFETs are then connected to the inductor connector through the Bottom Layer. Meanwhile, the small signals are connected through the Mid-Layer 2 to the signal connectors which is linked to the TI module. The empty spaces on the power plane are made to create room for the signal traces such that it is far enough from the power traces on the Bottom Layer.

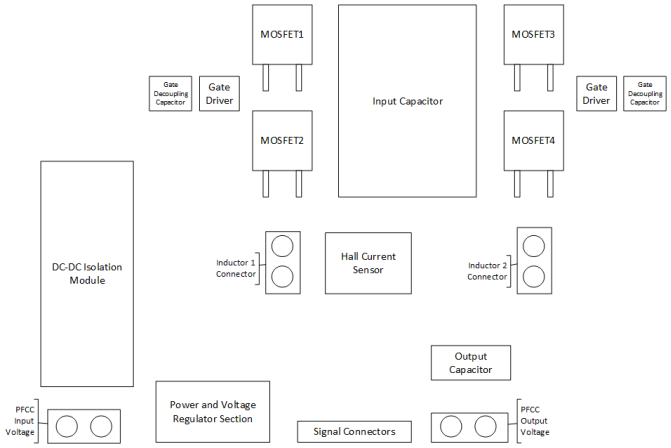

Figure 4.7: *PCB Components on the power plane*

4.7. Summary of Chapter 4

PFCC prototype has been successfully built as shown in figure 4.8 with parameters listed on table 4.5. The maximum power and output current is determined by VICOR module. Its secondary side has a rating of 800W. As 350V is used for the experiment, the secondary side voltage would be 43.75V due to a step-down ratio of the module. The PFCC input side, on the other hand, can handle 2.29A which is more than sufficient for the experiment as the primary side current would be 1/8 of the grid line. A capacitor of 47 μF acts as a filter on the input of full-bridge. It was excessively over-sized in terms of value and configuration as it can handle 100A rms ripple using 100 of 0.47 μF ceramic capacitor commonly used for an automotive application. This was done with a purpose to minimize the module influence to the control dynamic of full-bridge as well as mitigation for unexpected high current due to failures. On the output side, a ceramic capacitor of 30 μF is used. It has successfully limited the output voltage ripple as specification defined. Meanwhile, the inductors were not successfully made symmetric as expected. This is due to inevitable additional extension required for connection to the board as well as improper winding technique. Overall, the prototype has been built successfully and can serve its purpose to validate the function and requirements of PFCC in the experiment.

Table 4.5: Prototype Parameters

Parameter	Realization
Maximum Power [W]	800
Maximum Input Voltage [V]	410
Full-bridge Switching Frequency [kHz]	120
Full-bridge Input Capacitor [μF]	47
Full-bridge Output Capacitor [μF]	30
Full-bridge Output Inductor 1 [μH]	35.8
Full-bridge Output Inductor 2 [μH]	36.4

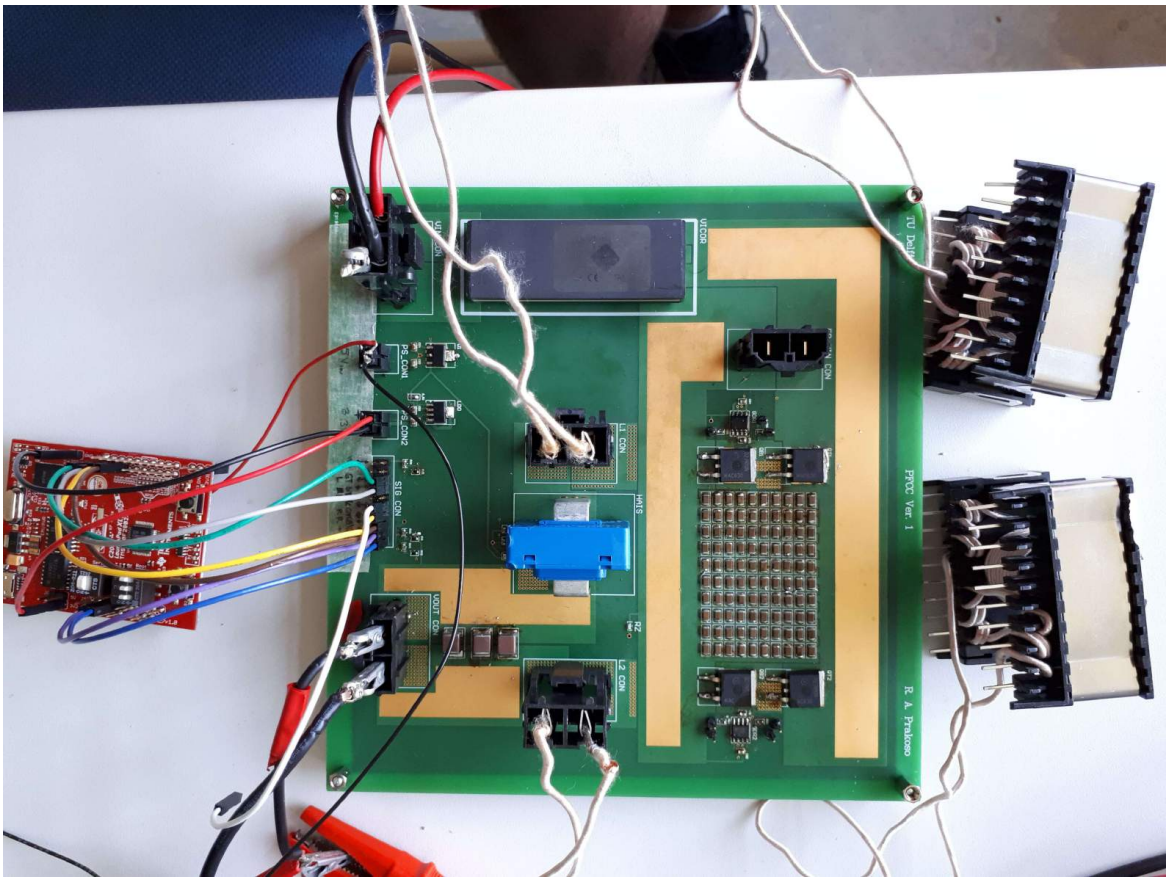

Figure 4.8: *PFCC Prototype with its control unit*

5

PFCC Experimental Result and Analysis

In this chapter, the results of experimental tests are presented. First, it is important to understand the performance of the prototype by testing its efficiency. Second, The main function of PFCC to regulate power was tested. Third, its partial power requirement was validated.

5.1. Efficiency Test

Efficiency test of the prototype is necessary to gain a better analysis on the validity of function and requirement. Low efficiency can mislead experimental data interpretation. In validating partial power requirement, it is necessary that the power processed inside PFCC is significantly lower compared to the grid power due to the effectiveness of PFCC topology and not due to low efficiency. Over a range of power, a variation of efficiency is common for a converter. This should not interfere with validation of power regulation function. In this section, the setup and result for efficiency test are presented.

5.1.1. Efficiency Test Setup

Full power range test is necessary for measuring the prototype efficiency. PFCC is designed to always process a proportion of grid power when it is configured as proposed in chapter three. Thus, the full power of the prototype in proposed configuration can only be tested when there is a grid with 6.4kW of power. As there is not enough DC power supply to make that level of a grid, an experiment setup presented in figure 5.1.

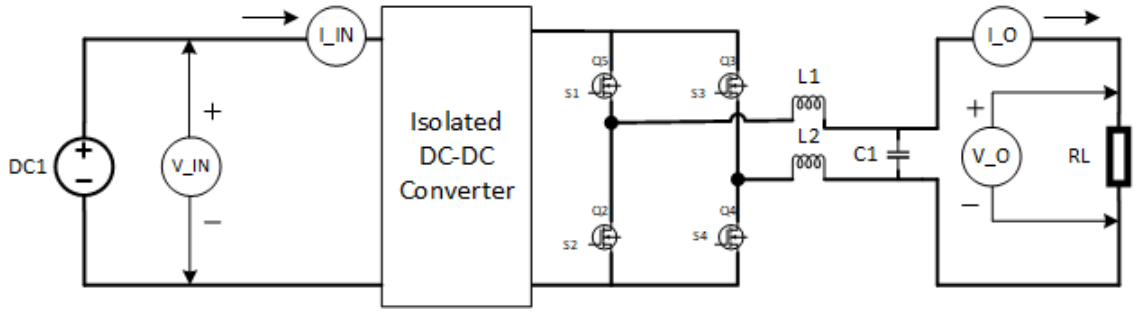

Figure 5.1: *Efficiency Test Setup*

The efficiency of the prototype is tested by supplying DC power on the input side and a constant resistive load on the output. Two DC power supplies are configured to create 3.12kW DC source. It is capable of supplying up to 600V and 5.2A. A constant voltage of 340V, however, is set to emulate the input voltage of DC grid. This means that, ideally, the output voltage can be up to 42.5V. The PFCC power is varied by changing the output voltage. It is increased from 5V to 30V with a step of 5V. The secondary side of PFCC, however, was limited to 20A. Thus, a resistance of 1.5 Ω is set on the output of PFCC. As a result, the maximum power that can be tested is 630W.

5.1.2. Efficiency Test Result

The efficiency test has been done as shown in figure 5.2. The measurement shows that the DC source gives out 338V with 2.3% ripple. This value is constant at the time of experiment although the rms current rose from around 0A to 1.8A. It means that there is no significant voltage drop between the DC source and PFCC. The output voltage was successfully incremented from 5V to 30V. For each reference value of output voltage, the error is ± 0.5V. The transient response does not show any overshoot and achieves steady state value in less than 2s. The speed of control is not a high priority in this experiment. Thus, the control response shows a satisfactory performance. The ripple is also managed to be kept below ± 1V across output voltage range. The output current closely follows its voltage according to its relation to the resistance which value was measured as 1.48 Ω. It shows a ± 1.1A ripple across the whole range of current. This is acceptable considering the current went up to 20A. The input current, on the other hand, suffers a significant ripple of more than 50%. These must be taken into account in efficiency calculation.

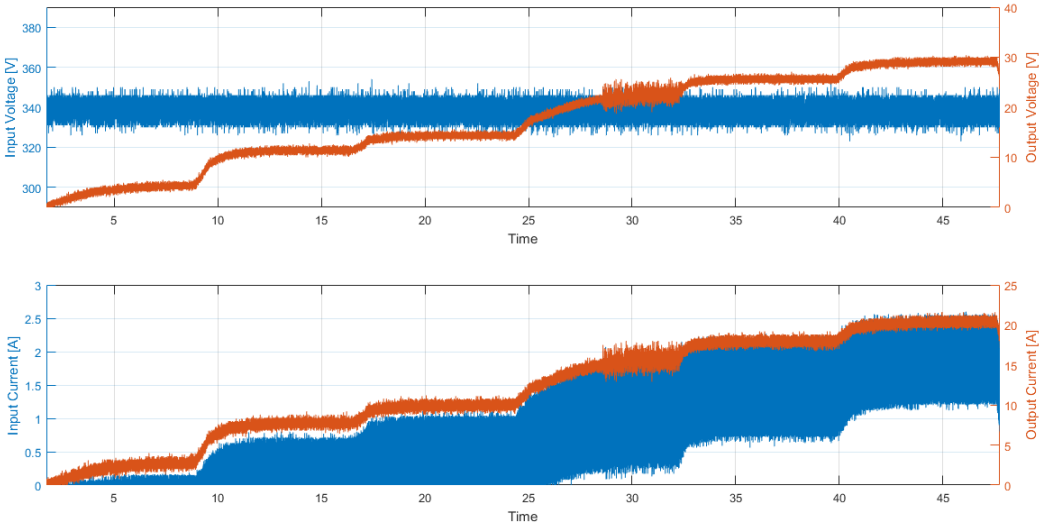

Figure 5.2: *Efficiency Test Input and Output Voltage and Current*

The efficiency curve is shown on figure 5.3. It shows the measured power range from 37W to 625W. The efficiency shown is a combination of both VICOR module and Full-bridge efficiency. The values are calculated by sampling two intervals for each output voltage. This is done to filter out the influence of current ripple to efficiency calculation. The two samples for each voltage reference shows a similar value. Datasheet of VICOR shows a similar curve in which the efficiency decreased dramatically with a load below 100W. Under 85.5W, the module shows an efficiency of 90%. The combined result also shows value below 70% under 100W. The low efficiency at light load and the curve show that the loss is dominated by conduction loss. Omitting values at light load, the average efficiency of the prototype is 86%. According to the curve, combined power loss is between 15W to 30W for loads above 100W. This is an acceptable value for function and requirement validation.

5.2. Power Regulation Test

Power regulation is the main function of PFCC that needs to be validated. The prototype must be able to change the power flowing on the grid by inserting a series voltage. In order to observe this change, at least two DC sources must be connected through two lines. The configuration of power regulation validation setup, as well as the result, are presented.

5.2.1. Power Regulation Test Setup

An experimental setup that represents proposed configuration is required to validate power regulation function. The setup is shown in figure 5.4. It represents the case presented in chapter three where one out of three nodes in DC grid suffered a failure and the rest of grid nodes are basically connected through two separated

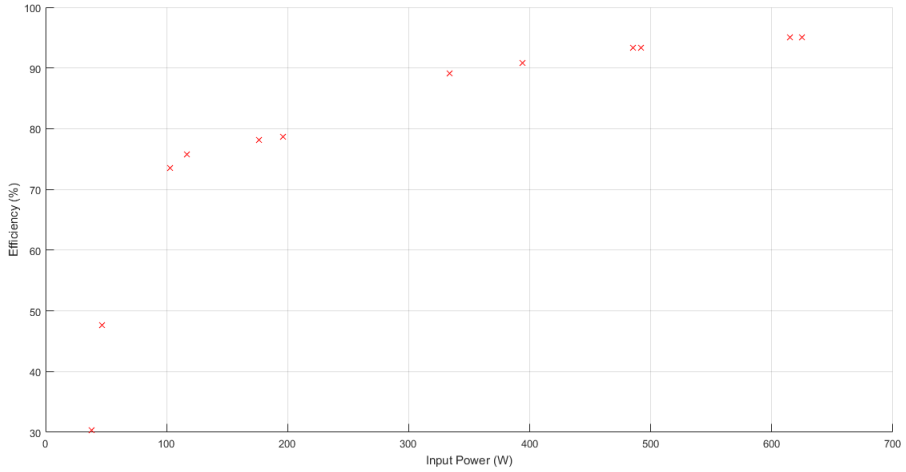

Figure 5.3: *Efficiency Test Result*

lines. This experiment is not intended to repeat the current limiter scenario on chapter three. It shows how the line power can be regulated between the two lines.

A 1.82kW grid with parameter shown on table 5.1 is set to verify PFCC main function. Ideally, DC nodes act as an active load in which it can transfer and consume power. The available DC power supplies, however, cannot behave as a sinking source. Thus, a parallel resistor is connected across it to absorbs the transferred power. DC power supplies used are N5772A Agilent Technologies with 1.56kW nominal power, 600V and 2.6A. The grid voltage is defined to be 350V. Two significantly different line are modeled using a parallel resistor. Under an unregulated condition, most power would flow through line 2 as its resistance is one tenth of line 1. With the presence of PFCC, however, the majority of power can be regulated to flow through line 1 where the converter is connected. The series voltage inserted to the line as PFCC output is varied from positive to negative 5V.

Table 5.1: Test Setup Parameters

Parameter	Acronym	Value
DC Source 1	DC1	350 [V]
DC Source 2	DC2	350 [V]
Load Resistance 1	R1	220 [Ω]
Load Resistance 2	R2	110 [Ω]
Line Resistance 1	RL1	2.2 [Ω]
Line Resistance 2	RL2	0.22 [Ω]

Seven measurements are set in the configuration. There are four readings for currents and three for the voltages. The currents are measured with clamp probe while the potential differences used a probe from an oscilloscope. As the value of the power supply is set constant, voltage readings are configured on the two parallel resistors (VR1 and VR2) to monitor whether there is a voltage drop inside the sources. Another voltage reading is placed on the output of PFCC to observe the inserted series voltage. Besides the two line current measurements (IL1 and IL2), the input current (I_{IN}) to PFCC is also monitored. This current is expected to be one-eighth of the current on line 1. The current flowing through R_1 is also measured to sense the direction of power flow.

5.2.2. Power Regulation Test Result

The control of PFCC is programmed to give out a square wave voltage between $\pm 5V$. The measurement results are depicted in figure 5.5 and 5.6. On figure 5.5, the two voltage across the resistance parallel to the source are shown. Figure 5.6 shows the functional validation of power regulation. The PFCC output voltage waveform governs the transient of other parameters such as line current and power. Using the two figures 5.5

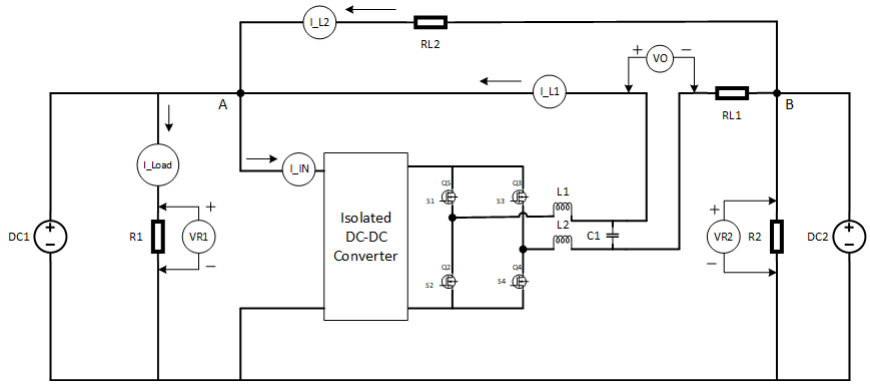

Figure 5.4: *Test setup with 1.82kW of non-sinking sources for each side*

and 5.6 the power regulation function is validated.

Figure 5.5 shows the two load voltages. The two load resistors, R1 and R2, are connected in parallel to the voltage sources which are set as 350.5V and 350V, respectively. The noise from the measurement is filtered out using Matlab function to give out the DC value. The measured voltage, however, is not the same with the set voltage on the source. This difference is due to internal resistance of the power source, voltage drop across the line, and forward voltage of protection diode in front of the source. From those value, it can be concluded that there is a 5.1V difference of potential from node A to B. The original measurement shows that the load voltage has a 24V peak to peak ripple which is 6% of the RMS voltage. The output voltage of PFCC, however, is a fifth of this peak to peak value.

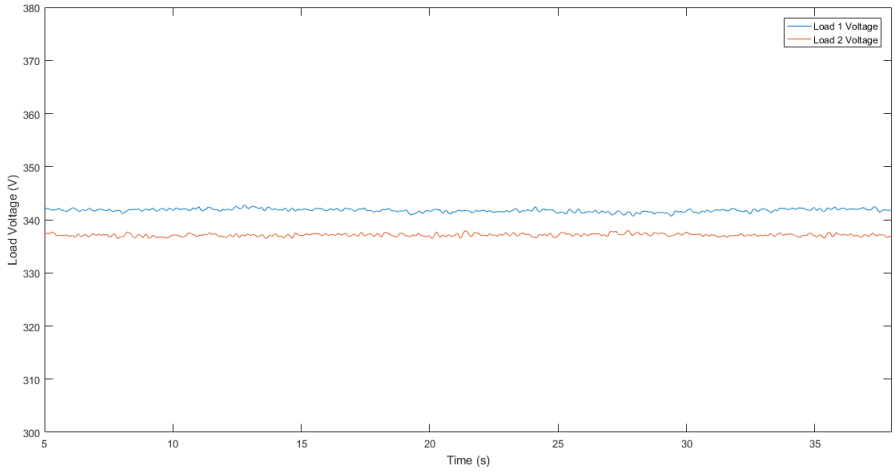

Figure 5.5: *Load voltage parallel to the DC sources.*

PFCC output voltage and its influence on the line and load current can be observed from figure 5.6. The first thing that should be analyzed is the PFCC output voltage. It is presented on the top figure of 5.6. It can seen that there is a disrepancy between the voltage reference and the actual value in both polarity. On the negative voltage output, there is $-0.5V$ error while on the positive one the value exceeds the reference by $1V$. This might be cause by the voltage measurement on the control board which does not measure it accurately. Despite of that, the series voltage is able to regulate the power flow. The current in line 1 changes to -2A when the PFCC outputs a negative voltage. When this voltage changed to a positive value, the line current also increase to 2A. The load voltage parallel to DC source shown in figure 5.5, however, shows that voltage of DC1 is always higher than the value of DC2. It means that the current flowing through the line 1 is governed mainly by the PFCC output. This would not be the case in the real distribution grid. It is expected that the DC sources are the one who dictate the power flow direction. However, there is no DC source available in

the laboratory that can act as a sink. Thus, this shows the limitation of this experiment. Despite of that, it is demonstrated that the PFCC can regulate the power flowing through the line.

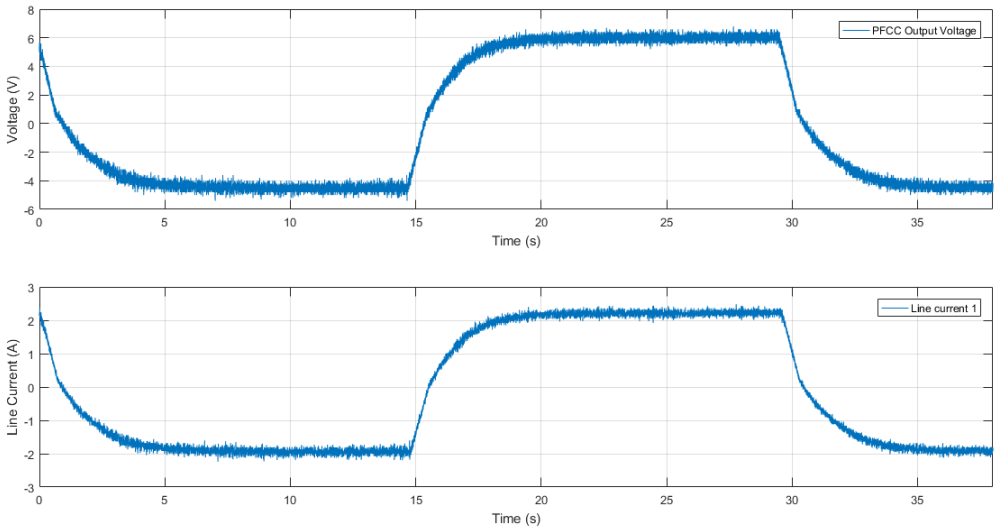

Figure 5.6: *Power regulation action by PFCC. The change in current direction and the load voltage in figure 5.5 shows that the PFCC dictate the power flow direction.*

5.3. Partial Power Validation

Partial power is an important requirement of PFCC that needs to be validated. It guarantees high efficiency on the grid level and low production cost. This is achieved by the step-down ratio of the isolation segment. Thus, ideally, the power of the prototype should have a fraction of the grid power. The measurement of partial power validation was taken from the same experiment for power regulation. The same measurements on figure 5.5 and 5.6 are valid for this section. Figure 5.7 shows the comparison between grid and PFCC power.

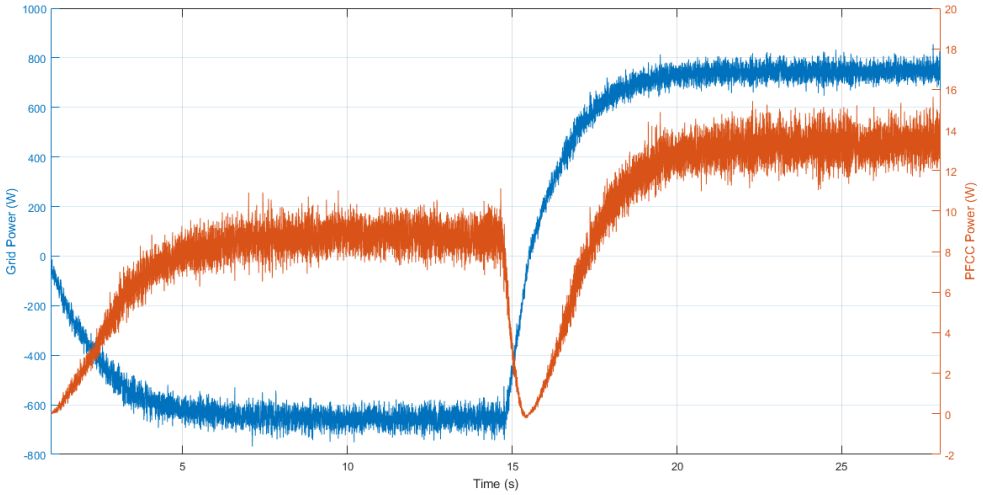

Figure 5.7: *Comparison of the grid power measured at load R2 and PFCC power at its full-bridge output. It shows that PFCC only process approximately 2% of the transferred power.*

A quick glance over figure 5.7 can conclude that PFCC only process power significantly lower than DC

network. The grid power was measured on the line 1 where the PFCC is installed. It is calculated based on voltage of load 1 and the current flowing through line 1 when it is in positive direction. The blue line on the figure shows that this node is transferring power in the direction of DC1. The PFCC power, on the other hand, is calculated based on the PFCC output voltage. The line current 1 which passed through the output side is multiplied by the voltage inserted to the grid. This is done due to a very low current on the input side. The grid power measured at load resistance R2 shows that the it is receiving power in the left half of the figure and transmitting power on the other half of the figure. The output of the converter, on the other hand, always receiving power from the input side. If one thinks that the power processed by PFCC is defined by the ratio of isolation segment, the grid power on the right half of 742W must have 93.13W on PFCC which is 1/8. Meanwhile, the figure shows only 14W. Thus, the appropriate logic is that the power ratio processed in the converter compared to the transferred power is defined by the ratio between the output voltage and the grid voltage. This, of course, does not reflect the rating that the PFCC should have. The rating of the converter depends on the grid voltage and the maximum output voltage of the full-bridge.

5.4. Summary of Chapter 5

This chapter has validated PFCC function to regulate power and its requirement of partial power rating. Firstly, an efficiency test was made to make sure further analysis would not mislead the conclusion of the experiment. An average of efficiency of 86% was measured for power above 100W. It means that the prototype only loss 15W to 30W for load between 100W to 630W. This is an acceptable efficiency performance for function and requirement validation. Secondly, the power regulation function was tested using a 1.82kW grid. The PFCC was controlled to gives out output voltage from positive to negative 5V. It is successfully regulate power in the case study by changing the direction of the line current. It happened because of the DC source limitation which cannot serve as a sinking source. In the real application the direction of power is expected to be governed by the DC nodes. This, however, does not negate the conclusion that the PFCC can regulate the power flow. Finally, partial power characteristic of PFCC was validated using the measurement from the same experiment for power regulation. The result shows that at the output of the PFCC, it processes 2% of the power transferred through the line it is installed. This shows that the power processed inside the converter is significantly less than the power transferred through the line.

6

Conclusion

The thesis has analyzed one novel alternative of partially rated power flow control converter. The device is expected to increase the controllability of meshed LVDC distribution grid by providing the ability for the system to regulate power flowing in the network.

In chapter two, a literature review over LVDC distribution grid, existing alternatives for DC power flow control devices, and PFCC function & requirements are presented. LVDC is considered to be more compatible to grid with significant DC sources, loads, and storage due to its better efficiency compared to LVAC. Mesh topology can improve its advantage further in terms of reliability and efficiency. There is, however, a challenge in terms of its optimal operation. DC power flow control device can help tackle this issue. Among its types, series voltage source is the best option in terms of power regulation with low losses. However, existing alternatives require this type of device to have additional connection to other line. This could be impractical in complex distribution network. Thus, it is decided that PFCC must be able to regulate power in all four V-I quadrants with a power fraction to the grid and requires no additional connection to other line.

In chapter three, the proposed PFCC topology is discussed and simulated. The converter consists of two cascaded circuit. The first stage is the isolation segment. This part prevent short circuit between the input and output port as well as providing a step down ratio essential to the partial power requirement. The second stage is the output regulator segment. This part controls the series voltage inserted to the line to control the power flow. Dual Active Bridge or LLC can serves as the first stage. Meanwhile, synchronous full-bridge and non-synchronous full-bridge can be used for the second stage. Which of these alternatives is the best one is not the scope of this thesis. A Dual Active Bridge and Synchronous full-bridge is modeled to simulate the PFCC operation. The simulation shows that PFCC can regulate power in all four V-I quadrants with partial power.

In chapter four, the design of PFCC prototype is discussed. An 800W hardware proof of concept was developed. The prototype uses an LLC resonant converter module as it is already available in the market with less cost and smaller dimension compared to DAB. The full-bridge is implemented using SMDs MOSFET, ceramic capacitors, and two in-house made inductors. The designed circuit is assembled on a PCB connected to a control unit in a separated board. It is shown that the proposed topology can be controlled with a simple PI control block.

In chapter five, the developed prototype was tested to validate the PFCC function. Firstly, the efficiency of the constructed hardware was measured. Its average value is 86% but it goes above 90% for load more than 400W. Secondly, the power regulation function was tested in a 1.82kW setup. It successfully regulate power by inserting positive and negative series voltage. Thirdly, the PFCC also shown that it only process a partial power with respect to the grid.

In this thesis, the proposed topology has been simulated and tested. At this early stage, the concept is proven to be working. The general conclusion of this thesis are:

1. A set of function and requirement of an LVDC distribution grid has been determined qualitatively. The PFCC must be able to regulate power flow in both power directions. Three requirements of the device are partially rated, works in the four V-I quadrants, and requires no connection to other cable.

2. The proposed topology has been simulated in a unipolar grid. The simulation shows that PFCC is capable of regulating power flow in the four V-I quadrants and partial grid power.

3. A prototype of PFCC is developed and tested in a laboratory scale two source network. Despite the under-rated setup, the prototype successfully perform the power flow regulation in a hardware experiment.

4. The prototype shows that the proposed topology can be controlled with a simple PI control.

The thesis has successfully contribute to the development of DC power flow control device for LVDC distribution grid by analyzing and validating a novel partially rated topology to perform bidirectional power flow regulation.

Despite of the progress, there are future works that needs to be done before PFCC is ready to be used. The proposed converter has the potential to work on a bipolar network with high grid efficiency. It is important to develop and validate the performance of the converter to its maximum potential. First, a prototype dedicated to prove its high efficiency and reliability on a larger power scale of experiment setup is necessary to prove that the marketability of the device in the current available semiconductor and heat-management technology. Second, the topology can be made to be modular. The option of its modularity and how it affects the performance of the converter is an interesting room of development. Finally, several number of PFCC can be implemented in a mesh network. In a low inertia environment such as LVDC distribution grid, it is interesting to analyze how it can work together in one system in terms of the time response to events in the network.

A

Printed Circuit Board

The Printed Circuit Board (PCB) was designed using Altium Designer software. The schematic and layout are attached in this appendix.

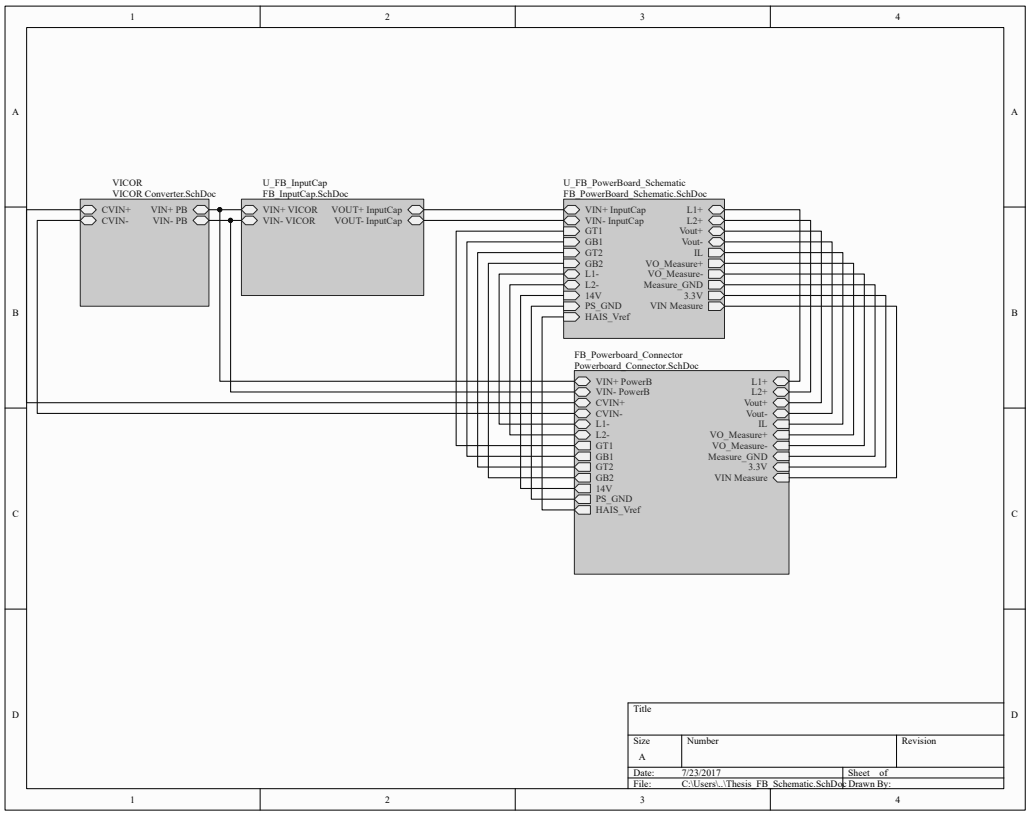

Figure A.1: *PCB Top Level Schematic*

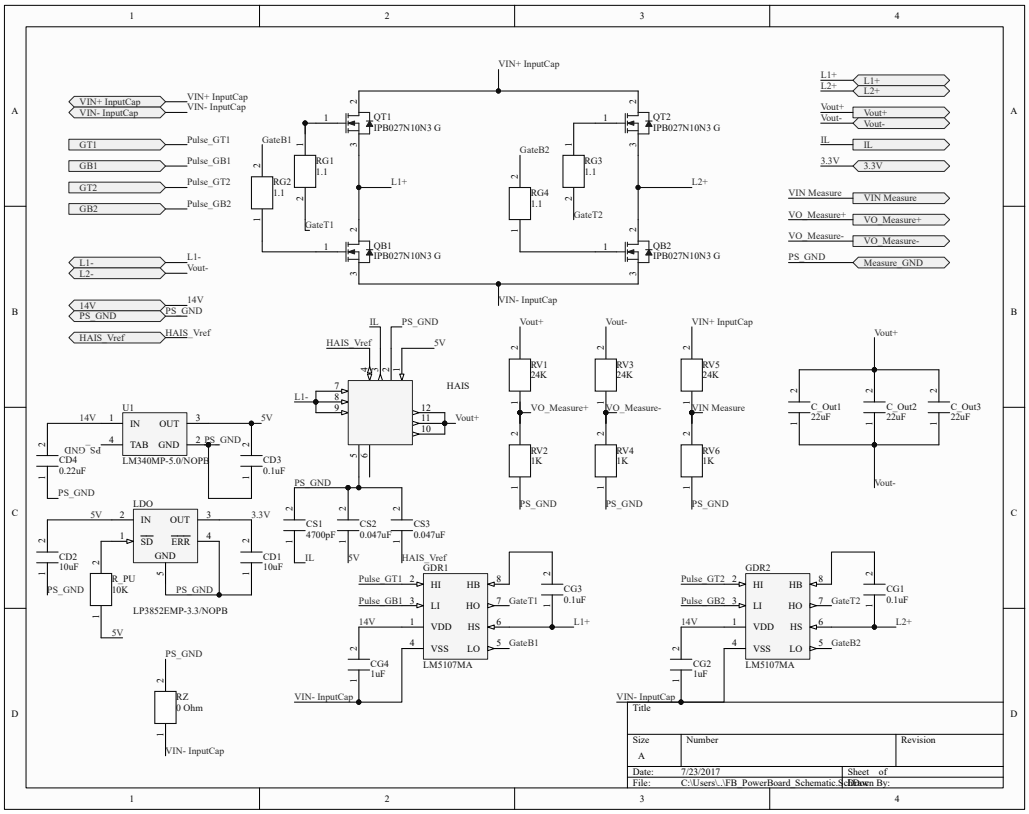

Figure A.2: *PCB Full Bridge Schematic*

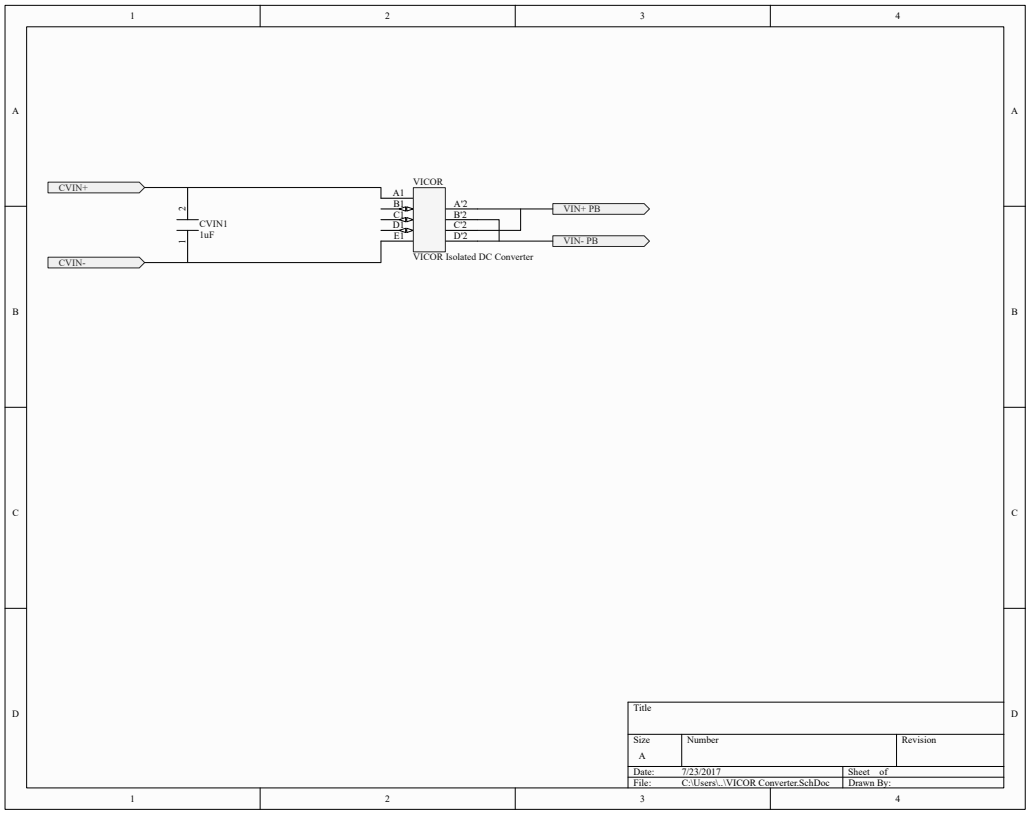

Figure A.3: *PCB Vicor Module Schematic*

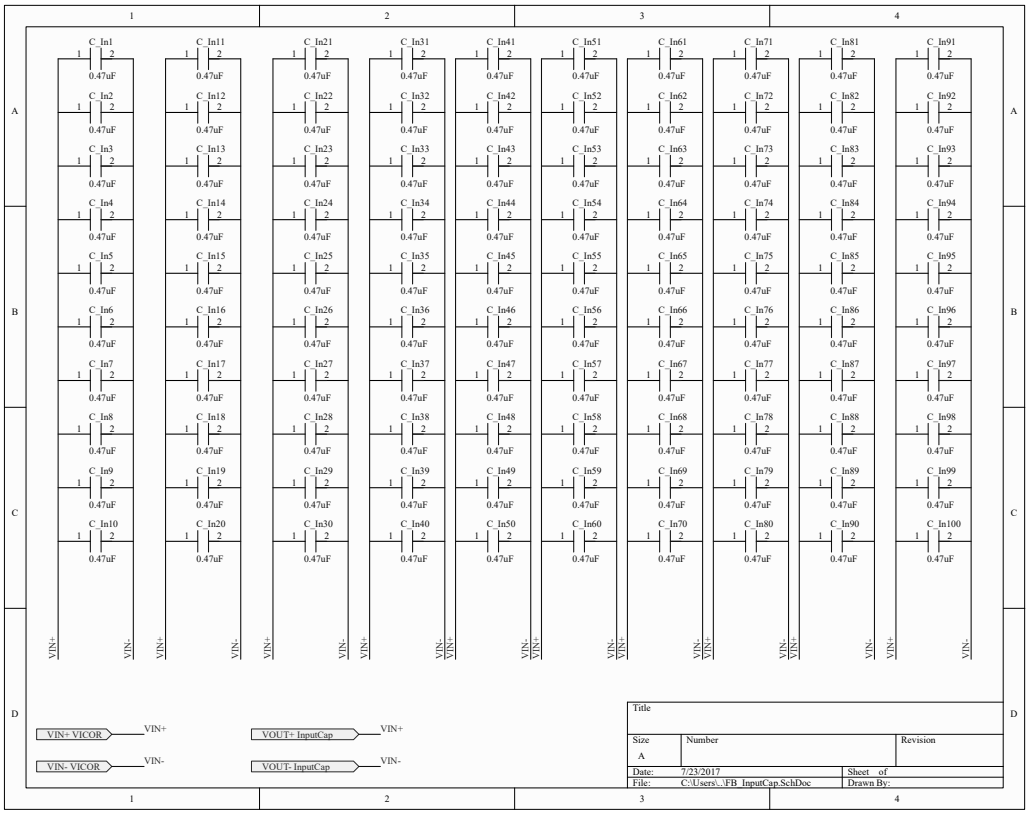

Figure A.4: *PCB Input Capacitor Schematic*

B

Published Work

A paper based partially on this thesis has been published in IEEE Second International Conference on DC Microgrids 2017.

P. Purgat, L. Mackay, R. Adilardi Prakoso, L. Ramirez-Elizondo and P. Bauer, "Power flow control converter for meshed LVDC distribution grids," 2017 IEEE Second International Conference on DC Microgrids (ICDCM), Nuremburg, Germany, 2017, pp. 476-483. doi: 10.1109/ICDCM.2017.8001089. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8001089&isnumber=8001013

An abstract for a paper based on this thesis has also been submitted to IEEE Applied Power Electronics Conference and Exposition 2018.

Power Flow Control Converter for Meshed LVDC Distribution Grids

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***Abstract*—Inside the meshed LVDC distribution grids the power flow is predominantly limited by the line impedances. In order to achieve economical and flexible operation of the meshed LVDC distribution grids, it is required to control the power flow. For that end, the line impedances need to be adjustable. The line impedance can be controlled by a DC-DC transformer, however, it needs to be rated for the full grid power. In order to reduce the installation costs, a partially rated device is desirable. Therefore, a partially rated power flow control converter (PFCC) is proposed. This paper presents the PFCC performance estimate and demonstrates the PFCC functionality.**

The PFCC is an economical solution for increasing the controllability of the power flow in the meshed LVDC distribution grids. However, due to high step down ratio inside the PFCC achieving efficient performance is challenging. Furthermore, due to unavoidable MOSFET paralleling the part count rises. The proposed PFCC consists of two cascaded converters, therefore the control range and stability depends, besides else, on the impedance interaction between the two stages.

I. Introduction

In the European Union and the United States, there is a growing discrepancy between the rise of the overall electricity consumption and the cost of that electricity, where the former has been stalled for almost 30 years, while the later has been steadily increasing. This can be partially explained by the shift in the energy policies of the aforementioned countries and by the aging of the energy distribution networks. Therefore, new solutions for the electric energy distribution network which allow multi-directional power flow are being explored such as DC networks [1]. In order to increase the grid utilization, meshed infrastructure was proposed [2]. However, the meshed DC networks are associated with the challenges in the protection and the control of the power flow in the network.

In the HVDC transmission, the advantages of the more complex grid structures were discussed for several years [3]. In the HVDC among the primary motivations for the introduction of the multi-terminal structures are increased availability of the grid, and the reduced construction and operation costs [4]. However, compared to the more traditional radial networks the protection of the meshed grids is more challenging [5]. Furthermore, in the meshed DC network, it is not readily possible to control power flow in all lines/cables which may result in significant overloads [6], [4]. The same challenges were described in the low voltage distribution for the secondary customers [7], [2].

Both for the LVDC and HVDC meshed grids the power flow can be manipulated by changing line' voltage, current or impedance. In the literature, three different methods are described to control power flow in the meshed grid. The first option is a variable resistor described both for the HVDC [6], [8] and LVDC [2]. The main disadvantage of this solution is that the excess power is turned to losses thus the solution though simple, it is inefficient. The second solution is based on the fully rated DC-DC converter such as [9] or [10]. The fully rated DC-DC converter is able to control the power flow, step-up the voltage level, integrate the protection and isolate different parts of the network. However, for the LVDC the fully rated DC-DC converters can prove to be expensive. Therefore in [7] and in [2], partially rated devices were proposed. The partially rated DC-DC converters can limit the current, or step-up the voltage. However, they cannot in itself provide the protection for the network. A combination of the fully rated network protection and partially rated power flow control devices might be an attractive solution from the economic standpoint.

The main trends in the literature concerning the power flow control in the meshed DC grids are to focus on the HVDC transmission and the investigation of the power flow controllers from the system perspective. However, the challenges imposed on the power electronics by this application were not studied before. The performance estimate of the converters is important for the evaluation of the solution' economic viability. Therefore, in this paper, the authors introduce a new solution for the power flow control for a meshed LVDC grid and assess the performance limitations of the proposed solution. This approach enables to incorporate the system constraints into the device design while providing a device performance estimate for the network design. The control of the power flow control converter (PFCC) is discussed due to the inherent limitation of the cascaded converter operation.

The rest of the paper is organized as follows, in the Section II the principle of the line voltage control in the meshed grids is explained. The Section III describes the design of the proposed power flow control converter and gives and an estimate of the losses in the converters. Section IV explains the control of the proposed converter, the Section V shows the operation of the proposed power flow control converter in two case studies. The last section is dedicated to the summary of the paper and the outlook on the future work.

II. Current Limiting and Voltage Stepping in Meshed DC Grids

In the Fig. 1 is a basic meshed LVDC grid on which the principle of the power flow control and the voltage stepping can be explained. For the sake of simplicity, it is assumed that the nodes are connected by the cables of equal lengths and

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equal electrical characteristics. The grid is assumed to be in the steady state and the line resistance is R. Node N_3 is connected to the MVAC grid, while nodes N_1 and N_2 are connected to the local DC microgrids. Due to a fault on the MVAC grid, the node N_3 is turned off. In such a case the equations of the line currents I_{L_i} in the grid are:

$$I_{L_2} = I_{L_3} = \frac{V_{1,2}}{2R} = \frac{V_1 - V_2}{2R} \tag{1}$$

and

$$I_{L_1} = \frac{V_{1,2}}{R} \tag{2}$$

where V_i is the voltage at the node N_i. In case that a significant amount of power from node 1 to node 2 needs to be transferred, the voltage difference $V_{1,2}$ between the two nodes will be increasing to a point where the current in the line 1 will reach the maximum rated value. In this special case, the current in the lines 2 and 3 will be only 50% of its maximum rated value.

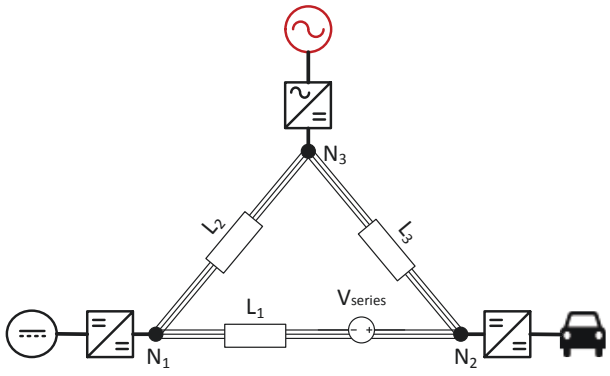

Fig. 1. Basic meshed bipolar LVDC grid, based on the lines with equal length and equal electrical characteristics. In the line between node 1 and 2 a voltage drop V_{series} is introduced to increase the power flow in the network. It should be noted that the series voltage is introduced in both poles of the bipolar network if necessary.

To improve the utilization of the meshed grid, the current in line 1 needs to be limited. This can be achieved by a voltage drop in one of the lines. If the voltage drop is introduced in line 1, then the currents will be

$$\begin{aligned} I_{L_2} &= I_{L_3} = \frac{V_{1,2}}{2R} \\ I_{L_1} &= \frac{V_{1,2} - V_{series}}{R} \end{aligned} \tag{3}$$

After the introduction of the V_{series} all lines start carrying the same current, and the power transfer in this particular case is increased by 33%. In this way, the PFCC can substitute the DC-DC transformer for the same voltage connections and improve the utilization of the meshed LVDC grid.

III. Power Flow Control Converter

The partially rated DC-DC converter for the power flow control can be constructed from modules in parallel to reduce the conduction losses in the semiconductors due to high currents flowing in the meshed DC grid. Furthermore, the modules can be interleaved to reduce the size of the capacitor which reduces the installation costs. The proposed topology of the power flow control converter is shown in the Fig. 2 which also illustrates the parallelization of the modules to meet different power ratings.

A. Topology

The module topology is shown in Fig. 2, the DC-DC converter consists of two stages. The first stage is dual active bridge (DAB) converter and the second is a full bridge converter which is operated in all four quadrants. The DAB is connected to the full grid voltage on one side but only to e.g. 10% of the rated current and on the low voltage side is connected through the decoupling capacitor to a full bridge. The full bridge has to sustain the rated grid current, however only a fraction of the grid voltage. The full bridge converter controls the current and expands the operational range of the power flow control converter into all four quadrants.

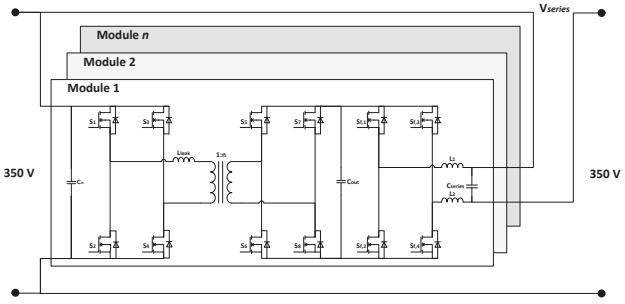

Fig. 2. The proposed power flow control converter is a cascaded Dual Active Bridge with a Full Bridge converter. The DAB provides galvanic isolation between the HV and LV side and a step down of the voltage, while the full bridge converter limits the current and inverses the V_{series} if necessary.

The main characteristics of the proposed power flow control converter are:

- Partial rating of the components with respect to the grid rating.
- The DAB provides galvanic isolation between the HV and the LV side and provides an arbitrary step-down ratio.
- The full bridge converter expands the control range of the power flow converter into all four quadrants.
- Soft-switching is achieved on the HV side of the DAB.

B. Design of the Power Flow Control Converter

For the design of the power flow control converter we assume that the nominal voltage of the meshed LVDC grid is 350 V and that the grid can operate between 300 V to 400 V. The current of the grid depends on the size of the cable and in general can be up to several hundred amperes. Therefore, we opt to design a module of a standard size and argue that to meet the system requirements the modules can be connected in input-parallel-output-parallel. The module specifications are given in Table I.

TABLE I. THE DESIGN PARAMETERS OF THE POWER FLOW CONTROL CONVERTER

Parameter	Acronym	Value
Rated module power	P_{max}	2 [kW]
Nominal grid voltage	V_{nom}	350 [V]
Grid voltage range	V_{grid}	300 to 400 [V]
Grid voltage ripple	$V_{nom,ripple}$	$0.05V_{grid}$ [V]
Series voltage range	V_{series}	-20 to 20 [V]
Series voltage ripple	ΔV_{series}	$0.002V_{series}$ [V]
Switching frequency	f_{sw}	100 [kHz]

1) Dual Active Bridge: The phase shifted dual active bridge can be designed to enhance the zero voltage switching region or to minimize the rms of the current [11]. The design of the dual active bridge is governed by the relationship between the maximum power P_{max} that can be transferred with the given leakage inductance L_{leak}:

$$P_{max} = \frac{nV_1V_2}{8f_{\text{sw}}L_{\text{leak}}} \tag{4}$$

where V_1 is the voltage on HV side, V_2 is the voltage on the low voltage side and n is the transfer ratio of the high-frequency transformer. The DAB parameters can be calculated as in [12], and are in the Table II.

TABLE II. THE DESIGN PARAMETERS OF THE DAB

Parameter	Acronym	Value
Maximum Power	P_{max}	2 [kW]
Nominal HV Voltage	$V_{1,\text{nom}}$	350 [V]
Nominal LV Voltage	$V_{2,\text{nom}}$	35 [V]
Leakage Inductance	L_{leak}	52.5 [μH]
Transformer ratio	n	1:8 [-]
Max. RMS Transformer Current	$I_{t,\text{RMS}}$	11.28 [A]
Max. RMS HV Side Switch Current	$I_{\text{HV}_{\text{RMS,sw}}}$	7.98 [A]
Max. RMS LV Side Switch Current	$I_{\text{LV}_{\text{RMS,sw}}}$	63.82 [A]
HV Side Decoupling Capacitor	C_{HV}	50 [μF]
LV Side Decoupling Capacitor	C_{LV}	300 [μF]

The losses in the DAB have three main sources: the active components, the passive components, and the auxiliary circuit. The auxiliary circuit losses are caused by the communication and the control circuitry. However these losses are negligible compared to the losses in the active and passive components for the non-optimized solution. The losses in the passive components are mainly dependent on the rms value of the current and its peak-to-peak value. For comparable optimized power electronic converters, these losses are usually less than one-fifth of the total losses [13], [14]. Because the main contributor to the losses are the semiconductor devices, only the losses in the MOSFETs will be evaluated in detail.

For the efficient operation of the DAB, the HV side MOSFETs need to operate within the zero voltage switching range. The zero voltage switching range of the phase-shift DAB can be estimated for the leading full bridge from (5) and for the lagging full bridge from (6) as was shown in [11].

$$\varphi > \frac{V_1}{2nV_2}\left(\left(\frac{nV_2}{V_1}-1\right)+8f_{\text{sw}}\sqrt{L_{\text{leak}}C_{\text{oss,eff}}}\right) \tag{5}$$

$$\varphi > \frac{1}{2}\left(\left(1-\frac{nV_2}{V_1}\right)+8f_{\text{sw}}\frac{n^2V_2}{V_1}\sqrt{L_{\text{leak}}C_{\text{oss,eff}}}\right) \tag{6}$$

φ is the phase shift and limited to $0 < \varphi < \frac{1}{2}$. $C_{\text{oss,eff}}$ is an estimate of the non-linear parasitic output capacitance(which is evaluated as the charge equivalent and not the energy-equivalent [15]) of the MOSFET.

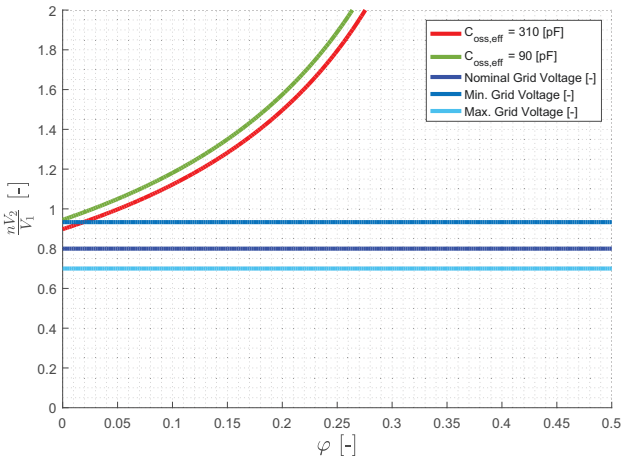

Fig. 3. The ZVS region of the DAB HV side H-bridge. The blue lines represent the input and output voltage ratios with the transformer ratio $n = 8$. The influence of the parasitic capacitance $C_{\text{oss,eff}}$ on the ZVS range is illustrated as well.

In the Fig. 3, the ZVS range of the leading full bridge of the DAB is depicted along with the voltage ratios for both the minimum and the maximum input voltage. It can be seen that for the leading full bridge the ZVS can be achieved almost for the whole switching range. The switches compared are STB23NM60ND($C_{\text{oss,eff}} = 310$[pF],$R_{\text{DS,on}} = 0.18[\Omega]$) and FCPF400N60($C_{\text{oss,eff}} = 90$[pF],$R_{\text{DS,on}} = 0.4[\Omega]$). The trade-off in choosing is between limiting the conduction losses due to drain-source on resistance of the MOSFET $R_{\text{DS,on}}$ and the switching losses which would be incurred when ZVS is lost. The conduction losses for the full bridge can be evaluated as [14]:

$$P_{\text{cond}} = 4R_{\text{DS,on}}I^2_{\text{HV}_{\text{RMS,sw}}} \tag{7}$$

Considering the fact that the conduction losses would be 2.2 times higher with the later switch, it seems reasonable to choose the former. However, consideration should be made whether the power flow control converter will not operate most of the time in a region with small grid voltage and almost no power transferred. If that would be the case, the hard switching must be avoided and the value of the parasitic capacitance becomes decisive.

The ZVS range of the lagging full bridge can be evaluated from (6), it can be shown that the ZVS is practically unachievable on the lagging full bridge with the phase shift control due to relatively high transformer ratio and relatively high $C_{\text{oss,eff}}$ of the low voltage, high current MOSFETs. Furthermore, due to the high currents the parasitic inductances of the drain L_D and source L_S influence the switch off losses [16]. The switch off loss due to the parasitic inductances can be calculated as $P_{\text{off}} = 4f_{\text{sw}}E_{\text{LV}_{\text{sw,off}}}$, where $E_{\text{LV}_{\text{sw,off}}}$ is calculated as:

$$E_{\text{LV}_{\text{sw,off}}} = \frac{1}{2}\left(L_D+L_S\right)I^2_{\text{LV}_{\text{RMS,sw}}}\frac{V_{(\text{br}),\text{ds}}}{V_{(\text{br}),\text{ds}}-V_2} \tag{8}$$

where the $V_{(br),ds}$ is the break down voltage of the MOSFET [16]. The turn-on loss of the MOSFET can be calculated

as:

$$P_{on} = \frac{\left(I_{\mathrm{LV_{RMS,sw}}} + I_{\mathrm{rr}}\right) V_2 \left(t_{\mathrm{ir}} + t_{\mathrm{vf}} + t_{\mathrm{rr1}}\right)}{2} f_{\mathrm{sw}} \tag{9}$$

where I_{rr} is the peak reverse recovery current, the t_{ir} is the current rise time, the t_{vf} is the current fall time and t_{rr1} is the first interval of the diode reverse recovery current in seconds [17]. Due to relatively high current the conduction losses on the LV side are significant:

$$P_{\mathrm{cond}} = 4 R_{\mathrm{DS,on}} I^2_{\mathrm{LV_{RMS,sw}}} \tag{10}$$

Since for the grid applications the active cooling can be impractical it is important to reduce the losses. One possibility to reduce the losses on the LV side full bridge is to parallel the MOSFETs. The parallelization of the MOSFETs is in general considered to be practical due to the positive thermal coefficient of the $R_{\mathrm{DS,on}}$ which ensures thermal stability, although the main advantage is relatively narrow range of differences between parts characteristics [18]. The estimation of the losses in paralleled MOSFETs on the LV side, calculated from (8), (9), and (10) is in Fig. 4. The extra losses due to the static and dynamic unbalances [19] of the paralleled MOSFETs are neglected in Fig. 4 because of the narrow difference range of MOSFETs characteristics.

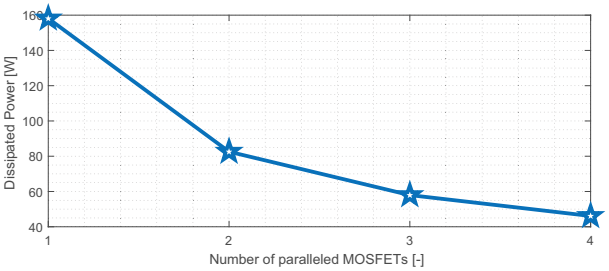

Fig. 4. The DAB LV side losses evolution with the number of paralleled MOSFETs. The MOSFET used for calculation is IRFRU7740PbF.

If 4 MOSFETs are paralleled the total losses in the semiconductors in the lagging full bridge will be 46.12 W. The losses in the leading full bridge are only caused by $R_{\mathrm{DS,on}}$, calculated with (7) and amount to 45.83W. The HV side must avoid hard switching at all costs, because the high voltage would result in substantial losses. This makes paralleling of the MOSFETs on HV impractical due to the $C_{\mathrm{oss,eff}}$ influence on ZVS range.

TABLE III. THE DESIGN PARAMETERS OF THE FULL BRIDGE CONVERTER

Parameter	Acronym	Value
Maximum Power	P_{max}	2 [kW]
Input Voltage	$V_{\mathrm{in,nom}}$	35 [V]
Output Voltage	V_{out}	-20 to 20 [V]
Max. Current	$I_{\mathrm{max,RMS}}$	-100 to 100 [A]
Line Inductance 1	L_1	0.15 [mH]
Line Inductance 2	L_2	0.15 [mH]
Line Series Capacitor	C_{series}	10 [μF]

2) Full Bridge Converter: The maximum current of the full bridge converter is given by the maximum rated current of the grid and the number of modules connected in parallel. The size of the capacitance is given by the allowable voltage ripple and the additional charge created by the current ripple. Since the capacitors are often the components with the lowest lifetime [12], the capacitances are usually kept low. The passives can be chosen from the calculation of the voltage and the current ripple of the full bridge with the bipolar modulation, such that the grid power quality requirements are met. In the Fig. 5 the relationship between the peak-to-peak value of the current ripple and the value of the inductance and capacitance is shown.

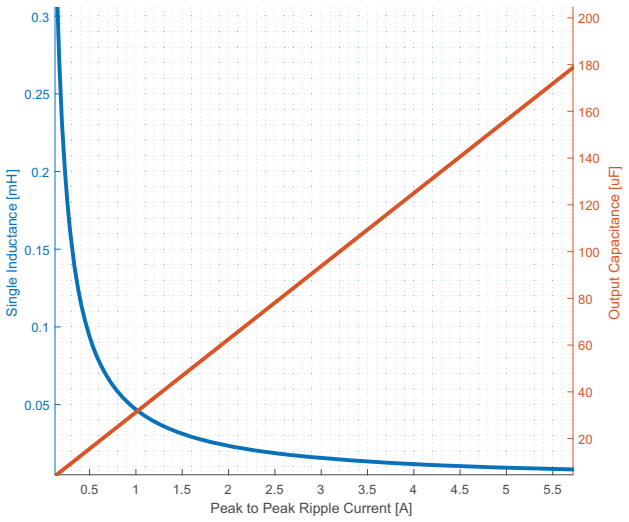

Fig. 5. The size of the passive components of the full bridge converter as a function of the peak to peak current ripple, when voltage ripple equal to 0.2% of V_{out} is allowed.

Since the full bridge converter is connected to large inductance reducing the switching losses through the zero voltage switching is not possible; therefore, the MOSFETs are paralleled. When four IRFP3206PBF are used the losses in the active part of the full bridge are 72.8 W.

This section illustrated the challenges in the design of the converter module for the power flow control converter. Processing of the high current and relatively large passive components limit the efficiency of the proposed device. However, the PFCC is rated only for a fraction of the grid power. Hence, for a DC grid rated for 100 kW, the installed PFCC can be rated for 10 kW. Using the given design, it would mean connecting five modules in parallel. The semiconductor losses in the module were estimated to be approx. 165 W. Thus the PFCC would operate at the efficiency of only $\approx 92\%$. However, from the grid perspective, it only represents $\approx 1\%$ losses. Therefore a comparable fully rated DC-DC transformer would need to have an efficiency of $98 - 99\%$.

IV. CONTROL OF THE POWER FLOW CONTROL CONVERTER

The control of the cascaded converters is a challenging task because the stability of the converter strongly depends on the impedance interaction between the converters [20]. Due to different control dynamics of the two converters large capacitor is required to absorb harmonics created by the operation of the cascaded converters [21]. The large capacitor is a weak point from the reliability point of view. Therefore several control

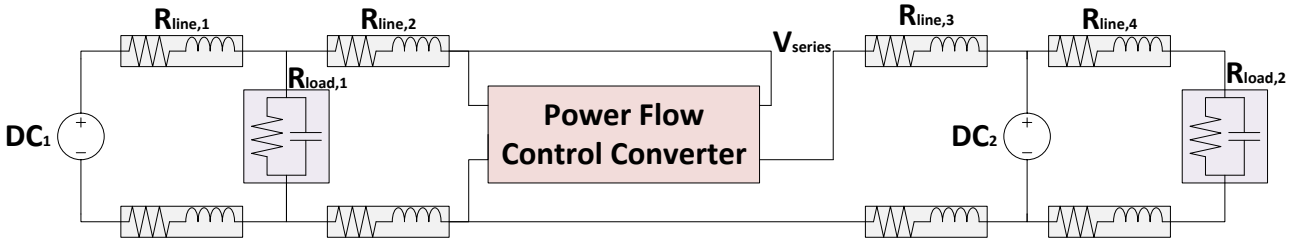

Fig. 6. The LVDC line with two sources and two loads. The power transfer is limited by the line characteristic impedances, each R_{line}, i represents 1 km long connection. The power flow can be increased by introducing a voltage drop in series with the line impedance.

improvements were proposed in the past for operation of the cascaded converters [21], [20].

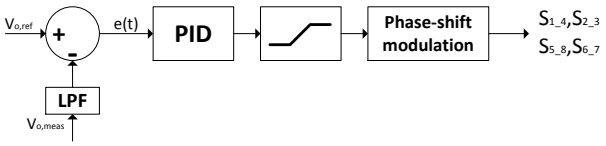

Fig. 7. Single loop control of the DAB. The control variable is the DC voltage on the DC link between the DAB and the full bridge. The DC link voltage is kept constant by the DAB.

Since for the current study the main aim is to study the functionality of the proposed device and identification of performance limitations, the authors have opted for a single loop control for the DAB. The decoupling capacitor between the DAB and the full bridge was chosen sufficiently large as a hardware solution for the aforementioned problem. To improve the performance a feed forward control for the DAB can be implemented, where the power reference of the full bridge is fed to the DAB control to improve the dynamic performance [21].

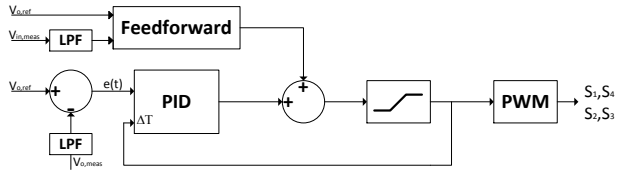

Fig. 8. The control of the full bridge converter implemented with the PID, feed forward, and tracking. The feed forward helps the full bridge to rapidly adapt the duty cycle, the derivative term damps out the oscillations and the tracking mode helps the anti-wind up.

The full bridge control has been implemented with a feed forward. The feed forward is based on the operation of the full bridge operated with the bipolar modulation. The feed forward is a duty cycle estimate

$$D = \frac{1}{2} + \frac{V_{\text{o,ref}}}{V_{\text{DC,in}}} \tag{11}$$

where the $V_{\text{o,ref}}$ is the output reference voltage of the full bridge converter, and the $V_{\text{DC,in}}$ is the DC link voltage. The back calculation with a tracking mode was applied to create an anti-wind up solution. The reference voltage for the full bridge comes from the system level control, that has information about the currents in other lines of the meshed grid.

V. Case Studies

In order to illustrate the functionality of the proposed power flow control converter, two case studies were selected. The first case is the basic meshed LVDC grid as illustrated in Section II and the second is an LVDC line. The first case study shows how the PFCC can prevent overloading of the LVDC line and the second case demonstrates how the power transfer limit of the line can be alleviated by the PFCC. In both cases, we have assumed a bipolar LVDC grid, with a power flow control converter operating on both poles of the grid. However, for the sake of simplicity, the simulation demonstrates only one pole. The line impedances are given in Table IV. The simulation was created in Simulink and the simulations start when the grid is in the steady state.

TABLE IV. The line impedances

Parameter	Acronym	Value
Line resistance	R_{line}	0.188 [Ω *per* km]
Line inductance	L_{line}	358 [μH *per* km]]

A. Meshed Grid Power Flow

The power flow limitations in a meshed grid are explained in the Section II. The case study connects three general nodes (modeled as voltage sources) by three lines of equal length and electrical properties. The electrical properties of the lines are in Table IV, each line is 1 km long. The situation is redrawn in Fig. 9. The power flow converter in this case study is operated in all four quadrants. The simulation parameters of the case study are given in Table V.

TABLE V. The simulation parameters for the LVDC meshed grid

Parameter	Acronym	Value
Source voltage	DC_1	375 [V]
Source voltage	DC_2	345-365 [V]
Source voltage	DC_3	345-365 [V]
PFCC output voltage	$V_s eries$	-10 - 10 [V]
Source capacitance	C_{1-3}	100 [μF]

In the Fig. 10 are the voltages in the lines measured with respect to the ground. The analysis start when the grid is in the steady state, and when the source DC_2 has the lowest voltage and the lines $R_{\text{line},3}$ and $R_{\text{line},1}$ are carrying the same current while the line $R_{\text{line},2}$ carries 80 A. The PFCC creates a positive series voltage equal to 10 V. The currents in the lines equalize. At 30 ms the lowest voltage is at source DC_3. The current flowing in line $R_{\text{line},3}$ reverses, and 80 A are flowing in line $R_{\text{line},1}$. The PFCC creates a negative series voltage equal to -10 V. The currents stabilize around the value of 60 A. It

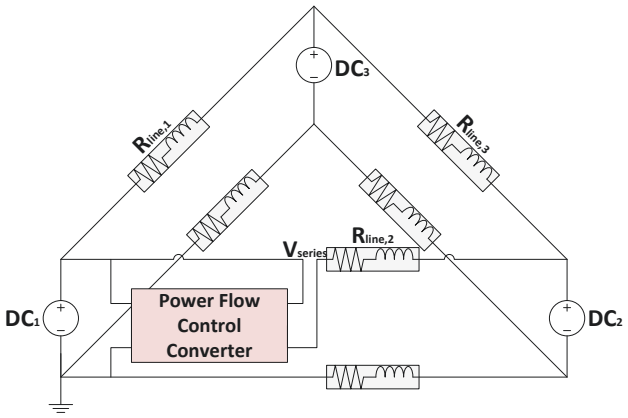

Fig. 9. The basic meshed grid, with three DC sources connected through lines of equal electric characteristics and equal length. The PFCC is installed at the DC source 1.

should be noted that the ringing in the voltage at 30 ms is created by the grid parameters and not by the PFCC.

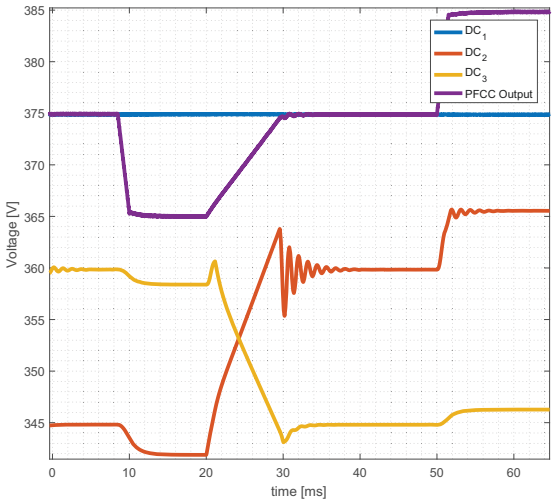

Fig. 10. The voltages of the nodes and the output of the PFCC. All the voltages are measured with respect to the ground.

B. Power Flow in LVDC line

The LVDC with two sources and two loads is shown in Fig. 6. The source DC_1 is operating at the 385 V, while the source DC_2 is operating at 340 V. The load $R_{\text{load},2}$ requires more power; however, the amount of power that can be transferred is limited by the line impedances. If the PFCC introduces a voltage drop in series with the line impedance, the amount of power that can be transferred increases. The simulation parameters of the case study are in the Table VI.

In the case of the line in Fig. 6, there are two unequal sources and two unequal loads. The power line ability to transfer power is limited by the line impedances. n Fig. 12 is illustrated a voltage drop created by the PFCC at time $t_1 = 8$ ms equal to -20 V. The current flowing from source 1 to load

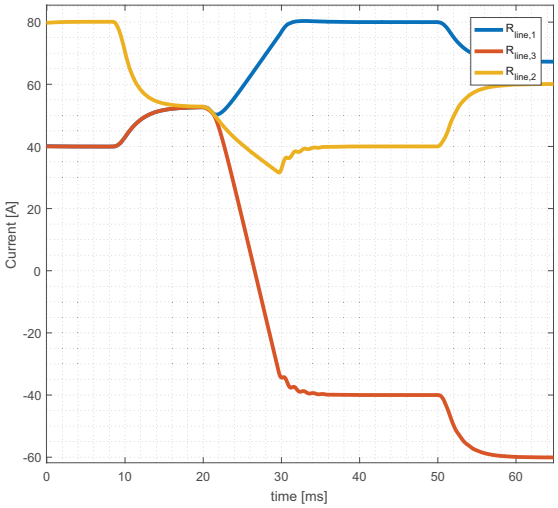

Fig. 11. The line currents in the basic meshed grid. The figure illustrates that the PFCC is able to accommodate the bidirectional power flow and create both positive and negative series voltage on the line $R_{\text{line},2}$.

TABLE VI. THE SIMULATION PARAMETERS FOR THE LVDC LINE.

Parameter	Acronym	Value
Source DC_1 voltage	DC_1	385 [V]
Source DC_2 voltage	DC_2	340 [V]
Load voltage	$V_{load,1}$	350 [V]
Load voltage	$V_{load,2}$	315 [V]
Source DC_1 capacitance	C_{DC_1}	100 [μF]
Source DC_2 capacitance	C_{DC_2}	100 [μF]
Load 1 resistance	$R_{\text{Load},1}$	5.5 [Ω]
Load 2 resistance	$R_{\text{Load},2}$	3 [Ω]
Load capacitances	$C_{\text{Load},1\&2}$	100 [μF]

2 are increased and the amount of power transfer through the line is increased as well.

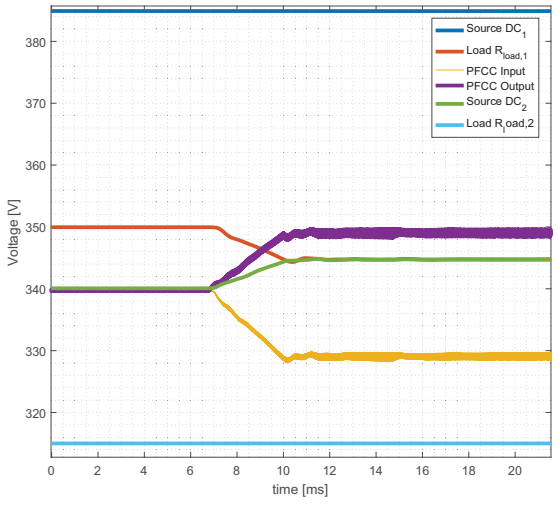

Fig. 12. The voltages measured to the ground on positions as illustrated in Fig.6. The voltages at the input and output of the PFCC contain ripple due to the switching of the converters.

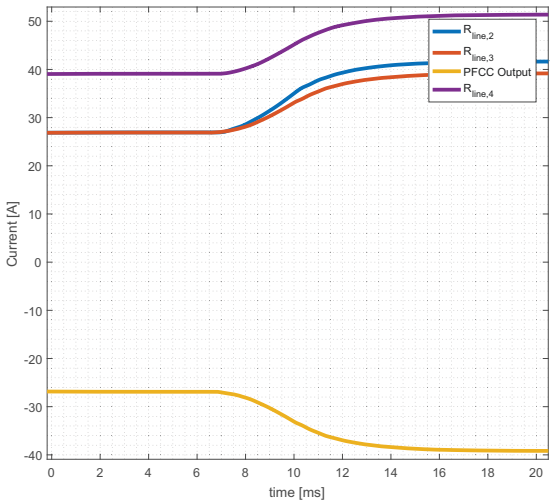

Fig. 13. The currents flowing in different parts of the LVDC line. The PFCC output current is the current which is circulated by the PFCC and therefore has a negative sign.

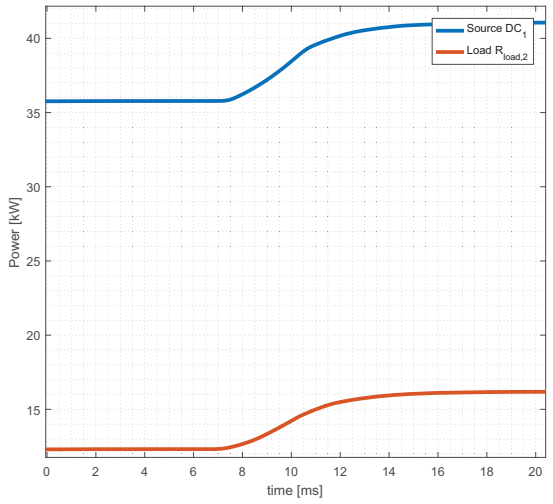

Fig. 14. The amount of transferred power increases due to the action of the PFCC.

This section demonstrated the functionality of the proposed power flow control converter. The power flow control converter can to some extent substitute fully rated DC-DC transformer in the connections and extended the range of the control solutions for the distribution operators. The PFCC can be used in the meshed LVDC grids, as well as in the point-to-point connections to improve the flexibility of the LVDC distribution.

VI. Conclusion

The controllability of the power flow control in the meshed distribution grids can be increased with PFCC which is rated only for a fraction of the grid rating. Compared to the fully rated DC-DC transformers the requirements on the efficiency of the PFCC can be loosened due to the partial rating. This is an important advantage considering the relatively high voltage step-down ratio inside the PFCC, which causes high currents in the LV part of the device. The high currents in LV side require MOSFET paralleling, which implies higher part count. Furthermore, the control range and the stability of the PFCC is inherently limited by the impedance interaction between the two sub-converters.

In preceding studies, the power flow control has been investigated for both the multi-terminal HVDC transmission grids and the meshed LVDC distribution grids. For both the HVDC transmission and the LVDC distribution the partially rated devices are an interesting option from the cost perspective. In order to better understand the potential of the partially rated PFCCs in the meshed LVDC distribution, the next step is to compare the PFCC with the fully rated DC-DC transformer in terms of efficiency, cost, and controllability. The comparison will establish estimates where the partially rated device is more advantageous than the fully rated one.

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