A low-noise amplifier for ultrasound imaging with continuous time-gain compensation

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by

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ABSTRACT

This work presents a low-noise amplifier (LNA) for ultrasound imaging with built-in continuous time-gain compensation (TGC), which compensates for the time-dependent attenuation of the received echo signal and thus significantly reduces its dynamic range (DR).

The proposed design combines the LNA and TGC functions in a single variable-gain current-to-current amplifier. Compared to conventional ultrasound front-ends, which implement the TGC function after an LNA that needs to handle the full DR of the echo signal, this approach can highly reduce the power consumption and the size. Compared to earlier programmable-gain LNAs with discrete gain steps, the continuous gain control avoids switching transients that may lead to imaging artefacts.

The TGC function is realized by a novel feedback network consisting of a double differential pair that feeds a fraction of the output current back to the input. This fraction can be changed continuously using a control voltage that is applied to the gates of the differential pairs, to realize a gain range from -20 dB to $+20$ dB.

To achieve an approximately constant closed-loop bandwidth in the presence of the changing feedback factor, a loop amplifier has been implemented whose gain is changed along with the feedback factor by dynamically changing its bias currents. This loop amplifier employs a current-reuse architecture to achieve high power-efficiency. In addition, a variable bias current source has been designed to appropriately bias the TGC feedback network. By employing a similar double differential pair topology as in the feedback network, this current source provides the required low noise at the highest gain setting and high current at the lowest gain setting within the available headroom.

The LNA with built-in TGC function has been realized in 180nm CMOS technology. It has been optimized to interface with a 7.5 MHz capacitive micromachined ultrasonic transducer (CMUT). Simulation results show that it achieves a 3dB bandwidth higher than 40 MHz across the full gain range. At the highest gain setting, its input current noise is 0.96 pA/$\sqrt{\text{Hz}}$ at 7.5 MHz. This leads to an input dynamic range of 93 dB, which is compressed into an output dynamic range of 53 dB by means of the 40 dB variable gain. The amplifier consumes 10.8 mW from a 1.8V supply, and occupies an estimated 320 x 320 μm^2 die area.

Keywords: Ultrasound application-specific integrated circuit (ASIC), low-noise amplifier, time-gain compensation, current-steering differential pair, variable bias current source.

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

LNA low-noise amplifier iii
TGC time-gain compensation iii
DR dynamic range iii
CMUT capacitive micromachined ultrasonic transducer iii
ASIC application-specific integrated circuit iii
TIA transimpedance amplifier x
ICE intracardiac echocardiography 1
RX receive 1
TX transmit 1
VGA variable gain amplifier 3
ADC analog to digital converter 3
CDN current division network 4
TGCLNA time-gain compensation low-noise amplifier 7
DC Direct-Current 9
AC Alternating-Current 12
rms root mean square 13
SNR signal to noise ratio 13
DAC digital to analog converter 15
PCB printed circuit board 46

1 INTRODUCTION

In the past, due to the expensive price and complicated process of diagnosis, cardiovascular diseases became the most common causes of death for poor people [1]. Nowadays, ultrasound imaging is a safe and cost-effective means of diagnosing cardiovascular diseases. In traditional ultrasonic imaging systems, the ultrasound probe is connected to a big machine via a cable [2].

In recent years, portable and miniaturized ultrasound scanners have emerged due to their potential of solving some of the limitations of static scanners. These devices are handheld sized or even smaller, and they have a much lower cost per unit, which enhances both the transportability and accessibility of ultrasound scanning. Such devices require ASICs to interface with the ultrasound transducer while minimizing the area and power consumption. [3]

A critical part of such ultrasound ASICs is the receive front-end, which processes the echo signals received by the transducer. This typically consist of an LNA followed by a TGC amplifier. This thesis focus on an LNA design that incorporates the TGC function to arrive at a more compact and power efficient solution.

1.1 BACKGROUND

An example application area in which the work described in this thesis may be applied is catheter-based ultrasound imaging during minimally-invasive interventions.

A variety of cardiovascular conditions can be treated using minimally-invasive interventions. These interventions are much less stressful to the patient than conventional surgery, shortening recovery time and allowing treatment to take place even at an advanced age. Ultrasonic imaging is one of the typical imaging methods used for minimally-invasive interventions.

In intracardiac echocardiography (ICE), a catheter containing a miniature ultrasound transducer is directed into the heart, allowing the imaging of cardiac structures from an intracardiac viewpoint. [4]

By using the ultrasonic imaging system, an ICE probe as shown in figure 1.1 can help in visualizing the left atrium and pulmonary veins during ablation treatment of atrial fibrillation. [5]

Figure 1.2 shows a block diagram of a typical ultrasound imaging system. The front-end electronics that interface with the transducer elements can be divided into a receive (RX) circuit and transmit (TX) circuit. In ultrasonic imaging, high-frequency acoustic waves are used to image tissue. These high-frequency acoustic waves are emitted by a transducer, when high voltage pulses which are generated by the TX circuit, are imposed on the transducer. The transducer is made of piezo material. As shown in figure 1.3, the transducer can be modelled as a resonator parallel with a capacitance. The acoustical wave reflects on materials with different acoustic impedance.

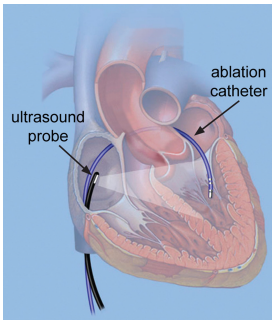


Figure 1.1: Ultrasound probe

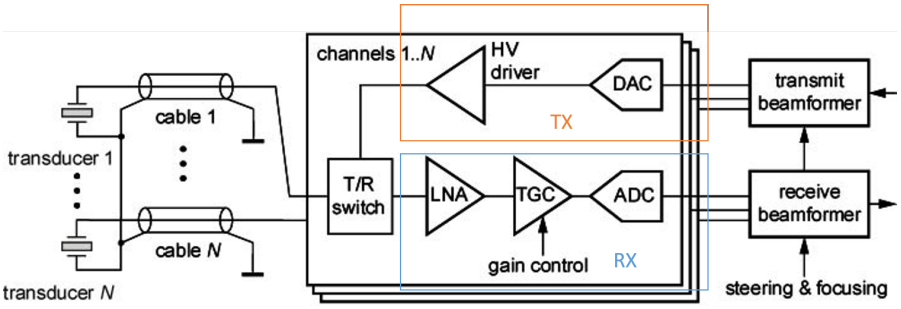


Figure 1.2: Diagram of an ultrasound imaging system

The reflection can be detected by the transducer as well, as a current signal is generated by the reflected wave. This echo signal is received by the RX circuit and is turned into an image at the end.

For minimally-invasive devices like an ICE probe, the front-end electronics need to be intergrated on an in-probe ASIC, the size of which should be small enough. Miniaturization is one of the main concerns to design the chip. In addition, a smaller area of the chip means lower cost of fabrication. In addition, for the safety of the patient, the power consumption of the probe cannot be high. Temperature rise associated with self-heating should be kept within regulatory limits.

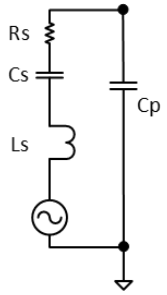


Figure 1.3: Equivalent circuit model of an ultrasound transducer

1.2 INTRODUCTION OF TIME GAIN COMPENSATION

A TGC amplifier is a key building block of an ultrasound RX front-end as shown in figure 1.2. It is a kind of variable gain amplifier (VGA). The gain of this VGA changes as a function of time.

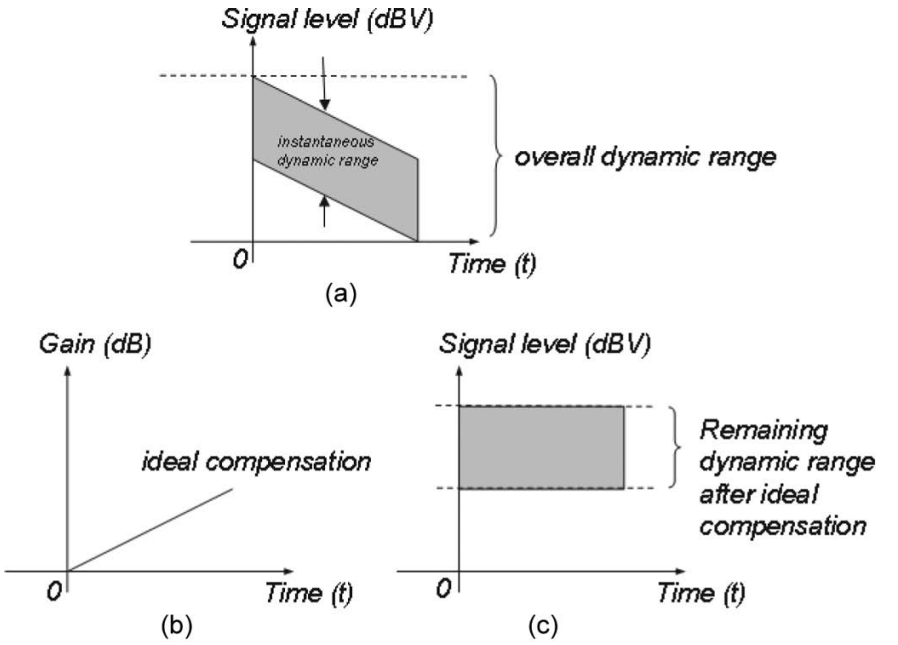


Figure 1.4: The echo signal amplitude before and after time-gain compensation [6]

The amplitude of the echo signal from the transducer is attenuated exponentially with the imaging depth. If the speed of acoustic waves can be assumed as constant, the receiving time of echo signal is proportional to the imaging depth as shown in figure 1.4a. Without compensation, the deeper tissues will correspond to smaller echo signal and thus will appear lighter in the ultrasound image because of different attenuation of the echo signal. Apart from the attenuation of the echo signal, the amplitude of the echo signal has a certain instantaneous dynamic range, i.e 40 dB. Therefore, the whole dynamic range of echo signal is a sum of the dynamic range (40 dB in this project) caused by the attenuation and the instantaneous dynamic range which is caused by the variation of the signal itself. To process such a high dynamic range without time gain compensation amplifier, a power hungry RX circuit is needed, including a potentially-large high-resolution analog to digital converter (ADC). In order to compensate for the attenuation of echo signal and reduce the requirement of ADC, a TGC is added between transducer and ADC to handle a 40 dB dynamic range of echo signal as shown in figure 1.4b, c.

For a TGC, the gain should change linearly in dB as a function of time as shown in figure 1.4b. The gain of the TGC has to change continuously and smoothly.

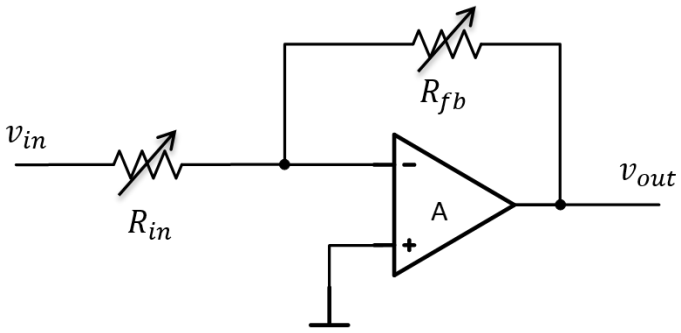


Figure 1.5: A TGC with digitally-programmable resistive feedback [10]

1.3 PRIOR ART

A time gain compensation amplifier is a special kind of variable gain amplifier. Conventional TGCs can usually be classified into three different kinds. These kinds of TGCs will be introduced below.

1.3.1 TGCs with discrete gain steps

TGC with discrete gain steps can be seen as a kind of programmable gain amplifiers. There are various ways in which programmable gain can be implemented, including

- Digitally-programmable resistive feedback [7]
- Digitally-programmable capacitive feedback [8]
- Digitally-controlled current division [9]

As shown in figure 1.5, the TGC can be realized by using digitally-programmable resistive feedback. The gain of the TGC is set by changing the effective values of the input resistance and the feedback resistance. [7]

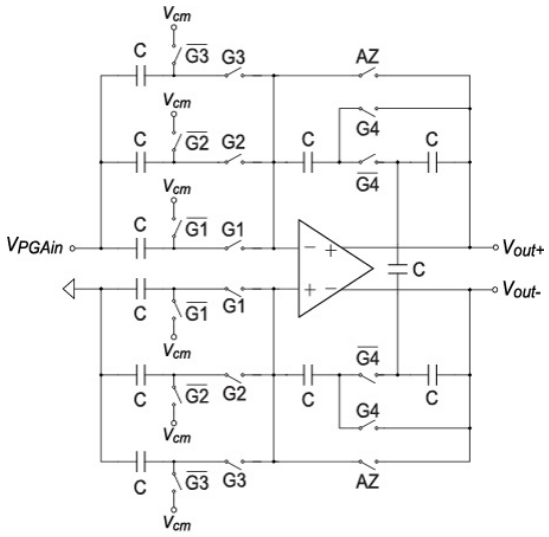
In addition, the TGC can also be realized by using digitally-programmable capacitive feedback as shown in figure 1.6. The gain of the TGC is determined by the ratio between input capacitance and feedback capacitance, which can be changed by turning on or turning off the switches in different branches. [11]

As shown in figure 1.7, instead of using a variable-resistance feedback, the TGC can also be realized by fixed-resistance feedback with a current division network (CDN). The gain of the TGC is determined by the ratio of the resistances and the current ratio of the input branch and the feedback branch. [12]

By changing the value of capacitance, resistance, or the g_m ratio in the feedback network, the gain of TGCs can be changed in discrete steps. However, an important problem of this kind of TGCs is that they will bring imaging artefacts when switching from one gain step to the next. To solve this problem, a variable gain amplifier with a smooth gain control is needed.

1.3.2 TGCs that interpolate between discrete gain steps

To avoid gain-switching artefacts, a TGC that interpolates between discrete gain steps is one kind of solution. The interpolation can be implemented



	G1	G2	G3	G4
6 dB	0	1	1	1
12 dB	0	1	0	0
18 dB	0	1	1	0
24 dB	1	1	1	0

Figure 1.6: A TGC with capacitive feedback associated with the gain control code map [11]

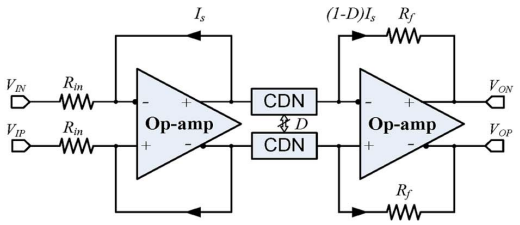


Figure 1.7: A TGC with current division network [12]

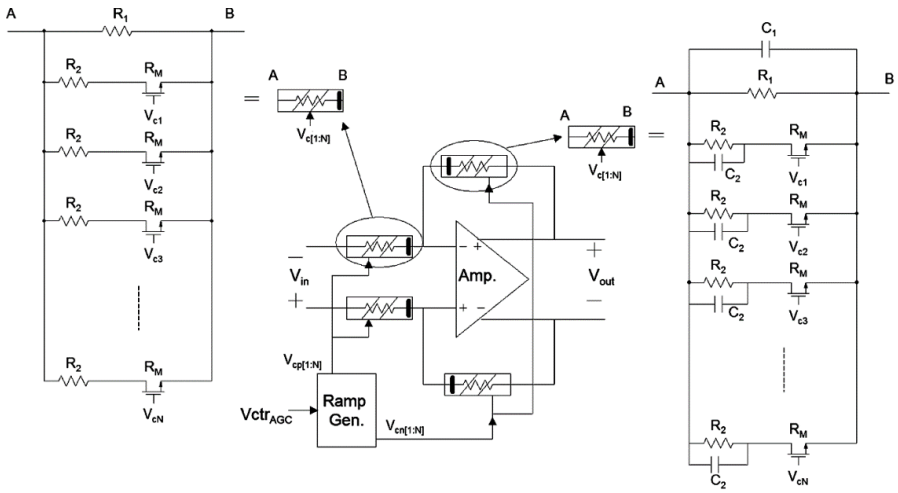


Figure 1.8: A TGC with the interpolation of tuned feedback resistors [10]

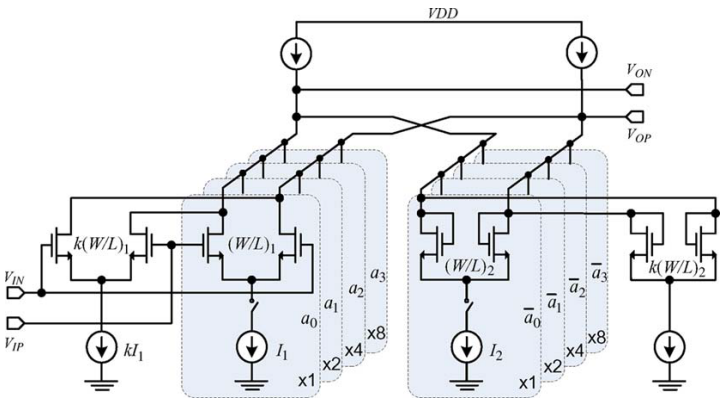


Figure 1.9: A TGC with multiple input pairs and load pairs [12]

by means of tuned feedback resistors as shown in figure 1.8. The effective value of the feedback resistors is controlled by a continuous ramp control signal. As a result, the effective feedback resistances change smoothly. [10] However, the noise problem of resistive feedback is hard to be solved.

Instead of using a feedback loop, an open loop can be used to build the TGC. The interpolation can also be implemented by means of multiple input pairs, as shown in figure 1.9. The differential pairs in a_1, a_2, a_3, a_4 will be active in different desired gain settings respectively. The gain of this circuit is determined by the ratio between effective $g_{m,input}$ and effective $g_{m,load}$. [12]

However, when multiple input stages are active simultaneously, the varying offset will cause ripple and non-linearity. For the other method, the resistor ladder loads the source, which may affect the input impedance of the input stage.

1.3.3 TGCs that use approximately-exponential variable-gain circuits

To achieve the exponential function, various ways of approximation have been reported [13, 14]. One of the most typical approximations is using equation 1.1 to realize exponential behavior [15].

$$e^{2x} \simeq (1+x)/(1-x). \tag{1.1}$$

1.4 MOTIVATION

Because of the poor noise performance, it is not a good choice for a TGC to be built with resistive feedback. In addition, to avoid the artefacts, a TGC should not be realized with discrete gain steps.

Besides, a TGC with capacitive feedback will occupy a large area due to the big capacitance. In order to reduce the area of the ASIC, the amplifier, whose gain is directly determined by the current division without capacitive feedback, will be designed in this project.

In the conventional circuits, due to the noise requirement, there is an LNA between the transducer and the TGC, as shown in figure 1.2. It means that the LNA still have to handle the full dynamic range of the echo signal, which is typically very power hungry. To reduce the power consumption of

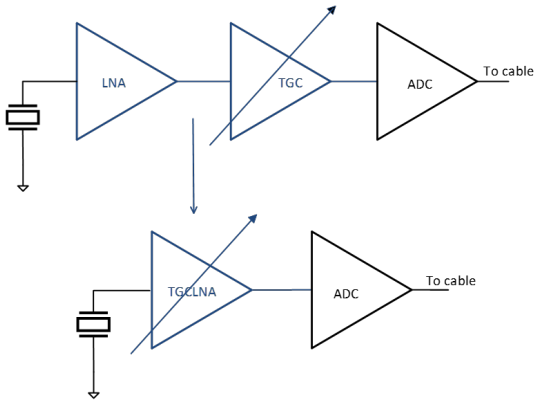


Figure 1.10: Combination of the TGC and the LNA

the RX circuit, a TGCLNA is necessary for ultrasound imaging, as shown in figure 1.10.

Therefore, in this thesis project, a TGCLNA will be designed by using approximately-exponential variable-gain circuits with the approximations in equation 1.1.

1.5 DESIGN OBJECTIVE

In this project, the time-gain compensation low-noise amplifier (TGCLNA) will be designed for a 64-channel 2D ICE probe. The ASIC will be designed in TSMC's 180 nm BCD-Gen2 technology. The target specifications of this TGCLNA are shown in Table 1.1. The area and power consumption of the ASIC will be minimized while achieving these design targets. The targeted area is smaller than $300\mu m \times 300\mu m$.

Table 1.1: Target specifications

Signal frequency	7.5 MHz
Bandwidth	>15 MHz
Gain range	-20 dB $\sim +20$ dB
Input signal amplitude	1 μA_{pk-pk} to 100 μA_{pk-pk}
Input noise (the smallest signal case)	1 pA/$\sqrt{\text{Hz}}$

The model of the CMUT, which is used for this work is shown in figure 1.11.

1.6 THESIS ORGANIZATION

This thesis presents the steps taken to design an LNA for ultrasound imaging with continuous time-gain compensation. The thesis starts with the concept ideas and discussions on possible circuit topologies converging towards a good circuit implementation.

Chapter 2 discusses the architecture of the TGCLNA.

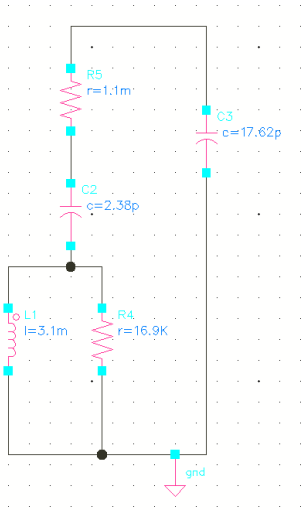


Figure 1.11: Model of the CMUT

Chapter 3 discusses the circuit implementations to realize the architecture onto an ASIC.

Chapter 4 shows the performance of the TGCLNA in simulation.

Chapter 5 concludes the thesis by discussing the performance of the final circuit and presents some ideas for future work and improving the design.

2 ARCHITECTURE

2.1 BASIC THEORY

From equation 1.1, a rational function is used to approximate the exponential function. This section will focus on the implementation of this $(1+x)/(1-x)$ function in the circuit.

2.1.1 Linearity of the differential pair

Because both $1+x$ and $1-x$ are linear functions, to design a circuit that implements the desired rational function, the linearity of the differential pair can be used.

First of all, a schematic of a differential pair is shown in figure 2.1. If the tail current I_{ss} of the differential pair is constant and the sizes of two transistors are equal, the difference of the drain currents in two branches is proportional to the difference of the gate voltages of the two transistors in small-signal regime. This ideal linearized Direct-Current (DC) characteristic of a differential pair is shown in figure 2.2. When the gate voltage V_{in1} of transistor M_1 is equal to V_{in2} of transistor M_2, half of tail current I_{ss} flows into the left branch. The rest of half I_{ss} flows into M_2.

Actually, the tail current splits into two branches according to the transconductance (g_m) ratio of these two transistors. If both transistors work in the same saturation state, the g_m of the transistor is proportional to the gate voltage minus the threshold voltage (V_{gt}) of the transistor. That is the reason why the drain current of each branch is proportional to the difference of gate voltages of two transistors as shown in figure 2.2. Therefore, from the differential pair, good linearity is shown between the drain current and the difference of gate voltages.

In fact, because of the different current densities of the two transistors, when the drain current of one transistor is small, the transistor may fall into the weak inversion region and finally cut-off, which will cause a mismatch between two transistors. This mismatch will bring some non-linearity to

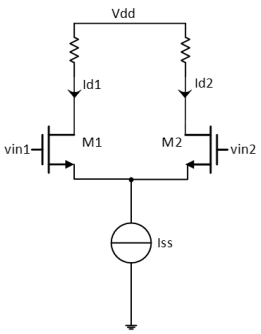


Figure 2.1: A schematic of a differential pair

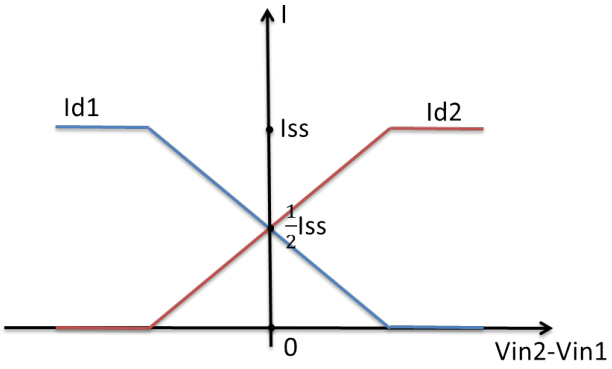


Figure 2.2: Ideal DC current of the differential pair

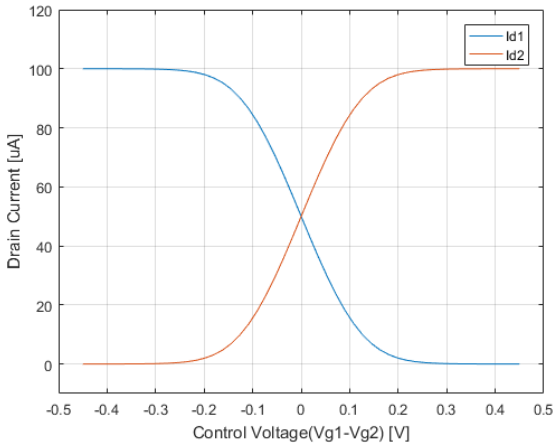


Figure 2.3: Simulated DC current of the differential pair

the differential pair. When the difference of the gate voltages is bigger, the mismatch of two transistors is larger. Finally, the drain current behavior of the differential pair looks like figure 2.3.

2.1.2 Realization of the $(1+x)/(1-x)$ function

After discussing the linearity of the differential pair, the use of the differential pair to obtain the $(1+x)/(1-x)$ function will be explained. As a first step, figure 2.4 shows how the $1+x$ function can be implemented. The tail current is the input and the drain current of M_2 is chosen as the output. I_{in} is the bias tail current. i_{in} is the small-signal input current injected from the top. I_{out} is the bias drain current of M_2. i_{out} is the small signal in the output. If both of transistors M_1 and M_2 work in saturation mode, the drain currents of two transistors are determined by the g_m ratio of M_1 and M_2. Then,

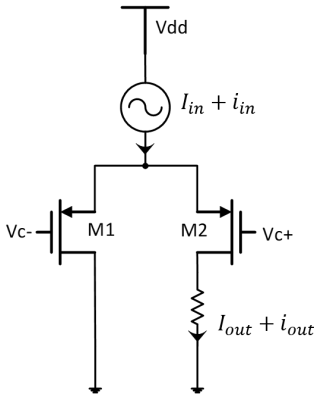


Figure 2.4: Implementation of the $1 + x$ function using a differential pair

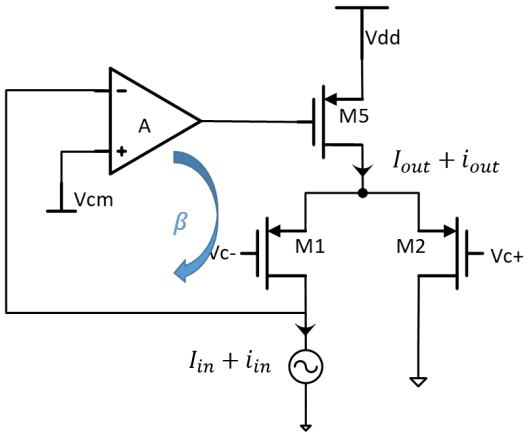


Figure 2.5: Implementation of the $1/(1-x)$ function using a differential pair

when M_1 and M_2 have the same width and length, the transfer function of the circuit can be expressed as [16]:

$$\frac{i_{out}}{i_{in}} \approx \frac{g_{m2}}{g_{m1}+g_{m2}} \approx \frac{\mu C_{ox}(W/L)_2 V_{gt2}}{\mu C_{ox}(W/L)_1 V_{gt1} + \mu C_{ox}(W/L)_2 V_{gt2}} = \frac{V_{gt2}}{V_{gt1}+V_{gt2}}$$
$$\approx \frac{V_{gt0} + \frac{1}{2}\triangle V_{gt}}{V_{gt0}} = \frac{1 + \frac{\triangle V_{gt}}{2V_{gt0}}}{2} \tag{2.1}$$

In this equation, $g_{m,n}$, W_n and $V_{gt,n}$ are the transconductance, the width and the difference between the gate voltage (V_g) and the threshold voltage (V_t) of transistor M_n, respectively. V_{gt0} is the V_{gt} when V_{g1} is equal to V_{g2}. In this situation, the threshold voltage of two transistors can be seen as the same.

If $x = \frac{\triangle V_{gt}}{2V_{gt0}}$, then the transfer function of the circuit in figure 2.4 can be simplified as:

$$\frac{i_{out}}{i_{in}} \approx \frac{1+x}{2} \quad \text{with} \quad (x = \frac{\triangle V_{gt}}{2V_{gt0}}) \tag{2.2}$$

As a second step, figure 2.5 shows how the $1/(1-x)$ function can be implemented. The drain current of transistor M_1 is the input and the tail

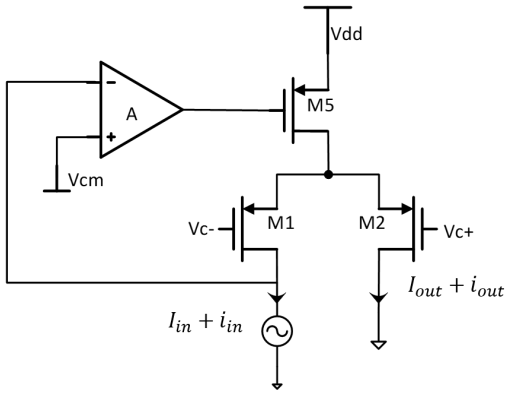


Figure 2.6: Implementation of the $(1+x)/(1-x)$ function using a differential pair

current is chosen as the output. If transistors M_1, M_2 and M_5 work in saturation mode, the drain currents of two transistors are determined by the g_m ratio of M_1 and M_2. Then, the transfer function of the circuit in figure 2.5 can be derived by the equation as follows, where β is the current-gain feedback factor from the output to the input:

$$\begin{aligned}\frac{i_{out}}{i_{in}} &= \frac{A}{1+A\beta} \approx \frac{1}{\beta} \approx \frac{\mu C_{ox}(W/L)_1 V_{gt1} + \mu C_{ox}(W/L)_2 V_{gt2}}{\mu C_{ox}(W/L)_1 V_{gt1}} \\ &= \frac{g_{m1}+g_{m2}}{g_{m1}} = \frac{V_{gt1}+V_{gt2}}{V_{gt1}} \approx \frac{2V_{gt0}}{V_{gt0}-\frac{1}{2}\triangle V_{gt}} = \frac{2}{1-\frac{\triangle V_{gt}}{2V_{gt0}}}\end{aligned} \tag{2.3}$$

If $x = \frac{\triangle V_{gt}}{2V_{gt0}}$, then the transfer function of the circuit in figure 2.5 can be simplified as:

$$\frac{i_{out}}{i_{in}} \approx \frac{2}{1-x} \quad \text{with} \quad (x = \frac{\triangle V_{gt}}{2V_{gt0}}) \tag{2.4}$$

After creating the circuits of $1+x$ and $1/(1-x)$ function respectively, a circuit with $(1+x)/(1-x)$ function can be designed by the combination of these two circuits,as shown in figure 2.6. In this circuit, the drain of transistor M_1 is seen as the input and the drain of M_2 is the output. The Alternating-Current (AC) gain of this circuit is determined by the g_m ratio of these two transistors, when M_1, M_2 and M_5 are in saturation region:

$$\begin{aligned}\frac{i_{out}}{i_{in}} &\approx \frac{g_{m2}}{g_{m1}} \approx \frac{V_{gt2}}{V_{gt1}} \approx \frac{V_{gt1}+V_{gt2}}{V_{gt1}} \times \frac{V_{gt2}}{V_{gt1}+V_{gt2}} \\ &= \frac{1+\frac{\triangle V_{gt}}{2V_{gt0}}}{1-\frac{\triangle V_{gt}}{2V_{gt0}}}\end{aligned} \tag{2.5}$$

If $x = \frac{\triangle V_{gt}}{2V_{gt0}}$, then the transfer function of the circuit in figure 2.6 can be simplified as:

$$\frac{i_{out}}{i_{in}} \approx \frac{1+x}{1-x} \quad \text{with} \quad (x = \frac{\triangle V_{gt}}{2V_{gt0}}) \tag{2.6}$$

2.2 TIME-GAIN COMPENSATION CIRCUIT

2.2.1 Single differential pair

From the last section, the exponential approximation is realized by the differential pair. In the approximation, the x is expressed as:

$$x = \frac{\triangle V_{gt}}{2V_{gt0}} = \frac{V_{c+} - V_{c-}}{2V_{gt0}} \tag{2.7}$$

V_{gt0} in equation 2.7 can be seen as constant. If the difference of the gate voltages $V_{c+} - V_{c-}$ changes linearly by time, then the gain of the circuit in figure 2.6 is changed arpproximately exponentially as a function of time. Thus, time-gain compensation can be implemented by using a single differential pair.

The noise of this circuit will now be analyzed, being noted that the bias point of the transistors changes considerably as the gain is swept across the desired 40 dB range.

In a single differential pair shown in figure 2.6, if most of the tail current flows into M_1, the input referred noise can be derived by equation [16]:

$$i_n \approx \sqrt{\frac{2}{3} 4kTg_{m,M1}B} \tag{2.8}$$

The amplitude of input current changes from 1 μA peak to peak to 100 μA peak to peak. If the circuit uses 1 μA to 100 μA DC current to bias the echo signal, the root mean square (rms) value of signal can be calculated as:

$$I_{sig,rms} = \frac{\sqrt{2}}{4} I_{sig,pk-pk} = \frac{\sqrt{2}}{4} I_{d,M1} \tag{2.9}$$

Meanwhile, the transconductance of the transistor M_1 can be defined as follows, when M_1 is in saturation region [16]:

$$g_{m,M1} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{d,M1}} \tag{2.10}$$

Therefore, assuming the noise of M_1 is the dominant noise source, the signal to noise ratio (SNR) can be expressed as:

$$SNR = 20lg(\frac{I_{sig}}{I_n}) = 20lg(\frac{\frac{\sqrt{2}}{4} I_{d,M1}}{\sqrt{\frac{2}{3} 4kTg_{m,M1}B}}) = 20lg(\frac{\frac{\sqrt{2}}{4} I_{d,M1}}{\sqrt{\frac{2}{3} 4kT \sqrt{2\mu C_{ox} \frac{W}{L} I_{d,M1}} B}}) \tag{2.11}$$

From equation 2.11, the signal floor is proportional to the fourth power of the noise floor. As shown in figure 2.7, the SNR is the worst, when the amplitude of input signal current is the smallest. In order to reduce the noise, a small g_m is required. In the high gain setting case, the bias input current is 1 μA. To reduce the g_m of the transistor, it means a small size and short width transistor is needed.

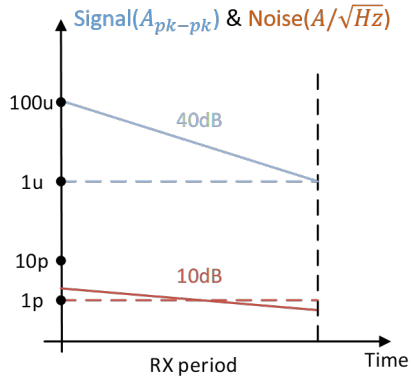


Figure 2.7: The signal amplitude and the noise floor

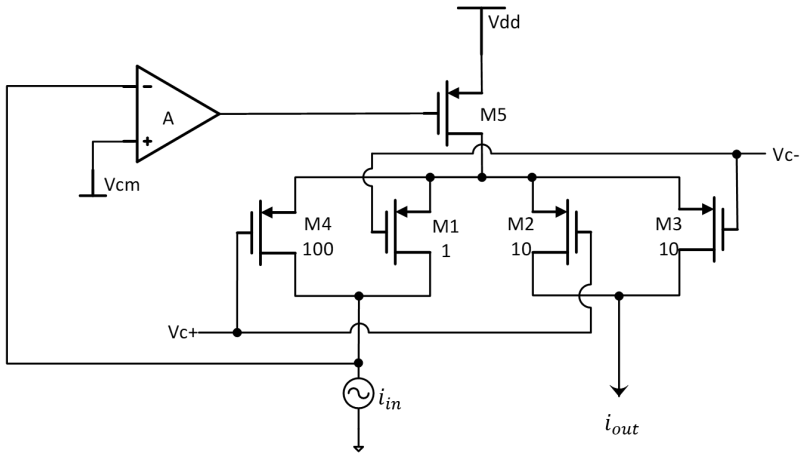


Figure 2.8: The TGC with parallel differential pair

On the contrary, transistor M1 in figure 2.6 is facing the whole 40 dB dynamic range of input current from 1 μA peak to peak to 100 μA peak to peak. In order to ensure M_1 works in saturation mode in the whole process, a large size and long width transistor is necessary. Otherwise, it will cause a large headroom problem of the circuit. Therefore, there is a trade-off between noise and headroom.

2.2.2 Parallel differential pair

As shown in figure 2.8, instead of keeping the width of differential pair transistors constant, a parallel differential pair is added to change the effective width of the whole differential pair as well.

In this circuit, when the input echo signal is the smallest with 1 μA peak to peak, the gate control voltage V_{c+} of transistors M_2 and M_4 is much higher than the other gate control voltage V_{c-} of transistors M_1 and M_3. In this case, the differential pair of M_1 and M_3 is on and the other differential pair of M_2 and M_4 is off. All the tail current $I_{d,5}$ flows into M_1 and M_3. The gain of this state is determined by the g_m ratio of M_3 and M_1, which is equal to the width ratio of M_3 and M_1, due to the gate voltage of these two transistors are the same. The DC gain is 10. Meanwhile, from the input, the transducer mainly sees the noise contributed from transistor M_1 with small size, small current and also small g_m. Therefore, in this case, the noise

contribution of TGC is the smallest case and the SNR is the best. The gain of TGC is the highest with 20dB gain.

On the contrary, when the input echo signal is the largest with 100 μA peak to peak, the gate control voltage V_{c+} is much lower than V_{c-}. In this case, the differential pair of M_2 and M_4 is on and the other differential pair of M_1 and M_3 is off. All the tail current $I_{d,5}$ flows into M_2 and M_4. At that time, the current gain from input to output is defined by the width ratio between M_2 and M_4, which is 0.1. Although the amplitude of the echo signal is increased, the effective size of the parallel differential pairs is also increased. The current density of the parallel differential pairs remains the same. Therefore, there is no headroom problem even in low gain setting case. In addition, the whole differential pair works in the same saturation region, which can avoid the mismatch of the transistor. In this state, the gain of TGC is the lowest with -20 dB gain.

In total, this circuit has 40 dB gain range. If the gate control voltage V_{c+} and V_{c-} are chosen properly, the gain of TGC can change exponentially as a function of time.

In this topology, the effective widths of the parallel differential pair change by the gate control voltage, instead of keeping the widths constant. Compared with the circuit with a single differential pair, the current density of the transistors remains the same in the whole gain range in this new circuit, so the headroom of two branches also remains the same in the whole gain range. If the headroom of this new topology in the highest gain setting case is enough, the headroom is enough in the whole gain range. Meanwhile, the highest gain setting case is the worst case for noise. Therefore, this topology only requires to choose a proper size of M_1 to leave enough headroom and have a good noise performance in the highest gain setting case, which is much better than the former topology.

However, because the effective widths of the parallel differential pair are also variable, if the second-order effect can be neglected, equation 2.5 can be corrected as:

$$\begin{aligned}
\frac{i_{out}}{i_{in}} &\approx \frac{g_{m2}}{g_{m1}} = \frac{\mu C_{ox}(W/L)_2 V_{gt2}}{\mu C_{ox}(W/L)_1 V_{gt1}} = \frac{W_2 V_{gt2}}{W_1 V_{gt1}} \\
&= \frac{W_1 V_{gt1} + W_2 V_{gt2}}{W_1 V_{gt1}} \times \frac{W_2 V_{gt2}}{W_1 V_{gt1} + W_2 V_{gt2}} \\
&\approx \frac{2W_0 V_{gt0}}{W_0 V_{gt0} - \frac{1}{2}\triangle W V_{gt}} \times \frac{W_0 V_{gt0} + \frac{1}{2}\triangle W V_{gt}}{2W_0 V_{gt0}} \\
&= \frac{1 + \frac{\triangle W V_{gt}}{2W_0 V_{gt0}}}{1 - \frac{\triangle W V_{gt}}{2W_0 V_{gt0}}} = \frac{1+x}{1-x} \quad \text{with} \quad (x = \frac{\triangle W V_{gt}}{2W_0 V_{gt0}})
\end{aligned} \tag{2.12}$$

In this equation, $W_{1,2}$ are the effective widths of two branches of the parallel differential pair, which changes as a function of the gate control voltage. W_0 is equal to $(W_1 + W_2)/2$. Compared with a single differential pair, x is much more complicated and no longer a linear function of the gain control voltage. This, however, can be dealt with by generating an appropriate non-linear time-varying control voltage, e.g. using a digital to analog converter (DAC).

In summary, a TGC network with the parallel differential pair has a better noise and headroom performance, but a more complicated gate control voltage is needed.

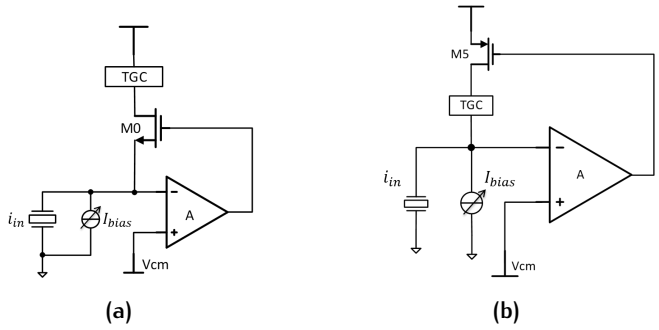


Figure 2.9: The topologies of the loop amplifier

2.3 THE LOOP AMPLIFIER

The echo signal from the transducer is a current signal. To receive the echo signal and transfer it to the TGC circuit, another feedback network is introduced as shown in figure 2.9a. In this feedback network, a loop amplifier with large g_m and small input impedance can reduce the input referred noise. In addition, a reference input voltage V_{cm} of the loop amplifier is introduced as a virtual ground to bias the input echo signal, because the inverting input assumes the same absolute potential as the non-inverting input of reference within a linear op amp application.

However, in this circuit, transistor M_0 still sees the whole dynamic range of the echo signal. Additionally, there is another similar feedback network in the TGC circuit. The input feedback network and the TGC network can be further merged. As shown in figure 2.9b, the input feedback network and the TGC block share the same loop amplifier. Therefore, except transferring the echo signal to the TGC circuit, this loop amplifier can also ensure the parallel differential pair works in saturation mode and obtain a certain small signal gain as TGC function.

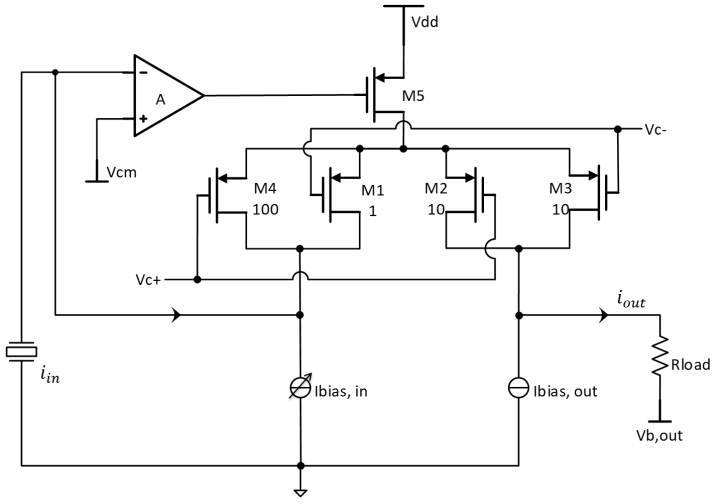


Figure 2.10: The architecture of the loop amplifier and the TGC circuit

The whole architecture of the loop amplifier and the TGC circuit is shown in figure 2.10.

2.4 VARIABLE DC CURRENT SOURCE

In figure 2.10, to receive the AC current from the transducer, a DC bias current source is necessary to bias the input of the TGC network. This DC bias current source also introduces noise. If a transistor is used as a current source, according to equation 2.8, it contributes as much noise as the input transistor of the TGC circuit. Meanwhile, according to equation 2.10, the DC bias current also affects the g_m of the input transistor of TGC. It is the same story as the TGC network with a differential pair, the worst case of noise problem is the high gain setting case when the input echo signal is 1 μA peak to peak. Therefore, to reduce the input noise, small DC bias current is needed. However, to bias the large echo signal current in the low gain setting case, a large bias current is needed. In summary, a variable DC current source is needed to bias the input of TGC.

At the output of the TGC, another DC bias current source is also needed. The bias current source at the output should provide a bias current equal to that of the output branch of the current-steering differential pair, so that only the AC signal current from the TGC flows through the load resistor. If the output DC current source of TGC is constant, the value of input bias current source should change exponentially as a function of time.

2.4.1 Biasing using parallel transistors

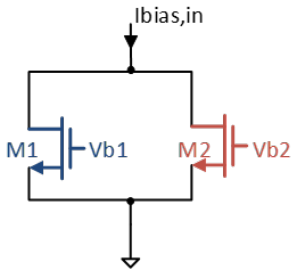
There are many approaches to implement the DC bias current source. For the output bias current source, the easiest way to build this source is to place a constant 10 μA current source by one transistor. The drain current of this transistor can be copied by a current mirror from a reference current source.

For the input variable bias current source, its drain current changes from 1 μA to 100 μA exponentially. There is also a trade-off between noise and headroom as same as the trade-off in the TGC circuit. Apparently, one transistor cannot handle this huge dynamic range with low noise behaviour. A similar way as the current-steering differential pair in the TGC network can be used to design the variable current source. In figure 2.11a, two transistors form the current source. In this circuit, transistor M_1 is a transistor with a high W/L ratio. On the contrary, transistor M_2 is a transistor with a low W/L ratio. The gate voltages of these two transistors behave as shown in figure 2.11b. T_1 and T_2 is the starting moment and the ending moment of the RX period respectively.

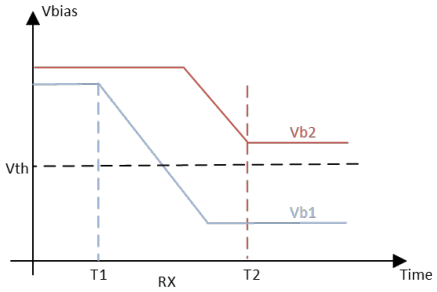
In the beginning, the amplitude of the echo signal is large, which means the bias current should be 100 μA. At that time, the gate voltages of both M_1 and M_2 are high, which can turn on these two transistors. Transistor M_1 with a high W/L ratio has enough headroom to handle the large-signal current.

With the decrease of the amplitude of the echo signal, the gate voltage V_{b1} of M_1 is also decreasing. In this process, the drain current I_{d1} of M_1 is reducing, so the total bias current is also decreasing. Meanwhile, the drain current I_{d2} of M_2 remains the same. When V_{b1} is much lower than V_{th} and M_1 is completely turning off, the gate voltage V_{b2} of M_2 begins to decrease. V_{b2} keeps decreasing until the drain current, also the total bias current, is equal to 1 μA at T_2.

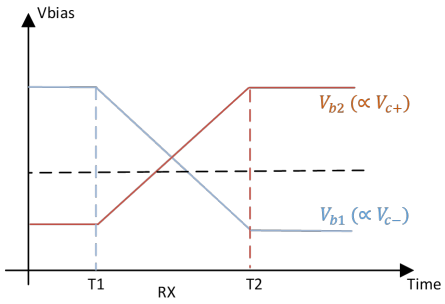
In this circuit, when the echo signal is small, big transistor M_1 is off. Only small transistor M_2 is on, so the total effective g_m of this current source is small. In this high gain setting case, the noise of the current source is small,



(a) Input bias current source



(b) Gate voltage of the input bias current source



(c) New Gate control voltage

Figure 2.11: Parallel transistors as bias current source

which can offer a good SNR performance. When the echo signal is large, both M_1 and M_2 are on, so this current source can offer a large amount of current. Even though in the low gain setting case, the noise behaviour is bad, but it is still enough for SNR. The gate voltage V_{b1} can be generated from a current source by a current-mirror fashion, using a diode-connected transistor. The drain current of that current source changes exponentially with time. The other gate voltage V_{b2} can be generated by V_{b1}, using a level shift block, e.g., a source follower. Meanwhile, the V_{b2} has to be limited to a certain voltage by a voltage limiting circuit, in order to prevent M_2 from going into triode region.

However, there are still some problems with this topology. The main problem is the mismatch between the bias current source and the TGC circuit, due to the use of different control voltages. If the DC bias current ratio between input branch and output branch is not equal to the ratio between the effective width of input branch and output branch in the TGC circuit, the final gain of TGC will be affected. It is hard to design the gate voltages of the bias current source, such that the right current is obtained, since these voltages are not naturally linked to the control voltage of the TGC circuit. In addition, because there is already a gate control voltage for the TGC circuit, generating another gate control voltage is not an efficient solution for circuit designing.

To improve the performance of input bias current source, the same control voltages as the TGC circuit can be used as $V_{b1,2}$, as shown in figure 2.11c. At low bias current levels, only transistor M_2 with a small W/L ratio is active, providing low noise, while at high bias current levels, transistor M_1 with high W/L is active, providing the required current within the available headroom.

2.4.2 Replica circuit

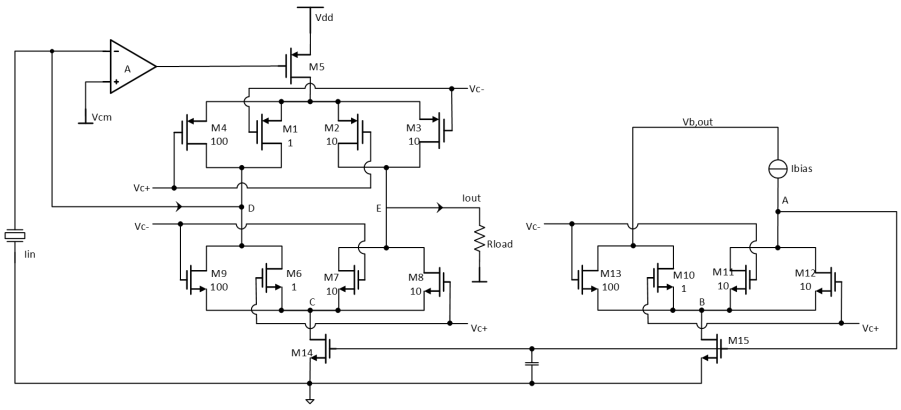


Figure 2.12: Architecture of the TGCLNA

For a further improvement, to make the circuit matched well and work efficiently, a replica bias current source circuit as shown in figure 2.12 will be used in this architecture. This replica circuit consists of transistors M_6 to M_{15}. The transistors M_6, M_7, M_8, M_9 and M_{14} in the left part of the replica circuit are symmetrical to the TGC circuit. The gate of transistor M_{14} is driven by the right part of the replica circuit. The current from I_{bias} is equal to 10 μA.

The bias circuit is a complementary NMOS version of the TGC circuit. As a result, the tail current I_{d14} splits between the feedback branch and the output branch in the same way as the signal current. The replica bias circuit on the right employs a feedback loop to bias the tail current in such a way that the current provided to the output is constant. In consequence, the bias current provided to the feedback branch is the desired $\frac{1-x}{1+x} I_{bias}$.

In this topology, the noise and headroom trade-off problem can be solved by the parallel differential pair. The replica bias current circuit can use the same control gate voltage in the TGC circuit. The same topology and control voltage can achieve a good match between the current ratio of the bias currents and the effective width ratio of the TGC circuit. Therefore, the topology of a replica bias current circuit is chosen to build the bias current sources.

3 CIRCUIT DESIGN

3.1 THE LOOP AMPLIFIER

From figure 2.10, the loop amplifier should handle 40 dB dynamic range of the input echo signal, while it also can offer a low input impedance in the high gain setting case to reduce the noise.

3.1.1 Noise of the loop amplifier

First of all, noise is the main concern of designing the loop amplifier. The input-referred voltage noise of the loop amplifier is shown in figure 3.1. The transducer can be modelled as a resonator in parallel with a 18 pF capacitance. At 7.5 MHz frequency, the effective impedance of this transducer can be calculated as:

$$Z_{in} = \left| \frac{1}{j2\pi fC} \right| = \left| \frac{1}{j2\pi 7.5M \cdot 18p} \right| \approx 1180\Omega \tag{3.1}$$

The input-referred voltage noise of the loop amplifier can be transferred to an equivalent input-referred current noise:

$$I_{n,in,opamp} = \frac{V_{n,in,opamp}}{Z_{in}} \tag{3.2}$$

As mentioned in table 1.1, the total input noise from the loop amplifier, feedback network and bias current source should be less than 1 pA$\sqrt{\text{Hz}}$ in the high gain setting case. So, the noise from the loop amplifier should be

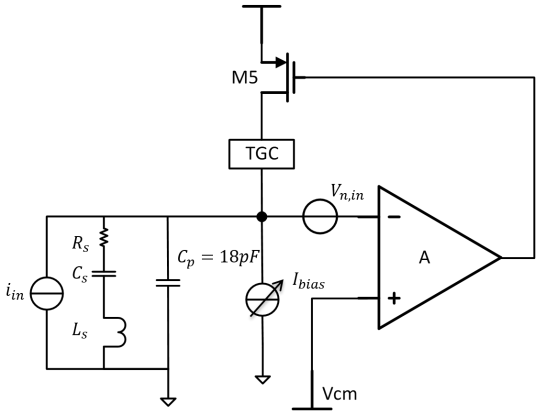


Figure 3.1: Input voltage noise of the loop amplifier

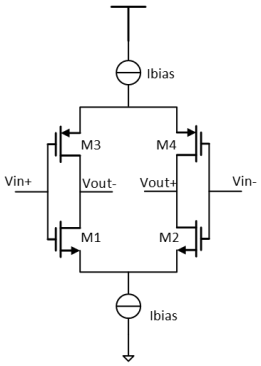


Figure 3.2: The first g_m stage of the loop amplifier

smaller than 1 pA$\sqrt{\text{Hz}}$. The input-referred noise of the loop amplifier can be expressed by the function of the effective input G_m of the loop amplifier:

$$V_{n,in,op-amp} = \sqrt{\frac{2}{3}\frac{4kT}{G_m}} \tag{3.3}$$

From equation 3.3, the input referred noise is proportional to the effective input G_m of the loop amplifier. A large G_m is needed to reduce the noise of the loop amplifier. Therefore, a current-reuse amplifier is chosen as the first stage of the loop amplifier, with a high effective input G_m as shown in figure 3.2. In this topology, the effective input G_m can be seen as the sum of $g_{m1,2}$ and $g_{m3,4}$. In order to obtain a large effective input G_m, a large bias current of 8.5 mA at the highest gain and high W/L ratio are used to bias transistors $M_{1,2,3,4}$ in weak inversion.

3.1.2 Bandwidth and stability

After discussing the noise problem, the bandwidth of the loop amplifier should be concerned. The echo signal frequency is 7.5 MHz. In order to pass the signal, the circuit needs at least 15 MHz for the -3 dB closed-loop bandwidth.

To analyze the stability and the bandwidth of the loop amplifier, first of all, the loop shown by the blue arrow in figure 3.3 is considered. For this loop, the capacitance C_p of the transducer is 18 pF. This capacitance will introduce a pole to the loop, which may be the dominant pole of the circuit. To make the problem simple, it can be assumed that the poles from the TGC circuit and the loop amplifier are the nondominant poles, i.e., far beyond the unity gain frequency of the loop. If the DC gain of the loop amplifier from node a to node b is A_{op-amp}, the transconductance of M_5 is $g_{m,5}$ and the current gain from node c to node a is the factor $(1-x)/2$, then the open-loop gain can be expressed as:

$$A_{OL}(\omega) = \frac{A_{op-amp} g_{m5}(1-x)/2}{j\omega C_p} \tag{3.4}$$

For the highest gain setting case, the input bias current $I_{d,1}$ is 1 μA and the output bias current is constant as 10 μA, so the tail current $I_{d,5}$ is the sum of the input bias current and the output bias current, which is equal to 11 μA. In this case, as the result derived from equation 2.1, the current gain

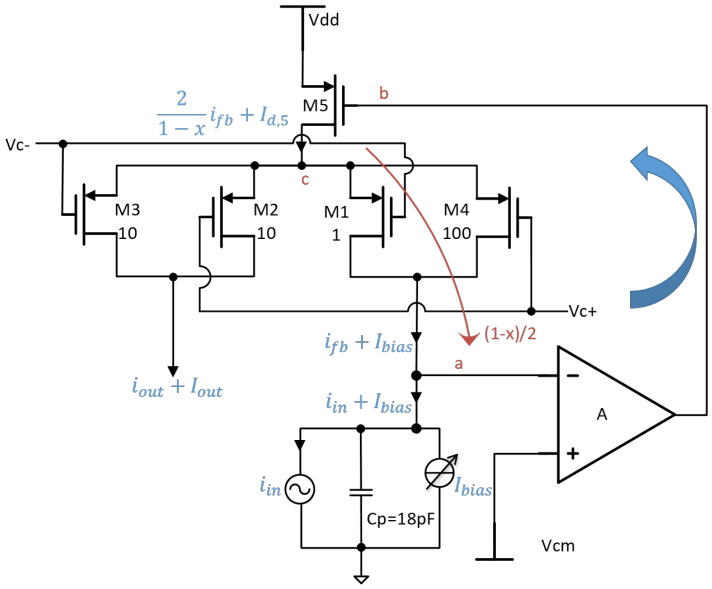
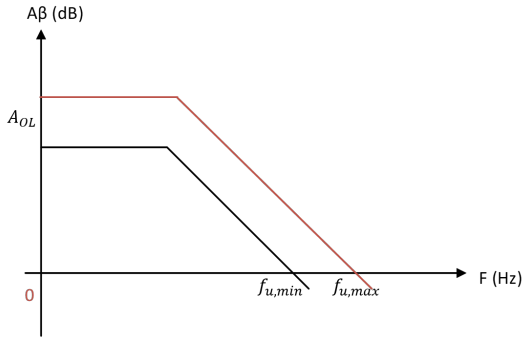
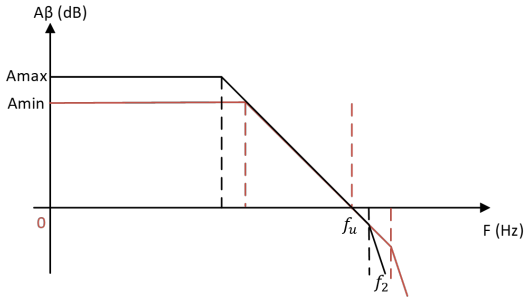


Figure 3.3: The loop of the TGC feedback network



(a) Bode plot when the gain of the loop amplifier is constant



(b) Bode plot when the gain of the loop amplifier is variable

Figure 3.4: Bode plot of the open loop

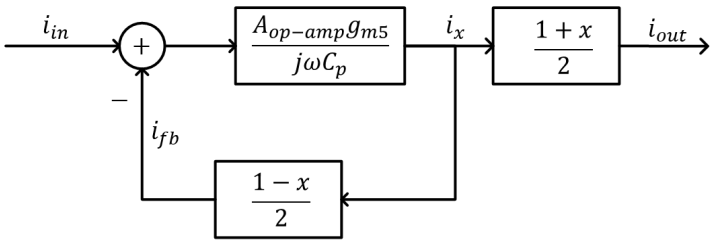


Figure 3.5: System of the closed loop

$\frac{1-x}{2}$ from node c to node a is equal to the drain current ratio between M_1 and M_5, which is equal to $\frac{1}{11}$.

In the lowest gain setting case, the input bias current $I_{d,4}$ is 100 μA and the output bias current remains 10 μA, so the tail current $I_{d,5}$ is 110 μA. Now, the current gain α is equal to $\frac{10}{11}$. If M_5 works in the weak inversion region, $g_{m,5}$ is proportional to $I_{d,5}$, which changes from 11 μA to 110 μA. According to figure 2.12, $I_{d,5}$ is proportional to $\frac{2}{1+x}$. Since both $\frac{1-x}{2}$ and $\frac{2}{1+x}$ vary by 20 dB. If the gain of the loop amplifier is constant, the unity gain frequency of the loop would vary by two decades. This is illustrated in the bode plot shown in figure 3.4a. The gain-bandwidth product of this open loop can be expressed as:

$$\begin{aligned} GBW = f_u &= \frac{A_{op-amp}g_{m5}(1-x)/2}{2\pi C_p} = \frac{A_{op-amp}\frac{I_{d5}}{nV_T}(1-x)/2}{2\pi C_p} \\ &= \frac{A_{op-amp}\frac{2/(1+x)I_{bias,\ output}}{nV_T}(1-x)/2}{2\pi C_p} \quad with \quad V_T = \frac{kT}{c} \end{aligned} \tag{3.5}$$

The signal path in close loop is shown in figure 3.5. In this circuit, the TGC circuit just plays a role as an attenuator, which will not affect the -3dB bandwidth. Therefore, the closed-loop transfer function can be derived as:

$$\begin{aligned} A_{CL}(\omega) = \frac{i_{out}}{i_{in}} &= \frac{\frac{1+x}{2}i_x}{i_{in}} = \frac{\frac{1+x}{2}(i_{in}-i_{fb})\frac{2}{1-x}A_{OL}(\omega)}{i_{in}} \\ &= \frac{\frac{1+x}{2}(i_{in}-\frac{A_{OL}(\omega)}{A_{OL}(\omega)+1}i_{in})\frac{2}{1-x}A_{OL}(\omega)}{i_{in}} = \frac{A_{OL}(\omega)}{A_{OL}(\omega)+1}\frac{1+x}{1-x} \end{aligned} \tag{3.6}$$

From this equation, the $-$3dB closed-loop bandwidth is located where $A_{OL}(\omega)$ is equal to 1. So, the unity gain frequency f_u of open loop is also the $-$3dB closed-loop bandwidth of the circuit, which means that f_u should be larger than 15 MHz. Actually, the requirement of the $-$3 dB closed-loop bandwidth is that $f_{u,min}$ should be larger than 15 MHz. If $f_{u,min}$ is assumed as 15 MHz, because of the two decades variation, $f_{u,max}$ would be equal to 1.5 GHz, corresponding to a much high closed-loop bandwidth than required. In previous paragraphs, the poles from the loop amplifier are not taken into account. Because of the requirement of stability, the $-$3dB frequencies of the poles from the loop amplifier should at least larger than $f_{u,max}$. To make a simple estimation, if the DC gain A_{op-amp} of the loop amplifier is constant as 100, the GBW of this amplifier is at least 150 GHz. This shows that a design based on a loop amplifier with constant gain would not be efficient.

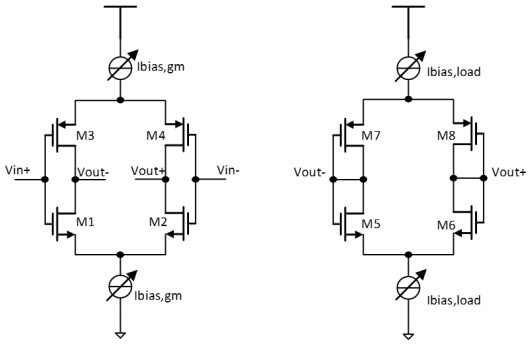


Figure 3.6: The architecture of the first stage of the loop amplifier

Instead of keeping the gain of the loop amplifier constant, a VGA can be used as the loop amplifier. If the gain of the loop amplifier is varied such that the open-loop GBW is kept constant and slightly larger than 15 MHz, the requirement of the frequency of the nondominant poles is quite relaxed. From equation 3.5, if the GBW is constant, then A_{op-amp} should be proportional to $\frac{1+x}{1-x}$.

This is illustrated in the bode plot shown in figure 3.4b. If the GBW of the loop amplifier is constant, when the gain of the loop amplifier is changing, as the second pole f_2 of the whole loop, the -3dB bandwidth of this amplifier is also changing, which will also affect the stability of the loop. In the highest gain setting case of the loop amplifier, it is the worst case of stability, because the -3dB frequency of the loop amplifier is the smallest.

In summary, if a VGA is used as the loop amplifier to compensate the loop gain and keep the GBW and closed loop bandwidth constant, the highest gain setting case will be the worst case for noise and stability.

3.1.3 The first stage of the loop amplifier

The topology of the first stage of the loop amplifier is shown in figure 3.6. As section3.1.1 mentioned, a current-reuse amplifier is chosen as a input G_m stage. Meanwhile, four diode-connected transistors are used as the load of the amplifier. If the values of $g_{m,5,6,7,8}$ are similar, the gain of this stage can be expressed as:

$$A_1 = \frac{g_{m1,3} + g_{m2,4}}{g_{m5,7} + g_{m6,8}} \tag{3.7}$$

In addition, if all the transistors are in the weak inversion region, their g_m are proportional to their tail currents I_{bias,g_m} or $I_{bias,load}$. If I_{bias,g_m} and $I_{bias,load}$ are proportional to $1+x$ and $1-x$ respectively, then the total gain of this stage is proportional to $\frac{1+x}{1-x}$. At the highest closed-loop gain, I_{bias,g_m} is in the largest case and $I_{bias,load}$ is in the smallest case. In this case, the input referred noise of the loop amplifier is the smallest due to the high effective input G_m. The gain of this stage is also large because of the high effective input G_m and the low $g_{m,load}$. In contrast, at the lowest closed-loop gain, when the input echo signal is large, the gain of this loop amplifier is low due to the low effective input G_m and the high $g_{m,load}$.

The whole circuit of the first stage is shown in figure 3.7. The circuit in the right is the $g_{m,load}$ stage. The circuit on the middle is the G_m stage. In order to create a high effective G_m, large size with high W/L ratio transistors are

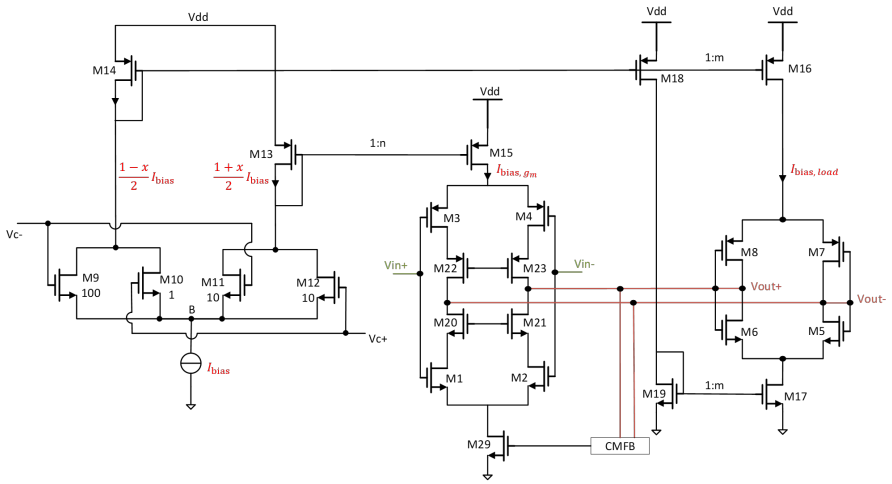


Figure 3.7: The first stage of the loop amplifier

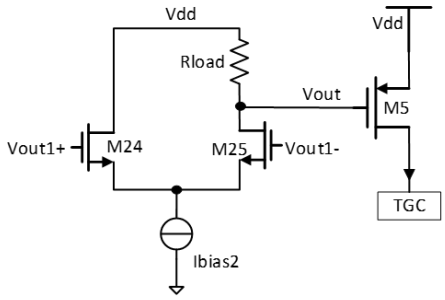


Figure 3.8: The second stage of the op-amp

chosen as $M_{1,2,3,4}$. As a drawback, these transistors are associated with big parasitic capacitance. Their C_{ds} are directly connected between input and output. Therefore, transistors $M_{20,21,22,23}$ are used as cascodes to reduce the effect of parasitic capacitances. The tail current on the bottom is generated by common-mode feedback, which will be discussed in section 3.1.5.

The circuit in the left is the bias circuit to generate the tail currents I_{bias,g_m} and $I_{bias,load}$. As shown in figure 3.7, a control circuit $M_{9,10,11,12}$ similar to the TGC circuit is used to generate the $1+x$ and $1-x$ function. If the tail current I_{bias} of the bias circuit is constant, the current on the left branch is proportional to $(1-x)/2$, which can be used as the tail current $I_{bias,load}$ of the $g_{m,load}$ stage. Meanwhile, the current on the right branch is proportional to $(1+x)/2$, which can be used as the tail current I_{bias,g_m} of the G_m stage.

3.1.4 The second stage of the loop amplifier

As shown in figure 3.3, this loop amplifier is a differential input, single-ended output amplifier. Moreover, one amplifier stage can hardly offer enough gain for at least 15 MHz bandwidth. Therefore, a broadband differential input single-ended output amplifier has been added as a second stage as shown in figure 3.8. Because the first stage already offers a high gain, it is not necessary for the gain of the second stage to be high. In this circuit, diode-connected transistor cannot be used as the load of the second stage, which can be seen as a current mirror to drive the gate of M_5. Because the tail current I_{bias2} is constant and the drain current I_{d5} of M_5 is

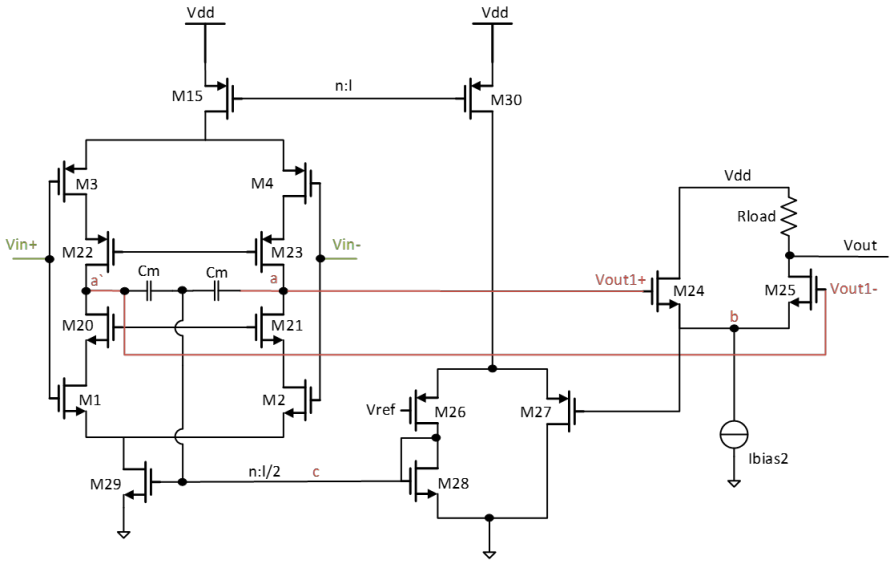


Figure 3.9: The common-mode feedback

variable, the current mirror will be broken due to the variation of I_{d5}. So a differential input, resistance-load topology is used. The gain of the second stage can be expressed as $g_{m24,25}R_{load}$. The $-3dB$ frequency is located at $\frac{1}{2\pi R_{load}C_{gs5}}$. The GBW is $\frac{g_{m24,25}}{2\pi C_{gs5}}$. From these expressions, C_{gs5} is defined by the TGC circuit. $g_{m24,25}$ should be large enough to handle the bandwidth and the gain trade-off. R_{load} should be chosen properly for the gain and DC bias.

3.1.5 Common-mode feedback

The last part of the loop amplifier is the common-mode feedback at the output of the first stage, which is shown in figure 3.9. The common-mode level is sensed from node b in the second stage, which is used to drive the gate of tail current transistor M_{29} in the first G_m stage through an amplifier in the middle part of the circuit. If the loop of this common-mode feedback is analyzed from nodes a, $a^{'}$ to node b, $M_{24,25}$ can be seen as a source follower with gain approximately as 1. The gain from node b to node c is the gain of the common-mode feedback amplifier A_{cm}. The voltage from node c to nodes a, $a^{'}$, is amplified by a common source transistor M_{29} and the common gate transistors $M_{1,2,20,21}$, so the loop gain of the common-mode feedback is high. For stability requirement, the common-mode feedback amplifier should be a low gain broadband amplifier. In this figure, a g_m input and diode-connected load amplifier is used as the common-mode feedback amplifier. $M_{28,29}$ work as a current mirror. To obtain the desired gain-dependent drain current I_{bias,g_m} of M_{29}, the drain current I_{d28} should also be variable. So, the tail current I_{d30} should also be proportional to $1+x$, which can be realized by connecting the gates of M_{30} and M_{15} together. Last but not least, two compensation capacitor C_m are placed between nodes a, $a^{'}$ and node c to stabilized the common-mode feedback loop.

In summary, the whole circuit of the loop amplifier is shown in figure 3.10.

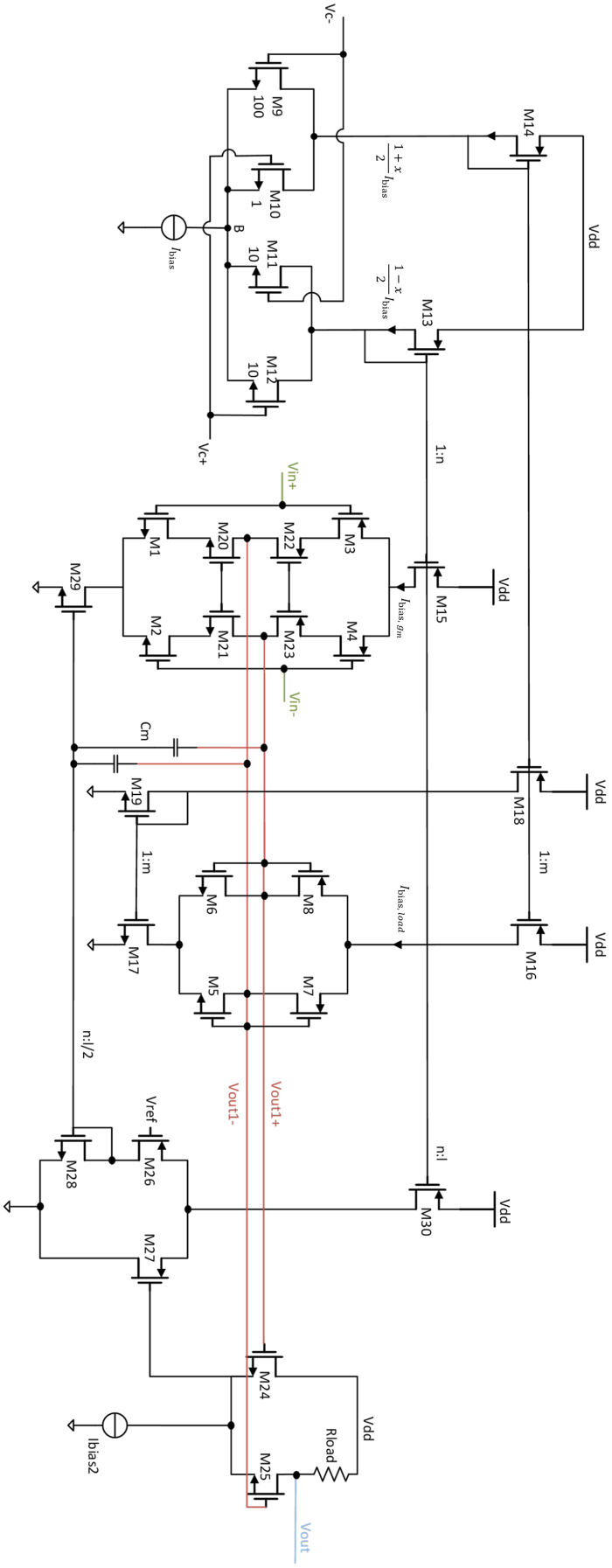


Figure 3.10: The whole circuit of the loop amplifier

3.2 BIAS CURRENT SOURCE

In section 2.4, the circuit of the bias current source is shown in figure 2.12. Compared with the PMOS transistors, the NMOS transistors have worse flicker noise performance in the same size scale. The bias circuit is a complementary NMOS version of the TGC circuit. In order to reduce the flicker noise from the bias current source, the NMOS transistors with long length (2 μm) are used.

3.3 TIME GAIN COMPENSATION FEEDBACK NETWORK

The thermal noise of the PMOS transistors in the TGC circuit is the main concern. So, transistors with a small W/L ratio are needed. In addition, the headroom and the output swing are also another important aspects, which are needed to be considered. Even though a parallel differential pair is used to avoid the problem, if the W/L ratios of the transistors are too small, the transistors will fall into the triode region. Therefore, choosing a proper length and a proper W/L ratio of the transistors is the most important part of the circuit of the TGC circuit.

4 SIMULATION RESULTS

4.1 AC PERFORMANCE

4.1.1 AC response

Figures 4.1 and 4.2 show the AC closed-loop response of the whole current to current LNA with TGC function. There are different curves as shown in the figures as a function of the control voltage (V_c) at the different gain settings. The control voltage the the difference of the gate voltages of the differential pairs ($V_{c+} - V_{c-}$).

The variation of the -3 dB bandwidth as a function of the DC gain is shown in figure 4.3. From the simulation result, the closed-loop bandwidth is always larger than 15 MHz, which is the required bandwidth of the circuit. However, the closed-loop bandwidth is not constant, but varies by a factor of 2, which is different from the expectation. It is reasonable because the TGC circuit, the bias circuit and the loop amplifier use different control circuits. The control circuit of the bias circuit and the loop amplifier are complementary NMOS versions of the TGC circuit. The W/L ratios of the NMOS transistors and the PMOS transistors are also different, which will cause a mismatch among the control circuits of the TGC circuit, the bias circuit and the loop amplifier. Therefore, the closed-loop bandwidth cannot be absolutely constant.

4.1.2 Linearity of TGC

Figure 4.4 shows the log-conformance between the control voltage and the DC gain of the TGC. Indeed, this TGC amplifier with a parallel differential pair does not have a linear-in-dB characteristic. However, this is not really

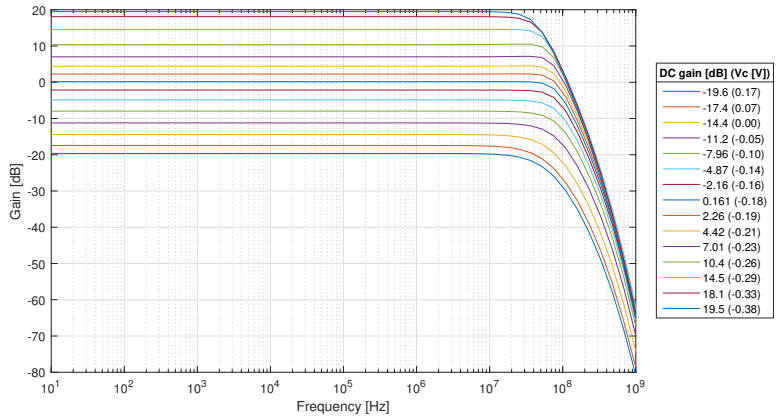


Figure 4.1: AC gain of the TGCLNA as a function of frequency, for different DC gains with corresponding gain-control voltages

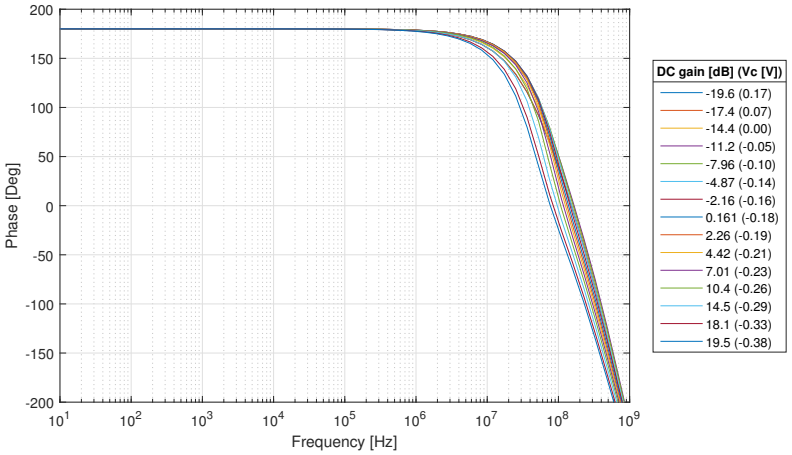


Figure 4.2: AC phase of the TGCLNA as a function of frequency, for different DC gains with corresponding gain-control voltages

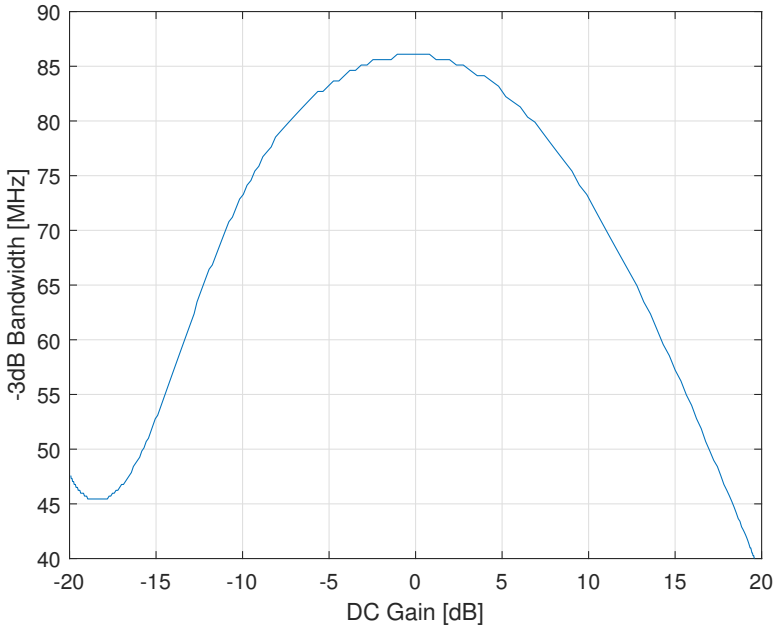


Figure 4.3: -3dB Bandwidth as a function of the DC gain

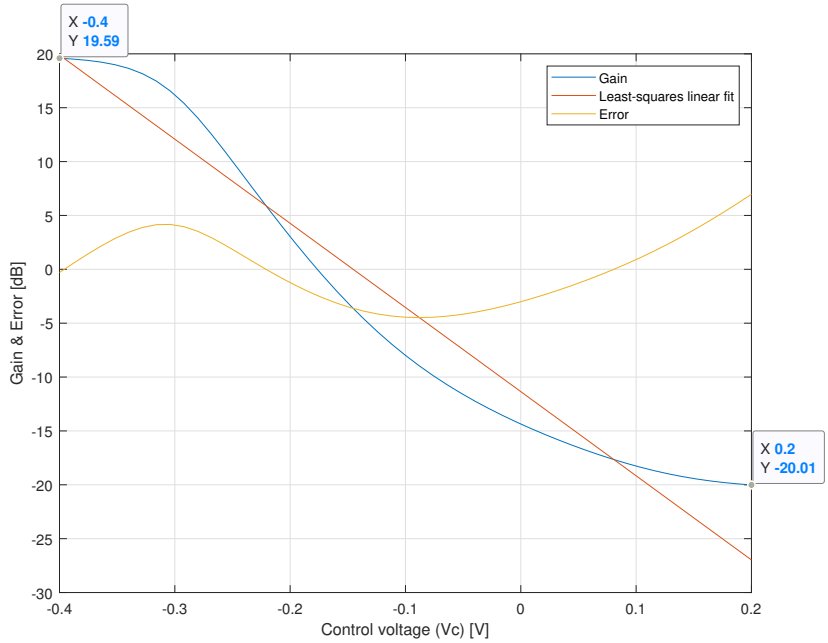


Figure 4.4: the log-conformance between the control voltages and the DC gain of the TGC

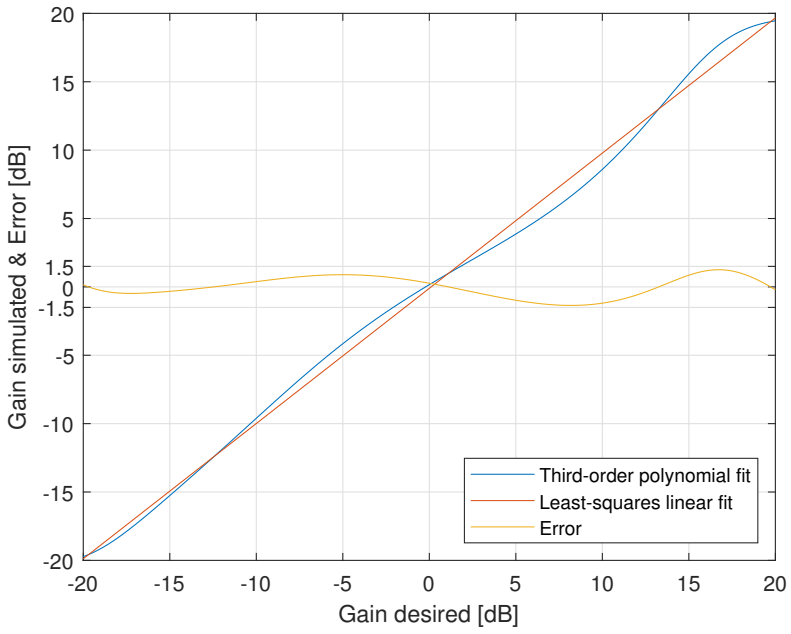


Figure 4.5: Linearity of the third-order polynomial fit

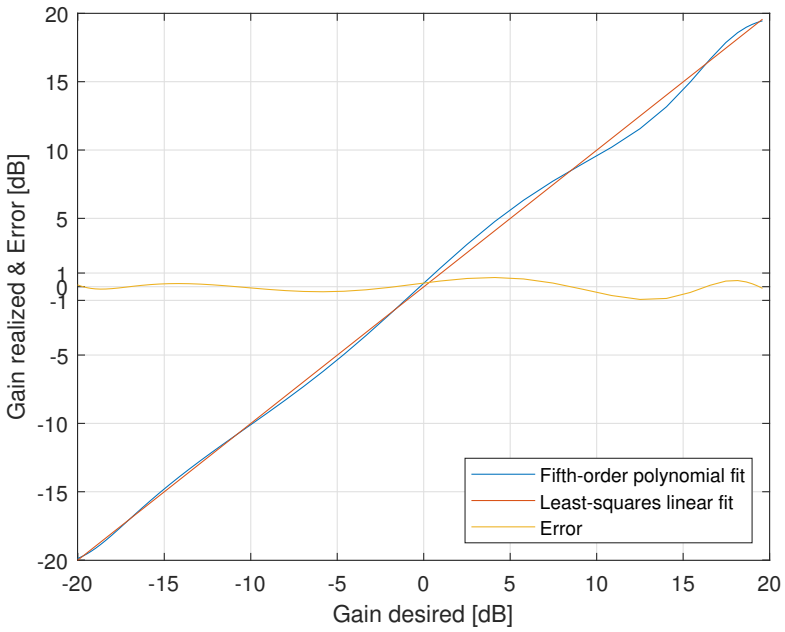


Figure 4.6: Linearity of the fifth-order polynomial fit

a problem, because in a typical imaging system in which many TGCs could share one control-voltage generator, one could implement a DAC that generates the appropriate non-linear gain-control voltage. Figures 4.5 and 4.6 show the third-order and fifth-order polynomial fit of the control voltages. As shown in the figures, the errors after the third-order and fifth-order polynomial fit are less than 1.5 dB and 1 dB respectively. Therefore, it is possible to generate this polynomial control voltage from a linear control factor by a DAC.

4.2 NOISE PERFORMANCE

Figure 4.7 shows the input referred noise as a function of frequency. The central frequency of the input echo signal is 7.5 MHz with a span of 5 MHz, from 5 MHz to 10 MHz. To make it more intuitive, figure 4.8 show the integrated (rms) noise and the integrated (rms) signal across the bandwidth of interest. In this figure, the integrated (rms) noise of the LNA is a bit higher than the transducer's in-band gain independent rms noise at the highest gain setting, because the transducer's spot noise is 0.92 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 7.5 MHz, which is 20% lower than the original target spot niose 1 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ as shown in table 1.1. The noise performance of the TGCLNA still can be improved, so it is not a big problem. In addition, as shown in figure 4.9, the SNR is the worst at the highest gain setting. With the decrease of the DC gain of TGCLNA, the SNR increases.

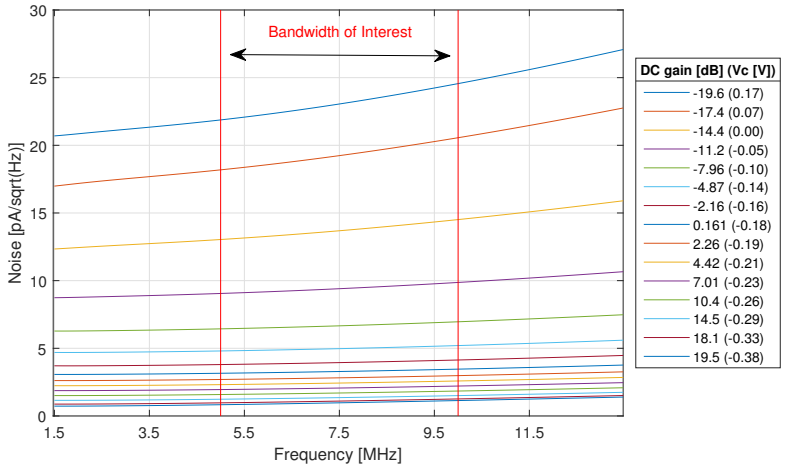


Figure 4.7: Input referred noise as a function of frequency, for different DC gains with corresponding gain-control voltages

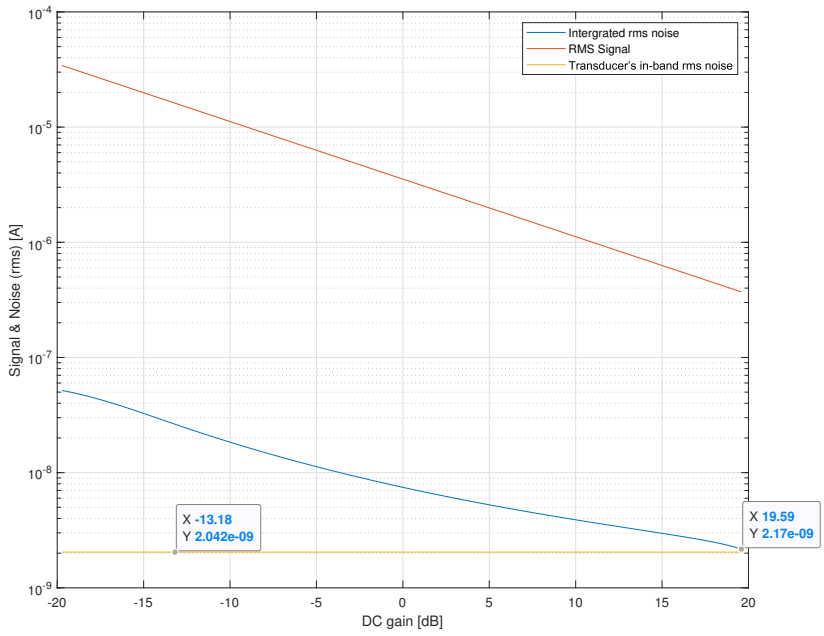


Figure 4.8: Noise and signal

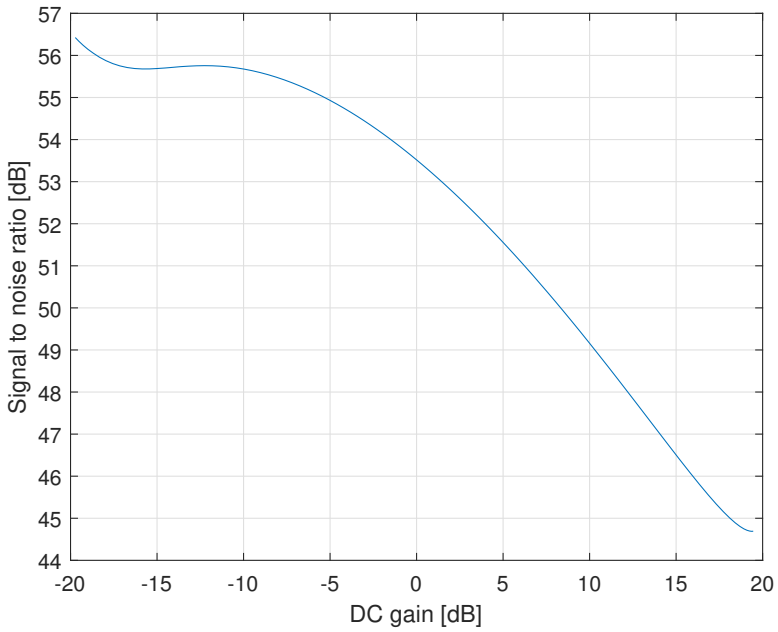


Figure 4.9: Signal to noise ratio of the TGCLNA

4.3 DYNAMIC RANGE AND DISTORTION

As shown in figure 4.10, this amplifier has an input dynamic range of 93 dB, which is compressed into an output dynamic range of 53 dB by means of the 40 dB variable gain.

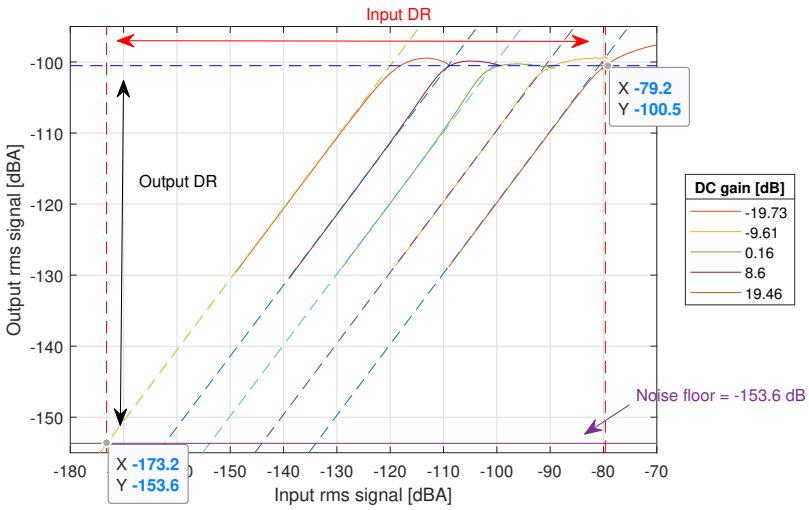


Figure 4.10: Dynamic range of the TGCLNA

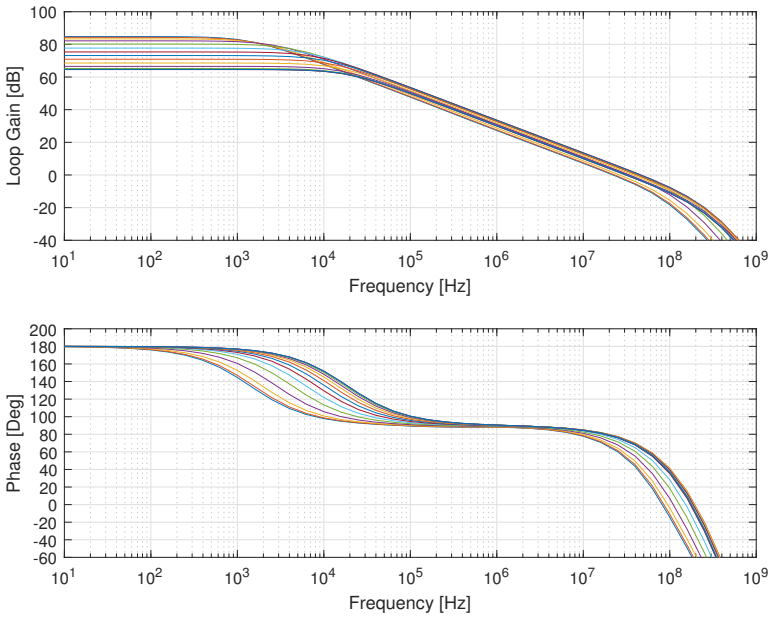


Figure 4.11: Bode plot of the amplifier's open-loop gain

4.4 STABILITY OF THE LOOP AMPLIFIER

4.4.1 Differential feedback loop

Figure 4.11 shows the bode plot of the amplifier's open-loop gain. As mentioned in the last section, because of the mismatch of the control circuits, the GBW of the whole feedback network is not absolutely constant.

Figure 4.12 shows the phase margin and the gain margin of the open loop as a function of the DC gain. Even if the GBW of the feedback network is constant, because of the variation of the second pole, the phase margin and the gain margin will still be variable. Also due to the mismatch of the control circuits and the different saturation region of the transistors, the simulation result is a little bit different from the expectation, which is that the phase margin is the worst at the highest gain setting case. The phase margins are larger than 58°. The gain margins are larger than 13 dB. The differential feedback loop is solidly stable over the full gain range.

4.4.2 Common-mode feedback loop

Figure 4.13 shows the bode plot of the amplifier's open-loop gain of the common-mode feedback loop. The circuit of the common-mode feedback network is shown in figure 3.9. The tail current of the g_m stage is proportional to the tail current of the common-mode feedback amplifier. So the DC gain of the common-mode feedback network is also variable.

Figure 4.14 shows the phase margin and the gain margin of the open loop of the common-mode feedback loop as a function of the DC gain of the TGCLNA. Due to the common-mode open-loop gain has the same monotony as the open-loop gain, the DC open-loop gain of the common-mode feedback loop is the highest, when the TGCLNA is at the highest gain setting. Therefore, the simulation result is in line with expectations, which is that

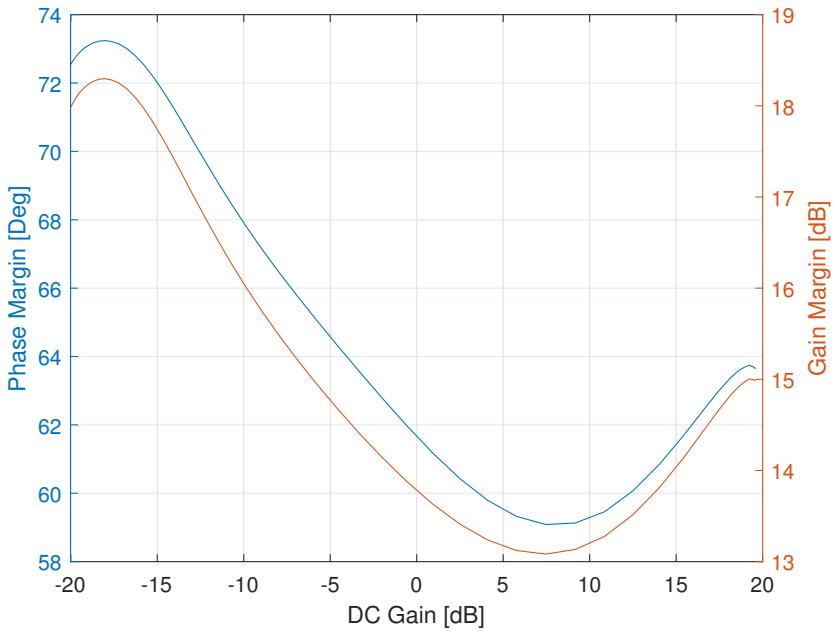


Figure 4.12: Phase margin & gain Margin as a function of the DC gain

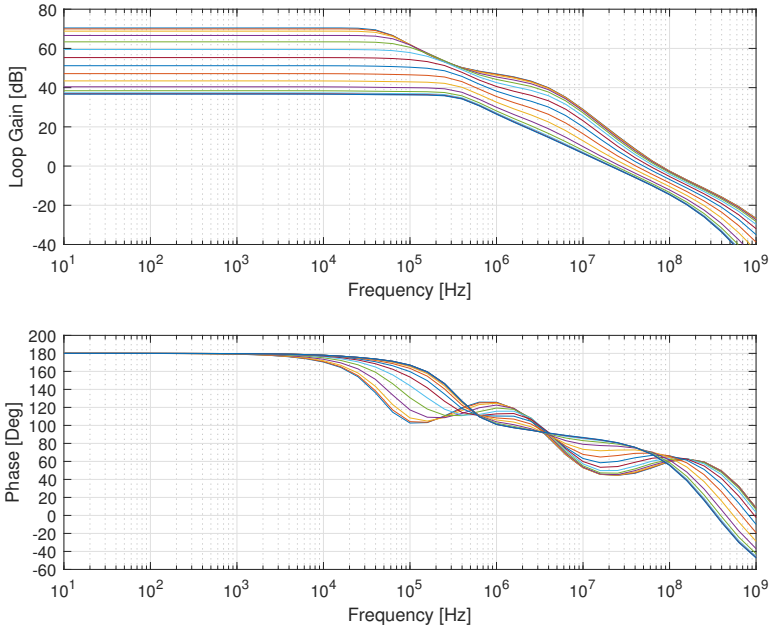


Figure 4.13: Bode plot of the open-loop gain of the common-mode feedback loop

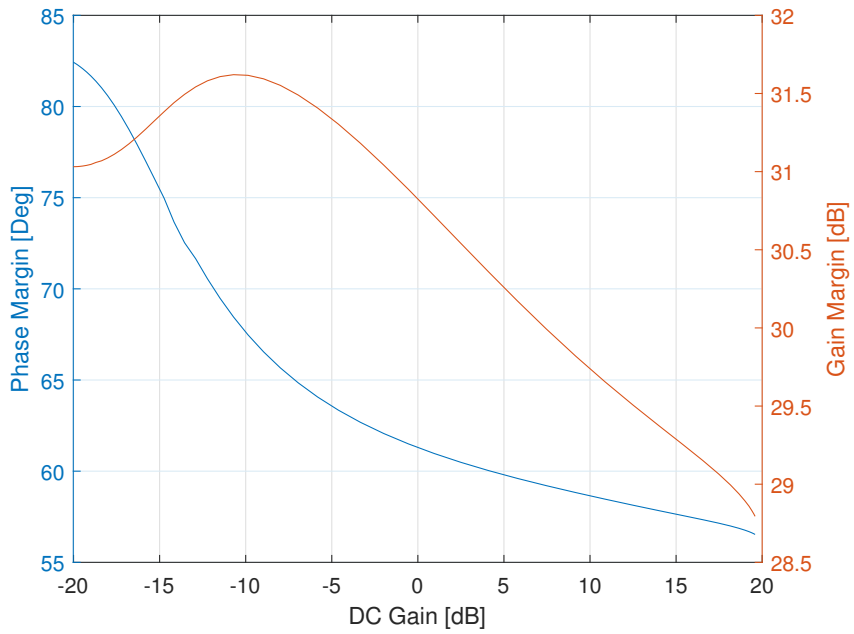


Figure 4.14: Common-mode feedback phase margin & gain margin as a function of the DC gain

the phase margin is the worst, when the DC gain of the TGCLNA is the highest. The phase margins are larger than 55°. The gain margins are larger than 28.5 dB. The differential feedback loop is also stable over the full gain range.

4.5 TRANSIENT RESPONSE

4.5.1 Transient response with sine wave input

Figures 4.15 to 4.18 show the transient response with sine wave input. These figures show a good transient performance with an exponentially-varying input amplitude, showing that the output range is reduced. The amplitude of the output AC signal stays around 10 μA peak to peak. Figure 4.15a shows the input signal as function of time. Figure 4.15b shows the variable bias current and the input signal after being biased as function of time. Figure 4.15c shows the AC output signal as function of time.

4.5.2 Transient response with square wave input

Figures 4.19 to 4.22 show the transient response with square wave input. Figures 4.20 and 4.22 show the large-signal behavior and the small-signal behavior for large pulses at maximum input amplitude of the echo signal and small pulses at minimum input amplitude of the echo signal respectively, by zooming in figure 4.19. During the high gain setting period, there a slight overshoot, because the DC bias point is actually different due to the large input signal at the high gain setting case.

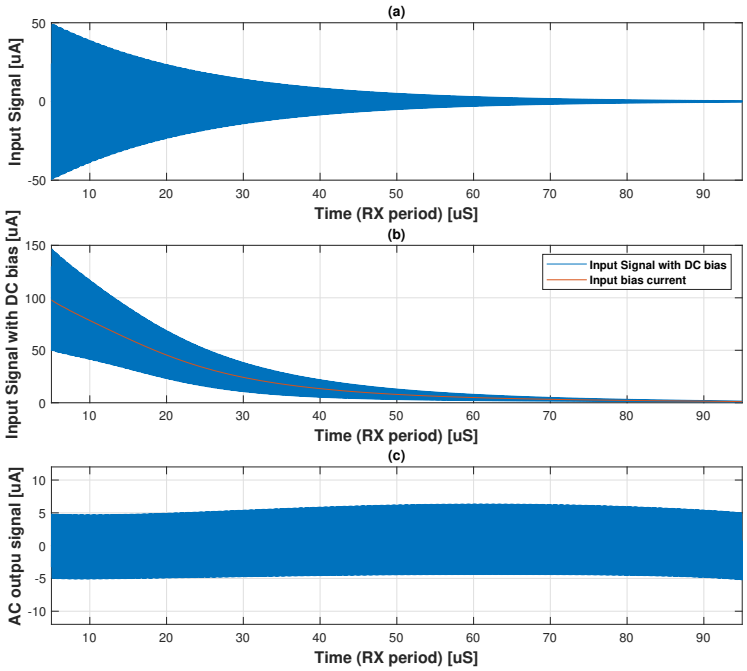


Figure 4.15: Transient response with sine wave input

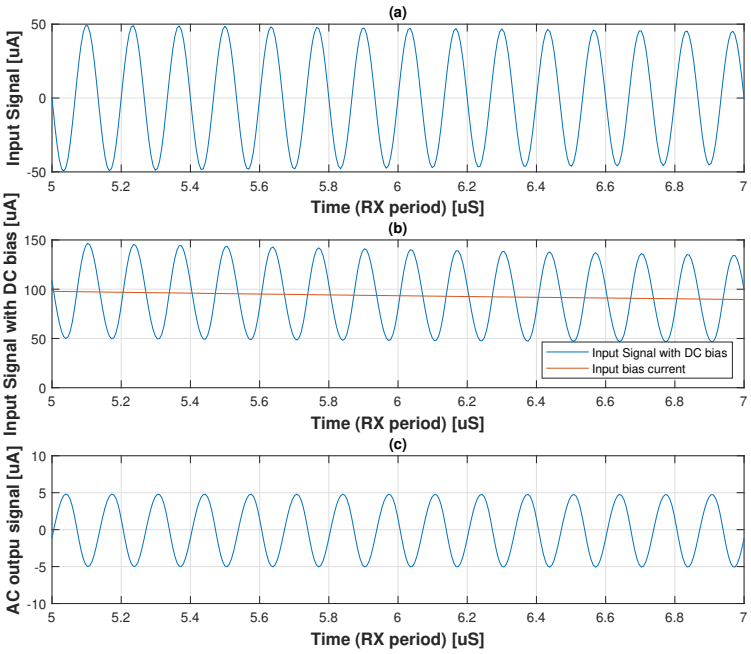


Figure 4.16: Transient response (zoom in) at the lowest gain

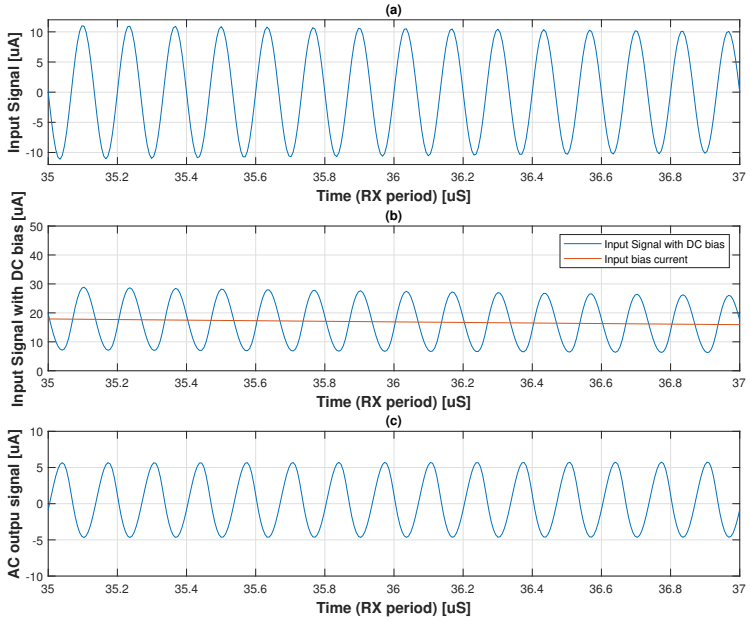


Figure 4.17: Transient response (zoom in) in the medium gain

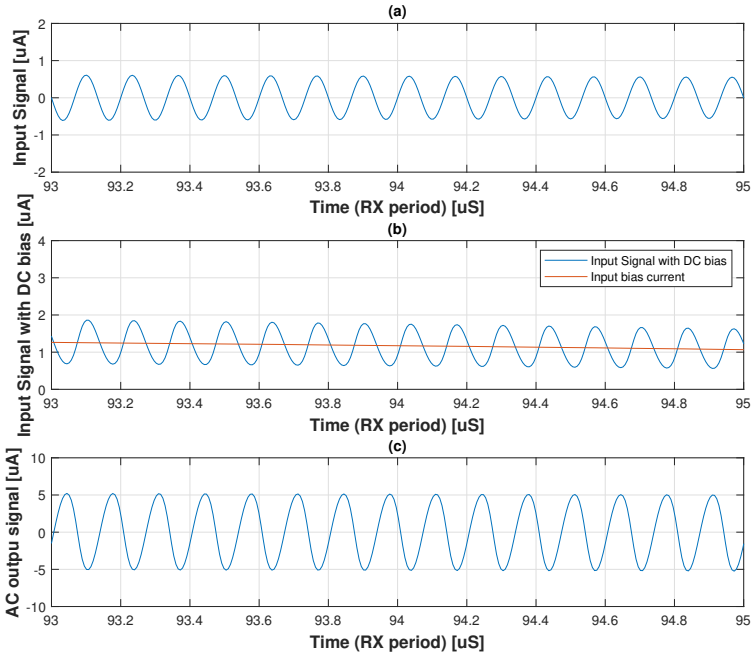


Figure 4.18: Transient response (zoom in) at the highest gain

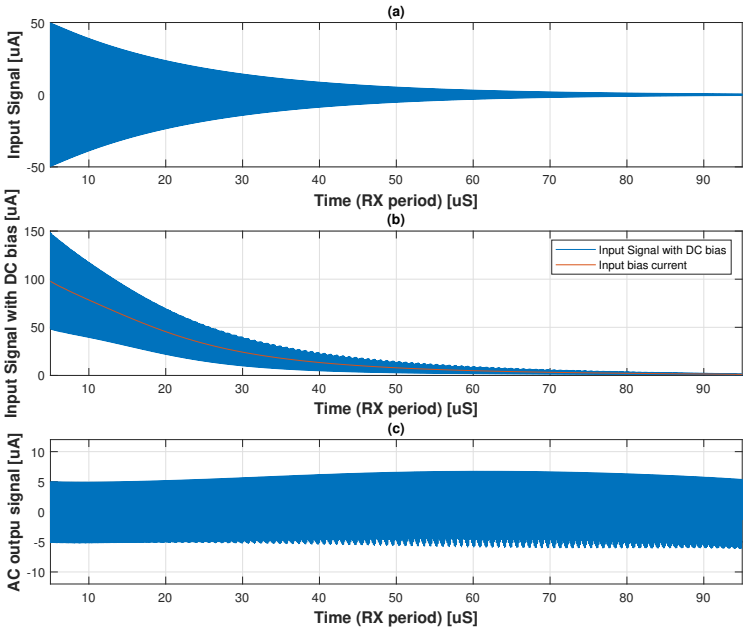


Figure 4.19: Transient response with sine wave input

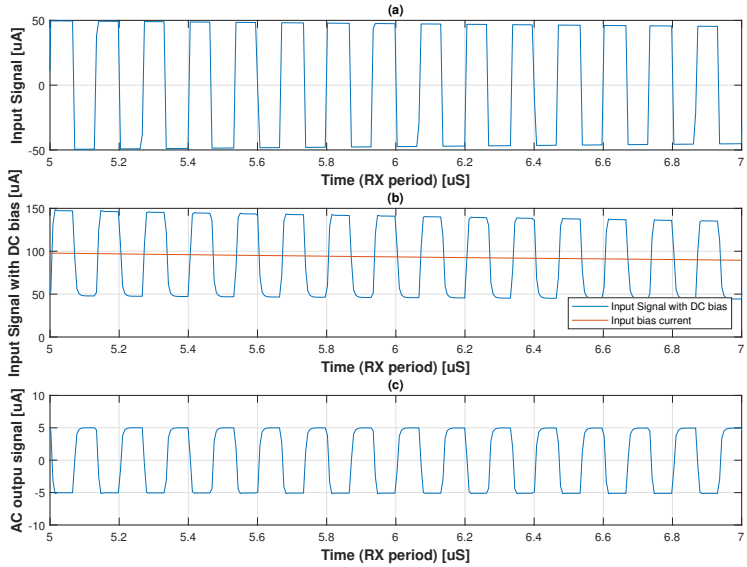


Figure 4.20: Transient response (zoom in) at the lowest gain

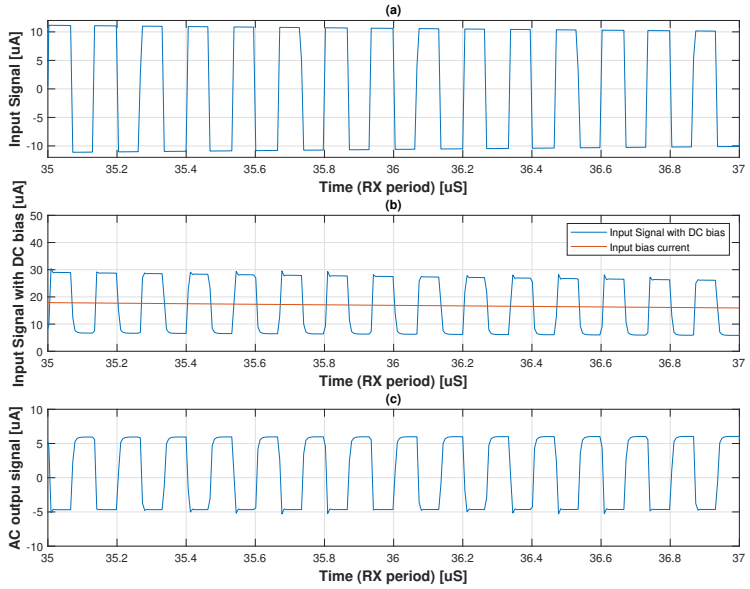


Figure 4.21: Transient response (zoom in) in the medium gain

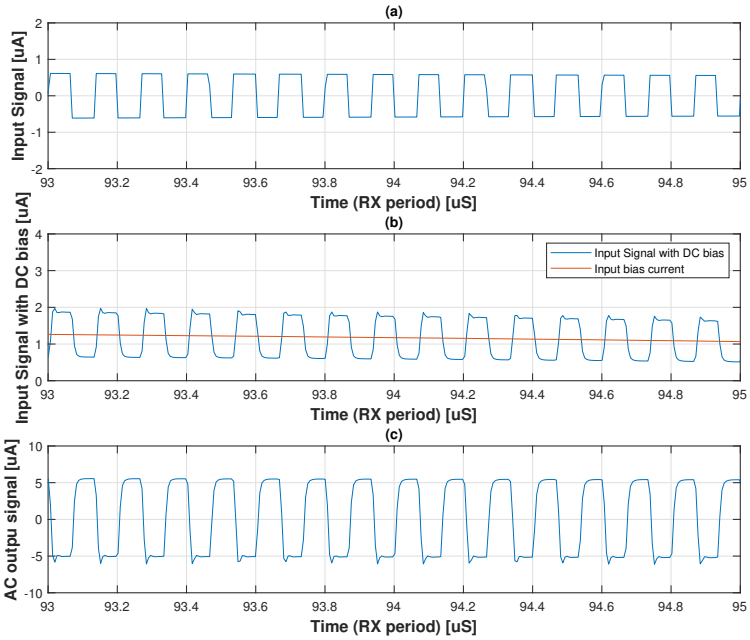


Figure 4.22: Transient response (zoom in) at the highest gain

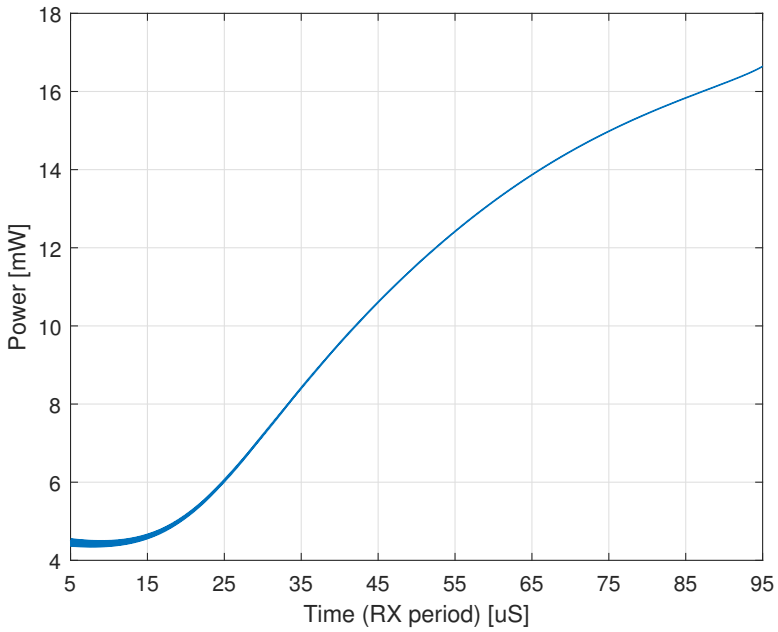


Figure 4.23: Instantaneous power as a function of time

4.6 POWER CONSUMPTION

Figure 4.23 shows the instantaneous power as a function of time in RX period. At the beginning of the RX period associated with low DC gain, the power consumption is low, while at the high gain setting, the power consumption is high. The total average power in the RX period is 10.8 mW.

4.7 AREA

The whole circuit occupies an estimated die area of $320\mu m \times 320\mu m$ with 80% utilization, which is a bit larger than expected The compensation capacitor of the common-mode feedback amplifier, the tail transistors of the input G_m stage of the loop amplifier occupy a large area of the circuit. That is the reason why the area of the TGCLNA is a bit larger than expected. These aspects can be improved in the future.

5 CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

The goal of this thesis was to create a low-noise amplifier for ultrasound imaging with continuous time-gain compensation.

To realize the TGC function, a rational function is used to approximate the exponential function. This rational function has been implemented by a feedback network with a current-steering differential pair. Because of the large dynamic range of the input echo signal, a single differential pair cannot receive the input echo signal with a low-noise performance and available headroom over the full gain range. So, to handle the problem of the noise and the headroom trade-off, a parallel differential pair is used as the current-steering differential pair, instead of a single differential pair.

To realize the DC bias current source, a replica circuit as a complementary NMOS version of the TGC circuit is used. This bias circuit provides the required variable bias current within the available headroom and sufficient SNR.

To realize the loop amplifier in the feedback network, a differential input single-ended output variable gain amplifier with two gain stages is used. The first stage is a differential input differential output variable gain amplifier, using a current-reuse amplifier as the effective input G_m and four diode-connected transistors as the load. The gain is of the amplifier is controlled by changing the tail currents of the G_m stage and the load stage. The second stage is a differential input single-ended output fixed gain amplifier, using a differential NMOS pair as the input and a resistor as the load. There is a common-mode feedback network in this amplifier. Another variable gain amplifier is used as the common-mode feedback amplifier. The loop amplifier offers a wide bandwidth within sufficient SNR.

The table shows the performance of the circuit compared with the prior art. Direct comparison of the performances, e.g. power efficiency, is dif-

Table 5.1: Performance summary and comparison with prior art

Ref.	[17]	[18]	[19]	**This work**
Process	0.18 μm HV	0.18 μm HV	0.18 μm HV	0.18 μm BCD
Center frequency	13 MHz	5 MHz	20 MHz	7.5 MHz
Bandwidth	16 MHz	10 MHz	40 MHz	40 MHz
Power	9.1 mW	1.4 mW	0.8 mW	10.8 mW
Gain range	12 dB	12 dB	Fixed gain	40 dB
Gain switching	Discrete	Discrete	Fixed gain	Continuous
Input capacitance	0.7 pF	2 pF	0.09 pF	18 pF
Input Noise at center frequency	3.0 pA/$\sqrt{\text{Hz}}$	0.41 pA/$\sqrt{\text{Hz}}$	0.31 pA/$\sqrt{\text{Hz}}$	0.96 pA/$\sqrt{\text{Hz}}$

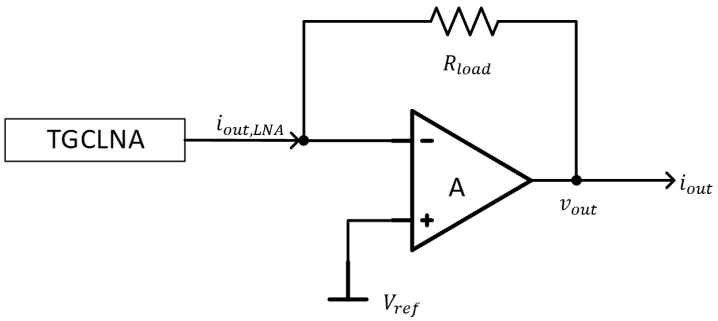


Figure 5.1: Load TIA

ficult because of the different transducer specifications targeted. In contrasts with the prior art, this work provides continuous gain control within the LNA, thus avoiding the imaging artefacts associated with discrete gain steps.

5.2 IMPROVEMENTS AND FUTURE WORK

5.2.1 Improvements

Some aspects of the TGCLNA leave room for improvement. In chapter 4, some results are different from the expectations due to the mismatch of the control circuits. This mismatch can be reduced by changing the W/L ratios of the PMOS and NMOS transistors.

In addition, the closed-loop bandwidth is a bit larger than the required bandwidth, which means that the noise and the power consumption can be optimized by sacrificing some closed-loop bandwidth. Therefore, a better balance can be made among the noise, the closed-loop bandwidth, the stability and the power consumption.

Two compensation capacitors, which occupy a relatively larger area, are used to stabilized the common-mode feedback loop. This can be improved by designing a better common-mode feedback loop of the loop amplifier with a smaller area.

5.2.2 Future work

This TGCLNA still lacks a control circuit to generate the control voltages. A DAC will be designed as a control circuit to generate the appropriate non-linear gain-control voltage, which can be used for the TGCLNAs in all channels.

Additionally, in order to receive the AC output signal from the amplifier, a TIA can be added after the TGCLNA in order to load the signal as shown in figure 5.1.

After the circuit is completed, this TGCLNA will be laid out and taped out. A printed circuit board (PCB) of test bench will be designed for measuring the real performance of the circuit.

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COLOPHON

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