A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall sensors

Jiang, Junfeng; Kindt, Wilco J.; Makinwa, Kofi A.A.

DOI
10.1109/JSSC.2014.2319252

Publication date
2014

Document Version
Accepted author manuscript

Published in
IEEE Journal of Solid State Circuits

A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall Sensors

Junfeng Jiang

Electronic Instrumentation Laboratory / DIMES

Delft University of Technology

Delft, the Netherlands

Email: j.jiang-1@tudelft.nl

Wilko J. Kindt

Texas Instruments Holland B.V.

Delft, the Netherlands

Kofi A. A. Makinwa

Electronic Instrumentation Laboratory / DIMES

Delft University of Technology

Delft, the Netherlands

Abstract: This paper presents a new ripple-reduction technique for spinning-current Hall sensors, which obviates the need for low-pass filtering to suppress the ripple caused by up-modulated sensor offset. A continuous-time ripple-free output is achieved by the use of three ripple reduction loops (RRLs), which continuously sense the offset ripple and then use this information to drive a feedback loop that cancels sensor offset before amplification. Since no low-pass filter is involved, the bandwidth of the resulting system can be much higher than the spinning frequency. Moreover, since the front-end no longer has to process sensor offset, the requirements on its dynamic range can be significantly relaxed. A prototype system consisting of a Hall sensor readout system realized in a 0.18um CMOS process was combined with three off-chip RRLs realized with off-chip electronics. At a spinning frequency of 1kHz, the RRLs reduce the offset ripple by more than 40 dB to about 10 μT, while also achieving low offset (25 μT) and wide bandwidth (over 100 kHz).

Key words: spinning-current, Hall sensor, ripple reduction loop

I. INTRODUCTION

Current sensing is an important part of energy management systems such as battery chargers, motor controllers, power meters etc. The conventional way of measuring current is by measuring the voltage drop across a shunt resistor, as in [1]. However, this inevitably involves some power loss in the shunt and adds extra resistance to the current path. A non-contact current sensor can be realized by using a magnetic

sensor to measure the magnetic field produced by the current flowing through a conductor. This approach avoids the need to insert a component in the current path and can be much more power efficient. However, the minimum detectable current will then be limited by the magnetic sensor's offset and noise in combination with practical constraints on the distance between the sensor and the conductor. In [2], an offset of a few micro-Tesla resulted in a minimum detectable current of few Amperes, while in [3] an offset of 10 μT resulted in a minimum detectable current of 30 mA. A further limitation is the sensor's bandwidth, which must extend to a few MHz [4] [5] in order to detect, for instance, the rapid transients produced by switched-mode power supplies. Wide bandwidth is also required for short-circuit detection [6] [7], where safety considerations may require response time in the order of a few microseconds [8]. Currently, state-of-the-art magnetic sensors implemented in CMOS technology either achieve low offset [9] [10] [3], or wide bandwidth [11], but not both.

Hall sensors are fully compatible with CMOS processing, and so are widely used as integrated magnetic sensors. They are typically realized as an n-well plate with four contacts, which can be modeled as a Wheatstone bridge, as shown in Fig. 1. Due to the Hall Effect, a magnetic field will induce a voltage difference between two opposing contacts when a bias current flows between the other two contacts. This Hall voltage V_{Hall} is proportional to the bias current and to the magnetic field component perpendicular to the plate. Depending on the doping profile and the thickness of the n-well, the sensor's sensitivity will vary between 100 and 400 V/AT [12]-[15]. In other

words, when biased by a 1 mA current, a typical Hall sensor will only generate a few tens of microvolts in the presence of the Earth's magnetic field (< 60 μT [16]). Higher sensitivity can be achieved with the help of magnetic flux concentrators, which can be implemented by depositing a ferromagnetic layer above the sensor in a post-processing step [17]. However, the resulting increase in sensitivity is typically less than a factor of 10 [18], and the inevitable spread in the concentrator's geometry leads to extra spread in the sensor's sensitivity.

Due to doping inhomogeneity and variations in the depth of the n-well, the resistances in the various branches of the Wheatstone bridge model will typically not match, e.g. in Fig. 1, R3 might be larger than R1, R2 and R4, and thus the sensor will exhibit a certain amount of offset when biased. The resulting offset is typically in the order of tens of milli-Tesla [19] [20], and is orders of magnitude larger than the sensor's own noise level. Fortunately, the effect of this offset can be significantly reduced by employing the spinning current technique [21]. This exploits the fact that swapping the functions of the readout and bias electrodes and thus changing the direction of the bias current through the sensor, will swap the relative polarities of the sensor's offset and V_{Hall}. By doing this periodically, the offset can be modulated to a so-called spinning frequency f_{spin}, while V_{Hall} can be recovered by averaging the voltage on the other two contacts, as shown in Fig. 2. To avoid the need for averaging (filtering), and also ensure better cancellation of time-varying offset, e.g. due to stress, two nominally identical Hall sensors biased in different directions can be connected in

parallel, as shown in Fig. 3 [22]. However, the inevitable mismatch between the two Hall sensors will lead to extra residual offset.

Since V_{Hall} is quite small, it is typically boosted by a low-offset amplifier prior to further signal processing. The requirements on the offset of this amplifier can be relaxed by employing a modified spinning-current technique such that the offset is kept at DC while V_{Hall} is modulated to the spinning frequency [10] [23]. As shown in Fig. 4, V_{Hall} can then be recovered by a demodulator at the output of the amplifier, which simultaneously up-modulates the offset of the Hall sensor and the amplifier to f_{spin}.
Due to the anisotropy of the n-well's resistivity, however, the resistance of the various branches of the Wheatstone bridge model also depends on the direction of the bias current [24]. As a result, the 2-phase spinning-current scheme shown in Fig. 2 will still exhibit significant residual offset. This can be reduced by employing all 4 possible bias current directions in a 4-phase spinning-current scheme. With this approach, offsets of a few tens of micro-Tesla can be achieved at spinning frequencies up to a few kHz [10] [3]. It should be noted that the use of 4 phases means that the offset will now be modulated to $2f_{spin}$ instead of to f_{spin}. By connecting four, orthogonally biased, octagonal n-well plates in parallel and employing an 8-phase spinning scheme, offsets below 4μT (3σ) can be achieved [9].

The averaging inherent to the spinning current technique means that signal components at multiples of f_{spin} will be cancelled. By exploiting this property, a

sensitivity calibration scheme was realized in which a spinning-current Hall sensor was transparently excited by a reference magnetic field at f_{spin} that was generated on-chip. The corresponding Hall voltage was then detected by an extra demodulator and used to trim the sensor's bias current, resulting in a sensitivity drift of less than 50 ppm/ºC [25].

The up-modulated offset produced by the conventional spinning-current technique causes ripple, which is usually suppressed by a low-pass filter. However, this filter will also limit the signal bandwidth. This is because f_{spin} is typically rather low (a few kHz), in order to allow the sensor to settle sufficiently after each change in bias current direction. As a result the associated filter time constants are rather large and so the resulting analog filters will occupy considerable area. Since increasing the spinning frequency leads to greater residual offset [11], the use of analog filters results in a tradeoff between filter area and offset. Another alternative is to digitize the sensor's output and then implement the low-pass filter in the digital domain. This approach is particularly effective when a sigma-delta ADC is used, since the notches of its decimation filter can be re-used for ripple suppression [26]. However, the bandwidth of the resulting digital LPF will then be less than $1/2f_{spin}$. For all these reasons, the bandwidth of low-offset CMOS Hall sensors is typically limited to less than 100 kHz [11], even though the sensor's intrinsic bandwidth can be as high as a few GHz [27].

To overcome this bandwidth limitation, this paper presents a technique that

continuously cancels the offset ripple due to the spinning-current technique, thus eliminating the need for any low-pass filtering and preserving the sensor's intrinsic bandwidth. With the proposed technique, a continuous-time bandwidth greater than 100 kHz has been demonstrated together with less than 25 μT offset.

The rest of the paper is organized as follows. Section II introduces the basic principle of the ripple reduction loop (RRL). Section III describes the proposed ripple-reduction technique, whose circuit implementation is then discussed in Section IV. Measurement results are presented in Section V, and the paper ends with conclusions and outlook.

II. Ripple reduction loop

The offset of an amplifier can be mitigated by using the chopping technique to modulate it up to a certain chopping frequency f_{chop}. As with the spinning-current technique, the up-modulated offset gives rise to ripple, and hence to a similar ripple reduction problem. In the case of chopper amplifiers, the use of a bandwidth-limiting low-pass filter can be avoided by employing a so-called ripple reduction loop (RRL) [28] [29]. As shown in Fig. 5, this senses the amplitude of the ripple at the output of the amplifier, and continuously feeds this back via an integrating path so as to cancel the amplifier's offset. The action of the RRL effectively creates a narrow notch at the chopping frequency in the amplifier's frequency response, without affecting the amplifier's high frequency response. And the notch can be circumvented by freezing

the loop once it reaches steady-state [30].

As shown in Fig. 6, a similar approach can be applied to a spinning-current Hall sensor. A ripple detector appropriately combines the amplifier's outputs $V_{1\text{-}4}$ during the 4 spinning phases (Fig. 6) to determine the ripple amplitude, which is proportional to the sensor's instantaneous offset V_{offset}, and then feeds this back via an integrating path. Apart from the bandwidth benefit, the dynamic range requirement on the amplifier is much relaxed because the offset is cancelled before amplification.

Although this approach is quite effective in the case of 2-phase spinning [31], it is less effective in the case of 4-phase spinning. This is because the magnitude of the sensor's offset changes during the various spinning phases, leading to some residual ripple at f_{spin} [8]. However, the use of a single RRL will still substantially reduce the sensor's offset and thus facilitates the use of a high gain front-end, as in [25].

III. Triple RRLs for 4-phase spinning current Hall sensor

In order to completely suppress the ripple of a 4-phase spinning-current Hall sensor, a more complex ripple-reduction algorithm is required. Fig. 7 depicts the outputs of a 4-phase spinning-current Hall sensor in a spinning cycle, where the offset ripple amplitude is not consistent as we discussed. If the outputs of a 4-phase spinning-current Hall sensor are denoted as $V_{1\text{-}4}$, then the Hall voltage V_{Hall} can be expressed as the average of these four voltages:

$$V_{Hall} = \frac{V_1 + V_2 + V_3 + V_4}{4} \quad (1)$$

The Hall sensor's instantaneous offset can then be defined as the difference between V_{Hall} and each of the outputs $V_{1\text{-}4}$. A first offset V_{os1} can be determined from V_1 and V_2,

$$V_{OS1} = \frac{V_1 - V_2}{2} \tag{2}$$

which can be used by a first RRL to cancel the ripple during the 1st and 2nd spinning phases. As shown in Fig. 7, this results in the new output voltages V_1' and V_2':

$$V_1' = V_1 - V_{OS1} = V_2' = V_2 + V_{OS1} = \frac{V_1 + V_2}{2} \tag{3}$$

In a similar manner a second RRL can be employed to extract a second offset from V_3 and V_4

$$V_{OS2} = \frac{V_3 - V_4}{2} \tag{4}$$

which can be used to cancel the ripple during the 3rd and 4th spinning phases. As shown in Fig. 7, this results in the new output voltages V_3' and V_4':

$$V_3' = V_3 - V_{OS2} = V_4' = V_4 + V_{OS2} = \frac{V_3 + V_4}{2} \tag{5}$$

Thus two RRLs can be used in a ping-pong fashion to extract the orthogonal offsets V_{OS1} and V_{OS2}, which can then be used to cancel the offset ripple associated with the 1st and 2nd spinning phases, and with the 3rd and 4th spinning phases, respectively. This means that the two RRLs act to cancel offset ripple at $2f_{spin}$. However, as shown in Fig. 7, V_1'=V_2' and V_3'=V_4' are not necessarily equal in a 4-phase spinning current Hall sensor, resulting in residual offset ripple at f_{spin}.

To remove this residual ripple, a third RRL can be used to extract a third offset from the voltages V1', V2', V3' and V4'

$$V_{OS3} = \frac{(V1' + V2') - (V3' + V4')}{4} = \frac{(V1 + V2) - (V3 + V4)}{4} \tag{6}$$

with which the residual ripple can be removed, leaving only V_{Hall} which can be expressed by:

$$V_{Hall} = V1' - V_{OS3} = V1 - V_{OS1} - V_{OS3} \quad (7)$$

$$V_{Hall} = V2' - V_{OS3} = V2 + V_{OS1} - V_{OS3} \quad (8)$$

$$V_{Hall} = V3' + V_{OS3} = V3 - V_{OS2} + V_{OS3} \quad (9)$$

$$V_{Hall} = V4' + V_{OS3} = V4 + V_{OS2} + V_{OS3} \quad (10)$$

The following observations can be made from this set of equations: 1) equations (7) - (10) are consistent with equation (1); 2) all 4 phases' output can be decomposed into linear combinations of the Hall signal V_{Hall} and three offset voltages V_{OS1}, V_{OS2} and V_{OS3}; 3) the three offsets are independent, and so the three RRLs can be operated simultaneously.

The Hall sensor's various offset is also clear through equation (7) – (10), namely $V_{OS1}+V_{OS3}$, $V_{OS1}-V_{OS3}$, $V_{OS2}-V_{OS3}$ and $V_{OS2}+V_{OS3}$ in spinning phase 1-4, respectively.

IV. System implementation

To demonstrate the effectiveness of the triple RRLs scheme, the system shown in Fig. 8 was built. It consists of a prototype chip on which a 4-phase spinning current Hall sensor and an instrumentation amplifier were implemented, and three RRLs, which were implemented with off-chip electronics for flexibility.

A. Capacitively-coupled chopper instrumentation amplifier (CCIA)

Since the instrumentation amplifier is directly connected to the Hall sensor, its noise

should be low enough to ensure that the system's noise performance is dominated by the Hall sensor (whose resistance is about 1 kΩ). It should also be power efficient, to minimize errors due to the local magnetic field generated by its supply current. Finally, to allow optimization of the Hall sensor's bias current, its input common-voltage range should extend from ground to about half the supply voltage.

In order to satisfy all these requirements, a capacitively-coupled chopper instrumentation amplifier (CCIA) was chosen (Fig. 8) [28]. The amplifier's gain is given by C_{in}/C_f. The input capacitors C_{in} block the Hall sensor's common-mode voltage, allowing its bias current to be flexibly set. Furthermore, in the case when the modified spinning-current technique is used, the capacitors also block most of the Hall sensor's offset, while passing the up-modulated V_{Hall} at $2f_{spin}$. The latter is a square-wave, which periodically charges and discharges C_{in}, which thus behaves like an impedance Z_{in} given by:

$$Z_{in} = \frac{1}{4 f_{spin} C_{in}} \tag{11}$$

To avoid loading the Hall sensor, C_{in} should be small. However, the noise contribution of the opamp can be expressed as:

$$V_n = \left(\frac{C_{in} + C_f + C_g}{C_{in}} \right) \cdot V_{nopamp} \tag{12}$$

where C_g is its input capacitance and V_{nopamp} is its noise voltage. Achieving low noise requires a large g_m, which in turn requires large input transistors with a large C_g. As a result, C_{in} must be made large enough to minimize the effect of V_{nopamp} on the overall noise performance. In this design, C_{in} = 48 pF, which results in an input impedance of

over 5 MΩ at f_{spin} = 1 kHz, and an input referred noise of about 10 nV/ √ Hz. Since the Hall sensor's sensitivity was not known a priori, the CCIA's gain can be switched between 50 and 800 by switching the feedback capacitor C_f between 960 fF and 60 fF. An auxiliary capacitor C_{cp} (= 240 fF) connected to the CCIA's virtual ground provides an input for the RRLs. The DC level of the virtual ground was fixed by large resistors implemented as MOSFETs operated in the sub-threshold region. Their equivalent resistance is larger than 10 GΩ, and so their noise contribution is negligible.

The opamp used in the CCIA is shown in Fig. 9. In order to flexibly drive external loads, a 2-stage opamp was implemented. It consists of a folded cascode amplifier whose output is buffered by source followers. Each transistor of the input pair is biased in weak inversion at 55 µA, resulting in a g_m of about 1 mS. The opamp has a DC gain of 96 dB and a GBW of about 10 MHz with a 50 pF load. The source followers relax the need for large resistors in the common-mode feedback and also drive the bonding pads. The opamp's offset can be trimmed by applying an external voltage to an auxiliary input pair with a g_m of about 10 µS.

B. Spinning-current with 4-phase non-overlapping clock

The implementation of the spinning-current Hall sensor is shown in Fig. 10, where signals $phi_{1\text{-}4}$ control the direction of the biasing current, while signals $out_{1\text{-}4}$ control the location of the output ports. As the biasing current and the location of the output ports of Hall sensor are periodically switched, transient spikes will be present in the

sensor's output signal. To minimize their effect, an on-chip clock generator implements the signals $out_{1\text{-}4}$ in a non-overlapping fashion (Fig. 11), such that the CCIA is briefly disconnected from the Hall sensor while the bias currents are allowed to settle.

C. RRL implementation

To compare different ripple-reduction algorithms, the three RRLs were implemented off-chip hardware as shown in Fig. 12a. The voltages $V_{1\text{-}4}$ output by the CCIA during the 4 spinning phases is sampled and digitized by a 16-bit ADC. The digital results are then stored and processed in a CPLD to extract the three residual offsets (V_{OS1}, V_{OS2} and V_{OS3}). These signals are then integrated by two 17-bit (V_{OS12}) and one 18-bit (V_{OS3}) accumulators whose 16 MSBs are then combined and applied to a 16-bit DAC to generate the appropriate compensation signal V_{DAC} for each spinning phase.

As the ADC under-samples the CCIA's wide-band noise, the computed offsets will be rather noisy. This problem can be mitigated by increasing the length of the accumulators at the expense of a longer start-up time. However, this approach leads to an exponential increase in the number of logic gates required to implement the accumulator's adder.

A simpler solution is to replace the accumulator with a comparator and up/down counter [30], as shown in Fig. 12b. The comparators determine only the polarities of

the residual offsets of V_{OS1-3}, and then appropriately increment or decrement the counters. The compensation signal can only change by 1 LSB in one spinning cycle, and so, at steady state, the amplitude of the residual ripple is limited to 1 LSB, which corresponds to a magnetic field of 7.6μT.

It is worthwhile to mention that the triple RRLs could be realized more elegantly with compact analog circuitry, as in chopper amplifiers like [28].

V. Experimental results

The spinning-current Hall sensor and the CCIA were implemented in a 0.18-μm 5-V supply CMOS process. The chip photo is shown in Fig. 13. To minimize residual offset, 4 orthogonally parallel-connected Hall sensors were used. Each Hall plate consists of a p+ pinched n-well, as shown in Fig. 14. The p+ layer reduces the thickness of the Hall sensor somewhat, thus increasing its Hall sensitivity [19]. Moreover, the sensor's 1/f noise will be reduced since the depletion layer formed by the reverse-biased p+/n-well junction effectively isolates the sensor from the crystal defects present at the Si/SiO_2 interface [32]. Furthermore, the p+ layer will keep the Hall sensor away from the shallow trench isolation (STI) oxide, which reduces the stress gradient created by STI.

The composite Hall sensor has a measured sensitivity of 50 mV/T when biased with 0.35 mA per Hall plate. Measurements on 8 samples, with f_{spin} = 1 kHz, show that the sensor's offset is less than 25 μT with a mean value of 3 μT. The input referred noise

of the sensor and amplifier corresponds to a thermal noise floor of 0.28 μT/ √ Hz.

Fig. 15 depicts sensor's residual offset versus spinning frequency without any RRL. It can be seen that the sensor's residual offset increases dramatically when the spinning frequency exceeds f_{spin} > 10 kHz. This is in line with other work as [11], and is probably caused by incomplete thermal settling of the Hall plates at high spinning frequencies, charge injection related in the CCIA and its finite linearity. To minimize the residual offset, the measurements described in the following sections were made with f_{spin} fixed at 1 kHz.

A. Residual ripple

Fig. 16 shows the FFT of the CCIA's output with zero magnetic input when a single RRL (Fig. 6) is used. It can be seen that although this approach effectively suppresses the offset ripple at $2f_{spin}$, there is still some residual square-wave ripple, which gives rise to spectral components at f_{spin} and its odd-order harmonics.

Fig. 17 shows the FFT of the CCIA's output with zero magnetic input and the accumulator-based triple-RRL scheme shown in Fig. 12a. It can be seen that this reduces the residual ripple at f_{spin} by further 40 dB. With this scheme, steady state can be achieved in 2 spinning cycles, i.e. 2ms when f_{spin}=1 kHz. However, the noise-aliasing associated with the ADC introduces extra noise around f_{spin} and $2f_{spin}$.

The noise-aliasing problem is solved by the comparator-counter-based triple RRLs at the expense of settling time. With f_{spin}=1 kHz, the system takes 6 seconds to settle. As can be seen from the resulting FFT plot (Fig. 18), the noise floor now becomes quite flat. Meanwhile, the residual ripple at f_{spin} and $2f_{spin}$ is now less than 10 μT, which is commensurate with the sensor's noise into a bandwidth of 1.2 kHz. The system's start-up time can be decreased by initially incrementing the counter in multi-LSB steps and then reducing the step size to 1 LSB once steady-state has been reached.

B. Bandwidth measurement

Fig. 19 shows the setup for the bandwidth measurement, where a voltage-to-current amplifier generates an AC current in a PCB trace under the test chip, thus generating an AC magnetic field with a known frequency. The comparator-counter-based RRLs were used and the CCIA output was measured by a HP3562A spectrum analyzer.

The Bode plot corresponding to a CCIA gain of 800 is shown in Fig. 20. The Hall sensor system exhibits a 12.5 kHz -3dB-bandwidth, which is determined by the CCIA. The RRLs also detect and then cancel any signal at f_{sipn} and $2f_{spin}$, resulting in two narrow notches in the sensor's frequency response. Reducing the CCIA's gain to 50 extends the system bandwidth above 100 kHz (the upper limit of the spectrum analyzer), as shown in Fig. 21.

Tab. 1 summarized the performance of the test chip and compares it to that of other

low-offset CMOS Hall sensors. With the triple RRLs scheme, the test chip achieves 3 times more bandwidth than [31], while achieving 8 times less offset. Compared to [3], an order of magnitude improvement in bandwidth was achieved, together with similar offset.

VI. Conclusion

A new readout technique for spinning-current Hall sensor is proposed. It involves the use of three ripple-reduction loops to suppress the up-modulated offset ripple at f_{spin} and $2f_{spin}$. A test chip with spinning-current Hall sensors and an on-chip capacitively-coupled chopper instrumentation amplifier was realized in a 0.18-μm CMOS process. This was combined with off-chip hardware to realize the triple RRLs, which were then able to reduce the offset to less than 25 uT, while also reducing the AC ripple by more than 40 dB, to about 10 uT. The triple RRLs scheme eliminates the need for any further low-pass filtering, thus preserving the system's full bandwidth, which was greater than 100 kHz.

ACKNOWLEDGMENT

The authors would like to thank Texas Instruments for chip fabrication and financial support.

References

[1] S. H. Shalmany, D. Draxelmayr, and K. A. Makinwa, "A micropower battery current

sensor with±0.03%(3σ) inaccuracy from− 40 to+ 85° C." *IEEE ISSCC Dig. Papers*, pp. 386-387, Feb. 2013.

[2] P. E. Schneider, and R. D. Lorenz, "Evaluation of point field sensing in IGBT modules for high bandwidth current measurement." *Energy Conversion Congress and Exposition (ECCE)*, pp. 1950-1957, Sep. 2011,

[3] M. Motz, U. Ausserlechner, M. Bresch, U. Fakesch, B. Schaffer, C. Reidl*, et al.*, "A miniature digital current sensor with differential Hall probes using enhanced chopping techniques and mechanical stress compensation," *IEEE Sensors,* Oct. 2012.

[4] M. Nymand and M. A. Andersen, "High-efficiency isolated boost DC–DC converter for high-power low-voltage fuel-cell applications," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 505-514, Feb. 2010.

[5] S.-W. Hong, T.-H. Kong, S.-H. Park, C. Park, S. Jung, S. Lee, et al., "High Area-Efficient DC-DC Converter With High Reliability Using Time-Mode Miller Compensation (TMMC)," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2457-2468, Oct. 2013.

[6] B. Miedzinski, A. Szymanski, W. Dzierzanowski, and B. Wojszczyk, "Performance of Hall Sensors when used in ground fault protections in MV networks," *Conf. Universities Power Engineering (UPEC)*, Sep. 2004.

[7] A. Elez, S. Car, and Z. Maljkovic, "Detection of inter-coil short circuits in synchronous machine armature winding on the basis of analysis of machine magnetic field," *Electrical Machines (ICEM), Conf. International XIX,* Sep. 2010.

[8] F. Blaabjerg, J. K. Pedersen, U. Jaeger, and P. Thoegersen, "Single current sensor

technique in the DC link of three-phase PWM-VS inverters: a review and a novel solution," *IEEE Transactions on Industry Applications,* vol. 33, pp. 1241-1253, Sep/Oct. 1997.

[9] J. C. Van Der Meer, F. R. Riedijk, E. van Kampen, K. A. Makinwa, and J. H. Huijsing, "A fully integrated CMOS hall sensor with a 3.65 μT 3σ offset for compass applications," *IEEE ISSCC Dig. Papers*, pp. 246-247, Feb. 2005.

[10] C. Schott, R. Racz, A. Manco, and N. Simonne, "CMOS single-chip electronic compass with microcontroller," *IEEE J. Solid-State Circuits,* vol. 42, no. 12, pp. 2923-2933, Dec. 2007.

[11] P. Dimitropoulos, P. Drljaca, and R. Popovic, "A 0.35 um-CMOS, wide-band, low-noise HALL magnetometer for current sensing applications," *IEEE Sensors,* pp. 884-887, Oct. 2007.

[12] R. Steiner Vanha, "Rotary switch and current monitor by Hall-based microsystems," Zürich, Physical Electronics Laboratory, Swiss Federal Institute of Technology (ETH), 1999.

[13] K. Skucha, P. Liu, M. Megens, J. Kim, and B. Boser, "A compact Hall-effect sensor array for the detection and imaging of single magnetic beads in biomedical assays," *Conf. Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS),* pp. 1833-1836, Jun. 2011,

[14] Y.-J. Min and S.-W. Kim, "A CMOS TDC-based digital magnetic Hall sensor using the self temperature compensation," *Conf. CICC,* pp. 329-332, Sep. 2008.

[15] Y. Xu, H.-B. Pan, S.-Z. He, and L. Li, "Monolithic H-bridge brushless DC vibration

motor driver with a highly sensitive Hall sensor in 0.18 μm complementary metal-oxide semiconductor technology," *IET Circuits, Devices & Systems,* vol. 7, pp. 204-210, Jul. 2013.

[16] R. T. Merrill, M. W. McElhinny, and P. L. McFadden, “Magnetic Field of the Earth,” vol. 63, USA, Academic Press, 1996.

[17] Z. B. Randjelovic, M. Kayal, R. Popovic, and H. Blanchard, “Highly sensitive Hall magnetic sensor microsystem in CMOS technology,” *IEEE J. Solid-State Circuits,* vol. 37, no. 2, pp. 151-159, Feb. 2002.

[18] S. Brugger, and O. Paul, “Magnetic field amplification by slender cuboid-shaped magnetic concentrators with a single gap,” *Sensors and Actuators A: Physical,* vol. 157, no. 1, pp. 135-139, Jan. 2010.

[19] P. Ripka and M. Janosek, "Advances in magnetic field sensors," *IEEE J. Sensors,* vol. 10, pp. 1108-1116, Jun. 2010.

[20] G. Boero, M. Demierre, P.-A. Besse, and R. Popovic, "Micro-Hall devices: performance, technologies and applications," *Sensors and Actuators A: Physical,* vol. 106, pp. 314-320, Sep. 2003.

[21] P. Munter, "A low-offset spinning-current Hall plate," *Sensors and Actuators A: Physical,* vol. 22, pp. 743-746, Jun. 1989.

[22] J.T. Maupin, M.L. Geske, ”The Hall effect in silicon circuits,” The Hall effect and its applications, pp. 421-445, Plenum New York, Springer US, 1980.

[23] J. Jiang, K. Makinwa, and W. Kindt, "A continuous-time ripple reduction technique for spinning-current Hall sensors," Conf. *ESSCIRC*, pp. 217-220. Sep. 2013,

[24] O. Paul, P. Ruther, L. Plattner, and H. Baltes, “A thermal van der Pauw test structure,” *IEEE Transactions on Semiconductor Manufacturing,* vol. 13, no. 2, pp. 159-166, May. 2000.

[25] M. Pastre, M. Kayal, and H. Blanchard, “A Hall sensor analog front end for current measurement with continuous gain calibration,” *IEEE J. Sensors,* vol. 7, no. 5, pp. 860-867, May. 2007.

[26] M. Blagojevic, M. Kayal, M. Gervais, and D. De Venuto, “SOI Hall-sensor front end for energy measurement,” *IEEE J. Sensors,* vol. 6, no. 4, pp. 1016-1021, Aug. 2006.

[27] L. Stephenson, and H. Barlow, “Power measurement at 4 Gc/s by the application of the Hall effect in a semiconductor,” *Proceedings of the IEE-Part B: Radio and Electronic Engineering,* vol. 106, no. 25, pp. 27-30, Jan. 1959.

[28] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. Makinwa, "A1.8 μW 60nV/ √Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS For Wireless Sensor Nodes," *IEEE J. Solid-State Circuits,* vol. 46, no. 7, pp. 1534-1543, Jul. 2011.

[29] Q. Fan, J. H. Huijsing, and K. A. Makinwa, "A 21 nV/ √Hz Chopper-Stabilized Multi-Path Current-Feedback Instrumentation Amplifier With 2 μV Offset," *IEEE J. Solid-State Circuits, ,* vol. 47, no. 2, pp. 464-475, Feb. 2012.

[30] R. Wu, J. H. Huijsing, and K. A. Makinwa, "A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error," *IEEE J. Solid-State Circuits,* vol. 46, no. 12, pp. 2794-2806, Dec. 2011.

[31] M. MOTZ, D. DRAXELMAYR, T. WERTH, and B. FORSTER, "A chopped hall sensor with small jitter and programmable true power-on function," *IEEE J. Solid-State Circuits,* vol. 40, no. 7, pp. 1533-1540, Jul. 2005.

[32] F. Hooge, T. Kleinpenning, and L. Vandamme, "Experimental studies on 1/f noise," *Reports on progress in Physics,* vol. 44, no. 5, pp. 479-532, May. 1981.

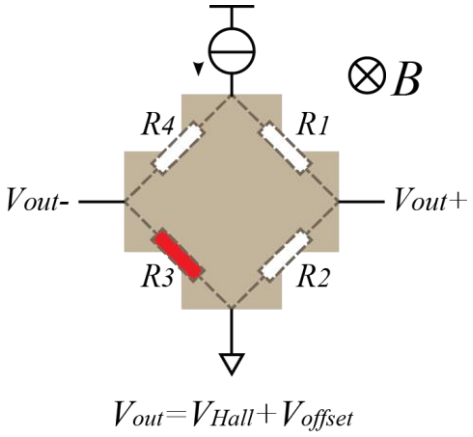

Fig. 1 Wheatstone bridge model of Hall sensor

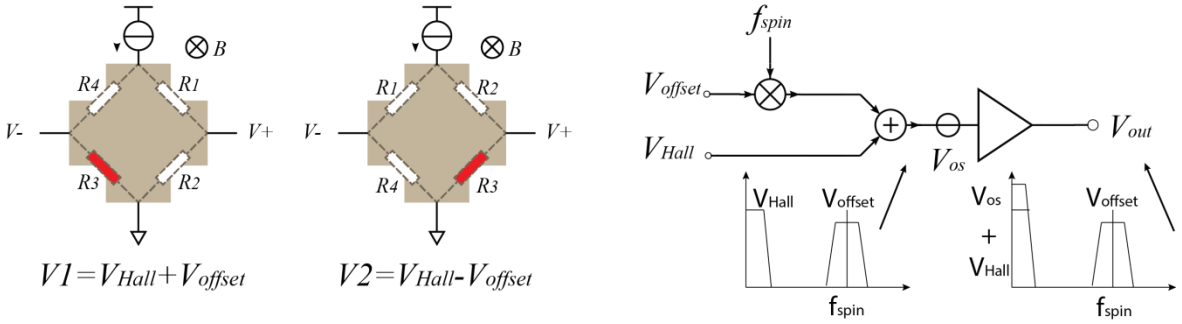

Fig. 2 Conventional spinning-current technique: offset at f_{spin}, signal at DC

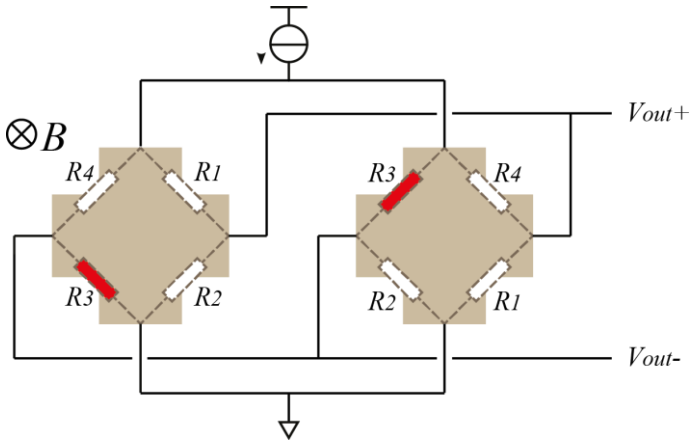

Fig. 3 Orthogonally parallel connected Hall plates

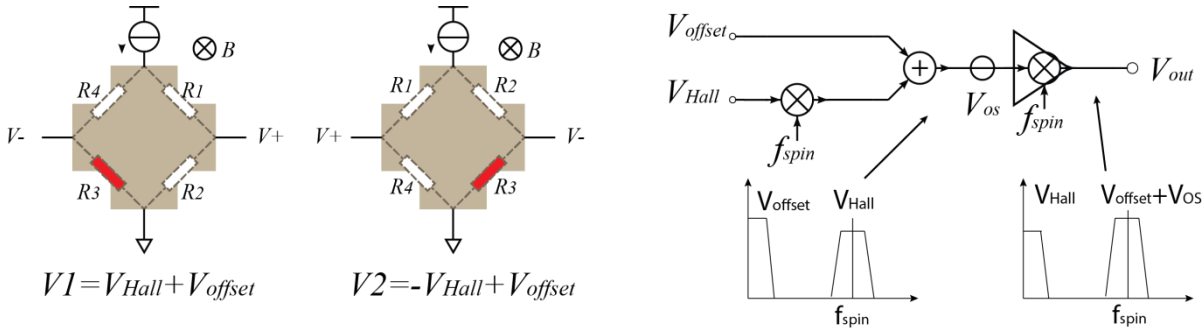

Fig. 4 Modified spinning-current technique: signal at f_{spin}, offset at DC

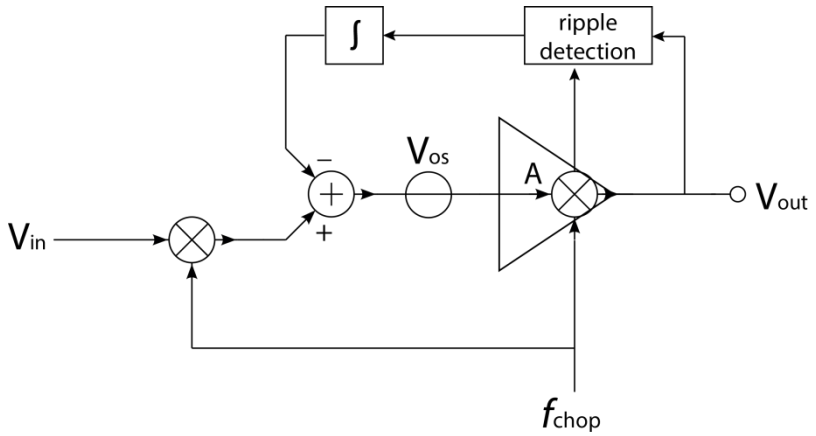

Fig. 5 Ripple reduction loop (RRL) in a chopper amplifier

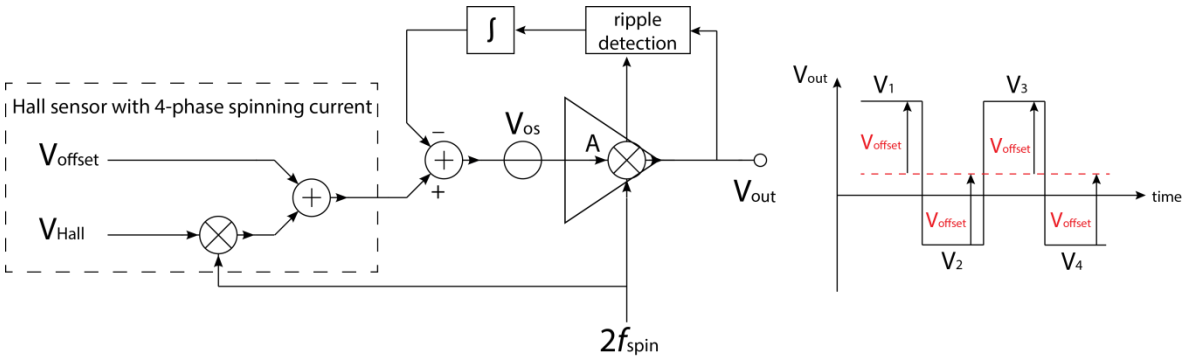

Fig. 6 Ripple reduction loop used in 4-phase spinning-current Hall sensor

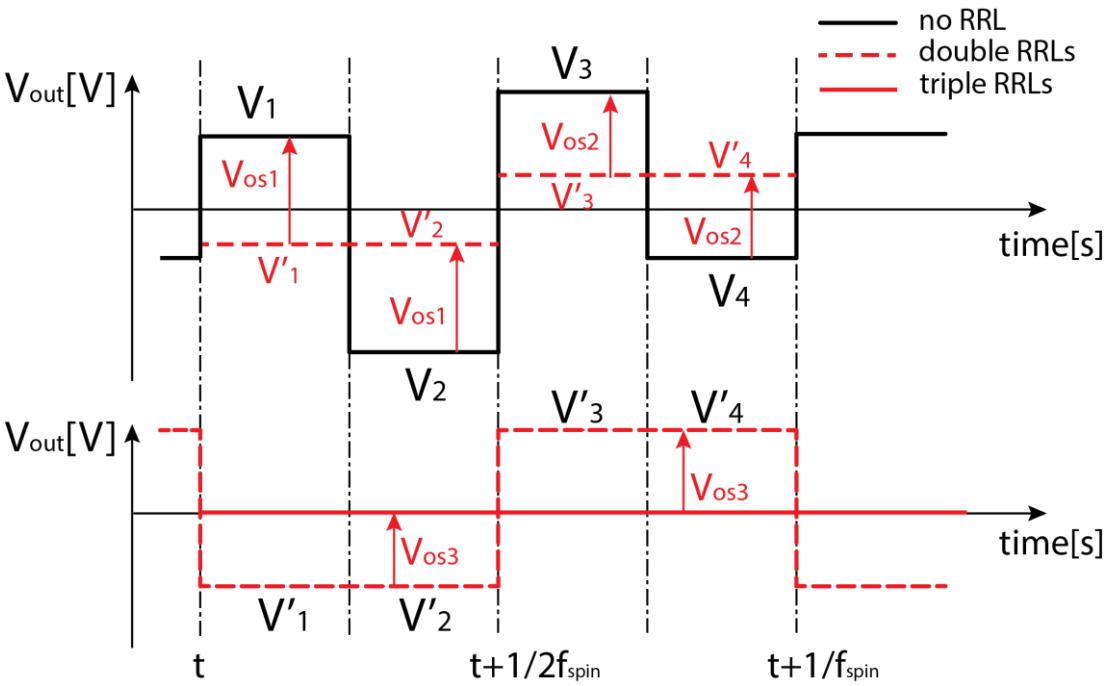

Fig. 7 The working principle of triple RRLs for 4-phase spinning-current Hall sensor

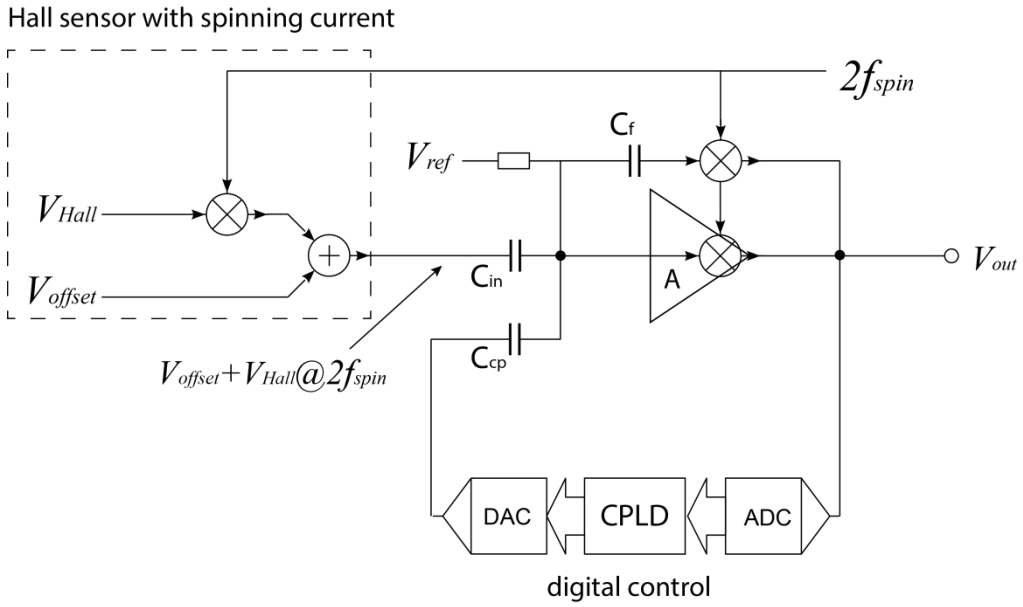

Fig. 8 Block diagram of the test system

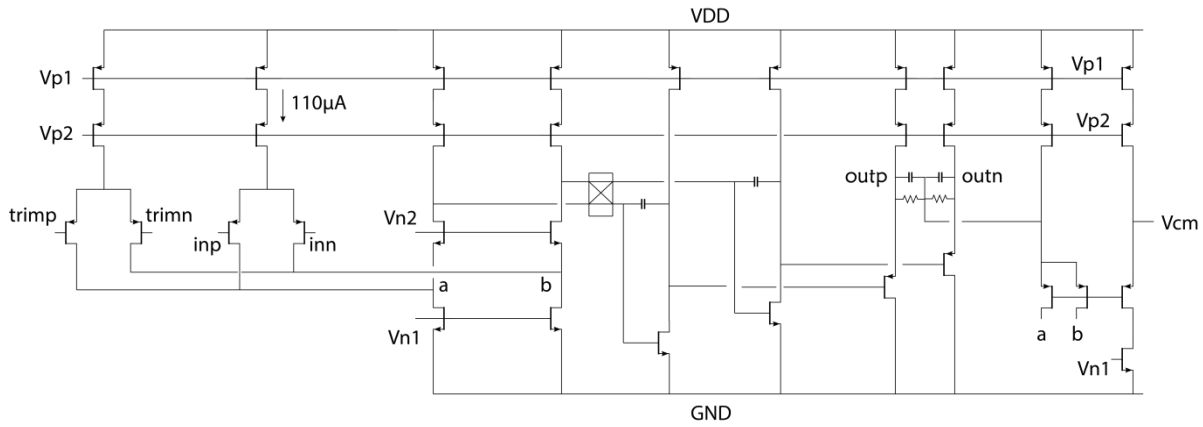

Fig. 9 Schematic of the opamp used in CCIA

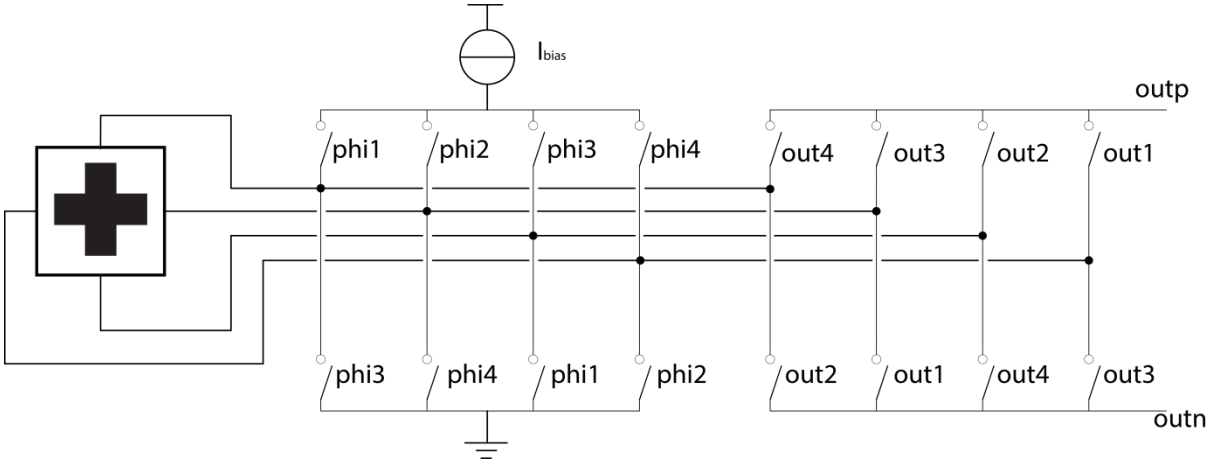

Fig. 10 Implementation of the 4-phase spinning-current Hall sensor

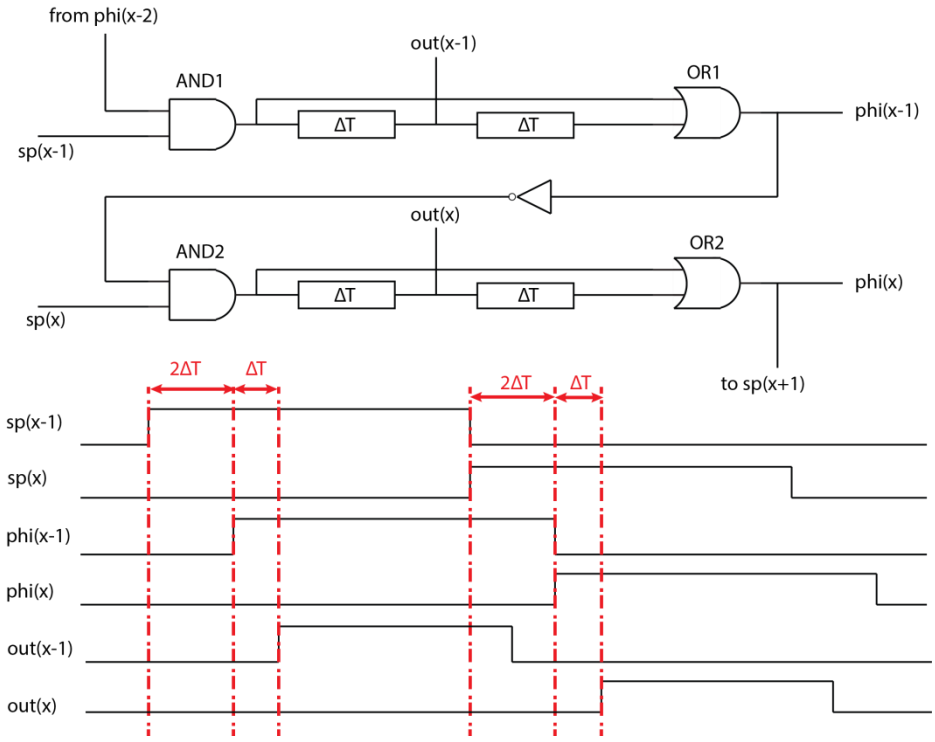

Fig. 11 Block diagram and timing sequence of the 4-phase non-overlapping clock generator

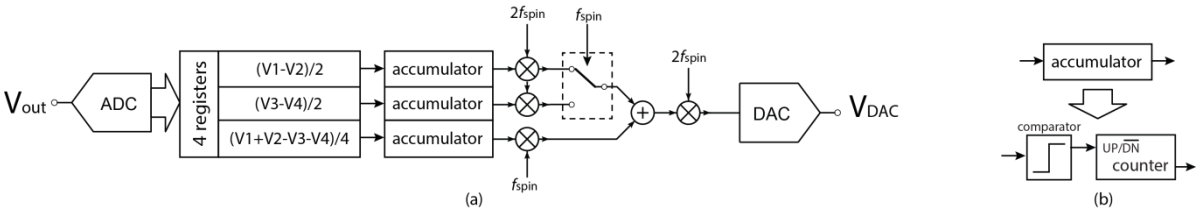

Fig. 12a triple RRLs implementation, Fig. 12b accumulator can be replaced with comparator and up/down counter

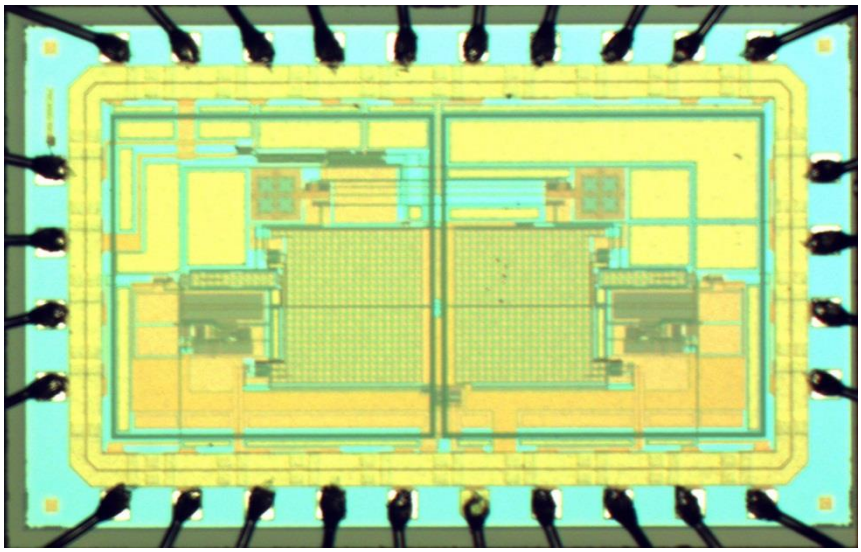

Fig. 13 Micro-photo of the test chip

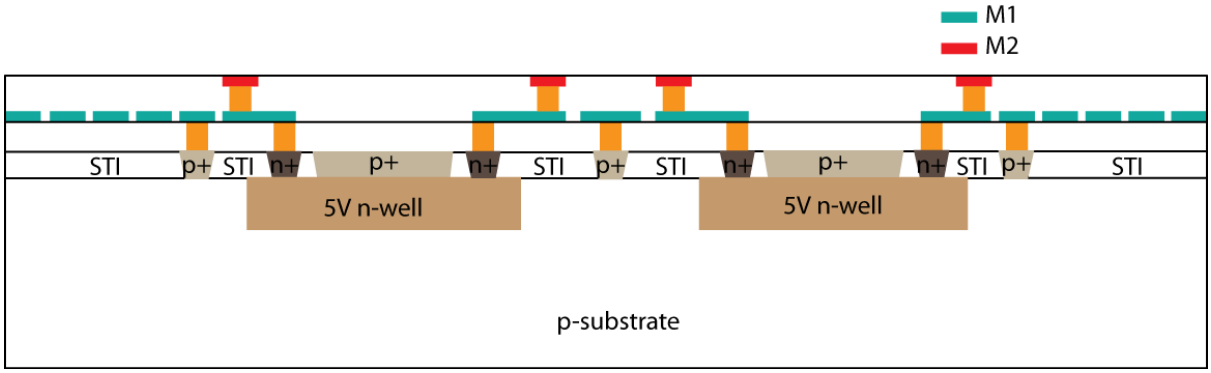

Fig. 14 Cross section of Hall sensor

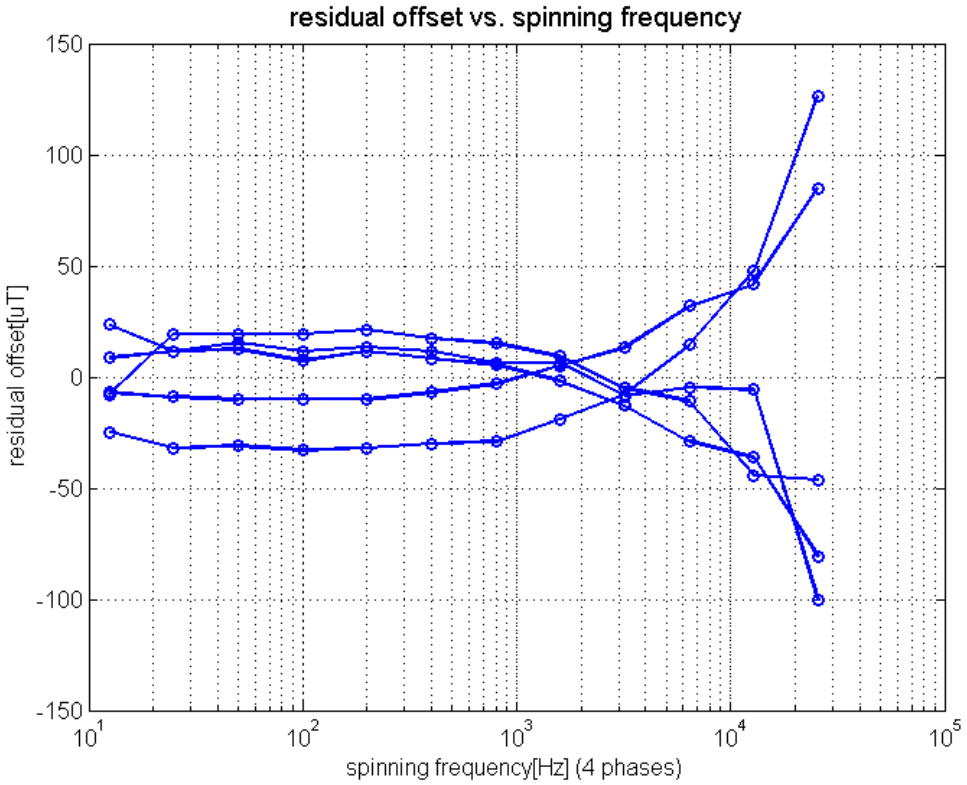

Fig. 15 Measurement result of residual offset versus spinning frequency

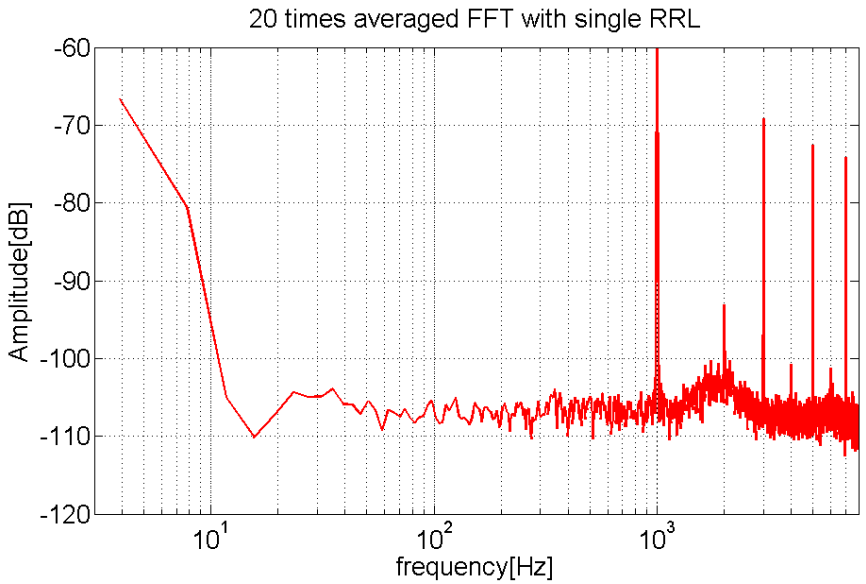

Fig. 16 FFT plot of the amplifier's output with a single RRL

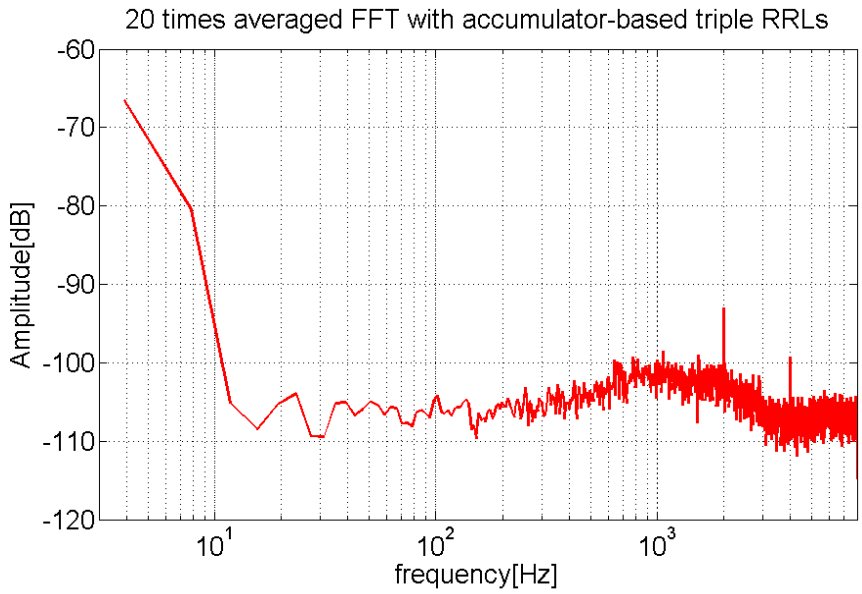

Fig. 17 FFT plot of the amplifier's output with triple RRLs

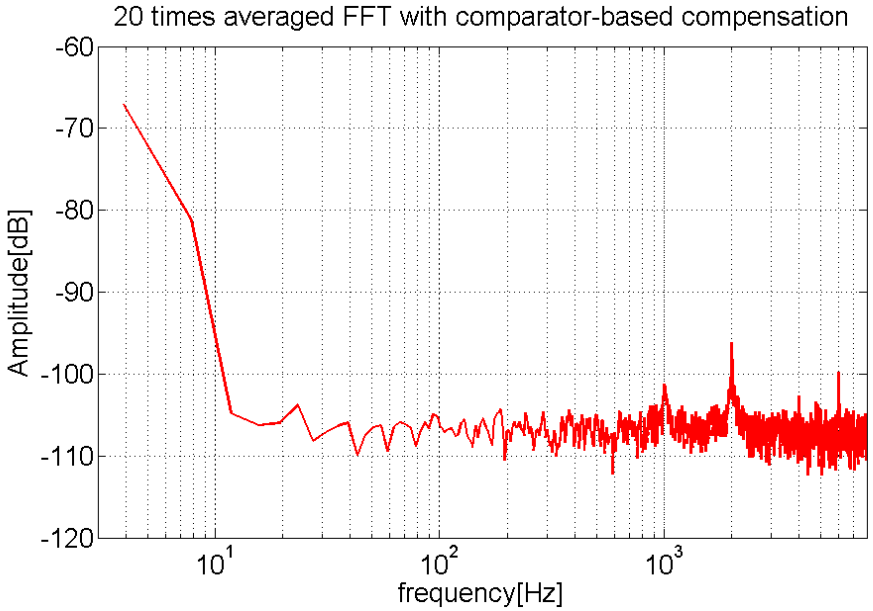

Fig. 18 FFT plot of the amplifier's output with comparator-counter based triple RRLs

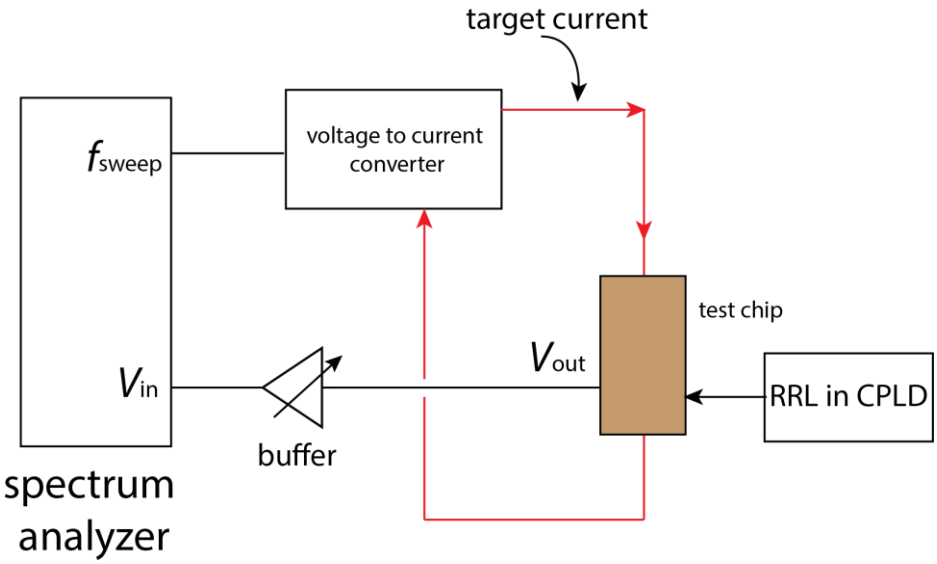

Fig. 19 Test setup for bandwidth measurement

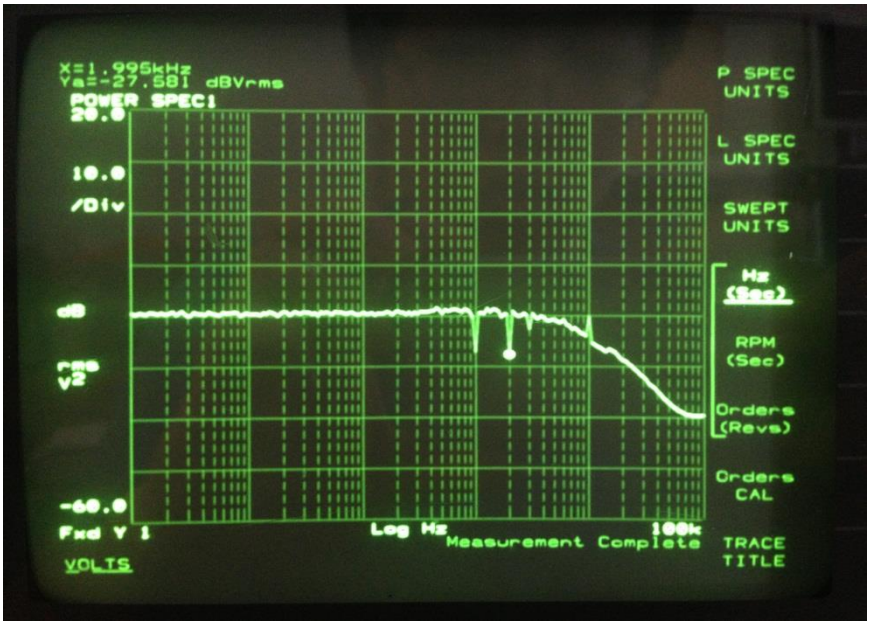

Fig. 20 Bandwidth measurement with on-chip gain of 800

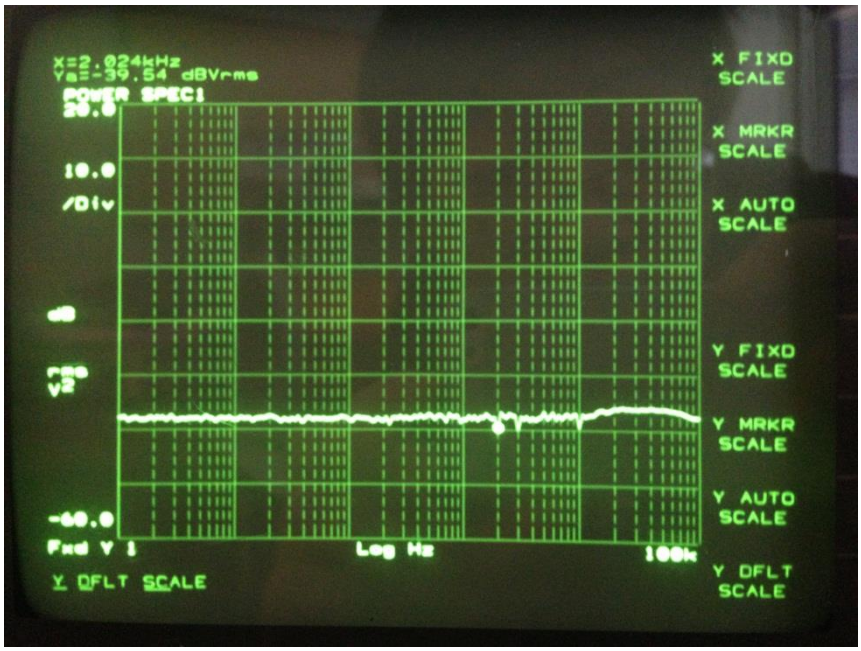

Fig. 21 Bandwidth measurement with on-chip gain of 50

Tab. 1 Comparison table of this work with other CMOS low-offset Hall sensors

Source	This work	[9]	[10]	[31]	[3]
Offset (μT)	25	3.65 (3σ)	10	<200	10
Spinning frequency (No. of phases)	1 kHz (4)	N/A (8)	50 kHz (4)	220 kHz (4)	40 kHz (4)
Bandwidth (kHz)	>100	N/A	0.1	30	10
Resolution (μT rms)	89	0.33	N/A	120	N/A