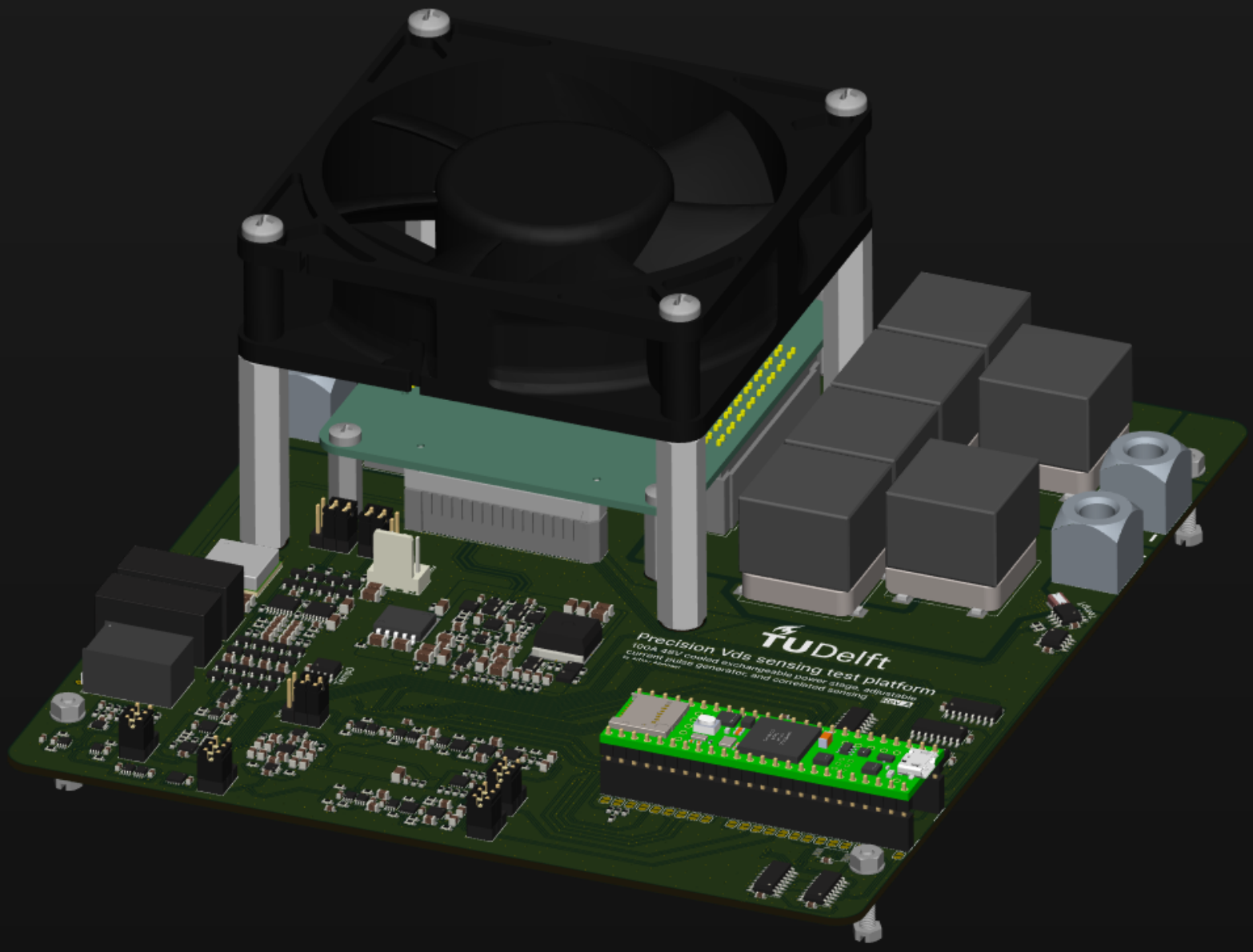
Low cost precision Vds current sensing

Arthur Admiraal



TU Delft

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In partial fulfilment of the requirements for the degree of

Master of Science
in Electrical Engineering

at the Delft University of Technology.

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Abstract

Vds current sensing has the potential to improve power density, efficiency, and cost compared to conventional current sensing methods by removing the need for a dedicated (quasi-)lossy sensing device. However, achieving high precision requires a temperature compensation method that has traditionally come at the expense of flexibility, test cost, or power density. This work proposes an online calibration method based on small signal resistance measurement through the periodic injection of small submicrosecond current pulses that are orthogonal to the load current. This provides an estimate of the large signal resistance that is insensitive to manufacturing tolerance and device type. Furthermore, junction temperature can be simultaneously estimated from the resistance variation. With $129\,\mathrm{mW}$ injection power, the method achieves $0.54\,\mathrm{A}$ RMS single point calibrated current error over a $\pm 54\,\mathrm{A}$ range on a $48\,\mathrm{V}$ single phase experimental platform. Since all circuitry is connected parallel to the power stage, the method is suited to integration into a smart gate driver IC.

Acknowledgements

In October 2022, I started on the final leg of my journey to completing my Master's degree. Little did I know that it would take over two years to arrive at my destination, during which time I would meet a partner, see my company turn from a scrappy student team to a professional organisation, and deal with a fire that nearly burnt it all down. Hence, I am indebted to a great many people for their support and encouragement that helped complete this work.

First of, I would like to express my deepest gratitude to my supervisor Prof. Dr. Ir. Qinwen Fan, whose guidance motivated me to push beyond what I thought possible and whose flexibility helped me keep advancing towards my goals, even in challenging and unforeseen circumstances. Beyond her academic support, I will also cherish the discovery of Rotterdam's best hot-pot restaurant on a team trip she led—a delicious bonus to my research journey.

Second, I am grateful to the members of the defense comittee, who were not only kind of enough to offer their time, but were also gracious enough to offer access to their lab equipment (in the case of Prof Dr. Ir. Aditya Shekhar) and give detailed feedback on my work, pushing me to be more creative (in the case of Ir. Anton Montagne).

I would also like to extend my sincere thanks to Prof. Dr. Ir. Kofi Makinwa for his encouragement in pursuing this work when I first had the idea, to my colleagues at Lobster for their kind understanding and less kind but effective ideas to motivate me, and to the ever-suffering technicians, system administrators, and workshop supervisors for their patience with my requests, in particular the kind people of DEMO for turning a cheese storage box into a sophisticated high voltage protection enclosure.

Finally, I want to acknowledge those who are closest to me. My heartfelt thanks go to my parents for their patience and support, and to my girlfriend who was always there for me.

Thank you all, I could not have done it without you.

Arthur Admiraal
Delft, Netherlands
December 2024

1 Introduction

1.1. Background

1.1.1. Driving small electric motors

The compactness, controllability, and low cost of small electric motors have enabled diverse applications, from cordless power tools and Light Electric Vehicles (LEVs) (e.g., e-bikes) to Unmanned Aerial Vehicles (UAVs) and lightweight robotics. Their low weight and size reduce strain in handheld uses and improve performance in mobile applications, where battery power is common. Smaller, lighter components further compound these advantages.

Industry has focussed on Brushless DC (BLDC) motors [1, 2], a type of Permanent Magnet Synchronous Motor (PMSM), due to their high torque density, efficiency, and reliability at a low cost [3, 4]. These motors rely on three-phase currents in stator windings, producing a rotating magnetic field that guides rotor magnets. This field, shaped by magnetic materials, creates a significant winding inductance of generally $10\,\mu\mathrm{H}$ to $1\,\mathrm{mH}$. Although nonlinear and rotor-dependent, this inductance largely limits the motor's electrical dynamics, while the rotor motion induces a back-EMF voltage in the windings.

BLDC motors require current at variable frequencies (usually up to $2\,\mathrm{kHz}$) and thus depend on motor drivers to manage power flow from a DC bus (mainly up to $50\,\mathrm{V}$). High power density and a low price are common goals [1] as is high efficiency, which extends battery life and reduces the need for bulky cooling systems [5, 6]. Typically, they comprise three inverters feeding the motor phases and a control system that manages switching, as shown in figure 1.1. Though many motor drivers are filterless, having a direct connection from the inverters to the motor, an additional output filter may be used to reduce the ripple current flowing into the motor.

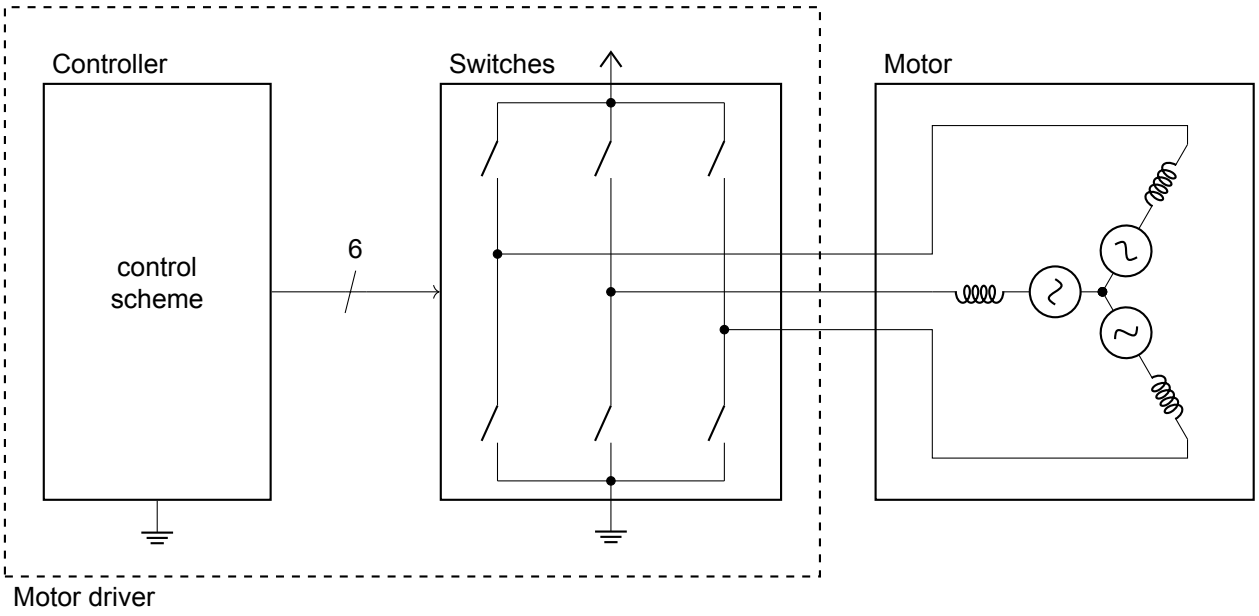


Figure 1.1: Typical motor driver system

Current sensing is essential for motor control and protection. It provides real-time feedback on the motor's operating state, allowing precise adjustment of torque and speed. By continuously monitoring and correcting the current, the control scheme can achieve precise motion control. This requires a low error, with typical Root Mean Squared

Errors (RMSEs) of at most $2\,\%$ of full scale. Current sensing is also used to detect faults such as short circuits, which protects both the motor and its driver from potential damage.

1.1.2. Discrete current sensing

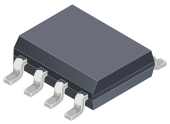
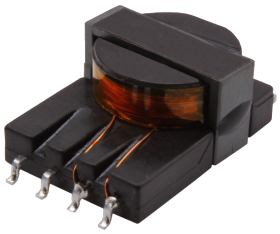
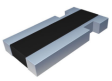
Many approaches to current sensing have been developed [7, 8, 9], though some are more commonly applied than others. Traditionally, dedicated discrete components play a key role.

Shunt resistors are widely used. They are based on Ohm's law: the current is passed through a known shunt resistance, creating a voltage that is proportional to the current. To limit power loss, the shunt resistance is kept very low - typically in the $\mathrm{m\Omega}$ range. This results in low signal swings that are scaled up for further processing, often by so-called current sense amplifiers.

Usually, the shunt resistors are not put inline with the output phases and there are fewer shunt resistors than phases. Instead, the shunt resistors are placed at some of the lower legs of the inverters. This saves cost by decreasing the amount of components and reducing the common mode swing requirements on the current sense amplifiers [10, 11]. Since the motor has three connections, one phase current can be fully reconstructed using measurements of two other phases. With slight modifications of the modulation, phase currents may also be reconstructed through sequential measurements of a single bus return current measurement [12].

Another approach to current sensing relies on measuring the magnetic field that forms around currents. In current transformers, the field induces a voltage in a secondary winding wrapped around a high magnetic permeability core that is placed around the current-carrying wire. Since only dynamic fields induce voltages, this technique does not pick up DC currents. Alternatively, strategically placed Hall effect sensors can be used to directly measure the fields and distinghuish both DC and AC current. These magnetic field-based methods avoid the inherent power loss of shunt resistors, making them effectively "lossless" while also naturally rejecting common-mode voltage swings. The galvanic isolation is also often noted as an advantage, but is not relevant to low voltage systems. Though more complex and costly than shunt resistors, they offer a viable alternative in certain applications.

Table 1.1: For a $50\,\mathrm{A}$ peak $48\,\mathrm{V}$ power stage based on the DRV8302, traditional current sensing methods come with significant cost factors.

			
Device	Hall sensor [13]	Current transformer [14]	Leg shunt resistor [15]
Price at 1k quanity	€1.74	€2.14	€0.20
Size	$6 \times 4.9 \times 1.6\,\mathrm{mm}^3$	$12.8 \times 20.5 \times 7.5\,\mathrm{mm}^3$	$1.5 \times 3.1 \times 0.5\,\mathrm{mm}^3$
Power loss	$625\,\mathrm{mW}$	$625\,\mathrm{mW}$	$469\,\mathrm{mW}$
Total error (typical)	$\pm 1.0\,\mathrm{A}$	Unspecified	$\pm 1.5\,\mathrm{A}$

As tabulated in table 1.1 each of these current sensing methods come with a cost in terms of power dissipation, area, capital, and complexity. First, there are the direct costs. Each discrete component comes with procurement and assembly costs. The inherent losses of shunt resistors come with a significant area requirement for adequate power dissipation. Furthermore, structures with the required electromagnetic coupling for magnetic current sensing tend to be bulky. Yet, the indirect costs may be more significant. Though the magnetic sensors are not inherently lossy, they do require the diversion of the flow of current through a structure with the appropriate electromagnetic properties. This indirectly forces additional power consumption in the parasitic resistance of the added wire length and thus makes these methods only quasi-lossless. Similarly, as devices move towards higher frequency operation the parasitic inductance of shunt resistors can require the adoption of more complex driving circuitry that is robust to the associated ground bounce [16]. In a practical sense, all of these methods are invasive, having to be accomodated by additional routing in-line with the current.

1.1.3. The desire for integration and its limits

Significant advances have been made in the efficiency, power density, and cost-effectiveness of motor drivers. Though much of this improvement has been driven by advances in switching devices, integration has also been recognised as a powerful tool to achieve these goals [17].

Yet, this integration has not always been realised. At high currents, switching devices are often not integrated. They tend to be manufactured using specialised processes that are not compatible with monolithic integration. Furthermore, the flexibility in the selection of the switching device is used to make an appropriate tradeoff of efficiency, size, and cost for the target application.

Instead, there has been a trend to integrating everything but the switching devices. Some commercial products integrate high and low side gate drivers, adjustable dead-time, overcurrent protection, precision current sense amplifiers, and a low-voltage supply for digital control circuitry [18]. Recent developments in smart-gate drivers have seen further integration of slew rate control circuitry, dead-time optimisation, and intelligent protection features that optimise efficiency and enable the removal of external damping components [19, 20].

Despite this trend, current sensing has usually been integrated to a limited extent. At high current levels, parasitics of common packages and process nodes form a barrier to the efficient conduction of the load current. The added parasitics of routing these currents from the power stage to gate drivers poses an additional challenge. Hence, though current sense amplifiers and inprecise overcurrent protection have long been a part of many gate drivers, invasive external components have traditionally been required to achieve a fidelity that is suitable for closed-loop motor control.

1.1.4. The potential and challenge of Vds sensing

Vds-based current sensing is a promising technique for enabling tighter integration of current sensing within smart gate drivers. As illustrated in figure 1.2, it involves using the parasitic resistance of the switching device as a shunt resistor so that the drain source voltage V_{ds} is taken to be proportional to the current. Since the sensing circuitry is in parallel to the power path and thus does not need to conduct the load current, integration into standard processes becomes viable. There is also the advantage of a higher signal swing, since a greater portion of the power budget is usually dedicated to losses in the switching device. Though this method shares the disadvantage of leg shunts that the current measurement must be performed in a limited window, three sensors are sufficient to fully reconstruct the phase currents, even at full modulation.

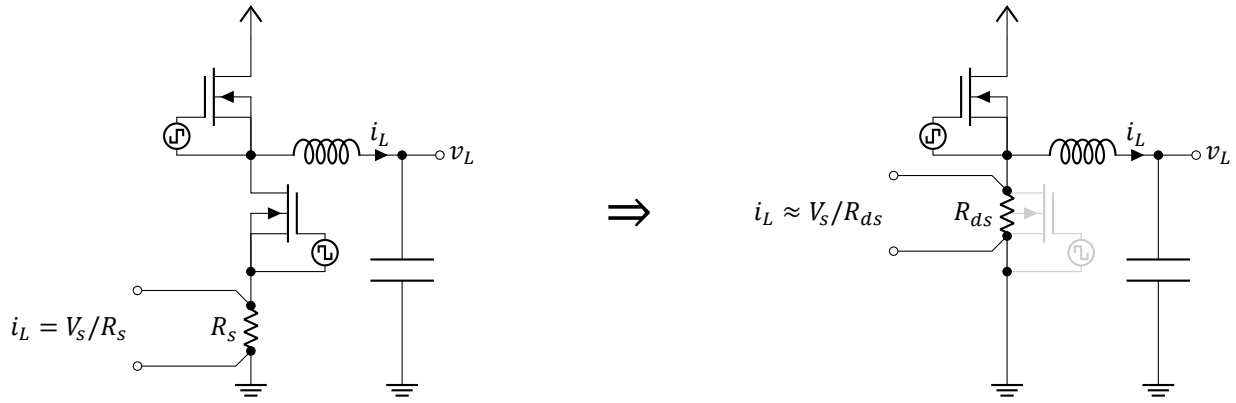


Figure 1.2: Vds sensing uses the parasitic on-state resistance to estimate output current.

Vds sensing comes with several challenges. One challenge is that the sensing circuitry must tolerate the large voltage swings at the switching node [21], which may overshoot the rails by up to $30\,\%$ of the bus voltage. However, the more fundamental challenge is that the parasitic resistance depends strongly on temperature and, to a lesser extent, on other environmental conditions. This has given Vds sensing a reputation of low accuracy [9, 8]. Several solutions can be considered, which will now be discussed.

Compensation-based techniques

Compensation-based techniques are based on the subtraction of an estimate of the error, thus correcting for the known component of the error. The advantage of these methods is that the error estimate can be derived from readily available or easily measurable information. However, their effectiveness is limited by the accuracy of the underlying model; unmodeled effects can significantly exacerbate errors. Notably, most of the approaches considered here fail to account for the degradation of the switching device, which can reach up to $20\,\%$ according to [21]. This omission raises concerns about the robustness of these methods

Replica sensing Perhaps the most complete model of a switching device is a copy of it. In replica current sensing, this idea is exploited by measuring the current through a scaled-down copy of the switching device with equal terminal voltages and in close proximity to the switching device. Since the devices are in close proximity, their temperatures are matched. As the replica copies all aspects of the device, it also compensates for other errors such as production tolerance and nonlinearity.

This idea has been widely applied in integrated circuits, where the voltage over the power and sensing devices are usually equalised using feedback at the drain [22, 23, 24, 25]. With discrete switches in higher power applications, accuracy is often traded for simplicity by sensing the voltage over a shunt resistor at the source, though feedback at the source has also been described [26, 27].

The accuracy of this method is limited by matching, at $\approx \pm 3\%$ in power semiconductors [26, 28, 29]. An advantage is that the method is in principle robust to degradation, which affects both the main switching device and replica.

Adoption is hampered by the increased cost and restriction of design freedom to a limited set of specialised devices [8].

Using a separate structure Co-integrated and thus closely thermally coupled temperature sensors have been used to implement linear temperature compensation. Total errors of 3% [30] and 5% [29] have been reported. Like replica sensing, these structures are only found in specialised devices, limit flexibility and come with inherent costs.

Case temperature compensation Measurements of the case temperature may be combined with Vds measurements and models of the switch behaviour to estimate the device temperature. In [31], models of the temperature dependence of the channel resistance, the thermal resistance of the case, and power losses of the switch are iteratively applied to find the junction tempereature, resulting in a 3σ error of 1.5% in steady state for static loads and case temperature rises of $15\,^{\circ}\mathrm{C}$.

The advantage of this method is that no specialised devices are required. Though a temperature sensor must be included, this is already found on many motor drivers for temperature monitoring. A disadvantage is that extensive testing must be performed to find the 6 model coefficients. Given that production tolerances may mean these coefficients are substantially different between devices, slow and thus expensive factory thermal characterisation may be needed. Initially gathering these coefficients will also increase development time. Given that dynamics were not modelled, this issue will become more severe if the method is adapted to dynamic loads, such as those found in motor drivers.

Using Temperature Sensitive Electrical Parameters The large body of work on estimating the junction temperature from electrical parameters of switching devices could provide another path towards die temperature compensation in ordinary devices, though no applications to Vds sensing are known to the author. Apart from on-resistance, commonly investigated Temperature Sensitive Electrical Parameters (TSEPs) include gate leakage current, gate resistance, threshold voltage, and switching delay times [32, 33]. A potential problem is that the available well-behaved TSEPs vary by device type. Furthermore, measuring the die temperature is only half the battle. The connection of the die to the circuit board has been shown to be a major contributor to the resistance of Insulated-Gate Bipolar Transistors (IGBTs) devices whilst not closely tracking the die temperature [34]. It may be possible to predict this temperature using a thermal model, though this would increase the calibration requirements for the system.

Feedback-based techniques

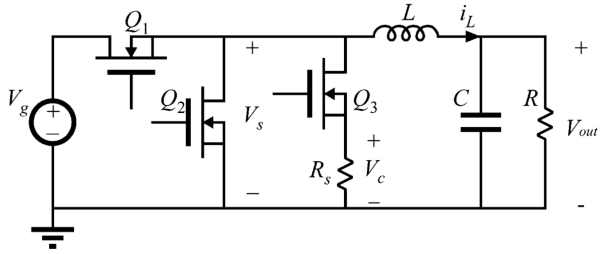
Feedback-based techniques are based on the subtraction of the measured error. The advantage of these approaches is that it can correct errors that are not easily predicted. However, the downside is that it requires a measurement of the error, which may not be straightforward. Case and point, the resistance is not in itself an electrical signal, and can thus only be measured from its response to a signal. This could be the current resulting from an applied voltage or the voltage resulting from an applied current. Applying a voltage requires a lower impedance source than the parasitic resistance of the switch, but this is usually not practical in a power stage, which requires a low parasitic resistance to reduce losses. Applying a current requires a higher impedance source than the parasitic resistance, and is thus a good fit.

Several approaches for measurements based on injecting such a test current will now be discussed.

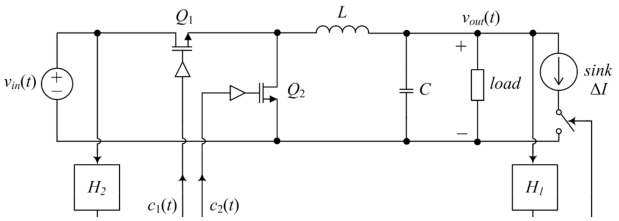
Through an alternate measurement of the load current One option is to turn the load current in a known test current through a separate measurement of it. The resistance may then be calculated using Ohm's law. The main proponents of this technique make the measurement by diverting the current through an alternate path that has a current sensing resistor [35], as illustrated in figure 1.3a. Since the calibration measurement is made very infrequently, this enables the measurement circuitry to be optimised for small size and cost.

Since an alternate path is used for the measurement, the current and voltage measurements do not occur at the same instant. This introduces an error, especially since the change in resistance due to the measurement path will cause a disturbance in the current. [35] introduces a scheme that suppresses this error to below $1\,\%$ but depends on the stability of the load over several cycles. Better transient performance may be attainable when the alternate path is only enabled for a part of the switching cycle, as in [36].

The advantage of this method is the large signal swing provided by the use of the load current. The downside is that even for low duty cycles, an alternate path still comes at a significant cost in high-current systems.



(a) The load current that normally flows through Q2 can be measured while flowing through the alternate path through Q3 [35].



(b) A small test current can be injected at the output [37].

Figure 1.3: Resistance measurement options

Through a known feature of the current If some feature of the load current signal is known, this could serve as the test current. For example, though the bulk current may be unknown, a high-frequency component may have known characteristics. Though this approach has not yet been explored in the context of Vds sensing, the idea has often been applied in Voltage Regulator Modules (VRMs) [38, 39]. Alternatively, though the instantaneous values may not be known, the statistical behaviour of the signal may be known. In motor drivers, such a feature may exist in the ripple current, given by:

$$\frac{\partial i}{\partial t} = \frac{V_{applied} - V_{bemf}}{L} \quad \Rightarrow \quad \Delta\frac{\partial i}{\partial t} = \frac{V_s - V_{bemf}}{L} - \frac{0 - V_{bemf}}{L} = \frac{V_s}{L}$$

Though the rising and falling ramp rate of the current depends on the back-emf, the difference between them depends only on the supply voltage and inductance. If the inductance is known, this may be used to predict this ramp rate, which may then serve as a test signal to find the current.

The advantages of this method are that it does not require circuitry to divert current from the switch whilst still providing a sizeable signal swing. The downside is that the accuracy is low, as the inductance has significant manufacturing tolerance and may vary due to the nonlinearity of the magnetics.

Through an injected reference feature If the load current does not contain a known feature, such a feature can be purposefully added by the injection of a current. This current should be small to prevent high power dissipation and significant heating of the switching device. It should also have a high enough frequency not to be shorted by the inductance but a low enough frequency not to be shorted by the parasitic capacitance. Furthermore, it should be possible to distinguish the current from the bulk current.

The advantage of this method is that the measurement process can be tighly controlled, but the disadvantage is that the signal swing is dependent on the size of the current feature that can be generated.

The test current could be injected before or after the output filter. Injection after the filter has been discussed [37, 40], as illustrated in figure 1.3b. An advantage of this method is the low voltage swing, easing requirements on the current source. The disadvantage is that the filter also affects the meaasurement, giving a low update rate. This technique is not applicable to filterless motor drivers.

Another design option that merits further investigation is the injection of a small current at the switching node, directly into the channel resistance. Compared to injection after the filter, this offers a higher update rate but comes at the expense of higher requirements on the current source. It also offers compatibility with filterless motor drivers. Though it has not been applied in the context of Vds sensing, injection directly into shunt resistors has been explored in accuracy monitoring of energy meters [41], where $0.1\,\%$ performance was achieved through measuring the response to an out-of-band pilot tone. Similarly to Vds sensing, the measurement was performed while the load flowed through the shunt resistor. Dissimilarly, the dynamics were significantly slower and the shunt resistor was continually connected, enabling long integration periods. Recently, a similar idea was used for self-calibration of trace shunt resistors [42], which achieved $0.2\,\%$ gain error but did so with the load unconnected for long integration times. Though there are big differences between these applications and Vds sensing, they show the potential of this method.

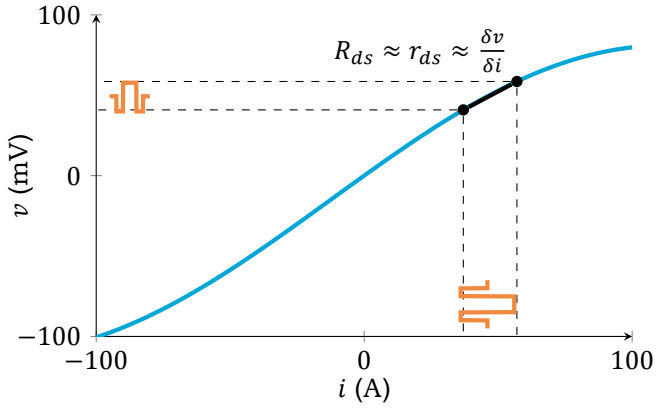
Conclusion

Compensation-based methods have not yet shown sufficient fidelity for use in motor drivers. Even if the error could be reduced, they inherently come with limited flexibility, expensive integration, or a large characterisation effort. Feedback-based approaches show promising performance, but existing injection methods have been costly, inaccurate, or too slow for Vds sensing. Yet, this is not a fundamental limitation. The rapid injection of current pulses at the switching node has not yet been explored and has the potential to reduce the cost of feedback-based Vds sensing.

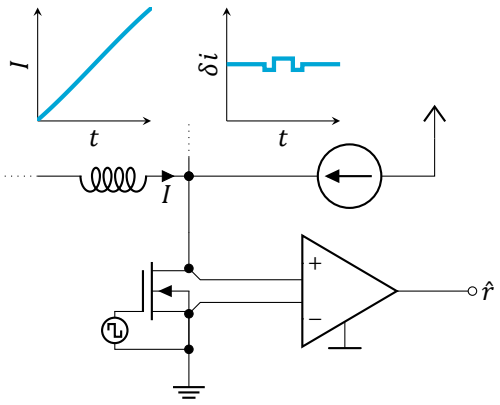
1.2. This work

So far, Vds sensing has not delivered on its promise of precision current sensing at a low cost, preventing integration into smart gate drivers. Existing methods do not achieve the required performance, or rely on the addition of costly

production processes and/or components. The goal of this thesis is to assess to what extent the cost to performance ratio of Vds sensing may be improved with measurement of the small-signal resistance through the injection of small currents at the switching node, as illustrated in figure 1.4.



(a) R_{ds} is estimated from r_{ds} measurement through a small injected current δi.



(b) The measurement path is in parallel to the power path.

Figure 1.4: The big idea is to estimate the current I from the drain-source voltage V through online measurement of the small-signal resistance.

First, chapter 2 provides an error analysis that informs what errors need suppresion. Then, chapter 3 will build upon this to motivate that linear online calibration is sufficient to achieve $2\,\%$ error, provided that a sufficient update rate is chosen. It will also argue that an architecture based on correlation processing and the injection of down-up-up-down pulses by a linear current source achieves a precision within $6\,\mathrm{dB}$ of the optimum while minimising cost factors. Furthermore, it will show that the architecture is insensitive to the most significant nonidealities through modelling their error. Chapter 4 describes a test platform in PCBA technology that achieves a $1\,\%$ RMSE while experiencing a $20\,\%$ shift in channel resistance in under $30\,\mathrm{s}$. Finally, chapter 5 concludes this thesis.

2

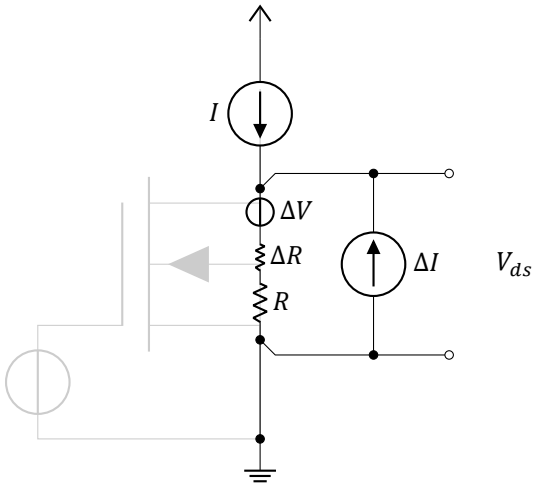
Errors in Vds sensing

Vds sensing is based on the assumption that channel resistances of switching devices behave as ohmic resistors, such that $I = V_{ds}/R_{ds}$. In reality switching devices deviate from this assumption, exhibiting several effects that become sources of error when not addressed. Hence, achieving high fidelity requires suppresing the impact of some of these effects. However, this suppresion comes with costs. Hence, the highest performance to cost ratio achieved when the suppresion is limited to effects that reduce performance below the desired level.

Here these effects are identified by quantifying the impact of several potential sources of error based on electrothermal simulation models of a representative silicon MOSFET (IPT010N08NM5) and GaN HEMT (EPC2031).

2.1. Error model

The errors can be divided in three categories: current errors, voltage errors, and resistance errors. Each affects the estimated current in a different way, as illustrated in figure 2.1. Under a small fluctuation assumption, resistance errors cause gain errors of $\Delta G_r = \Delta R/R$, voltage errors cause offsets of $\Delta I_{off} = \Delta V/R$, and current errors cause offsets of ΔI that are subject to the gain errors.



$$\hat{I} = \frac{V_{ds}}{R} = \frac{\Delta V + (\Delta I + I) \cdot (R + \Delta R)}{\hat{R}} = (I + \Delta I) \cdot \left(1 + \frac{\Delta R}{R}\right) + \frac{\Delta V}{R}$$

Figure 2.1: Voltage, current, and resistance errors each affect the estimated current in a unique way.

In general, the instantaneous error is not meaningful, as it may be current-dependent and stochastic. Rather, an average quantity gives more insight. The Root Mean Square (RMS) error is a natural fit due to the widespread familiarity with RMS measures. Under a small fluctuation approximation and for the T-periodic signals found in motor drivers, the total RMS error is:

$$\Delta\hat{I}_{rms} = \sqrt{\frac{1}{T}\int_0^T \Delta\hat{i}(t)^2 \,\mathrm{d}t} \approx \sqrt{\frac{1}{T}\int_0^T \left(i(t) \cdot \frac{\Delta r(t)}{R} + \Delta i(t) + \frac{\Delta v(t)}{R}\right)^2 \mathrm{d}t}$$

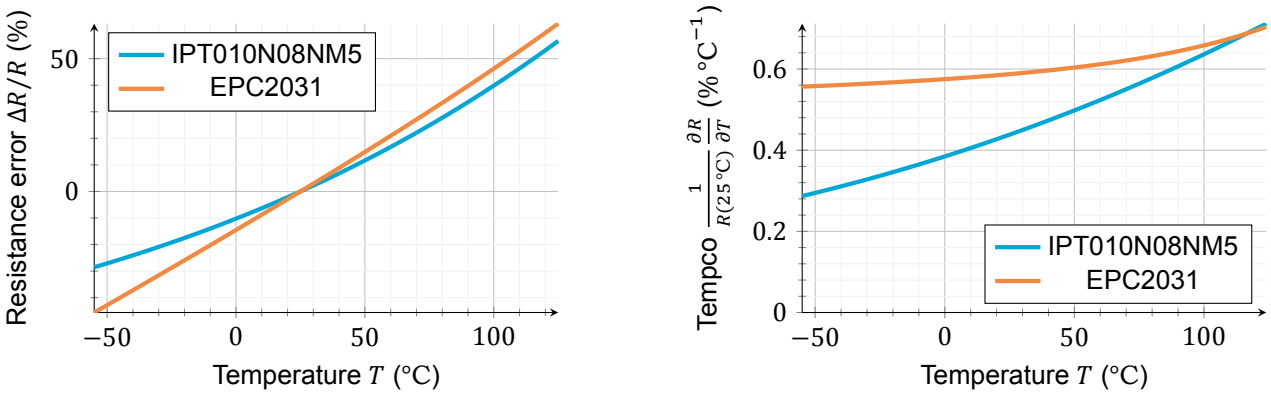
The contribution of individual RMS errors to the total depends on their mutual correlation. The contribution to the total error is highest when the errors are fully correlated, in which case the RMS errors add. Hence, the RMS error evaluated for individual error sources can be seen as a pessimistic estimate for their contribution to the total error.

Errors may also depend on factors specific to a unit or the environment. In a Bayesian approach, the average would be taken over a statisical model of such factors, so that the error metric emphasizes circumstances that are most likely to occur. However, many applications will have poorer performance than this average. Hence, a classical approach will be adopted here, with no statistical assumptions on these factors. Instead, worst case analysis will be applied to find the worst case RMS error. This ensures the error metric can be interpreted as the minimum performance in any application.

2.2. Sources of error

2.2.1. Temperature dependence

The temperature dependence of switching resistances is commonly cited as a major source of error [31, 8, 9, 43, 35, 29]. It can be modelled as a resistance error on top of a nominal resistance. Figure 2.2 shows the simulated small-signal resistance at no load current over temperature. A significant variation can be observed. Figure 2.2b shows that the associated temperature coefficient is roughly $0.5\,\%\,°\mathrm{C}^{-1}$.



(a) The resistance varies with a factor of $\approx 2\times$ over temperature.

(b) The temperature coefficient of the resistance exceeds 0.5%.

Figure 2.2: The temperature dependency of the switching resistance gives a considerable error.

Taking the room temperature resistance as the nominal resistance and assuming full-scale sinusoidal currents, the worst-case RMS error due to temperature dependence occurs at the maximum temperature of $125\,°\mathrm{C}$:

$$\Delta\hat{I}_{temp,rms} = \frac{I_{FS}}{\sqrt{2}} \cdot \frac{|\Delta R|_{max}}{R} \quad \Rightarrow \quad \frac{\Delta\hat{I}_{temp,rms}}{I_{FS}} = \frac{1}{\sqrt{2}} \cdot \frac{|\Delta R|_{max}}{R} = \frac{1}{\sqrt{2}} \cdot 63\,\% = 45\,\% \tag{2.1}$$

2.2.2. Production tolerance

Another widely recognised source of error is uncertainty about the value of the parasitic resistance due to production tolerance [9, 43, 35, 29] or lack of manufacturer documentation [8]. This can be modelled as a resistance error. Switching device datasheets do not typically list the minimum resistance value, only the typical and maximum value [44, 45]. This gives an indication of the positive tolerance, which is illustrated in figure 2.3, along with an estimate for both the positive and negative tolerance from Motorola application note [26], a switching device manufacturer.

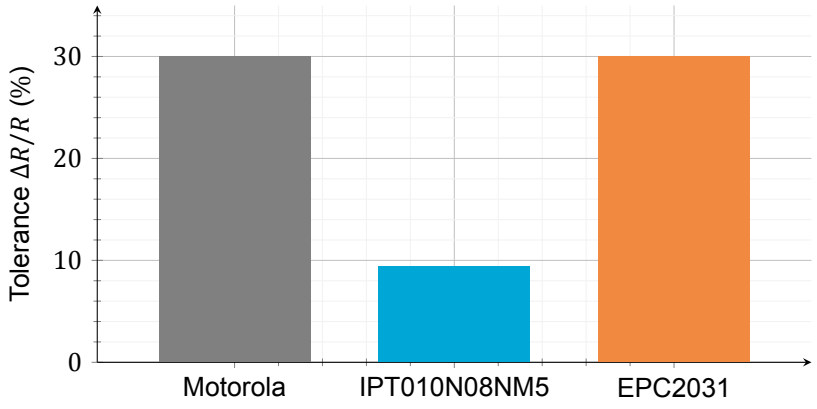


Figure 2.3: Various sources indicate a production tolerance of about 30% worst-case.

There is a reasonable agreement between the sources, though the IPT010N08NM5 exhibits a significantly better

tolerance. This may be attributable to its low channel resistance, which makes the resistance of relatively precise metal bonding elements a larger contributor, as shown in section 2.2.3. The worst-case RMS error due to production tolerance then is:

$$\frac{\Delta\hat{I}_{tol,rms}}{I_{FS}} = \frac{1}{\sqrt{2}} \cdot \frac{|\Delta R|_{max}}{R} = \frac{1}{\sqrt{2}} \cdot 30\,\% = 21\,\% \tag{2.2}$$

2.2.3. Gate voltage dependency

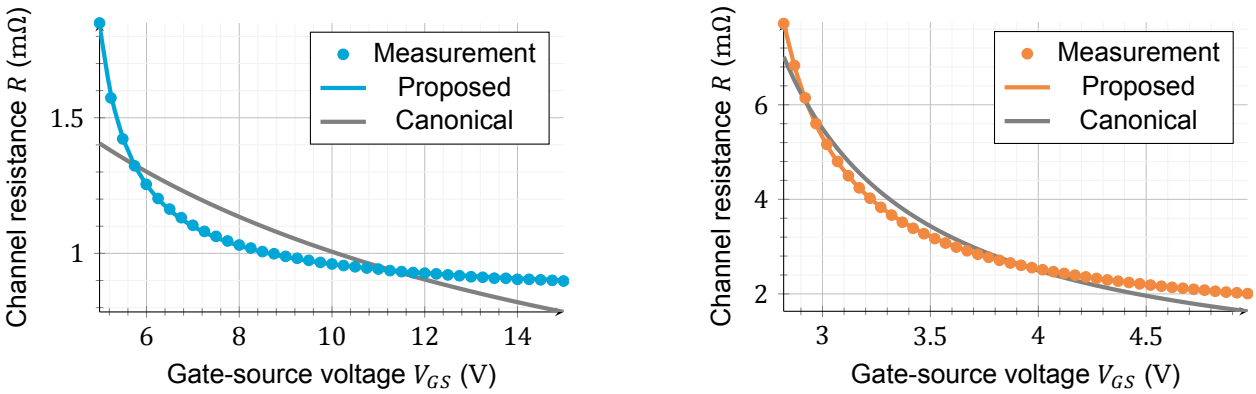
The dependency of the resistance on gate voltage is often noted [31, 8, 9, 43, 29], though not explicitly associated with a source of error. This can be modelled as a resistance error. For the square law model of a mosfet in triode region, the resistance can be found through a derivative:

$$I_D = \frac{W}{L} \cdot \mu C_{ox} \cdot \left(\left(V_{gs} - V_{th}\right) \cdot V_{ds} - \frac{V_{ds}^2}{2} \right) \quad \Rightarrow \quad R = \frac{\partial V_{ds}}{\partial I_D} = \frac{L}{W \cdot \mu C_{ox} \cdot \left(V_{gs} - V_{th}\right)} \tag{2.3}$$

And this formula is frequently stated [9, 8, 43, 43]. Yet, it is not a good fit to the resistance to gate voltage dependency curves in datasheets, as illustrated in figure 2.4. This is because it does not take into account the linear parasitic resistances at the source and drain of the device, which become significant for high currents. The effect can be modelled using a single linear bonding resistance R_{bond}, as derived in appendix A.1:

$$R = \frac{\partial V_{ds}}{\partial I_D} = \frac{L}{W \cdot \mu C_{ox} \cdot \left(V_{gs} - V_{th}\right)} + R_{bond} \tag{2.4}$$

As illustrated in figure 2.4, this model achieves a close fit to datasheet curves. Note that at the maximum gate voltage the bonding resistance is a significant fraction of the resistance for both devices, even dominating the resistance of the IPT010N08NM5.



(a) IPT010N08NM5, $R_{bond} = 0.83\,\text{m}\Omega$, $R_{mos,min} = 0.07\,\text{m}\Omega$

(b) EPC2031, $R_{bond} = 1.18\,\text{m}\Omega$, $R_{mos,min} = 0.82\,\text{m}\Omega$

Figure 2.4: The square-law model fits poorly to datasheet measurements, but the discrepancy is resolved when modelling bonding resistance.

Using equation 2.4, the sensitivity of the relative on-resistance error to gate voltage errors can be found:

$$\frac{1}{R} \cdot \frac{\partial R}{\partial V_{gs}} = -\frac{1}{\left(V_{gs} - V_{th}\right) \cdot \left(1 + \frac{R_{bond}}{R_{mos}}\right)} \quad \Rightarrow \quad \frac{\Delta R}{R} \approx -\frac{1}{1 - \frac{V_{th}}{V_{gs}}} \cdot \frac{1}{1 + \frac{R_{bond}}{R_{mos}}} \cdot \frac{\Delta V_{gs}}{V_{gs}} \tag{2.5}$$

In which R_{mos} is the square law resistance of the mos device, as given in equation (2.3). Equation (2.5) shows that the relative error in the on-resistance is directly related to the relative error in gate voltage, scaled up or down depending on the ratio of the gate voltage to threshold voltage and the bonding resistance to mosfet resistance.

It is difficult to determine the relative error in the gate voltage, since it strongly depends on the specific gate driver implementation. However, an educated guess can be made for a typical system based on a traditional bootstrap capacitor driven by a controlled power supply through a diode. The power supply is typically tightly controlled, to within 1%. Hence, the voltage over the diode when the high-side switch is actived is the dominant source of error.

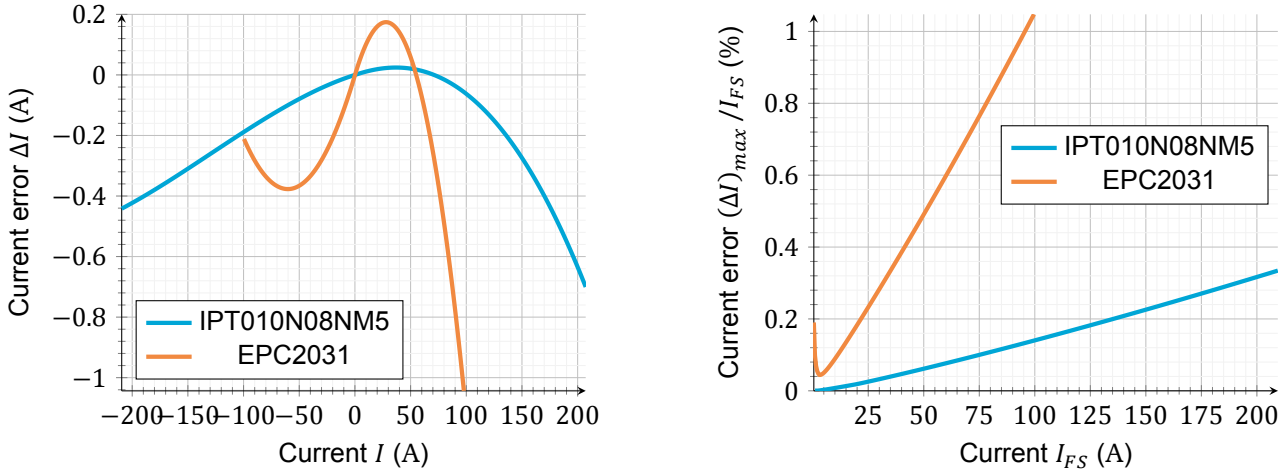
After the switching node voltage goes low, the diode becomes strongly forward biased and thus has a low small-signal resistance. As a result, the bootstrap capacitor quickly charges. However, as the bootstrap capacitor gets charged, the forward bias over the diode grows weaker, decreasing the impedance and exponentially slowing the charging. Because of this, the voltage on the bootstrap capacitor at a given sufficiently late moment is relatively insensitive to the starting voltage or charging time but very sensitive to the low-current forward voltage of the diode. This voltage is heavily temperature dependent. As an example, it varies between $0.35\,\text{V}$ and $0.7\,\text{V}$ for the UCC27282-Q1 gate driver IC used in the test setup described in chapter 4. For the lowest gate-voltage EPC2031 device, this corresponds to a $\pm 4\,\%$ error compared to nominal voltage.

Then the worst-case RMS error due to gate voltage dependency occurs at the maximum gate voltage deviation and for the EPC2031:

$$\frac{\Delta\hat{I}_{vgate,rms}}{I_{FS}} = \frac{1}{\sqrt{2}} \cdot \frac{1}{1-\frac{V_{th}}{V_{gs}}} \cdot \frac{1}{1+\frac{R_{bond}}{R_{mos}}} \cdot \frac{\Delta V_{gs}}{V_{gs}} = \frac{1}{\sqrt{2}} \cdot \frac{1}{1-\frac{2.51\,\mathrm{V}}{5\,\mathrm{V}}} \cdot \frac{1}{1+\frac{1.18\,\mathrm{m\Omega}}{0.82\,\mathrm{m\Omega}}} \cdot 4\,\% = 2\,\% \tag{2.6}$$

2.2.4. Nonlinearity

The parasitic resistance of the switching device is not perfectly linear, which some have named among dominant sources of error [9]. Assuming that nonlinearities scale with resistance changes such that $i = i(v) \cdot R_{nom}/R$, they are best modelled as current errors. Figure 2.5a shows the simulated error compared to a least squares zero-offset linear fit for drain voltages between $-200\,\mathrm{mV}$ and $200\,\mathrm{mV}$ at a junction and case temperature of $25\,°\mathrm{C}$. The voltage was limited to $\pm 200\,\mathrm{mV}$ because higher voltages correspond to power dissipation that would be too high for typical applications.



(a) The nonlinearity remains below 1% over a large current range.

(b) As the maximum current is reduced, the linearity increases.

Figure 2.5: A linear model gives a good approximation of the resistance of the switching devices.

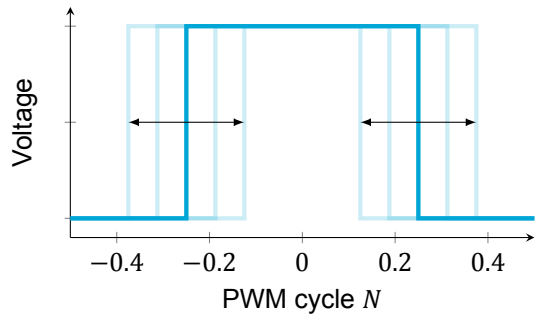
It can be seen that the error remains lower than 1% over a large current range range. As the range of currents is reduced, the i,v characteristics of the switching devices become better approximated by an Ohmic resistance, giving a lower error compared to the full-scale current. This tradeoff is shown in figure 2.5b. For very low current ranges, the simulation model of the EPC2031 exhibits an offset that gives an increased error. Whether this does or does not correspond to reality could be settled by experiment but is not relevant to the current ranges considered in this work.

The usable RMS current range of the devices is about $50\,\mathrm{A}$ for the EPC2031 and $100\,\mathrm{A}$ for the IPT010N08NM5 due to the thermal constraints facing most applications. In this range, the worst-case RMS error due to nonlinearity occurs at $50\,\mathrm{A}$ for the EPC2031 and is given by:

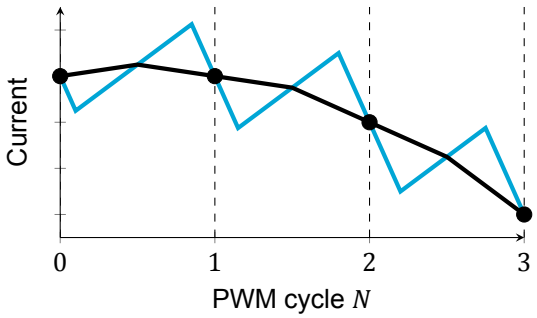
$$\frac{\Delta\hat{I}_{linear,rms}}{I_{FS}} = 0.5\,\% \tag{2.7}$$

2.2.5. Limited access

When the switching devices are disabled, the current starts flowing through a different leg of the inverter and the Vds sensing method can not be applied. Because of this, the current information is masked for large parts of the switching cycle. Though this makes it impossible to recover the full current waveform in the general case, it is fully compatible with the sampling strategy used to extract low-frequency current information that is used in many motor drivers.



(a) The modulation is symmetric around a midpoint.



(b) The ripple is zero at the midpoint.

Figure 2.6: Midpoint sampling nullifies coupling from ripple to current samples.

Generally motor drivers employ midpoint sampling, where the switching moments are centred around the sampling moment. As illustrated in figure 2.6, this aims to ensure no ripple current is present at sampling moment, so that only the 'average' low-frequency current is sampled. In this scheme, the current information is only accessed when Vds sensing is possible, so that the limited access poses only a synchronisation problem [31].

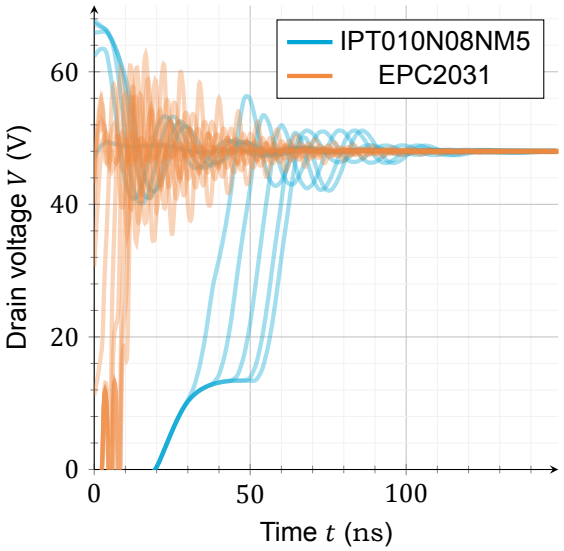
The idea that the instaneous current at the midpoint corresponds to the average current is based on the assumption that the current varies linearly. In practice, nonlinearitites in the current waveform introduce errors [46]. However, these errors are not commonly considered and are not unique to Vds sensing. Hence, they should thus not be considered as part of this analysis.

As such, the worst-case added RMS error due to limited access is insignificant:

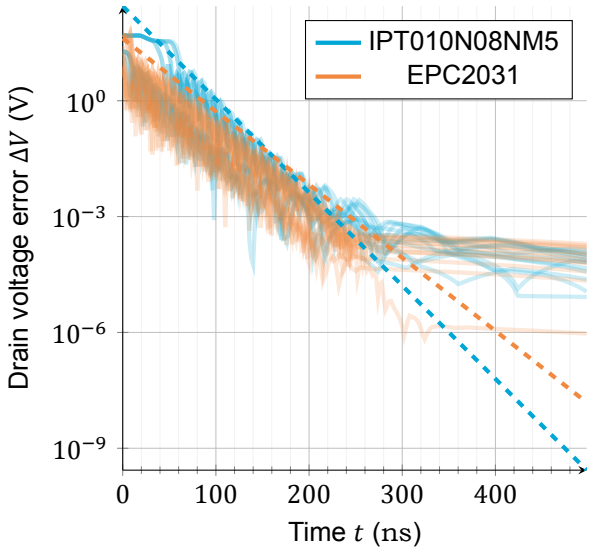
$$\frac{\Delta \hat{I}_{access,rms}}{I_{FS}} < 0.01\,\% \tag{2.8}$$

2.2.6. Ringing

Unmodelled dynamics give rise to ringing following switching transitions. These can be modelled as voltage errors. Figure 2.7 shows the decay of simulated transients during the rising edges in half bridge output stages of simulated switching devices carrying one period of a $1\,\mathrm{kHz}$ $100\,\mathrm{A}$ (IPT010N08NM5) and $50\,\mathrm{A}$ (EPC2031) sine wave.



(a) The ringing dies down rapidly.



(b) The ringing is below millivolt level within $250\,\mathrm{ns}$.

Figure 2.7: Though large transients are created by switching, they die down rapidly.

Figure 2.7a gives an overview of the transients. The difference between hard and soft switching can clearly be seen. Meanwhile, the decay can be reviewed more precisely in figure 2.7b, where the difference with the final value has been plotted on a logarithmic scale. Due to uncertainty in the final value, the error saturates around $0.1\,\mathrm{mV}$. Hence, some trend lines are drawn, which illustrate the expected amplitude of the ringing.

Assuming a settling time of at least $400\,\mathrm{ns}$, the the worst-case RMS error due to ringing occurs at $400\,\mathrm{ns}$ for the EPC2031 and is insignificant:

$$\frac{\Delta \hat{I}_{ringing,rms}}{I_{FS}} = \frac{\Delta V}{R \cdot I_{FS}} = \frac{1\,\mu\mathrm{V}}{2.0\,\mathrm{m\Omega} \cdot 50\,\mathrm{A}} < 0.01\,\% \tag{2.9}$$

2.2.7. Leakage current

When the switches enter the off-state, they pass a leakage current. This leakage current adds as a current error to the sensed phase current. Figure 2.8 shows the simulated leakage current over temperature for a $48\,\mathrm{V}$ bus voltage.

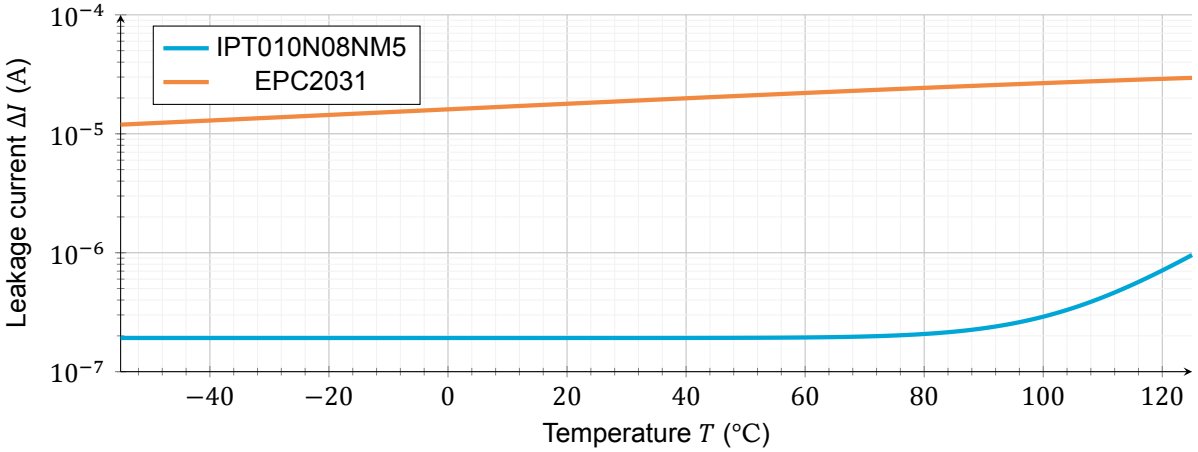


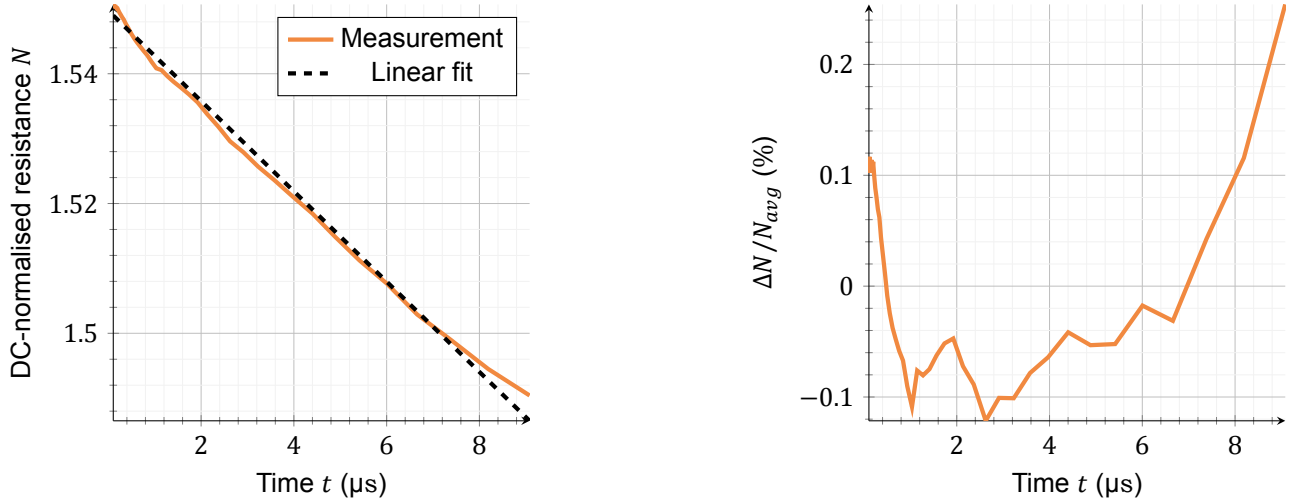
Figure 2.8: The leakage current is low, even as it increases with temperature.

The worst-case RMS error due to leakage occurs at $125\,^{\circ}\mathrm{C}$ for the EPC2031 and is insignificant:

$$\frac{\Delta\hat{I}_{leakage,rms}}{I_{FS}} = \frac{\Delta I}{I_{FS}} = \frac{30\,\mu\mathrm{A}}{50\,\mathrm{A}} < 0.01\,\% \tag{2.10}$$

2.2.8. Dynamic changes in resistance

Changes of the on-resistance with time have been reported for Gallium Nitride (GaN) switching devices [47], with dynamics at the switching frequency. These are best modelled as resistance errors. Though these changes are not incorporated in the simulation models, measurements for the EPC2045 device have been reported [47] and are shown in figure 2.9.



(a) Linear fit to changing resistance

(b) Difference between measurement and fit

Figure 2.9: The dynamic Ron effect is well approximated by a linear slope for short periods. Adapted from the EPC2045 measurements in [47].

It can be seen that the resistance may grow by over 54% compared to DC conditions. Within a $9\,\mu\mathrm{s}$ period the resistance is relatively stable, but still changes by $6\,\%$. As illustrated, the variation is linear over time to within an error of roughly 0.1% for time periods smaller than $8\,\mu\mathrm{s}$. Since the key reason the industry is moving towards GaN switches is to achieve a higher switching frequency, this condition should always be satisfied.

Assuming that the nominal resistance includes dynamic on-resistance effects, the error is given by the changes in on-resistance over changes in operating conditions. There is an effort to characterise the size of such changes for the purpose of efficiency modelling. It has revealed dependencies on pulse length and operating voltage [47]. Extrapolating from figure 2.9a, there may be a change of up to $0.66\,\%\,\mu\mathrm{s}^{-1} \cdot 12.5\,\mu\mathrm{s} = 8\,\%$ for off-times between $0\,\mu\mathrm{s}$ and $25\,\mu\mathrm{s}$ (and midpoint sampling at half the off-time). Furthermore, for a 2:1 input voltage range, the dynamic

resistance may change by up to $20\,\%$. Assuming a nominal resistance in the middle of these changes, the uncertainty is $(8\,\% + 20\,\%)/2 = 14\,\%$

Then the worst-case RMS error due to dynamic changes in resistance can be approximated by:

$$\frac{\Delta\hat{I}_{rdynamic,rms}}{I_{FS}} = \frac{1}{\sqrt{2}} \cdot \frac{|\Delta R|_{max}}{R} = \frac{1}{\sqrt{2}} \cdot 14\,\% = 10\,\% \tag{2.11}$$

2.2.9. Lead inductance

The switching devices contain lead inductance, over which current ramps induce voltages that can be modelled as voltage errors. Figure 2.10 gives a simplified circuit model.

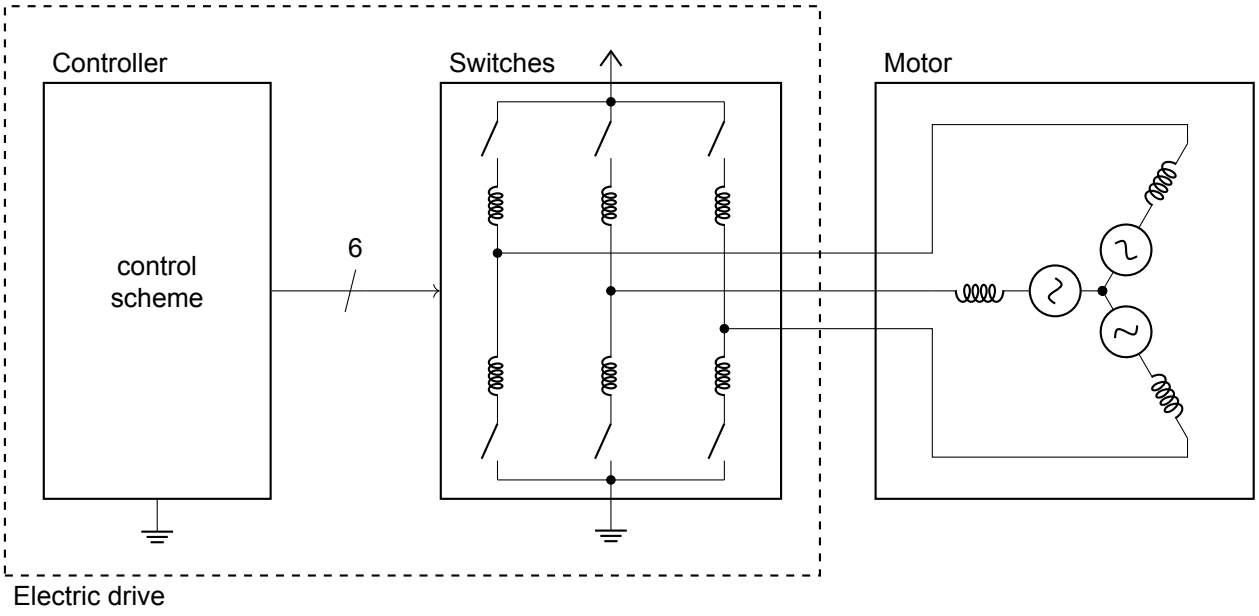


Figure 2.10: Both the back-EMF of the motors and the other inverters create offsets on the lead inductances.

Since the current ramps originate from voltages over the motor inductances, the error voltages can be modelled as the output of voltage dividers formed by the motor and lead inductances. Two voltage sources induce offsets: the back-EMF of the motor and the output voltages of the other inverters. In the worst case, the back-EMF of the motor is equal to the bus voltage, and both other inverters are in the opposite state of the inverter that is being sensed. In that case:

$$\Delta V_L \approx V_{bus} \cdot \frac{2L_p}{3L_w} \tag{2.12}$$

So that the worst-case RMS error due to lead inductance occurs for the IPT010N08NM5 at the minimum motor inductance of $10\,\mu\mathrm{H}$ and the maximum bus voltage of $48\,\mathrm{V}$:

$$\frac{\Delta\hat{I}_{inductance,rms}}{I_{FS}} = \frac{\Delta V}{R \cdot I_{FS}} \approx \frac{V_{bus}}{R \cdot I_{FS}} \cdot \frac{2L_p}{3L_w} = \frac{48\,\mathrm{V}}{0.90\,\mathrm{m\Omega} \cdot 100\,\mathrm{A}} \cdot \frac{2 \cdot 3\,\mathrm{nH}}{3 \cdot 10\,\mu\mathrm{H}} = 11\,\% \tag{2.13}$$

2.2.10. Noise

Noise poses a fundamental limit to the information that can be extracted from any system. The noise can be modelled as a current error due to thermal noise:

$$\bar{\Delta I^2} = \frac{4kT}{R} \cdot B \tag{2.14}$$

In which B is the noise bandwidth of the measurement, which is limited by the parasitic dynamics of the inverter, which form a RLC filter. The bandwidth can be estimated as:

$$B_{IPT} \approx \frac{1}{2\pi \cdot \sqrt{LC}} = \frac{1}{2\pi \cdot \sqrt{3\,\mathrm{nH} \cdot 3\,\mathrm{pF}}} = 1.7\,\mathrm{GHz} \qquad B_{EPC} \approx \frac{1}{2\pi \cdot \sqrt{LC}} = \frac{1}{2\pi \cdot \sqrt{0.5\,\mathrm{nH} \cdot 0.5\,\mathrm{pF}}} = 10\,\mathrm{GHz}$$

Where the small contribution above the cutoff frequency was ignored for a first approximation.

Then the worst-case RMS error due to noise occurs for the EPC2031 at $125\,^\circ\mathrm{C}$ and is insignificant:

$$\frac{\Delta\hat{I}_{noise,rms}}{I_{FS}} \approx \frac{1}{I_{FS}} \cdot \sqrt{\frac{4kT}{R} \cdot B} = \frac{1}{50\,\mathrm{A}} \cdot \sqrt{\frac{4 \cdot 1.38 \cdot 10^{-23}\,\mathrm{J\,K^{-1}} \cdot 400\,\mathrm{K}}{2\,\mathrm{m\Omega}} \cdot 10\,\mathrm{GHz}} < 0.01\,\% \tag{2.15}$$

2.3. Conclusion

Table 2.1 summarises the worst-case error contribution of various effects. Gate voltage dependency and nonlinearity have often been named as sources of error, but even in the worst case are not limiting in practice. Similarly, though lead inductance and dynamic changes in resistance have not traditionally been considered major sources of error, in some cases they may be among dominant error sources. Nevertheless, it should be noted that they may not be for many devices and in many operating conditions because they represent the worst-case. However, for the large range of devices and operating conditions encountered in the application of motor drivers, the worst case is likely to be encountered.

Table 2.1: Impact of potential error sources (arranged in descending order of importance).

Effect	**Worst-case MSE (% FS)**	**Notes**
Temperature dependence	45	
Production tolerance	21	
Lead inductance	11	
Dynamic changes in resistance	10	Only occurs in GaN devices
Gate voltage dependency	2	
Nonlinearity	0.5	
Ringing	< 0.01	Provided the settling time exceeds $400\,\mathrm{ns}$
Leakage current	< 0.01	
Limited access	< 0.01	
Noise	< 0.01	

3

Architecture design

3.1. Choice of error suppression method

Several approaches could be considered to suppress the errrors found in chapter 2.

In single-point calibration, errors are measured at fabrication time and subsequently compensated. This compensates for the fixed production tolerance, but not dynamic errors. Ideally, the production tolerance is fully suppressed. In reality, the suppresion will be limited by degradation.

In temperature compensation, the temperature dependency is corrected with an estimate of the error based on a temperature measurement or estimate. Ideally, this method fuly suppresses the temperature dependency error. In reality, the suppression is limited by errors in the temperature estimate and the model of the temperature dependency.

Linear feedback of the resistance error can be used to suppress all linear resistive errors. Lead inductance effects are not suppressed since they do not originate from the resistance. Nonlinear effects also cannot be compensated due to the linear nature of the feedback. Ideally, all resistive errors are fully supressed. In reality, the suppresion is limited by the bandwidth of the feedback and errors in the resistance measurement.

With lead inductance compensation, the voltage over the lead inductance could be corrected with an estimate based on an uncorrected output currente estimate, the measured bus voltage, the known state of the inverters, and a model of the load behaviour. Ideally, the error due to lead inductance is fully suppressed. In reality, the suppresion is limited by the errors in the the model of the load behaviour.

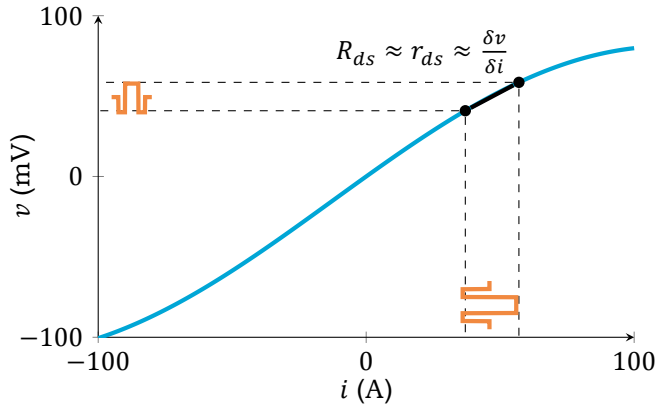
Table 3.1: Even with ideal performance, no single error suppression method achieves the desired suppression of the worst-case RMSE in % FS.

Effect ↓ method →	Unsuppressed	Single-point calibration	Temperature compensation	Linear feedback	Lead compensation
Temperature dependence	45	45	0	0	45
Production tolerance	21	0	21	0	21
Lead inductance	11	11	11	11	0
Dynamic changes in resistance	10	10	10	0	10
Gate voltage dependency	2	2	2	0	2
Nonlinearity	0.5	0.5	0.5	0.5	0.5
Total	89.5	68.5	44.5	11.5	78.5

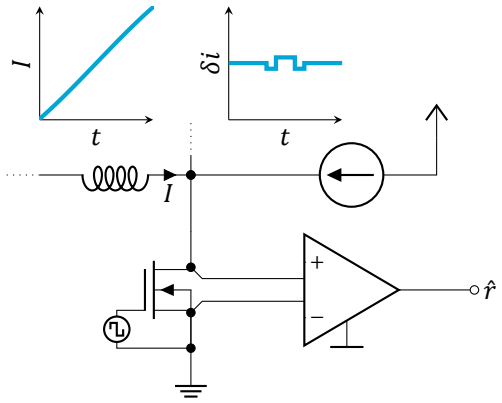
As tabulated in table 3.1, even with ideal behaviour no single method can achieve the desired performance. In silicon devices, a combination of single-point calibration and compensation methods may achieve the desired performance. However, the suppresion would not be robust to degradation and the method is not applicable to GaN devices. In contrast, a method based on the combination of linear feedback and lead inductance would not only achieve the desired performance, but be applicable to GaN devices and have robustness to degradation. Hence, it will be adopted here.

The adopted methods will now be considered more closely.

3.1.1. Linear resistance feedback



(a) R_{ds} is estimated from r_{ds} through an injected current δi.



(b) The measurement requires current injectionand voltage sensing.

Figure 3.1: The big idea is to estimate the current I from the drain source voltage V through on-line measurement of the small-signal resistance.

Linear resistance feedback depends on a measurement of the resistance. However, resistance is not a quantity that can be directly observed. It is only meaningful as the response to some excitation. Hence, measuring the resistance requires observing the response to some test signal applied to the channel resistance of the switching device.

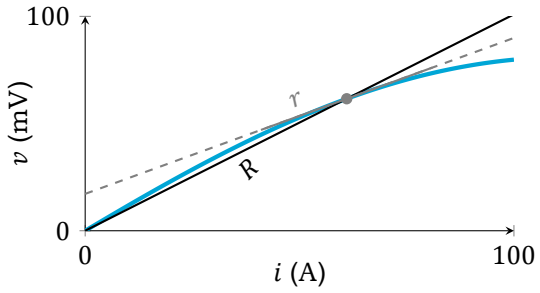
There are several methods that could be used to generate this test signal. As motivated in section 1.1.4, current injection at the switching node is the most promising method in terms of accuracy, stability, and bandwidth.

The key idea is to use continual measurements of the small-signal resistance r_{ds} of the switching device as an estimate of the large signal resistance R_{ds}. r_{ds} is measured through finding the amplitude of the small voltage pulse δv in response to a known small injected current pulse δi, as illustrated in figure 3.1a. This requires current injection and voltage sensing, as illustrated in figure 3.1b.

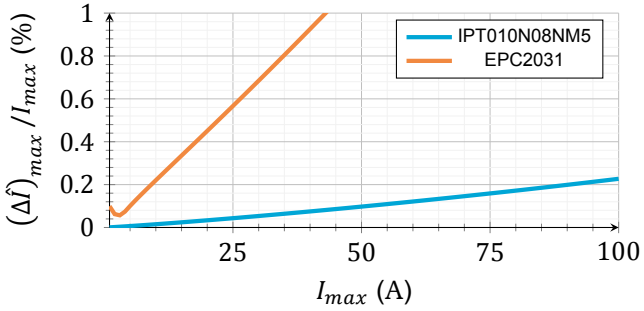
This method inherently comes with several errors. These will now be considered in more detail.

Linearity assumption

The method is based on the idea that the small-signal drain-source resistance r_{ds} is a good approximation of the large signal resistance R_{ds}. This is true for linear resistors. However, this assumption is only true to within a certain accuracy for practical switching devices. This will create a resistance error, as illustrated in figure 3.2a.



(a) The large signal and small signal resistances differ due to nonlinearity, giving rise to an error.



(b) As the maximum current is reduced, the linearity increases.

Figure 3.2: The linearity assumption comes with an inherent error, but it is manageable.

The error can be quantified in terms of the maximum deviation with respect to the full scale current:

$$\Delta \hat{I}_{linear} < I_{max} \cdot \frac{(r-R)_{max}}{R} \quad \Rightarrow \quad \frac{\Delta \hat{I}_{max}}{I_{max}} = \frac{(r-R)_{max}}{R} \tag{3.1}$$

Thanks to the roughly linear behaviour of the resistance, the small signal resistance is a good estimate of the large signal resistance.

Insufficient tracking of thermal ramps

During operation, the switching devices dissipate power causing temperature variations. Due to the temperature dependency of the switch resistance, this in turn causes the resistance to fluctuate. Depending on the interval between resistance measurements, a significant error may be accumulated compared to the last estimate.

Quantifying the error requires quantifying the temperature fluctuations. This can be accomplished with a thermal model of the switching device. Though modelling the exact behaviour for a dynamic power flow creates an unwieldy result, an upper bound can be found. As shown in appendix A.2 the resistance error is:

$$\Delta\hat{R}_{thermal} < \left(\frac{\partial R}{\partial T}\right)_{max} \cdot \min_i P_{max} \cdot \left(\frac{1}{\Delta t_{sample,R} \cdot \sum_{k=0}^{i} C_k} + \sum_{k=0}^{i} R_k\right) \tag{3.2}$$

Voltage offsets & low-frequency noise

Voltage errors due to offset and low frequency noise in the voltage measurement path directly translate to current offsets and low-frequency noise. The resulting current error is given by:

$$\left(\Delta\hat{I}\right)_{offset} = \hat{I} \cdot \frac{\Delta\hat{V}}{\hat{V}} = \frac{v_{off}(t)}{R} \tag{3.3}$$

In which v_{off} is the offset voltage, including low-frequency noise, in V.

Gain mismatch between voltage and resistance estimation paths

Fabrication tolerances will inevitably cause gain mismatches between the voltage and resistance measurements. This combination of voltage and resistance errors will create gain errors in the estimated current, which can be estimated from the error model:

$$\Delta\hat{I}_{mismatch} = \hat{I} \cdot \left(\frac{\hat{V} \cdot \Delta G_v}{\hat{V}} - \frac{\hat{r} \cdot \Delta G_r}{\hat{r}}\right) = \hat{I} \cdot (\Delta G_v - \Delta G_r) \tag{3.4}$$

3.1.2. Lead inductance compensation

The voltage errors over the lead inductances can be compensated using post-processing. This requires a rough estimate of the motor to lead inductance voltage division ratio, defined as the ratio of voltage offset over one of the connected lead inductances to a voltage source in series with either of the other phases, as illustrated in figure 3.3. Note that this ratio is independent of the inverter output states. It can be measured during design time.

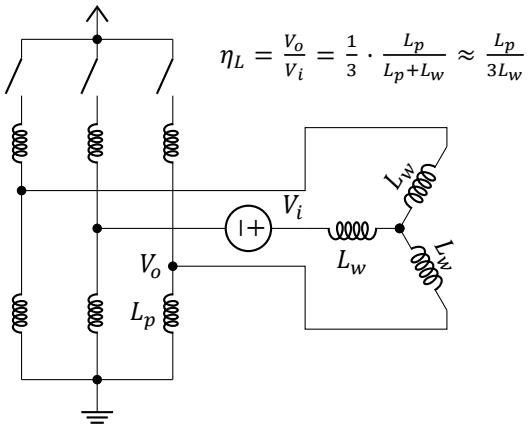


Figure 3.3: η_L is the ratio of voltage offset over the connected lead inductance to a voltage source in series with either of the other phases.

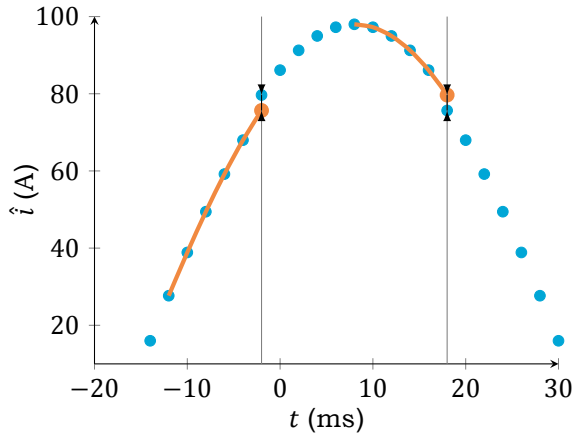


Figure 3.4: The inductance voltage division ratio can be measured from the jump in estimated current around an inverter state transition.

The compensation also requires knowledge of the back-EMF. Its estimation is already part of many motor control algorithms. If an estimate is not already available, it is also possible to estimate the back-EMF from the derivative of current estimate, duty cycle history, and a rough estimate of the motor inductance.

The offset contributions due to inverter outputs and the back-EMF are calculated using the voltage division ratio, estimated back-EMF and a measurement of the bus voltage. They are then subtracted from the raw measurements, compensating for the errors over the lead inductances of the switching devices. The motor inductance will in general be different than estimated due to unit-to-unit mismatch, core saturation effects, the rotation of the motor, and temperature dependency. However, a large certainty is not needed. Even if the estimate is off by $\pm 10\%$, the lead inductance errors can be suppressed by an order of magnitude. Nevertheless, some computation power can be used to refine the estimate through measurements of the division ratio from jumps in the estimated current compared to the quadratic trend before an inverter output transition, as illustrated in figure 3.4. Alternatively, a single point calibration can be performed at fabrication time to cancel unit-to-unit mismatch.

Residual offset over the lead inductance

The lead inductance voltage offset compensation is never perfect, so that a residual offset exists. This manifests as a voltage error as modelled in section 2.1. Since the compensation voltage scales with the inductor ratio, the voltage error can be expressed in the inductor ratio error:

$$\left|\Delta\hat{I}\right|_{lead} = \hat{I} \cdot \frac{\Delta\hat{V}}{\hat{V}} < \left|\hat{I} \cdot \frac{2 \cdot V_{bus} \cdot (\eta_L - \hat{\eta}_L)}{\hat{V}}\right| = \frac{2 \cdot V_{bus}}{R} \cdot |\Delta\hat{\eta}_L| \tag{3.5}$$

3.2. Choice of detector

Two measurements are made to implement Vds sensing. One is of the Vds voltage, the other of the resistance. The resistance measurement is the most constraining, since it involves measuring the voltage created by an injected current that is only a fraction of the load current that causes the Vds voltage. The voltage measurement can be a simplified version of the resistance measurement. Hence, the focus will be on the resistance measurement.

Injecting the resistance test signal requires power. Since this power is wasted, it is desirable to keep it to a minimum. This increases the total power efficiency of the system and also decreases the power handling requirements of the injection source. In contrast, observation will come with noise. Since a lower noise will - all other things being equal - require more resources such as power and size, it is desirable to be able tolerate the maximum amount of noise.

These are contradictory requirements: larger test signals can be spotted in larger amounts of noise, whereas strict noise tolerances enable the detection of small test signals. Hence, it is important to make efficient use of the injected signal by optimising the signal chain. This starts at the detector.

Since the electrical dynamics of the switching device must be quicker than the switching dynamics, the voltage over the switching element in the blocking phase is not meaningfully related to the current, and the behaviour of the closed switch is nearly linear, the switching device can be modelled as a variable linear resistor with intermittent access.

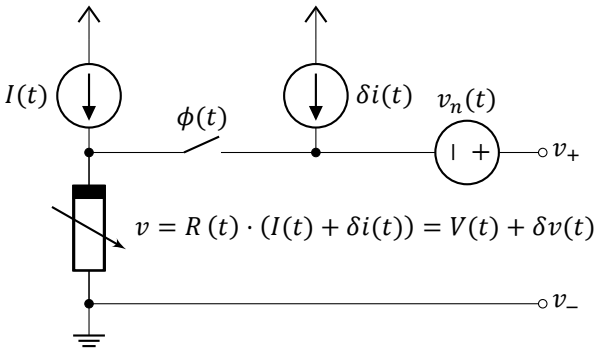


Figure 3.5: Model of the detection problem.

The detection problem can be modelled as shown in figure 3.5, where the size of the response δv of the unknown time-dependent resistance $R(t)$ to a small known current $\delta i(t)$ must be determined in the presence of an additive white Gaussian input noise voltage $v_n(t)$ and an unknown bulk current $I(t)$. Ideally, the signal to noise ratio for a given injected power is maximised.

A near-optimal detector for this problem can be found through a perturbation argument. Say that $\phi(t) = 1, I(t) = 0$, and $R(t) = R$ is constant, then the optimal detector is given by the matched filter [48], with a time-domain description of:

$$\hat{R} = \frac{\int_{-T}^{T} \delta i(t) \cdot v(t)\,\mathrm{d}t}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t}$$

In which $[-T, T]$ is the support of the injected current. The Signal to Noise Ratio (SNR) is independent of the shape of δi and is given by:

$$\mathrm{SNR} = \frac{2E}{N_0} = \frac{2R^2 E_i}{N_0}$$

In which E is the normalised voltage energy of the applied signal, E_i is the normalised current energy of the applied signal δi, and N_0 is the single-sided input voltage noise density. The distribution of the associated resistance estimation error can be found from the SNR:

$$\Delta\hat{R} \sim \mathcal{N}\left(0, \frac{R^2}{\mathrm{SNR}}\right) = \mathcal{N}\left(0, \frac{N_0}{2E_i}\right) \tag{3.6}$$

3.2.1. Effect of intermittent access

In reality $\phi(t)$ changes with time, so that the access to the resistor is intermittent. When the switch is open, no information can be gained about the resistance. If $\Delta i \neq 0$ when $\phi = 0$, this breaks one of the preconditions for the matched filter, and the detector is not optimal. However, if $\delta i = 0$ when $\phi = 0$, the detector is essentially blind to what happens when the switch is open, so that the output is unaffected. Since the performance is independent of pulse shape, this still gives optimal performance. Hence, a proper choice of injected signal the matched filter is an optimal detector.

3.2.2. Effect of bulk current

In reality, $I(t) \neq 0$, which creates interference with the detector. The magnitude of this interference can be found from the time-domain description of the matched filter:

$$\Delta\hat{R} = \frac{\int_{-T}^{T} \delta i(t) \cdot R \cdot I(t)\,\mathrm{d}t}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} = \frac{R}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} \cdot \int_{-T}^{T} \delta i(t) \cdot I(t)\,\mathrm{d}t$$

For the zero interference condition $\Delta\hat{R} = 0$, the injected current must be orthogonal to the bulk current $\int_{-T}^{T} \Delta i(t) \cdot I(t)\,\mathrm{d} = 0$. Hence, for a proper choice of injected signal, the matched filter is an optimal detector.

3.2.3. Effect of resistance changes

In reality, $R(t) \neq R$. Changes in temperature and dynamic changes in on-resistance will cause changes in resistance with dynamics near harmonics of the modulated signal frequency, so that $R(t) = R(0) + \delta R(t)$. This interferes with the detector. There are two effects, which will now be considered.

First, the changes in resistance will create changes in voltage, giving an error of:

$$\Delta\hat{R} = \frac{\int_{-T}^{T} \delta i(t) \cdot \delta R(t) \cdot I\,\mathrm{d}t}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} = \frac{I}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} \cdot \int_{-T}^{T} \delta i(t) \cdot \delta R(t)\,\mathrm{d}t$$

Like with the bulk current, for the zero interference condition $\Delta\hat{R} = 0$, the injected current must be orthogonal to the bulk current $\int_{-T}^{T} \delta i(t) \cdot \delta R(t)\,\mathrm{d}t = 0$. Hence, for a proper choice of injected signal, the matched filter is an optimal detector. The same argument holds for mixing effects with the bulk current.

Second, the resistance becomes a moving target, so that the measurement may not accurately reflect a single sample. The associated error in resistance is given by:

$$\Delta\hat{R} = \frac{\int_{-T}^{T} \delta i(t) \cdot \delta i(t) \cdot R(t)\,\mathrm{d}t}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} - R(0) = \int_{-T}^{T} \frac{\delta i(t)^2}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} \cdot R(t)\,\mathrm{d}t - R(0) = \int_{-T}^{T} \frac{1}{\int_{-T}^{T} \delta i(t)^2\,\mathrm{d}t} \cdot \delta i(t)^2 \cdot \delta R(t)\,\mathrm{d}t$$

Which is the difference between the instantaneous value and the weighted average of the resistance. For the zero error condition $\Delta\hat{R} = 0$, the square of the injected current must be orthogonal to the changes in resistance $\int_{-T}^{T} \delta i(t)^2 \cdot \delta R(t)\,\mathrm{d}t = 0$. Hence, for a proper choice of injected signal, the matched filter is an optimal detector.

3.2.4. Constraints due to unmodelled effects

Dynamics In reality, various dynamic elements surround the switching device, which will cause ringing that is not modelled, as discussed in section 2.2.6. These effects can be blocked by setting the injected current to 0 in the detector while in reality already applying the current, giving a settling time. This is no longer an optimal detector, as there is inefficiency since fraction of power needed to injected current during the settling time is wasted according to $\eta_{settle} = 1 - T_{settle}/T_{measurement}$. However, the performance remains near-optimal for a sufficiently small settling time. As discussed in section 2.2.6, such $T_{dead} \approx 400\,\mathrm{ns}$ dead band times are achievable. As shown in section 3.4.2, the system-level performance is optimised for $\eta_{settle} = 0.5$, so that the performance of the detector is reduced by no more than a factor of $2\times$ compared to the optimum

Lead inductance Changes in bulk current will create voltages over the lead inductance, which can interfere with the detector. The argument about interference due to bulk current over the resistance holds for these contributions.

Pink noise $1/f$ noise was ignored in the derivation of this detector, but could introduce additional error. However, the zero interference conditions imply that the detector is insensitive to DC offsets, and thus low frequencies. Hence, the pink noise can be expected to not significantly affect the output of the detector and ignoring it is justified.

3.2.5. Enhancement by filtering

Though the matched detector gives near-optimal instaneous measurement of a single injected pulse, the combination of these measurements may not be an optimal representation of the signal. For example, for a constant signal the average of the measurements is a much better representation of the signal than the time sequence of instaneous measurements. Similarly, for a bandwidth-limited signal a filtered sequence more closely matched the underlying signal. Assuming sampling above the nyquist rate and perfect reconstruction, the signal to noise Power Spectral Density (PSD) ratio of a uniformly sampled sequence of measurements at a sampling frequency f_s is:

$$\frac{P_s}{\partial P_n/\partial f} = \frac{f_s}{2} \cdot \frac{2R^2 E_i}{N_0}$$

So that for filtered version of the signal the SNR is:

$$\mathrm{SNR} = \frac{f_s \eta_f}{2B} \cdot \frac{2R^2 E_i}{N_0} = \eta_f \cdot \frac{R^2 P_i}{N_0 B}$$

In which $\eta_f = B/B_{noise}$ is an optimality factor of the filter, with $\eta_f \leq 1$, and $\eta_f = 2/\pi$ for a first order time-continuous filter. It can be seen that the SNR is dependent on the normalised injected current power P_i rather than the pulse energy. This shows that the amount of pulses is not important to the SNR, only the rate of energy delivered. Hence, a system based on a matched detector achieves the same performance as a continuous-time system with equivalent bandwidth.

3.2.6. Conclusion

All in all, the matched filter is not an optimal solution to the intermittent resistance detection problem. Settling of unmodelled dynamics limits the amount of signal captured and more noise is captured due to the presence of pink noise. However, despite these adverse effects, under reasonable orthogonality constraints on the injected current there is no significant room for improvement over the matched filter. Furthermore, efficient implementation exist, such as using a multipler and integrator, as shown in figure 3.6. Hence, it is adopted here.

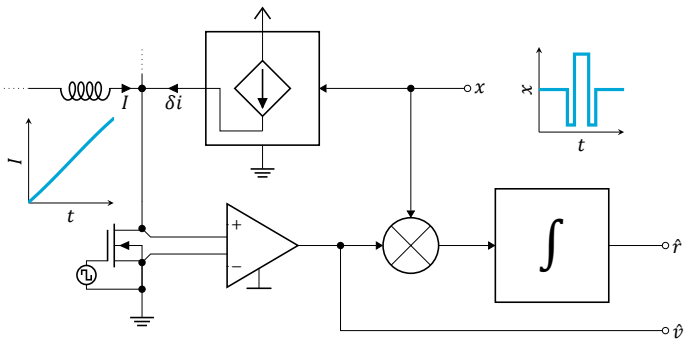


Figure 3.6: A correlator is used to find the amplitude of the small signal voltage pulse δv.

This has several implications for the design.

First of, the performance of the system is independent of the shape of the injected current, only its power. Second, this shape must adhere to several orthogonality constraints:

$$\int_{-T}^{T} \left|\delta i(t)\right| \cdot \bar{\phi}(t)\,\mathrm{d}t = 0 \qquad \int_{-T}^{T} \delta i(t) \cdot I(t)\,\mathrm{d}t = 0 \qquad \int_{-T}^{T} \delta i(t) \cdot \delta R(t)\,\mathrm{d}t = 0 \qquad \int_{-T}^{T} \delta i(t)^2 \cdot \delta R(t)\,\mathrm{d}t = 0 \tag{3.7}$$

In addition, a settling time $T_{settle} > 400\,\mathrm{ns}$ must be observed.

3.3. Injected current signal shape

3.3.1. Signal class

For a constant injected power, the shape of the injected signal does not influence the SNR of the measurement. However, the shape can influence the performance to cost ratio of the system. In particular, signal shapes may be grouped in four classes, depending on the continuous or pulsed operation and continuous or discrete amplitude. Representatives of these classes are illustrated in figure 3.7.

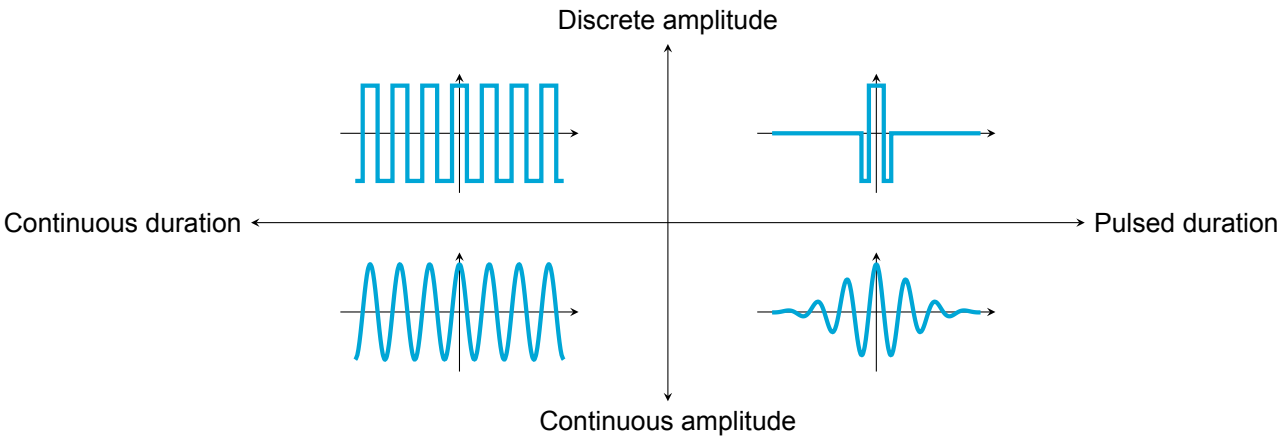


Figure 3.7: Signal shapes may be grouped depending on continous or pulsed duration and continuous or discrete amplitude.

Since resistance information is only available in one of the switching phases, continuous signals introduce a mixing behaviour with the duty cycle. This introduces an unnecessary problem, and is thus best avoided. Furthermore, there are several reasons to prefer discrete amplitudes over continous amplitudes. First, the generation and detection can be efficiently implemented using switches and chopped integrators. Second, the power delivery capability of the injection power stage can be fully used. Hence, discrete amplitude pulsed signals are adopted here.

3.3.2. Satisfying constraints

Orthogonality to inverter output

The shape of the injected signal must be orthogonal to several signals. First, its absolute value must be orthogonal to the output of the inverter $\bar{\phi}(t)$. This is a center-aligned Pulse Width Modulation (PWM) signal with a varying duty cycle. Orthogonality requires the injected pulse length to fit inside of the low period of this PWM signal.

There is a tradeoff between the length of this measurement window and the duty cycle range over which resistance measurements can be performed. For a given maximum current amplitude, longer injection lengths impart more energy giving a better SNR. However, a longer injection length also gives a smaller maximum duty cycle. As discussed in section section 3.4.2, the optimum measurement time is roughly as long as the settling time of the system. Hence, good performance can be attained for a small decrease in modulation range. Furthermore, a full modulation range can be maintained when the 'blind' current is estimated using the current measurement from two other phases, such as used to avoid blind spots in leg shunt current measurements [12]. Finally, note that the measurement window need not be contiguous and constrained to a single cycle. A the injected signal could be spread over pulses in multiple fixed duty cycle PWM cycles to allow more measurement time. This is particularly relevant to the high switching frequencies the industry is moving towards.

There is also the option to adapt the length of the measurement signal to the available time. This improves the SNR for lower duty cycles, at the cost of added complexity. Yet, this method has the same worst case RMSE as a constant-time approach. Hence, the constant time approach is adopted here for its simplicity.

Orthogonality to bulk current and resistance errors

The injected signal is required to be orthogonal to the bulk current $I(t)$ and resistance error $\delta R(t)$. In general, these signals consist of a complex combination of time-varying distorted sinusoids and sawtooth waves. However, any signal becomes well approximated by its Nnth order Taylor polynomial for sufficiently short timespans. Hence, any signal that is orthogonal to polynomials of sufficiently high orders will have the required orthogonality properties.

As confirmed by the outline of a proof in appendix A.4, such signals can be found for any base pulse shape and any polynomial order N by repeated application of shifting, mirroring and rotatating. The procedure starts with a base pulse shape. To make it orthogonal to 0th order polynomials (constant values), the start of the signal is right-aligned with the zero axis. Then, a $180°$ rotated version is added to it. To make it orthogonal to 1st order polynomials (offset ramps), the resulting signal is again right-aligned with the zero axis and its mirror image along that axis is added. For orthogonality with higher order polynomials, rotation is applied for odd orders and mirroring for even orders. The resulting signals for a unit pulse base shape are shown in figure 3.8.

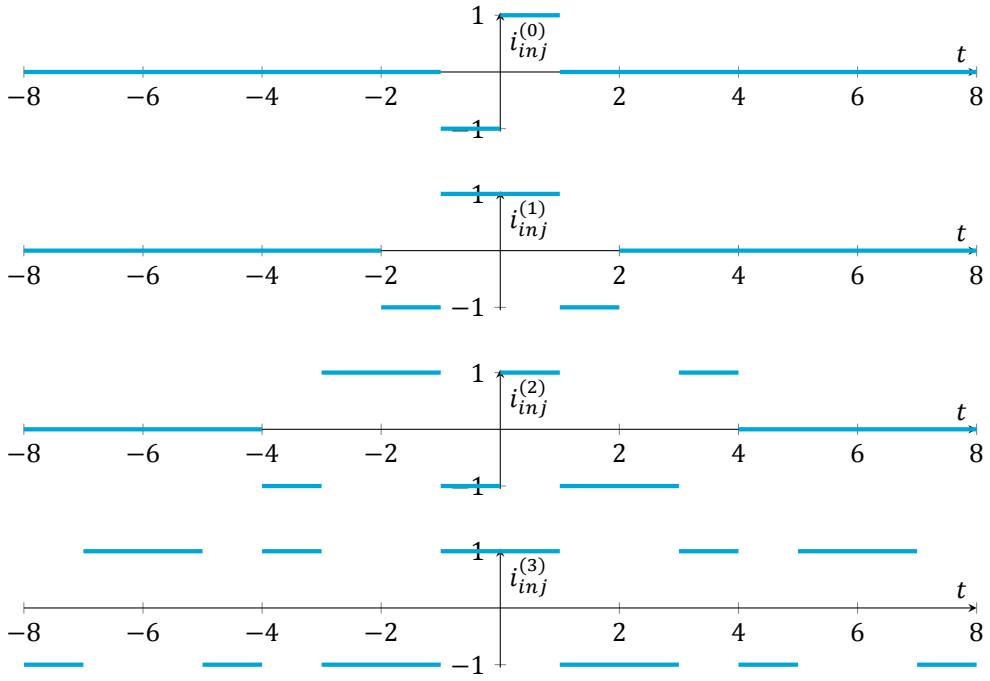
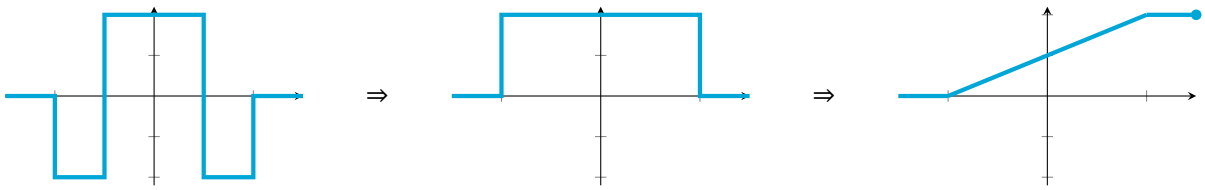
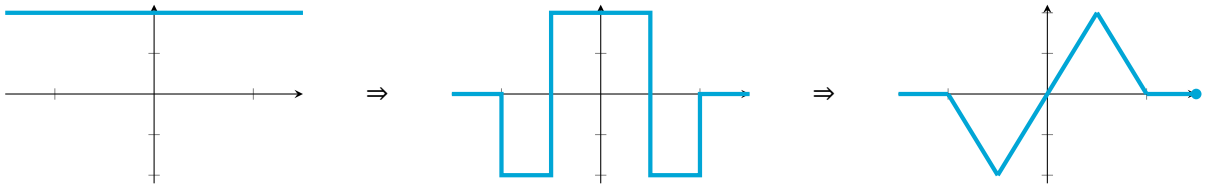


Figure 3.8: Signals orthogonal to first 4 orders of polynomials can be constructed from unit pulses.

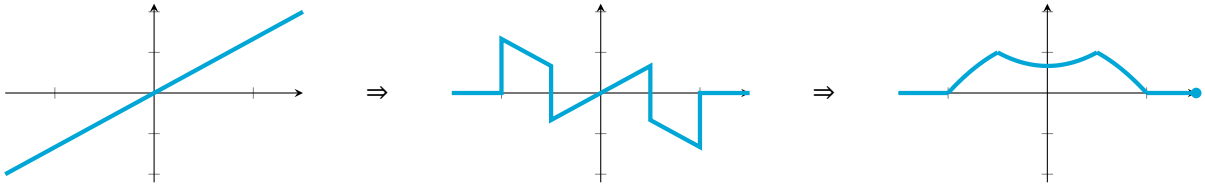
Since every edge comes with ringing and thus additional time and power overhead incurred due to dead time, the amount of edges should be minimised. For a given order N, the use of the unit gate pulse as the base pulse shape achieves this goal, as it has the minimal amount of edges of any discrete base pulse shape. To further minimise the edges, the order N should be minimised.



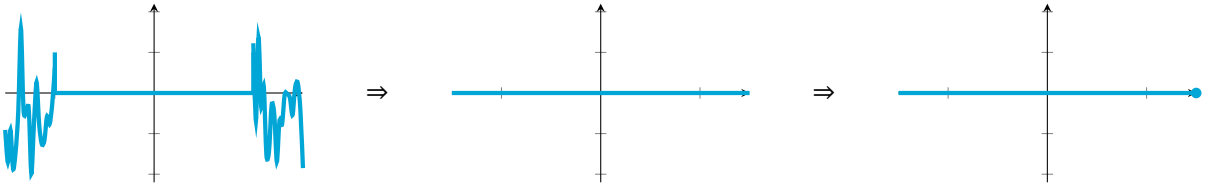
(a) Nominal operation results in a nonzero output at the end of the measurement.



(b) The injected signal is orthogonal to constant offsets which thus result in zero output at the end of the measurement.



(c) The injected signal is orthogonal to ramps which thus result in zero output at the end of the measurement.



(d) The injected signal is orthogonal to signals outside its support which thus result in zero output at the end of the measurement.

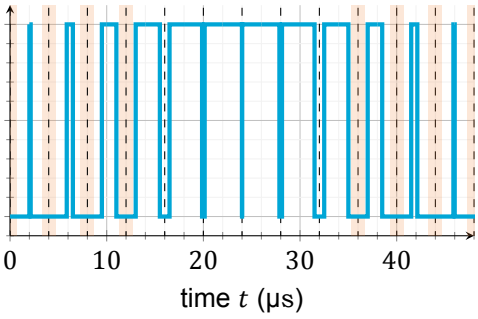
Figure 3.9: The down-up-up-down pulse is orthogonal to offset linear interference. On the left, various input signals are shown. In the middle, the product with the down-up-up-down pulse is shown. On the right, the running integral of the signals is shown. The sampling moment is indicated with a dot, with the vertical deflection corresponding to the result of the measurement.

The measurement window is generally short enough to make even low order Taylor expansions a good approximation of the bulk current and resistance error. During the low state of the inverter the bulk current consists of a relatively slowly varying sinusoidal load current along with a linear ramp of ripple current, barring small nonlinearities caused by core saturation effects. The resistance error similarly consists of relatively slowly varying thermal components due to the load current along with a relatively linear ramp due to dynamic on resistance effects. In fact, from the model of the slow variation of the bulk current in section 3.3.4, the model of the slow variation of the resistance in appendix A.3, and the data about the dynamic on-resistance in section 2.2.8, and assuming linear ripple, the signals can be modelled with a 1st order polynomial to within $0.1\,\%$. Hence,the 1st order down-up-up-down pulse is sufficiently orthogonal to the interference signals, as illustrated in figure 3.9.

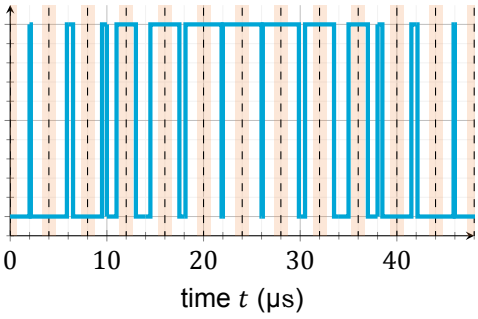
Impact on modulation

If any of the other phases change its output the measurement window, there is an abrupt change in the ramp rate of the ripple current as well as a step in offset over the inductive offset. These signal shapes can not be easily suppressed and should thus be avoided.

A simple solution is to to perform the measurement during a period where none of the phases are switching. As illustrated in figure 3.10a, the switching moments of conventional center-aligned PWM fall within the duration of the measurement period at low duty cycles. Not only does this block the ability to perform a resistance measurement in this phase, it also creates unacceptably large interference in the two other phases. One solution to this problem is to keep always keep the duty cycle low enough to not cut into the measurement window. However, this comes at the cost of modulation range. With a small change to the modulation method, the inverter switching events can always be placed outside the measurement window. This way, no interference is generated and two phases can always be used to measure current.



(a) Conventional center-aligned PWM cuts into the measurement window.



(b) Flipover at $t = 10\,\mu s$ and $t = 38\,\mu s$ for $D = 50\%$ preserves the window.

Figure 3.10: Inverting the modulation preserves a clean measurement window. The control signal of the class D stage is shown in cyan, with the measurement windows in translucent orange.

As illustrated in figure 3.10b, the approach relies on a single rule: whenever the switching events would fall inside of the measurement window, invert both the active value of the phase and the duty cycle. This preserves the average value of the signal, but centers the high part of the signal on the measurement window, which is much longer than the measurement window. Essentially, the modulation 'flips over'. This scheme introduces an additional switching event where the flipover occurs. This slightly increases switching losses, but not to a significant extent since the flipover happens infrequently. The output signal is also not significantly distorted as the flipover occurs when the ripple current crosses 0.

Orthogonality to resistance bias

The square of the injected signal is required to be orthogonal to the resistance error $\delta R(t)$. Since this error is purely linear to within $0.1\,\%$, it point-symmetric to within an acceptable error. Then any symmetric signal is orthogonal to it. The square of signals constructed with the procedure described in the last section are always symmetric because $(\pm x)^2 = x^2$, which changes the square value of a roated signal into the mirrored squared signal. Hence, this constraint is satisfied.

Settling time

As discussed in section 3.2.4, a deadband is needed to suppress errors due to ringing. This can be achieved by setting the correlation signal to zero at times of significant ringing and settling while not altering the injection signal. As illustrated in figure 3.11, this requires the injected current to become different from the correlation signal.

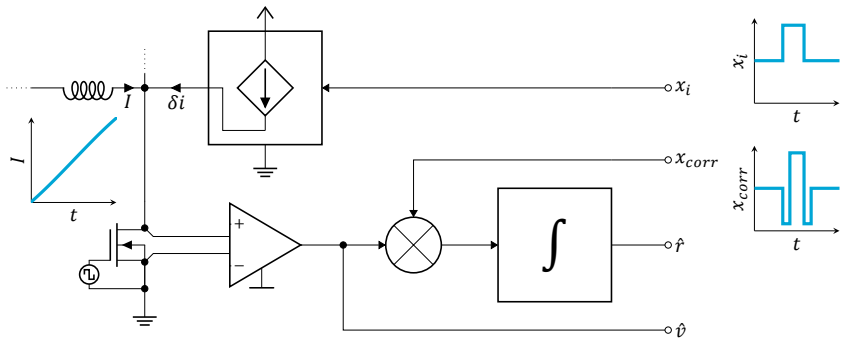
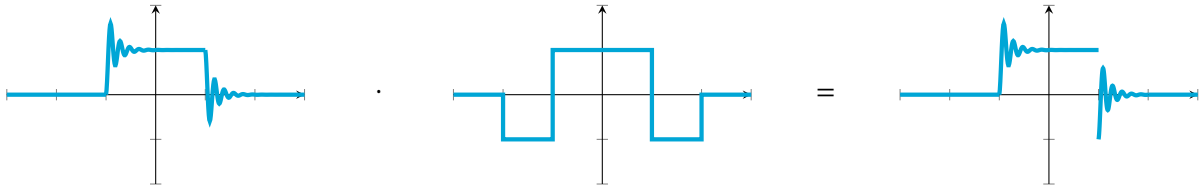
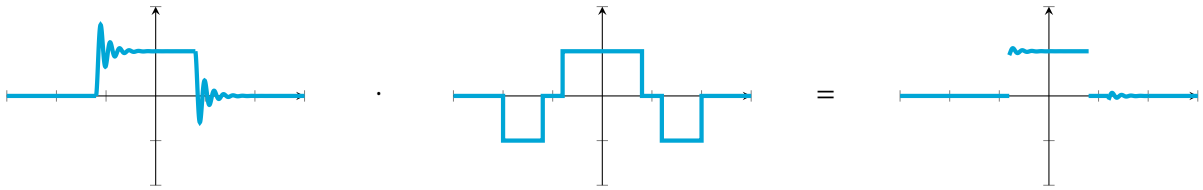


Figure 3.11: The injected current is different from the correlation signal.

As illustrated in figure 3.12, this scheme suppresses errors due to ringing. The orthogonality properties are preserved when these blanking periods are added.



(a) Without blanking, the correlator experiences significant interference.



(b) With blanking, the interference experienced by the correlator is suppressed.

Figure 3.12: Blanking periods are used in the correlation signal to prevent ringing interfering with the measurement.

3.3.3. Simplifying the injected signal

The injected current signal can be simpler than the correlation signal. Thanks to the orthogonality properties of the correlation signal, a simple unipolar current pulse has the same performance as a down-up-up-down pulse. Since the detector is insensitive to constant offsets, an offset current can be added to the injected current. This makes the injection current source unipolar rather than bipolar. Setting the current outside the support of the injected signal to 0 reduces the amount of levels from 3 to 2.

3.3.4. Error susceptibility

The selected pulse shape comes with various error sources, that will now be discussed.

Noise

The noise on the input voltage will impart a stochastic error on the measurement, as illustrated in figure 3.13.

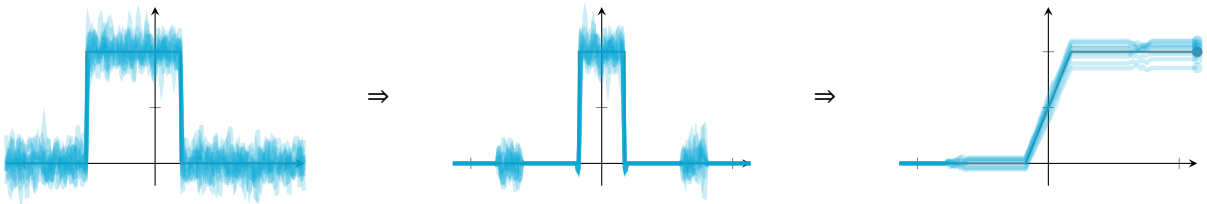


Figure 3.13: Noise imparts a stochastic error (10 realisations shown, exagerrated).

The effect of the error is best understood in terms of its variance, which is given by:

$$\mathrm{Var}\left(\left(\frac{\Delta\hat{R}}{\hat{R}}\right)_{noise}\right) = \mathrm{Var}\left(\left(\frac{\Delta Q}{Q_n}\right)_{noise}\right) = \mathrm{Var}\left(\frac{\int_{-\infty}^{\infty} x(t)\cdot i_n(t)\,\mathrm{d}t}{\int_{-\infty}^{\infty} x(t)\cdot \delta i(t))\,\mathrm{d}t}\right) = \frac{T_i\sigma_{i_n}^2}{(T_i\delta_i)^2} = \frac{1}{T_i}\cdot\left(\frac{\sigma_{v_n}}{R\delta_i}\right)^2$$

In which the third to last equality follows by using the definition of variance to expand the integration to a 2D integral, exchanging the order of integration, and using that the variance of white noise behaves as a Dirac delta function.

Bulk current feedthrough

Apart from the injected measurement current, there is also the bulk output current. Part of this current can feed through to the measurement. Since the injected current is orthogonal to pointsymmetric signals, only the even component of the bulk current feeds through to the measurement. For sinusoidal output currents, this occurs at the peaks in bulk current, as illustrated in Figure 3.14.

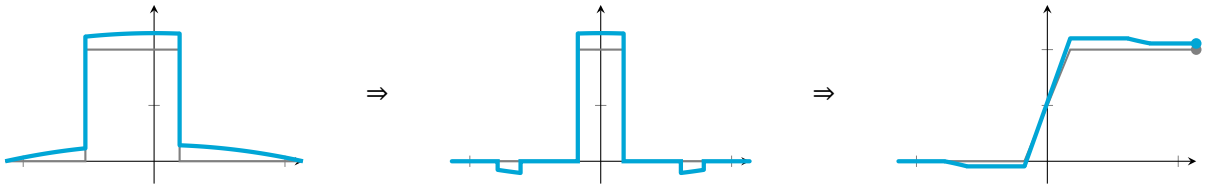


Figure 3.14: Bulk current feedthrough gives a signal-dependent error that peaks at the output current peaks (worst case, exaggerated by $20\times$).

Then the error due to bulk current feedthrough is bounded by the error made in this case, which is given by the correlation with the injected signal:

$$\left|\frac{\Delta\hat{R}}{\hat{R}}\right|_{bulk} = \left|\frac{\Delta Q}{Q_n}\right| < \frac{\int_{-\infty}^{\infty} x(t)\cdot I_{worst-case}(t)\,\mathrm{d}t}{\int_{-\infty}^{\infty} x(t)\cdot \delta i(t))\,\mathrm{d}t} =$$

$$= \frac{2I\cdot\left(\int_0^{T_i/4}\cos(\omega_m t)\,\mathrm{d}t - \int_{T_{gap}+T_i/4}^{T_{gap}+T_i/2}\cos(\omega_m t)\,\mathrm{d}t\right)}{T_i\cdot\delta i} = \text{(symmetry)}$$

$$= \frac{I}{\delta i}\frac{1}{\omega_m T_i}\cdot 2\cdot\left(\sin\left(\frac{\omega_m T_i}{4}\right) - \sin\left(\omega_m\cdot\left(T_{gap}+\frac{T_i}{4}\right)\right) + \sin\left(\omega_m\left(T_{gap}+\frac{T_i}{2}\right)\right)\right) \quad (3.8)$$

In which $I_{worst-case}(t)$ is the worst case bulk current.

Degradation in bulk current rejection due to jitter

Since the injected measurement signal is orthogonal to constant offsets and linear ramps, bulk current such as ripple and the average current ideally do not affect the measurement. However, this suppresion can be deteriorated due to jitter, as illustrated in figure 3.15.

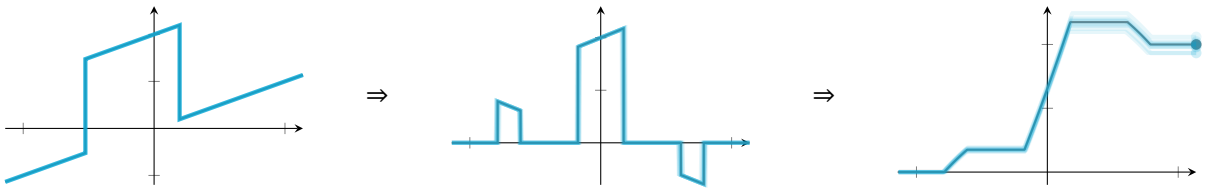


Figure 3.15: Jitter imparts a stochastic error (10 realisations shown, ramp understated, jitter exaggerated).

The error due to the jitter is best understood by its variance. The error charge is given by the charge that is mistakenly integrated, so that:

$$\left(\frac{\Delta\hat{R}}{\hat{R}}\right)_{jitter} = \frac{\sum_{k=0}^{5}\int_{t_{edge,k}}^{t_{edge,k}+j_k} I(t)\mathrm{d}t}{T_i\delta i} \approx \frac{\sum_{k=0}^{5} j_k\cdot I(t_{edge,k})}{T_i\delta i}$$

In which j_k is the jitter at edge k, and the final equality follows from a small fluctuation approximation. Since the jitter is a stochastic phenomenon, so is the associated error. Assuming Independent Identically Distributed (IID) (and thus white) jitter, the effect can be described in terms of its variance:

$$\mathrm{Var}\left(\left(\frac{\Delta\hat{R}}{\hat{R}}\right)_{jitter}\right) \approx \frac{\sum_{k=0}^{5}\mathrm{Var}(j_k)\cdot I(t_{edge,k})^2}{T_i^2\delta i^2} = \mathrm{Var}(j)\cdot\sum_{k=0}^{5}\left(\frac{I(t_{edge,k})}{T_i\delta i}\right)^2 \quad (3.9)$$

In which the variance distributes over the summation thanks to the independence of the j_k and the variance can be written as a single quantity thanks to the identical distribution.

Feedthrough of bulk current due to changing resistance
The resistance of the switching device will change over temperature and due to dynamic on-resistance effects. The change in resistance changes the voltage over it, essentially mixing with the bulk current. This can cause a measurement error, as illustrated in figure 3.16.

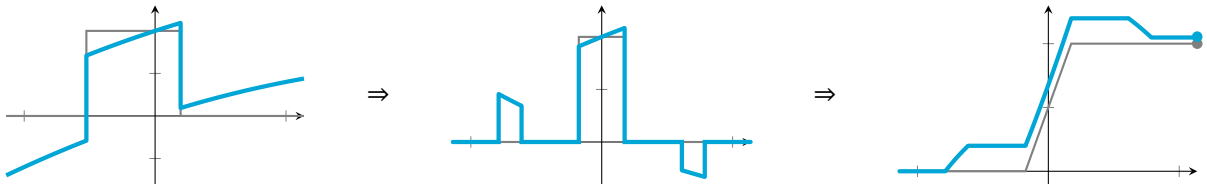


Figure 3.16: Gradual changes in bulk resistance cause additional feedthrough due to mixing with the average bulk current.

Since both the bulk current and resistance have the same mathematical role in causing a voltage $v_{R_{ds}} \approx I \cdot R_{ds}$, a change in bulk voltage due to resistance and a change in bulk voltage due to current are indistinghuisable at the input of the measurement system. Hence, the effect can be modelled by an equivalent current $\Delta I_{eff,R}$ given by:

$$\left(I + \Delta I_{eff,R}\right) \cdot R_{ds,nominal} = I \cdot \left(R_{ds,nominal} + \Delta R_{ds}\right) \Rightarrow \Delta I_{eff,R} \cdot R_{ds,nominal} = I \cdot \Delta R_{ds} \Rightarrow \Delta I_{eff,R} = I \cdot \frac{\Delta R_{ds}}{R_{ds,nominal}}$$

Thus, linear changes in R_{ds} will be suppressed like ripple, and nonlinear changes may cause bulk feedthrough. The effective current should be taken into account when evaluating equations 3.8 and 3.9.

Injection ringing and settling
Unmodelled dynamics of the switching devices cause ringing when a current is injected, as well as a slower settling component. The dead time fully supresses the ringing towards insignificance, but not the settling. This causes a slight underestimate of the resistance.

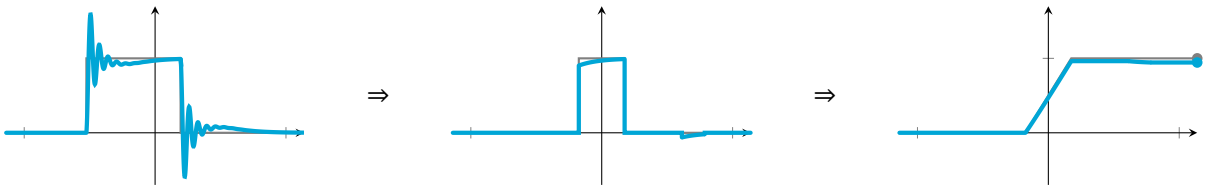


Figure 3.17: Unmodelled dynamics cause high frequency ringing (understated) and lower frequency settling (exagerrated) due to the current injection.

Locally modelling the settling component as an exponential function, the error can be found from:

$$\begin{aligned}\left(\frac{\Delta\hat{R}}{\hat{R}}\right)_{ringing} = \left(\frac{\Delta Q}{Q_n}\right) \approx \frac{\int_{-\infty}^{\infty} \Delta x(t) \cdot \delta i(t)\,\mathrm{d}t}{\int_{-\infty}^{\infty} x(t) \cdot \delta i(t))\,\mathrm{d}t} &= \\ = -\frac{\int_{-T_i/4}^{T_i/4} B \cdot \mathrm{e}^{-(t+T_{gap}+T_i/4)/\tau} \cdot \delta i\,\mathrm{d}t + \int_{T_{gap}+T_i/4}^{T_{gap}+T_i/2} B \cdot \mathrm{e}^{-(t-T_i/4)/\tau} \cdot \delta i\,\mathrm{d}t}{T_i \cdot \delta i} &= \\ = \frac{\tau}{T_i} \cdot B\mathrm{e}^{-T_{gap}/\tau} \cdot \left(\mathrm{e}^{-T_i/(2\tau)} + \mathrm{e}^{-T_i/(4\tau)} - 2\right) & \end{aligned} \tag{3.10}$$

Changing resistance distorts the measurement signal
The resistance of the switching device will change over temperature and due to dynamic on-resistance effects. The change in resistance changes the voltage over it due to the injected current, as illustrated in figure 3.18.

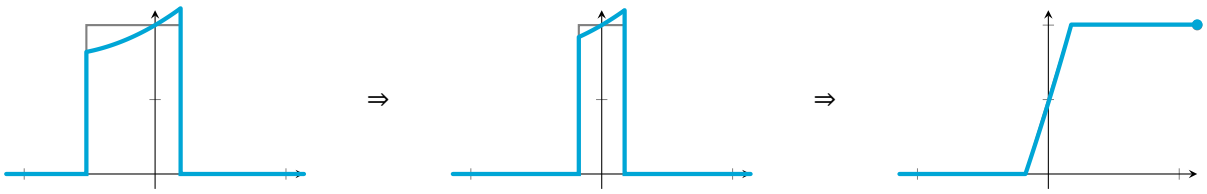


Figure 3.18: Changes in resistance distort the measurement signal.

The error is given by the difference in the measured resistance and the resistance at the sampling interval:

$$\left(\frac{\Delta\hat{R}}{\hat{R}}\right)_{change} = \left(\frac{\Delta Q}{Q_n}\right) \approx \frac{\int_{-\infty}^{\infty} x(t)\cdot\frac{\Delta r_{ds}(t)}{r_{ds}(0)}\cdot\delta i(t)\,\mathrm{d}t}{\int_{-\infty}^{\infty} x(t)\cdot\delta i(t))\,\mathrm{d}t} = \frac{2\delta i\cdot\int_{-T_i/4}^{T_i/4}\frac{\Delta r_{ds}(t)}{r_{ds}(0)}\,\mathrm{d}t}{T_i\cdot\delta i} = \frac{1}{T_i/2}\cdot\int_{-T_i/4}^{T_i/4}\frac{\Delta r_{ds}(t)}{r_{ds}(0)}\,\mathrm{d}t$$

Which is the average of the relative error in resistance over the positive integration pulse. This supresses odd components, such as linear ramps. Due to the high speed of the measurement, all changes in resistance are well approximated by these linear ramps, and this effect is insignificant.

3.4. Current injection method

3.4.1. Acceptable output conductance

The test signal has been modeled as an ideal current injection. However, practical current sources have a nonzero output conductance, which may impact the measurement. This section aims to establish acceptable output conductance limits to maintain measurement quality.

First, observe that a constant output conductance does not influence the system accuracy, as it simply becomes part of the unknown parasitic resistance. However, the output conductance may vary with the current. This can be modelled as a rise in conductance G_{vary} when positive current is injected:

$$G(t) = G_{vary}\cdot u\left(\delta i(t)\big|_{G(t)=0}\right) \quad\Rightarrow\quad \delta i(t) = \delta i(t)\big|_{G(t)=0} - G_{vary}\cdot u\left(\delta i(t)\big|_{G(t)=0}\right)\cdot I(t)R \tag{3.11}$$

In which $u(x)$ is the Heaviside step function and $\delta i(t)\big|_{G(t)=0}$ is the injected current when output conductance is not taken into account. The impact of G_{vary} is then due to the second term in equation (3.11). It describes a pulse with amplitude $G_{vary}RI(t)$. Since the pulse is correlated with the injected current, it passes directly to the output of the correlator. This gives rise to a bias:

$$\frac{\Delta\hat{R}}{\hat{R}} = \frac{G_{vary}RI(t)}{2\delta i} \quad\Rightarrow\quad G_{vary} < \left|\frac{\Delta\hat{R}}{\hat{R}}\right|_{max}\cdot\frac{2\delta i}{|I_{max}|}\cdot\frac{1}{R} \approx 0.1\,\%\cdot\frac{2\cdot 1\,\mathrm{A}}{100\,\mathrm{A}}\cdot\frac{1}{1\,\mathrm{m\Omega}} = 20\,\mathrm{mS} \tag{3.12}$$

In which the factor 2 is included because the pulse is only active for half of the integration time. The maximum output conductance can be further relaxed if the current through the injection branch is monitored using a second matched filter. Essentially, this method makes the current due to the conductance part of the injected current. The error is due to the degradation of the orthogonality properties and is given by the difference with a pulse of equal amplitude but an ideal shape:

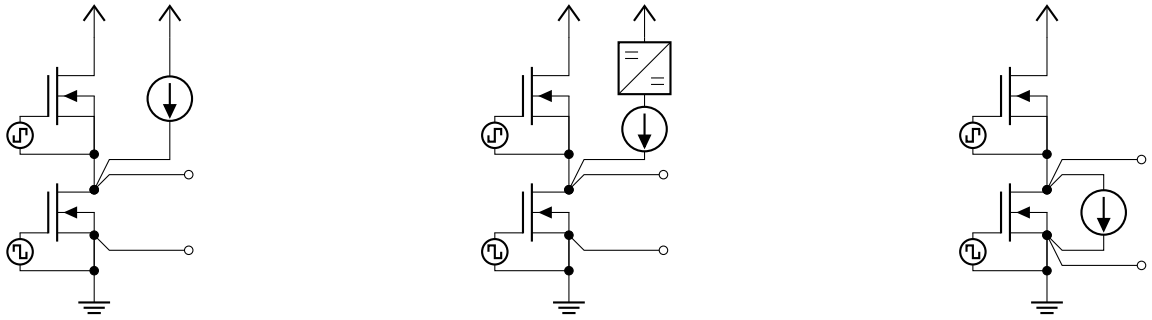
$$\delta i_G = \frac{\int_{-T}^{T} x(t)\cdot\delta i(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot\delta x(t)\,\mathrm{d}t} \qquad \Delta\hat{R} = \frac{\int_{-T}^{T} x(t)\cdot v(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot\delta i(t)\,\mathrm{d}t} - \frac{\int_{-T}^{T} x(t)\cdot v(t)\big|_{\delta i(t)=\delta i_G\cdot x(t)}\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot\delta i(t)\,\mathrm{d}t} \tag{3.13}$$

In which $x(t)\in\{-1,0,+1\}$ is the shape of the injected signal and $\delta i(t)$ is the monitored injected current. As calculated in appendix A.5, the degradation gives no more than $50\,\mathrm{mA}$ error over practically the full range of load currents.

In conclusion, the output conductance does not limit measurement quality and can remain a degree of freedom. However, conductances higher than the limit given by equation (3.12) come with the added complexity of current monitoring.

3.4.2. Choice of power source

Though current sources are often modelled as active devices, practical implementations consist of an active power source along with a passive current regulator. The choice of power source has a strong influence on the performance to cost characteristics of the circuit and thus merits closer attention. Figure 3.19 shows the available power source options.



(a) From a pre-existing high or low voltage rail.

(b) From power preserving supply like switchmode.

(c) From drain voltage.

Figure 3.19: Passive current source power supply options

For a given $\delta i(t)$, each implementation injects an equal normalised current power:

$$P_i = f_s \cdot E_i = f_s \cdot \int_{-T}^{T} \delta i(t)^2 \,\mathrm{d}t = 2 \cdot T f_s \cdot \delta i^2 \cdot \eta_{settle} = \frac{T f_s}{2} \cdot I_{inj}^2 \cdot \eta_{settle}$$

In which I_{inj} is the maximum unipolar injected current. The second equality follows because $(\delta i(t))^2 = (\pm \delta i)^2 = \delta i^2$ and the third equality because $\delta i = I_{inj}/2$, as half of the current functions as a bias.

Voltage rail

A fixed voltage rail can be used as the power source for the current injection. This rail may be the bus voltage, or a lower voltage bus used to power control circuitry, which is often generated using a power preserving supply such as a switchmode buck converter.

This concept combines simplicity, flexibility, and a low area. The current is constant, giving measurement quality that is independent of the bulk current. A single open loop mosfet CS stage would be a perfomant implementation. Assuming saturation and using the square-law model [49], the area can be found:

$$I_D = \frac{W}{L} \cdot \frac{\mu C_{ox}}{2} \cdot V_{GT}^2 \quad \Rightarrow \quad A = L \cdot W \approx \frac{I_D \cdot L^2}{\mu C_{ox} \cdot V_{GT}} \cdot \frac{2}{V_{GT}} \approx \frac{I_D \cdot L^2}{\mu C_{ox} \cdot V_{GT}} \cdot \frac{2}{4\,\mathrm{V}} = K \cdot 0.5\,\mathrm{V}^{-1} \tag{3.14}$$

In which K is a scaling constant. Additional circuitry will be needed to maintain a known current over PVT variations, for example using the monitoring function described in section 3.4.1. Various low relative area implementation exist, such as those based on replica sensing [50]. Hence, this is unlikely to significantly affect the area.

The advantages come at the cost of power efficiency. Since the voltage over the switching device is low, most of the voltage drop is over the passive current regulator so that little energy contributes to the measurement. In particular, the dissipated input power is given by:

$$P_{dis} = f_s \cdot V_{dd} \cdot \int_{-T}^{T} i_{inj}(t) \,\mathrm{d}t = T f_s \cdot V_{dd} I_{inj} \tag{3.15}$$

The injected normalised current power can be related to the dissipated power:

$$\frac{P_i}{P_{dis}} = \frac{\frac{T f_s}{2} \cdot I_{inj}^2 \cdot \eta_{settle}}{T f_s \cdot V_{dd} I_{inj}} = \frac{\eta_{settle} \cdot I_{inj}}{2 V_{dd}} \approx \frac{0.5 \cdot 1\,\mathrm{A}}{2 \cdot 5\,\mathrm{V}} = 0.05\,\Omega^{-1} \tag{3.16}$$

As expected, higher settling efficiencies η_{settle} are more efficient. Lower V_{dd} and higher injected currents I_{inj} are also beneficial. This can be explained by the fact that this matches the voltage over the switching device and the power rail, giving a higher ratio of energy that contributes to the measurement. V_{dd} and P_{dis} are usually fixed, but there are two other factors that affect I_{inj}:

$$P_{dis} = T f_s \cdot V_{dd} I_{inj} \quad \Rightarrow \quad I_{inj} = \frac{P_{dis}}{V_{dd} \cdot T f_s} \tag{3.17}$$

A lower measurement frequency f_s and shorter injection time T both concentrate the input power in a shorter time, increasing the injected current. This leads to the tradeoff between T and η_{settle}. For a given settling time T_{settle}, lower T increases I_{inj} which increases P_i/P_{dis}, but decreases η_{settle} which decreases P_i/P_{dis}. An optimum P_i/P_{dis} is can be found through combining equations 3.16 and 3.17, using that $\eta_{settle} = 1 - T_{settle}/T$, and optimising:

$$\frac{\partial}{\partial}\left(\frac{P_i}{P_{dis}}\right) = 0 \Rightarrow \frac{\partial}{\partial T}\left(\frac{P_{dis}}{2 V_{dd}^2 f_s} \cdot \frac{1 - T_{settle}/T}{T}\right) = 0 \Rightarrow T = 2T_{settle} \tag{3.18}$$

So that $\eta_{settle} = 0.5$. Note that this conditions optimises the signal to noise ratio, which only optimises system performance if the system is noise-limited. Since half of the injection time is spent on settling, Q_{inj} is only half of what it could be in the limit of $T_i \to \infty$. This increases interference by a factor of $2\times$. Hence, $T > 2T_{settle}$ could be chosen to trade of interference and noise.

DC-DC

Another option is to use some type of power-preserving DC-DC supply as the source of the injected current. This concept retains the flexibility of the voltage rail, but also has a near-optimal efficiency. The dissipated input power is:

$$P_{dis} = f_s \cdot \frac{1}{\eta_{DC-DC}} \int_{-T}^{T} R \cdot (\delta i(t))^2 \, \mathrm{d}t = \frac{R}{\eta_{DC-DC}} \cdot P_i \tag{3.19}$$

In which $\eta_{DC-DC} < 1$ is the efficiency of the DC-DC converter. Hence, the measurement efficiency is:

$$\frac{P_i}{P_{dis}} = \frac{\eta_{DC-DC}}{R} \rightarrow \frac{1}{R} \tag{3.20}$$

Which is near-optimal, up to the efficiency. One important factor limiting this efficiency is the resistance of the switches used in the converter. In particular, the injected current will flow through at least one such switch. This then gives losses of at least $R_{switch} \cdot P_i$ so that:

$$\eta_{DC-DC} < \frac{R \cdot P_i}{P_{dis}} = \frac{R}{R + R_{switch}} \approx \frac{R}{R_{switch}} \quad \Rightarrow \quad \frac{P_i}{P_{dis}} < \frac{R/R_{switch}}{R} \approx \frac{1\,\%}{1\,\mathrm{m\Omega}} = 10\,\Omega^{-1} \tag{3.21}$$

In which the final equality follows because the measurement circuit is desired to be much smaller than the power stage and to not be implemented in a specialised low on-resistance process. Hence, the practical efficiency is far from ideal. The switch also requires significant area. According to the square law model in the triode region[49]:

$$R_{switch} = \frac{L}{W \cdot \mu C_{ox} \cdot V_{GT}} \Rightarrow A = L \cdot W \approx \frac{L^2 \eta_{DC-DC}}{R \cdot \mu C_{ox} \cdot V_{GT}} = \frac{I_D \cdot L^2}{\mu C_{ox} \cdot V_{GT}} \cdot \frac{\eta_{DC-DC}}{I_D R} \approx K \cdot \frac{1\,\%}{1\,\mathrm{A} \cdot 1\,\mathrm{m\Omega}} = K \cdot 10\,\mathrm{V}^{-1} \tag{3.22}$$

Further disadvantages are the larger complexity due to the control of the converter and the large area requirement of either bulk capacitors or a bulk inductor, which cannot be integrated in a standard CMOS process.

Drain voltage

The final option is to use the voltage over the switching device as the power source, diverting part of the current. A similar method has been proposed in [36], where the current is briefly diverted through a sensing path. The approach described here improves on this method because the diversion path need not handle the full load current and is always active in parallel with the main switching device, reducing system losses.

This concept combines a low area, simplicity, and beyond-optimal efficiency as no input power is required and the system efficiency is even improved by the addition of the measurement stage. Again, a simple open-loop CS stage can implement the current source. However, these advantages come with the disadvantage of low flexibility. The current can only be drawn when the voltage over the switching device is higher than the saturation voltage of the current source. Hence, this option cannot be used to inject a constant current over the entire load current range.

There are several options to deal with this limitation. One option is to design low-saturation voltage current sources, giving good operation in a certain operating window of high enough drain voltages. This may achievable through linearisation with feedback for example. However, this comes with additional area and complexity. A particularly elegant approach is to adapt the test current δi to the drain voltage $v(t)$ according to $\delta i \propto v(t)$. This changes the behaviour of the current source into that of solely a conductance G_{inj}, so that it may be implemented with a CS stage biased in the triode region. As explored in section 3.4.1, this does not significantly affect the measurement quality. The downside of this concept is the injected current can become very low, leading to lower measurement performance. The injected normalised current power is given by:

$$P_i = \frac{Tf_s}{2} \cdot I_{inj}^2 = \frac{Tf_s}{2} \cdot \left(G_{inj} \cdot V\right)^2 = \frac{Tf_s}{2} \cdot \left(G_{inj} \cdot R\right)^2 \cdot I^2 \tag{3.23}$$

Which shows that the injected normalised current energy becomes strongly dependent on the load current. This load current-dependent noise does not necessarily limit system performance. Using the error model from section 2.1 and resistance estimation noise distribution from section 3.2, the RMS error current is given by:

$$\Delta \hat{I}_{RMS} \approx \sqrt{\frac{1}{T} \int_0^T (i(t))^2 \cdot \frac{\mathrm{Var}\left(\Delta r(t)\right)\big|_{I=i(t)}}{R^2} \, \mathrm{d}t} = \sqrt{\frac{N_0}{R^2} \cdot \frac{1}{Tf_s}} \cdot \frac{1}{G_{inj} R} \tag{3.24}$$

Which is independent of load current.This is due to the fact that errors in resistance give gain errors in the current estimate, which become linearly less pronounced for lower load currents. Hence, a linearly decreasing signal to noise ratio simply cancels out. Though the system-level current estimation performance is affected by the decreased resistance estimation performance, the worst-case noise is unaffected.

Since this method of current injection does not draw significant input power, the concept of measurement efficiency does not apply. However, the injection stage does dissipate heat P_{dis} inside the injection stage, which can be related to the injected current energy:

$$\frac{P_i}{P_{dis}} = \frac{\frac{Tf_s}{2} \cdot \left(G_{inj} \cdot R\right)^2 \cdot I^2}{Tf_s \cdot G_{inj} \cdot \left(R \cdot I\right)^2} = \frac{G_{inj}}{2} = \frac{I_{inj}}{2V_{DS}} \approx \frac{1\,\mathrm{A}}{2 \cdot 100\,\mathrm{mV}} = 5\,\Omega^{-1} \tag{3.25}$$

A disadvantage of this concept is that the low voltage of the power source requires low resistances to achieve a given current. This increases the significance of parasitic resistances, such as those from bond wires. It is also more area intensive, though operation in the triode region minimises the area. Using the square law model[49], the area can be estimated as:

$$I_D = \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{GT} \cdot V_{DS} - \frac{V_{DS}^2}{2}\right) \quad \Rightarrow \quad A = L \cdot W \approx \frac{I_D \cdot L^2}{\mu C_{ox} \cdot V_{GT}} \cdot \frac{1}{V_{DS}} \approx \frac{I_D \cdot L^2}{\mu C_{ox} \cdot V_{GT}} \cdot \frac{1}{100\,\mathrm{mV}} = K \cdot 10\,\mathrm{V}^{-1} \tag{3.26}$$

The area penalty can be partly mitigated by a decrease in injected current. Since this method of current injection does not increase power consumption, T may be chosen arbitrarily long and f_s may be maximised without a power penalty. This also optimises $\eta_{settle} \to 1$. A tradeoff remains between the injection time T and the available duty cycle range.

Selection

Table 3.2 summarises the key cost factors of the circuits. Both typical values and relative scale factors are given. Introducing a separate DC-DC converter is an obviously unviable option because it requires an unacceptable off-chip component. Both injection from the drain voltage and from a voltage rail have strong advantages. Injection from the drain voltage minimises thermal stress on the package and requires no significant input power. However, injection from the rail comes with a much smaller area. Given that the reduced efficiency of rail injection does not pose a barrier to meeting the power and precision requirements as seen in section 3.6, the lower area is preferred here. The consistent measurement quality that simplifies on-resistance monitoring is an added bonus. Hence, rail injection was adopted.

Table 3.2: Voltage rail injection is the most suitable option ($\eta_s = \eta_{settle}$, $\eta = \eta_{DC-DC}$).

Factor	**Scaling factors**			**Typical value**			**Justification**
	Rail	DC-DC	Drain	Rail	DC-DC	Drain	
Area	$\frac{2}{V_{GT}}$	$\frac{\eta}{I_{inj}R}$	$\frac{1}{V_{DS}}$	0.5	10	10	Relative scale factors at fixed I_{inj}
External components				0	1	0	
Input power P_{in}/P_i	$\frac{2V_{dd}}{I_{inj}}$	$\frac{R}{\eta}$	0	20	0.1	0	Relative scale factors
Dissipated heat $P_{dis,h}/P_i$	$\frac{2V_{dd}}{I_{inj}}$	$\frac{R}{\eta}$	$\frac{2V_{DS}}{I_{inj}}$	20	0.1	0.2	Relative scale factors
Resistance monitoring				+	+	±	

3.5. Topology

Both the high- and low side switches may be used to estimate current. Input switches are used to select the device and disconnect the input when the voltage is large. Voltages offsets are needed to adapt the input voltages to the common mode input range of the input amplifier. If capacitors are used, they can also directly be used to implement autozeroing, decreasing input offset.

The amplitude of the injected current step is tightly controlled as it serves as the reference current for the measurement, with offsets causing gain errors. For high-side measurements, the current is drawn from the bus voltage through the switching device to ground. The current for low-side measurements is drawn from the computing supply and flows to ground via the switching device. Since this supply is often generated using a power-preserving switchmode converter, this makes the low-side measurements less energy-intensive.

The correlator is implemented with switches, like those used for selecting the input device. A multiplication by $+1$ is implemented by passing the differential signal through unaltered. For a multiplication by -1, the connections are flipped. Multiplication by 0 is achieved by disabling all signals, so that the signal is not passed through. An input amplifier is specified to reduce offset and noise requirements on later stages.

equation (3.9) implies that when interference due to the load current is only supressed by the correlator, the measurement becomes highly sensitive to jitter. Since the load current is much higher than the injected current, even

a small change in the length of the upwards pulse compared to the downwards pulse can create large offsets. Hence, the bulk offset should be reduced by cancelling the bulk voltages, for example by sampling the voltage on capacitors. The length of the upward and downward pulses should also be determined by some common structure to prevent degradation of the suppresion.

The voltage is measured using a switched integrator structure that is controlled using the $+1$ phase control signal of the resistance integrator. This correlates jitter-induced gain fluctuations between the measurements, supressing their effect on the current estimate. Similarly, the gain of the first stage does not directly affect the current estimate. Figure 3.20 shows the resulting architecture along with typical operating waveforms.

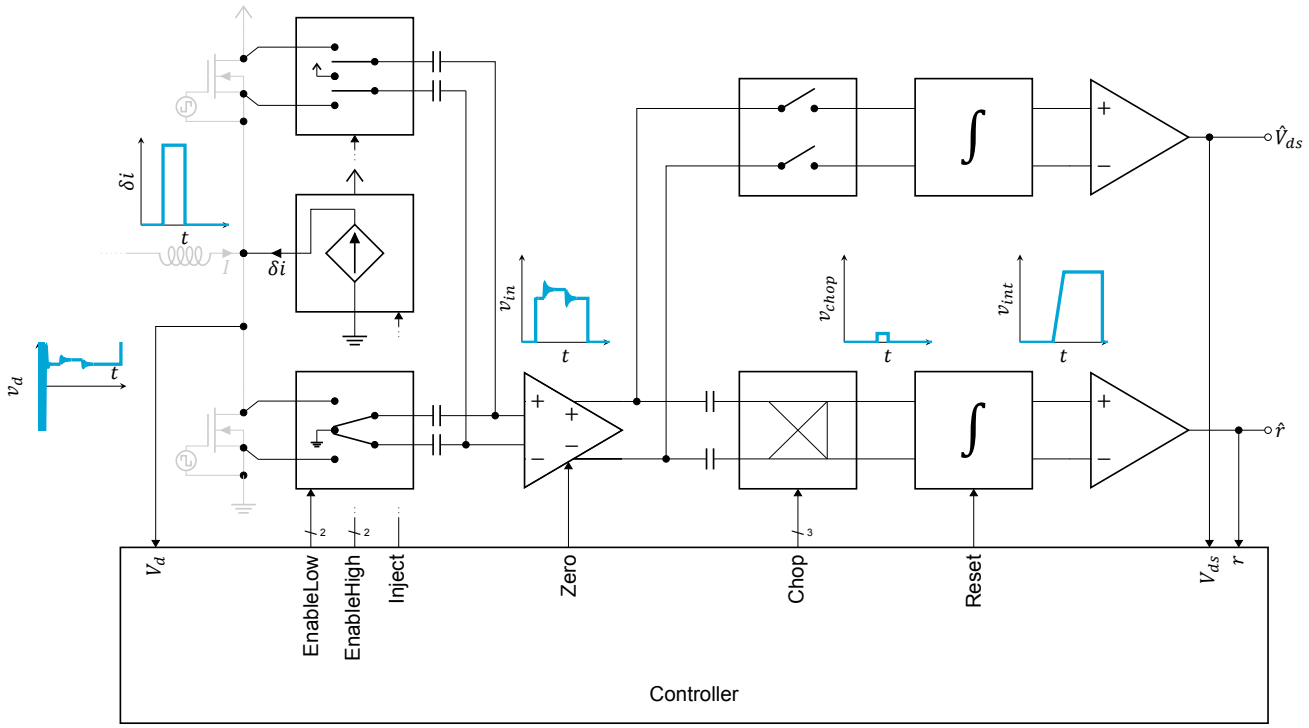


Figure 3.20: The architecture consists of switches, capacitors, integrators, amplifiers, and a current source.

The resistance measurement circuitry need not be active every cycle, which reduces power consumption due to current injection. The injected current causes an offset that can be compensated in post-processing. Since it is accurately known, it can simply be subtracted.

This implementation comes with a new error source, which will now be discussed.

3.5.1. Errors introduced by integrator input offset voltage and current

Though offsets before the chopper are heavily suppressed, offsets at the input of the integrator are not. These offsets may be constant, but could also grow with time as in the case of input bias currents flowing through capacitive voltage offset capacitors. This creates a resistance error of:

$$\left(\frac{\Delta\hat{R}}{R}\right)_{offset} = \frac{T_{active} \cdot V_{off,1} + \frac{1}{2} \cdot T_{active}^2 \cdot V_{off,2}}{G_1 \cdot T_i \cdot (\delta I \cdot R)} \tag{3.27}$$

In which G_1 is the unitless gain of the first stage, $V_{off,1}$ is the constant voltage offset at the input of the integrator in V, $V_{off,2}$ is the slope of the linearly growing voltage offset at the input of the integrator in $\mathrm{V\,s^{-1}}$, T_{active} is the time the integrator is active in s, and T_i is the time the resistance signal is integrated in s.

3.6. Dimensioning

For a given measurement power budget, selecting a sample rate fixes the injection current. This introduces a tradeoff between stochastic errors due to measurement noise and systematic errors due to insufficient tracking of changing errors. Good performance requires optimisation of several system parameters. The most constraining measurement is that of the small signal resistance, which will now be considered.

First, the injected current timing is determined based on the settling time using equation (3.18). This minimises the noise. With the measurement timing in hand, the measurement rate can be determined. The optimum is found by sweeping the maximum error models over possible sample rates and selecting the optimum. All sample rates must be integer divisions of the modulation frequency. The resulting error tradeoff for a $40\,\mathrm{kHz}$ system with the IPT010N08NM5, $L_w = 90\,\mu\mathrm{H}$ and a per-phase power budget of $100\,\mathrm{mW}$ is illustrated in figure 3.21. The optimum is at a sample rate of $13.3\,\mathrm{kHz}$ and $\delta i = 0.9\,\mathrm{A}$, giving an expected worst-case error of 1%. Note that this method assumed constructive interference of all systematic errors, which in reality will not be the case, but does give an upper bound. Hence, it is desired the estimated noise is dominated by systematic errors, so that in the likely case of destructive interference the performance may improve towards the 0.2% noise-limited error.

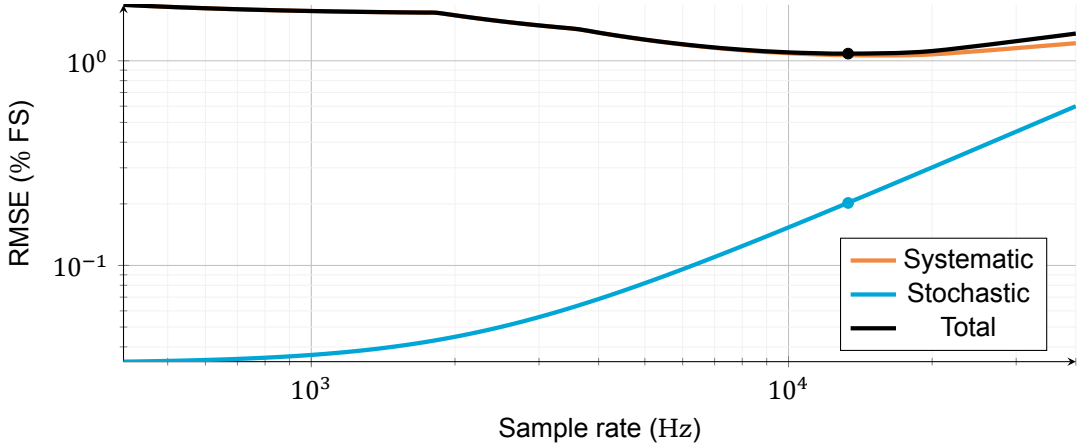


Figure 3.21: Since the error increases for both low and high sample rates, there is an optimal sample rate.

3.7. Operation

3.7.1. Measurement

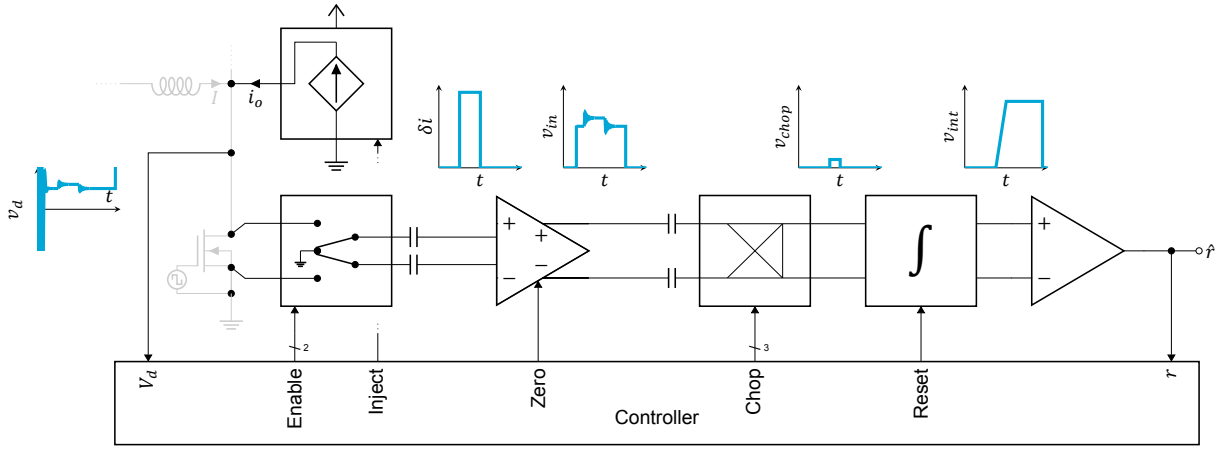


Figure 3.22: After the measurement, the system is restored to its initial state.

The measurement process is illustrated in figure 3.22. Since the voltage path has a subset of the functionality of the resistance measurement path, it is not shown.

At the start of the measurement, the selected switching device has activated, causing the drain voltage to settle. During this settling, the drain voltage is not connected to the input amplifier. Instead, it is zeroed and the integrator is reset.

The measurement window opens when the drain voltage has settled to the point of insignificant error. The input switches are enabled, causing the input amplifier to present the drain voltage to the signal processing circuitry. The chopper is initially fully connected, which samples the approximate current on its input capacitors.

At $1320\,\mathrm{ns}$ before the midpoint the chopper is configured for passing the inverted signal. This serves as a reference sample, which will help suppress interference from the bulk current.

After a $300\,\mathrm{ns}$ integration time, the chopper is configured for zero signal passthrough. Following a $100\,\mathrm{ns}$ waiting time, the current δi is injected from $920\,\mathrm{ns}$ before the midpoint. Since the chopper is disabled, the ringing does not affect the output.

When the ringing has decreased to an acceptable level at $320\,\mathrm{ns}$ before the midpoint, the chopper is configured for signal passthrough. This serves as the main measurement, and causes a significant change in the integrator output. During this period, the bus voltage is sampled at the midpoint.

Upon the completion of the main measurement at $320\,\mathrm{ns}$ after the midpoint, the chopper is disabled and quickly thereafter the current injection is stopped. A $700\,\mathrm{ns}$ waiting period follows, during which the ringing does not affect the output.

After the waiting period, at $1020\,\mathrm{ns}$ after the midpoint, the chopper is configured for passing the inverted signal. This serves to complete the reference sample, further suppressing interference from the bulk current.

A $300\,\mathrm{ns}$ integration period completes the measurement. At $1320\,\mathrm{ns}$ after the midpoint the chopper is disabled. The input switches are also disabled, which protects the input amplifier from the large voltages at the switching node. The output signal is sampled, from which the current at the midpoint is estimated using $\hat{I} \approx \hat{V}_{ds}/\hat{r}_{ds}$.

Finally, the reset signals are asserted to bring the system back to its initial state.

All in all, the measurement takes about $2.64\,\mu\mathrm{s}$, of which $1.2\,\mu\mathrm{s}$ falls within the main integration window.

3.7.2. Post-processing

The error compensation starts with the calculation of the offset due to inverter outputs:

$$\Delta v_{ds,inverters,i} = V_{bus} \cdot \eta_L \cdot \sum_{k=1}^{3} o_k - o_i \tag{3.28}$$

In which $o_i \in \{0, 1\}$ is the unitless output state of inverter with index $i \in \{1, 2, 3\}$ during the measurement window, V_{bus} is the measured bus voltage in V, and η_L is the unitless estimated motor to lead inductance voltage division ratio. The second step is the calculation of the offset due to back-EMF:

$$\Delta v_{ds,back-EMF,i} = \eta_L \cdot \left(3 \cdot v_{back-EMF,i} - \sum_{k=1}^{3} v_{back-EMF,k} \right) \tag{3.29}$$

In which $v_{back-EMF,i}$ is the back-EMF of phase i in V. The current is then estimated using:

$$\hat{\imath} = \frac{(1 - 2 \cdot o_i) \cdot \hat{V}_{ds} - \Delta v_{ds,inverters,i} - \Delta v_{ds,back-EMF,i}}{\hat{r}} - (1 - 2 \cdot o_i) \cdot I_{inj} \tag{3.30}$$

In which the first $(1 - 2 \cdot o_i)$ factor is used to ensure positive voltages are measured from the output to the supply rail for both the top and bottom switching device, despite the different assignment of the noninverting and inverting measurement terminals. I_{inj} is the magnitude of the injected current in A.

Motor to lead inductance division estimation

In order to estimate the motor to lead inductance voltage division ratio η_L, a 2nd order polynomial $p_i(n)$ is least-squares fitted to the 50 samples before a state transition at sample $n_{transition}$ on either other inverter. The estimated inductance voltage division ratio is then given by:

$$\hat{\eta}_{L,raw} = \frac{\left(\hat{\imath}_{raw}\left(n_{transition}\right) - p_i\left(n_{transition}\right) \right) \cdot \hat{r}\left(n_{transition}\right)}{V_{bus} \cdot \Delta o} \tag{3.31}$$

In which $\hat{\imath}_{raw}$ indicates the current estimate without compensating for lead inductance voltage offsets, and the bracket number indicates that the value is taken at that sample and Δo indicates the state transition of the other inverter, being -1 when it goes low and 1 when it goes high. The estimates are then 1-st order IIR filtered to suppress noise.

Back-EMF estimation

A good estimate of the winding inductance L_w of the motor can be made through combining the inductance ratio with an estimate of the lead inductance $\hat{L}_p$:

$$\hat{L}_w \approx \frac{L_p}{3\eta_L} \tag{3.32}$$

Since the lead inductance has no core and a fixed geometry, it serves as a relatively stable reference against which to measure the relatively unstable motor inductance. Then, the constitutive relationship of an inductor is used to estimate the voltage:

$$\hat{L}_w \cdot \frac{\Delta \hat{\imath}\,(n)}{\Delta t} = \Delta V\,(n) = D\,(n) \cdot V_{bus}\,(n) - V_{back-EMF}\,(n) \quad \Rightarrow \quad V_{back-EMF}\,(n) = D\,(n) \cdot V_{bus}\,(n) - \hat{L}_w \cdot \frac{\hat{\imath}_i\,(n) - \hat{\imath}_i\,(n-1)}{T} \tag{3.33}$$

In which D is the unitless output duty cycle and $\hat{\imath}_i$ is an intermediate current estimate, in which the offset due to back-EMF is not subtracted. This prevents potentially unstable coupling between the back-EMF estimate and compensation.

4 Verification

4.1. Methods

The proposed method was tested using a single-phase electrical analogue of a motor driver system. This consists of two $48\,\mathrm{V}$ $60\,\mathrm{A}$ inverters applying a sinusoidal current through a $62\,\mu\mathrm{H}$ inductor. The inductor simulates the inductive behaviour of the motor and its parasitic $130\,\mathrm{m}\Omega$ resistance simulates the back-EMF. Since two inverters are used, the load current can circulate back to a $4.4\,\mathrm{mF}$ capacitor bank at the input supply in a Power In Loop (PIL) fashion, reducing the input power requirements. It also simulates the switching dynamics found in motor drivers. A reference current measurement is performed using a conventional $200\,\mu\Omega$ phase shunt resistor and INA240 current sense amplifier. This measurement is also used to control the current using a P-controller. An implementation of the proposed method is connected to one of the inverters, with an input noise of $1.7\,\mathrm{nV}\sqrt{\mathrm{Hz}}^{-1}$, an injected current of $I_{inj} = 0.75\,\mathrm{A}$, an integration length of $600\,\mathrm{ns}$, a zero time of $700\,\mathrm{ns}$, and an update rate of once per cycle at $40\,\mathrm{kHz}$. With a $3.3\,\mathrm{V}$ power supply, this would correspond to an injected power of $129\,\mathrm{mW}$. Both the current estimation and the power stage are controlled and monitored by a microcontroller, which streams its measurements to a host computer over USB. The setup was realised in Printed Circuit Board Assembly (PCBA) technology and is illustrated in figure 4.1. The power stage was implemented on a daughterboard for added flexibility, as shown in figure 4.2. To address excessive coupling between the instrumentation $5\,\mathrm{V}$ power supply and input stage, the power supply was replaced by a lab power supply. The $12\,\mathrm{V}$ power supply was connected by $\approx 5\,\mathrm{cm}$ wires to reduce inductive coupling. Furthermore, the integrated inductors were shorted and an external load inductor used for greater flexibility.

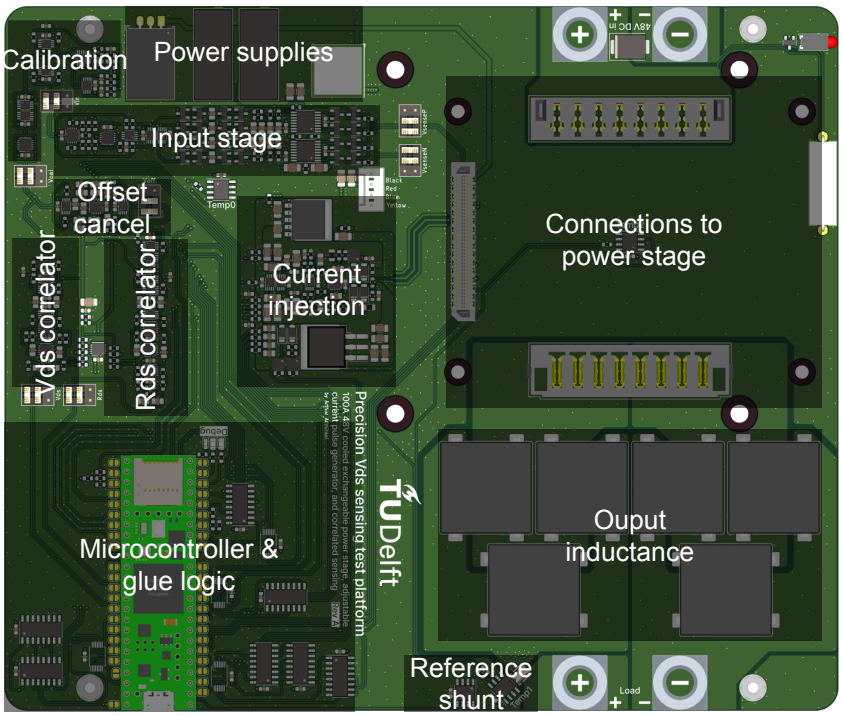


Figure 4.1: Floorplan of the main test setup PCBA.

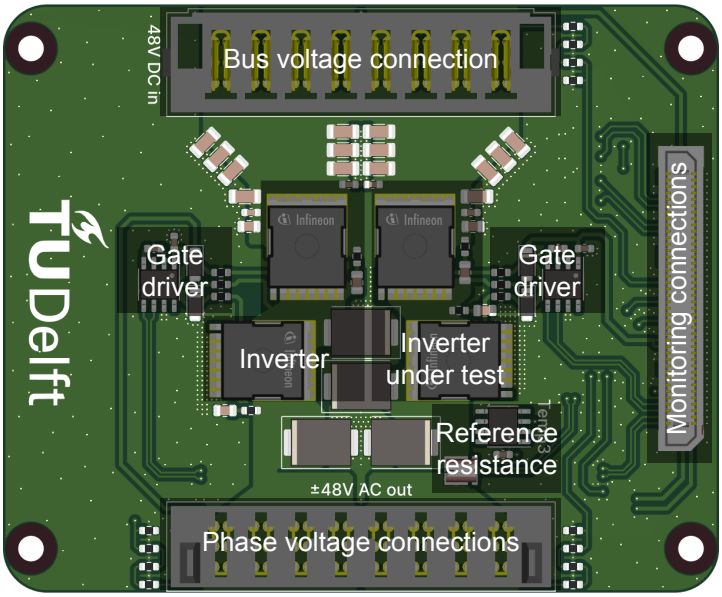
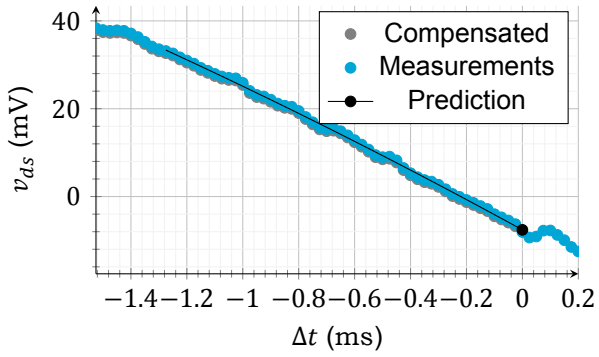


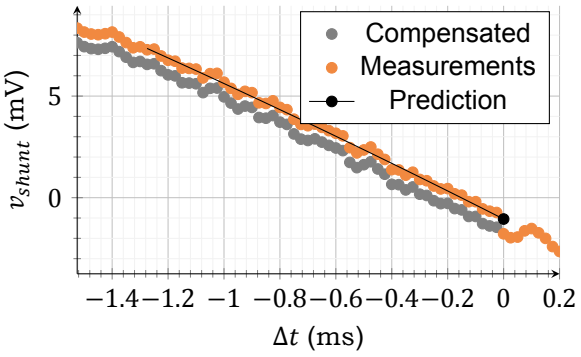
Figure 4.2: Floorplan of the power stage PCBA. Not to scale with main PCBA.

4.2. Experimental results

The test platform was used to generate a 100 Hz 109 A pk-pk sine current through the load for a period of 28 s. The lead inductance of the reference shunt and switching device were corrected using the method described in section 3.1.2. As shown in figure 4.3, the lead inductance of the reference measurement was especially significant.



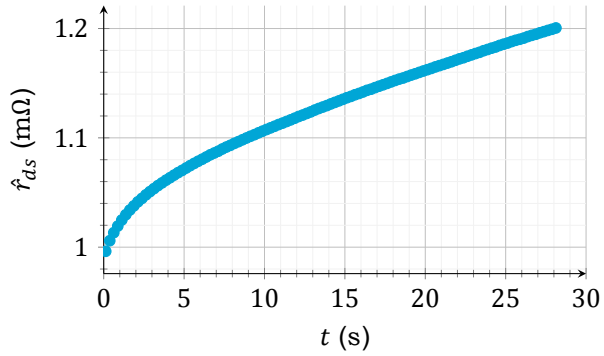
(a) Switching device ($L_p \approx 90\,\mathrm{pH}$)



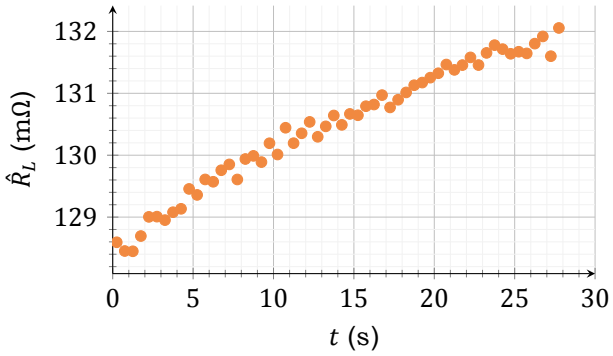
(b) Reference shunt ($L_p \approx 759\,\mathrm{pH}$)

Figure 4.3: The parasitic inductance of the reference shunt had a significant effect before compensation.

The power stage and load were not actively cooled. The power stage was also heated by applying 200 °C hot air to its heat sink using a hot air gun. The resulting estimated resistance profiles are shown in figure 4.4.



(a) Switching device (averages over 250 ms)

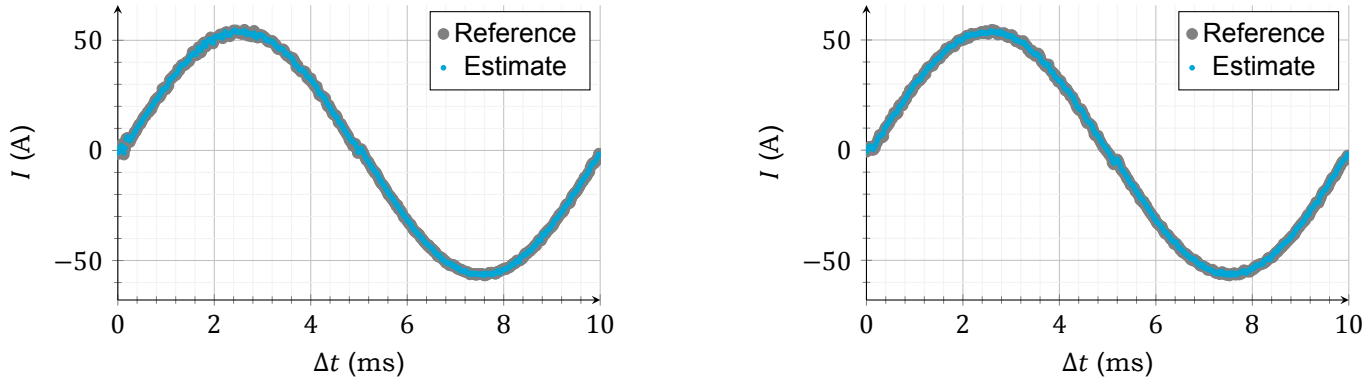


(b) Load inductor (method of section 3.7.2 in 500 ms segments)

Figure 4.4: Both the parasitic resistance of the inverter under test and the load inductance experienced significant increases.

4.2.1. The proposed method achieves the required performance

As shown in figure 4.5, the current estimated by the proposed method closely tracks the reference measurements.

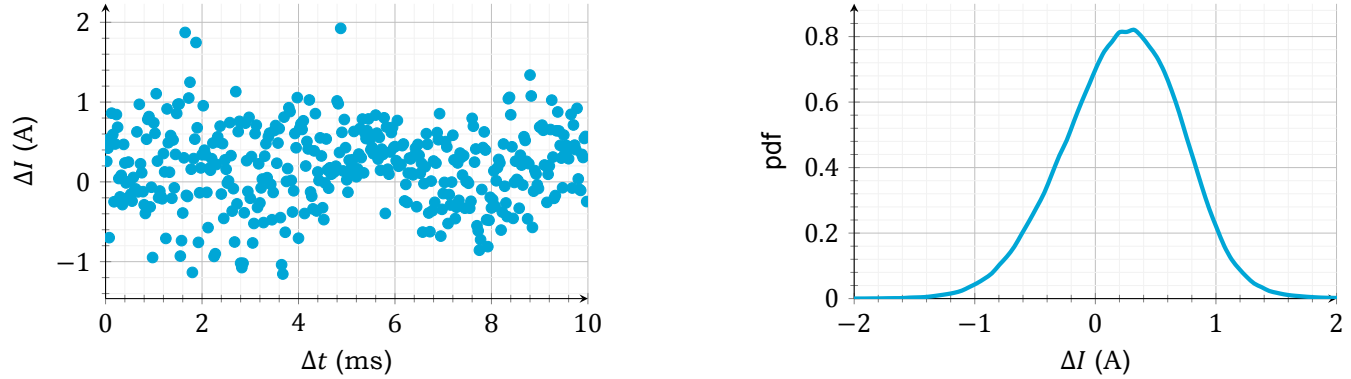


(a) At 1 s, $\hat{r}_{ds} = 1.02\,\mathrm{m\Omega}$

(b) At 25 s, $\hat{r}_{ds} = 1.19\,\mathrm{m\Omega}$

Figure 4.5: The current estimated by the proposed method closely tracks the reference measurement despite fluctuations in channel resistance.

As illustrated in figure 4.6 the RMSE of $0.536\,\mathrm{A}$ consists of a $80\,\mathrm{mA}$ offset, a $-0.146\,\%$ gain error, and a residual error with a roughly bell-shaped distribution and standard deviation of $0.508\,\mathrm{A}$.



(a) Errors over time at 1 s

(b) Error distribution histogram, 200 bins

Figure 4.6: The errors are dominated by a roughly normally distributed stochastic error.

4.2.2. Coupling from injection to input requires compensation

The resistance estimation was compared to a reference measurement based on the correlation between the voltage and reference current in one period of the load current. The correlation is illustrated in cyan within figure 4.7, along with several other datasets in other colors. There are significant gain errors ranging from $-6\,\%$ to $0.2\,\%$ and offsets ranging from $57\,\mu\Omega$ to $119\,\mu\Omega$. The error at $1\,\mathrm{m\Omega}$ seems to be more consistent, within $60\,\mu\Omega \pm 10\,\mu\Omega$.

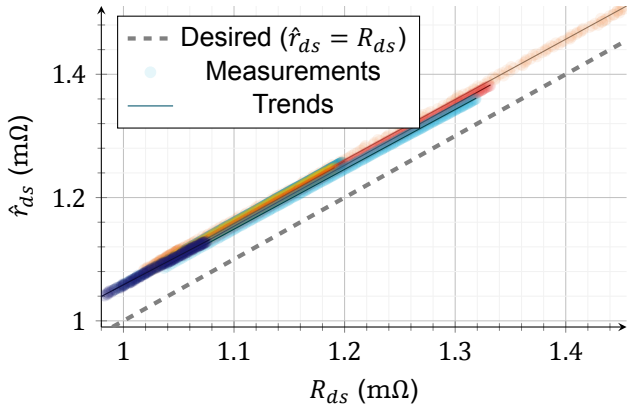


Figure 4.7: There are significant offset and gain errors in the resistance measurement.

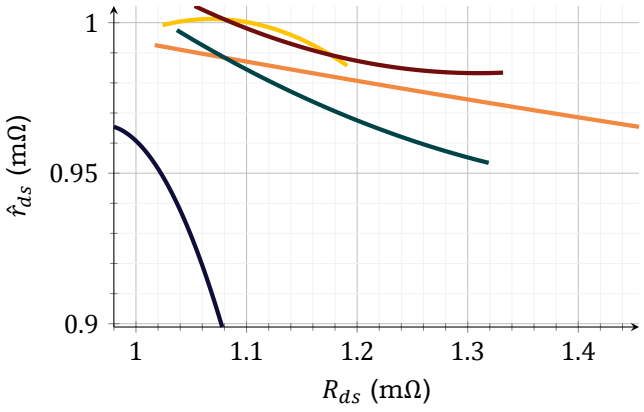


Figure 4.8: The gain errors change over datasets, suggesting missing state information.

There are several candidate explanations of the offset. One could be that there is insufficient suppresion of the common mode ground bounce caused by the current injection. However, this is not consistent with the measured robustness against bus voltage fluctuations described in section 4.2.3. The error could also be explained by inductive voltage division of the voltage over the load resistor. However, this would require a roughly $3\,\mathrm{nH}$ parasitic inductance, which is inconsistent with the small voltage jumps in figure 4.3. There is the possibility that some kind of magnetic coupling between the inverters cancels the effect of current ramps due to the supply voltage but not those due to the back-emf in the load, but it is unlikely the matching would be good enough to suppress the voltage jumps to this degree.

Three explanations have not yet been disproven.

First, there could be a difference in the current distribution of the load current compared to the injected current. The addded resistance then come with its own temperature dependence and thus gain error. This is consistent with the relative stability of the offset at a ground truth resistance of $1\,\mathrm{m\Omega}$.

Another idea is that there is significant coupling between the current injections tage and the input stage. There is some common loop area between the injecting current path and the voltage sensing current path, so that inductive coupling is a real possibility. Since this coupling is mainly geometry-dependent, it can be expected to be stable over multiple units, time, and temperature so that it can be compensated by a single point calibration at design time.

Finally, a problem in the test setup cannot be ruled out. In fact, there is some evidence to support this idea. There is a slight nonlinearity to the measurements, which correspond to changing gain errors figure 4.8. Since the gain errors are different in each dataset, this suggests there is state information in the measurement setup that alters the measurement results. This support the idea that there is unintended behaviour, such as temperature ramps affecting the gain of measurement circuitry.

More research will be needed to find the exact cause of the offset and gain error. However, since the offset is relatively stable, it can be compensated. Hence, a compensation by $60\,\mu\Omega$ has been applied for the measurement results in this chapter. Since the gain error only affects the difference with the room temperature resistance, the current estimate shows acceptable performance even without resolving this problem.

4.2.3. The high-side has differential-mode interference

Estimating currents through the high side switching device is desirable because it would enable support for measuring over the full duty cycle range. High-side shunt measurements have been described in industry literate [10, 11], where the additional benefit of detecting fault currents is noted. However, the measurement quality of high side resistance estimation was tested to be much poorer then at the low side.

One explanation is that the common mode suppresion is unsufficient for the wider voltage fluctuations on the higher-impedance bus voltage. However, this is not reflected in the data. When the inputs were shorted to the bus voltage, the mean error became significantly lower than during nominal operation without load, even when a load was added. This is shown in figure 4.9. Hence, there is a bigger error component than insufficient suppresion of common mode interference. Interference from Switch-Mode Power Supplys (SMPSs) may be that error source. When they are removed from the bus, the error becomes significantly lower than nominal as shown in figure 4.9. This suggests that common mode fluctuations in bus voltage due to inteference from the SMPSs generate differential-mode currents through the switching device because of parasitic impedances at the switch node. Because the interference is not synchronous with the resistance estimation, it does not get suppressed by the down-up-up-down pulse. Since the copper planes in the power stage circuit board are ground-referenced the parasitics from the switching node to ground are much larger than the parasitics from the switching node to the supply, so that this error is much stronger for the high side.

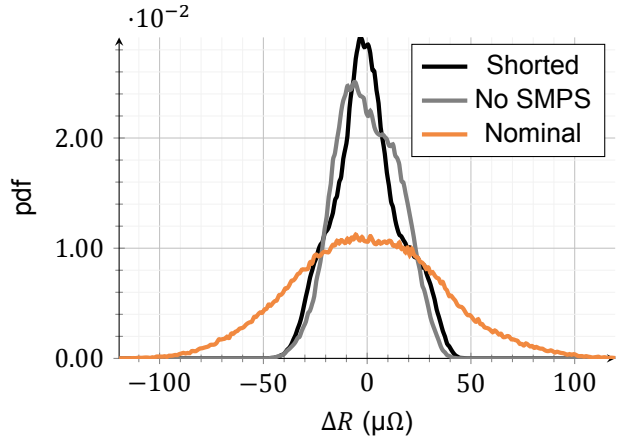


Figure 4.9: High side error distribution over various conditions. Results without load, except for $10\,\mathrm{A}$ pk-pk load with shorted inputs.

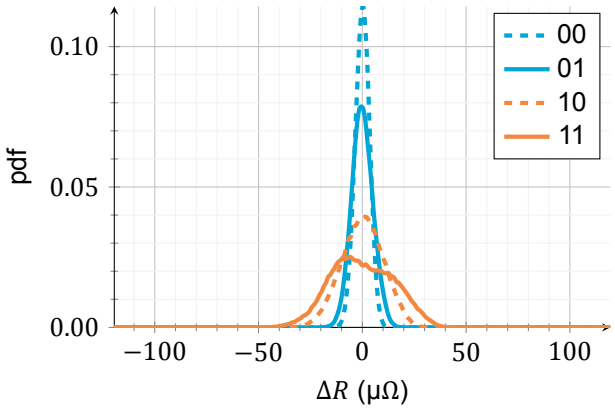


Figure 4.10: The resistance error varies with inverter state. First digit is inverter under test, second is load inverter.

4.2.4. The loading inverter state influences the noise of the measurement

As shown in figure 4.10, the state of the loading inverter changes the resistance error distribution of the inverter under test. One explanation could be that when the the inverters have opposite states, fluctuations in the bus voltage can more easily couple to the parasitic resistance of the inverter under test, as a path through the load inductance is created. Yet, the data shows that the resistance error increases when the loading inverter is high, no matter the state of the inverter under test.

The effect of the load inverter can also be seen from the average resistance over each period of the load current shown in figure 4.11. A fast roughly $\pm 0.5\,\%$ fluctuation can be seen in the first half of the signal, where the load inverter is high. The fluctuation in the resistance is correlated with a corresponding error in the average current. As illustrated, it seems to be correlated with the derivative of the bus voltage.

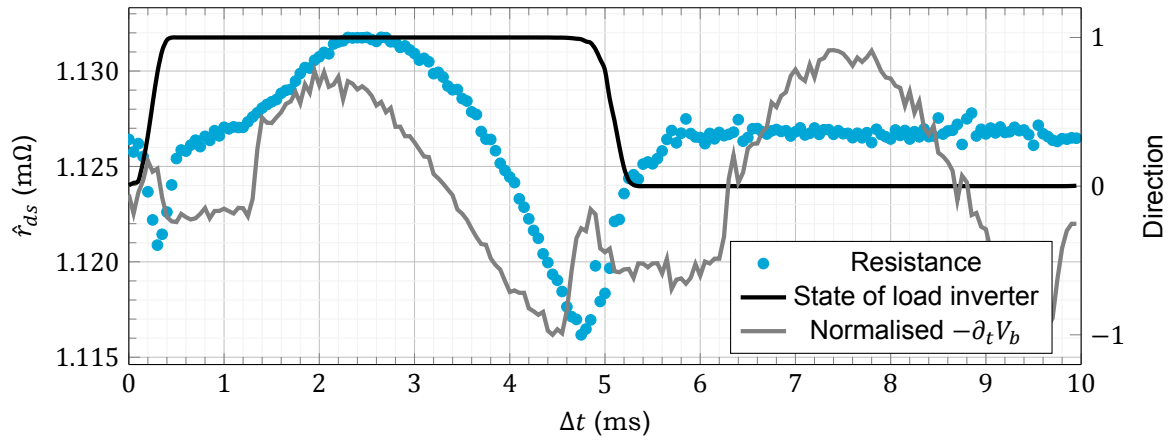


Figure 4.11: Without chopping, there is a significant resistance error.

The observations suggest there may be some type of magnetic coupling of the differential mode error currents described in section 4.2.3. More research would be needed to determine the exact cause of the effect. Fortunately, it is small enough not to hamper operation.

4.2.5. Robustness is improved by system chopping

There was an unexpectedly large amount of coupling between the power stage and the measurement circuitry, causing significant voltage fluctuations over the ground plane of the measurement circuitry. This large interference was not adequately suppressed by the use of differential signaling and the chosen measurement pulse. It was adressed by system chopping, where the duty cycle was fixed for two samples, with opposing polarity of the injected current in each. This provided an additional degree of rejection of common mode signal. Figure 4.12 shows the average contribution of the common mode component, which is supressed by the chopping scheme. It can be seen that the system chopping scheme greatly reduces error.

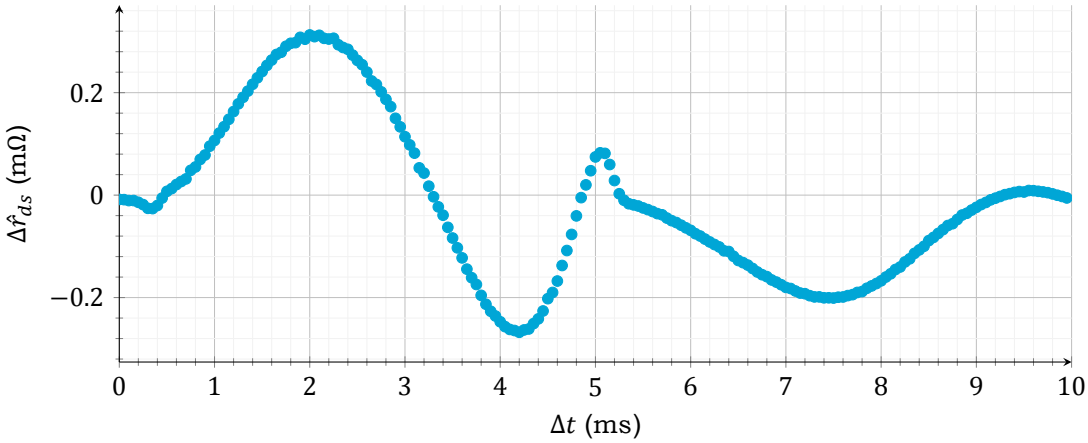


Figure 4.12: Without chopping, there is a significant resistance error.

5

Conclusion

This work introduced an approach to Vds current sensing that has sufficient fidelity for closed-loop current control of small electric motors while not requiring the high-cost production processes or components that have traditionally been required. An online calibration scheme of the resistance was proposed based on measurements of the small-signal resistance through the injection of down-up-up-down current pulses at the switching node. Following single-point calibration, a prototype PCBA achieved a RMSE of $0.536\,\mathrm{A}$ at $109\,\mathrm{A}$ pk-pk during a $20\,\%$ ramp in channel resistance.

However, there are several challenges that must be addressed before practical application. The origin of offset and gain errors in the resistance measurement has not yet been confirmed, along with a $\pm 0.5\,\%$ resistance fluctuation when the load inverter is in a high state. Furthermore, the miniaturisation of the measurement circuitry into an integrated circuit has not yet been thoroughly explored.

Fortunately, several results were found that may help tackle these challenges. First, the dynamics of the temperature dependency were shown to be slow. This means that future work could trade bandwidth for a higher noise budget. Second, it was shown that the current injection could have highly resistive behaviour, to the point where it could be implemented with only a switched resistance. This gives future efforts considerable design freedom, including the ability to inject long current pulses without a power penalty. Finally, many error sources were analytically modelled, easing future tradeoff studies.

In conclusion, this work demonstrated the viability of integrating precision current sensing and resistance monitoring into smart gate drivers and provides a solid foundation for future efforts. With continued refinement and further investigation, the benefits of integration could be brought to motor drivers in a wide range of applications.

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A

Selected derivations

A.1. Small-signal source resistance acts as drain resistance in triode region

Section 2.2.3 discusses the need to include the source and drain resistance into the model of the mosfet on-resistance gate voltage dependency. The resistance at the drain does not affect the gate-source voltage and thus adds to the device resistance. However, since the source resistance does affect the gate-source voltage, it is not obvious that it also adds linearly. The derivation below shows that it does.

Given a source resistance R_S:

$$I_D = \frac{W}{L} \cdot \mu C_{ox} \cdot \left(\left(V_{gs} - I_D R_S - V_{th}\right) \cdot \left(V_{ds} - I_D R_S\right) - \frac{\left(V_{ds} - I_D R_S\right)^2}{2} \right) = \tag{A.1}$$

$$= \frac{W}{L} \cdot \mu C_{ox} \cdot \left(\left(V_{gt} - I_D \cdot R_S\right) \cdot \left(V_{ds} - I_D \cdot R_S\right) - \frac{\left(V_{ds} - I_D \cdot R_S\right)^2}{2} \right) = \tag{A.2}$$

$$= \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{gt} V_{ds} + I_D^2 \cdot R_S^2 - I_D R_S \cdot \left(V_{gt} + V_{ds}\right) - \left(\frac{V_{ds}^2}{2} - V_{ds} I_d R_S + \frac{I_D^2 \cdot R_S^2}{2} \right) \right) = \tag{A.3}$$

$$= \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{gt} V_{ds} - \frac{V_{ds}^2}{2} + \frac{I_D^2 R_S^2}{2} - I_D R_S V_{gt} \right) = \tag{A.4}$$

$$= \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{gt} V_{ds} - \frac{V_{ds}^2}{2} - \left(V_{gt} I_D R_S - \frac{I_D^2 R_S^2}{2} \right) \right) \tag{A.5}$$

In which $V_{gt} = V_{gs} - V_{th}$. Then from implicit differentiation:

$$1 = \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{gt} \frac{\partial V_{ds}}{\partial I_D} - V_{ds} \cdot \frac{\partial V_{ds}}{\partial I_D} - \left(V_{gt} - I_D R_S\right) \cdot R_S \right) \tag{A.6}$$

So that for small $V_{ds} \to 0$ where $I_D \to 0$:

$$1 = \frac{W}{L} \cdot \mu C_{ox} \cdot \left(V_{gt} \frac{\partial V_{ds}}{\partial I_D} - V_{gt} R_S \right) \quad \Rightarrow \quad R = \frac{\partial V_{ds}}{\partial I_D} = \frac{1}{\frac{W}{L} \cdot \mu C_{ox} \cdot V_{gt}} + R_S \tag{A.7}$$

Hence, both the drain and source resistances add linearly.

A.2. The error due to temperature ramps has an upper bound

Switching device have thermal models that are usually specified as an equivalent circuit consisting of a concatenation of RC filters. First, observe that removing power flow to subsequent stages creates a more pessimistic estimate, since it causes more power to flow through the same impedance. Then an upper bound can found if all the power flows through only the first RC stage:

$$\Delta T_{max,0} < P_{max} \cdot \left(\frac{1}{\Delta t_{sample,R} \cdot C_0} + R_0 \right) \tag{A.8}$$

In which P_{max} is the maximum power dissipated by the switch in W, $\Delta t_{sample,R}$ is the time between resistance samples in s, R_0 is the resistance of the first stage in Ω, and C_0 is the capacitance of the first stage in F. A similar bound can be found for the second and subsequent RC stages. Notice that the temperature on any node cannot exceed the next

node by more than $P_{max} \cdot R_n$, since at most the full power can flow through the thermal resistance. These observations give rise to a family of upper bounds:

$$\Delta T_{max,i} < P_{max} \cdot \left(\frac{1}{\Delta t_{sample,R} \cdot \sum_{k=0}^{i} C_k} + \sum_{k=0}^{i} R_k \right) \tag{A.9}$$

In which the R_i and C_i correspond to the resistances and capacitances of each stage, and the capacitances of prior stages could be summed to the capacitance of the stage under consideration since they are charged to at least the same temperature as stage k. This makes considering a parallel connection a pessimistic assumption. The maximum temperature ramp is then obtained through finding the minimum of the bounds. The maximum resistance error can then be found via the maximum relative temperature coefficient:

$$\Delta \hat{I}_{thermal} < \left(\frac{\partial R}{\partial T} \right)_{max} \cdot \min_i P_{max} \cdot \left(\frac{1}{\Delta t_{sample,R} \cdot \sum_{k=0}^{i} C_k} + \sum_{k=0}^{i} R_k \right) \tag{A.10}$$

A.3. The variation in the resistance is slow compared to the measurement period

The temperature has a significant third harmonic. In the worst case, all of the temperature variation is in this harmonic, and a sample is taken on its peak. Then the peak uncompensated resistance error is:

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \frac{\Delta T_{pk-pk}}{2} \cdot (\cos(3\omega T) - 1) \approx \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \frac{\Delta T_{pk-pk}}{4} \cdot (3\omega T))^2 \quad \Rightarrow \quad \omega T \lessapprox \frac{2}{3} \cdot \sqrt{\frac{\Delta R/R}{\Delta T_{pk-pk}} \cdot \left(\frac{1}{R} \frac{\partial R}{\partial T} \right)^{-1}}$$

For the worst case, in a low thermal resistance device at a high frequency:

$$\omega T \lessapprox \frac{2}{3} \cdot \sqrt{\frac{1}{1\,°\mathrm{C}} \cdot \left(0.01\,°\mathrm{C}^{-1} \right)^{-1} \cdot 0.1\%} = 0.2$$

Which for $f_s > 6 f_m$ does not pose a restriction for the measurement period.

A.4. It is always possible to construct a signal orthogonal to any polynomial of a given order

A generative inductive proof will now be given for the fact that there is an infinite choice of $\delta i(t)$ that are orthogonal to any polynomial $P_N(\vec{\alpha}; t)$ of order N. First, observe that:

1. $P_N(\vec{\alpha}; t - \Delta t) = P_N(\vec{\alpha}'; t)$: shifting a polynomial in time preserves order but changes coefficients.
2. $a \cdot P_N(\vec{\alpha}; t - \Delta t) = P_N(a \cdot \vec{\alpha}; t)$: scaling a polynomial preserves order but changes coefficients.

Now, observe that on symmetric intervals any even monomonial is orthogonal to point-symmetric functions:

$$\begin{aligned}
f(t) = -f(-t) \Rightarrow \int_{-T}^{T} f(t) \cdot t^{2k} \,\mathrm{d}t &= \\
= \int_{-T}^{0} f(t) \cdot \left(t^2\right)^k \,\mathrm{d}t + \int_{0}^{T} f(t) \cdot \left(t^2\right)^k \,\mathrm{d}t &= \\
= -\int_{T}^{0} f(-u) \cdot \left(u^2\right)^k \,\mathrm{d}u + \int_{0}^{T} f(t) \cdot \left(t^2\right)^k \,\mathrm{d}t &= \\
= -\int_{0}^{T} f(u) \cdot \left(u^2\right)^k \,\mathrm{d}u + \int_{0}^{T} f(t) \cdot \left(t^2\right)^k \,\mathrm{d}t &= 0
\end{aligned}$$

Similarly, on symmetric intervals any odd monomonial is orthogonal to even functions:

$$
\begin{aligned}
f(t) = f(-t), (-x)^k = -x^k \Rightarrow \int_{-T}^{T} f(t)\cdot t^k \,\mathrm{d}t &= \\
= \int_{-T}^{0} f(t)\cdot t^k \,\mathrm{d}t + \int_{0}^{T} f(t)\cdot t^k \,\mathrm{d}t &= \\
= -\int_{T}^{0} f(-u)\cdot (-u)^k \,\mathrm{d}u + \int_{0}^{T} f(t)\cdot t^k \,\mathrm{d}t &= \\
= \int_{T}^{0} f(u)\cdot u^k \,\mathrm{d}u + \int_{0}^{T} f(t)\cdot t^k \,\mathrm{d}t &= \\
= -\int_{0}^{T} f(u)\cdot u^k \,\mathrm{d}u + \int_{0}^{T} f(t)\cdot t^k \,\mathrm{d}t &= 0
\end{aligned}
$$

Hence, say a function $f_{n-1}(t)$ with support $t \in \{T_0, T_1\}\}$ is orthogonal to any polynomial $P_{n-1}(\vec{\alpha}; t)$ of order $n-1$. Then:

$$
\int_{-\infty}^{\infty} f_{n-1}(t)\cdot P_{n-1}(\vec{\alpha}; t)\,\mathrm{d}t = 0
$$

Then the shift $\Delta T = -(T_0 + T_1)/2$ maps f_{n-1} to a function $f'_{n-1}(t)$ that has a symmetric support $t \in \{-T, T\}\}$. Since any shift or scaling in f can be transformed to a shift or scaling of the polynomial, which yields another polynomial, any shifted or scaled version of f_{n-1} is also orthogonal to the polynomial. In particular, $f'_{n-1}(t)$ is orthogonal to the polynomial. Any polynomial of order N can be decomposed in a monomonial of order N and polynomial of order $N-1$. There are two cases:

- If the monomonial is even, the function $f_n = f'_{n-1}(t+T) - f'_{n-1}(T-t)$ is orthogonal to the monomonial (by the first symmetry property), and to the polynomial of lower order (by definition of f'_{n-1}). Hence, it is orthogonal to the polynomonial of order N.
- If the monomonial is odd, the function $f_n = f'_{n-1}(t+T) + f'_{n-1}(T-t)$ is orthogonal to the monomonial (by the first symmetry property), and to the polynomial of lower order (by definition of f'_{n-1}). Hence, it is orthogonal to the polynomonial of order N.

Any function is orthogonal to a polynomial of order -1, as $P_{-1}(;t) = 0$. Hence, by perfect mathematical induction, there is an infinite set of $\Delta i(t)$ which are orthogonal to the polynomial of order N.

A.5. Resistive current injection does not significantly degrade interference robustness

The error due to the degradation of the orthogonality properties is given by:

$$
\begin{aligned}
\delta i_G &= \frac{\int_{-T}^{T} x(t)\cdot \delta i(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta x(t)\,\mathrm{d}t} \\
\Delta\hat{R} &= \frac{\int_{-T}^{T} x(t)\cdot v(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta i(t)\,\mathrm{d}t} - \frac{\int_{-T}^{T} x(t)\cdot v(t)\big|_{\delta i(t)=\delta i_G\cdot x(t)}\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta i(t)\,\mathrm{d}t}
\end{aligned}
\qquad \text{(equation (3.13))}
$$

The monitored injected current is given by:

$$
\delta i(t) = \delta i(t)\big|_{G(t)=0} - G_{vary}\cdot u\left(\delta i(t)\big|_{G(t)=0}\right)\cdot I(t)R \qquad \text{(equation (3.11))}
$$

First, observe that the error component is entirely due to the second term. Considering that $\delta i(t)\big|_{G(t)=0} = \delta i \cdot x(t)$, and taking $\delta i(t) = \delta i(t)\big|_{G(t)=0}$:

$$
\delta i_G = \frac{\int_{-T}^{T} x(t)\cdot \delta i\cdot x(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta x(t)\,\mathrm{d}t} = \delta i \qquad \text{(A.11)}
$$

$$
\Delta\hat{R} = \frac{\int_{-T}^{T} x(t)\cdot R(t)\cdot(\delta i\cdot x(t) + I(t))\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta i\cdot x(t)\,\mathrm{d}t} - \frac{\int_{-T}^{T} x(t)\cdot R(t)\cdot(\delta i\cdot x(t) + I(t))\,\mathrm{d}t}{\int_{-T}^{T} x(t)\cdot \delta i\cdot x(t)\,\mathrm{d}t} = 0 \qquad \text{(A.12)}
$$

Then the error is due to the conductive component. In the worst case, the conductive component dominates the error, which is given by:

$$\delta i_G = \frac{\int_{-T}^{T} x(t) \cdot -G_{vary}(t) \cdot u\left(x(t)\right) \cdot I(t)R(t)\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot \delta x(t)\,\mathrm{d}t} =$$

$$= -\frac{1}{a}\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t \tag{A.13}$$

$$\Delta\hat{R} = \frac{\int_{-T}^{T} x(t) \cdot R(t) \cdot \left(-G_{vary}(t) \cdot u\left(x(t)\right) \cdot I(t)R(t) + I(t)\right)\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot -G_{vary}(t) \cdot u\left(x(t)\right) \cdot I(t)R(t)\,\mathrm{d}t} - \frac{\int_{-T}^{T} x(t) \cdot R(t) \cdot (\delta i_G \cdot x(t) + I(t))\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot \delta i_G \cdot x(t)\,\mathrm{d}t} =$$

$$= \frac{\int_{-T}^{T} x(t) \cdot R(t) \cdot \left(-G_{vary}(t) \cdot x_2(t) \cdot I(t)R(t) + I(t)\right)\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot -G_{vary}(t) \cdot x_2(t) \cdot I(t)R(t)\,\mathrm{d}t} - \frac{\int_{-T}^{T} x(t) \cdot R(t) \cdot (\delta i_G \cdot x(t) + I(t))\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot -G_{vary}(t) \cdot x_2(t) \cdot I(t)R(t)\,\mathrm{d}t} =$$

$$= \frac{\int_{-T}^{T} x(t) \cdot R(t) \cdot \left(x_2(t) \cdot G_{vary}(t)I(t)R(t) - x(t) \cdot \frac{1}{a}\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t\right)\,\mathrm{d}t}{\int_{-T}^{T} x(t) \cdot G_{vary}(t) \cdot x_2(t) \cdot I(t)R(t)\,\mathrm{d}t} \tag{A.14}$$

In which $x_2(t) = u(x(t))$ and a is the length of nonzero $x(t)$. Taking $x(t) = x_2(t) - x_1(t)$:

$$\Delta\hat{R} = \frac{\int_{-T}^{T} (x_2(t) - x_1(t)) \cdot R(t) \cdot \left(x_2(t) \cdot G_{vary}(t)I(t)R(t) - (x_2(t) - x_1(t)) \cdot \frac{1}{a}\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t\right)\,\mathrm{d}t}{\int_{-T}^{T} (x_2(t) - x_1(t)) \cdot G_{vary}(t) \cdot x_2(t) \cdot I(t)R(t)\,\mathrm{d}t} =$$

$$= \frac{\int_{-T}^{T} (x_2(t) - x_1(t)) \cdot R(t) \cdot \left(x_2(t) \cdot G_{vary}(t)I(t)R(t) - (x_2(t) - x_1(t)) \cdot \frac{1}{a}\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t\right)\,\mathrm{d}t}{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t} =$$

$$= \frac{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)\left(R(t)\right)^2 I(t) - R(t) \cdot (x_2(t) - x_1(t))^2 \cdot \frac{1}{a} \cdot \left(\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t\right)\,\mathrm{d}t}{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t} =$$

$$= \frac{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)\left(R(t)\right)^2 I(t)\,\mathrm{d}t}{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t} - \frac{1}{a} \cdot \int_{-T}^{T} R(t) \cdot (x_2(t) - x_1(t))^2\,\mathrm{d}t =$$

$$= \frac{\int_{-T}^{T} R(t) \cdot x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t}{\int_{-T}^{T} x_2(t) \cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t} - R - \frac{\int_{-T}^{T} \delta R \cdot \left(\delta i(t)\big|_{G(t)=0}\right)^2\,\mathrm{d}t}{\int_{-T}^{T} \left(\delta i(t)\big|_{G(t)=0}\right)^2\,\mathrm{d}t} \tag{A.15}$$

The last term is the orthogonality relation to bulk resistance error, which is insignificant as explained in section 3.3.2. The first term is the weighted average of the resistance over the monitored injected current. The error can be estimated

using a small fluctuation model:

$$
\begin{aligned}
&\frac{\int_{-T}^{T} R(t)\cdot x_2(t)\cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t}{\int_{-T}^{T} x_2(t)\cdot G_{vary}(t)R(t)I(t)\,\mathrm{d}t} - R && = \\
&= \frac{\int_{-T}^{T} (R+\delta R(t))\cdot x_2(t)\cdot \left(G_{vary}+\delta G_{vary}(t)\right)\cdot (R+\delta R(t))\cdot (I+\Delta I(t))\,\mathrm{d}t}{\int_{-T}^{T} x_2(t)\cdot \left(G_{vary}+\delta G_{vary}(t)\right)\cdot (R+\delta R(t))\cdot (I+\Delta I(t))\,\mathrm{d}t} - R && \approx \\
&\approx \frac{\int_{-b}^{b} R\cdot \left(G_{vary}RI + G_{vary}R\Delta I + \delta G_{vary}(t)RI + 2G_{vary}\delta R(t)I + \delta G_{vary}(t)R\Delta I(t) + 2G_{vary}\delta R(t)\Delta I(t)\right)\mathrm{d}t}{\int_{-b}^{b} \left(G_{vary}RI + G_{vary}R\Delta I + \delta G_{vary}(t)RI + G_{vary}\delta R(t)I + \delta G_{vary}(t)R\Delta I(t) + G_{vary}\delta R(t)\Delta I(t)\right)\mathrm{d}t} - R && = \\
&= R\cdot\left(\frac{\int_{-b}^{b} \left(G_{vary}RI + G_{vary}R\Delta I(t) + \delta G_{vary}(t)RI + 2G_{vary}\delta R(t)I + \delta G_{vary}(t)R\Delta I(t) + 2G_{vary}\delta R(t)\Delta I(t)\right)\mathrm{d}t}{\int_{-b}^{b} \left(G_{vary}RI + G_{vary}R\Delta I(t) + \delta G_{vary}(t)RI + G_{vary}\delta R(t)I + \delta G_{vary}(t)R\Delta I(t) + G_{vary}\delta R(t)\Delta I(t)\right)\mathrm{d}t} - 1\right) && = \\
&= R\cdot\frac{\int_{-b}^{b} G_{vary}\delta R(t)I + G_{vary}\delta R(t)\Delta I(t)\,\mathrm{d}t}{\int_{-b}^{b} \left(G_{vary}RI + G_{vary}R\Delta I(t) + \delta G_{vary}(t)RI + G_{vary}\delta R(t)I + \delta G_{vary}(t)R\Delta I(t) + G_{vary}\delta R(t)\Delta I(t)\right)\mathrm{d}t} && = \\
&= R\cdot\frac{\int_{-b}^{b} G_{vary}\delta R(t)\cdot (I+\Delta I(t))\,\mathrm{d}t}{\int_{-b}^{b} \left(G_{vary}R + \delta G_{vary}(t)R + G_{vary}\delta R(t)\right)\cdot (I+\Delta I(t))\,\mathrm{d}t} && = \\
&= R\cdot\left(\frac{\int_{-b}^{b} \left(G_{vary}R + \delta G_{vary}(t)R\right)\cdot (I+\Delta I(t))\,\mathrm{d}t}{\int_{-b}^{b} G_{vary}\delta R(t)\cdot (I+\Delta I(t))\,\mathrm{d}t} + 1\right)^{-1} && \approx \\
&\approx R\cdot\left(\frac{\int_{-b}^{b} G_{vary}RI + \delta G_{vary}(t)R\Delta I(t)\,\mathrm{d}t}{\int_{-b}^{b} G_{vary}\delta R(t)\Delta I(t)\,\mathrm{d}t} + 1\right)^{-1} && = \\
&= R\cdot\left(\frac{\int_{-b}^{b} I + \frac{\delta G_{vary}(t)}{G_{vary}}\cdot\Delta I(t)\,\mathrm{d}t}{\int_{-b}^{b} \frac{\delta R(t)}{R}\cdot\Delta I(t)\,\mathrm{d}t} + 1\right)^{-1} && \text{(A.16)}
\end{aligned}
$$

In which $I(t) = I + \Delta I(t)$ was taken, because the fluctuation plays a dominant role for $I \to 0$ so that correlations with other variables can not be ignored. The second approximation follows from the fact that $\delta R(t)$ and $\Delta I(t)$ are both highly linear, as argued in section 3.3.2. That makes their correlation with constant variables insignificant, due to the symmetric integration domain. Instead, the product of constant variables and the quadratic product of linear variables dominate. The error is insignificant when expression in brackets is large, certainly much higher than 1. This is the case when the quotient is large:

$$
\begin{aligned}
\frac{\int_{-b}^{b} I + \frac{\delta G_{vary}(t)}{G_{vary}}\cdot\Delta I(t)\,\mathrm{d}t}{\int_{-b}^{b} \frac{\delta R(t)}{R}\cdot\Delta I(t)\,\mathrm{d}t} &\approx \frac{2bI + \frac{2b^3}{3}\cdot\frac{1}{G_{vary}}\frac{\partial G_{vary}}{\partial t}\cdot\frac{\partial I}{\partial t}}{\frac{2b^3}{3}\cdot\frac{1}{R}\frac{\partial R}{\partial t}\cdot\frac{\partial I}{\partial t}} = \frac{\frac{3}{4}T_{inj}^{-2}I\cdot\left(\frac{\partial I}{\partial t}\right)^{-1} + \frac{1}{G_{vary}}\frac{\partial G_{vary}}{\partial t}}{\frac{1}{R}\frac{\partial R}{\partial t}} \approx \\
&\approx \frac{\frac{3}{4}\cdot(1\,\mu\mathrm{s})^{-2}\cdot I\cdot\left(-5\,\mathrm{A}\,\mu\mathrm{s}^{-1}\right)^{-1} + 0.1\,\%\,\mu\mathrm{s}^{-1}\cdot\alpha}{0.7\,\%\,\mu\mathrm{s}^{-1}} = -21\cdot I + 0.1\cdot\alpha \qquad \text{(A.17)}
\end{aligned}
$$

In which T_{inj} is the total injection time (excluding settling) and $\alpha \in [-1, 1]$ is a normalised correlation coefficient. For the maximum current of $I = 100\,\mathrm{A}$, the error is smaller than $0.05\,\%$. For smaller currents, the error grows linearly. However, this does not couple to bigger outputs in the estimated current, since the influence of resistive errors also decreases linearly with current. Using the error model from section 2.1:

$$
\Delta\hat{I}_{RMS} \approx \sqrt{\frac{1}{T}\int_0^T (i(t))^2\cdot\frac{\left(\kappa\cdot\frac{R}{i(t)}\right)^2}{R^2}\,\mathrm{d}t} = \sqrt{\frac{1}{T}\int_0^T \kappa^2\,\mathrm{d}t} = \kappa \approx 47\,\mathrm{mA} \qquad \text{(A.18)}
$$

For small currents, such as $I < 100\,\mathrm{mA}$, the error is no longer well behaved, and the error may grow unbounded depending on the relative size of the errors.

In conclusion, if the injected current is monitored the error due to output conductance is not significant for nearly all the load current range, except for some currents close to $0\,\mathrm{A}$.