ASIC Design for a Single-Cable 64-Element Ultrasound Probe

van Willigen, D.M.; Janjic, Jovana; Kang, Eunchul; Chang, Zu Yao; Noothout, Emile; Verweij, Martin; de Jong, Nicolaas; Pertijs, Michiel

DOI
10.1109/ULTSYM.2018.8580162

Publication date
2018

Document Version
Final published version

Published in
2018 IEEE International Ultrasonics Symposium (IUS)

ASIC Design for a Single-Cable 64-Element Ultrasound Probe

Douwe van Willigen*, Jovana Janjic†, Eunchul Kang*, Zu Yao Chang*,
Emile Noothout‡, Martin Verweij†‡, Nicolaas de Jong†‡ and Michiel Pertijs*

*Electronic Instrumentation Lab., Delft University of Technology, Delft, the Netherlands
†Dept. of Biomedical Engineering, Erasmus MC, Rotterdam, the Netherlands
‡Lab. of Acoustical Wavefield Imaging, Delft University of Technology, Delft, the Netherlands

Email: d.m.vanwilligen@tudelft.nl

***Abstract*—This paper presents an ASIC (Application Specific Integrated Circuit) design for a catheter probe that interfaces 64 piezoelectric elements directly integrated on top of the ASIC to an imaging system using a single micro-coaxial cable. Each of the piezo elements can be used for both transmit (TX) and receive (RX), enabling full synthetic aperture imaging. A prototype has been realized with a 1.5 mm diameter circular layout, intended for 3D intra-vascular ultrasound imaging. The functionality of this ASIC has been successfully demonstrated in a 3D imaging experiment. The design allows a single-element transducer to be replaced by a transdcuer array while using the same cable, making it a promising solution for 3D imaging with size constrained probes.**

***Index Terms*—Intravascular ultrasound, front-end ASIC, cable count reduction, single cable**

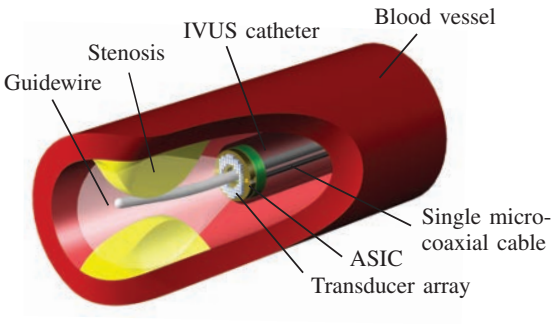

Fig. 1: Artist impression of the ASIC mounted onto a catheter.

I. Introduction

The large number of elements needed in 3D medical ultrasound probes calls for a reduction in the amount of cables interfacing the probe with the imaging system [1]–[3]. Especially in catheter-based ultrasound devices, it is valuable to keep the number of interface connections limited to facilitate a more flexible probe shaft and leave room for a guide-wire.

In this work we present a front-end ASIC for forward-looking intra-vascular ultrasound (FL-IVUS) probes. FL-IVUS probes are important for the diagnosis and treatment of chronic total occlusions [4]. They typically employ a mechanically-rotated single-element transducer to image the artery. 3D imaging without rotation is desirable to simplify the mechanical design and reduce the artefacts caused by the rotation, but requires the integration of an array of tens of transducer elements at the catheter's tip. Directly wiring these elements in a small catheter is undesirable due to the increased stiffness and the high cost of connecting the micro-coaxial cables.

A probe that uses a single-cable connection, but can still produce 3D ultrasound images is interesting as it can replace current single-element probes by a matrix array with 3D-imaging capabilities without changing the cable infrastructure. This work shows a prototype ASIC that can connect 64 piezo elements (PZT, 13 MHz) to an imaging system using a single micro-coaxial cable. Fig. 1 shows an artist impression of the ASIC mounted onto a catheter.

II. ASIC Architecture

A prototype ASIC has been designed to transmit and receive with a matrix of 64 PZT transducer elements. The ASIC can be connected to an imaging system using an additional circuit on the system side to drive, configure and read out the ASIC. The ASIC cycles through three modes: First configuration data can be sent to the ASIC to select the channels for the upcoming transmit-receive cycle. Then a high-voltage transmit (TX) pulse is applied to the cable to send an acoustic pulse with one or multiple piezo transducer elements. After the transmit pulse, the circuit switches to receive (RX) mode, amplifying the current generated in the piezo material by the received echoes of a selected channel. The amplified current is sent over the cable which also provides a supply voltage to the ASIC.

In Fig. 2 a block diagram of the ASIC is depicted. The ASIC is powered by a DC voltage of 3 V in receive mode and when configuring the ASIC. Programmable switches S_{tx} and S_{rx} allow each element to be connected to the cable for TX, or to an LNA for RX. To configure the switches, pulse-width modulated (PWM) data (500 $\mathrm{mV_{pp}}$) is superimposed on the power supply. The data is recovered on the ASIC by

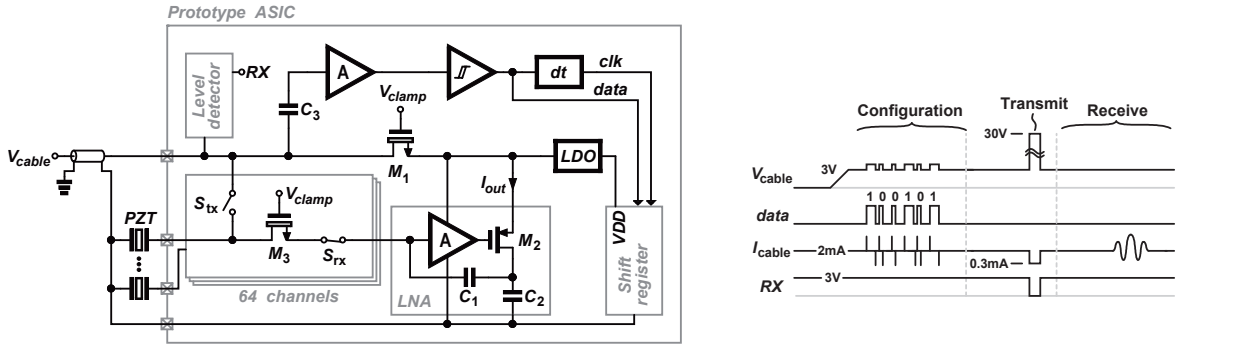

Fig. 2: Block diagram of the prototype ASIC and some of the corresponding waveforms.

AC coupling (C_3), amplifying and thresholding, and then used to load a configuration shift register. A low-dropout (LDO) regulator prevents the modulated supply from affecting the operation of the associated logic. After configuration, a high voltage TX signal with a maximum peak amplitude of 30 V can be supplied to the cable, which will drive the elements selected for TX to generate an acoustic pulse. Compared to using on-chip pulsers [2], [5], this is more power efficient, and allows the pulse waveform to be defined on the system side. Clamping transistors M_1 and M_3 protect the low-voltage circuitry, by ensuring that their source voltage doesn't rise above V_{clamp}. A bias circuit (not shown) generates bias currents and the clamping voltage V_{clamp}, which is stored on a capacitor during TX, when a stable supply voltage is absent. When a level detector senses that V_{cable} is below 6 V longer than 200 ns, the ASIC switches back to RX phase by turning off the TX switches and enabling the LNA. In the receive phase, a DC voltage of 3 V on the cable powers the ASIC. The acoustic echoes received by the element selected for RX create a small signal-current that is amplified by the LNA and returned to the system superimposed on the supply current. The supply current is a constant offset, because the logic is quiet in this period, and can therefore easily be filtered out on the system side. Compared to the conventional solution of driving the cable with a signal voltage [5], which requires that the ASIC drives the cable capacitance, this current mode signalling is more power efficient.

III. Circuit Implementation

A. Receive Electronics

In receive mode one of the 64 elements is connected to the LNA by a multiplexer that is controlled by the shift register. The LNA has a current gain $I_{\mathrm{out}}/I_{\mathrm{in}}$ of $1+C_2/C_1$ [6], where C_1 can be switched to program the gain in two 6 dB steps. To obtain an input noise level around 1 pA/$\sqrt{\mathrm{Hz}}$, the LNA including output transistor M_2 consumes about 1.5 mA. Output transistor M_2 generates the desired signal-dependent supply current (I_{out}).

B. Transmit Electronics

In the transmit phase, latched transmit switches are used to pass the signal on the cable to the selected piezo elements. Fig. 3 shows the circuit implementation of the TX switches. During configuration, the data bit that controls the switch is sampled and held on capacitor C_6, turning M_5 on or off. When M_5 is on, C_4 and C_5 form a capacitive divider, causing M_4 to turn on with a safe gate voltage when a high-voltage pulse is applied. If M_5 is off, the parasitic capacitance of M_5, C_{p}, appears in series with C_5. Because C_4 and C_5 are much larger than this parasitic capacitance, the gate-source voltage on M_4 now remains small when a high-voltage pulse is applied, ensuring that the TX switch stays off. This switch structure does not require a supply voltage during TX, and is substantially smaller (7300 µm^2) than conventional level-shifter based switches, allowing 64 switches to be integrated on the ASIC.

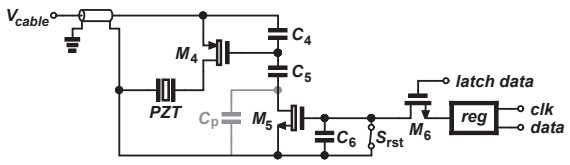

Fig. 3: Circuit implementation of latching transmit switch.

C. System-Side Circuitry

An additional circuit is used to connect the ASIC to a conventional imaging system and program the shift registers. Fig. 4 shows a simplified diagram of this system-side circuit. During RX, a trans-impedance amplifier (TIA) is used to supply the ASIC with a fixed supply voltage (V_{sup}) while at the same time converting the amplified signal current to a voltage V_{RX} with a trans-impedance gain set by R_1. Resistor R_2 is used to match the cable impedance, while capacitor C_8 rejects the DC component associated with the ASIC's supply current. To configure the ASIC, the PWM-encoded data V_{data} is added to V_{sup}, causing the virtual ground of the TIA to follow this signal, thus transmitting it over the coaxial cable to the ASIC.

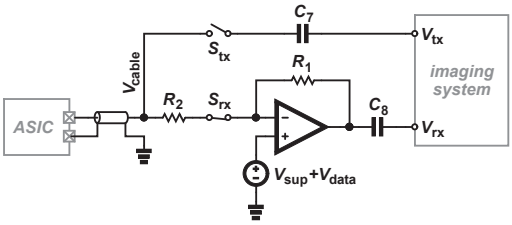

Fig. 4: Simplified diagram of the system-side circuit to interface the ASIC with a conventional imaging system.

In the transmit phase, the high voltage signal V_{TX} generated by the system is AC-coupled to the cable.

IV. Fabrication

The ASIC has been fabricated in a 0.18 µm BCD process (Fig. 5a). Its 1.5 mm diameter circular shape will in a later stage be laser cut out to fit into the catheter's diameter. A central 0.5 mm circle is left empty to accommodate a guidewire. The two square bondpads inside the circular sealring are the connections to the cable, the octagonal bondpads are used for the piezo transducers and the bondpads on the edge are for test purposes. For initial tests an array of 64 100 µm-pitch PZT transducer elements with a center frequency of 13 MHz has been built on the ASIC using the approach of [7] (Fig. 5b). The center hole is covered by dummy elements to simplify fabrication for the initial prototype. The ASIC was then wire bonded to a printed circuit board (PCB) for electrical and acoustical characterization and a ground foil was glued to provide a ground connection to the array elements (Fig. 5c).

V. Electrical Characterization

The ASIC was first tested electrically by wire-bonding it to a PCB. Fig. 6 shows the RX transfer function measured by injecting a signal current into the LNA through a test input of the RX multiplexer and recording the current sensed by the TIA on the system side. The 3 dB-bandwidth of 21 MHz and 12 dB programmable gain are in good agreement with simulations and are suitable for the IVUS application.

Fig. 7 shows a measurement of the system side output voltage for different input current levels. The noise floor of the amplifier, visible in the bottom left of the plot, is below the expected noise floor of the piezo transducers (4.5 nA RMS). From the plot we can derive that the system has a dynamic range of about 71 dB, including the 2 gain steps.

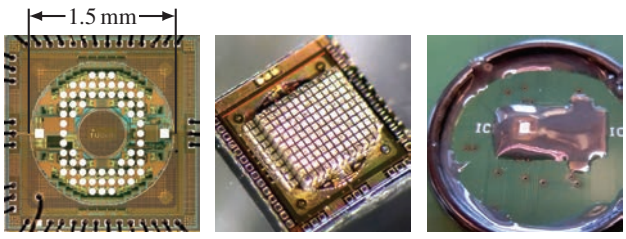

Fig. 5: (a) Die micrograph of the fabricated ASIC, (b) ASIC with piezo transducers (before placing the ground-foil) and (c) completed ultrasound ASIC on a PCB.

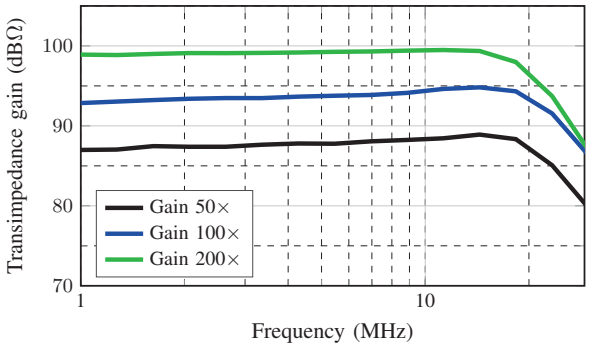

Fig. 6: Transfer function for the 3 gain settings.

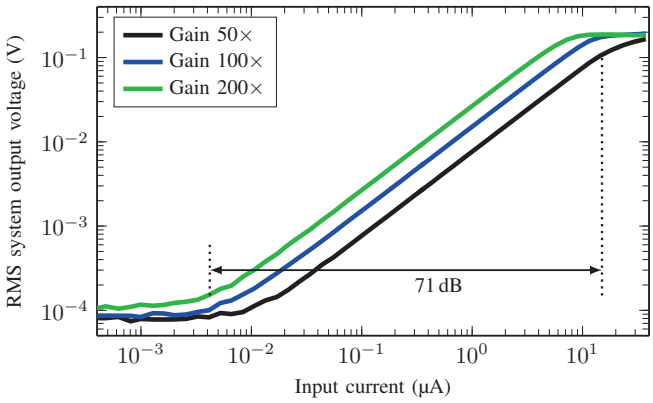

Fig. 7: Dynamic range measurement of the electrical input.

VI. Experimental Results

To measure the performance of the ASIC in its intended application, the ASIC was connected to the system side circuit using a single 1.5 m long AWG-42 coaxial cable. For acoustic characterization, a small water bag was mounted on top of the ASIC (Fig. 10). A pulse-echo experiment with a plate reflector, shown in Fig. 8, shows that the amplitude of the echo received by one element increases with the number of elements selected for TX, demonstrating effective switching of the applied 30 V pulses.

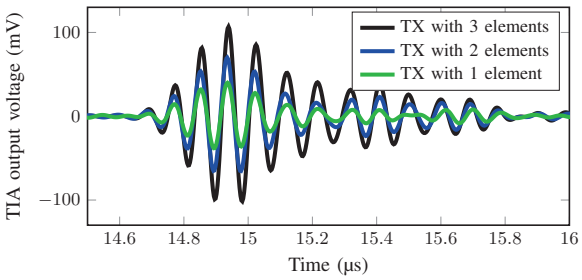

Fig. 8: Measured echo with one or multiple elements used for TX.

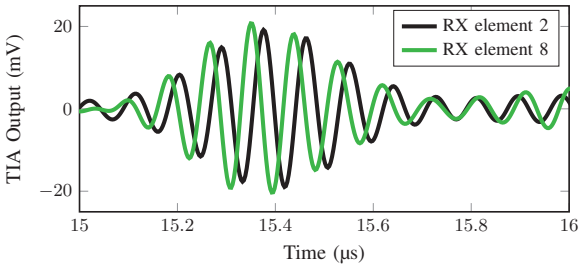

Fig. 9: Measured echo of two individual non-adjacent elements.

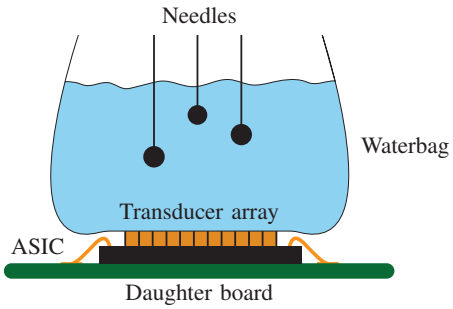

Fig. 10: Waterbag with needle phantom mounted on top of the ASIC.

The echoes received by two different elements also show the expected arrival time difference (Fig. 9).

A needle phantom consisting of 3 needles at different depths was placed in the waterbag (Fig. 10) and an imaging experiment was performed by successively pulsing the 64 elements and successively capturing the echoes received by all 64 elements.

A projection of the volumetric image was obtained with a full synthetic aperture acquisition scheme. The image, shown in Fig. 11, clearly shows the three needles placed in front of the array. The artefacts visible in the image are to be expected for the regular array topology and chosen imaging algorithm.

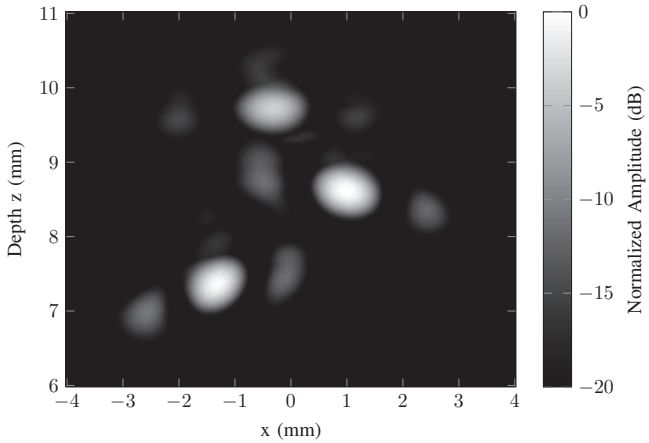

Fig. 11: Maximum projection of a 3D image of the needle phantom, reconstructed using synthetic aperture beamforming.

VII. Conclusion

This work shows that it is possible to perform 3D imaging with a transducer array that is interfaced to an imaging system by an ASIC using only a single cable connection. It enables 3D imaging in probes in which single-element transducers have been used before. The performance is comparable to state-of-the art work, at the cost of a reduction in frame-rate. The same cable is used to power the ASIC, configure switches, send high voltage transmit pulses and receive echo signals. An LNA has been proposed that outputs a signal current to return the echo signal to the imaging system in a power-efficient manner. A new latching high voltage switch has been designed to reduce the area required by the high voltage switches.

In imaging experiments with a needle phantom the successful operation of the ASIC has been shown by reconstructing an image of a needle phantom.

This work showed the first ASIC that interfaces a transducer array via a single micro-coaxial cable, with the potential of greatly simplifying the realization of catheter-based 3D imaging devices.

References

[1] J. Janjic, M. Tan *et al.*, "A 2D Ultrasound Transducer with Front-End ASIC and Low Cable Count for 3D Forward-Looking Intravascular Imaging: Performance and Characterization," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, 2018.

[2] C. Tekes, T. Xu *et al.*, "Real-time imaging system using a 12-MHz forward-looking catheter with single chip CMUT-on-CMOS array," in *Proceedings of the 2015 IEEE International Ultrasonics Symposium (IUS)*. IEEE, 2015.

[3] M. Tan, C. Chen *et al.*, "A Front-End ASIC With High-Voltage Transmit Switching and Receive Digitization for 3-D Forward-Looking Intravascular Ultrasound Imaging," *IEEE Journal of Solid-State Circuits*, no. 99, pp. 1–14, 2018.

[4] B. K. Courtney, N. R. Munce *et al.*, "Innovations in imaging for chronic total occlusions: a glimpse into the future of angiography's blind-spot," *European heart journal*, vol. 29, no. 5, pp. 583–593, 2008.

[5] G. Gurun, C. Tekes *et al.*, "Single-chip CMUT-on-CMOS front-end system for real-time volumetric IVUS and ICE imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 61, no. 2, pp. 239–250, 2014.

[6] B. Razavi, "A 622 Mb/s 4.5 pA/$\sqrt{}$Hz CMOS transimpedance amplifier [for optical receiver front-end]," in *Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International*. IEEE, 2000, pp. 162–163.

[7] C. Chen, S. B. Raghunathan *et al.*, "A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography," *IEEE transactions on ultrasonics, ferroelectrics, and frequency control*, vol. 63, no. 1, pp. 47–59, 2016.