Indirect Current Feedback Instrumentation Amplifier with a Common-Mode Input Range that Includes the Negative Rail

Bernard J. van den Dool and Johan H. Huijsing, Senior Member, IEEE

Abstract—An instrumentation amplifier is presented which can handle common-mode voltages that extend 200 mV below the negative supply. The extended range is combined with a commonmode rejection of 92 dB and an accuracy of 0.1%, without the need for on-chip trimming. This has been achieved by the use of two p-n-p V-to-I converters in an indirect current feedback configuration. The output voltage can reach the negative supply. The offset voltage is 0.3 mV, and the noise voltage is 30 nV/ \sqrt{Hz} . The circuit operates at supply voltages down to 2.5 V, and the quiescent current is 240 μ A. The instrumentation amplifier has been integrated in a semi-custom bipolar process.

I. INTRODUCTION

I N many electrical measurement systems there is a need for the amplification of small differential sensor voltages. However, the differential sensor signal is often accompanied by interference in the form of strong common-mode voltages at the inputs. Fig. 1 shows an example of a setup in which an instrumentation amplifier is used. A sensor generates the desired signal V_S and has a source resistance R_S . The sensor and the amplifier are often connected to a common ground terminal. If the sensor and the amplifier are separated some distance, a voltage V_{CM} will be present between the two ground connections. This common-mode (CM) voltage can drive the amplifier inputs below the amplifier ground rail.

The aim of the present design has been to build an instrumentation amplifier for the kind of application shown in Fig. 1. Examples of this setup can be found in automotive electronics and in battery-operated systems. Three important demands on the amplifier can be derived from Fig. 1. Firstly, the sensor signal V_S should be amplified accurately. Secondly, the common-mode interference must be rejected sufficiently. Thirdly, the common-mode input range must include ground, a feature that is not encountered in existing instrumentation amplifiers. Furthermore, the circuit should be simple and should not require on-chip trimming.

There are two basic approaches to the design of an instrumentation amplifier: resistive feedback and current feedback. The most significant difference between these approaches is the method by which a good common-mode rejection ratio (CMRR) is obtained. In the case of resistive feedback, a high

The authors are with the Electronic Instrumentation Laboratory, Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands.

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Fig. 1. Measurement system with sensor and instrumentation amplifier.



Fig. 2. Three-op-amp instrumentation amplifier.

CMRR requires a well-balanced resistor feedback network. Current feedback, on the other hand, uses both isolation and balancing techniques to obtain a good CMRR. The input part of the amplifier is designed to isolate the common-mode input voltage from the rest of the circuit. Because isolation will never be perfect, additional balancing is used to enhance the CMRR.

A widely used instrumentation amplifier with resistive feedback is shown in Fig. 2. The common-mode input voltage is passed on to nodes A and B. Therefore, relatively large common-mode currents will flow through R4 + R6 and R5 +R7 towards the output and ground nodes of the amplifier. Consequently, the resistor bridge needs to be trimmed well to obtain a good CMRR, which is a serious drawback of the resistive feedback instrumentation amplifier [1]. Another disadvantage of the three-op-amp instrumentation amplifier is that the outputs of op amp 1 and op amp 2 cannot become zero or negative and therefore the CM ranges of the amplifier cannot include ground.

An example of an instrumentation amplifier using current feedback is shown in Fig. 3 [2], [3]. Q1, Q2, and R1 form a V-to-I converter with transfer 1/R1. Feedback from the output is realized by another V-to-I converter Q3, Q4, R2 with transfer 1/R2. Loop amplifier A adjusts $V_{\rm OUT}$ so that $V_{\rm OUT}/V_{\rm IN} = R2/R1$. A disadvantage of this setup is that two accurate V-to-I converters are needed to obtain an accurate and linear transfer. Q1 and Q2 are linearized by the pres-

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Fig. 3. Current-feedback instrumentation amplifier.



Fig. 4. Indirect current-feedback instrumentation amplifier.

ence of loop amplifier A, which keeps the collector currents at a constant value. The second V-to-I converter must be linearized by using composite transistors for Q3 and Q4. A second disadvantage of the circuit of Fig. 3 is the stacking of the two V-to-I converters, which reduces the input CM range and does not permit a CM range that includes ground.

In the present design a more elegant configuration with current feedback has been used. It eliminates the disadvantages of the circuits shown in Figs. 2 and 3. The following section starts with an explanation of the principles of the used configuration. Then a complete circuit description is given. Measurement results are given in the fourth section and the paper ends with conclusions.

II. PRINCIPLE OF INDIRECT CURRENT FEEDBACK

In Fig. 4, the basic setup of the instrumentation amplifier is shown [4]–[6]. Transconductance stage T1 converts the input voltage into a current $i_1 = Gm_1 \cdot V_{IN}$ and the second transconductance stage T2 does the same with the attenuated output voltage. Loop amplifier A with high gain will make $i_1 - i_2 = 0$, and therefore the overall transfer function becomes

$$\frac{V_{\rm OUT}}{V_{\rm IN}} = \frac{Gm_1}{Gm_2} \cdot \frac{R3 + R4}{R4}.$$
 (1)

This method is called indirect current feedback, because the output voltage is not fed back directly to the input of the amplifier but to the input of a second input stage T^2 , and then the output currents of input stages T^1 and T^2 are compared and fed back to the loop amplifier. The resulting circuit resembles the current feedback circuit shown in Fig. 3, but now the V-to-I converters are no longer stacked on top of each other. The gain of the circuit shown in Fig. 4 can be set in two different ways. The first method takes $(R^3 + R^4)/R^4 = 1$ and sets the gain with resistors R^1



Fig. 5. Instrumentation amplifier with p-n-p V-to-I converters.

and R2. Both transconductance stages should be accurate and linear so that $Gm_1/Gm_2 = R2/R1$. The second method takes $Gm_1/Gm_2 = 1$ and sets the gain with R3 and R4. The advantage of this is that the absolute errors in Gm_1 and Gm_2 are not important, as long as Gm_1 and Gm_2 are well-matched and their ratio remains equal to one. This method has been used in the present design.

The advantage of the indirect current feedback method over the resistive feedback circuit shown in Fig. 2 is that the balanced resistor network, connecting the output to the input, has been eliminated. This does not mean that we now automatically have a good common-mode rejection. Rather, the problem of achieving a good CMRR has been shifted to the input stage T1. The input stage is also responsible for handling the common-mode input voltages below ground. Therefore, we take a closer look at the transconductance stages in the following section.

III. CIRCUIT DESCRIPTION

A. P-N-P Input Stages

A demand on the present design is that the commonmode input range includes ground. This can be achieved by using p-n-p differential pairs as transconductance stages at the input, as shown in Fig. 5, Q11, Q12, and R1 form the first transconductance stage T1, and the second transconductance stage T2 consists of Q21, Q22, and R2. To realize a current comparison, the collectors of the two stages are connected crosswise so that the currents are subtracted and the result is fed back in the correct polarity. The collector bias currents of the input stages flow to ground through R31 and R32. This biases the voltages across R31 and R32 at about 0.3 V. The input CM voltage can then exceed ground by about 0.2 V before forward-biasing the collector-base junctions of input stage Q11, Q12.

B. Common-Mode Rejection

The CMRR of the circuit shown in Fig. 5 is mainly determined by the input stage Q11, Q12, R1. In Fig. 6 the input stage is shown again. Both p-n-p transistors have been replaced by their small-signal model, with a base-emitter impedance, a controlled current source, and a collector impedance. The input of amplifier A is modeled by load resistor R_L . As indicated by the bold lines in Fig. 6, the base-emitter parts of the input stage



Fig. 6. Input stage with finite isolation.

are carrying the common-mode input voltage V_{CM} , which is floating between the four current sources. In the case of ideal isolation the CMRR is infinite. But the four current sources have finite impedances, hence common-mode currents will flow up through r_{I13} and r_{I14} and down through r_{o11} and r_{o12} . The four resistor values should be as large as possible, to approach the situation of perfect isolation. Additional matching of the left and right parts of the circuit helps to balance out the imperfections in isolation, and further improves commonmode rejection. In the present design the output impedances of the upper current sources have been made large by the use of emitter degeneration, so that they can be neglected. The CMRR determined by finite values of r_{o11} and r_{o12} can be found as follows. When neglecting R31 and R32, the voltage across r_{o11} equals V_{CM} . The resulting current is V_{CM}/r_{o11} and corresponds to an equivalent base-emitter voltage $V_{BE11} = V_{CM} \cdot r_{e11}/r_{o11}$. For r_{o12} we find in the same way $V_{BE12} = V_{CM} \cdot r_{e12}/r_{o12}$. Therefore the commonmode input voltage corresponds to a differential input voltage $V_{DM} = V_{BE11} - V_{BE12} = (r_{e11}/r_{o11} - r_{e12}/r_{o12})V_{CM}$. This results in a CM rejection:

$$\frac{1}{\text{CMRR}_{1}} = \frac{r_{e11}}{r_{o11}} - \frac{r_{e12}}{r_{o12}} = \frac{1}{\mu_{11}} - \frac{1}{\mu_{12}} \approx \frac{\Delta\mu}{\mu} \frac{1}{\mu} \quad (2)$$

where μ is the intrinsic transistor gain $\mu = g_m \cdot r_0 = V_{\text{EARLY}}/(kT/q)$ of the p-n-p input transistors and $\Delta \mu$ is the difference in voltage gain between Q11 and Q12. We call μ the isolation factor and $\Delta \mu/\mu$ the balancing factor. For an Early voltage of 25 V we find that μ is approximately 1000. If $\Delta \mu/\mu$ is approximately 2%, without on-chip trimming, this results in a CMRR₁ of 94 dB. The CMRR will be even better in another chip process with a larger Early voltage and a better balancing factor (by matching or trimming).

Signal source resistors R_{S1} and R_{S2} in combination with the common-mode base currents $V_{CM}/\beta r_o$ of Q11 and Q12 give another contribution to the CM rejection:

$$\frac{1}{\text{CMRR}_2} \approx \frac{R_S}{\beta r_o} \left(\frac{\Delta R_S}{R_S} + \frac{\Delta \beta}{\beta} \right)$$
(3)

where $R_S = (R_{S1} + R_{S2})/2$, $\Delta R_S = R_{S1} - R_{S2}$, $\beta = (\beta_{11} + \beta_{12})/2$, and $\Delta \beta = \beta_{11} - \beta_{12}$. In the case of a single source resistor R_S , as shown in Fig. 1, the term $\Delta R_S/R_S$ is one. If we assume that $\Delta \beta/\beta \ll 1$ and take $R_S = 1 \text{ k}\Omega$, $r_o = 1 \text{ M}\Omega$, and $\beta = 100$, we find CMRR₂ = 100 dB. The total

common-mode rejection is approximated by

$$\frac{1}{\mathrm{CMRR}} = \frac{1}{\mathrm{CMRR}_1} + \frac{1}{\mathrm{CMRR}_2}.$$
 (4)

For contributions $CMRR_1 = 94 \text{ dB}$ and $CMRR_2 = 100 \text{ dB}$ the resulting CMRR is 90 dB.

For high frequencies the common-mode rejection can be derived in a similar way, taking the parasitic capacitances across r_{I13} , and r_{I14} and the collector-base capacitors of Q11 and Q12 into account.

C. Accuracy

To obtain a good accuracy of the closed-loop amplification, two conditions have to be met. The first condition is that the two transconductance stages must have equal transfers. Their transfer functions can be approximated as

$$Gm_{1} \approx \frac{1 - 1/\beta_{1}}{R1 + r_{e11} + r_{e12}}$$
$$Gm_{2} \approx \frac{1 - 1/\beta_{2}}{R2 + r_{e21} + r_{e22}}$$
(5)

where β_1 is the average current gain of Q11 and Q12 and β_2 is the average current gain of Q21 and Q22. As can be seen from these equations, Gm_1 and Gm_2 depend on the value of r_e , which is a function of bias current and temperature. In the present design the ratio Gm_1/Gm_2 must be exactly one, hence all resistor values, current gains, bias currents, and component temperatures must have well-matched values. To obtain good matching, the resistors as well as the transistors of the two input stages have been placed close together on the chip in a symmetrical layout. The accuracy of the amplifier will be limited by the matching achieved between the two transconductance stages.

The second requirement for good accuracy is that the gain of the loop amplifier A (see Fig. 5) is large. For an accuracy of 0.1% at a closed-loop gain of 1000, the open-loop gain must be at least 10^6 . To simplify frequency compensation the uncompensated loop should have not more than two dominant poles. Therefore the number of amplifier stages should be as small as possible. In Fig. 7 the schematic of the loop amplifier is shown. The loop amplifier consists of input cascode stage Q31, Q32, Darlington output stage Q51, Q52, and a highgain intermediate stage Q41–Q47. In this topology the voltage gain and the pole positions are mainly determined by the intermediate gain stage. Therefore we pay special attention to this interesting subcircuit of the amplifier design [7], [8].

The function of the gain stage is to obtain the highest possible gain from input to output. The gain stage consists of a Darlington differential pair Q41-Q44 loaded by folded current mirror Q45, Q46 with bootstrap transistor Q47. The all n-p-n setup is used to obtain good high-frequency behavior. To explain the gain improvement, we will first compare it to a gain stage without bootstrap transistor Q47. In that case, the emitters of transistors Q45 and Q46 in Fig. 7 should be grounded. The differential stage Q41-Q44 in combination with current mirror Q45 and Q46 has a transconductance g_m . At node X the current is converted into a voltage. The



Fig. 7. Instrumentation amplifier with intermediate gain stage Q41-Q47.

magnitude of this voltage is determined by the total resistance between node X and ground. When Q47 is left out and Q45 and Q46 are grounded, this resistance consists of the output resistances r_{o44} and r_{o46} of Q44 and Q46, the output resistance r_{2I} of the current source 2I, and the load resistance $\beta^2 R_L$ formed by the output stage. Then we find for the voltage gain

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_m \cdot (r_{o44} || r_{o46} || r_{2I} || \beta^2 R_L).$$
(6)

If r_{2I} and R_L are large enough, the gain is mainly limited by the Early effect of Q44 and Q46. The resulting value of the gain is related to the intrinsic transistor gain:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_m \cdot \frac{1}{2} r_o \approx \frac{1}{2} \mu \approx 500.$$
⁽⁷⁾

In case of a bootstrapped gain stage with Q47, exactly as shown in Fig. 7, transistor Q47 senses the voltage at the collector of Q44 and feeds it back to the collector of Q43. Hence, the voltages at the collector nodes become nearly equal in magnitude and phase. As a result the leakage current through r_{o44} is balanced out by the leakage current through r_{o43} . The leakage through r_{o46} is also eliminated because Q47 holds Q46 at a nearly constant base–collector voltage. The result is that the voltage gain of the intermediate stage increases to

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_m \cdot (\beta^2 R_L). \tag{8}$$

The load R_L is determined by the feedback resistors R3 + R4and the actual load resistor at the output. Supposing R_L is approximately equal to $1/g_m$ and $\beta = 100$, the gain would be about 10 000. Other improvements of the gain stage are the better CMRR and PSRR caused by the improved symmetry and the dc base current compensation $(i_{b45} + i_{b46} = i_{b47} + i_{b51})$.

If the intermediate stage was not loaded by the impedance of the output stage $\beta^2 \cdot R_L$, then the gain would be limited by two other effects which were not mentioned before. The first effect is due to imperfection of the voltage feedback action of Q47. The current that flows from node X to ground is not exactly compensated by the current that flows from node Y to ground. In a CMOS version of the gain stage this is the



Fig. 8. Bootstrapped gain stage with dc current flow.

most important gain-limiting factor [8]. In the present bipolar version the dc gain is mainly limited by a second effect, finite values of the current gains β of transistors Q45-Q47. The dc gain can be derived using Fig. 8. The total impedance from node X to ground is called r_X and the total impedance from node Y to ground is called r_Y . We assume that the voltages at nodes X and Y are both equal to V_{OUT} and that $r_X \approx r_Y = r$. The voltage signal at nodes X and Y causes common-mode current V_{OUT}/r through r_X and r_Y . These currents enter the circuit again through Q47 and the current mirror Q45/Q46. The resulting base currents of Q45-Q47 flow as a differential current through Q43 and Q44. This differential current corresponds to an equivalent differential input voltage:

$$V_{\rm IN} = \frac{4}{g_m \cdot \beta \cdot r} \cdot V_{\rm OUT}.$$
 (9)

For $\beta = 100$ and $g_m \cdot r \approx \mu \approx 1000$ the maximum gain of the unloaded intermediate stage would be 25 000.

The output stage Q51, Q52. a Darlington emitter follower with open emitter and resistive load (R3 + R4), allows output voltages down to the ground rail. The output stage serves as a voltage buffer that can deliver large output currents to the load and feedback resistors. For the complete amplifier an openloop gain of $3 \cdot 10^6$ was achieved, which satisfies the condition for an accuracy better than 0.1% even for closed-loop gains in the order of 1000.

D. Noise and Offset

The noise of a well-designed amplifier is determined mainly by the input stage. In the present indirect feedback configuration two "input" stages T1 and T2 are connected in parallel (Fig. 6) and therefore the equivalent input noise (in square volts per hertz) is doubled. This, however, is not a specific disadvantage of the indirect current feedback configuration. The three-op-amp instrumentation amplifier, shown in Fig. 2, also has double input noise because of the two op amps at the input. The formula for the total input noise for the instrumentation amplifier of Fig. 7 is given by

$$Un_{eq}^{2} \approx 4kT \left[\frac{1}{2} (r_{e11} + r_{e12} + r_{e21} + r_{e22}) + (R1 + R2) + \left(\frac{1}{2}R1\right)^{2} + \left(\frac{1}{R13} + \frac{1}{R14} + \frac{1}{R31} + \frac{1}{R32} + \frac{1}{R35} + \frac{1}{R36}\right) + \left(\frac{1}{2}R2\right)^{2} \left(\frac{1}{R23} + \frac{1}{R24}\right) \right].$$
(10)

The first term represents the collector shot noise of the four input transistors. The second term is the thermal noise of the emitter resistors. The third and fourth terms are the noise contributions of the current sources in conjunction with R1 and R2. To reduce these contributions it is recommended to take current sources Q13 and Q14 together into one current source connected to the middle of R1. This turns the noise current of R13 and R14 into a common-mode current, eliminating the contribution to the input noise. The same applies to the noise of the current sources with R23 and R24. The reason why split current sources are used in this design is just a practical one. To split up R1, two well-matched 5-k Ω resistors are needed, placed close to the p-n-p input transistors. These resistors were not available on the semi-custom chip on which the circuit has been fabricated.

For the offset, the contributions of input stages T1 and T2 are added and the input stage of the op amp (Q31 and Q32) gives an extra contribution. The offset from layout and doping mismatches of the three transistor pairs Q11/Q12, Q21/Q22, and Q31/Q32 has an estimated value of 0.25 mV for each pair. The contribution to the offset from mismatches between the current sources with R13/R14, R23/R24, and R35/R36 has an estimated value of 0.1 mV for each pair of current sources. The estimation for the total worst-case offset of the amplifier is thus about 1 mV.

E. High-Frequency Behavior

For an analysis of the high-frequency behavior, we take a look at the amplifier loop. Fig. 9 shows a simplified schematic of the amplifier. The loop consists of feedback stage T2, a buffer stage, a gain stage, an output stage, and the resistor network R3, R4. Input stage T1 is outside the loop. V-to-I converter T2 causes no dominant poles because it is driven by the low output impedance of the output stage (assuming R3||R4 is low as well) and because it is loaded by the low



input impedance of the buffer stage. The two dominant poles, located at the input and the output of the intermediate gain stage, allow simple frequency compensation using a single Miller capacitor. In the schematic of Fig. 7, C_{M1} is placed over the gain stage from the inverting input to the output, and C_{M2} is inserted at the other input of the gain stage to balance the effect of C_{M1} . As a result poles p_1 and p_2 are split apart and one is made dominant. The unity-gain frequency of the compensated amplifier is determined by the transconductance of input stages and the Miller capacitors, according to

 $2\pi f_t = G_m \left(\frac{1}{C_{M1}} + \frac{1}{C_{M2}}\right) = \frac{2Gm}{C_M}$

with

$$Gm = Gm_1 = Gm_2, \quad C_M = C_{M1} = C_{M2}.$$
 (11)

In a voltage-follower configuration, with unity-gain feedback (R3 = 0), a third pole in the loop will cause a pair of complex poles in the overall gain, which causes peaking in the frequency response and some overshoot in the step response. The compensation is optimized for gains larger than 1.

F. Biasing

The biasing circuit of the instrumentation amplifier is shown in Fig. 10. The transistors Q62-Q69 form a constant current source, which creates a reference current of 10 μ A for biasing the current sources in the amplifier circuit of Fig. 7. The reason why a constant current source is used rather than the usual PTAT current source can be understood by looking at the collector voltages of Q11 and Q12 in Fig. 7. The voltage at these nodes is biased at $3 \cdot I \cdot R31 = 0.3$ V at room temperature. If current I was proportional to the absolute temperature, then the common-mode input range would decrease too much for increasing temperature (see subsection A).

IV. MEASUREMENT RESULTS

The instrumentation amplifier has been implemented in a semi-custom bipolar process with vertical n-p-n and lateral p-n-p transistors. Five chips from one wafer have been tested. The average values of the measured characteristics of the amplifier are listed in Table I. Fig. 11 shows a chip photograph of the integrated instrumentation amplifier.

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Fig. 10. Bias circuit of the amplifier.

 TABLE I

 MEASUREMENT RESULTS OF THE INSTRUMENTATION AMPLIFIER

Parameter	Value	Unit
Common-mode input range	-0.2 to 4	v
CMRR	92	dB
Gain range	1 to 1000	
Gain error	< 0.1	%
Nonlinearity, V _{in} =100 mV	< 0.1	%
Input offset voltage	0.3	mV
Input bias current	240	nA
Input offset current	2	nA
Input noise voltage	30	nV/√Hz
DM input impedance CM input impedance	620 30	kΩ MΩ
GB product, G= 1 to 1000	1.2	MHz
Slew rate	1.2	V/µs
Supply voltage range	2.5 to 15	v
Supply current	240	μA





Fig. 11. Photo of the semi-custom chip.

In Fig. 12 the CMRR of the amplifier as a function of frequency is plotted. The low-frequency value is 92 dB, close





Fig. 13. Closed-loop frequency response for gains of 1, 10, 100, and 1000.



Fig. 14. Pulse response at unity gain.

to the estimated value of Section III-B. For frequencies above 400 Hz the parasitic capacitances in the input stage reduce the CMRR. The common-mode rejection is independent of the closed-loop gain, set by feedback resistors R3 and R4.

In Fig. 13 the closed-loop gain as a function of frequency is given for four values of the gain. For unity gain there is 4-dB peak at 1.2 MHz, showing that the amplifier is slightly undercompensated. For higher gains the bandwidth decreases, according to a constant gain-bandwidth product of about 1.2 MHz.

Finally, Fig. 14 shows the step response of the unity-gain configuration to a 100-mV step at the input. The overshoot corresponds to the unity-gain frequency response, plotted in Fig. 13. Because of the asymmetric design of the output stage, Q51 and Q52 in Fig. 7, the rising edge of the response is faster than the falling edge.

V. CONCLUSIONS

An instrumentation amplifier has been designed with a common-mode input range that extends 0.2 V below the negative supply. The extended range is combined with a good CMRR of 92 dB and an accuracy better than 0.1%, which was achieved without using trimmed components. The instrumentation amplifier has been fabricated in a simple semicustom bipolar process, using standard lateral p-n-p transistors. The good performance of the amplifier is achieved by the special design using simple p-n-p transconductance input stages in an indirect current-feedback configuration with a high loop gain.

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Bernard J. van den Dool was born in De Lier, The Netherlands, on December 13, 1963. In 1992 he received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands. His thesis was on the subject of low-voltage instrumentation amplifier design. The research was performed at the Electronic Instrumentation Laboratory of the university.



Johan H. Huijsing (SM'81) was born in Bandung, Indonesia, on May 21, 1938. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1969, and the Ph.D. degree from the same university in 1981 for work on operational amplifiers.

Since 1969 he has been a member of the research and teaching staff of the Electronic Instrumentation Laboratory at the Department of Electrical Engineering of the Delft University of Technology, where he is now a Professor in electronic instrumen-

tation. He teaches courses on electrical measurement techniques, electronic instrumentation, operational amplifiers, and analog-to-digital convertors. His field of research is analog circuit design (operational amplifiers, analog multiplexers, etc.). He is the author or co-author of some 70 scientific papers and he holds 12 patents.