

Residue-free plasma etching of polyimide coatings for small pitch vias with improved step coverage

Benjamin Mimoun^{a)}

Electronic Components, Technology and Materials (ECTM) – DIMES, Delft University of Technology, Feldmannweg 17, 2628 CT Delft, The Netherlands

Hoa T. M. Pham and Vincent Henneken

Micro Systems and Devices, Philips Research, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands

Ronald Dekker

Electronic Components, Technology and Materials (ECTM) – DIMES, Delft University of Technology, Feldmannweg 17, 2628 CT Delft, The Netherlands and Micro Systems and Devices, Philips Research, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands

(Received 10 August 2012; accepted 28 December 2012; published 23 January 2013)

The authors have found that patterning polyimide coatings containing organosilane adhesion promoter using pure oxygen plasma resulted in a thin silicon-rich residue layer. They show in this paper that adding small amounts of fluorine-containing gas to the etching gas mixture is necessary in order to achieve residue-free polyimide plasma etching. They report residue-free plasma etching of polyimide coatings with both isotropic and anisotropic profiles, using either metal or oxide hard masks. These etching methods are however not sufficient for the fabrication of high density metal filled vias in 10 μm thick polyimide coatings. In order to improve the metal step coverage over the vias while keeping the pitch as small as possible, the authors have developed a two-step etching recipe combining both isotropic and anisotropic profiles, resulting in wine-glass shaped vias. © 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4788795>]

I. INTRODUCTION

Polyimide (PI) is a widely used material in microfabrication because of its outstanding properties such as excellent chemical and thermal stability, superior dielectric properties, and high mechanical strength.^{1,2} PI coatings are usually applied from poly(amic) acid solutions onto substrates by spin-coating, and cured at elevated temperatures (up to 400 °C) in inert ambient. A thin layer of adhesion promoter (organosilane) is usually spin coated before PI deposition.^{3–5} Virtually all standard polyimides used in electronics are also commercialized in the form of self-priming precursors, containing small amounts of organosilane. Photosensitive polyimides are also commercially available. They are patterned using specific developers after a standard exposure step. The smallest achievable feature with photosensitive polyimide is however usually much larger than what can be achieved with non-photosensitive polyimide.^{6,7} In this paper, we will focus on non-photosensitive polyimides only.

Depending on the application, different types of PI patterning are required. When PI is used as sacrificial layer, isotropic etching is used in order to release the top functional layer.⁸ PI is also very often used as dielectric layer, or as substrate material for flexible applications. In this case, different types of etching are required for the fabrication of electrical vias running through the PI layer. Anisotropic etching is needed in order to obtain vertical vias for subsequent electro(less) plating of metal.^{9,10} This technique allows high density, fine pitch vias fabrication, provided that a good anisotropy can be achieved for the PI layer etching.

However, the interconnection metal layer is usually either sputtered or evaporated on top of the underlying PI layer, requiring sloped via walls in order to ensure good step coverage and electrical conduction. This can easily be done by wet etching of the PI layer in a tetramethylammonium hydroxide-based solution using a resist mask before the curing stage,¹¹ or using dry-etching techniques with parameters resulting in tapered via walls after the curing stage.^{12,13} The tapered via profile however increases the minimum achievable via pitch, especially when the thickness of the PI layer increases.

Several studies have been published on the characterization of polyimide dry etching using different plasma chemistries, etching methods, and parameters.^{14–17} Atomic oxygen is the main etchant of polyimide by abstraction and/or addition of oxygen atoms to unsaturated groups.¹ It is important to note that atomic oxygen is not capable of attacking undamaged structures. Ion bombardments and/or natural defects are necessary in order to open the benzene rings and allow etching. Addition of atomic fluorine in the plasma chemistry has been proven to enhance the production of atomic oxygen,¹⁴ thereby increasing the etching efficiency. In addition, atomic fluorine also reacts in two different ways with the PI surface to increase the etch rate.¹⁶ Addition of fluorine to unsaturated benzene rings produces an intermediate saturated polymer with a lower activation energy. Atomic fluorine also generates HF molecules by combining with hydrogen atoms from the polyimide surface, leaving free surface radical sites for subsequent oxidation by atomic oxygen. Nitrogen (N_2) has also been reported to increase the production of atomic oxygen when added to the plasma chemistry.¹

^{a)}Electronic mail: b.a.z.mimoun@tudelft.nl

In this paper, we present the fabrication of residue-free fine pitch vias for subsequent metal deposition, based on a two-step combination of both isotropic and anisotropic dry etching of the polyimide layer. We first present the process flowchart and the etching parameters used in this study. We then discuss the origin of the residue layer, and demonstrate methods to achieve residue-free plasma etching of self-priming polyimide layers. We finally present a two-step etching approach for the production of fine pitch vias in 10 μm thick polyimide layers.

II. EXPERIMENT

The processing of the wafers was carried out on both standard 6 and 4 in. silicon wafers. A schematic view of the process flow used is shown in Fig. 1.

A 500 nm thermal silicon oxide (SiO_2) etch-stop layer was first grown at 1100°C. Although the polyimide used was advertised as self-priming, we found that spin-coating an organosilane-type adhesion promoter (VM-652 from HD Microsystems) prior to spin-coating of the polyimide layer significantly improved the adhesion. After application of the primer, polyimide (115A from Fujifilm) was spin-coated (15 s at 350 rpm and 45 s at 1000 rpm) and softbaked at

120°C for 6 min in order to remove most of the solvents. The thickness of the softbaked polyimide layer was of about 15 μm . The wafers were then cured at 400°C for 2 h in a 200 mbar nitrogen environment. The curing step produced fully imidized 10 μm thick polyimide layers. Next, the masking layer was deposited. Oxides and metals are most often used as masking layer for dry etching of polyimide. The selection of the masking material for the etching is usually based on two parameters: selectivity toward the etched material, and integration of the masking material in the process flowchart. In order to demonstrate the feasibility of the presented etching methods, both metal and oxide etch masks were used. A 500 nm thick plasma enhanced chemical vapor deposition (PECVD) SiO_2 layer was deposited at 300°C on some of the wafers and a 250 nm thick aluminum/1% silicon ($\text{Al}/1\%\text{Si}$) layer was sputtered at 25°C on the other wafers. The hard mask was subsequently covered with resist and patterned using conventional lithography and dry etching. After opening of the SiO_2 and $\text{Al}/1\%\text{Si}$ layers, the polyimide coatings were ready to be etched using the different recipes. The resist covering the hard mask was also removed during the polyimide etching step. Residue-free isotropic and anisotropic polyimide etching recipes were first developed and characterized. A two-step combination of those recipes was then optimized to produce fine pitch vias. In order to investigate the step coverage of a metal routing layer in the polyimide vias, a 1.5 μm thick $\text{Al}/1\%\text{Si}$ layer was subsequently sputtered and patterned using conventional lithography.

The etch profiles and step coverage were characterized using a scanning electron microscope (SEM) and the etch rates measured with a profilometer. For the plasma etching experiments, a barrel-type etcher (TEPLA IPC 9200) and an inductively coupled plasma-reactive ion etching (ICP-RIE) machine (Trikon Omega 201) were used.

III. RESULTS AND DISCUSSION

Isotropic dry etching of polyimide coatings is only possible with chemical etching. In a barrel-type etching machine, the plasma etching is done by ionizing a gas mixture inside a chamber to obtain ions that will react with the material to be etched. The ionization of the gases is done by RF excitation emitted by an electrode at the top of the chamber. The wafer to be etched is placed on an electrode connected to ground. Through random motion, the ions inside the chamber reach the target resulting in a purely chemical etching process. As explained previously however, ion bombardment is necessary in order to initiate the etching process. In a barrel etcher, ion bombardment occurs through the random motion of the ions in the plasma, thereby increasing the isotropy of the etching process. Figure 2 shows a 500 nm thick PECVD SiO_2 layer released by etching of a 10 μm thick PI layer in pure oxygen plasma in a barrel etcher. The etch holes in the SiO_2 layer are 5 μm wide with a pitch of 10 μm .

Etching of polyimide coatings in pure O_2 resulted in a thin residue layer of about 400 nm in thickness. Figure 3 shows an SEM top view of a sample etched in pure O_2 , using a 250 nm thick $\text{Al}/1\%\text{Si}$ masking layer in a barrel etcher.

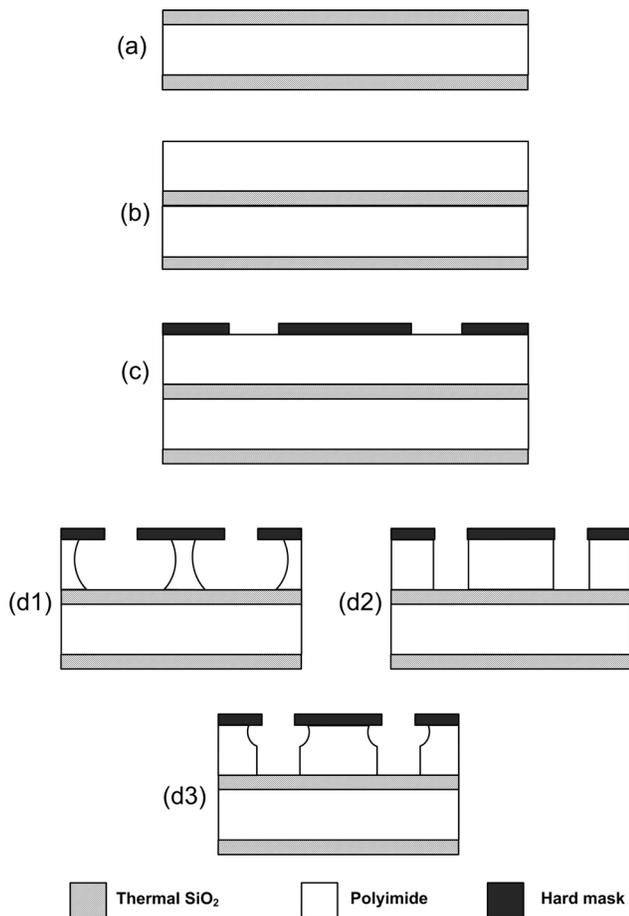


Fig. 1. Schematic representation of the polyimide etching experiments flowchart. After thermal oxidation (a), polyimide coating and curing (b), hard mask deposition and patterning (c). The polyimide etching recipe is then applied with an isotropic (d1), anisotropic (d2), or a “wine glass” (d3) profile.

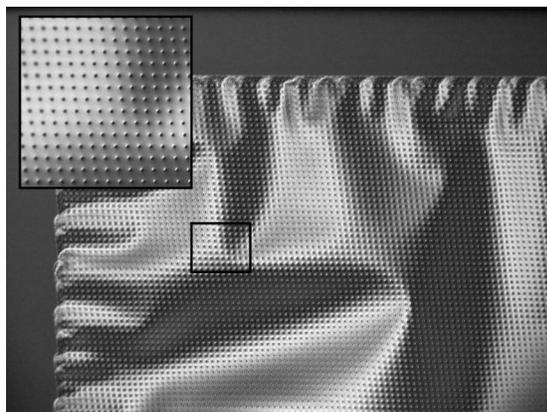


FIG. 2. Released PECVD SiO₂ membrane with a 10 μm thick polyimide coating used as sacrificial layer. The stress in the SiO₂ layer induces buckling of the membrane.

Prolongation of the etching process does not remove the residue layer. Figure 4 shows an SEM cross-section of the sample after etching at 130 °C and 1000 W for 1 h [Fig. 4(a)] and 1 h 30 min [Fig. 4(b)]. The thickness of the residue layer remains practically constant even after a longer etching time, demonstrating that the residue layer is not etched in the O₂ plasma. The polyimide etch rate was ca. 200 nm min⁻¹ and strongly depends on the temperature and the power.

Formation of “grass” during etching of polyimide in pure O₂ plasma has been previously explained by the inability of the ion bombardment to generate enough reactive sites to successfully destroy all polyimide chains, producing nonvolatile components and causing local masking.¹⁶ Micromasking due to the deposition of aluminum atoms sputtered-off from the hard mask has also been reported as a possible cause for formation of “grass” during polyimide etching in pure O₂ plasma.¹² We however observed a “residue-layer,” rather than “grass” due to local micromasking. We claim that this residue layer is mainly composed of the silicon-containing active ingredient (a-aminopropyltriethoxysilane) contained in the VM652 adhesion promoter, which improves the adhesion of the spin-coated polyimide to the thermal oxide layer by forming Si–O bonds. This assumption is further

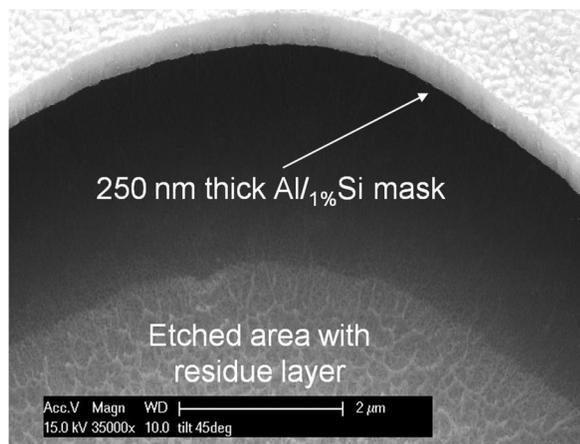
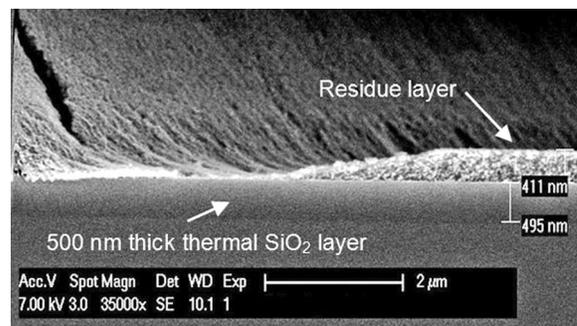
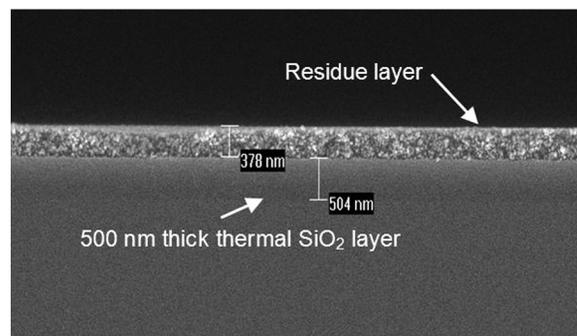


FIG. 3. SEM top view of the residue layer after isotropic plasma etching of polyimide in pure O₂ using a 250 nm thick Al_{1%}Si mask.



(a)



(b)

FIG. 4. SEM cross-section of the etched polyimide coating with residue layer after 1 h of etching (a) and after 1 h 30 min of etching (b).

supported by energy dispersive x-ray analysis (EDX) of the etched surface shown in Fig. 5. The atomic ratio silicon/oxygen clearly indicates that the residue layer contains silicon-rich compounds. By comparison, the underlying layer of thermal SiO₂ has an atomic silicon/oxygen ratio of 1/2.

In order to remove the silicon-rich residue layer, a fluorine-containing gas was added to the etching gas mixture, as fluorine is a known silicon etchant.¹⁸ It appeared that

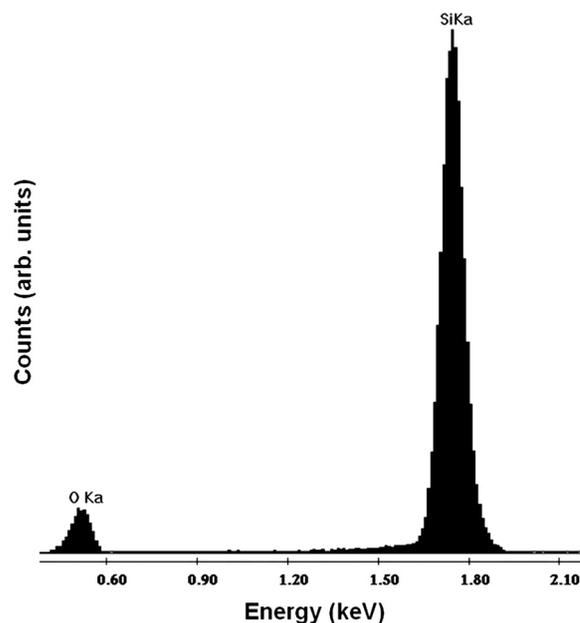


FIG. 5. *In situ* EDX measurement of the residue layer on top of a thermal SiO₂ etch-stop layer.

even a very small amount of carbon tetrafluoride (CF_4) was sufficient to achieve residue-free etching of the polyimide. Figure 6 shows an SEM picture of the isotropic profile of a polyimide layer etched in a barrel etcher with a gas composition of 95% O_2 and 5% CF_4 , using a 250 nm thick $\text{Al}/1\% \text{Si}$ mask and a power of 1000 W. The etch rate of the polyimide was ca. 400 nm min^{-1} . The underlying thermal SiO_2 layer was however also etched during the process. It is indeed known that O_2/CF_4 plasmas etch SiO_2 .¹⁸ Since the fluorine, which is the active etchant of the SiO_2 layer, is only present in a very small amount in the gas mixture, the etch rate of the thermal SiO_2 is much lower than the etch rate of polyimide (ca. 30 nm min^{-1}). Isotropic residue-free etching of polyimide could be achieved by using either an aluminum or SiO_2 hard etch mask.

An ICP-RIE etcher was used in order to obtain an anisotropic etching profile by mostly using physical etching. In an ICP-RIE etcher the etching principle is almost the same as in a barrel etcher, but in this case the chamber's top electrode is connected to ground and the wafer placed on the excitation electrode. Since the wafer is now connected to the RF signal instead of ground, electrons are statistically more often in contact with the target than the positive ions (which are heavier). Electrons are highly reactive species and are easily adsorbed by the target material, polarizing it negatively. Simultaneously, the loss of electrons in the plasma results in a globally positively charged ion "cloud," thereby producing an acceleration of the ions toward the wafer. The velocity of the ions results in an etching mechanism called physical etching. The molecules of the layer to be etched are sputtered-off as a result of the impact of the ions on the wafer. The plasma is generated by a magnetic field, and densified by a second magnetic field generator. The objective is to achieve a high ionization rate in the plasma in order to enhance the RIE effect. As a result, the chemical etching process occurs in combination with the physical process. The anisotropy of the etching was maximized by reducing the pressure to 20 mTorr and increasing the power to 500 W. Again, a small amount of CF_4 was added to the O_2 gas mixture in order to remove the residue layer and to increase the

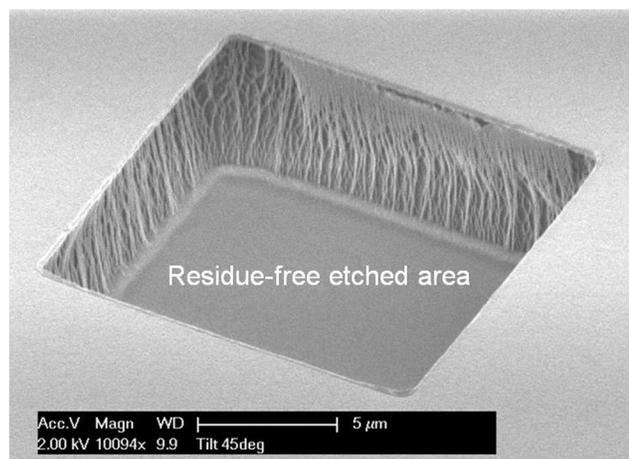


Fig. 6. SEM picture of a $5 \mu\text{m}$ thick isotropic residue-free etched surface using a barrel etcher.

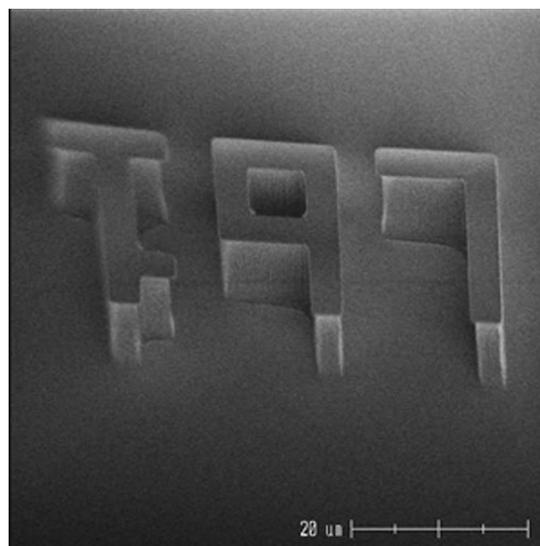


Fig. 7. SEM picture of a $10 \mu\text{m}$ thick polyimide coating etched anisotropically with a residue-free landing area.

etch rate. N_2 was also added to the etching gas mixture in order to increase the production of atomic oxygen. The exact gas composition used for this recipe was 80% O_2 , 13% N_2 , and 7% CF_4 . The thermal SiO_2 layer underneath the polyimide was slightly etched to a depth of several nm. Both metal and SiO_2 masks were successfully tested. Figure 7 shows an SEM picture of a residue-free anisotropically etched polyimide layer using a 250 nm $\text{Al}/1\% \text{Si}$ mask. The etch rate of polyimide in the ICP-RIE tool was approximately $1 \mu\text{m min}^{-1}$, while the etch rate of thermal SiO_2 was 55 nm min^{-1} . It is therefore possible to create high density anisotropic vias in a $10 \mu\text{m}$ thick polyimide layer using this anisotropic etching recipe. However, the vertical edge profile led to insufficient step coverage of the resist masking layer for subsequent aluminum interconnection patterning (Fig. 8).

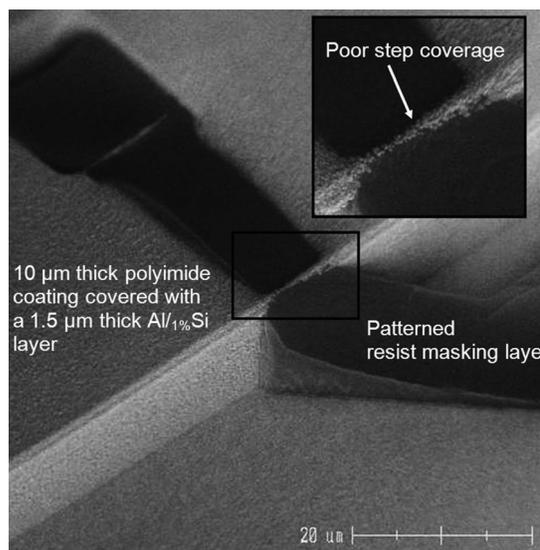


Fig. 8. Poor resist step coverage on top of a $10 \mu\text{m}$ thick polyimide coating with a $1.5 \mu\text{m}$ thick $\text{Al}/1\% \text{Si}$ layer sputtered on top, for subsequent interconnection patterning.

It appears that the fabrication of high density vias in $10\ \mu\text{m}$ thick polyimide layers using either purely isotropic or anisotropic etching recipes is not possible due to high undercut or bad step coverage, respectively. We propose here to use a combination of both the isotropic and anisotropic plasma etching recipes reported previously to create small pitch vias with good step coverage in $10\ \mu\text{m}$ thick polyimide coatings. The main idea behind this etching method is to follow the shape of a wine glass by gradually increasing the vias walls slope from a low angle (isotropic etching) to a nearly vertical shape (anisotropic etching), in order to improve the step coverage while retaining a high vias density. Polyimide coatings were first etched in a barrel-etcher to a depth of $4\ \mu\text{m}$, using the isotropic recipe. The remaining $6\ \mu\text{m}$ of polyimide was then etched in an ICP-RIE etching tool using the anisotropic recipe. A $250\ \text{nm}$ thin $\text{Al}/1\%\text{Si}$ mask was used as the mask erosion of $\text{Al}/1\%\text{Si}$ is less than that of PECVD oxide. Figure 9 shows $5\ \mu\text{m}$ wide openings in the polyimide layer after removal of the hard mask in PES. The edge wall angle gradually increases from top to bottom, to end up with nearly vertical via walls, resembling the shape of a wine glass. It is therefore possible to reduce the pitch of the vias fabricated in the $10\ \mu\text{m}$ thick polyimide layer to $10\ \mu\text{m}$. In addition, the etching method greatly improves the resist step coverage. Figures 10(a) and 10(b) show a $3\ \mu\text{m}$ thick patterned negative resist layer, ready to be used as masking layer for patterning the $1.5\ \mu\text{m}$ thick $\text{Al}/1\%\text{Si}$ layer sputtered on top of the etched PI coating. The resist layer perfectly covers the wall edges.

An alternative method to improve the step coverage is to tune the deposition parameters of the layers on top of the etched polyimide coating. Techniques such as spray-coating, electrodeposition and bias sputtering have been reported to significantly improve the step coverage of resist¹⁹ and aluminum²⁰ layers, respectively. These techniques however usually require extraprocessing steps and/or nonstandard tools. The two-step polyimide etching method presented here offers the advantage of improving the step coverage of sub-

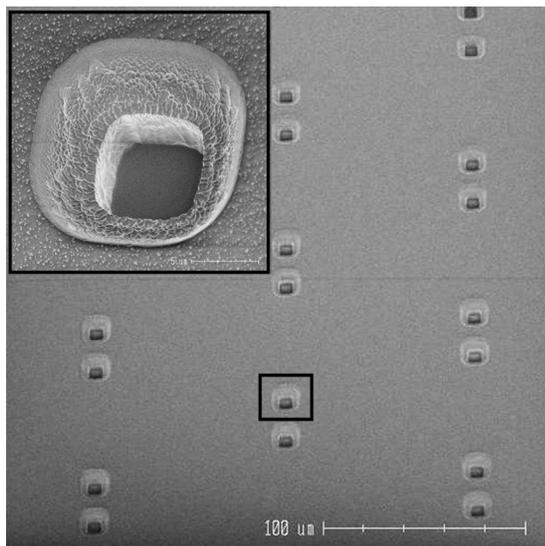
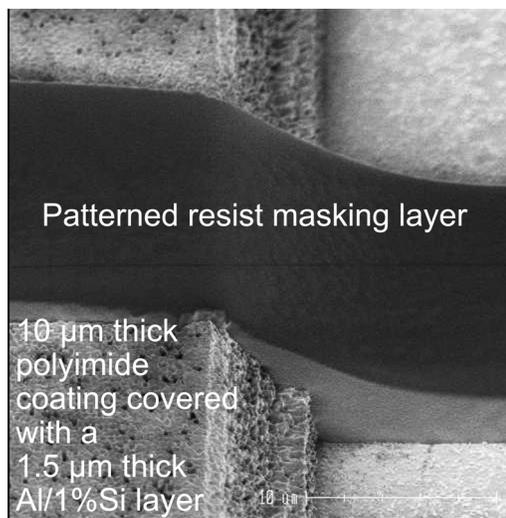
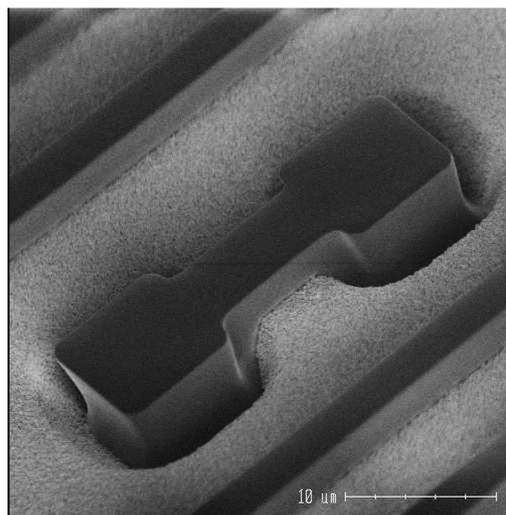


Fig. 9. SEM picture of wine-glass shaped vias etched in a $10\ \mu\text{m}$ thick polyimide coating with a pitch of $10\ \mu\text{m}$. The edge wall angle gradually increases to end up in a purely anisotropic profile.



(a)



(b)

Fig. 10. (a) and (b) SEM pictures of a $3\ \mu\text{m}$ thick patterned negative resist layer, ready to be used as masking layer for patterning the $1.5\ \mu\text{m}$ thick $\text{Al}/1\%\text{Si}$ layer sputtered on top of the etched polyimide coating. The step coverage of the resist is improved compared to a purely anisotropic etched polyimide coating.

sequent layers with standard processing parameters and equipments. It is moreover independent of the type of layer deposited on top of the polyimide coating.

IV. SUMMARY AND CONCLUSIONS

We have shown that patterning of self-priming polyimides in pure O_2 plasmas after curing resulted in a thin silicon-containing residue layer. This layer was proven to be resistant against further O_2 plasma etching. However, the addition of a small amount of fluorine-containing gas to the etching mixture resulted in the complete removal of the residue layer. Both purely isotropic and purely anisotropic residue-free plasma etching of polyimide coatings have been demonstrated. These etching methods are useful when polyimide is used as sacrificial layer (isotropic etching) or as a masking layer for subsequent plating of metal interconnects

(anisotropic etching). These recipes are however not suitable for the fabrication of high density vias in relatively thick layers of polyimide due to the high undercut of the isotropic etch and the bad step coverage of the anisotropic etch. We used a combination of both isotropic and anisotropic etching to gradually increase the vias walls slope from a low angle to a nearly vertical angle, following the shape of a wine glass. This resulted in good step coverage of any subsequent layer while retaining high via density. The presented etching method is expected to facilitate the development of polyimide-based applications where high density vias in polyimide coatings are needed.

ACKNOWLEDGMENTS

The authors would like to thank Mario Laros from the DIMES support staff for his help with the polyimide dry-etching experiments. This work has been partly supported by the Dutch Technology Foundation (STW), under Project SmartSip 10046.

¹M. K. Gosh and K. L. Mittal, *Polyimides: Fundamentals and Applications* (Marcel Dekker, New York, 1996).

²L. B. Rothman, *J. Electrochem. Soc.* **127**, 2216 (1980).

³A. V. Patsis and S. Cheng, *J. Adhes.* **25**, 145 (1988).

⁴R. R. Tummala and E. J. Rymaszewski, *Microelectronics Packaging Handbook* (Van Nostrand Reinhold, New York, 1989).

⁵L. P. Buchwalter, *J. Adhes. Sci. Technol.* **4**, 697 (1990).

⁶A. Endo, M. Takada, K. Adachi, H. Takasago, T. Yada, and Y. Onishi, *J. Electrochem. Soc.* **134**, 2522 (1987).

⁷T. Fukushima, T. Oyama, T. Iijima, M. Tomoi, and H. Itatani, *J. Polym. Sci., Part A: Polym. Chem.* **39**, 3451 (2001).

⁸A. Bagolini, L. Pakula, T. L. M. Scholtes, H. T. M. Pham, P. J. French, and P. M. Sarro, *J. Micromech. Microeng.* **12**, 385 (2002).

⁹A. O. Aggarwal, P. M. Raj, and R. R. Tummala, *IEEE Trans. Adv. Packag.* **30**, 384 (2007).

¹⁰S. Sugitani, K. Onodera, S. Aoyama, M. Hirano, and M. Tokumitsu, *J. Vac. Sci. Technol. B* **20**, 1019 (2002).

¹¹G. Rabilloud, *High-Performance Polymers* (Technip, Paris, 2000), Vol. 3.

¹²S. J. Till, A. G. Brown, and V. G. I. Deshmukh, *Microelectron. Eng.* **3**, 491 (1985).

¹³M. Deschler and P. Balk, *Microelectron. Eng.* **4**, 207 (1986).

¹⁴G. Turban and M. Rapeaux, *J. Electrochem. Soc.* **130**, 2231 (1983).

¹⁵W. E. Vanderlinde and A. L. Ruoff, *J. Vac. Sci. Technol. B* **6**, 1621 (1988).

¹⁶U. Buder, J.-P. von Klitzing, and E. Obermeier, *Sens. Actuators, A* **132**, 393 (2006).

¹⁷V. Bliznetsov, A. Manickam, J. Chen, and N. Ranganathan, *J. Micromech. Microeng.* **21**, 067003 (2011).

¹⁸C. J. Mogab, A. C. Adams, and D. L. Flamm, *J. Appl. Phys.* **49**, 3796 (1978).

¹⁹J. O'Brien, P. J. Hughes, M. Brunet, B. O'Neill, J. Alderman, B. Lane, A. O'Riordan, and C. O'Driscoll, *J. Micromech. Microeng.* **11**, 353 (2001).

²⁰D. W. Skelly and L. A. Gruenke, *J. Vac. Sci. Technol. A* **4**, 457 (1986).