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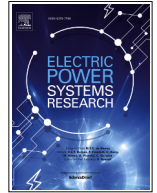
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Risk assessment of voltage violations during unintentional islanding events

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ABSTRACT

The increasing penetration of distributed generators (DGs) has led to the proposal of fault ride-through (RT) requirements. These requirements enhance the reliability of the electrical system; however, reduce the sensitivity of anti-islanding protections, potentially exposing sensitive equipment to severe overvoltages before DG disconnection when an unintentional islanding occurs. To assess the extent of these events, also reported as load rejection overvoltage, this paper introduces the Voltage Violation Region (VVR) concept, i.e., an area in the $\Delta P \times \Delta Q$ plane given by the operating points in which anti-islanding protections fail to rapidly disconnect DGs before violating sensitive load tolerance limits. Based on dynamic simulations and the VVR, a risk assessment method is proposed to quantify the probability of post-islanding voltages violating the tolerance limit of voltage-sensitive loads. Our analysis of practical passive and active islanding detection methods (IDMs) reveals that RT requirements may significantly delay the activation of anti-islanding protections, resulting in high risks of voltage violations, depending on the tolerance curve and power imbalance measurements. When active IDMs are enabled, these violations may occur even in scenarios with deficit of active power imbalance within the islanded grid. The results support distribution engineers in identifying high-risk feeders, requesting end-users to apply additional protection for sensitive loads, or re-setting the DG's anti-islanding protections.

1. Introduction

1.1. Motivation and incitement

Renewable energy resources are steadily employed worldwide due to their techno-economic-socio-environmental opportunities. However, the increasing penetration of these distributed generators (DGs) brings control and protection challenges to the safe operation of the distribution systems, e.g., the possibility of forming an unintentional island. This unplanned situation happens when a portion of the distribution system containing loads and DGs disconnects from the main grid [1]. Unintentional islanding may cause negative consequences for the electrical system and utilities' personnel [2], which must be avoided by disconnecting the DGs after an islanding occurrence. In this context, the IEEE Std. 1547-2018 recommends disconnection of DGs within 2 s after the islanding event [1].

To disconnect DGs after an unintentional islanding, several islanding detection methods (IDMs) have been proposed in the literature,

classified into remote and local techniques [2]. Remote methods are reliable but complex and expensive since they are based on communication between DGs and grid switches (breakers and reclosers). Local methods are cheaper, less complex, and are grouped into passive, active, and hybrid types. Passive techniques, which measure electrical quantities at the DG point of common coupling (PCC), are commonly used in the industry. However, they may not detect islanding when power mismatches between DGs and loads are small, creating moderate/large non-detection zones (NDZs). Active techniques, widely used in inverter-based distributed generators (IBDGs), such as grid-tie solar inverters [3,4], inject a small disturbance into current or voltage control loops, causing frequency and voltage deviations beyond standard limits when the DGs are islanded. This effectively mitigates/eliminates NDZs but may degrade power quality (PQ) due to increased harmonics [5,6]. Hybrid methods trigger the active technique only after a passive method detects a suspicious islanding event, reducing NDZs without harming PQ. However, their detection time is large due to the two-stage process [7,8].

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This paper focuses on active and passive IDMs because they are widely applied to IBDGs' protection schemes. The anti-islanding protection aims to provide a fast DG disconnection to avoid negative impacts caused by an unplanned islanded operation. However, the increasing penetration of DGs raised serious concerns about their massive disconnection due to the incorrect operation of the protection schemes. Recent events involving the cascade disconnection of DGs have brought attention to the voltage and frequency ranges within which DGs should remain connected to the grid [9,10]. Thus, ride-through (RT) requirements were proposed in the IEEE Std. 1547-2018 [1] and in recent grid codes, e.g., Brazilian regulation Prodist Module 3 [11]. Consequently, anti-islanding protection schemes have to be configured with less sensitive settings to meet the voltage and frequency RT requirements, thereby delaying the time required to disconnect the DGs.

An extended islanding detection time in a scenario with RT requirements and complex distribution systems can expose the islanded grid to severe voltage transients from the moment of islanding until the DGs are disconnected. This condition may damage voltage-sensitive equipment, such as customers' loads and surge arresters. Additionally, the growing number of sensitive loads, such as electronic ballasts, adjustable speed drivers, and energy-saving lamps, highlights the importance of PQ phenomena in the electrical grid [12]. Therefore, it is crucial to assess the potential risk of damaging voltage-sensitive loads under this new condition, in which the anti-islanding protection actuation is delayed.

1.2. Literature review

In the literature, PQ issues affecting the operation of sensitive loads have motivated several works. Most studies focus on load disconnection due to voltage sags and interruptions, proposing methods to calculate the disconnection probability or to identify the voltage tolerance curve (VTC) of sensitive loads. In [12], the authors characterized the main events that can damage sensitive converter-interfaced loads by performing susceptibility tests on each component and presented a prototype PQ monitor to detect the identified events. In [13], a new optimized model is proposed to assess the financial losses of industrial processes due to voltage sags and short interruptions. In [14], a random forest regression-based method for evaluating the index of load loss rate of sensitive users is presented. In [15], a method is proposed to assess the interruption probability of an industrial process without relying on detailed data from industrial users. In [16], a method based on an energy-loss diagram is presented to address the same issues. The authors of [17] focus on identifying the characteristics of sensitive loads and their voltage tolerance profiles based on power monitoring data. Finally, [18] develops a new method for predicting equipment malfunction and reconstructing voltage tolerance curves. Therefore, there is still a lack of research on the impact of PQ issues caused by unintentional islanding events on sensitive loads.

Other works investigated the occurrence of real-world events involving violations of overvoltage limits due to unexpected and sustained islanding events, leading to PQ issues and potentially damaging sensitive loads and utility equipment [19–23], a phenomenon referred to as load rejection overvoltage (LROV). The authors of [19] analyzed three years of operating data. They identified 131 islanding events with transient overvoltages, among which 44% are at the border of the surge arresters' voltage supportability curve. In addition, all events are within the prohibited region of the Information Technology Industry Council (ITIC) tolerance curve from reference [24], indicating that these islanding events can potentially damage sensitive loads, surge arresters, and metering devices. In [20], on-site islanding tests were performed during the commissioning of an inverter-interfaced 1 MW microturbine and a 20 MW battery energy storage system, which revealed the occurrence of LROVs. In the worst-case scenarios, phase voltages exceeded 178% of the nominal value for a short period and violated the RT limits from IEEE Std. 1547-2018, even though all equipment was properly certified, indicating the necessity of a detailed analysis to verify the extent and causes

of these events. Also, [21] tested six different commercially available photovoltaic inverters to quantify the impact of LROV for various power imbalance scenarios. Some tests yielded transients overvoltages of up to 190% of the nominal value for large power imbalances, and results varied from one fabricant to another, highlighting the need to evaluate different IBDG models. The technical report [22] investigated grounding practices for IBDGs and explored the LROV phenomenon through electromagnetic transients (EMT) simulations, during which overvoltages of up to 1.6 p.u. were observed when IBDG's frequency and voltage protections were adjusted according to IEEE Std. 1547-2018 requirements. The authors of [23] assessed transient overvoltages due to ground fault and load rejection events through EMT simulations, and verified a peak voltage of 125% for 6 cycles when no fault precedes the islanding event.

Despite the contributions of previous work, most of which focus on case-specific assessments, there is still a lack of research investigating the impact of PQ issues caused by unintentional islanding. Therefore, the following gaps are identified that still need to be overcome:

- In works that employ EMT simulations, such as [22,23], the IBDG model is simplified and does not incorporate active IDMs, which significantly contribute to post-islanding disturbances by causing instabilities in the IBR control;
- Existing research has not investigated methods to help utility engineers identify critical feeders with a real risk of post-islanding voltage violations and define countermeasures to mitigate the impacts of these events;
- The literature does not provide a detailed analysis of the settings for frequency and voltage protections that should be adopted to ensure DG disconnection before the supportability of sensitive equipment is violated.

1.3. Contributions and paper organization

In this context, recognizing the contributions of previous literature, this paper contributes to this issue by investigating the main causes and extensions of those voltage variations. It then introduces the concept of Voltage Violation Region (VVR) and proposes a method for calculating the probability of damage to voltage-sensitive loads during islanding events. A thorough sensitivity analysis is performed to identify the main factors that affect the VVR and the probability of voltage violation, which has not been presented in the literature so far. The main active and passive IDMs commonly applied to IBDGs were investigated, in addition to various RT requirements and voltage tolerance curves. The methodologies for obtaining the VVR and calculating the probability index can be reproduced for any distribution system by modeling its components and performing dynamic simulations. Moreover, the application results presented in this paper represent practical conditions commonly found in real electrical systems.

The proposed method serves as a valuable tool for distribution engineers to identify critical feeders that may require corrective measures to ensure the secure operation of the electrical system, such as revising the settings of DGs' anti-islanding protection or requesting end-users to apply additional protection for sensitive loads. Therefore, the main contributions of this paper can be listed as follows:

- Understand the key factors that affect the severity of post-islanding voltage transients before the IBDG disconnection;
- Introduce the concept of VVR, i.e., a region comprising operating conditions in the active power imbalance vs reactive imbalance plane ($\Delta P \times \Delta Q$) that may damage voltage-sensitive equipment when an unintentional islanding occurs;
- Introduce a method to calculate the probability of voltage violation due to voltage variations during unintentional islanding events;
- Assess how RT requirements impact the performance of the most widespread passive and active anti-islanding techniques applied to IBDGs.

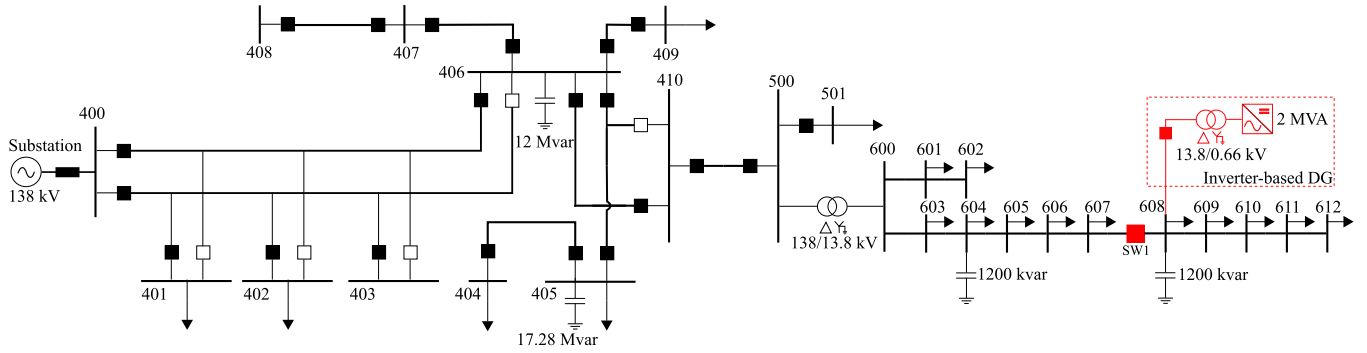


Fig. 1. Electrical system modeled in ATP. Based in: [25].

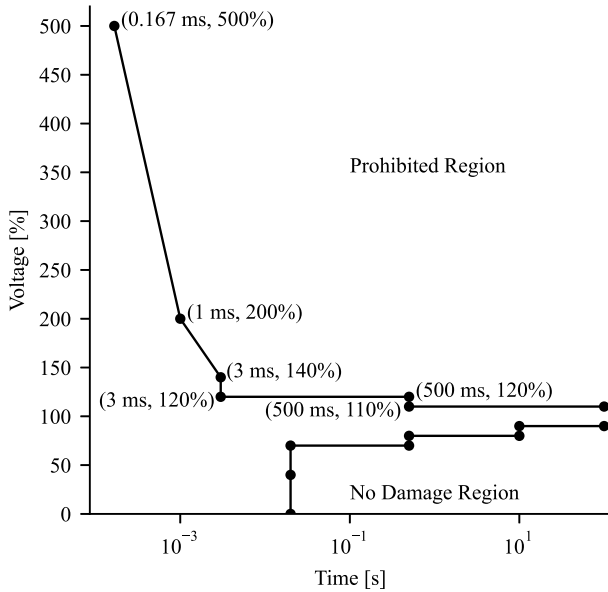


Fig. 2. ITIC voltage tolerance curve [24].

The paper is organized as follows: Section II elaborates on the problem under investigation. Section III presents the method for obtaining the VVR. The proposed method for quantifying the probability of voltage violation is presented in Section IV. Afterward, the application and simulation results are demonstrated in Section V, and Section VI discusses the main factors that affect the probability of voltage violation. Finally, the main conclusion and a few suggestions for future works are presented in Section VII.

2. Problem characterization

To explain the problem addressed in this paper, this section discusses simulation results that demonstrate severe overvoltages following unintentional islanding events, which can damage voltage-sensitive loads. The test system presented in Fig. 1 and the ITIC requirements [24] of Fig. 2 are employed. The ITIC voltage tolerance curve defines the tolerable limits for voltage excursion without affecting proper operation or damaging electronic devices [24].

The electrical system is based on a Brazilian distribution grid and comprises a high-voltage portion of 138 kV and a medium-voltage (MV) portion of 13.8 kV [25]. For the simulation results presented in this paper, all loads were modeled as constant impedance, as this is the most challenging scenario for islanding detection according to several studies [26–29] and is required by the IEEE Std. 1547.1-2020 [30] in the

conformance tests. There is a three-phase IBDG with a rated power of 2 MVA and constant power control connected to the MV grid at bus 608 through a 13.8/0.66 kV Dyn transformer. The average model of the IBDG was adopted to simplify the modeling of the switching devices. The IBDG control is implemented in the dq -frame and all parameters are described in the Appendix. In addition, the IBDG's output current is limited using the vector amplitude limitation technique [31]. The settings of under/overfrequency (ANSI 81U/O) and under/overvoltage (ANSI 27/59) protection functions are defined to disconnect the IBDG only if the frequency and voltage enter the shall trip region of IEEE Std. 1547-2018 [1], i.e., frequency thresholds of 56.5/62 Hz and voltage thresholds of 0.45/1.21 p.u., with a time delay of 160 ms.

The simulations are performed using the Alternative Transients Program (ATP), in which an unintentional islanding event is caused by the opening of switch SW1 (Fig. 1) at the time instant of 1 s. The results are presented in Fig. 3, which includes simulations under two operating conditions. In Fig. 3a, the ΔP and ΔQ are -0.08 p.u. and 0.51 p.u., respectively, with positive values indicating a deficit of active or reactive power. Also, the simulations presented in Fig. 3b have ΔP and ΔQ values of -0.12 p.u. and 0.10 p.u., respectively. In both scenarios, the results obtained with the IBDG operating solely with passive techniques are compared with results in which the General Electric Voltage Shift (GEVS) active IDM is enabled. More details regarding the modeling of this active IDM and the IBDG control are presented in Section 5.

In Fig. 3a, when the IBDG is operating with only passive techniques, the PCC voltage surpasses the overvoltage tolerance limit 134 ms after the islanding event ($t = 1$ s); however, in this case, the IBDG is disconnected only 178 ms after island formation. On the other hand, for the simulation with the GEVS active technique and the same operating conditions, the voltage transient does not violate the ITIC tolerance limit, and the IBDG is disconnected 176 ms after islanding.

Additionally, in Fig. 3b, a voltage violation occurs only when the IBDG is equipped with the GEVS active technique. In this case, the voltage surpasses the ITIC limit 20 ms after islanding, while the DG is disconnected only 177 ms after the event. Repeating the simulation with only passive techniques, the DG is disconnected 202 ms after islanding, and the voltage transient does not enter the ITIC damage region.

In both scenarios, voltage-sensitive loads could be damaged due to voltage transients occurring before the DG disconnection. This highlights the importance of understanding the phenomenon and motivates the development of an assessment methodology to identify risky operating conditions.

3. Voltage violation region

To map the operating conditions that cause damage to sensitive loads between islanding taking place and the DG disconnection, we propose the concept of VVR, i.e., an area in the $\Delta P \times \Delta Q$ plane, given by the operating points with voltage violation before DG disconnection. The

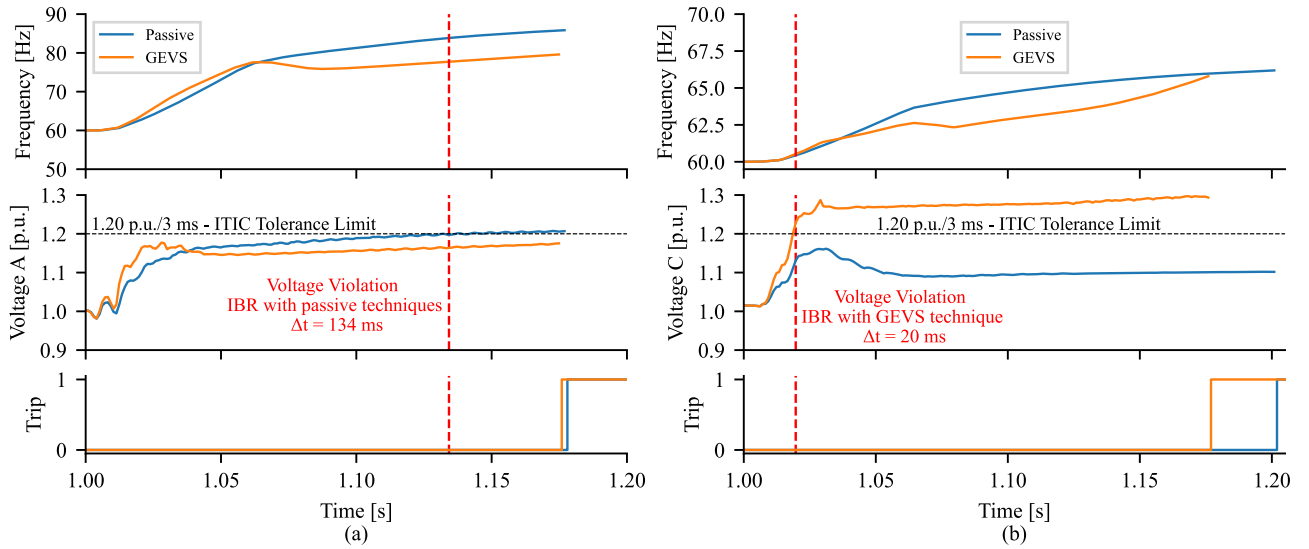


Fig. 3. Example of voltage violation during an islanding operation, when the IBDG is equipped with only passive techniques and with GEVS technique. Simulation with (a) ΔP of -0.08 p.u. and ΔQ of 0.51 p.u.; (b) ΔP of -0.12 p.u. and ΔQ of 0.10 p.u.

assessment of voltage violation must consider duration and amplitude requirements, similar to the ITIC curve of Fig. 2.

The method for determining the VVR is based on repeated dynamic simulations of unintentional islanding events. Consequently, all electrical system components must be carefully modeled for the simulations. The DG and load models should represent the characteristics of the DGs and load types typically found in the electrical system under analysis. Therefore, the following steps are required to obtain the VVR:

- Step 1:** Define the anti-islanding protection scheme and respective settings complying with voltage and frequency RT requirements defined by the utility/DG connection guidelines [1,11];
- Step 2:** Apply the voltage violation limits, concurring with the utility requirements [32] or VTC of sensitive loads [24] connected to the grid;
- Step 3:** Simulate several islanding events for a representative set of ΔP and ΔQ operating points, and identify cases where the load buses' voltages violate the pre-defined voltage violation limits before the trip of DG anti-islanding protections. In this step, the voltage in the load bus with the most significant variation is monitored;
- Step 4:** The VVR covers the set of operating points determined in the previous step.

The islanding simulations for delimiting the VVR are performed with ΔP and ΔQ operating points ranging from -1 p.u. to $+1$ p.u. This wide range is necessary to encompass a representative set of cases with over-voltages caused by the various active IDMs applied in the industry. The scenarios with an excess of active power ($\Delta P < 0$) are generated by fixing the IBDG active generation at 1 p.u. (unitary power factor), and varying the active load demand from 0 p.u. to 1 p.u. in small steps. Plus, cases with a deficit of active power ($\Delta P > 0$) are obtained by fixing the active load demand at 1 p.u. and varying the IBDG active power output from 0 p.u. to 1 p.u. in small steps. To map the operating points with different reactive power imbalances, the IBDG operates with a unitary power factor, and the reactive load demand varies from 0 p.u. to $(1 + Q_{CB})$ p.u., where Q_{CB} is the total reactive power of all capacitor banks inside the island (if any).

Fig. 4 presents an example of two VVRs obtained through multiple simulations carried out in ATP, with the IBDG operating with only 81U/O and 27/59 passive IDMs and with the GEVS technique. The islanding protection settings, VTC, IBDG model, and electrical system are the same from Section 2. For this set of islanding protection and voltage

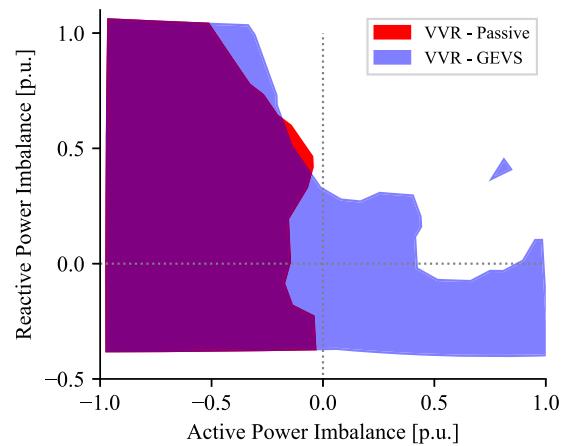


Fig. 4. VVRs when IBDG is operating with only passive techniques and with GEVS active technique.

requirements, the VVR with the GEVS technique is wider than the VVR in the simulations with only passive techniques. Still, the possibility of operating in a VVR when the IBDG has only passive techniques cannot be ruled out since it encompasses a region with ΔP values up to -1 p.u.

The subsequent sections will present the proposed method for assessing the probability of voltage violation. Moreover, the main factors affecting the VVR will be discussed through an in-depth sensitivity analysis employing dynamic simulations.

4. Probability of voltage violation

The previous section presented the method for obtaining the VVR, which consists of performing multiple dynamic simulations to delimit a region in the $\Delta P \times \Delta Q$ plane in which sensitive loads may be damaged due to severe post-islanding voltage transients. Therefore, considering an operating window (hours, days, or months), there is a real risk of voltage violation and damage to sensitive loads if the electrical system operates with power imbalance values within the VVR.

This concept is illustrated in Fig. 5, in which the opening of a switch results in an islanded system with an IBDG and some loads. The ΔP

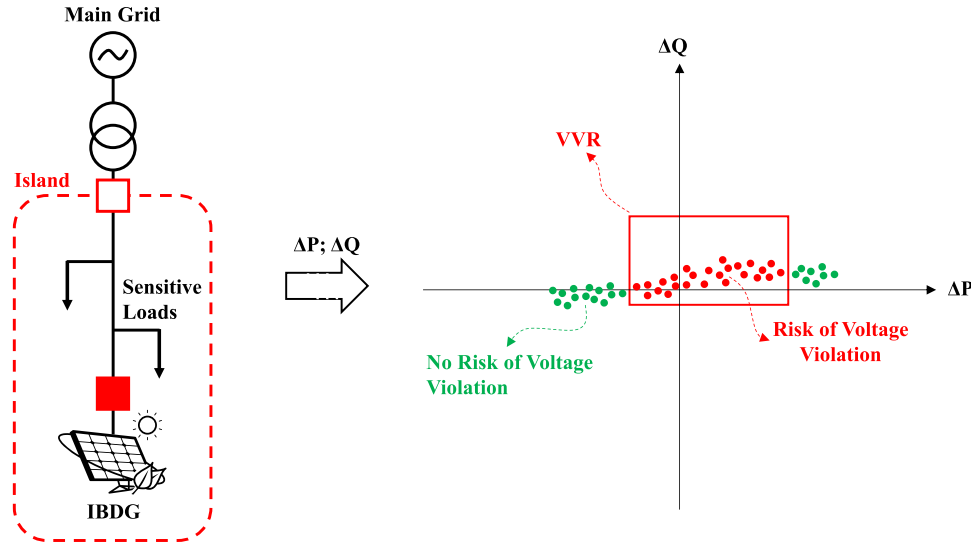


Fig. 5. Concept of the probability of voltage violation.

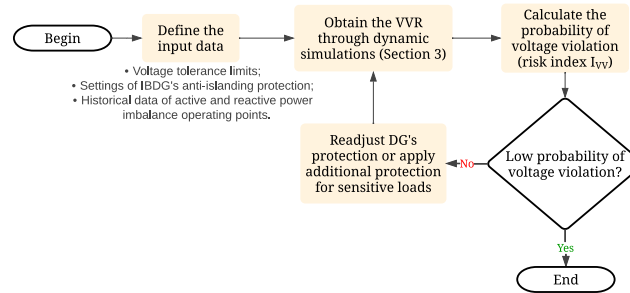


Fig. 6. Flowchart of the proposed method for probability of voltage violation calculation.

and ΔQ values represent the mismatches between load consumption and DG's generation. In this work, the probability of voltage violation is represented by the risk index of post-islanding voltage violation (I_{VV}) given by:

$$I_{VV} = \frac{N_V}{N_M} \times 100[\%] \quad (1)$$

where N_V is the number of power imbalance measurements inside the VVR in the $\Delta P \times \Delta Q$ plane, and N_M is the total number of power imbalance measurements.

The outputs of this work are valuable for utility engineers to identify critical feeders that need actions to guarantee a secure operation of the electrical system, e.g., review the settings of DG islanding protections or request additional protection for sensitive loads. The complete method for VVR definition and calculation of the probability of voltage violation is divided into three main steps: initialization, execution of dynamic simulations, and analysis of the power imbalance measurements. These steps, illustrated by flowchart of Fig. 6, are described as follows:

- Step 1:** Define the input data, i.e., historical data of ΔP and ΔQ operating points, settings of the IBDG's anti-islanding protection, and voltage violation limits present in grid codes or regulations;
- Step 2:** Obtain the VVR (Section 3) by performing the simulation of islanding events and storing the ΔP and ΔQ operating points in which the voltage signals enter the prohibited region of the VTC before DG's disconnection;
- Step 3:** Calculate the risk index of voltage violation (I_{VV}) given by the number of power imbalance operating points that are within the VVR;
- Step 4:** Decision-making process.

5. Application and results

This section presents a sensitivity analysis of the VVR and the probability of voltage violation for different islanding protection requirements and VTCs. The results are obtained for the test system shown in Fig. 1, modeled in ATP for the transient simulations required to obtain the VVR. The defined test cases, including the IBDG model, anti-islanding protections, and PQ requirements, encompass practical scenarios representative of the challenges faced in the operation of modern power systems.

The IBDG anti-islanding protections and inverter's control are modeled in ATP using the MODELS language. The employed active IDMs are based on the positive feedback concept: slip-mode frequency shift (SMS), Sandia frequency shift (SFS), general electric frequency shift (GEFS), and GEVS. These IDMs are chosen for their wide application in the grid-tie solar inverter industry [3,4,33], and the block diagrams of the IBDG control with each technique are depicted in Fig. 7. All defined parameters are presented in Appendix A. Additionally, case studies are conducted considering the IBDG equipped only with passive techniques ANSI 81U/O and ANSI 27/59, since they are required by several grid codes [11,24].

The islanding event is simulated by the opening of switch SW1. In addition, the voltage and frequency signals are monitored at the PCC of the IBDG (bus 608), which is disconnected if the 81U/O or 27/59 protection functions trip. Two different groups of settings are evaluated in this paper, as presented in Table 1. Setting 1 is defined with basis on the RT requirements presented in IEEE Std. 1547-2018 [1], and all functions have a time delay of 160 ms. Furthermore, the requirements of Brazilian grid code PRODIST Module 3 [11] are considered in Setting 2, which has instantaneous stages for the 27/59 functions.

Table 1
Settings of frequency and voltage protection functions.

ANSI	Setting 1		Setting 2	
	Threshold	Time Delay	Threshold	Time Delay
81U	56.5 Hz	160 ms	56.9 Hz	100 ms
81O	62 Hz	160 ms	63.1 Hz	100 ms
			0.50 p.u.	500 ms
27	0.45 p.u.	160 ms	0.20 p.u.	0 ms
			1.11 p.u.	1000 ms
59	1.21 p.u.	160 ms	1.20 p.u.	0 ms

Table 2
Voltage tolerance limits.

Curve	Voltage Limit	Duration
ITIC [24]	1.10 p.u.	500 ms
	1.20 p.u.	3 ms
	2.0 p.u.	2 ms
Brazilian Regulation [32]	1.10 p.u.	16.67 ms

Moreover, the voltage signals are monitored at the load buses to assess the possibility of voltage violation. Two voltage tolerance characteristics are defined in Table 2, according to the ITIC curve [24] and Brazilian regulation (PRODIST Module 8) [32]. For the ITIC curve (Fig. 2), the prohibited region for events with a duration longer than 2 ms is solely considered. Also, Brazilian regulation [32] defines nine sensitivity regions in terms of the amplitude and duration of short-term voltage variations to characterize the impact of these events. The regions are proposed based on the tolerance of several loads connected to the electrical grid. This paper solely considers the most sensitive region (i.e., overvoltage violations) with a voltage swell with an amplitude of at least 1.10 p.u. and a duration of 1 cycle.

To determine the voltage violation probability, 14,208 power imbalance measurements (ΔP and ΔQ power measurements) were obtained at switch SW1 (Fig. 1) through power flow calculations in OpenDSS, using real load/generation profiles provided by a Brazilian utility from September 2022 to July 2023. From this amount, 7245 measurements refer to a period with solar irradiation. In Fig. 8a to c, the mean active and reactive power of the loads and the mean generation profile of the

IBDG for each month are presented in the per unit system (same basis as the IBDG of 2 MVA). These profiles, used as inputs for the power flow calculations in OpenDSS, result in the power imbalance measurements at switch SW1, as shown in Fig. 8d. In a practical application, if power imbalance measurements are directly available at the switching device responsible for island formation, these power flow calculations would not be necessary. Therefore, the historical data could be used to directly determine the risk index with basis on the VVR.

The following subsections present the simulation results obtained for two cases: 81U/O and 27/59 protection functions adjusted in compliance with IEEE Std 1547-2018 and protection settings based on the requirements of the Brazilian grid code. In all results presented in sequence, the power imbalance values are expressed in per unit, on the same basis as the IBDG under study, i.e., a base power of 2 MVA.

5.1. IEEE RT requirements

This subsection presents the VVR and probability of voltage violation when the 81U/O and 27/59 are adjusted based on the RT requirements of IEEE Std. 1547-2018 [1] (Setting 1 from Table 1).

Fig. 9 presents the graphical representation of the VVR and the probability of voltage violation when the IBDG is equipped with only passive islanding detection methods. In Fig. 9a and b, the VVR is shown considering the voltage tolerance limits from the ITIC curve and Brazilian regulation, respectively. Additionally, in Fig. 9c and d, graphical representations of the probability of voltage violation in the $\Delta P \times \Delta Q$ plane are presented for the same voltage tolerance limits. The ΔP and ΔQ power imbalance measurements within the VVR are colored in red and represent the violation region. Moreover, the secure region refers to the ΔP and ΔQ power imbalance measurements located outside the VVR, i.e., voltage transients after unintentional islanding remain within the overvoltage violation limits.

Considering the ITIC tolerance curve in Fig. 9a, the VVR encompasses a wide region in the $\Delta P \times \Delta Q$ plane with an excess of active power imbalance ($\Delta P < 0$), resulting in a probability of voltage violation of 67% (Fig. 9c). Moreover, the VVR increases (Fig. 9b), and the probability index reaches 72% (Fig. 9d) by adopting requirements from Brazilian regulation since it defines a strict overvoltage limit of only 1.1 p.u. with duration of one cycle.

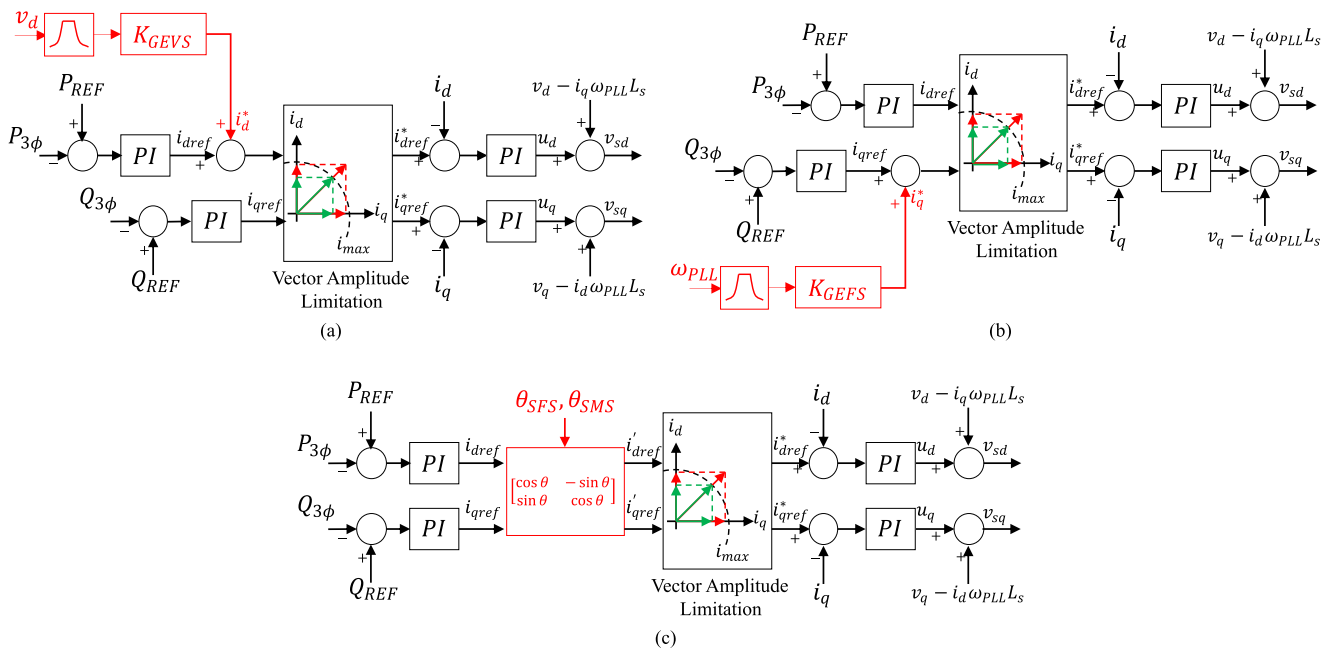


Fig. 7. Block diagram of the IBDG's control in the dq -frame with: (a) GEVS, (b) GEFS, (c) SFS and SMS technique.

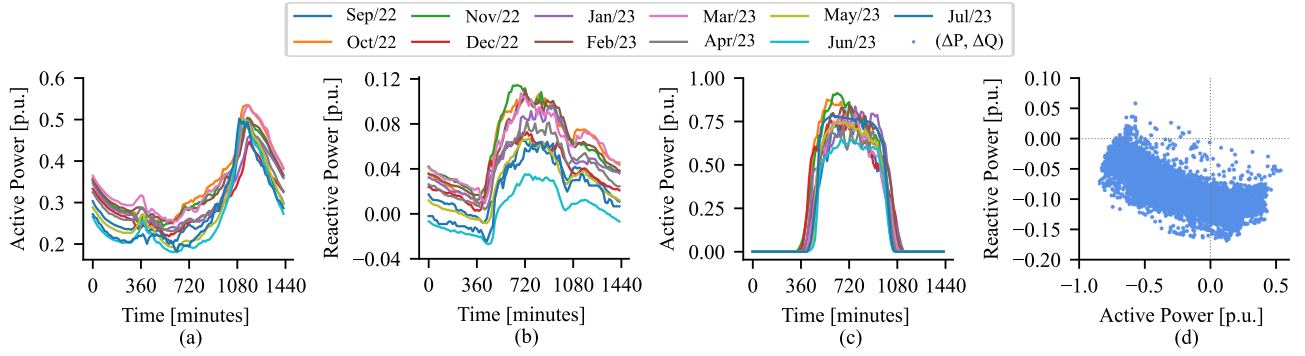


Fig. 8. Measured data in Brazilian feeder: (a) Load's active power, (b) Load's reactive power, (c) IBDG's generation profile, and (d) power imbalances (ΔP , ΔQ) at switch SW1.

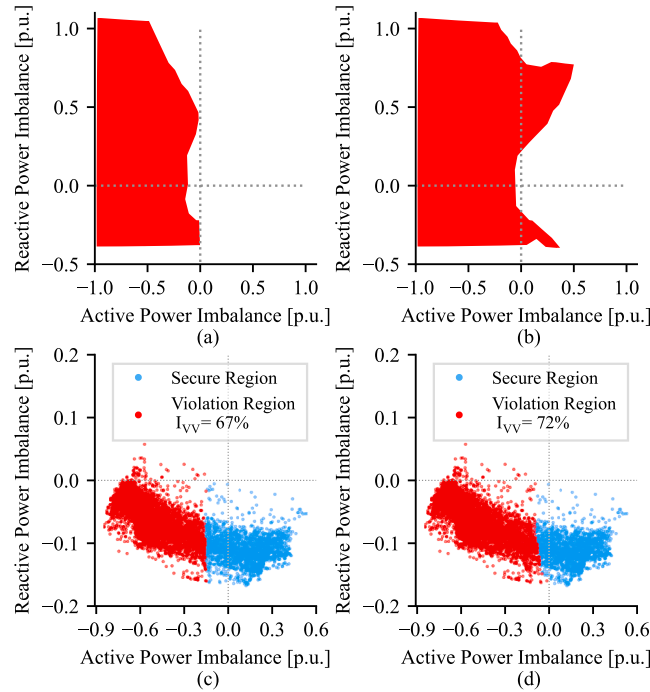


Fig. 9. (a, b) VVRs and (c, d) corresponding probabilities of voltage violation I_{VV} in the $\Delta P \times \Delta Q$ plane for simulations with passive IDMs adjusted with Setting 1, considering the ITIC curve (a, c) and Brazilian regulation (b, d).

The same study is conducted for the different active IDMs, and the results are shown in Fig. 10, considering only the overvoltage violation limits from the ITIC curve. The VVR is represented by the red area in Fig. 10a to d for the SFS, SMS, GEVS, and GEFS active techniques, respectively. Also, Figs. 10e to h illustrate the probabilities of voltage violation for the same active techniques, in which the power imbalance measurements within the respectively VVR are represented by red points.

The most critical scenarios occur when the IBDG is equipped with the GEVS (Fig. 10c) and GEFS (Fig. 10d) schemes. For these IDMs, the instability caused by the positive-feedback loop is sufficient to cause a transient after the islanding inception that violates the ITIC tolerance limit. The voltage at the load buses violates the overvoltage limit even for a wide range of operating points with a deficit of active power ($\Delta P > 0$). Additionally, the SMS technique shows the smallest VVR among the studied active IDMs (Fig. 10b) as it causes frequency disturbances after islanding without leading to transient overvoltages in scenarios with $\Delta P > 0$.

The I_{VV} index for the studied active IDMs is shown in Fig. 11, considering the overvoltage violation limits from both the ITIC curve and the Brazilian Regulation. When 81U/O and 27/59 protection functions are

adjusted with setting 1, the probability of voltage violation is greater than 67% for all islanding protections. Among the active IDMs, GEFS and GEVS present the highest indexes (up to 100%), while the SFS scheme has the lowest indexes of 72% and 69%. This scenario has a high probability of voltage violation because the overvoltage function is adjusted with a threshold of 1.21 p.u. and a time delay of 160 ms, not being coordinated with the overvoltage tolerance limits. The prohibited region of the ITIC curve has a first stage in 1.1 p.u./500 ms and a second stage in 1.2 p.u./3 ms, violating the overvoltage limit before the disconnection of the IBDG for several power measurements. In addition, Appendix B presents a sensitivity analysis on the impact of the different seasons of the year on the I_{VV} index.

After changing the tolerance curve to the Brazilian regulation limits, the results are similar since this regulation defines a sensitive voltage violation limit of 1.1 p.u. for more than 16.67 ms.

5.2. Brazilian grid codes

This subsection outlines the results of adjusting islanding protections based on Brazilian grid codes (Setting 2 from Table 1). This setting

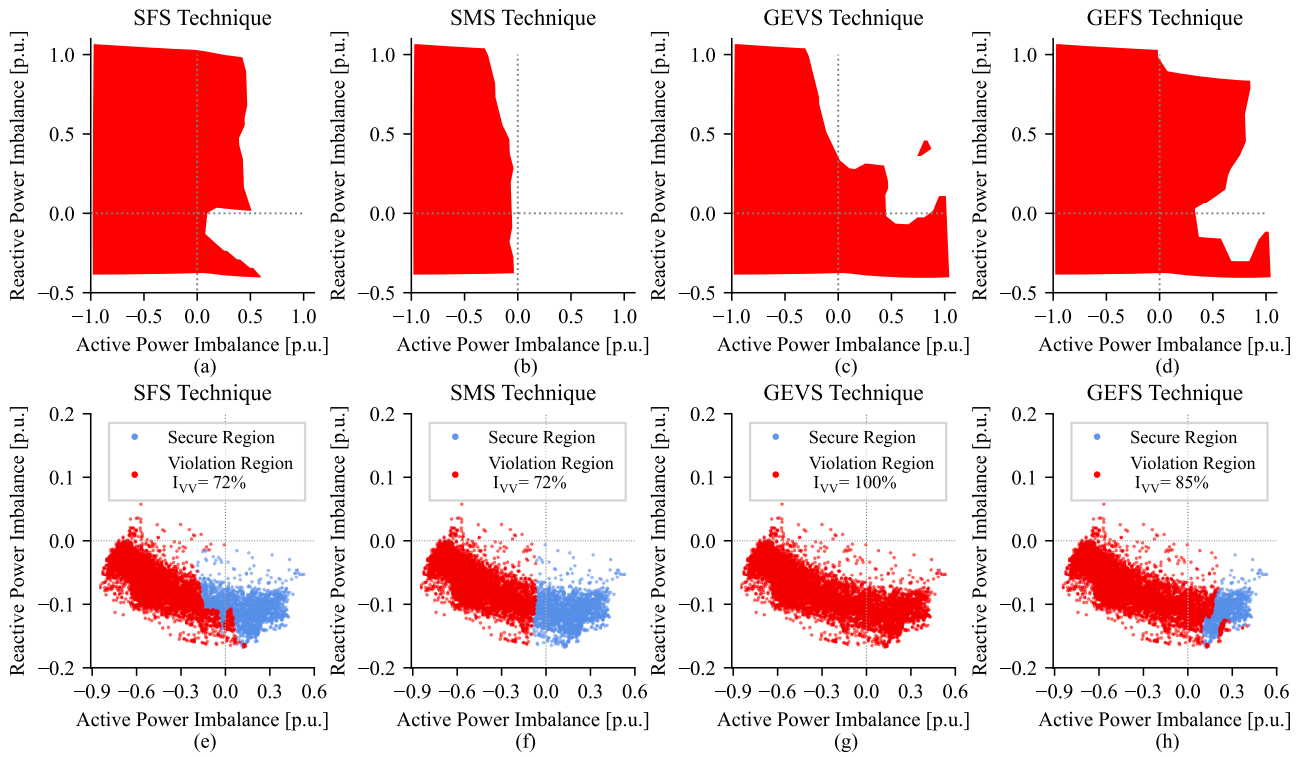


Fig. 10. (a-d) VVR and (e-h) corresponding probabilities of voltage violation when the IBDG is equipped with four different active IDMs. The islanding protections are adjusted with Setting 1, and the ITIC requirements are defined for voltage violation.

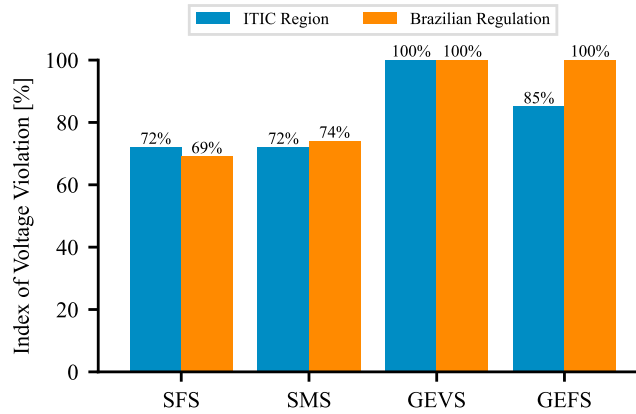


Fig. 11. I_{VV} index of voltage violation when the IBDG is operating with different active IDMs. Function 81U/O and 27/59 adjusted with Setting 1.

presents different pickups and time delays compared to Setting 1, and the most significant difference is that it includes instantaneous stages on 27/59 protection functions, enabling a fast disconnection of the IBDG if the grid is subjected to severe voltage transients after islanding. Moreover, frequency functions have a reduced time delay of 100 ms.

Fig. 12 shows the VVR (Fig. 12a) and the power imbalance measurements within the VVR (violation region in Fig. 12b) when the IBDG is equipped only with passive techniques. Also, the voltage tolerance limits from the Brazilian regulation are considered. In this scenario, the VVR is limited to ΔP values close to zero, while in the ΔQ axis, it is extended from -0.5 p.u. to $+1$ p.u. It happens because the voltage excursions after islanding are strongly related to the ΔP magnitude [34]. Hence, the instantaneous thresholds of the voltage protections ensure a fast disconnection of the IBDG for increased ΔP values before the violation of the tolerance limit. Moreover, this region is significantly smaller

than the VVR obtained with protections adjusted with Setting 1. Also, only a few power imbalance measurement points are inside the VVR region, resulting in a probability of voltage violation of only 4%.

The results obtained for the different active IDMs are presented in Fig. 13, which displays the VVR (Fig. 13a to d) and the power imbalance measurements probabilities in the $\Delta P \times \Delta Q$ plane (Fig. 13e to h) for the SFS, SMS, GEVS and GEFS techniques, respectively.

The adoption of the protection settings from the Brazilian grid code results in a reduction in the VVR for all studied active IDMs. The SFS scheme shows the smallest VVR with only three power imbalance points (Fig. 13a). Further, the VVR in terms of ΔP are eminently small for SMS and GEVS IDMs, i.e., close to zero in Fig. 13b and c. The most critical scenario happens for the GEFS IDM (Fig. 13d), in which the VVR encompasses several operating points with $\Delta P > 0$.

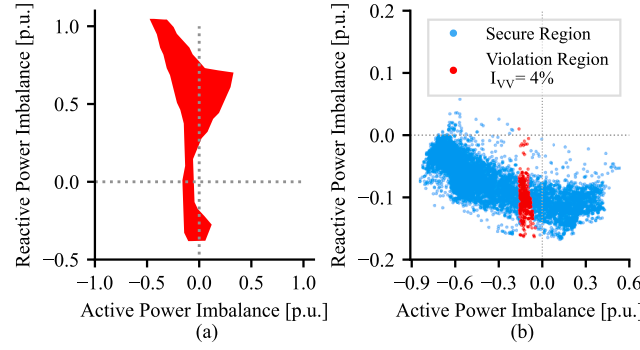


Fig. 12. (a) VVR and (b) power imbalance measurements with voltage violation when the IBDG operates with only passive techniques, adjusted with Setting 2 and VTC based on Brazilian regulation.

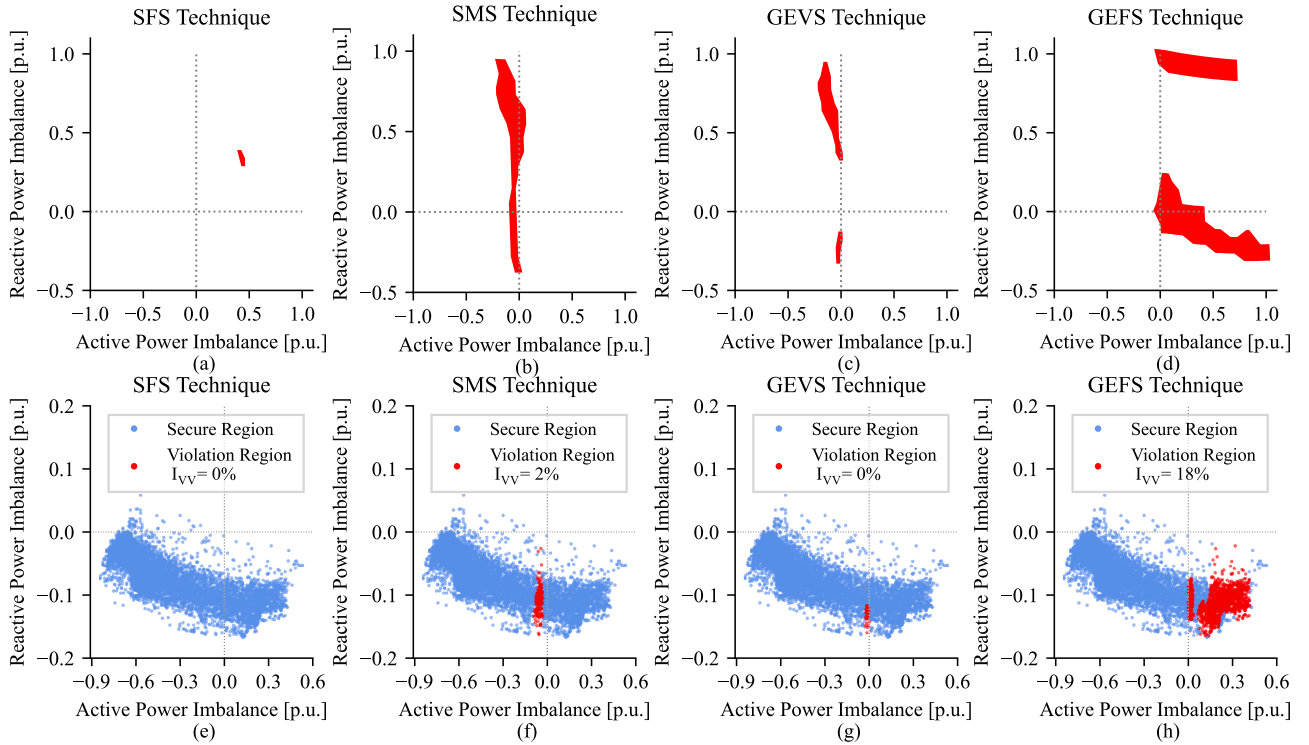


Fig. 13. (a-d) VVR and (e-h) power imbalance measurements with voltage violation when the IBDG operates different active IDMs. Frequency and voltage protections adjusted with Setting 2 and VTC based on Brazilian regulation.

Regarding the analysis of the power imbalance measurements inside the VVRs (Fig. 13e to h), in the scenario with the SFS technique, the probability index I_{VV} is zero since no operating point is within the region defined by the VVR. Moreover, the probability index I_{VV} is only 0.5% and 2% for the GEVS and SMS techniques, respectively. The most critical condition occurs for the GEVS technique, with an I_{VV} index of 18%. These indices are also highlighted in Fig. 14, in which the adoption of the ITIC curve did not result in a VVR, regardless of the IDM (passive or active). This performance is expected since the settings of 27/59 protection functions are more sensitive than the ITIC limit.

6. Discussions

In the previous section, IEEE Std. 1547-2018 was adopted as a reference for adjusting islanding protections. Under this configuration, an increased VVR was observed. This increase resulted in probability indexes from 69% to 100%, regardless of the voltage tolerance limits considered. On the other hand, by adopting at least one instantaneous stage

of voltage protections (required by the Brazilian grid codes), the VVR is reduced, and the probability indexes are limited to 18%.

To highlight the different transients imposed by the studied active techniques, Fig. 15 presents the results of simulations of an islanding event at $\Delta t = 1$ s with 0.43 p.u. of ΔP and 0.29 p.u. of ΔQ , frequency and voltage protection functions adjusted with Setting 2. In this situation, there is a voltage violation only when the IBDG is operating with the SFS technique and the voltage tolerance limit from Brazilian regulation is adopted.

When the IBDG is equipped with the SFS technique, only the Brazilian regulation tolerance limit of 1.10 p.u. is violated for one cycle. Moreover, the post-islanding dynamic imposed by the GEFS technique is similar in this operating condition since voltage A drops to 0.4 p.u. before rising above 1.1 p.u. However, since the protection trips if the voltage reaches 1.20 p.u., the limit from the Brazilian regulation is not exceeded for more than one cycle, and consequently, there is no voltage violation for the GEFS technique. Furthermore, when the IBDG is operating with the SMS technique, voltage in phase A rapidly decreases after islanding, reaching a value of 0.2 p.u., which violates the threshold of function

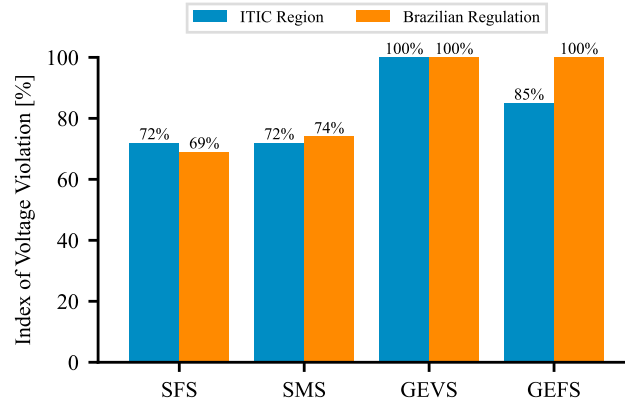


Fig. 14. Index of voltage violation when the IBDG is operating with different active IDMs. Function 81U/O and 27/59 adjusted with Setting 2.

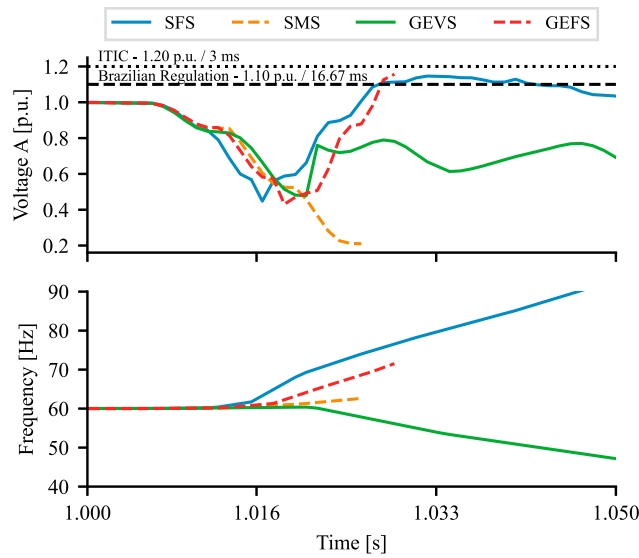


Fig. 15. Results of simulations with SFS, SMS, GEVS and GEFS techniques. Operating condition with ΔP of 0.43 p.u. and ΔQ of 0.29 p.u., functions 81U/O and 27/59 adjusted with Setting 2.

27 and disconnects the DG. At the same time, the frequency remains close to 60 Hz. Finally, the GEVS technique leads to a decrease in the post-islanding voltage magnitude with values within the range of 0.4 to 0.8 p.u. During the same interval, the frequency drops below 50 Hz.

It is important to highlight that the obtained results may vary depending on the parameters of the active IDMs. The strategy adopted in this paper is to select the minimum gains in the positive-feedback loop that ensure islanding detection in a condition with a resonant load and unitary load quality factor (more details in the Appendix); however, as the gain in the feedback loop increases, the greater the disturbance and harmonic distortion imposed by the active techniques.

From the results presented in this paper, it is possible to identify four main factors that influence the probability of voltage violation, which are briefly discussed below:

1. **RT requirements:** Grid codes recommend ranges of frequency and voltage in which DGs must remain connected to the grid, giving support in the occurrence of disturbances. Therefore, if the DG is required to operate even for large frequency/voltage excursions, sensitive loads nearby will be subjected to severe transients after island formation. On the other hand, if the RT requirements are more per-

missive, the DG may be rapidly disconnected after unintentional islanding, avoiding risks to consumers.

2. **Anti-islanding protection:** Each active IDM has its operating principle, resulting in different transients after island formation. This paper verified that the GEFS technique results in the largest VVR due to voltage transients after islanding. It is also shown that the operation with only passive techniques poses a risk to sensitive loads. These results highlight the importance of establishing requirements for the parameterization of active techniques so that the islanded system is not subject to excessive voltage variations for extended periods.
3. **Voltage tolerance limits of sensitive loads:** Some loads may support severe transients for longer periods. For example, the PRODIST voltage tolerance limit [32] is violated if the voltage signal exceeds 1.10 p.u. for more than one cycle (60 Hz). On the other hand, the ITIC tolerance limit [24] is violated if the voltage signal exceeds 1.20 p.u. for more than 3 ms or 2 p.u. for more than 2 ms. In this paper, the obtained VVR for the PRODIST tolerance limit is thereby larger than the region for the ITIC tolerance limit, except for the simulations with the SFS active technique.
4. **Active and reactive power imbalances operating points:** The factors mentioned above directly determine the size of the VVR in the

Table 3
Comparison of the presented paper with other related literature.

Ref.	Methodology	Anti-Islanding Protection	RT Requirements	Voltage Tolerance Curves	Risk Assessment
[19]	Assessment of historical data	Not specified	No	Yes	No
[20]	On-site tests	Not specified	Yes	No	No
[21]	Hardware tests	Not specified	No	No	No
[22]	EMT simulations and hardware tests	Passive	Yes	Yes	No
[23]	EMT simulations	Passive	No	No	No
Presented Paper	Dynamic Simulations	Passive and active	Yes	Yes	Yes

$\Delta P \times \Delta Q$ plane. Moreover, the voltage tolerance limit of the loads will only be violated if the islanding event occurs while the electrical system operates inside this critical region.

A comparison of the main characteristics of the presented paper with other related literature is presented in Table 3. The occurrence of over-voltages following unintentional islanding events has been addressed by previous literature through different methods, which include assessment of historical data [19], on-site tests [20], in addition to hardware tests [21,22] and EMT simulations [22,23]. However, most of these studies do not specify the IBDG model or the anti-islanding protection under analysis or consider only passive IDMs. Also, only references [20] and [22] have considered the RT from IEEE Std. 1547-2018 in the presented analysis. Another relevant topic, which has been addressed only by references [19] and [22], is the violation of voltage tolerance curves for sensitive loads and PQ criteria due to voltage transients following unintentional islanding events. Moreover, recent literature focuses on proving the magnitude of these violations, without proposing a risk-assessment method for grid operators.

In contrast, the presented work proposed a method based on dynamic simulations to map the operating conditions that pose a risk to voltage-sensitive loads and violation of PQ requirements. Moreover, based on a thorough sensitivity analysis, this work incorporates the most widespread passive and active IDMs, RT requirements, and voltage tolerance limits from different standards and grid codes.

7. Conclusion

This paper introduced the new concept of the VVR and proposed a method for calculating the I_{VV} index, which has not been reported in the literature so far. From this measure, utility engineers can assess the probability of voltage violations when unintentional islanding occurs and islanding protections fail to disconnect the DG promptly. The proposed methods are based on dynamic simulations and can be reproduced in any electrical system by modeling its components, such as loads and DGs. The results of this work were obtained for the most widespread passive and active IDMs in the grid-tie solar inverter industry, and the test cases encompass the main characteristics of real electrical systems. Relying on a thorough sensitivity analysis, this paper demonstrates that the most recent frequency and voltage RT requirements can increase the detection time of the most common passive and active anti-islanding protections, thereby increasing the risk of PQ disturbances and damage to voltage-sensitive loads before DG disconnection during unintentional islanding.

When active IDMs are employed, the VVR can be extended to scenarios with deficit of active power imbalance. In addition, voltage violations can be significantly reduced by properly adjusting the anti-islanding protection. The proposed I_{VV} index offers a valuable tool for distribution engineers to assess these risks and propose mitigation strategies to ensure the secure operation of the electrical system. Therefore, in

practice, feeders that need additional protection for sensitive equipment or a revision in frequency and voltage requirements can be identified. Although the results are presented for grid-following IBDGs, new simulations can be extrapolated to grid-forming IBDGs and synchronous-based DGs. Further research also includes analyzing different electrical systems and load types, such as nonlinear loads, which may affect transients after an unintentional islanding event and affect the size of the VVR.

CRediT authorship contribution statement

Rodrigo de Barros Iscussati: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Conceptualization; **José Carlos Melo Vieira:** Writing – review & editing, Writing – original draft, Visualization, Supervision, Methodology, Conceptualization; **Reza Bakhshi-Jafarabadi:** Writing – review & editing, Writing – original draft, Methodology, Investigation, Conceptualization; **Daniel Motter:** Writing – review & editing, Writing – original draft, Methodology, Investigation, Conceptualization; **Marjan Popov:** Writing – review & editing, Writing – original draft, Supervision, Methodology, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

Appendix A. IBDG and active IDMs parameters

The parameters of the IBDG modeled in this paper are presented in Table A.4. The active IDMs settings were defined through dynamic simulations in an islanding test system based on the IEEE Std. 1547.1-2020 [30], and are presented in Table A.5. The strategy was to guarantee islanding detection with minimum harmonic distortion in a condition with a resonant load and unitary quality factor.

Table A.4
Parameters of the studied IBDG.

Parameter	Value	Parameter	Value
Filter Capacitance	300 μF	Rated AC Voltage	660 V
Filter Inductance (Grid)	0.53 mH	Frequency	60 Hz
Filter Inductance (IBDG)	1.5 mH	DC Link Voltage	1500 V
Fixed P Control - K_f	5	Rated Power	2 MVA
Fixed P Control - K_p	0.5	Maximum Current	1.10 p.u.
Fixed I Control - K_i	8	PLL - K_f	2.76
Fixed I Control - K_p	0.5	PLL - K_p	0.6

Table A.5
Parameters of the active techniques.

Active Technique	Parameters
SFS	$K_{SMS} = 0.026$; $C_{f0} = 0.05$
SMS	$\theta_m = 7.81^\circ$; $f_m = 63.5$ Hz
GEFS	$K_{GEFS} = 0.012$; $T_w = 0.159$ s; $T_0 = 0.0159$ s
GEVS	$K_{GEVS} = 1.43$; $T_w = 0.159$ s; $T_0 = 0.0159$ s

Appendix B. Impact of seasonality on the index of voltage violation

This appendix presents an analysis of the I_{VV} index in the face of variations on power imbalance operating points throughout the different seasons of the year.

Fig. B.16 presents the power imbalance measurements of the distribution system under analysis, based on a real electrical system located in the southeast region of Brazil, grouped by each season of the year. An important characteristic of the load/generation profiles is that the

data refer to an electrical system located in a region with tropical climate, where irradiation levels do not vary significantly throughout the year, except during the winter. This feature reduces the variability of the imbalance measurements.

It is noted that only the maximum and minimum reactive power imbalance values change slightly across the different periods of the year. In contrast, the active power imbalance values remain within the same maximum and minimum values. This is observed because the peak load, previously presented in Fig. 8 from Section 5, represents only 50% of the maximum generation. Therefore, although load profiles may differ throughout the year, they are not reflected in the power imbalance operating points.

Fig. B.17 presents the I_{VV} index for each season of the year, considering the IBDG equipped with different active IDMs. Moreover, 81U/O and 27/59 protection functions are adjusted with Setting 1. Since most measurements have negative ΔP values, i.e., an excess of active power, the risk index does not vary significantly and remains high throughout the year.

For the SFS and SMS techniques, the risk index varies only 4% independent of the voltage tolerance curve under consideration (ITIC or Brazilian Regulation). Also, for the GEVS technique, the index is close to 100% throughout the entire period under analysis. The greatest variation in the index occurs for the GEFS technique, ranging from 81% to 89% when the voltage tolerance limits from the ITIC curve are considered.

Therefore, for the test system under analysis, the conclusion would be similar regardless of the time of year, and a small number of power imbalance measurements could be selected. It is worth noting that the conclusions of this analysis apply only to the electrical system under analysis, and the results may differ for other electrical systems.

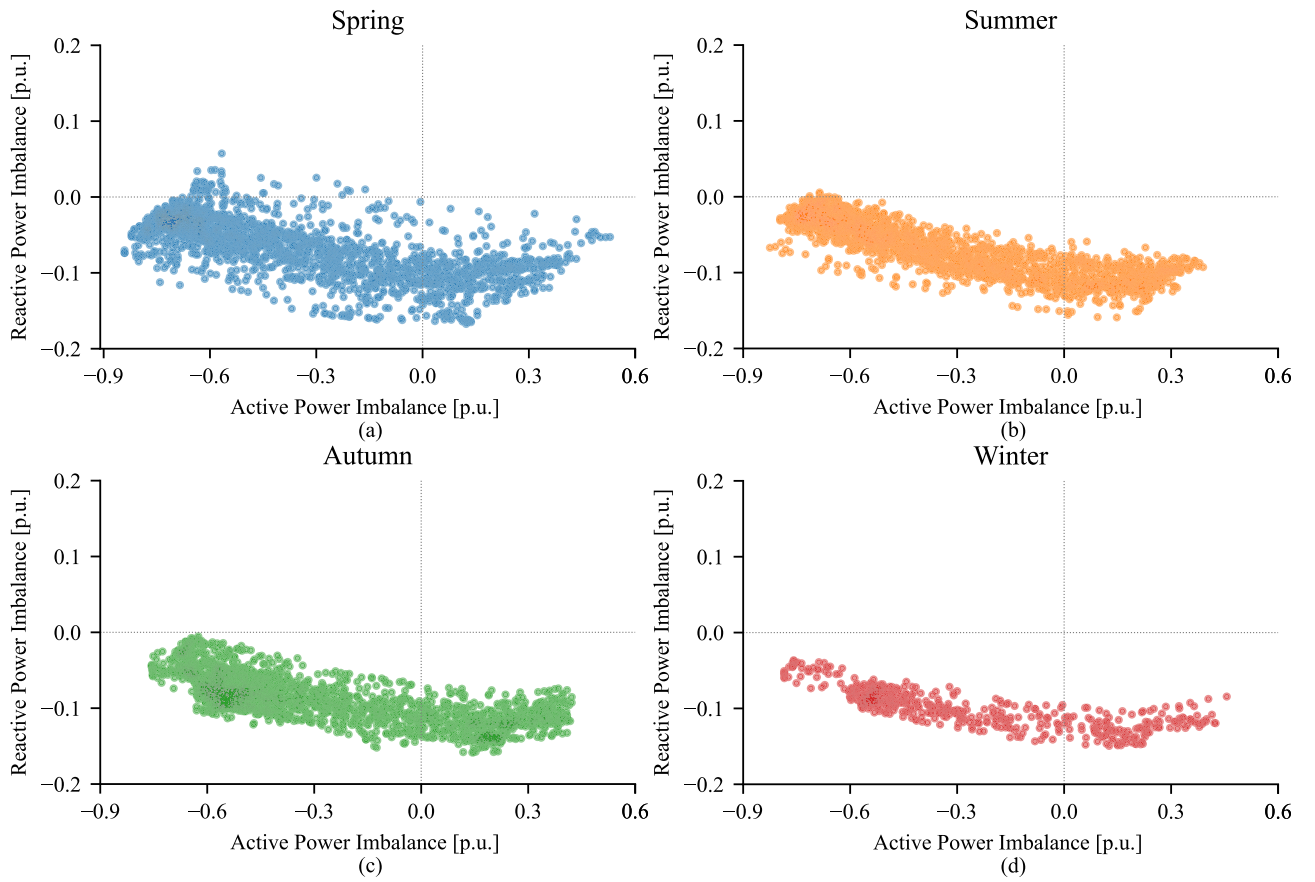


Fig. B.16. Power imbalance measurements grouped by season: (a) Spring, (b) summer, (c) autumn, and (d) winter.

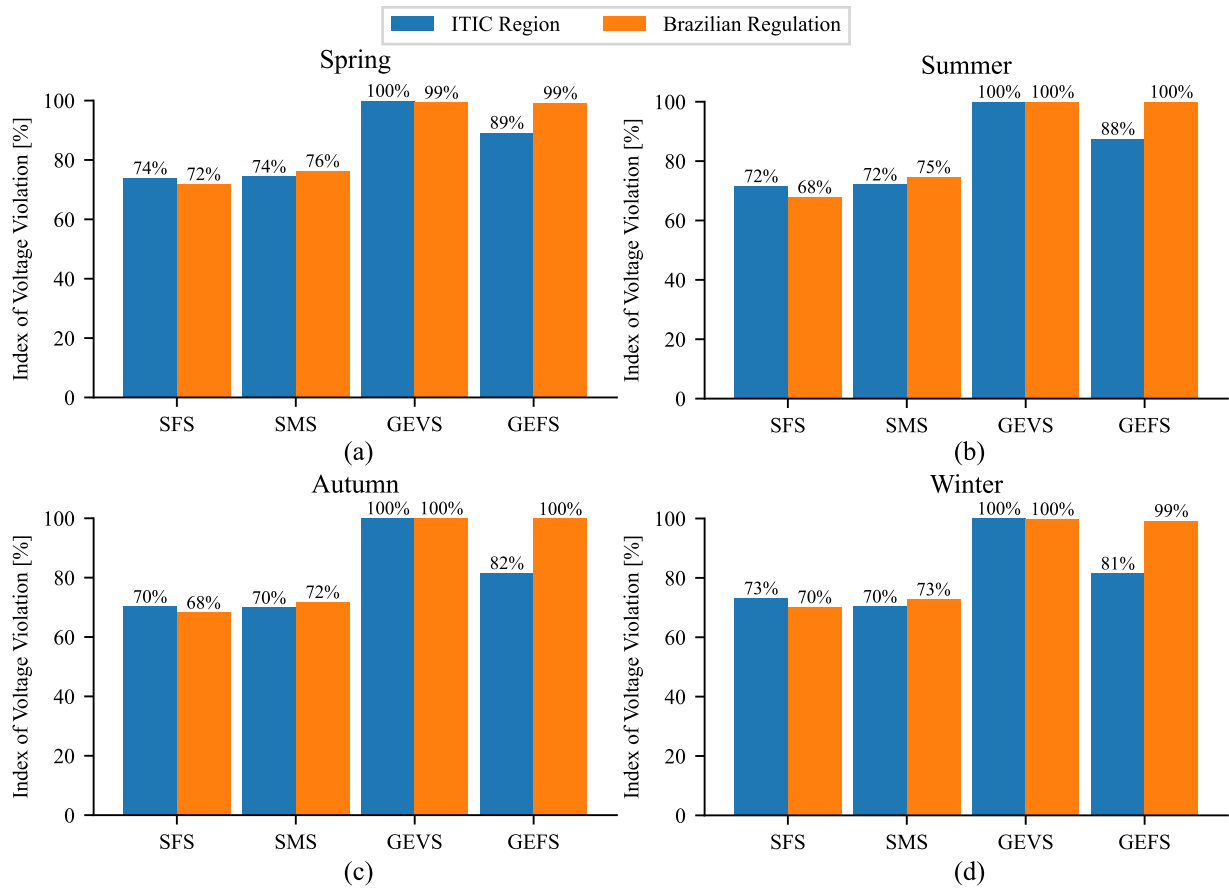


Fig. B.17. Risk index I_{VV} for different seasons of the years considering all active IDMs under study. Protection functions 81U/O and 27/59 are adjusted with Setting 1.

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