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A Class-D Piezoelectric Speaker Driver Using A Quadrature Feedback Chopping Scheme achieving 29dB Large-Signal THD+N Improvement

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Abstract

This paper presents a Class-D piezoelectric speaker driver that employs a quadrature feedback chopping scheme (QCS). Compared to a conventional single feedback chopping scheme (SCS), the use of QCS can eliminate the timing skew between low-voltage (LV) and high-voltage (HV) choppers, greatly improving large-signal linearity. A prototype implemented in a 180nm BCD process achieves a peak THD+N of -88dB/-92.5dB for a 1kHz/ 6kHz input frequency and 37μV_{RMS} output noise (A-weighted) while driving a 4μF load. Thanks to QCS, the large-signal THD+N has been improved by 29 dB, while the output voltage swing achieving -60dB THD+N has been extended from 86.9% to 99.5% of the full-scale (FS).

Introduction

Piezoelectric speakers are mainly capacitive. They have a small form factor and have become increasingly attractive for audio applications. For better audio quality, speakers with higher capacitance are preferred, which require drivers to provide high output current and large output voltage swing with good linearity [1]. Conventional Class-D amplifier (CDA) drivers employ an inductor in series with the speaker and require a series resistor (~10Ω) [2] to dampen the LC resonance, seriously limiting the output current and voltage swing, while consuming power. A low-power resistorless CDA [1] [Fig. 1(a)] can deliver high output current, and reach nearly FS output swing while damping the LC resonance. Chopping was employed to minimize the components mismatch in the feedback network, ensuring good THD and PSRR. However, due to different input/output signal swings (1.8V/14.4V), LV input chopper and HV feedback chopper are employed and some ns timing skew between the choppers is present [3]. This greatly degrades the large-signal linearity as will be explained in the next section. Employing a dummy delay can alleviate the issue [3]. However, due to poor matching of HV LDMOS, the residual timing skew is still several hundred ps. To eliminate this, QCS is proposed.

Quadrature Feedback Chopping Scheme

Unlike wide-band precision chopper amplifiers such as [4], chopping in CDAs does not suffer from intermodulation distortion (IMD) between chopping and input signals as long as the chopping frequency (100kHz in this work) is much higher than the audio band (20kHz). However, to mitigate IMD between chopping and PWM, the chopping transitions in [1] were synchronized to the peak of the PWM carrier as shown in Fig. 1(b). As a result, all chopping transitions should happen while the differential output of the CDA $V_{SW\text{-}dif}$ is near zero, which occurs around the peak of the PWM carrier when a push-pull modulation scheme is applied. However, with an input signal approaching FS, the PWM duty cycle increases, decreasing the duration of $V_{SW\text{-}dif} \approx 0$. The delayed feedback HV chopper would then switch after $V_{SW\text{-}dif}$ becomes high, introducing a large error to the virtual ground current $I_{vir,dif}$ and thus significantly decreasing large-signal linearity. This issue becomes even more severe with high PWM frequency. Moreover, a PWM ripple voltage is superimposed on the audio signal at the loop filter output ($V_{LF,dif}$), shifting the center of the PWM pulse before the peak of the PWM carrier, further aggravating the issue. It is worth mentioning that the rising edge of $V_{SW\text{-}dif}$ will always occur after the peak of the PWM carrier since the slope of the ripple voltage must be smaller than that of the PWM carrier to guarantee a stable system [5].

Inspired by [4], a QCS using two identical HV feedback paths is proposed to accurately align the HV and LV chopper transitions to the peak of the PWM carrier. The two HV feedback paths are chopped at f_{CH} but with quadrature phase shift as shown in Fig. 2(a). Multiplexing switches ($S_{1/2,A/B}$) at the integrator's virtual ground are driven by a clock synchronized to $2f_{CH}$. During Φ_1, R_{FB1}s are connected to the virtual ground while R_{FB2}s are connected to the virtual ground CM voltage V_{CM} (1.1V) through $S_{2,C/D,}$ and a voltage buffer, and vice versa. Since $S_{1/2,A/B}$ are implemented with small-sized 1.8V devices, HV chopper transitions are always lagging. Therefore the switching behavior seen at the virtual ground is only governed by $S_{1/2,A/B}$. Moreover, the current spikes due to HV chopper switching are made invisible to the virtual ground since the corresponding feedback path is connected to V_{CM} when the spikes occur, and then has a quarter cycle to settle before it reconnects to the virtual ground. In the presence of large input signals, the virtual ground current is thus ideally error-free. $S_{1/2,A/B/C/D,}$ and the input choppers are bootstrapped for adequate linearity and small sizes for minimum timing delay and switching artifacts.

Measurement Results

The prototype is designed in a 180nm BCD process and occupies an active area of 7.1mm^2 (Fig. 3). Compared to SCS, QCS increases the area by only ~3% due to one extra HV chopper. The chip is powered from 14.4V/1.8V supplies (P_{VDD}/A_{VDD}) and is loaded by a 4μF capacitor in series with a 1.1μH inductor. During idle operation, the amplifier consumes 8.7mA from P_{VDD} and 5mA from A_{VDD}. Fig. 4 shows the peak THD+N with 1kHz/6kHz inputs. Compared to the case with SCS, enabling QCS has improved the large-signal THD+N by 29dB, decreasing from -50.8dB to -79.8dB at 90% FS. Moreover, the output voltage swing achieving -60dB THD+N has been extended from 86.9% to 99.5% FS. Beyond FS, signal clipping dominates nonlinearity. Fig. 5 shows the measured HD2/HD3 of a small output signal (0.25V_{RMS}) have also been improved by 6.8dB and 3.7dB respectively. Fig. 6 shows the PSRR of the amplifier. Table I summarizes the performance of the proposed driver. At 90% FS, this work achieves at least 23.6dB better THD+N compared to other resistorless drivers, and 15.4dB better THD+N compared to the rest while driving a much higher capacitive load. It also achieves the highest output swing (99.5% FS) @ -60dB THD+N, the best PSRR @ 217Hz, the lowest output noise, competitive output peak current and peak THD+N for both 1kHz and 6kHz signals.

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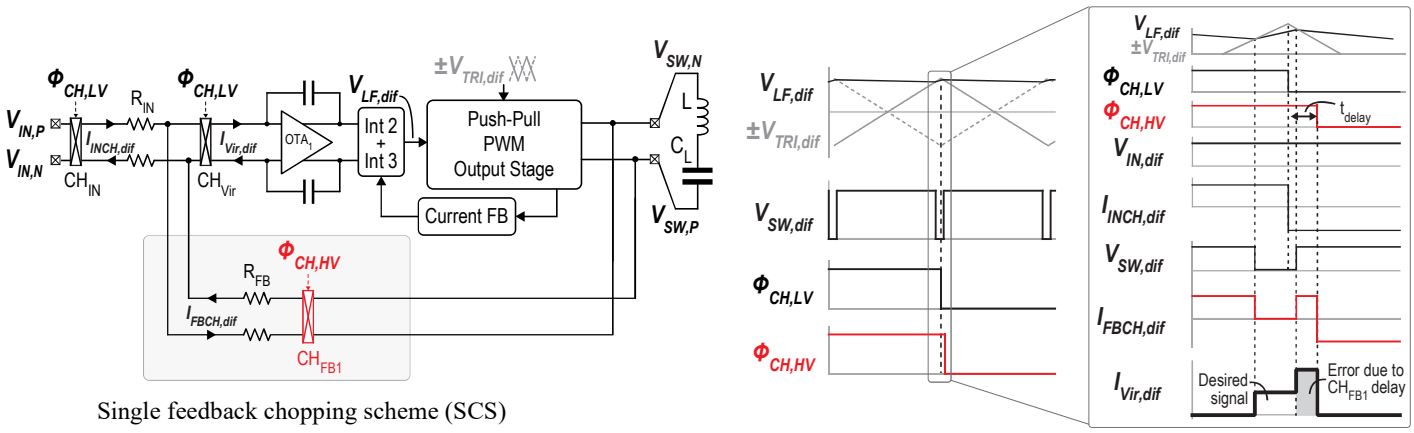
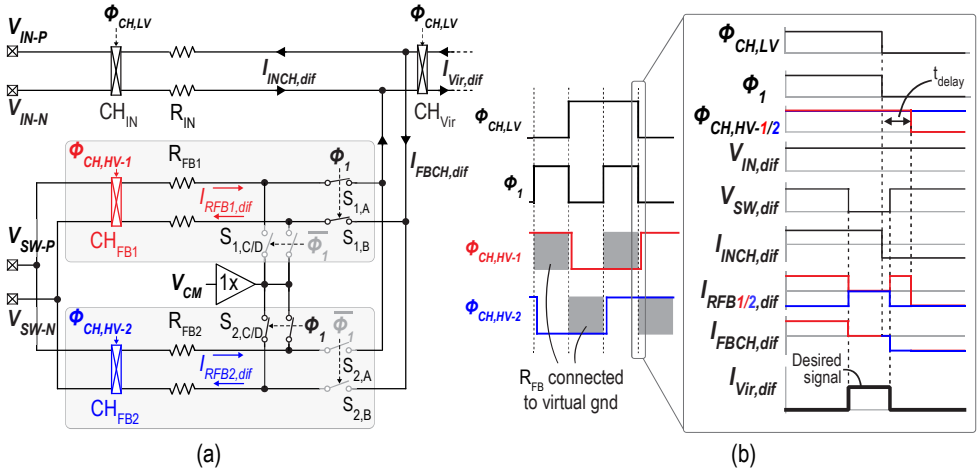


Single feedback chopping scheme (SCS)

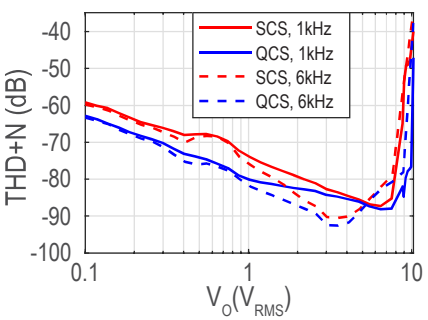
(a) (b)

Fig. 1. (a) Prior-art piezoelectric speaker driver with single feedback chopping scheme (SCS) [1], and (b) its timing diagram.

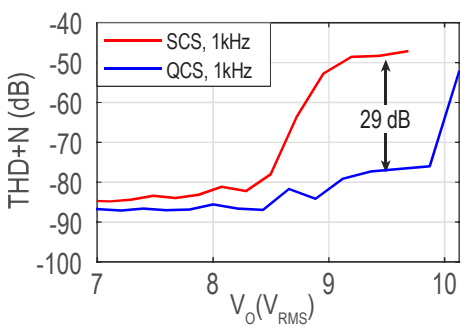


(a) (b)

Fig. 2. (a) Proposed quadrature feedback chopping scheme (QCS), and (b) its timing diagram.



(a)



(b)

Fig. 4. (a) Measured THD+N vs. output voltage in RMS, and (b) large-signal THD+N zoom-in.

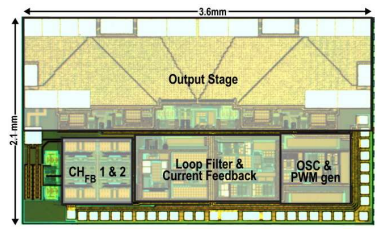


Fig. 3. Die micrograph.

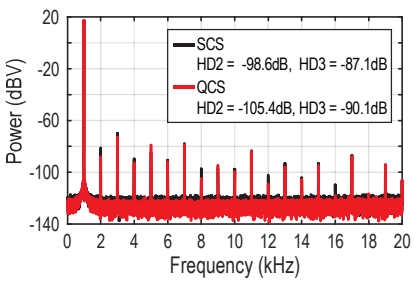


Fig. 5. Output spectra w/i and w/o QCS.

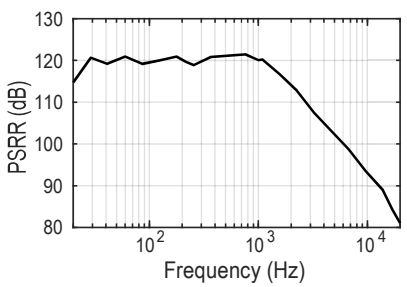


Fig. 6. Measured PSRR.

Table I. Performance summary and comparison.

	This Work	[1]	[6]	[2]	[7]	[8]
PVDD (V)	14.4	14.4	24	10 (Boosted)	10 (Boosted)	15 (Boosted)
Piezo Load (μF)	4	4	4	1	1	1.5
Damping Resistor	No	No	No	Yes (5-20Ω)	Yes (10Ω)	Yes (10Ω)
Peak Output Current (A)	4.4	4.4	4.9*	0.66*	0.7*	0.49*
Peak THD+N (dB) (fin = 1k)	-88.2	-87.3	-77.6*	-65*	-94*	-66*
Peak THD+N (dB) (fin > 1k)	-92.5 (6kHz)	-91.1 (6kHz)	-76* (5kHz)	-58.1* (5kHz)	-73.6* (10kHz)	-44.4* (5kHz)
THD+N (dB) @ 90%FS (fin = 1k)	**-79.8**	-50.9*	-56.2*	-64.4*	-63.1*	-46.0*
Output Swing / FS @ -60dB THD (fin = 1k)	**99.5%**	86.9%*	84.9%*	95.9%*	94%*	80%*
Dynamic Range (dB) [A-wt.]	108.9	106.5	111	-	106	-
Output Noise (μVrms) [A-wt.]	37	45	45	120	-	134
I_Q (mA)	8.7	8.5	10.9	4	8	4
PSRR (dB) (Frequency)	119/80 (217Hz / 20kHz)	93* / 68 (217Hz / 20kHz)	72 (1kHz)	100* / 80* (217Hz / 20kHz)	77* / 58* (217Hz / 20kHz)	79* / 50* (217Hz / 20kHz)

*Estimated from plots