Warpage Optimization for SiC MOSFET Multichip Fan-Out Panel-Level Packaging With Thermal–Mechanical Finite-Difference Numerical Modeling and In Situ Digital Image Correlation Validation

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***Abstract*—Fan-out panel-level package has become a trend in silicon carbide MOSFET packaging due to its superior electrothermal performance and cost-effectiveness. However, the increased size of multichip embedded fan-out panel-level packaging (FOPLP) introduces greater challenges in sample preparation and thermal–mechanical stresses. In this article, a large-sized (20 mm∗20 mm∗0.78 mm) FOPLP with four SiC MOSFETs embedded is investigated. A 3-D thermal–mechanical numerical model is derived based on heat conduction and elasticity theories. It utilized analytical solutions of Fourier temperature conduction and finite-difference results for thermoelastic models to describe the temperature and deformation distribution during the FOPLP operation. It also reveals the heat-coupling issue of multiple chips. Compared with the finite-element simulation, the proposed method shows less than 2.5% error in temperature and 2.3% error in deformation. The computational speed is one-tenth that of the finite-element method, while the memory usage is reduced to one-fifth. To mitigate the influence of chip thermal coupling on temperature and warpage, an optimized layout was employed to achieve temperature uniformity improvement. Finally, FOPLPs with the two layouts were fabricated. The warpage was monitored using a digital image correlation platform. To achieve the same temperature, the current required for the optimized layout was increased by 9% . The warpage of the optimized layout at 60 °C was reduced by 13.5%, and at 100 °C, it was reduced by 14.7%, validating the accuracy of the model and the significance of thermal decoupling.**

***Index Terms*—Fan-out panel-level packaging (FOPLP), numerical modeling, silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET), thermal coupling, thermo-mechanical, warpage.**

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I. Introduction

THE advent of silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) has revolutionized the power electronics industry due to their superior electrical and thermal performance. Therefore, SiC power modules are widely used in electric vehicles, photovoltaic inverters, rail transportation, and industrial power supplies [1], [2]. To meet the requirements of different applications, the packages of SiC power modules are continuously optimized to enhance thermal performance, reduce parasitic inductance, and improve power density. The mainstream SiC power module packages and their parasitic inductance parameters are summarized in Fig. 1. In traditional packaging, the wire bonding leads to parasitic inductance exceeding 10 nH across packages of various sizes [3], [4], [5]. Under high switching speeds, SiC devices face challenges with voltage overshoot. Therefore, to fully exploit the potential of SiC devices for operation at higher voltage levels and faster switching frequencies, the development of low-inductance and low-thermal resistance packaging has become a critical issue to be addressed [8]. Compared with the conventional aluminum wire bonding, ribbon bonding [9] and Cu clip [10]—owing to their greater width and reduced thickness—are more effective at minimizing loop inductance [11], [12]. To further suppress

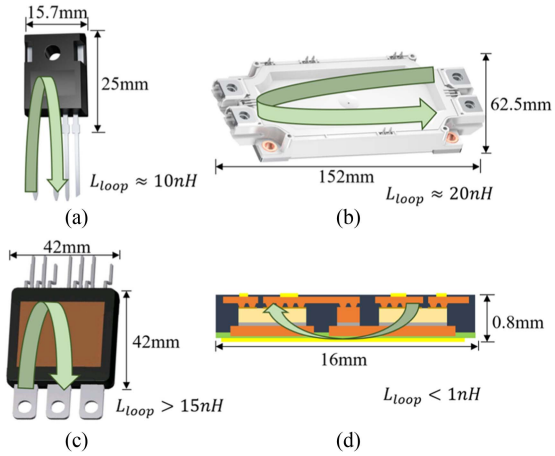


Fig. 1. Commercial SiC power modules and the parasitic inductance value. (a) TO247-4 [3]. (b) Econodual [4]. (c) Double-side cooled module [5]. (d) Fan-out package [6], [7].

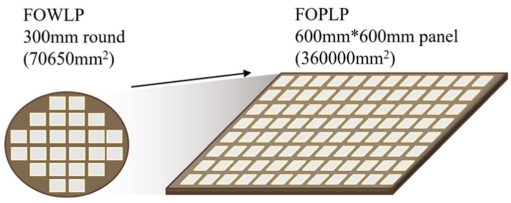


Fig. 2. Output efficiency of FOWLP and FOPLP.

the parasitic inductance, both academia and industry have proposed novel alternatives. For example, Liang [13] implemented a dual-sided DBC solution, achieving a parasitic inductance of approximately 12.8 nH. Zhang et al. [14] introduced a multistacked DBC structure that employs mutual-inductance cancelation alongside electromagnetic shielding, reducing loop inductance to 4.5 nH. Interleaved packaging, based on electromagnetic cancelation principles, has lowered the inductance of a 1200 V half-bridge SiC power module to 3.8 nH [15], [16]. In addition, Virginia Tech and Huazhong University of Science and Technology independently demonstrated hybrid packaging methods that achieve the parasitic inductances of 3.6 nH and 3.38 nH, respectively [17], [18]. These advances now approach the physical limits of conventional power modules. More recently, Infineon Technologies and Schweizer Electronic reported an embedded-package architecture using redistribution layers (RDLs) for top-side interconnects, realizing a loop inductance of 1.69 nH [19], [20]. Hou et al. [21] further achieved an embedded half-bridge SiC power module via fan-out packaging (FOP), with parasitic inductance below 2.1 nH.

Among various packaging solutions, the FOP has emerged as a trendsetting approach for SiC MOSFETs [6], primarily attributed to its low parasitic inductance [7]. Fan-out wafer-level packaging (FOWLP) size is limited by the wafer size. In addition, the circular wafer layout results in low utilization of edge chips, leading to significant material waste. By adopting fan-out panel-level packaging (FOPLP), as shown in Fig. 2, the panel size is larger, allowing more chips to be packaged on the same carrier, reducing edge losses. More packages can be produced in a single manufacturing cycle, which would increase the production capacity. In addition, FOPLP has better scalability compared with FOWLP, supporting larger package and accommodating more advanced and complex packaging requirements, such as 2.5-D/3-D packaging and chiplet packaging. Meanwhile, the FOPLP process shares similarities with printed circuit boards (PCBs) manufacturing workflows, including steps, such as component placement, lamination, and etching. Compared with the traditional packaging, FOPLP eliminates wire bonding and silica-gel encapsulation. It replaces the conventional cavity molding with a panel-level lamination molding process, allowing simultaneous embedding of all dies across the panel. By collaborating with PCB manufacturers, FOPLP production can be efficiently scaled while enabling seamless integration of external circuit designs. Therefore, FOPLP is more suitable for the future development of high integration, low power consumption, and high-performance chips.

However, the demands for higher power densities and miniaturization have also led to increasing thermal stress and mechanical strain challenges. As for large-sized FOPLP, the thermal and mechanical stresses can introduce substantial risks of failure for both the integrated chips and the packaging structure. Therefore, rigorous thermal and mechanical assessment and design of these devices are of paramount importance. In addressing the complex thermomechanical challenges, various methods for analyzing temperature and stress distributions have been developed, as summarized in Table I. These include the following.

Analytical Methods—Approaches, such as the Fourier equation method and transfer-matrix method, provide precise solutions for problems with well-defined boundary conditions [22], [23]. However, the derivation process for analytical solutions is highly complex, requiring the coupling of all thermoelastic theory equations with Fourier decomposition. Moreover, both the derivation and results are uniquely dependent on boundary conditions. Altering boundary conditions necessitates rederiving the formulae, making the process time-consuming and limiting practical applications of analytical methods.

Numerical Solutions—Finite-difference method (FDM) and finite-element method (FEM) allow for greater flexibility in handling complex geometries and boundary conditions [24], [25]. FEM allows for irregular mesh generation, which makes it well suited for modeling complex geometries. However, numerical integration in FEM leads to high computational cost and time complexity. In contrast, FDM requires fewer computational resources for linear problem solving compared with FEM while still being capable of addressing complex problems.

Previous studies have numerically analyzed the thermal–mechanical behavior of various models, including square structures, beam structures, prismatic bars, and more complex geometries [34], [35]. To improve both accuracy and feasibility, several methods, such as the generalized finite-difference method (GFDM) [36] and meshless FDM, have been proposed [37]. Although these approaches can achieve high accuracy, they are often computationally intensive when dealing with irregular boundaries [24]. Moreover, most of these studies focus on the mechanical behavior of single-material structures, which limits

TABLE I
NUMERICAL MECHANICAL MODEL METHODS

Numerical Method	Applicable Problem	Application Scenario	Key Features	Advantages and disadvantages	References
Transfer-Matrix Method	2-D laminated beam structures	Stress and temperature distribution in multi-span beams	Determines boundary conditions via Fourier expansion	High accuracy, but complex for intricate boundary conditions	[26], [27], [28]
Double Laplace Transform	Thermal-mechanical coupled models	Dynamic analysis under combined thermal and mechanical loads	Uses Durbin's technique for accurate time-domain inversion	Accurate in the time domain, but computationally complex	[29]
Ritz Method	Axially functionally graded cantilever beams	Dynamic analysis under sinusoidal loading	Combined with Newmark average acceleration method	High accuracy in dynamic analysis, but resource-intensive	[30]
FEM	Complex thermal-mechanical coupling problems	Precise solutions under complex geometries and boundaries	Highly flexible, adaptable to diverse boundary conditions	High computational cost and time complexity	[31], [32], [33]
FDM	Heat conduction and stress distribution	Suitable for regular geometries with simple boundary conditions	Simple and effective for solving heat conduction and mechanical issues	Accuracy dependent on mesh quality; ideal for regular structures	[24], [25]
GFDM	Elastic–plastic torsion problems	Localized analysis for complex cross-sectional structures	Node-based calculations, ideal for complex geometries	High accuracy but computationally demanding for irregular boundaries	[34], [35]

their applicability to heterogeneous integration in advanced packaging.

Given these limitations, it is necessary to develop a fast thermal–mechanical evaluation method for advanced packaging technologies, especially FOPLP. In addition, as power density increases, the demand for dual-sided cooling becomes more critical. In this article, a dual-sided cooling thermomechanical coupling model based on FDM is first proposed, specifically designed for multichip FOPLP structures.

The rest of this article is organized as follows. Section II provides a detailed description of the thermal and mechanical modeling methodology. Section III discussed the result of applying the proposed model on FOPLP with fabrication process and optimized layout. Section IV presents the experimental validation of the model and the optimization outcomes. Finally, Section V concludes this article with a summary of the findings and potential directions for future research.

II. MECHANISM OF THERMOMECHANICAL NUMERICAL MODEL

A. Analytical Modeling of Thermal Conduction

For FOPLP structures, the packaging process typically involves stacking entire layers of materials [22]. Therefore, it can be simplified into a rectangular structure composed of multiple stacked materials, as shown in Fig. 3. The orange squares are the heating surfaces of the chips. This plane is selected as the axis origin plane in the thermal conduction calculations. The Fourier heat conduction equation for a 3-D structure is

$$\nabla^2 T(x,y,z) = \frac{\partial^2 T(x,y,z)}{\partial x^2} + \frac{\partial^2 T(x,y,z)}{\partial y^2} + \frac{\partial^2 T(x,y,z)}{\partial z^2} = 0 \quad (1)$$

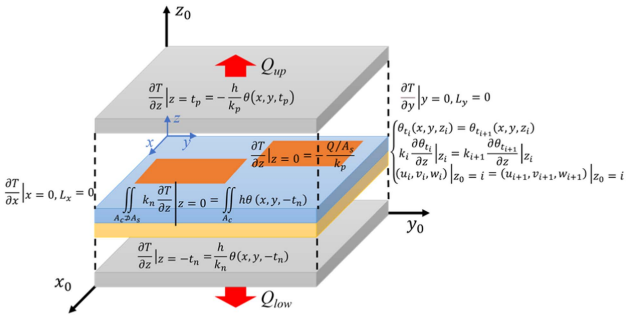


Fig. 3. Schematic of the thermomechanical model of the FOPLP structure.

$T(x,y,z)$ is the temperature of spot (x,y,z). The general solution is typically expressed as $\theta(x,y,z)$, where $\theta(x,y,z) = T(x,y,z) - T_{\text{air}}$. T_{air} is the ambient temperature,

$$\begin{aligned}\theta(x,y,z) = A_0 + B_0 z + \sum_{m=1}^{\infty} \cos(\lambda x)\left[A_1 \cosh(\lambda z) + B_1 \sinh(\lambda z)\right] \\ + \sum_{n=1}^{\infty} \cos(\delta y)\left[A_2 \cosh(\delta z) + B_2 \sinh(\delta z)\right] \\ + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} \cos(\lambda x)\cos(\delta y)\left[A_3 \cosh(\beta z) + B_3 \sinh(\beta z)\right] \quad (2)\end{aligned}$$

where $\lambda = m\pi/L_x$, $m = 1,2,3,\cdots$, $\delta = n\pi/L_y$, $n = 1,2,3,\cdots$, $\beta = \sqrt{\lambda^2+\delta^2}$, and $B_i = \phi(\xi)A_i$, $i = 1,2,3$. The length of the package is L_x. The width of the package

is L_y. Given that the FOPLP packaging thickness is substantially less than the cross-sectional length, the convective heat transfer from the sidewalls to the external environment can be neglected. Consequently, heat dissipation to the environment occurs primarily through the top and bottom surfaces. At the interfaces between different layers, temperature and heat flux are maintained in a continuous state. The coefficients of each parameter are interrelated. It depends on the thermal power output by the chips, the thermal conductivity of the constituent materials, and the thickness of each structural component. Fig. 3 also provides a comprehensive framework for the boundary conditions with their corresponding mathematical expressions to complete the thermal conduction model.

As for multiple heat sources, the linear temperature rise superposition leads to a composite heating effect across the system. This phenomenon enables the discrete thermal contributions of each heat source to be individually calculated and subsequently aggregated to ascertain the collective temperature profile. Assuming that there are n heat sources within the structure, the temperature distribution at various locations can be expressed as follows:

$$\begin{aligned}(x,y,z) = \theta_1\ (x,y,z) + \theta_2\,(x,y,z) \\ + \cdots + \theta_n\,(x,y,z) + T_{\text{air}}.\end{aligned} \tag{3}$$

In practical applications, the heat generation among multiple chips may vary due to several factors, such as current imbalance in parallel chip configurations, leading to nonuniform heating. Additional contributors include differences in ON-state resistance and temperature sensitivity among different chips. For a given chip i, with heat generation power Q_i and chip area A_{si}, the temperature gradient at the chip interface can be expressed as follows:

$$\left.\frac{\partial \theta_i}{\partial z}\right|_{z\ = z_{\text{chip layer}}} = -\frac{Q_i/A_{si}}{k_p}. \tag{4}$$

Thermal power must be determined based on the device's switching conditions. The losses usually arise from conduction loss, switching loss, diode conduction loss, and diode reverse recovery loss.

B. Finite-Difference Numerical Modeling of Thermoelasticity

When the temperature changes, the thermal expansion of the material affects the deformation and stress distribution within the structure. For thermoelastic mechanics, the constitutive equation can be expressed in tensor form as follows:

$$\varepsilon_{ij} = \frac{1}{2G}\left[\sigma_{ij} - \frac{\nu}{1+\nu}\sigma_{kk}\delta_{ij}\right] + \alpha\,(T - T_0) \tag{5}$$

where $i, j = 1, 2, 3$. Here, ε_{ij} represents the sum of elastic and thermal strains, G is the shear modulus, ν is Poisson's ratio, $(T - T_0)$denotes the temperature variation, α is the linear coefficient of thermal expansion, and $\delta_{ij}$is the Kronecker delta. The thermoelastic constitutive equation expressed in terms of the stress tensor is given as follows:

$$\sigma_{ij} = 2\mu\varepsilon_{ij} + \left[\lambda\varepsilon_{kk} - \alpha\,(3\lambda + 2\mu)\,(T - T_0)\right]\delta_{ij} \tag{6}$$

where $\mu = G$, and λ is the Lamé constant, defined as $\lambda = \frac{2G\nu}{1-2\nu}$.

The geometric equation in tensor form is given by

$$\varepsilon_{ij} = \frac{1}{2}\,(u_{i,j} + u_{j,i})\,. \tag{7}$$

Without considering external forces, the equilibrium equation in tensor form is expressed as follows:

$$\sigma_{ij,j} = 0. \tag{8}$$

Substituting the geometric equations (7) into the constitutive equations (6) and then into the equilibrium equations (8) yields differential expressions for the three displacement components

$$\begin{aligned}&(2G+\lambda)\frac{\partial^2 u}{\partial x^2} + G\frac{\partial^2 u}{\partial y^2} + G\frac{\partial^2 u}{\partial z^2} + (G+\lambda)\frac{\partial^2 v}{\partial x \partial y} \\ &+ (G+\lambda)\frac{\partial^2 w}{\partial x \partial z} \\ &- \alpha\,(3\lambda + 2\mu)\frac{\partial \theta}{\partial x} = 0\end{aligned} \tag{9}$$

$$\begin{aligned}&G\frac{\partial^2 v}{\partial x^2} + (2G+\lambda)\frac{\partial^2 v}{\partial y^2} + G\frac{\partial^2 v}{\partial z^2} + (G+\lambda)\frac{\partial^2 u}{\partial y \partial x} \\ &+ (G+\lambda)\frac{\partial^2 w}{\partial y \partial z} \\ &- \alpha\,(3\lambda + 2\mu)\frac{\partial \theta}{\partial y} = 0\end{aligned} \tag{10}$$

$$\begin{aligned}&G\frac{\partial^2 w}{\partial x^2} + G\frac{\partial^2 w}{\partial y^2} + (2G+\lambda)\frac{\partial^2 w}{\partial z^2} + (G+\lambda)\frac{\partial^2 u}{\partial z \partial x} \\ &+ (G+\lambda)\frac{\partial^2 v}{\partial z \partial x} \\ &- \alpha\,(3\lambda + 2\mu)\frac{\partial \theta}{\partial z} = 0.\end{aligned} \tag{11}$$

Using the FDM, the second-order derivative term can be expanded and expressed as follows:

$$\frac{\partial^2 u}{\partial x^2} = \frac{u\,(x_{i+1}, y_j, z_k) + u\,(x_{i-1}, y_j, z_k) - 2u\,(x_i, y_j, z_k)}{\Delta x^2} \tag{12}$$

$$\begin{aligned}\frac{\partial^2 v}{\partial x \partial y} = \frac{1}{4\Delta x \Delta y}\,[&v\,(x_{i+1}, y_{j+1}, z_k) + v\,(x_{i-1}, y_{j-1}, z_k) \\ &- v\,(x_{i+1}, y_{j-1}, z_k) - v\,(x_{i-1}, y_{j+1}, z_k)].\end{aligned} \tag{13}$$

The displacements at each location can be inferred from the adjacent. The transformation of a partial differential equations system into a corresponding set of difference equations results in a linear algebraic system expressed as $Ae = b$, where A represents the coefficient matrix. Therefore, when boundary conditions are determined, the warpage of the entire structure can be solved recursively. The compilation process is shown in Fig. 4.

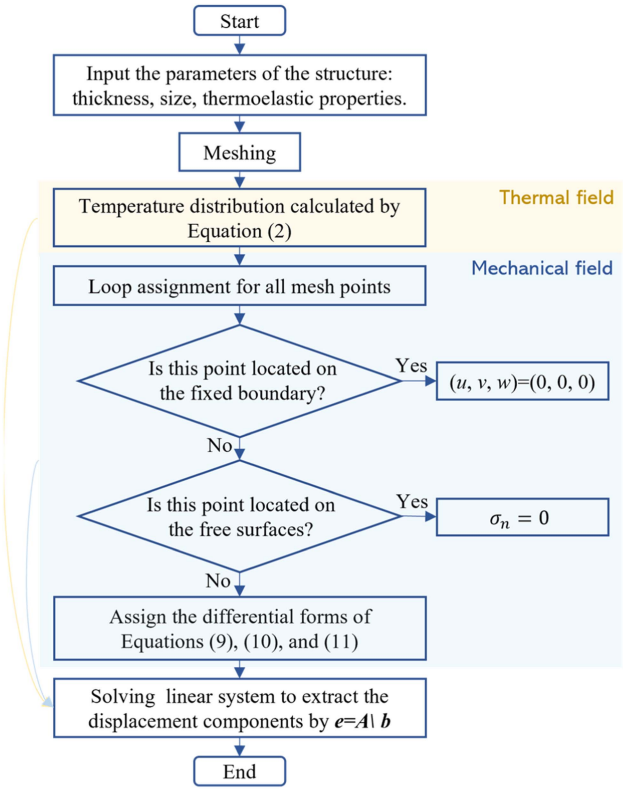


Fig. 4. Compilation flowchart of the thermoelastic model.

III. Multichip FOPLP Thermoelastic Model

A. Half-Bridge FOPLP Samples Manufacturing

To further illustrate the applicability of this method to FO-PLP, a half-bridge topology FOPLP with two parallel chips was fabricated. The multichip panel-level packaging process shares similarities with its single-chip counterpart, with the capacity to implement both face-up and face-down assembly processes. However, the intricacies warpage of half-bridge circuit topologies, coupled with the vertical construction of SiC MOSFETs, typically favor the face-down method for multichip configurations [7]. Fig. 5 illustrates the packaging process of the FOPLP samples used in this article. The process begins with attaching the chips to the carrier board. For half-bridge topology packaging, it is essential to design the current flow paths and differentiate the electrodes on the substrate. To address the disparity in height between the source and drain, copper blocks are strategically positioned on the carrier board to ensure a balanced and effective electrical interconnection.

The copper blocks, integral to the electrical interconnections, are carefully processed and reflow soldered onto the carrier board concurrently with the chips, ensuring a robust connection within the circuit topology. Following this, insulative molding materials that also offer mechanical support are laminated onto the substrate, providing a foundation for the subsequent encapsulation of the chips. Then, a full sheet of copper is laminated on the top surface for the formation of the RDL. These RDLs are crucial, as they are applied to the copper blocks to establish the necessary electrical connections within the half-bridge topology. The tight connection between the molding layer and the RDL layer is achieved through polyimide adhesive, similar to the connection between FR4 and the copper layer in the PCB board. A vacuum-assisted rapid hot press is applied with a pressure of 6 kgf/cm^2 during both epoxy molding compounds (EMC) and copper foil lamination, ensuring uniform pressure distribution across the entire panel. To enable the vertical interconnect access, blind vias are crafted on the chip and copper block surfaces through a combination of computerized numerical control engraving and laser processing. After plasma cleaning, metal needs to be deposited into the blind vias. Direct electroplating of copper can result in poor adhesion between the blind via and the chip's pad, leading to potential delamination. To ensure a robust connection between the blind via and the chip's RDL, a thin layer of titanium (Ti) and nickel (Ni) is first sputtered as an adhesive layer. Next, copper is chemically deposited onto the sidewalls of the blind vias to promote better adhesion. Finally, the blind vias are fully filled using electroplating. This step finalizes the interconnection process, ensuring a seamless electrical link between the chips and the copper blocks.

In order to achieve a specific current path, the top RDL needs to be divided into certain areas. Utilizing photolithographic etching techniques, the copper layer is intricately etched to form a predefined circuit pattern. Then, a layer of polypropylene (PP) and a heat sink are affixed to the underside of the structure to enhance thermal management and structural stability. Subsequently, a solder mask is laminated onto the top surface, providing protection and ensuring the reliability of the soldering process. On top of the solder mask, a photoresist is applied for the development of the graphic patterns to facilitate connections with external circuits. To conclude the fabrication process, the sample surface undergoes silver plating, which not only ensures excellent electrical conductivity but also contributes to the durability and antioxidant of the contact pads.

Finally, the entire panel is singulated into individual packages. In this process, a panel measuring 508 mm by 203 mm was cut to produce 40 samples. The fabrication of a 1200 V FOPLP is now complete. If sufficient chips are available and the layout of individual packages can be made more compact, a single fabrication run could yield even more samples. This would enhance efficiency and reduce the cost of panel-level packaging.

B. FOPLP Thermoelastic Performance

The cross section of the prepared FOPLP sample was examined to discern the structure and thickness of each constituent layer. Utilizing an Axioscope 5 metallographic microscope, the distinct layers were observable, as depicted in Fig. 6. The material parameters for each layer, from bottom to top, are listed in Table II . This sample contains four embedded SiC MOSFETs. The chip size is 3.74 mm by 4.13 mm, and the copper block size is 2 mm by 2 mm. The overall package measures 20 mm by 20 mm. Considering the insulation between different electrode regions and the compression of the molding compound, the spacing between different potential structures needs to be greater than 0.6 mm. The EMC employed in this fabrication has a dielectric breakdown strength of 60 kV/mm. Fig. 7 illustrates

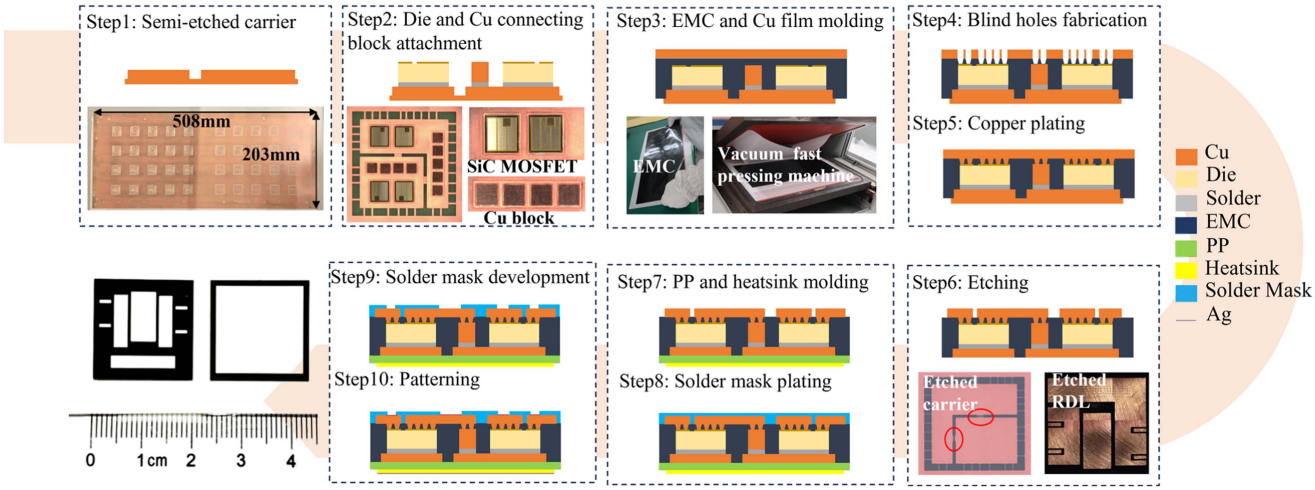


Fig. 5. Schematic diagram of the FOPLP fabrication process.

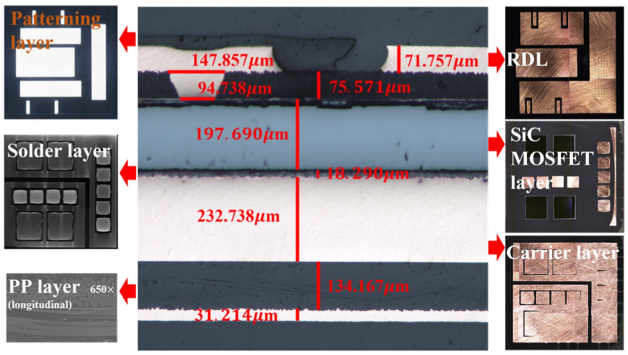


Fig. 6. Longitudinal and cross-sectional views of an FOPLP sample.

TABLE II
THICKNESS AND MATERIAL PARAMETERS OF EACH LAYER IN THE FOPLP 3-D LAMINATED STRUCTURE

Structure of each layer	Thickness	Young's modulus	Poisson's ratio	CTE	Thermal conductivity
	μm	GPa	/	ppm / K	W/(m·K)
Heatsink	31	110.00	0.34	17	400
pp	134	13	0.38	15	2.1
Carrier	232	110.00	0.34	17	400
Solder	20	49	0.38	31	70
SiC MOSFET	200	400	0.142	5.1	150
EMC	76	15	0.38	10	0.96
Blind vias	76	110.00	0.34	17	400
RDL	72	110.00	0.34	17	400
Patterning	20	83	0.38	19	429

the cross-sectional perspective of the blind via layer, where the diameter of the blind vias exceeds 170 μm. The upper surface connection consists of two materials with differing thermal conductivities. The blind vias, which have a higher thermal conductivity, occupy a smaller volume, whereas the EMC, with lower thermal conductivity, occupies a larger volume.

TABLE III
THREE-PHASE TWO-LEVEL AFE SPECIFICATIONS

Condition	Value
Input AC Voltage (V_{in})	311 V_{LL}
Output DC Voltage (V_{out})	700 V
Rated power (P_{out})	20 kW
Grid Frequency (F_{ac})	50 Hz
Switching Frequency (F_{sw})	100 kHz
Inductance (L)	1 mH

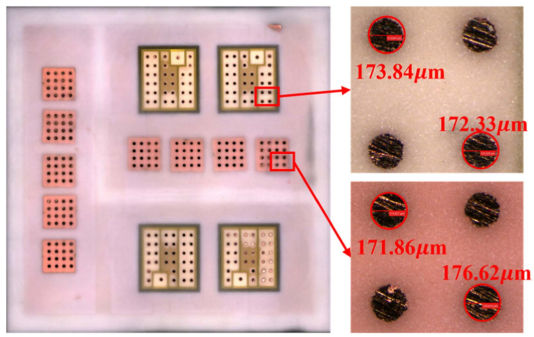


Fig. 7. Cross-sectional view of the blind via layer.

To precisely characterize the heat transfer in the upper layer of the chip, the equivalent volume method has been employed. The equivalent thermal conductivity of the chip's upper layer is determined to be 7.96 W/(m·K) by (14). This method eliminates the 2.5% error caused by direct simplification,

$$R_{\text{th.com}} = \frac{1}{\frac{1}{R_{\text{th.1}}} + \frac{1}{R_{\text{th.2}}}} = \frac{t^2}{k_1 V_1 + k_2 V_2} = \frac{t^2}{k_{\text{eq}} V_{\text{eq}}} \tag{14}$$

where subscripts 1 and 2 represent two different materials, respectively, k represents the thermal conductivity, V represents the volume, and t represents the thickness. The subscript eq represents the equivalent parameter.

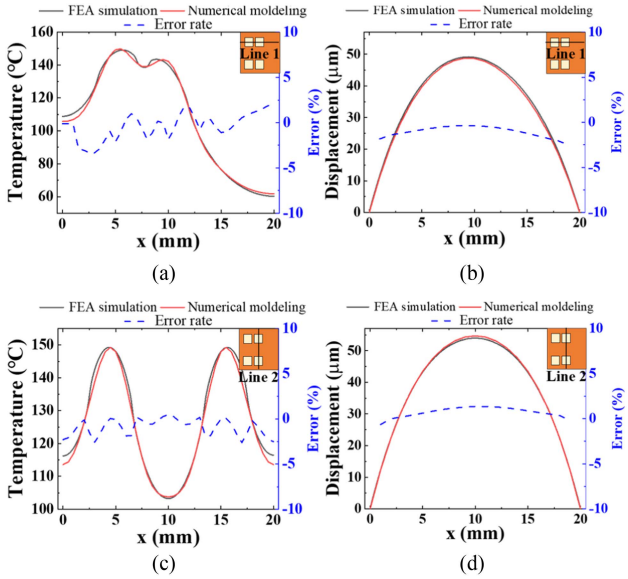


Fig. 8. Comparison of the proposed method and FEM simulation. (a) Temperature distribution along line 1. (b) Displacement distribution along line 1. (c) Temperature distribution along line 2. (d) Displacement distribution along line 2.

In order to verify the accuracy and effectiveness of the proposed model, comparisons were made with FEM simulation results in COMSOL. In an FOPLP configuration, the power terminals are located above the chips, minimizing inductance differences between paralleled current paths. The SiC MOSFETs would mitigate current imbalance at high temperatures since the ON-state resistance $R_{\mathrm{ds(on)}}$ exhibits a positive temperature coefficient from room temperature to high temperatures. Furthermore, each SiC MOSFET is assumed to be identical. The current sharing among the parallel chips is assumed to be uniform, resulting in homogeneous heat dissipation. The fabricated FOPLPs are assumed to be employed in a three–phase, two–level active front end (AFE) as shown in Table III. This topology incorporates three FOPLP modules, and the parameters are provided in Table II. Simulation results indicate a total conduction loss of 133.47 W and a total switching loss of 217.1 W. The combined loss is 350.57 W, averaging approximately 30 W per chip. The heat transfer coefficient is assumed to be 2000 W/(m^2·K) [38], [39]. The structural and material parameters of the FOPLP described above were incorporated into the proposed thermoelastic model. The four edges of the bottom surface are assumed to be fixed. Temperature and deformation were extracted along two cross-sectional lines and compared with finite element analysis (FEA) simulation results, as shown in Fig. 8. A strong agreement between the two prediction methods could be observed. The proposed model predicts a maximum junction temperature of 149.8 °C, compared with 149.1 °C obtained from FEA simulation. Moreover, the model accurately captured the thermal-coupling effect between multiple chips. Along line 1, where the chip spacing is smaller, the junction temperature was noticeably elevated due to the influence of the adjacent chip. Owing to thermal expansion, the package exhibits an overall upward–convex warpage. In addition, due to the asymmetric chip placement, the warpage peak along line 1 shifts toward the hotter side. The temperature prediction error was within 2.5%, and the warpage prediction error was less than 2.3% . In terms of computational performance, the proposed method and the FEA simulation employ 31 600 and 34 607 mesh vertices, respectively. The FEA simulation required 378 s, consuming 12.97 GB of physical memory and 18.19 GB of virtual memory. However, the proposed model completed the computation in only 37.2 s—saving 90% of the time—with a peak memory usage of 1.45 GB. It is verified that the proposed model could significantly reduce computational resource while maintaining high accuracy for advanced package thermoelastic prediction.

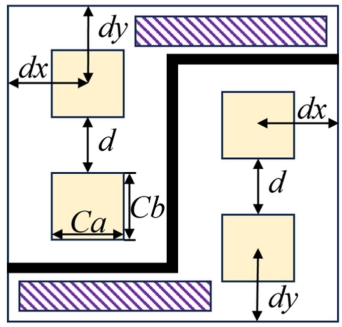


Fig. 9. Optimized symmetrical layout.

C. Layout Optimization

In the design of parallel power MOSFETs, thermal-coupling effects can cause uneven power dissipation and temperature distribution across devices. This necessitates a carefully planned chip layout to ensure optimal thermal performance. For a half-bridge topology involving four chips, it is crucial to symmetrically distribute the upper and lower arms to maintain the best thermal performance during alternating operation. This approach helps in mitigating the intense thermal accumulation that can occur due to the thermal coupling when multiple chips are working in parallel. The initial analysis used a factory-supplied packaging layout, which did not account for temperature distribution and mechanical stress. The optimized layout addresses this by symmetrically positioning the upper and lower bridge arms, which enhances thermal and mechanical balance.

Z-shaped slots, as shown in Fig. 9, are used on the carrier to achieve the symmetrical layout. This configuration allows for the precise placement of chips, which is controlled by three distinct positional parameters. With a specified slot spacing of 0.6 mm, these parameters are interrelated to ensure an optimal and balanced arrangement of the components on the carrier.

$$\begin{cases} 0.6+\frac{1}{2}Ca \le dx \le 9.1-\frac{1}{2}Ca \\ d \ge 0.6 \\ 0.6+\frac{1}{2}Cb \le dy \le 15.6-\frac{3}{2}Cb \\ dy+d \le 16.2-\frac{3}{2}Cb. \end{cases} \tag{15}$$

The multiobjective optimization based on the proposed thermoelastic numerical model is used to propose an optimized layout. The criteria for assessment were the maximum junction temperature among the four chips ($T_{j.\max}$), temperature variance

TABLE IV
CALCULATED JUNCTION TEMPERATURES AND DISPLACEMENTS FOR DIFFERENT DESIGN PARAMETERS

(*dx*, *dy*, *d*)	$T_{j.max}$ (°C)	σ^2	Warpage (μm)	Score
(2.5 mm, 2.8 mm, 5 mm)	162.8	193	41	150.5
(3.5 mm, 5 mm, 2.5 mm)	149.8	23.5	44	78.1
(4 mm, 4.8 mm, 1.5 mm)	153.9	39.7	45.15	86.2
(6 mm, 6 mm, 3 mm)	136.8	0.01	49.6	64.6
(5 mm, 4.8 mm, 3.5 mm)	138.5	2.3	47.2	65.8
(5 mm, 5.5 mm, 3.5 mm)	136.2	1.3	46.85	64.3

(σ^2), and the z-direction displacement at the top surface. The temperature variance is calculated as follows:

$$\sigma^2 = \frac{1}{n}\sum_{i=1}^{n}\left(T_i - \bar{T}\right)^2 \tag{16}$$

where T_i represents the junction temperature of each chip, and $\bar{T}$ is the average junction temperature of the four chips. This metric quantifies the thermal uniformity across multiple chips. Junction temperature directly influences the electrical performance of the chips and limits the maximum current-carrying capacity of the device, making it a primary cause of thermal failure. Meanwhile, warpage compromises mechanical reliability and is a leading factor in mechanical failure. Therefore, to ensure both short-term safety and long-term reliability, equal weight ($w_1 = w_2 = 0.4$) is assigned to $T_{j.\max}$ and warpage in the optimization process. The temperature uniformity among different chips, while considered secondary, remains an important factor and is, thus, assigned a moderate weight ($w_3 = 0.2$). The solutions based on the proposed method are searched using a large step size, then gradually reduce the step size within that region to determine the optimal position. Due to differences in magnitude, the warpage value is amplified by a factor of 10^6, denoted as $W_{\max}$, to normalize the contribution. The performance of each design is evaluated using a weighted score defined as follows:

$$\text{Score} = w_1 \cdot T_{j.\max} + w_2 \cdot \sigma^2 + w_3 \cdot W_{\max} \tag{17}$$

where a lower score indicates a more favorable layout. Table IV summarizes the results for various design configurations along with their corresponding scores. All programming and compilation processes were executed within MATLAB, ensuring the integration of numerical simulations and data analysis. This optimization using the proposed model required only half an hour, whereas the equivalent optimization via FEA simulation would take 5 h. This significant reduction in computation time further attests to the superiority of the proposed thermoelastic model. The optimal layout position parameters obtained through calculations were (*dx*, *dy*, *d*) = (5 mm, 5.5 mm, 3.5 mm).

D. Evaluation of Optimization Improvements

Consistent with the assumptions used in the previous simulations, the thermal dissipation per chip is 30 W. The heat dissipation coefficient is 2000 W/(m^2·K). To evaluate the thermal performance of the FOPLP structure under different operating

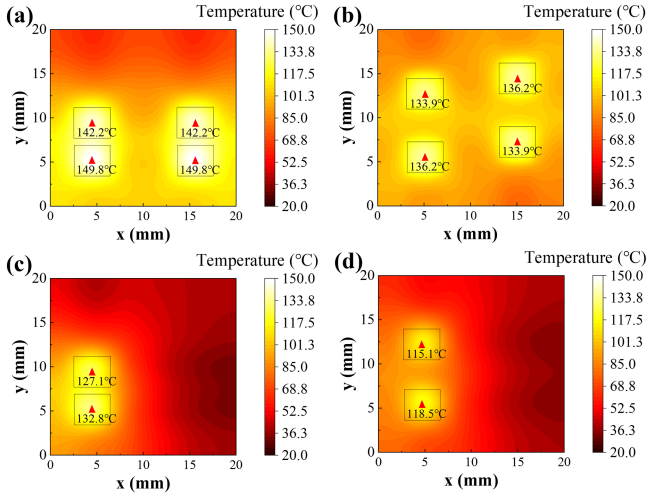


Fig. 10. Proposed thermoelastic model results of the temperature distribution on the chip layer of (a) before and (b) after optimization with four chips heating and (c) before and (d) after optimization with two chips heating.

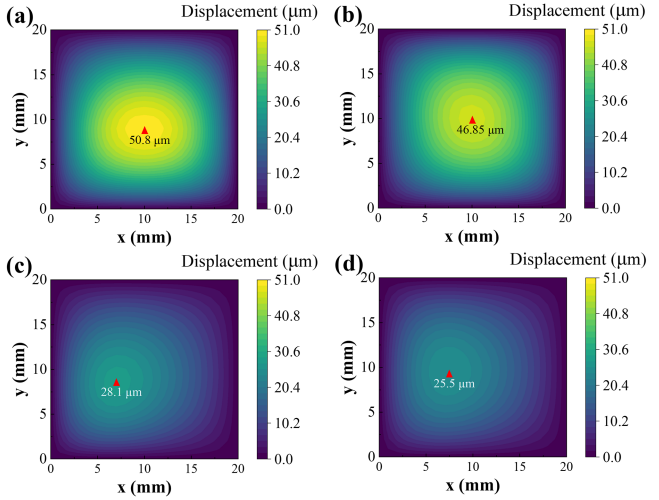
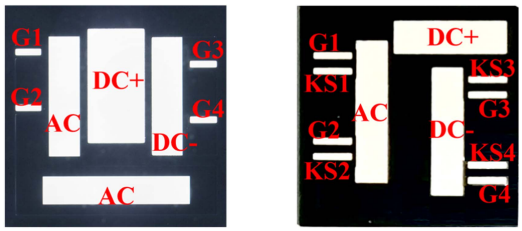


Fig. 11. Proposed thermoelastic model results of the deformation distribution of (a) before and (b) after optimization with four chips heating and (c) before and (d) after optimization with two chips heating.

conditions, two representative scenarios are simulated: First, simultaneous heating of all four chips in the full half-bridge module, and second, heating of two parallel chips in a single half-bridge leg. The four-chip heating case is presented in Fig. 10(a) and (b). The junction temperatures of the original layout are 149.8, 149.8, 142.2, and 142.2 °C, with a corresponding variance $\sigma_{\text{before}}{}^2$ of 14.4. The average heatsink surface temperature is 89.18 °C, yielding a calculated thermal resistance of 0.51 K/W. After layout optimization, the junction temperatures were reduced to 136.2, 136.2, 133.9, and 133.9 °C, with a variance $\sigma_{\text{after}}{}^2$ of 1.3 and a reduced thermal resistance of 0.41 K/W. The lower temperature variance after optimization clearly indicates the improved thermal uniformity. To account for application scenarios in which only a half-bridge leg operates, the temperature distributions with two parallel chips heating are presented in Fig. 10(c) and (d). In this case, the average heatsink surface



(a) (b)

Fig. 12. Package outline drawing of the (a) original FOPLP and the (b) optimized FOPLP.

temperatures are 54.6 °C and 54.5 °C, while the maximum junction temperatures are 132.77 °C and 118.5 °C, respectively. The resulting thermal resistances are 1.3 and 1.07 K/W. This demonstrates the importance of reducing thermal coupling in small-size layouts to decrease thermal resistance.

The calculated distributions of deformation in the z-direction on the top surface are depicted in Fig. 11. The boundary condition is that all four edges of the bottom surface are fixed. The warpage decreased 3.95 μm by the optimization when four chips were heating and 2.6 μm when two chips were heating. In the optimized layout, the thermal coupling is mitigated due to the increased spacing between chips. The optimized chip layout not only reduced the maximum junction temperature but also enhanced thermal uniformity among multiple chips and minimized warpage. The improved thermomechanical performance of the FOPLP provides a strong foundation for ensuring its long-term reliability.

IV. Experiments

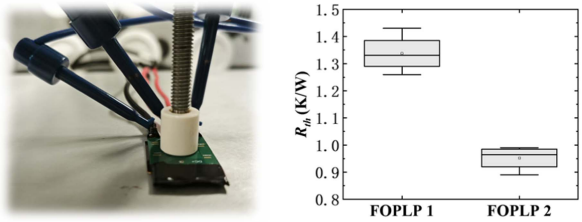
A. FOPLP Fabrication Validation

In order to minimize the influence of systemic errors, the chips for the two layouts were sourced from an identical wafer. The fabrication process for both layouts was carried out on a single panel, thereby ensuring uniformity in the encapsulation process and the associated process parameters. The package outline drawings of both layouts are shown in Fig. 12. $G1$ and $G2$ correspond to the gate terminals of the two paralleled chips in the upper bridge arm, while $G3$ and $G4$ correspond to the two paralleled chips in the lower bridge arm. The gate terminals require external circuitry for parallel connection. A preliminary assessment of the static parameters of the samples was undertaken to detect potential damage incurred during encapsulation and to confirm the parallel configuration of the chips. The Keysight B1505 platform was utilized for the static tests. As the FOPLP does not conform to commercial standard packaging, the design of a custom test adapter was essential to facilitate the connection between the package's electrode pads and the test platform's ports.

The static characteristics experimental results are delineated in Table V, demonstrating that all parameters are well within the acceptable limits. $F1$ and $F2$ represent the sample with the pre- and postoptimization, respectively. The footprints up and low represent the up bridge and the low bridge of the FOPLPs. The $R_{\mathrm{DS(on)}}$ of the bare die is 46.5 mΩ, indicating that

TABLE V
Static Characteristics Test Results of the FOPLP

	Test Conditions	Unit	$F1_{up}$	$F1_{low}$	$F2_{up}$	$F2_{low}$
$V_{(br)DSS}$	V_{GS}=0V, I_D=100μA.	V	1616	1619	1600	1654
I_{DSS}	V_{DS}=1.2kV, V_{GS}=0 V.	A	18.7	18.5	18.3	18.4
$V_{GS(th)}$	I_D=10 mA.	V	2.62	2.66	2.58	2.64
$R_{DS(on)}$	V_{GS}=15V, I_D=33.3A.	mΩ	27.27	28.83	26.66	27.34
C_{iss}	V_{GS}=0V, V_{DS}=1kV, f=100 kHz.	nF	3.66	3.77	3.60	3.68
C_{oss}		nF	0.25	0.23	0.25	0.23
C_{rss}		pF	17	17.3	16.5	16.9



(a) (b)

Fig. 13. Thermal resistance tests. (a) Setup. (b) Results.

the packaging-induced resistance is approximately 4 mΩ. This additional resistance likely arises from the vertical interconnect stack between the SiC die and the top-side RDL, which may introduce contact resistance at the interfaces. The static test results from the samples show that the packaging process can ensure the normal operation of the chips. This validates the feasibility of the panel-level packaging process and the proposed structural design.

The thermal resistance of the FOPLP samples was measured using the dual-interface method. The heat sink surface is attached to the water-cooling plate. The test equipment is the Siemens Mentor T3Ster system. Each test channel provides only one power path and one sensing path. Due to these hardware constraints, it is not feasible to simultaneously energize both half-bridge legs during measurement. Only one half-bridge leg was conducting current and generating heat during the tests. Four samples each of the preoptimization (FOPLP 1) and postoptimization (FOPLP 2) layouts were evaluated, with the test setup and results, as shown in Fig. 13. The optimized chip placement successfully reduced the packaging thermal resistance from 1.34 to 0.95 K/W. This trend is consistent with the temperature prediction results of the proposed model, both showing that the optimized layout has a lower junction temperature under the same thermal power.

B. Warpage Comparison

This study aims to monitor the thermal and deformation responses of the FOPLPs during operation by concurrently measuring two critical parameters: case temperature (T_c) and the deformation at the top surface. To induce self-heating, the FOPLPs are subjected to an energized state through an external circuit that supplies a constant current. T_c is ascertained using an

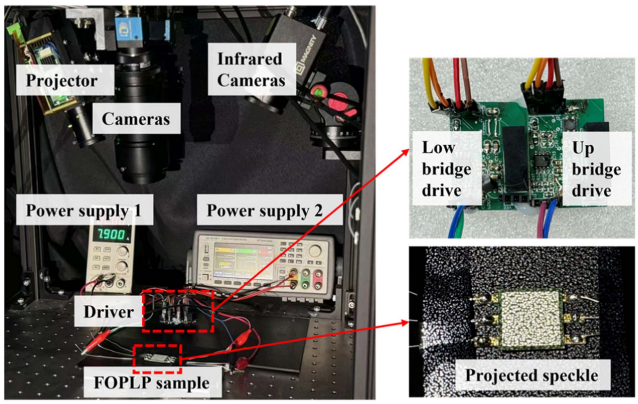


Fig. 14. Thermoelastic DIC platform setup.

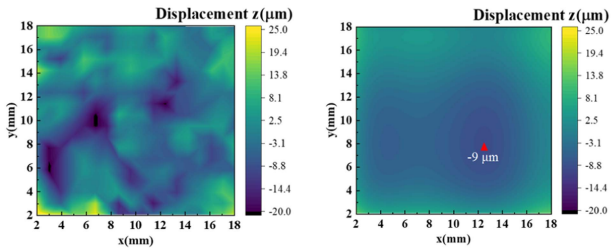


Fig. 15. Warpage of the original FOPLP at ambient temperature. (a) Raw data. (b) After fitting.

infrared thermal tester, which provides a synchronized thermal profile. To assess warpage, the FOPLP is positioned on a digital image correlation (DIC) platform [40], as shown in Fig. 14. The measurement principle involves using dual cameras to capture the speckle pattern projected onto the surface of the sample. One camera serves as a reference, while the other captures the surface morphology [41].

Samples that performed well in static tests were selected for thermoelastic testing. Power supply 2 provides a 15-V signal to the upper and lower bridges of the sample. The current from power supply 1 flows through dc+ and dc−, heating the device via its ON-resistance. Since the heat-dissipating surface must remain unobstructed as it is the measured surface during warpage monitoring, the device cannot be mounted on a heat sink for such measurements. Moreover, the bottom of the device needs to be electrically insulated from the testing system, which further eliminates any heat dissipation capabilities. In this scenario, neither the top nor the bottom surface of the device under test has an auxiliary cooling system, meaning that the heat dissipation conditions for both surfaces can be considered identical. The steady-state T_c of the original sample can reach 60 °C and 100 °C at currents of 5.5 A and 7.2 A, respectively. The initial morphology of the FOPLP captured at an ambient temperature of 20 °C is shown in Fig. 15(a). The morphology after applying polynomial curve fitting to remove noise is displayed in Fig. 15(b). However, in the thermomechanical theoretical modeling of the laminated structure, the device surface at ambient temperature is assumed to be an ideal plane. To better compare the warpage during the heating experiment, the postheating warpage was described in

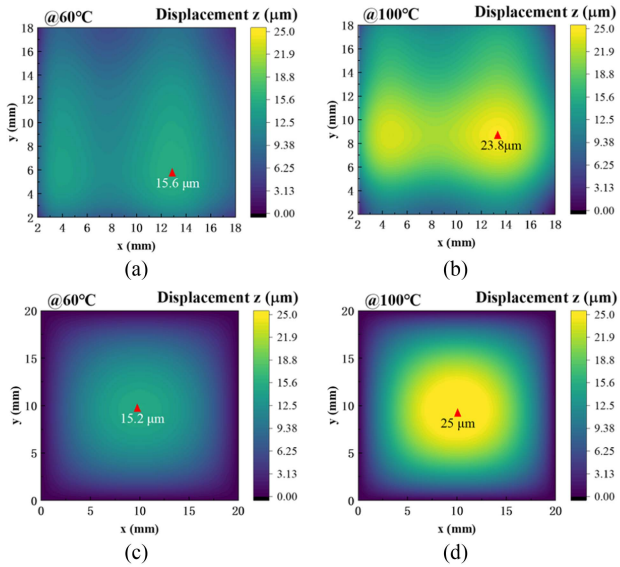


Fig. 16. DIC test results of the relative warpage generated by the original FOPLP self-heating at (a) 60 °C and (b) 100 °C. The displacement predicted by the proposed method at (c) 60 °C and (d) 100 °C.

relative terms, subtracting the morphological characteristics of the sample surface at the initial temperature.

Fig. 16 presents the relative warpage test results and thermoelastic prediction results of the original FOPLP with T_c of 60 and 100 °C. This prediction considers the PCB adapter used in the actual measurement. Attaching the device to the PCB can help mitigate warpage caused by thermal expansion. The surface warpage exhibits an overall upward curvature, with increased warpage observed above the chips. In the thermomechanical model, the air convection coefficient is set to 30 W/(m^2·K). The power dissipation of each chip is 0.25 and 0.58 W based on the calculation of the input current. Under these circumstances, the warpage test results at 100 °C exceed those at 60 °C by 52.7% . In addition, the numerical warpage results exhibit strong agreement with the experimental measurements, thereby confirming the accuracy of the proposed model.

Then, the optimized FOPLP was tested under the equivalent conditions. Due to the mitigation of thermal coupling, the optimized sample required a higher current to reach the same temperatures. When the steady-state T_c reached 60 °C and 100 °C, the currents were 5.9 A and 7.9 A, respectively, reflecting a 9% improvement in current-carrying capacity. Fig. 17(a) depicts the initial surface morphology of the optimized sample at ambient temperature, while Fig. 17(b) shows the noise-filtered morphology obtained through polynomial curve fitting. The optimized FOPLP exhibited less warpage upon heating compared with the original. As shown in Fig. 18, surface warpage was reduced by 13.5% at 60 °C and by 14.7% at 100 °C in DIC tests. It is proved that the optimization of layout is effective to improve the thermal–mechanical properties. In the numerical prediction results, the optimized FOPLP exhibits less warpage compared with the original. This demonstrates that reducing the thermal coupling between chips enhances the uniformity of both temperature and warpage distribution. The experimental results

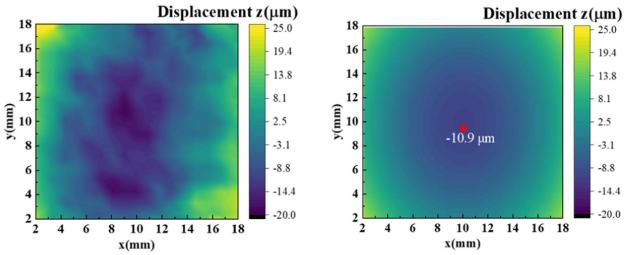


Fig. 17. Warpage of the optimized FOPLP at ambient temperature. (a) Raw data. (b) After fitting.

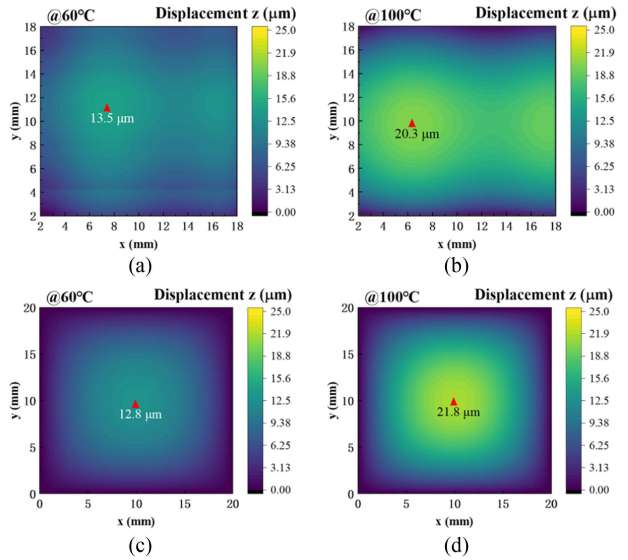


Fig. 18. DIC test results of the relative warpage generated by the optimized FOPLP self-heating at (a) 60 °C and (b) 100 °C. The displacement predicted by the proposed method at (c) 60 °C and (d) 100 °C.

are consistent with the predictions from the numerical model, thereby validating the accuracy and effectiveness of the proposed model.

V. Conclusion

A numerical model for thermoelastic analysis is introduced for double-sided heat dissipation. An innovative packaging approach, FOPLP, validates its efficacy. Throughout the model development, the analytical solution for thermal conduction and the finite-difference numerical solution for the mechanical model associated with the double-sided cooling configuration were derived. Two types of FOPLP samples with four embedded chips each were designed and fabricated, with one sample featuring a thermal-decoupling layout to enhance thermal–mechanical performance based on the proposed numerical method. A DIC testing platform was established to measure warpage in both FOPLP samples at self-heating temperatures of 60 and 100 °C. The trends predicted by the thermal–mechanical numerical model for warpage were found to align with the experimental outcomes.

While this study addressed warpage in FOPLP samples during operation, it is also critical to investigate warpage arising within the panel level package (PLP) manufacturing process, especially for high–precision RDL fabrication. Although this study has successfully developed and experimentally validated the FOPLP manufacturing process and demonstrated its thermomechanical performance, further refinement of the dielectric insulation design is required. Moreover, the existing RDL manufacturing techniques may introduce additional resistance. The optimization of top–side chip interconnection remains an open challenge. This work aims to establish a rigorous scientific foundation to guide the development of advanced packaging solutions for power semiconductor devices.

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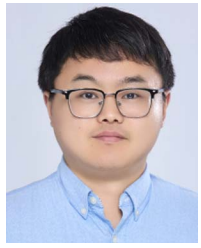

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