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A 33-ppm/°C 240-nW 40-nm CMOS Wakeup Timer based on a Bang-Bang Digital-Intensive Frequency-Locked-Loop for IoT Applications

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***Abstract*—This paper presents a wakeup timer in 40-nm CMOS for Internet-of-Things (IoT) applications based on a bang-bang Digital-intensive Frequency-Locked Loop (DFLL). A self-biased $\Sigma\Delta$ Digitally Controlled Oscillator (DCO) is locked to an RC time constant via a feedback loop consisting of a single-bit chopped comparator and a digital loop filter, thus maximizing the use of digital circuits while keeping only the RC network and the comparator as the sole analog blocks. Analysis and behavior level simulations of the DFLL have been carried out to guide the optimization of the long-term stability and frequency accuracy of the timer. High frequency accuracy and a 10$\times$ enhancement of long-term stability is achieved by the adoption of chopping to reduce the effect of comparator offset and 1/f noise and by the use of $\Sigma\Delta$ modulation to improve the DCO resolution. Such highly digitized architecture fully exploits the advantages of advanced CMOS processes, thus enabling operation down to 0.7 V and a small area (0.07 mm^2). The proposed timer achieves the excellent energy efficiency (0.57 pJ/cycle at 417 kHz at 0.8-V supply) over prior art while keeping excellent on-par long-term stability (Allan deviation floor $<$20 ppm) and temperature stability (33 ppm/°C at 0.8-V supply).**

***Index Terms*—Wakeup timer, Digital-intensive, Frequency locked-loop, internet of things, Low-power, Oscillator.**

I. Introduction

In order to extend battery lifetime of remote wireless sensor nodes in Internet-of-Things (IoT) applications, duty-cycling has been used to achieve an extremely low average power consumption [1]. This approach requires an accurate wakeup timer to turn on the sensor node when required. In addition, since the wakeup timer is continuously running, its energy efficiency is crucial, thus requiring a sub-μW power consumption. Quartz crystals and MEMS-based timers can meet the accuracy and power requirements, but demand off-chip components [2], [3]. This increases timer's cost and module size, which are critical for many IoT applications. As a result, fully-integrated RC oscillators are usually preferred for those applications [4]–[19].

Among fully integrated oscillators, conventional RC relaxation oscillators are limited in accuracy by the delay of power-hungry continuous-time comparators, which are vulnerable to PVT variations [4]–[6], [16]. To circumvent this problem, oscillators based on frequency-locked loops (FLL) have been employed, but they heavily rely on analog-intensive circuits, which require significant power, area and a high supply voltage [7]–[9], [14], [20]. Hence, they are not friendly to technology scaling in terms of area and required supply voltage. On the contrary, operating the whole IoT radio at a lower supply voltage has been recently investigated [21], [22] as a mean to reduce power consumption, extend battery life time, comply with a wide range of energy sources (e.g., button batteries and energy scavengers) and simplify power management by avoiding boost converters.

To operate the wakeup timer at a low supply voltage, a bang-bang Digital-intensive FLL (DFLL) architecture is introduced [23], [24]. By minimizing the amount of analog circuitry, this digital-intensive architecture fully exploits the advantages of advanced CMOS processes, thus allowing low area, low power and low supply voltage. The prototype timer achieves 0.57-pJ/cycle energy efficiency at a low supply voltage (0.8 V), while maintaining excellent on-par long-term stability (Allan deviation floor below 20 ppm), temperature stability (33 ppm/°C at 0.8-V supply and 106 ppm/°C at 0.7-V supply) with a small chip area (0.07 mm^2 in 40-nm CMOS).

The rest of the paper is organized as follows. The architecture of the DFLL is presented in section II. The high-level analysis of the proposed system given in III. The circuit implementation details are described in section IV. Finally, experimental results are presented in section V and conclusions are drawn in section VI.

II. DFLL architecture

The block diagram of the proposed DFLL and the relative timing diagram are shown in Fig. 1 and Fig. 2. The timer consists of a RC-based Frequency Detector (FD), a dynamic comparator, a Digital Loop Filter (DLF), a Digitally-Controlled-Oscillator (DCO) and divider-based clock generation circuits. Similar to conventional analog FLL based oscillators [7]–[9], the output frequency of the DCO f_{osc} is locked to a reference frequency, f_{ref}, which is defined by the resistors and capacitors in the FD. A scaled version of the output frequency $f_{\text{osc}}/(2N)$ is compared to f_{ref} in the FD, and the resulting error $[f_{\text{ref}} - f_{\text{osc}}/(2N)]$ is directly converted into a single digital bit by the comparator for further processing in the DLF. This approach differs from conventional analog-FLL-based designs that use an analog loop filter to process this error. The DLF generates a multi-bit Frequency Control

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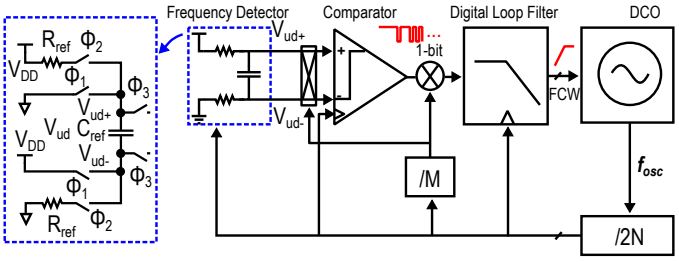


Fig. 1. Block diagram of the proposed Digital FLL.

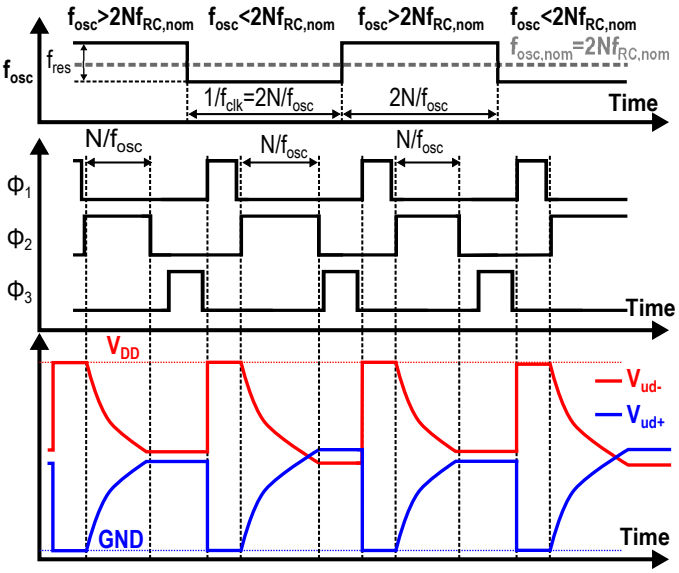


Fig. 2. Timing diagram of the DFLL and its frequency locking behavior.

Word (FCW) for the DCO, which adapts its frequency f_{osc} accordingly until the FLL reaches its steady state. Compared to bang-bang All-Digital Phase-Locked Loop (ADPLL) [25], the proposed DFLL operates in frequency domain instead of phase domain due to the lack of a reference clock.

The frequency detector is similar to the one proposed in [8] and works as follows: When Φ_1 is high, C_{ref} is reset to $V_{ud} = V_{ud+} - V_{ud-} = -V_{DD}$. During Φ_2, C_{ref} is discharged to $V_{ud} = V_{DD}$ through the two resistors R_{ref}. The voltage V_{ud} on C_{ref} at the end of Φ_2 can be expressed as:

$$\begin{aligned} V_{ud} &= V_{ud+} - V_{ud-} = V_{DD} \cdot \left[1 - 2 \cdot e^{-\frac{t_{\Phi_2}}{2R_{ref}C_{ref}}}\right] \\ &= V_{DD} \cdot \left[1 - 2 \cdot e^{-\frac{1}{4R_{ref}C_{ref}f_{clk}}}\right], \end{aligned} \tag{1}$$

where $f_{clk} = f_{osc}/(2N)$ and $t_{\Phi_2} = 0.5/f_{clk}$ is the duration of Φ_2. During Φ_3, the voltage on C_{ref} is held and represents the frequency error between the timer output frequency and the reference frequency. The capacitor is then connected to the comparator, so that this error is quantized. The error is processed by the DLF and drives the DCO such that, in average, $V_{ud} = 0$. Thus, in the steady state, the nominal oscillator output frequency is given by

$$f_{osc,nom} = 2Nf_{clk,nom} = \frac{N}{2\ln(2)R_{ref}C_{ref}}, \tag{2}$$

Thanks to the feedback loop, no active components other than switches are used to determine the nominal oscillation frequency $f_{osc,nom}$, which only depends on resistor and capacitor values, unlike conventional designs that involve the performance of analog intensive blocks, e.g., comparator delay [4] or amplifier gain [7]. In addition, the digital-intensive architecture exploits the energy efficiency of digital circuits and their operation at a low supply voltage, thus being amenable to CMOS process scaling. By exploiting such advantages, the goal of this work is to improve the energy efficiency to better than 1 pJ/cycle, while still keeping on-par long-term stability (<20 ppm Allan deviation floor) and temperature stability (<100 ppm/°C).

III. System Analysis

In this section, a high-level system analysis of the DFLL is provided and design considerations for the wakeup timer in terms of noise and accuracy are discussed. An s-domain model is proposed to predict the effect of noise on the long-term stability. In addition, a time-domain behavioral model is built in MATLAB to verify the prediction of the s-domain model and to simulate the performance of the timer in presence of circuit non-idealities.

A linearized small signal model for the DFLL is shown in Fig. 3. The frequency detector is modelled with a gain K_{RC} and an additive noise source $v_{n,RC}$. The comparator is modeled by an additive noise source $v_{n,CMP}$ equal to the input-referred physical noise of the comparator, a quantization noise Q_{CMP} and a gain g. Note that in the linearized model of the comparator, the gain g depends on the power of the signal applied at the input of the comparator since the comparator output is fixed as either 1 or 0, as typically happens in the modelling of $\Sigma\Delta$ modulators [26]. A 1^{st}-order DLF is assumed, which is approximated as the cascade of a gain K_{DLF} and an integrator with unity-gain frequency f_{DLF}, so that the DLF transfer function is $K_{DLF} \cdot f_{DLF}/s$. The DCO model is characterized by a gain factor K_{DCO}. The factors $2\pi/s$ and $s/2\pi$ are used to convert the DCO output from the frequency to the phase domain and vice versa and thus enable the addition of the DCO phase noise ϕ_{DCO}.

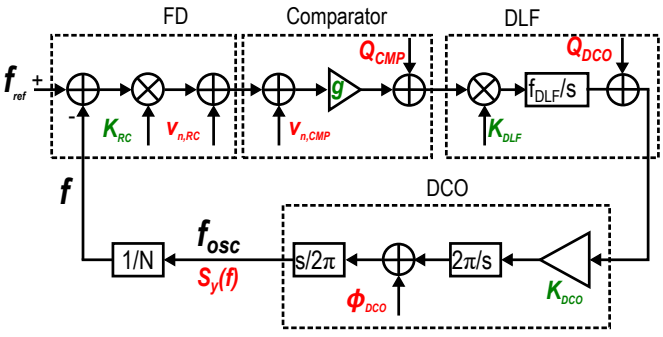


Fig. 3. A linear model of the proposed DFLL.

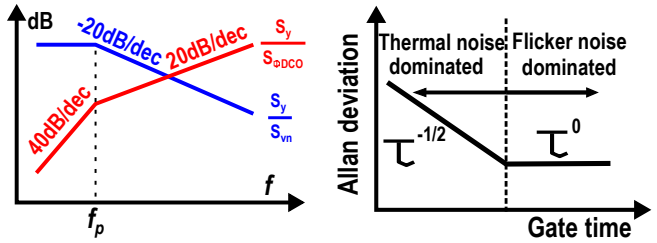
A. Random noise

There are three main random noise sources in the proposed oscillator: $v_{n,RC}$, $v_{n,CMP}$ and ϕ_{DCO}. Using the model, the

transfer functions from each of these sources to the output fractional frequency fluctuation S_y can be calculated as:

$$\frac{S_y}{S_{v_{n,RC}}} = \frac{S_y}{S_{v_{n,cmp}}} = \frac{gNK_{DLF}K_{DCO}f_{DLF}}{Ns + gK_{RC}K_{DLF}K_{DCO}f_{DLF}}; \quad (3)$$

$$\frac{S_y}{S_{\phi_{DCO}}} = \frac{Ns^2}{2\pi(Ns + gK_{RC}K_{DLF}K_{DCO}f_{DLF})}. \quad (4)$$



(a) (b)

Fig. 4. Gain plots of the noise transfer functions (a) and Allan deviation illustration (b).

The plots of the transfer functions in (3) and (4) in Fig. 4(a) show that $v_{n,RC}$ and $v_{n,CMP}$ are first-order low-pass filtered, whereas ϕ_{DCO} is second-order high-pass filtered. Since a wakeup timer is usually continuously running in the background and the sleep time is typically in the order of hundreds of milliseconds or more, long-term stability is the relevant noise parameter for wakeup timers. Allan deviation is usually used to evaluate the long-term stability of the wakeup timer for a specific gate time τ, over which the frequency deviation is evaluated. The Allan variance at gate time τ can be computed as [27]:

$$\sigma_y^2(\tau) = \int_0^{f_h} S_y(f)\frac{2\sin^4(\pi\tau f)}{(\pi\tau f)^2}\mathrm{d}f, \quad (5)$$

where f_h is the high-frequency cut-off of the measurement instrumentation. As shown in the simplified Allan deviation diagram of a typical oscillator in Fig. 4(b), for a relatively short gate time, i.e. in the $\tau^{-1/2}$ region, the Allan deviation is dominated by white frequency noise, such as thermal noise, while for a relatively long gate time, i.e. in the τ^0 region, it is limited by low-frequency noise, such as the 1/f noise. Due to the noise transfer functions [Fig. 4(a)], the noise of the FD and of the comparator are the major contributors to the long-term stability in eq. (5), while the noise of the DCO is filtered by the noise transfer function [see eq. (4)] in the region of interest for long-term stability, i.e. close to DC.

The noise of a switched-capacitor network in the FD, $v_{n,RC}$, is white with standard deviation:

$$\sigma_{v_{n,RC}} = \sqrt{\frac{kT}{C_{ref}}}, \quad (6)$$

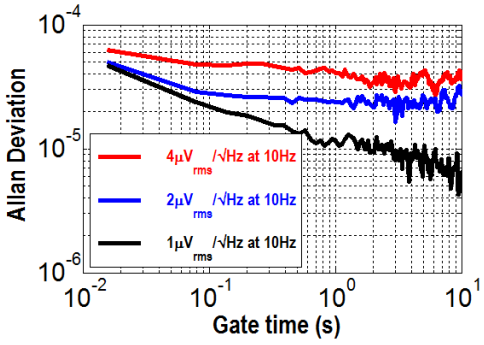
thus, it does not significantly contribute to the long-term stability. However, if the capacitor is implemented as programmable switched-capacitor array, as shown later in section IV, the off-state leakage of the switches in the capacitor array can contribute flicker noise, but this contribution is negligible in typical cases. As a result, the flicker noise determining the long-term stability is only contributed by the comparator.

Since the comparator and the DCO are extremely non-linear component, a time-domain behavioral model for the DFLL has been implemented in MATLAB to confirm the predictions of the linearized model on the contribution of the comparator and the DCO noise. The event-driven method described in [28] has been employed in the simulation to model the phase noise. The key parameters of the DFLL are kept fixed in all the following behavioral simulations, including R_{ref}=6.9 MΩ, C_{ref}=4 pF, K_{DLF}=1/8, K_{DCO}=250 Hz, N=16, resulting in $f_{osc} = 524$ kHz, while the amount of noise introduced by the comparator and the DCO is swept and based on the realistic values predicted by the circuit simulations. When not explicitly specified, the comparator noise is assumed composed by flicker noise with 2.5 μV/$\sqrt{Hz}$ Power Spectral Density (PSD) at 10 Hz and by a thermal noise floor is 1 μV/$\sqrt{Hz}$. For the DCO, the phase noise has a flicker-noise component with -42 dBc/$\sqrt{Hz}$ PSD at a 1-kHz offset from the carrier and a -100 dBc/$\sqrt{Hz}$ phase-noise white floor. As shown in Fig. 5(a), higher comparator flicker noise leads to a higher Allan deviation floor. To achieve an Allan deviation floor lower than 20 ppm, the comparator flicker noise has to be lower than 1 μV_{rms} at 10 Hz. Note that since the DCO noise is high-pass filtered, it influences the Allan deviation mostly at small gate times, as shown in Fig. 5(b). Although the DCO phase noise has less impact on the Allan deviation floor, it can still be non-negligible if too large. To ensure a negligible degradation of the Allan deviation for gate time beyond 1 s, the DCO phase noise should be less than approximately -40 dBc/Hz at 1 kHz frequency offset.

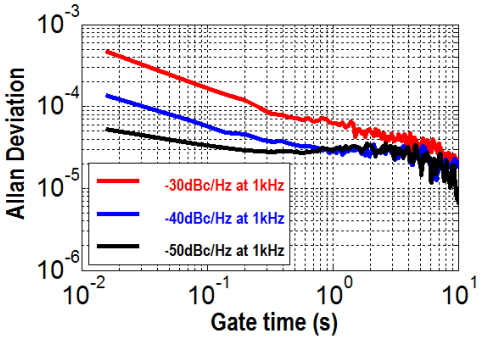
B. Quantization noise

There are two quantization-noise sources in this system: the comparator quantization noise Q_{CMP} and the DCO quantization noise Q_{DCO}. The comparator quantization noise Q_{CMP} is included in the model, but can not be modified manually. Since we assume a single-bit comparator, no direct tuning of the comparator quantization noise is possible. However, its impact on the reference performance varies depending on the other loop parameters. The DCO quantization noise is due to the truncation at the DLF output to adapt the DLF digital output to the finite resolution of the DCO, and therefore represent a parameter for the optimization of the design. Due to the bang-bang operation of the DFLL, the DCO output frequency will continuously toggle in the steady state. If the random noise in the loop is neglected, the DCO control word will toggle between two consecutive values corresponding to the frequencies f_{osc1} and f_{osc2} that straddle $f_{osc,nom}$, as shown in Fig. 6. Since such locking condition is satisfied for any $f_{osc,nom}$ between f_{osc1} and f_{osc2}, this results in a worst-case frequency offset $|f_{os}| < \frac{f_{osc1}-f_{osc2}}{2} = \frac{f_{res}}{2}$, where f_{res} is the DCO resolution. Although this source of inaccuracy is partially mitigated by the dithering effect of random noise, care has been taken to maximize the DCO resolution not to degrade the timer accuracy.

The quantization noise Q_{DCO} may also affect the Allan deviation, since it can be modelled as white noise. The Allan



(a)



(b)

Fig. 5. Allan deviation as a function of comparator noise (a) and DCO phase noise (b) obtained by time-domain simulation in Matlab. DCO phase noise and comparator noise are kept constant in (a) and (b), respectively.

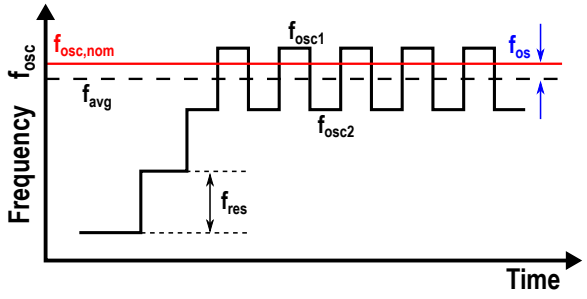


Fig. 6. Illustration of the frequency error due to the DCO finite resolution.

deviation has been simulated using the time-domain model with both high quantization noise (high Q_{DCO}) and low quantization noise (low Q_{DCO}), which corresponds to a DCO resolution f_{res} of 2 kHz and 250 Hz, respectively. The results in Fig. 7 show that the Allan deviation is lower in case of a smaller f_{res} for a short gate time, i.e. in the region dominated by white noise where the Allan deviation scales with $\tau^{-1/2}$. This confirms the validity of approximating quantization noise as white noise, since a finer f_{res} would result in a lower noise level and consequently a lower Allan deviation in the $\tau^{-1/2}$ region.

C. Comparator offset and flicker noise

The temperature-dependent comparator offset error V_{os} could also degrade the frequency stability of the oscillator. Since V_{os} is directly added to V_{ud}, the original zero-crossing time of the differential voltage V_{ud} time will deviate. As a

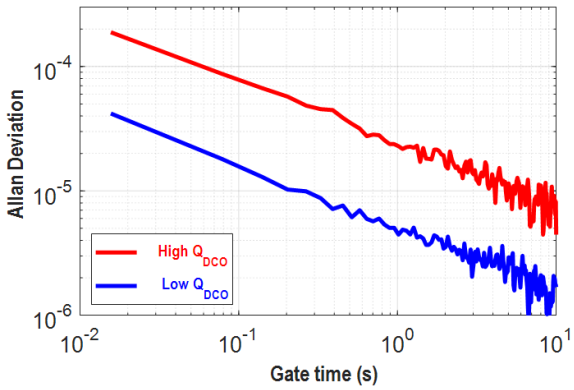


Fig. 7. Simulated Allan deviation with respect to DCO quantization noise.

result, a DC frequency offset will be present on the nominal output frequency $f_{osc,nom}$. Assuming the comparator offset voltage $V_{os} \ll V_{DD}$, the resulting fractional frequency offset can be calculated from (1) and (2) as

$$\Delta f = \frac{f_{osc} - f_{osc,nom}}{f_{osc,nom}} = -\frac{\ln\left(1+\frac{V_{os}}{V_{DD}}\right)}{\ln\left(1+\frac{V_{os}}{V_{DD}}\right) - \ln(2)} \approx \frac{2}{\ln 4}\frac{V_{os}}{V_{DD}}. \quad (7)$$

For V_{DD}=0.7 V, an offset of 2 mV will cause a fractional frequency offset of 0.4% on $f_{osc,nom}$. This result agrees with the simulation result generated by the MATLAB behavioral model shown in Fig. 8. To tackle the effect of the comparator offset, the chopping technique is used for the comparator, as shown in Fig. 1. By using chopping, both offset and flicker noise are up-modulated to the chopping frequency and then low-pass filtered by the DFLL closed-loop response. As a result, the frequency error due to V_{os} is reduced to a negligible level (Fig. 8). In addition, as expected and as confirmed by the MATLAB behavioral simulations, the effect of the flicker noise is also reduced, leading to an improvement of the Allan deviation, as shown in Fig. 9.

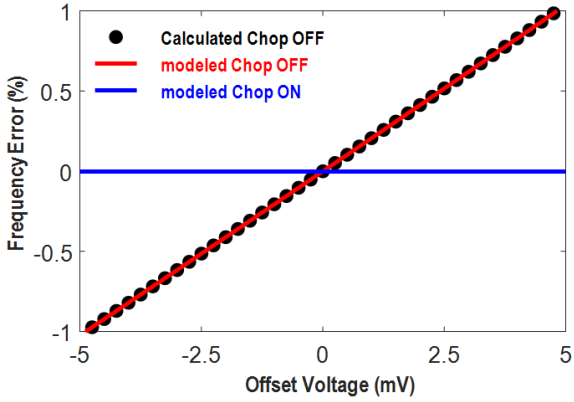


Fig. 8. The relation between comparator offset and timer's frequency offset.

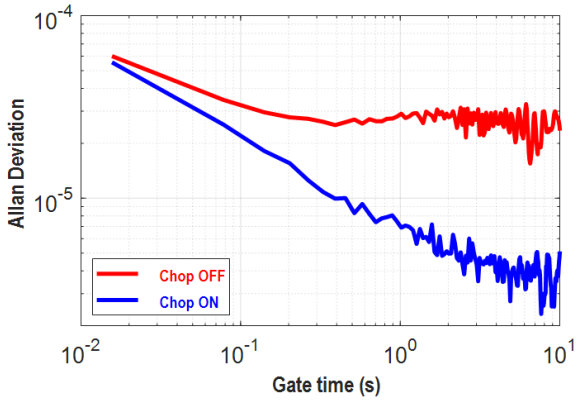


Fig. 9. Simulated Allan deviation due to comparator noise with the chopping technique on and off.

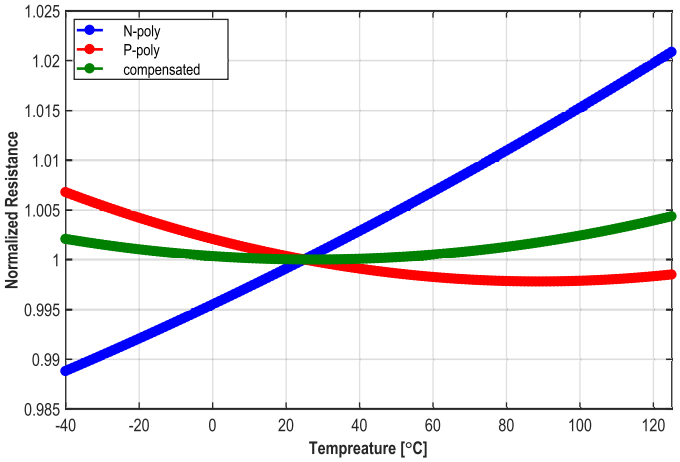


Fig. 10. Temperature dependencies of the resistors.

D. Accuracy of the RC network

The frequency of the timer is mainly determined by the resistance (R_{ref}) and capacitance (C_{ref}) of the components in the FD (Eq. 2). Process variations of the resistors and the capacitors can be easily compensated by a one-time trimming to remove the static frequency error of the DFLL. However, the temperature coefficient of the resistors and the capacitors would result in a residual temperature-dependent frequency error. When using a metal-oxide-metal (MOM) capacitor for C_{ref}, the temperature coefficient (TC) of the capacitor can be neglected in comparison to that of the resistor [29]. A popular 1^{st}-order temperature compensated resistor topology can be used to partially cancel the resistor TC. It is usually implemented by placing two resistors with opposite TC in series and properly tuning the ratio α between their resistance to minimize the TC of the equivalent series resistance. For example, when using a N-poly resistor R_{np} with a TC of 187 ppm/°C together with a P-poly resistor R_{pp} with a TC of -69 ppm/°C for a 1^{st}-order temperature compensation, the TC of the total resistance can be minimized down to 27 ppm/°C, as shown in Fig. 10. The residual 27 ppm/°C TC of the compensated resistor is dominated by its higher-order temperature dependencies. Process spread can degrade the accuracy of α and therefore the TC of the compensated resistor. This is investigated by Monte Carlo simulations of the circuit implementation of the compensated resistor. The 3σ variation of the TC error after one-point temperature compensation is 0.42 ppm/°C. Besides, for the switches in the FD, they should have small on-resistance compared to the resistance value of the RC network to minimize their impact on the overall TC of the FD. Taking into account those effects, a residual TC of approximately 50 ppm/°C is expected, mostly dominated by the switch on-resistance.

E. Power consumption of the timer

In this section, we analyze the limits in the power consumption of the proposed timer architecture. The power consumption of the timer P_{TOT} can be broken down into four parts: the power consumption of the frequency detector (P_{FD}), of the comparator (P_{CMP}), of the digital section, i.e. the digital loop filter and the divider, (P_{DIG}), and of the DCO (P_{DCO}).

If we neglect the power required to drive the switches in the FD[1], P_{FD} is mainly contributed by charging the reference capacitor C_{ref}, and thus can be approximated as:

$$P_{FD} = \frac{1}{2} C_{ref} V_{DD}^2 \cdot \frac{f_{osc,nom}}{2N} = \frac{V_{DD}^2}{8 \ln(2) R_{ref}}, \qquad (8)$$

where (2) has been used.

The power consumption of digital circuits in this relatively low-speed design is mainly determined by the total switched capacitance in the digital cells C_{DIG}, and can then be approximated as $P_{DIG} = C_{DIG} V_{DD}^2 f_{osc,nom}/(4N) + I_{leak} V_{DD}$, where the leakage current $I_{leak} = \alpha_{leak} C_{DIG}$ is assumed proportional to the digital-circuit area and, hence, also to C_{DIG}. For the comparator, there are no strict requirements for thermal noise because it does not contribute to the timer's Allan deviation floor. The flicker noise and the offset of the comparator are tackled by the chopper, hence they also do not influence the comparator power. In addition, as shown later in section IV-B, the speed of the comparator is relaxed thanks to the DFLL-based architecture. Therefore, small devices can be tolerated in the comparator, thus making its power consumption similar to that of a digital circuit $P_{CMP} = C_{CMP}[V_{DD}^2 f_{osc,nom}/(4N) + \alpha_{leak} V_{DD}]$, where C_{CMP} is the equivalent total switched capacitance of the comparator. For the DCO, its noise is high-pass filtered by the loop transfer function, as analyzed before [see Fig. 4(a)]. Hence, the DCO can be optimized for power consumption, instead than for noise. Leakage-based oscillators are a very power-efficient choice for low-frequency ultra-low-power wakeup timers [30]. Assuming their use, the DCO power consumption is proportional to the oscillation frequency and can be estimated as $P_{DCO} = C_{DCO} V_{DD}^2 f_{osc,nom}$, where C_{DCO} is the equivalent total switched capacitance of the DCO[2]. As a result, the total power is given as

[1]Although the power required to drive the switches is proportional to their size and hence to their equivalent conductance, the lowest power consumption will be reached for large R_{ref}, as explained in the following, thus allowing for minimum-size switches. In that case, such driving power could be considered as part of the digital power consumption.

[2]The power of the frequency divider is also included in the DCO power.

$$P_{TOT} = (C_{CMP} + C_{DIG}) \cdot \left(V_{DD}^2 \cdot \frac{f_{osc,nom}}{4N} + \alpha_{leak} V_{DD} \right) + \frac{V_{DD}^2}{8ln2R_{ref}} + C_{DCO} \cdot V_{DD}^2 \cdot \frac{f_{osc,nom}}{2}. \quad (9)$$

Eq. (9) provides a few indications to optimize the power consumption of the proposed timer. Firstly, the power consumption of both the digital circuits and the comparator can be reduced by operating at a lower frequency with a larger division ratio N, although this could significantly slow down the loop and degrade its regulating properties. Secondly, Eq. (9) suggests that the power consumption of the FD depends only on the reference resistor R_{ref}. Although power could be reduced with a larger R_{ref}, this is at the cost of a larger area for the resistors. Thirdly, the power of the DCO, the digital and the comparator can be reduced by operating at a lower frequency $f_{osc,nom}$ or by further pushing down the supply voltage V_{DD}. In addition, in a more advanced technology, smaller devices and smaller parasitic, which lead to smaller C_{DIG}, C_{CMP} and C_{DCO}, and lower supply voltage are expected, thus leading to further power savings. For instance, while the proposed design dissipates 240 nW (see Table II) for $N = 16$ and $R_{ref} = 6.9M\Omega$, the power consumption could go down to 62 nW, with P_{CMP}+P_{DIG}=20 nW (limited by leakage in 40nm CMOS), P_{FD}=0.8 nW, and P_{DCO}=41 nW, for $N = 512$ and R_{ref} =110 MΩ when keeping the same values for the other parameters, such as the output frequency $f_{osc} = 417$ kHz .

As mentioned above, the power consumption of the comparator and the DCO can be reduced by using small devices but smaller devices have higher flicker noise. Although the effect of the comparator flicker noise is cancelled by the chopper, reducing the power consumption would lead to higher thermal noise, and thus the gate time to reach the Allan deviation floor will also increase, which means longer averaging time in real applications. Furthermore, if the DCO flicker noise is too high, the residue noise after filtering could still be significant, thus degrading the Allan deviation (Fig. 5(b)).

F. System performance

The key specifications for each sub-block to achieve the required performance for the timer are summarized in Table I. The contributions to the Allan deviation floor comes mainly from the DCO, the comparator, and the FD. Since the DCO phase noise is high-pass filtered as mentioned before, its contribution is relatively small. According to Fig. 7, a 250-Hz DCO tuning step can assure a sufficiently small Allan deviation (<2ppm). For the comparator, its 1/f noise is tackled by using a chopper, leading to an expected contribution to the Allan deviation floor below 10 ppm according to behavioral simulation. The 1/f noise in the FD resistors can contribute to Allan deviation floor, but since Poly resistors in CMOS technology usually have small 1/f noise, a small contribution is expected (<20 ppm) [7], [15]. The DCO resolution is kept high (<250Hz) to have sufficient margin for a worst-case frequency error (<300ppm). The timer's TC is mainly limited by the TC of the FD resistor network, assuming that the comparator offset can be removed by a chopper. By trimming the resistor network, a <50 ppm/°C TC can be achieved for the timer according to the simulations.

TABLE I
SPECIFICATION FOR THE SUB-BLOCKS.

	Sub-block performance	Sub-block resulted timer performance		
		Allan deviation floor	TC	Frequency offset
Comparator 1/f noise	<2μV/√Hz at 10Hz	<10ppm (after chopping)	-	-
DCO resolution	≤250Hz	<2ppm	<3ppm/°C	<300ppm
Freq. detector TC	50ppm/°C	-	<50ppm/°C	-
Freq. detector 1/f noise	-	<20ppm	-	-
Comparator offset (after chopping)	<0.015mV	-	<0.3ppm/°C	<30ppm
Total Allan deviation floor	-	≤20ppm	-	-
Total TC	-	-	<50ppm/°C	
Frequency error	-	-	-	<300ppm

IV. CIRCUIT IMPLEMENTATION

The detailed architecture of the proposed DFLL is shown in Fig. 11. The differential frequency detector (FD) is driven at a clock frequency f_{clk}=f_{osc}/32 derived from the output frequency of the DCO f_{osc}. At the end of Φ_2, the output of the FD V_{ud} is processed by the comparator and its sign is detected and further processed by the DLF at a rate $f_{osc}/32$. The 11-bit FCW from the DLF drives the DCO in a negative feedback to ensure that, on average, $V_{ud} = 0$ and, hence, $f_{osc}/32 = f_{nom}$. The DCO output frequency is fed into a multi-phase clock divider to provide all the clocks required in this self-clocked FLL. The large adopted frequency division factor N=32 is advantageous: Φ_2 and, consequently, the output frequency (f_{osc}) can be accurately set thanks to the availability of multiple phases; moreover, most of the circuit in Fig. 11 runs at a much lower frequency, thus saving power. For example, a fixed and relatively long comparator delay (≈ 4.8 μs) can be allowed compared to the ∼ns delay of continuous-time comparators [4], thus enabling the comparator to be optimized for power instead of speed. A longer comparator delay is allowed in this architecture, since f_{osc} only depends on the duration of Φ_2. The main drawback of running the loop filter at a lower frequency is an increase in the loop settling time.

The only analog components in the DFLL are the switching passive RC network for the FD, the comparator and the DCO. As shown in Section II, such analog circuits can be implemented using switches and inverter-based structures, so that they can be easily integrated in a nanometer CMOS process with a low power consumption, a low supply voltage and a small area.

A. Frequency detector

The DFLL output frequency is set to $f_{osc,nom} = 32 f_{RC,nom} = 8/(R_{ref} C_{ref} \ln 2) \approx 417$ kHz with $R_{ref} =$

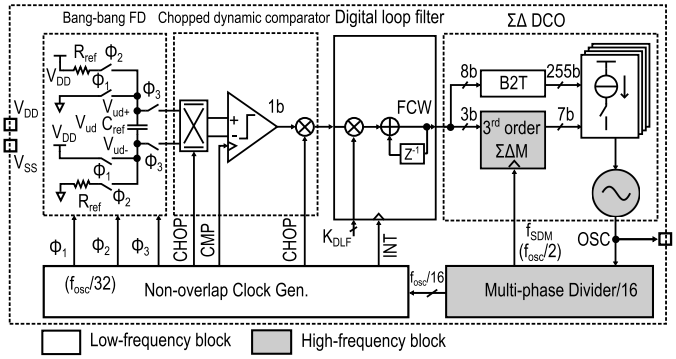


Fig. 11. Implemented architecture of the proposed DFLL wakeup timer.

6.9 MΩ and $C_{ref} = 4$ pF chosen for minimum die area occupation. The differential circuit topology of the FD ensures a high immunity against supply and ground noise. The resistor R_{ref} is implemented by a series combination of non-silicided p-poly and n-poly resistors with opposite temperature coefficients (TC) to provide a first-order compensation of the TC of f_{osc} (Fig. 12). Both R_{ref} and C_{ref} are implemented as switchable arrays that can be digitally tuned to compensate for process spread. For the capacitor bank, a Metal-Oxide-Metal (MOM) capacitor is used to implement the 3.25-pF fixed capacitance and a customized finger capacitor is used to implement the 10-bit tunable capacitor bank. Since the on-resistance of switch SW2 adds to R_{ref}, it must be minimized, but, at the same time, SW2 must show has a small leakage current in the off-state. Thus, thick-oxide transistors are used, which achieve a 58-kΩ on-resistance (limited by the low supply voltage and the relatively large threshold voltage of thick-oxide transistors) and an 80-pA leakage current in the nominal case at room temperature.

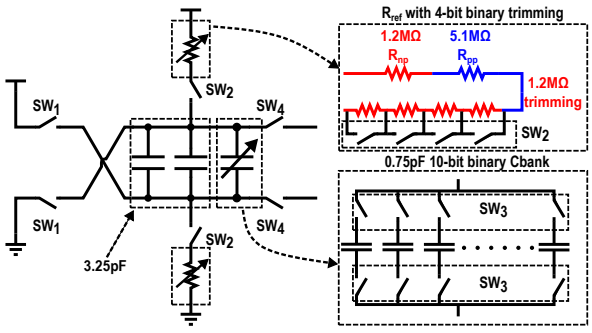


Fig. 12. Reconfigurable RC network.

B. Chopped dynamic comparator

Unlike traditional RC relaxation oscillators requiring continuous-time comparators, the comparator is implemented as a two stage dynamic comparator (Fig. 13) and works as follows: Firstly, when CLK is low, the first stage's outputs AP and AN are charged to V_{dd}, while the second stage's outputs OUTP and OUTN are reset to ground, thus preparing the comparator for the next comparison. Secondly, when CLK goes high, AP and AN will discharge with different rates according to the difference between INP and INN and the cross-coupled latch will make a decision accordingly [31].

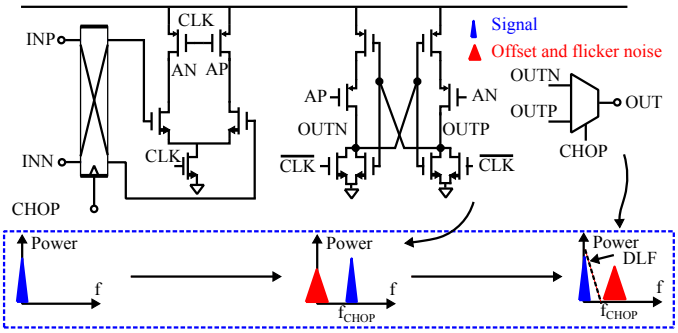


Fig. 13. Dynamic comparator with a hybrid chopper.

In conventional RC relaxation oscillators, the delay of the continuous-time comparator contributes to the oscillation period. Since such delay is sensitive to PVT (Process, Voltage and Temperature) variations, the comparator delay must be minimized down to ∼ns for good frequency stability [4]. However, this requires non-negligible power in the comparator. A long comparator delay up to $2/f_{osc}$ (≈ 4.8 μs) is allowed in this architecture, thus allowing the design of a comparator with a simulated power consumption of only 10 nW.

To suppress the effect of both offset and flicker noise, the dynamic comparator is chopped at a frequency of $f_{osc}/128$ by means of an analog and a digital chopper at the comparator input and output, respectively (Fig. 13). In this way, the input offset and flicker noise are up-converted to higher frequencies and gets filtered out by the cascaded DLF, while the input signal stays at DC.

C. Digital loop filter

The digital loop filter (Fig. 11) comprises a configurable gain (K_{DLF} in Fig. 11) and a digital accumulator which, thanks to the comparator output being single-bit, are implemented in a compact and low-power form by a bit-shifter and an up/down counter, respectively. The accumulator is 18-bit length while the DLF gain can be configurable. By changing the digital filter gain, the overall bandwidth of the DFLL can be easily configured and more reliably predicted than in conventional analog FLL's, which are more vulnerable to PVT variations. This feature allows the DFLL to flexibly trade-off bandwidth and noise for different IoT scenarios. For example, applications dealing with fast temperature or supply changes prefer a higher loop gain, which results in wider loop bandwidth; instead, applications requiring a lower noise need a lower loop gain.

D. ΣΔ DCO

As shown in section II, the resolution f_{res} of the DCO has to be better than 250 Hz to have sufficient margin for small frequency error and low Allan deviation floor (<20ppm). At the same time, sufficient tuning range (500 kHz) for the DCO is required to tackle its frequency drift over PVT. Therefore,

an 11-bit DCO is required, which is challenging with the very limited power budget in the wakeup timer ($\ll 1\mu$W). To address this challenge, a $\Sigma\Delta$ DAC is introduced to improve the DCO resolution (Fig. 14).

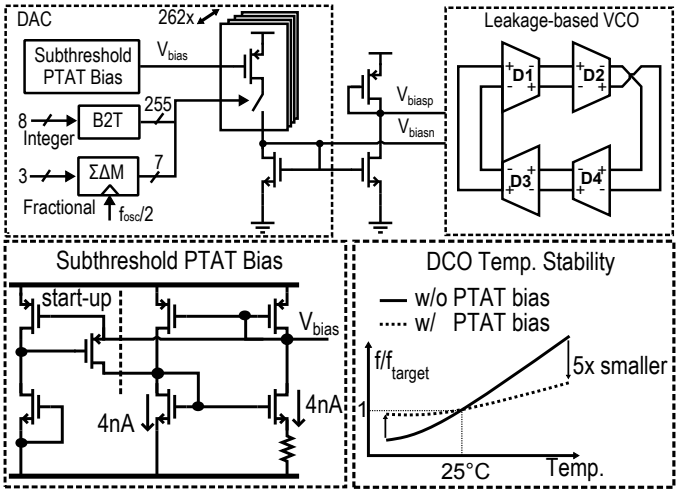


Fig. 14. Implementation of the self-biased $\Sigma\Delta$ DCO.

The self-clocked $\Sigma\Delta$ DAC consists of 255+7=262 unary-coded elements driven by an 8-b integer thermometric DAC clocked at $f_{osc}/32$ and a 3-b fractional DAC processed by a 3rd-order digital $\Sigma\Delta$ modulator. Thanks to the feedback loop, no strict linearity requirements are required for the DAC other than the monotonicity necessary for loop stability. Monotonicity is ensured by the unary nature of the DAC. The $\Sigma\Delta$ modulator is clocked at $f_{osc}/2$ (16× oversampling ratio) to further improve the DCO resolution from 2 kHz to below 250 Hz. The modulator used in this design is a 3^{rd}-order multi-stage noise shaping (MASH) modulator (Fig. 15) [32]. It consists of three accumulators, three logic delays and one logic combiner to generate the thermometer code for the fractional DAC. The effect of the third-order $\Sigma\Delta$ modulator in resolution enhancement is also confirmed with simulations in the time-domain model as introduced in section II. The DCO intrinsic phase noise is small enough to meet the Allan deviation specifications.

A 4-stage differential ring oscillator employing an ultra-low-power leakage-based delay cell is adopted to keep the oscillator power below 60 nW (Fig. 14) [9]. In addition, a sub-threshold local proportional-to-absolute-temperature (PTAT) current bias is used to lower the DCO temperature drift while exploiting a nW oscillator topology. This effectively reduces the oscillator temperature drift by 5×, thus relaxing the DAC design (Fig. 14). All the transistors in the PTAT circuits operate in deep subthreshold region, consuming only 8 nA in total. A start-up circuit is added to ensure the successful start-up over all corners.

V. Measurements

The 0.07-mm^2 wakeup timer was fabricated in a standard TSMC 1P5M 40-nm CMOS process (Fig. 16) and draws 259 nA from a single 0.7-V supply for an output frequency of 417 kHz (power breakdown: 32% FD/comparator, 38% digital, 30% DCO). This corresponds to a state-of-the-art energy efficiency of 0.43 pJ/cycle.

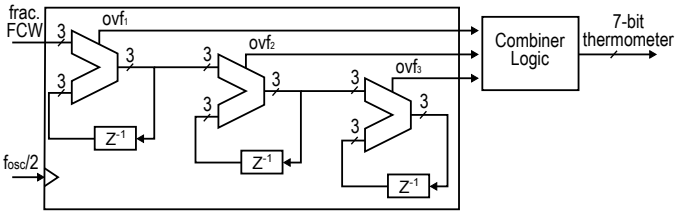


Fig. 15. Implementation of the MASH $\Sigma\Delta$ modulator.

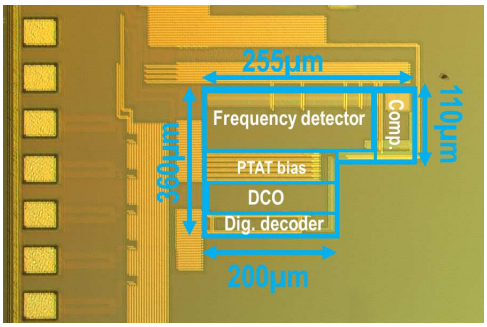
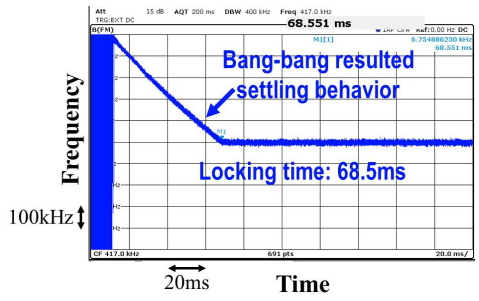
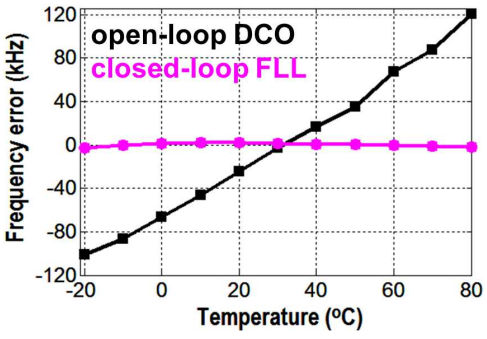


Fig. 16. Chip micrograph.



(a)



(b)

Fig. 17. Measured DFLL settling (KDLF=1/8) (a) and open/closed loop performance (b).

Once enabled, due to the bang-bang operation, the frequency of the DFLL increments or decrements towards the steady-state frequency (Fig. 17(a)). The locking of the FLL can be observed in Fig. 17(b), in which the DCO output frequency in open-loop and closed-loop configuration are compared. As shown in Fig. 18, large spurs are observed in the DFLL output

spectrum when the ΣΔ modulator is disabled, indicating the existence of limit cycles. Enabling the ΣΔ modulator partially breaks the limit cycle, thus leading to a reduction of the spurs.

Thanks to the self-clocked ΣΔ and the chopped comparator, the long-term stability (Allan deviation floor) improves by 10× down to 12 ppm beyond a 100-s integration time (Fig. 19). The long-term stability is relatively insensitive to temperature and supply-voltage variations (Fig. 20).

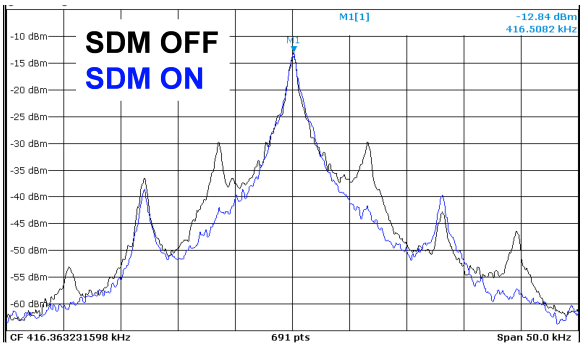


Fig. 18. DFLL output spectrum with SDM on and off.

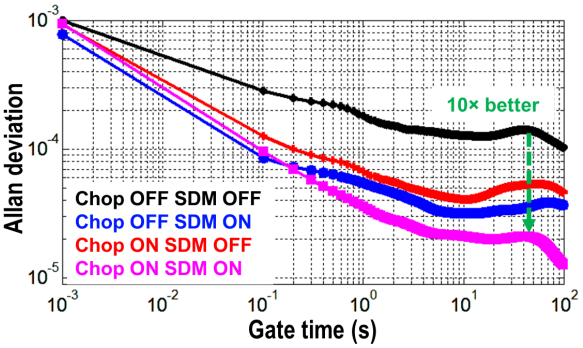


Fig. 19. Measured long-term stability of the timer.

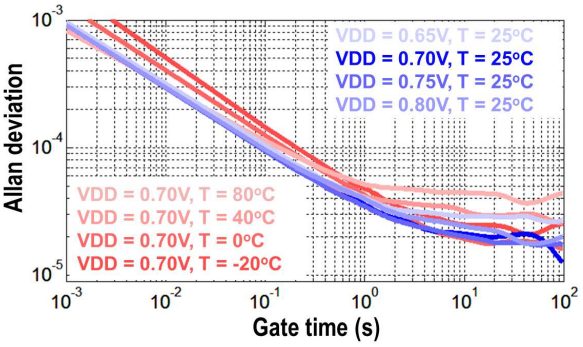


Fig. 20. Measured long-term stability against temperature and supply voltage variations.

The temperature sensitivity of the output frequency improves from 134 ppm/°C to 106 ppm/°C when activating the chopping and the ΣΔ modulation, thanks to smaller errors due to a smaller DCO step and the mitigation of comparators offset (Fig. 21). The timer operates over the 0.65-0.8-V supply range with a deviation of ±0.6% (Fig. 21). In addition, the temperature stability measurements have been repeated over three chips. By trimming the resistors in each chip to minimize the timer TC over the whole temperature range and keeping the same setting over temperature, all samples show similar temperature stability: 106 ppm/°C, 123 ppm/°C, 177 ppm/°C, for a supply voltage of 0.7 V (Fig. 22). Although such temperature and supply sensitivities are sufficient for typical IoT applications and are on par with state-of-the-art designs (see Table II), simulations show that they are limited by the on-resistance of the FD switches at such low supply and could be improved in a re-design. When the characterization is repeated with the supply voltage increased to 0.8 V, the TC improves by a factor as high as 5× down to 48 ppm/°C, with a worst-case TC over the tested samples of 33 ppm/°C.

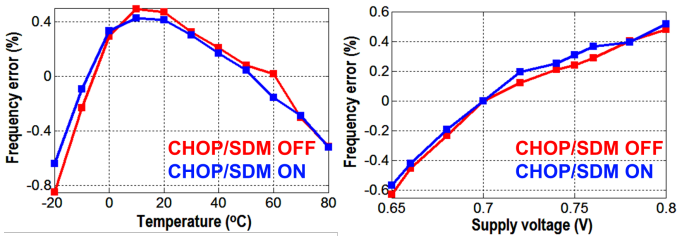


Fig. 21. Measured frequency stability against temperature and supply voltage variation.

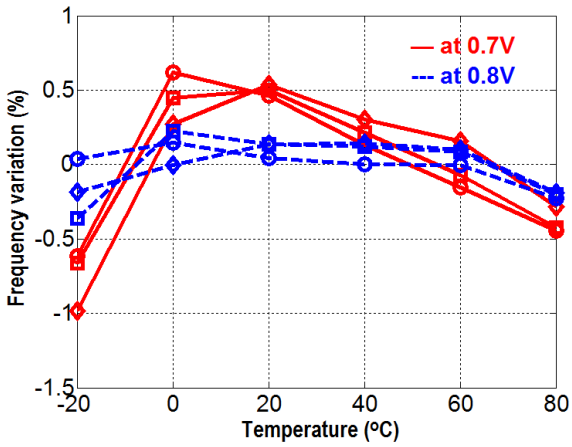


Fig. 22. Frequency stability measurement over multiple samples.

The performance is summarized and compared with other sub-μW state-of-the-art designs in Table II. Being integrated in the most advanced CMOS process (40 nm) among nW timers to show its scaling advantages, the presented timer achieves a excellent power efficiency (0.57 pJ/cycle) with a relatively low operating supply voltage (0.8V) with comparable temperature coefficient (33ppm/^{o}C) and Allan deviation floor (12ppm) among state-of-the-art sub-μW timing references.

VI. Conclusion

An ultra-low-power wakeup timer employing a bang-bang digital-intensive frequency-locked loop has been integrated in a 40-nm CMOS process. Thanks to the highly digital architecture, this timer achieves the best power efficiency

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This work		Savanth ISSCC'17	Paidimarri JSSC'16	Jang ISSCC'16	Choi JSSC'16	Wang JSSC'16	Griffith ISSCC'14	Tokairin VLSI'12	Jung JSSC'18	Jiang JSSC'18	Truesdell SSCL'19	Dai CICC'15
Architecture	**DFLL**		Relaxation oscillator	Relaxation oscillator	Analog FLL	Analog FLL	Capacitive discharging	RC oscillator	Relaxation oscillator	Analog FLL	Relaxation oscillator	Analog FLL	Relaxation oscillator
Process (nm)	**40**		65	65	180	180	250	65	90	180	180	65	180
Frequency (Hz)	**417k**		1350k	18.5k	3K	70.4k	6.4k	33k	100k	32.7k	1.22k	1016k	122k
VDD (V)	**0.7**	**0.8**	1.4	1	0.85 - 1.4	1.3	0.8	1.15 - 1.45	0.8	-	0.4	0.6	0.6
Power (nW)	**181**	**240**	920	130	4.7	110	75.6	190	280	35.4	1.14	45.3	14.4
Freq. Var. to VDD (%)	**±0.6 @ 0.65–0.8V**	**± 0.53 @ 0.7–0.9V**	±0.54@ 0.9–2.0V	<±0.25@ 0.95-1.05V	±0.14@ 0.85-1.4V	±0.23@ 1.2-1.8V	±0.27@ 0.6-0.9V	<±0.14@ 1.15-1.45V	±0.3@ 0.5–1.0V	±0.35@ 1.0–1.8V	4.3@ 0.4–0.65V	20@ 0.6–0.8V	7.2@ 0.6–1.8V
TC (ppm/°C)	**106 @ -20-80°C**	**33 @ -20-80°C**	96@ 0-145 °C	28~85@ -40-90 °C	13.8@ -25-85 °C	34.3@ -40-80 °C	144@ -20-80°C	38@ -20-90 °C	105@ -40-90°C	13.2@ -20-100°C	94@ -20-70°C	20.3@ -20-60°C	327@ -20-100°C
Allan Deviation Floor (ppm)	**12 (>100s)**	**12 (>100s)**	-	20(>100s)	63(>100s)	7(>12s)	60 (>100s)	4 (>2s)	-	<10 (>1s)	58(>3s)	300 (>100ms)	40 (>50ms)
Energy/Cycle (pJ/Cycle)	**0.43**	**0.57**	0.68	6.5	1.6	1.56	11.8	5.8	2.8	1.08	0.93	0.044	0.12
Area (mm^2)	**0.07**		0.005	0.032	0.5	0.26	1.08	0.015	0.12	0.16	0.2	0.098	0.03

(0.43 pJ/cycle) at a relatively low supply voltage and in a low area, while keeping on-par long-term stability and on-par stability over supply and temperature variations. This demonstrates that the proposed architecture is suitable for IoT applications requiring accurate ultra-low-power timers integrated in advanced CMOS processes.

REFERENCES

[1] S. Drago *et al.*, "Impulse-based scheme for crystal-less ULP radios," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 5, pp. 1041 – 1052, Feb. 2009.

[2] D. Ruffieux *et al.*, "A $3.2\times1.5\times0.8mm^3$ 240nA 1.25-to-5.5V 32kHz-DTCXO RTC Module with an Overall Accuracy of $\pm$1ppm and an All-Digital 0.1ppm Compensation-Resolution Scheme at 1Hz," in *IEEE ISSCC Dig. Tech. Papers*, 2016, pp. 208 – 209.

[3] S. Zaliasl *et al.*, "A 3 ppm $1.5\times0.8mm^2$ 1.0μA 32.768kHz MEMS-Based Oscillator," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 291 – 302, Jan. 2015.

[4] A. Paidimarri *et al.*, "An RC Oscillator with Comparator Offset Cancellation," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1866 – 1877, Aug. 2016.

[5] J. Koo *et al.*, "A Quadrature Relaxation Oscillator with a Process-Induced Frequency-Error Compensation Loop," in *IEEE ISSCC Dig. Tech. Papers*, 2017, pp. 94 – 95.

[6] A. Savanth *et al.*, "A 0.68nW/kHz Supply-Independent Relaxation Oscillator with $\pm0.49\%$/V and 96ppm/^{o}C Stability," in *IEEE ISSCC Dig. Tech. Papers*, 2017, pp. 96 – 97.

[7] M. Choi *et al.*, "A 110nW Resistive Frequency Locked On-Chip Oscillator with 34.3ppm/^{o}C Temperature Stability for System-on-Chip Designs," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2106 – 2118, Jun. 2016.

[8] J. Lee *et al.*, "A 4.7MHz 53μW Fully Differential CMOS Reference Clock Oscillator with 22dB Worst-Case PSNR for Miniaturized SoCs," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 106 – 107.

[9] T. Jang *et al.*, "A 4.7nW 13.8ppm/^{o}C Self-Biased Wakeup Timer Using a Switched-Resistor Scheme," in *IEEE ISSCC Dig. Tech. Papers*, 2016, pp. 102 – 103.

[10] D. Griffith *et al.*, "A 190nW 33kHz RC oscillator with$\pm0.21\%$ temperature stability and 4ppm long-term stability," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 300 – 301.

[11] H. Wang *et al.*, "A Reference-Free Capacitive-Discharging Oscillator Architecture Consuming 44.4pW/75.6nW at 2.8Hz/6.4kHz," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1423 – 1435, Jun. 2016.

[12] T. Tokairin *et al.*, "A 280nW, 100kHz, 1-cycle start-up time, on-chip CMOS relaxation oscillator employing a feedforward period control scheme," in *IEEE VLSI Symposium*, 2012, pp. 16 – 17.

[13] F. Sebastiano *et al.*, "A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1544 – 1552, Jul. 2011.

[14] S. M. Kashmiri *et al.*, "A scaled thermal-diffusivity-based 16 MHz frequency reference in 0.16 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1535 – 1545, Jul. 2012.

[15] J. Jung *et al.*, "A 1.08-nW/kHz 13.2-ppm/^{o}C Self-Biased Timer Using Temperature-Insensitive Resistive Current," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2311 – 2318, Aug. 2018.

[16] H. Jiang *et al.*, "A 0.4V 0.93-nW/kHz Relaxation Oscillator Exploiting Comparator Temperature-Dependent Delay to Achieve 94-ppm/^{o}C Stability," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 3004 – 3011, Oct. 2018.

[17] P. M.-Y. Fan *et al.*, "A 0.98nW/kHz 33kHz Fully-Integrated Subthreshold-Region Operation RC Oscillator With Forward-Body-Biasing," in *IEEE ESSCIRC*, 2019.

[18] D. Truesdell *et al.*, "A 0.6-V 44.6-fJ/Cycle Energy-Optimized Frequency-Locked Loop in 65-nm CMOS With 20.3-ppm/^{o}C Stability," *IEEE Solid-State Circuits Letters (SSCL)*, vol. 2, no. 10, pp. 223 – 226, Oct. 2019.

[19] S. Dai *et al.*, "A 14.4 nW 122KHz Dual-phase Current-mode Relaxation Oscillator for Near-zero-power Sensors," in *IEEE CICC*, Sep. 2015, pp. 1 – 4.

[20] . Grleyk *et al.*, "A CMOS Dual- RC Frequency Reference With $\pm$200-ppm Inaccuracy From -45 ^{o}C to 85 ^{o}C," *IEEE J. Solid-State Circuits*.

[21] M. Ding *et al.*, "A 0.8V $0.8mm^2$ Bluetooth 5/BLE Digital-Intensive Transceiver with a 2.3mW Phase-Tracking RX Utilizing a Hybrid Loop Filter for Interference Resilience in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2018, pp. 446 – 447.

[22] J. Yin *et al.*, "A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2018, pp. 450 – 451.

[23] M. Ding *et al.*, "A 0.7-V 0.43-pJ/cycle Wakeup Timer based on a Bang-bang Digital-Intensive Frequency-Locked-Lopp for IoT Applications," *IEEE Solid-State Circuits Letters (SSCL)*, vol. 1, no. 2, pp. 30 – 33, Feb. 2018.

[24] M. Ding *et al.*, "Ultra-Low-Power Clock Generation for IoT radios," in *Advances in Analog Circuit Design workshop*, 2018.

[25] D. Liu *et al.*, "A Frequency-Based Model for Limit Cycle and Spur Predictions in Bang-Bang All Digital PLL," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 6, pp. 1205 – 1214, Jun. 2012.

[26] S. Pavan, R. Schreier, and G. C. Temes, *Understanding delta-sigma data converters*. John Wiley & Sons, 2017.

[27] W. J. Riley, "Handbook of frequency stability analysis," in *NIST SP 1065, US Department of Commerce, National Institute of Standards and Technology*, 2008.

[28] R. Staszewski *et al.*, "Event-driven Simulation and modeling of phase

noise of an RF oscillator," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 4, pp. 723 – 733, Apr. 2005.
[29] F. Sebastiano, L. J. Breems, and K. A. Makinwa, *Mobility-based time references for wireless sensor networks*. Springer Science & Business Media, 2013.
[30] I. Lee *et al.*, "A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 697 – 711, Feb. 2016.
[31] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585 – 1595, Jul. 2011.
[32] B. Miller and R. J. Conley, "A Multiple Modulator Fractional Divider," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 578 – 583, 1991.

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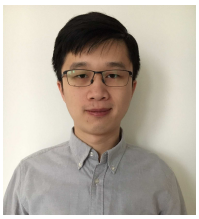
His research has resulted in 1 book, 2 book chapters, 6 patents and over 20 technical publications.



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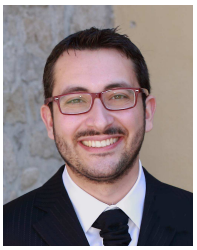

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