Thermally Driven Sound Source: Application of CNT nanofoams

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Challenge the future

THERMALLY DRIVEN SOUND SOURCE: APPLICATION OF CNT NANOFOAMS

by

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ABSTRACT

This thesis project focuses on the development and characterization of robust, scalable, cleanroom compatible thermally driven sound sources using novel 3D architectures of carbon nanotube (CNT) foamy material. We employ micro-fabrication technology to produce a thermoacoustic (TA) device with a clear advantage over conventional sound sources. Acoustic devices occupy a large market which includes smart electronics (smart watch, phone, laptop, etc.), car audio systems, home audio systems, earphones, ultrasonic applications (medical, underwater), wave field imaging and directional sound systems. Conventional acoustic devices contain mechanical and magnetic components. These traditional devices have a complex structure which require assembly. This complexity forms obstacles for miniaturization, integration and thus cost reduction. However, thermoacoustic devices offer a potential solution due to their simpler structure, wide spectrum response and their compatibility with cleanroom micro-fabrication. It is mechanical and magnetic free and doesn't require multiple part assembly. Moreover, the production process of TA devices is extremely scalable when using cleanroom micro-fabrication technology. Hence, TA technology can lead to high performance and low cost acoustic products.

Research work of TA devices nowadays mainly suffer from a lack of robustness, low power efficiency, incompatibility with cleanroom fabrication. On chip grown CNT nanofoam has a large surface to volume ratio and excellent thermal electrical properties, which is suitable to be used as a thermoacoustic heater. In our proposed technology, CNT nanofoams are anchored by top and bottom metal layer and patterned in hexagonal structures which improves the robustness. The highly porous foam exchanges heat with surrounding air efficiently. Every processing step is specifically designed to be CMOS compatible using cleanroom micro-fabrication. This design is expected to be a novel, robust, efficient TA device. All the advantages allow massive, parallel production, miniaturization and integration.

Chapter 1 starts with a short description of the historical development of speakers. Focusing on the cutting edge novelty of thermoacoustic sound sources with tremendous advantages and basic physics of thermoacoustics. Chapter 2 discusses state-of-the-art designs based on CNTs, their advantages and disadvantages, based on which the motivation of our design are determined. Chapter 3 gives the details of our new design with CNT nanofoam, and motivations for certain material and structural considerations. COMSOL Multiphysics simulation is used to assist and analyze the design before fabrication which is discussed in Chapter 4. The fabrication process and its challenges are described in chapter 5. The fabrication results are analyzed using scanning electron microscopy. In Chapter 6, measurement and characterization results are analyzed. Chapter 7 concludes the thesis work and an outlook for potential future work.

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1

INTRODUCTION

Before any form of electrical speakers are invented, horns were the earliest equipment for audio amplification. The horns occupied the market for more than 40 years until a good performance standard electrodynamic loudspeaker was first built in the 1920's. To improve the sound performance, electrostatic loudspeakers are invented in the 1960's. And more close to the present day, distributed mode loudspeaker is designed in 1990's. Figure 1.1 shows the historical development of commercial speakers.

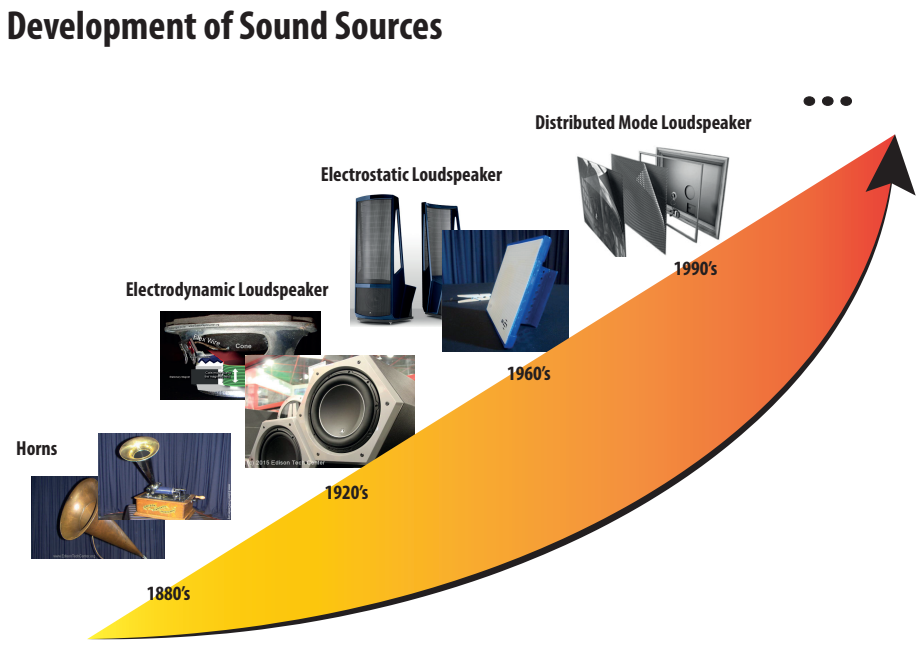


Figure 1.1: The development of sound source, starting from late 19th century till now very little improvments are made in the sound source industry, nowadays people still rely on the old inventions.

Electrodynamic loudspeakers which are widely used nowadays in various audio systems, sound boxes and headphones, after replacing the horns, have ruled the market for more than 90 years. Other type of designs like electrostatic loudspeaker, flat panel electrostatic loudspeaker and DML (distributed mode loudspeaker) joined the market afterwards but never beat the electrodynamic ones. During all these years, only

improvements over the design are made for the electrodynamic loudspeakers, the fundamental physics stays the same. The fact that a speaker is consist of a movable diaphragm and permanent magnet has not been changed. Especially when in need of a certain loudness, the loudspeakers used are usually heavy and bulky. As shown in Figure 1.2, loudspeakers/headphones nowadays are formed by multiple parts. To improve the performance, extra acoustic architecture are added.

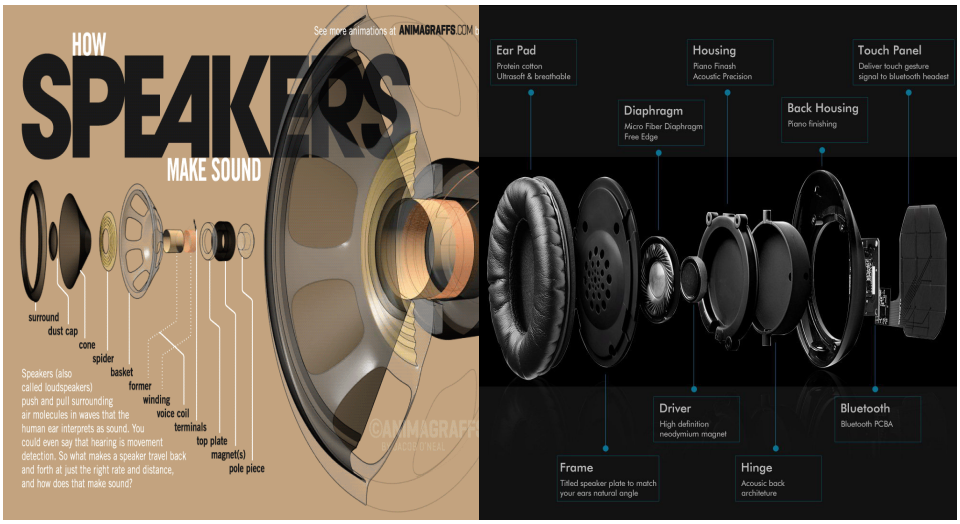


Figure 1.2: An anatomic view of speaker and headphone, the latest designs of bluetooth headphones still employs electrodynamic acoustic drivers.[1, 2] Thermoacoustics sound source can be potentially integrated on to a chip with other electronics.

Modern acoustic engineers are looking for a loudspeaker which can be light, small size, magnet free and at the same time provide high quality sound and sufficient loudness. For reproducing good quality sound, both low and high frequency are important. Some commercial hifi system use multiple drivers and cross-circuit to amplify separately the low and high frequencies of the audio signal to obtain a excellent performance. For low frequencies, a woofer is used and while for high frequencies, a tweeter is used. Most of the sounds we hear in our daily lives fall in the lower range of audible frequencies, however sounds from 16,000 to 20,000 Hz give us other information, such as the environment type. If someone is speaking in a small room or auditorium we can tell because of the high frequencies. Developing a speaker which could reproduce a wider band of frequencies equally or even possible to tune was the greatest final challenge in inventing all speakers.

Around the beginning of 20th century when everyone was looking for new designs to substitute horns, except the mainstream electrodynamic loudspeakers, other novel designs like plasma loudspeaker and thermo-phones as well arose [3]. Both the "Talking arc" and thermo-phones work under principles which are different from those of the electrodynamic or electrostatic loudspeakers. No moving diaphragm nor magnet is required. The electrical energy is converted into acoustic energy through discharging arc or thermal effect. The "Talking Arc" is more of an art than practical application, since the high voltage required is unsafe to human beings. On the other hand, thermo-phones, which is called thermoacoustic sound sources nowadays, have no such safety issue, the concept is to heat up air very quickly and create pressure waves. Due to the limited material choices and technologies at that time, prototypes of thermo-phones were not successful. Starting from the 1960's, micro-technology became a taking-off industry and dramatically changed human society for decades. But the idea of applying micro-technology to loudspeakers has not yet made it to any success nor widely attempted. The ideal loudspeaker with features such as light in weight, miniaturization, high performance and potentially with novel properties, for examples flexible, thin film, transparent, can all be possible with MEMS and NEMS fabrication technologies.

Acoustic devices still occupy a large market share in a wide variety of fields nowadays ranging from; smart

phones, laptops, earphones, car/home audio-systems towards ultrasonic applications for medical purposes and underwater detections. Conventional acoustic devices have a complex structure containing mechanical and magnetic components which are rather bulky and require assembly. It forms an obstacle for miniaturization, integration and therefore cost reduction. Thermoacoustic effect is a potential driver for the revolutionary development of next generation sound sources. Comparing with the conventional electrodynamic loudspeakers, using thermoacoustic effect for sound generation have clear advantages. Inside a working thermoacoustic sound source, there is no moving diaphragm. Diaphragms are normally fragile, thus the device theoretically has an improved robustness. Since the sound wave is not produced by mechanical movement, no voice coil nor magnet is needed. In such a way, thermoacoustic loudspeakers have simple structures, magnetic free, requires no assembly after fabrication and potentially compatible with micro-processing on wafer scale. The recent development of micro-fabrication and materials have sparkled a renewed interest in the thermoacoustic loudspeaker. Thermoacoustics is going to open an era of fabricating loudspeaker on chips.

1.1. LITERATURE REVIEW OF THERMOACOUSTICS

The first observation of the thermoacoustic effect goes back to the 18th century when the glassblowers discovered sound emission from a tube which is attached to a hot bulb. This phenomenon was later found to be thermoacoustic oscillation [4, 5]. Many studies have worked on the thermoacoustic oscillations to construct engines or refrigerators [6]. In 1917, the first thermoacoustic device to serve as a loudspeaker is designed by H. D. Arnold and B. Crandall [7]. The thermo-phone, as they called it, is formed mainly by a 0.7 um thin platinum strip, and driven by alternative electric current. Before their time, research work are mostly qualitative analysis, and there was a desire of developing quantitative theory for the thermoacoustic effect. In Arnold and Crandall's work, early mathematical calculations are done. In their work, the temperature distribution in time and space is derived as well as the sound pressure distribution both under an open air condition and closed medium of which the size is within one wave length. Within the 20th century, there were more effort devoted into thermoacoustic engines and cryogenic systems than loudspeakers. The work of H.Shinoda published on *Nature* in 1999 combined thermoacoustic sound emission with micro-fabrication and novel porous silicon material [8]. The device produces ultrasound up to 100 kHz with a flat response from 10 kHz up. This finding brings thermoacoustic sound source back to the stage. The research of thermoacoustic sound emissions potentially as loudspeakers started to attract more interest since then. In Shinoda's work, the porous silicon thermoacoustic design was focused on ultrasonic emission, and until 2008 when a novel CNT thin film thermoacoustic loudspeaker was built [9], the application of thermoacoustic sound source started to shift to audio range, trying to beat a normal loudspeaker as well. Lin.Xiao, the designer of CNT thin film loudspeaker, introduces modifications to the thermoacoustic theory from year 1917 for modeling the nanotube thin film. The CNT thin film loudspeaker exhibits comparable performance to the electrodynamic ones. They demonstrate that their CNT loudspeaker can be flexible, stretchable and transparent. This just remind people of those years in the beginning of 20th century when a horn was about to leave the stage. Varieties of thermoacoustic loudspeaker designs emerges after 2008, including designs with Al suspended wires, Au nano wires, silver meshes, graphene, reduced graphene oxide(RGO), CNT thin yarns,CNT Sponge etc [10–16]. Other than the CNT thin film loudspeaker, the thermoacoustic designs with CNT thin yarns and RGO have been packed into headphone casings. Figure 1.3 shows the mile stones in the history of thermoacoustic sound source and the recent progress in researches.

In recent leading researches, CNT thin film, CNT thin yarn, graphene, metal wires, other conductive thin films are the main design trends. Among them, sound source designs which choose CNTs as the heater material for thermoacoustic actuation achieve higher SPL due to several novel properties of CNTs. Comparing

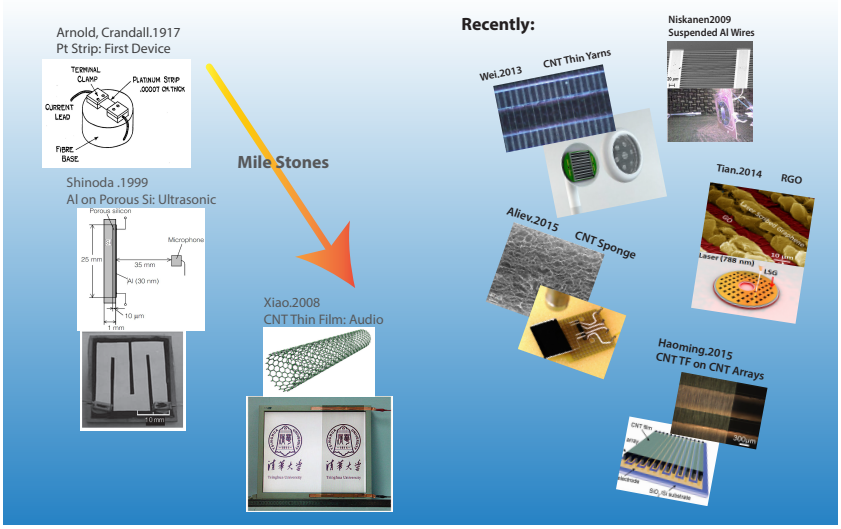


Figure 1.3: The Development of Thermoacoustic Sound Sources, the discovery of CNT thin film as thermoacoustic heater is the mile stone for recent development of thermoacoustic designs.

with other material choices, carbon nanotubes have large surface area to volume ratio(SA:V), micro/nano scale architecture [17], excellent thermal and electrical conductivity, extremely light in weight and ultra low thermal capacity [18]. A comparison between different heater materials is given in Table 1.1.However, designs relying on CNT thin films require extra steps to fabricate the thin film after CNT growth and extra steps to transfer CNT thin film to a desired substrate. Though stretchable, flexible and transparent, the free standing CNT thin film can be extremely fragile. Once the nanotubes are broken off, which seems to be easy, they will float in the air and become a threat to human health. The extra steps for producing CNT thin films makes the whole process less compatible with Si technology and massive fabrication.

1.2. PHYSICS OF THERMOACOUSTIC EFFECT

Thermoacoustics, studies the physics of sound waves that are stimulated by periodical temperature variations in the air. Temperature variations in the air result in pressure variations due to expansion and contraction of the air, which can be perceived as sound.

A device that can transfer energy from thermal source to an acoustic field is called thermoacoustic transducer. Specially, when a thermoacoustic transducer can work within the audio range, which means it has a reasonable frequency response from 20 Hz to 20 kHz, we can call it a thermoacoustic loudspeaker.

Sound is intrinsically pressure waves in air, more specifically it is the molecular density of air molecules variation through time and space. Conventional electrodynamic loudspeakers use a moving diaphragm to push air molecules to create such density waves. In a thermoacoustic loudspeaker, a heater becomes the driver instead. An ultra fast heat exchange between the heater and air can instantly change the kinetic energy of the molecules, a higher average level of kinetic energy of a volume with same molecular density as the rest of the system exhibits a higher pressure. Audible sound waves can be generated when a sufficiently fast and stable heat exchange happens with sufficient energy transfered into pressure waves. A flat wide band frequency response and a high energy efficiency are both critical to a thermoacoustic loudspeaker. Figure 1.4 shows the working principles of a TA device. A thermoacoustic loudspeaker system is mainly constructed with a heater and isothermal layer. When a AC current is passing through the heater, it heats up the surrounding air periodically. The heating cycles result in periodical expansion and contraction of air which generates air

Table 1.1: Performance of TA devices with different heater material, at normalized 1 W power and frequency of 3 kHz and measured at 3 cm distance. [16]

Comparison of Different TA Heater Materials					
Heater Material	P_{rms}(Pa)	SPL (dB)	Size(cm^2)	Efficiency	Reference
CNT sheet	0.117	75	25	1.7×10^{-5}	single-layer free-standing MWCNT sheet,D=10 nm
Graphene(1)	0.0045	47	2.25		three-layer graphene suspended on 80% porous PDMS
Graphene(2)	0.0028	43	6.25		three-layer graphene suspended on 80% porous PDMS
Graphene	0.0115	55	1.0	10^{-6}	20 nm thick graphene film on paper
PEDOT:PSS	0.0025	32		10^{-6}	100 nm PEDOT:PSS filmon PET substrate
ITO film	0.0028	57			100 nm ITO film on PET substrate
Al film on porous silicon	0.00235	41			30 nm thin Al film on 10 um porous silicon
Au film on porous polymeric	0.034	64			40 nm thin Au film on 14 um porous hydrogel substrate
Al film on polymide	0.0019	39.5			40 nm Al film on 75 um polymide substrate
Suspended metal wire array	0.035	65			3 um wide and 30 nm thick Al nanowires

pressure waves or sound.

For a conventional electrodynamic loudspeaker, the diaphragm movement completes one cycle when the signal runs through one cycle. In thermoacoustics, sound waves are a response of the heating cycle, therefore the frequency is doubled from the original signal, as shown in Equation (1.1). The principle is shown in the schematic below in Figure 1.5.

$$Power = RI^2 sin^2 \omega t = \frac{RI^2}{2}(1 - cos2\omega t) \tag{1.1}$$

One way to get rid of the double frequency effect is to superimpose a a DC current I_0 on top of the AC signal written as in Equation (1.2) below. As we can see from the equation, when a sufficiently large I_0 is chosen comparing to I', the double frequency term can be neglected.

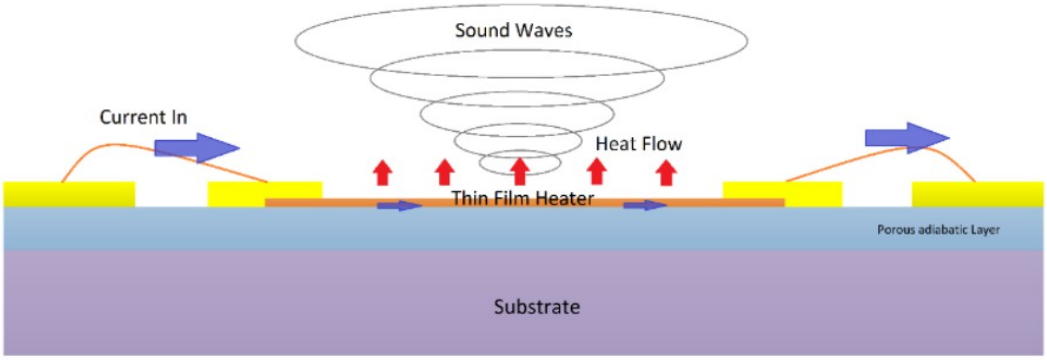


Figure 1.4: A simple schematic of the physics of thermoacoustics: Heat is generated by AC current and passed to the surrounding air causing pressure variation which is sound waves.

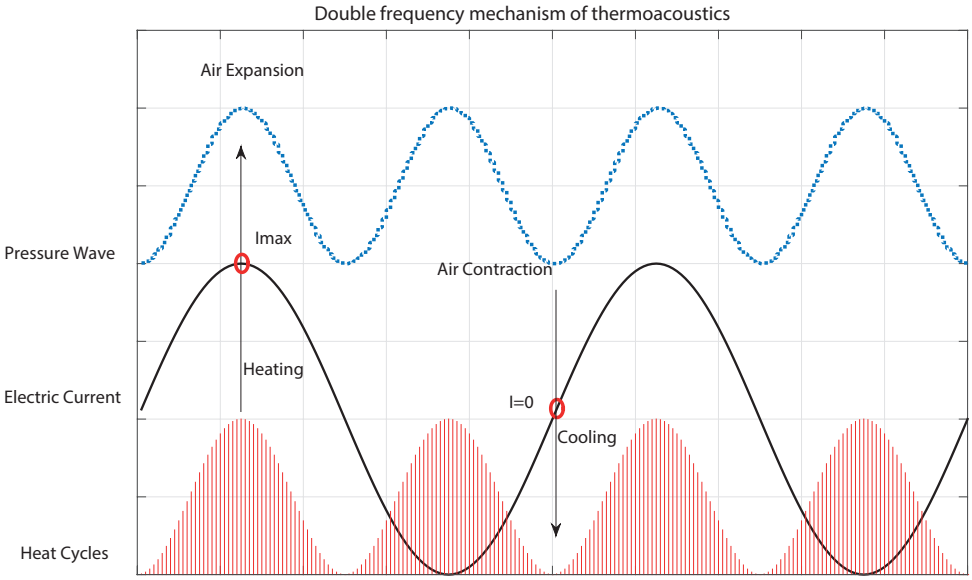


Figure 1.5: The mechanism of double frequency effect in thermoacoustics.

$$Power' = R(I_0 + I' sin\omega t)^2 = R(I_0^2 + \frac{I'^2}{2}) + 2RI_0 I' sin\omega t - \frac{RI'^2}{2} cos2\omega t \tag{1.2}$$

A thermoacoustic device which works under a superimposing DC current, the mean working temperature is determined by the DC power dissipated on the heater. For generating a pure single frequency signal, it is better to use a pure AC input signal which is half the demanded frequency. For a loudspeaker type of thermoacoustic sound source which is supposed to play speeches and music, either a converter for the signal or the DC current superimposition is in need to get rid of the double frequency effect.

Figure 1.3 is used to describe energy conservation between the electric input power and the heat that is generated. Since the heater is almost purely resistive, only R is taken into consideration. The energy that is induced by electrical heating can either dissipate through conduction convection and radiation or be stored by the thermal capacitance of the heater. Equation (3) was originally given by Arnold and Crandall, thus is suitable to describe a thin flat rectangular heater.

$$R(I_0 + I' sin\omega t)^2 = 2\alpha\beta T + \alpha\gamma \frac{dT}{dt} \tag{1.3}$$

α is the surface area of one side of the heater, β is the rate of heat loss per unit area of a thin film heater (due to conduction and radiation) per unit rise in temperature above that of its surroundings, and $\alpha\gamma$ is the heat capacity of the heater while γ equals to the product of the thickness of the thin film by the specific heat per unit volume.

For the CNT thin film thermoacoustic loudspeaker, the theory from Arnold and Crandall is no longer suitable due the difference between the heater material properties. Since the CNT thin film is formed by nanotubes with diameter of around tens of nanometers and the arrangement of the nanotubes are of low density thus high porosity, the thermal inertia which is considered as much larger than the thermal dissipation (conduction, convection, radiation) by Arnold and Crandall is then comparable and thus β should not be neglected for the CNT thin film TA loudspeakers. The calculation for the platinum stripe is modified by Xiao, et al. to make it suitable for the CNT thin film. Except keeping β in the equation, another parameter $Q_0 = -k\frac{\delta T(x,t)}{\delta x}|_{x=0}$ the instantaneous heat flow per unit area into the surrounding is introduced to the equation. The fundamental equation of energy conservation in electrical heating is given below in equation (4) in case of only AC signal applied,

$$(Isin\omega t)^2 R = 2\alpha\beta_0 T_f + 2\alpha Q_0 + \alpha c_s \frac{dT_f}{dt} \tag{1.4}$$

Following Equation (1.4), the root mean sound pressure is derived as Equation (1.5) below,

$$p_{rms} = \frac{\sqrt{\alpha}\rho_0}{2\sqrt{\pi}(T_0 + T_a)} \cdot \frac{1}{r} \cdot P_{input} \cdot \frac{\sqrt{f}}{c_s} \cdot \frac{\frac{f}{f_2}}{\sqrt{(1+\sqrt{\frac{f}{f_1}})^2 + (\frac{f}{f_2} + \sqrt{\frac{f}{f_1}})^2}} \tag{1.5}$$

The descriptions of various parameters used in Equation (1.4) and Equation (1.4) are given in the table. Unlike other sound generation techniques (coil loudspeakers, piezoelectric, magnetostrictive, and electromechanical transducers), the efficiency of TA projectors, η, is proportional to the applied power [19–21]:

$$\eta = \frac{\pi f^2}{\rho_g v_g C_p^2 T_0^2} P_h \tag{1.6}$$

It is can be understood that from equation Equation (1.6) that to achieve high efficiency, a TA device should work at high excitation frequencies and in the environment of gases with low heat capacity Cp (or high molecular weight).

Table 1.2: Parameters and constants used in Equation (1.4) and Equation (1.5)

Symbol	Definition	Unit
α	Surface area of one side of the thin film	m^2
β_0	the rate of heat loss per unit area of a thin film heater (due to conduction and radiation) per unit rise in temperature above that of its surroundings	W/m^2
T_f	Temperature of the thin film above its surrounding	K
Q_0	Instantaneous heat flow per unit area from thin film to surrounding	W/m^2
c_s	Heat capacity per unit area of thin film	$J/m^2 \cdot K$
ρ_0	Density of ambient gas	kg/m^3
T_0	Temperature of remote ambient gas(base temperature of the environment)	K
T_a	Mean temperature of the thin film above its surrounding	K
r	Distance to the measuring location of a microphone	m
p_{rms}	Root mean square sound pressure	Pa
P_{input}	Electric input power	W
f	Frequency of the input signal	Hz
f_1	Mathematical parameter, $f_1 = (\alpha\beta_0^2)/(\pi\kappa^2)$	
f_2	Mathematical parameter, $f_2 = \beta_0/\pi c_s$	
κ	Thermal conductivity of gas	$W/m \cdot K$

1.3. THESIS OBJECTIVES

In this research work a novel thermoacoustic device is designed for sound generation using advanced carbon nanotube based nanofoam material. The ultimate goal is to create the next generation sound source which can replace the traditional electrodynamic sound source. To start with, this research work is arranged to explore a new design concept for achieving better thermoacoustic efficiency and a method to make the device compatible with micro-fabrication and mass production. The objectives of the thesis project are shortly summarized below:

- Design a thermoacoustic device with improved audio performance, compared to state-of-the-art thermoacoustic designs, which is suitable for mass production.
- Develop an efficient CMOS compatible micro-fabrication approach using standard processing techniques.
- Thermoacoustic device fabrication, based on the proposed design and experimental characterization of the performance.

2

STATE OF THE ART

As originated from 1900s', thermoacoustic is an old technology. However, the application as general sound source is a modern development. An important milestone is the CNT thin film design of Xiao, etc. in 2008. The state of the art TA designs since then can be sorted into 3 categories, 1),CNT based, 2),Graphene based, 3),Other thin film/wire based. They will be discussed separately in the sections below.

2.1. CNT BASED TA DESIGNS

CNT based TA designs includes CNT thin film/yarn, single suspended CNT, CNT Sponge and CNT forest. CNT thin film/yarn with its unique properties for efficient thermoacoustic emission is most popular among others [9, 10, 22–24].

CNT thin films can be drawn out of aligned CNT arrays from the substrate [25]. The drawn-out CNT thin film has width up to 10 cm (diameter of 4 inch wafer) and is composed of nanotubes around 10 nm in diameter as shown in Figure 2.1. The typical mass per unit area is reported as 1.5 $\mu g/cm^2$ for 550 nm thick single-layer CNT thin film, the transparency is 78% accordingly. Such drawn out CNTs thin film has sheet resistance around $1k\Omega/\square$ for a single-layer. It is claimed in Xiao's work that the ac impedance of a CNT thin film is purely resistive within 1 MHz bandwidth. They have shown that CNT thin films can be assembled into larger area, tailored into various shapes, covering curved surfaces and stretched up to 50%. To achieve clear and loud tones, 50 $V_r ms$ sine wave input is fed to the unoptimized CNT film device at a power as high as 12 W.

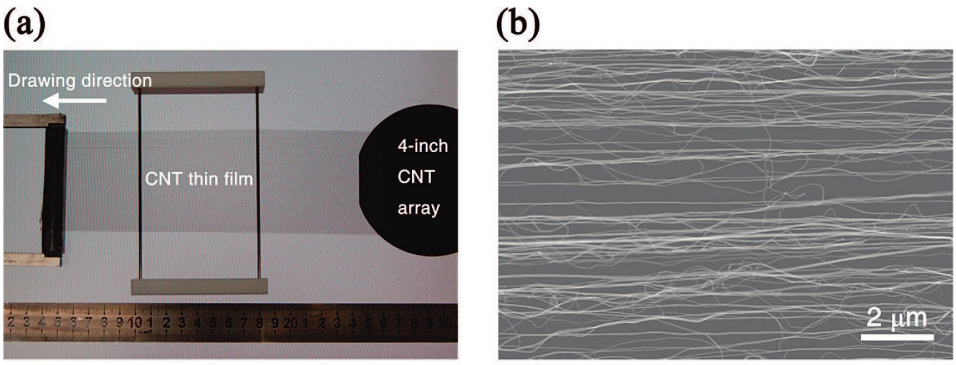


Figure 2.1: CNT thin film design [9], drawing and handling the CNT thin film is a difficult and delicate process which is not suitable for mass-production.

As an optimization of the original CNT thin film TA design, CNT thin yarn chips achieve an wafer level fabrication as shown in Figure 2.2. Yarns are obtained by laser patterning and ethanol atomization bath of CNT thin film which is transfered on to a target wafer. Firstly, CNT strips are obtained by a focused laser beam, 30μm in width and 120μm in pitch. These stripes shrined down to 1μm diameter yarns after atomization bath. Periodic grooves are etched to ensure the suspension of CNT thin yarns for the purpose of thermal isolation. The grooves are 600 μm wide and pitch is 900 μm. The depth of the grooves is varied to inspect the influence on acoustic emission. It is then observed that the groove depth has an effect on the sound pressure that is generated. The reason for this phenomenon is explained as the dependence of heat dissipation on the groove depth. Inter-digital electrodes are used in the CNT thin yarn design to lower the resistivity of the whole component thus a lower driving voltage is possible. The micro chips are in the end assembled into earphones.

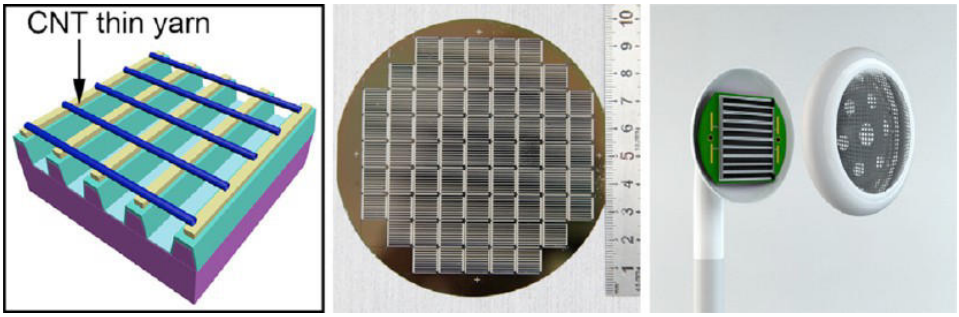


Figure 2.2: CNT thin yarn design [10], fabrication of CNT thin yarn requires transfer of CNT thin film, laser patterning and atomization which is not efficient and low scalability.

In 2015, CNT thin film is transfered onto laser patterned CNT arrays to construct a TA chip [24]. The CNT thin film is suspended by the support of parallel aligned CNT arrays. The patterned CNT arrays also act as electrodes to connect the CNT thin film with the gold inter-digital contact pads. The patterns are made after a whole piece of aligned CNTs is transferred to the target substrate by a focused laser beam. These aligned CNTs are patterned into stripes which are 15 mm in length, 300 μm in width, and 900 μm in pitch. The CNT strip arrays are aligned with the gold pads underneath. A thermoacoustic chip was accomplished by finally coating a 10 mm wide CNT film on the pattern, as shown in Figure 2.3 below.

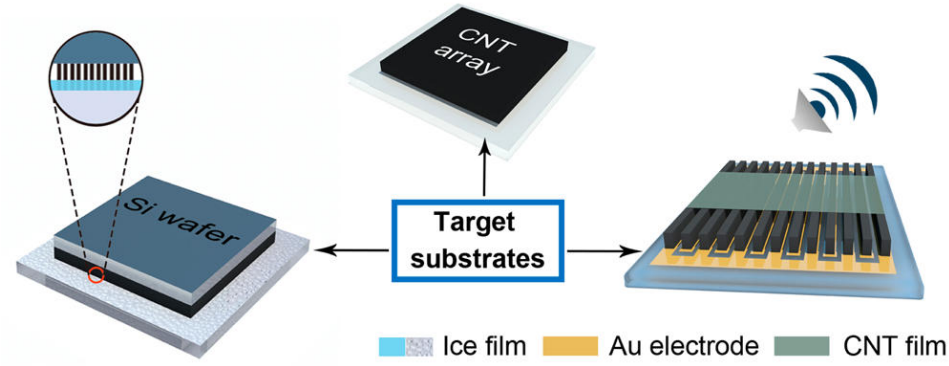


Figure 2.3: CNT thin film over laser patterned CNT arrays [24], extra complexity of fabrication with ice transfer, still lack ability of scaling down and mass-production.

Suspended individual CNT is under research [26] of its ability for thermoacoustic emission as well. Such individual suspended CNT component is claimed to be the smallest thermoacoustic system. The CNT applied in the system is approximate 2 μm long, 1 nm in diameter shown in Figure 2.4. By applying an AC voltage of 1.4 V_{rms} at 16 kHz to the component, an rise of 23 nV output voltage of the microphone (Rode NT1-A) is detected over a time span of 50 seconds. As the author addressed, 23 nV is equivalent as -28 dB in SPL due to the sensitivity of the microphone is 32 mV/Pa. This observation is taken as the evidence of an acoustic emission from the individual CNT. However, this conclusion is not sufficiently convincing, since Rode NT1-A has a noise level at 5 dB.

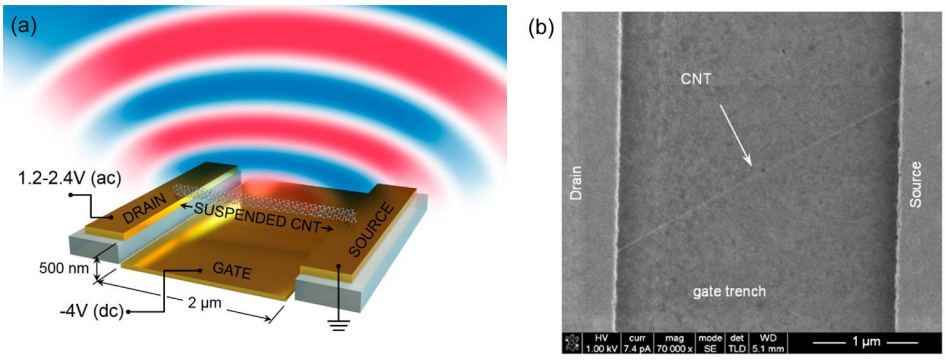


Figure 2.4: Single suspended CNT TA device [26] is scientifically the smallest acoustic unit measured, however not suitable for consumer application.

2.2. GRAPHENE BASED TA DESIGNS

Graphene is used as a sound emission component due to its ultra-low heat capacity per unit area (HCPUA). The electrical mobility of single layer graphene (SLG) is about 200000 cm^2V^{-1} s^{-1} at room temperature for both carriers [27]. Due to its unique crystal structure and high carrier mobility, the thermal conductivity of graphene is as high as 5000 $m^{-1}K^{-1}$. Filter papers with aperture of 30 to 50 um[14] and anodic aluminum oxide (AAO) [27] are used as the substrate. Single layer graphene on AAO thermoacoustic device is reported to be able to produce a 95 dB high SPL at a distance of 5 cm with a sound frequency of 20 kHz, 1W input power. In Tian's work, the frequency range of 20 - 50 kHz is highlighted, however the audio range is not discussed in detail.

Other than single layer or multilayer graphene, reduced graphene oxide (RGO) also become an candidate for thermoacoustic sound production [15]. Compared to the approach of using graphene layer obtained by

CVD growth, the fabrication of laser-scribed graphene (LSG)is time saving and low cost. Graphene oxide nano-powder is dispersed in water to make the precursor. After the laser exposure, the graphene oxide is reduced and polycrystalline graphene flakes are formed. These polycrystalline graphene lines are porous, air gaps exist in between the flakes. This unique property increases the SA:V of the material and forms a higher thermal resistance towards the substrate. The electrical resistance has been reduced by 5 orders of magnitude after the laser scribing, from 580 $M\Omega$ to 8.2 $k\Omega$, as reported. The RGO thermoacoustic device is assembled into a earphone, and the performance is compared with commercial earphone, shown in Figure 2.5 below.

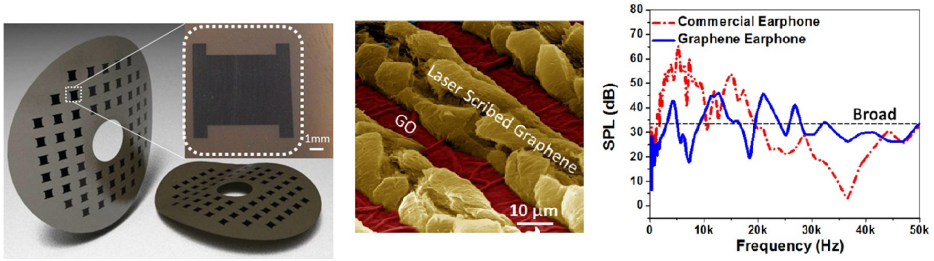


Figure 2.5: TA design with reduced graphene oxide [15]. Large peaks exits in the SPL frequency response. Fabrication requires laser scribing which is not suitable for mass-fabrication.

2.3. OTHER THIN FILM BASED TA DESIGNS

Other thin film/wire that are recently explored are Al wire, silver mesh, Indium Tin Oxide (ITO), gold nanowire, PEDOT:PSS, Ag/Pd-glass-alumina sandwich layer [11–13, 28–30]. Among them, silver mesh, ITO and PEDOT:PSS are candidates to make transparent thermoacoustic sound source over screens. Their performance is relatively poor, the achieved SPL is relatively low at normalized power of 1 W. The thermoacoustic design with suspended Al wires shows high dependence of SPL on frequency. The response is linear in the range of 40 kHz wide band. The device is on a full 4 inch wafer, with 233200 Al wires. These wires are 200 μm in length, 3 μm wide and 30 nm thick. It is driven by nearly 10 W power including DC and AC.

3

Design Approach for CNT Nanofoam Devices

3.1. Introduction

In this chapter we will first discuss the CNT material properties in Section (3.2). The thermal and electrical properties of CNT nanofoam material have a considerable influence on the thermoacoustic device performance. In Section (3.3) we discuss the limitations of the CNT process. Combined the previous sections will determine the geometrical design consideration that are made in Section (3.4).

3.2. Material Considerations for TA Sound Source

CNTs have made excellent achievements and attracted a growing interest mainly due to its ultra low HCPUA. Metal wire arrays are limited by its porosity and surface to volume ratio, the ability to define pitches, wire width and make them suspended can improve the SA:V, however it is still no competition to CNTs. Graphene layer although possess ultra low HCPUA just like CNTs, it lacks porosity and more importantly the ability to be patterned and scaled down. Graphene oxide can be reduced to graphene flakes by laser exposure. It is not compatible with lithography, weak adhesion to substrate and challenging to make suspended structures. In conclusion, CNT based materials are the most promising option for thermoacoustic sound sources. Recent thermoacoustic designs based on CNTs mostly employ the CNT thin film or derivations of CNT thin film, like CNT thin yarns, as the heater. These designs give extraordinary thermoacoustic emission because of the materials' high porosity and low thermal capacity. After being drawn out from a wafer, CNT thin films are even more porous than aligned grown CNTs. It possesses ultra low HCPUA, which is the major advantage over other materials. However, the fabrication and transfer of CNT thin films are less compatible with microchip fabrications. CNT thin film is known to be fragile, the nanotubes are easy to break off from the film which makes the device less reliable and could become a threat to human health.

To get rid of above shortcomings, we choose as-grown CNT nanofoam as heater material to design a vertical heating system to avoid the use of CNT thin film. CNT nanofoam possess the same advantages like high porosity [34] and ultra high thermal conductivity. And the fabrication process of our proposed design requires no transfer of CNTs. Thus the vertically aligned CNT nanofoam is the suitable and valuable option for our design.

Table 3.1: Comparison of heater material properties

Material Properties				
Material Options	Dimension	Thermal conductivity (W/(m·K))	Electrical conductivity (S/m)	Porosity
CNT	10 to 30 nm diameter	3000~950 [31]	2×10^7 ~ 16.7 [32]	high
Graphene	10nm thick	5000 [33]	1×10^8	none
Al	30nm thinck, 3um wide	237	35.5×10^6	none
Ag		429	61.6×10^6	none
Gold	100nm	318	45.6×10^6	none
RGO	5um			good

3.2.1. CNT ARRAY STRUCTURE

According to the number of walls CNTs are sorted into SWCNT, Double-Walled Carbon Nanotubes (DWCNT) and MWCNT. Beside the number of walls, other parameters of interest are the tube diameter, chirality, length, quality and bundles density or porosity. Carbon nanotubes are simply wrapped graphene sheet. Fullerene also known as bucky ball, is a zero dimensional carbon material while CNT is 1D and graphene is 2D carbon material as shown in Figure 3.1

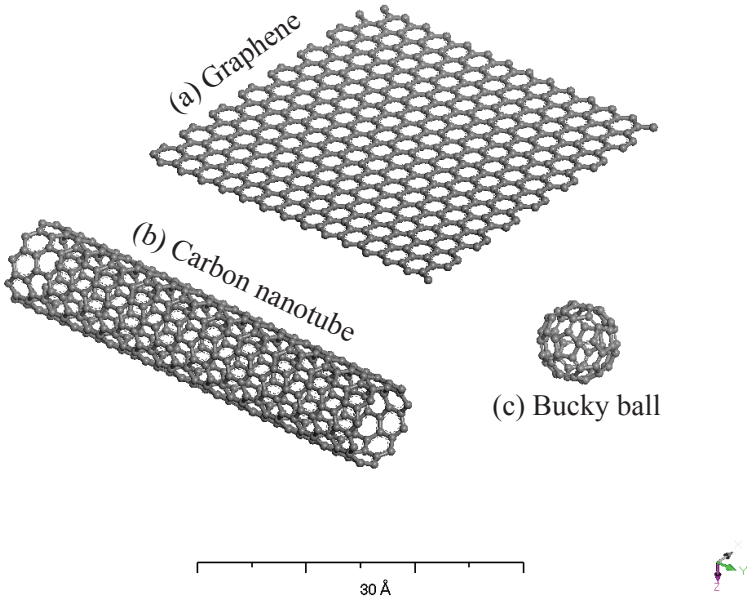


Figure 3.1: (a) Illustration of graphene showing a single layer of carbon atoms in a honeycomb lattice, the material is considered to be two-dimensional (2D). Multiple layers of graphene stacked is called graphite. (b) The rolled up version of the single or multilayer graphene sheets are called single- or multiwall carbon nanotubes, respectively, and they are considered to be 1D. (c) The last example shows a Buckminsterfullerene C60 which is considered to be a 0D material

Among above parameters, chirality and quality are important for the thermal and electrical properties of CNT. Chirality of the CNT determines whether it is metallic or semi-conductive. It is defined by the chiral vector C_h and its indexes (n,m). It expresses how the graphene layer is rolled-up to form the tube compared

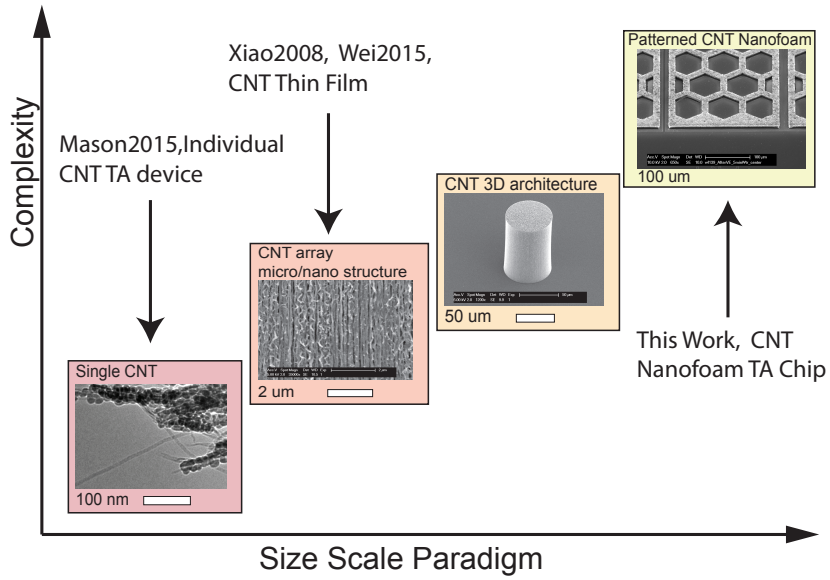


Figure 3.2: The scale and complexity regarding CNT based TA device

to the unit vectors of the graphene unit cell. The rolling up of the graphene sheet changes the band structure of the CNT and thus its electrical properties are altered [35]. In case that a CNT has chiral indexes where n = m (armchair) the tube is metallic. When $n - m = 3i$, the tube is semi-metallic with a bandgap of a few meV, i is a non-zero integer. In any other circumstances the nanotubes are semiconductor, with its diameter determining the bandgap.

The quality of CNT is used to describe how well the crystallinity is. Unlike chirality, there is no vector nor factor to evaluate the quality of CNT. A simple straight forward expression of high or low quality is generally addressed. Quality can be investigated by Transmission Electron Microscope (TEM), but TEM is generally expensive, the process is time consuming and the results are highly dependent on the viewed area. In our project, Raman spectroscopy is preferably used, which is time saving (measurements generally take just tens of seconds to a few minutes), non-destructive and low cost. To determine the crystal quality using Raman spectroscopy mostly used is the intensity ratio between the D-band and G-band. The D-band is defect related and peak around 1350 cm^{-1} while G-band represents Raman active mode of graphitic materials and the peak is around 1582 cm^{-1}.

MWCNT can be grown in vertical aligned arrays. Multiple wall nanotubes have diameters vary from ~10 nm to ~100 nm. These aligned CNT arrays are conductive along the tube axis direction and has very low conductivity along the lateral direction. As shown in Figure 3.2, thermoacoustic sound sources are explored with single CNT and CNT thin film arrays which are both on a low complexity. In this work, we proposed a thermoacoustic deign with patterned 3D architecture arrays that has higher complexity on the large scale.

3.2.2. ELECTRICAL PROPERTIES OF CNTS

Carbon nanotubes are well known of its super electrical properties: super high carrier mobility and current density [36]. SWCNTs have have a carrier mobility of 10,000 $cm^2V^{-1}s^{-1}$, which is nearly an order of magnitude higher than silicon (1,000 $cm^2V^{-1}s^{-1}$), and the maximum electrical current density it can be loaded with is up to $4x10^9$ A/cm^2, which is three orders of magnitude higher than a typical metal, such as copper or aluminum. MWCNTs are composed of multiple shells of SWCNTs, typical spacing between shells is approximately 0.34 nm [37], it is similar to the case of carbon layers in graphite. The energy gap between shells result in poor conductivity laterally at room temperature and thus MWCNTs can be still considered as 1D conduc-

tors. For bundles of MWCNTs, the maximum current density allowed is found to be 9 MA/cm^2 [38]. The difference between this value and that of the SWCNT is due mainly to the existence of defects in MWCNTs and density of tubes in the bundle regarding to certain process for growth. We have applied the same process of growing CNTs with LPCVD as in Ref.xx, the resistivity of MWCNT bundles are given in Figure 3.3 below,

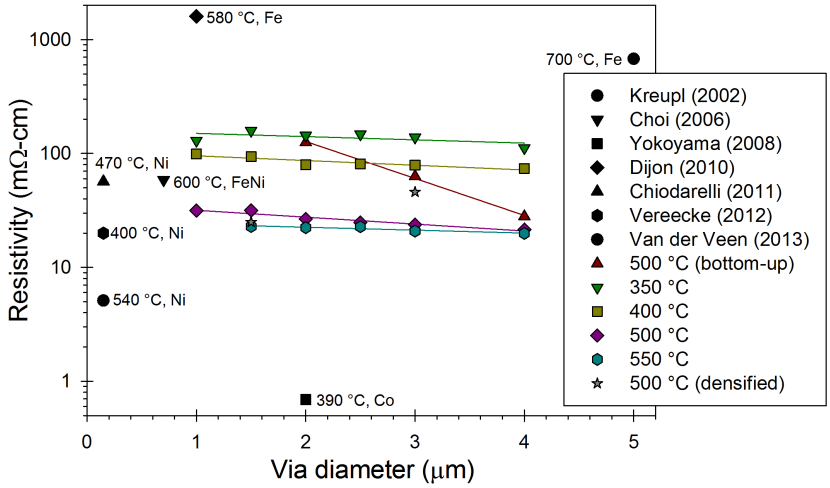


Figure 3.3: Resistivity of bundles obtained at different temperature and catalyst [38].

The measured resistivity of CNT bundles in Vollebregt's work regarding different temperature with Fe (500°C and 550°C) and Co (350°C and 400°C) indicates that CNTs that are grown at 550°C with Fe catalyst have the best electrical conductivity and are less dependent on the size of the bundle. Fe yields better uniformity of the conductivity of CNTs across different temperatures, especially with larger scales of bundle. The metal Co on the other hand produces CNTs which are an order of magnitude more resistive than the ones produced with Fe, and a gap of resistivity between 350°C and 400°C is observed.

3.2.3. THERMAL PROPERTIES OF CNTS

The specific heat and thermal conductivity of CNTs are determined primarily by acoustic phonon [35], unlike metals which are dominated by electrons. The strong sp^2 bonds between carbon atoms give SWCNTs thermal conductivity along axis as high as 6600 W/mK at 300 K [39], theoretically. According to the measurement of suspended single MWCNT [40], the observed thermal conductivity was more than 3000 W/mK at room temperature. The thermoelectric power plot can tell which type of the carrier is dominating. As shown in their measurement, the MWCNT is dominated by holes as indicated by the plus sign of voltage. Since holes are the carriers for electrical conduction in metallic MWCNTs, free electrons are not the majority, and thus the heat conduction is mainly through phonon as mentioned before.

3.2.4. POROSITY OF CNT NANOFOAM

The porosity of CNT nanofoam can be calculated using the density of tubes per unit area and the tube diameter. From high resolution SEM images we determine the number of CNTs per unit area, which gives a density of 10^{10} cm^{-2}. The diameter of a single CNT is about 9 nm.

In Figure 3.4, SEM images of compressed CNT nanofoam bundles are shown. The first row shows bundles with 100 μm, 80 μm and 60 μm diameters were compressed 25%, 20% and 17% respectively and the second row shows bundles with 50 μm, 40 μm and 30 μm diameters were compressed 80%. As grown CNTs bundles have been shown able to be compressed by 80% [34].

$$Porosity = Area\ (cm^2) * Density\ (cm^{-2}) \tag{3.1}$$

$$Area = \pi \frac{D_{cnt}{}^2}{2} \tag{3.2}$$

For CNTs grown with 5 nm Fe catalyst, which is our case, the related carbon nano tube diameter is nearly 30 nm and the density is in the range of 10^{10} cm^{-2}, thus the calculated porosity is in value of 93% which is still very high and the distance between individual nanotubes is around 70 nm. The porosity of the CNT nanofoam can be calculated using Equation (3.1) and Equation (3.2).

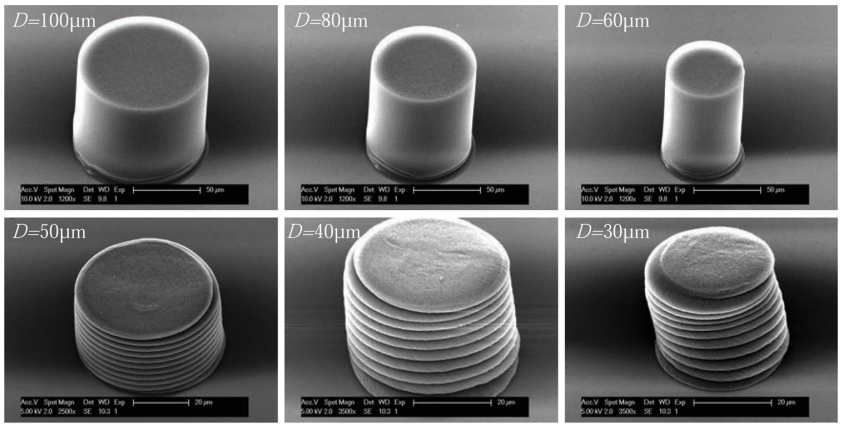


Figure 3.4: SEM images of compressed CNT nanofoam in different diameters [34].

3.3. LIMITATIONS OF CNT GROWTH ON TIN

TiN is an excellent supporting layer for both Fe and Co as the catalyst, allowing vertically aligned growth of large arrays of CNTs. In case of using Fe catalyst on TiN, growth temperatures of CNTs are in the range of 450-750°C, while Co allows growth at 350°C as the lowest record. In our experiment, we choose Fe as the catalyst over Co, since Fe results in better quality of CNTs and better alignment of the tubes. According to Ducati et al.[41], the growth rate (R) is proportional to:

$$R \propto \frac{D_0 S_0 exp(-\frac{Q+q}{kT})}{x} \tag{3.3}$$

where D_0 and S_0 are the diffusivity and solubility prefactors, x the diffusion distance, Q and q are the activation energies for diffusivity and solubility,respectively.The activation energy of Fe (0.56 eV) is higher than that of the Co-based catalyst (0.40-0.43 eV). This specifies the reason why at lower temperature growth with the Co and Co-Al catalyst is possible. A lower activation energy allows a sufficient growth rate at even lower temperatures.

The growth rates of different temperatures with Fe catalyst on TiN is compared in the table below. The minimum temperature for CNT growth with Fe catalyst is 450°C, since the growth rate at 450°C was quite low, 500°C is practically the lowest temperature. The CNT grow vertically aligned, and length increases with temperature.

For our design, top metal deposition and patterning are required. The openings between the CNT foams are firstly filled with hexagonal sacrificial structures. The requirements for thick sacrificial materials include uniform and low stress deposition, high temperature (>500 C) and stability during CNTs growth. Further-

Table 3.2: Growth rate of CNTs with 5 nm Fe catalyst at different temperatures [38]

Temperature(°C)	450	500	550	600	650
Growth Rate(nm/min)	120	480	1200	4200	6000

more, it should be easily removable after CNT growth with a selective isotropic etching method. PECVD TEOS oxide is a suitable material for this purpose.LPCVD CNTs are grown in a high temperature environment, from 350°C to more than 700°C []. At temperature less than 500°C, CNTs has more defects in their crystal structures and is more random in direction, less aligned and limited in height. Based on these considerations, our experiments grow CNTs at 550°C to obtain reasonable quality and sufficient height.

3.4. MICRO/NANO DESIGN OF THERMOACOUSTIC DEVICES

The CNT arrays allow for the fabrication of 3D micro-architectures suitable for micro-electro mechanical systems (MEMS) and promising thermoacoustic devices when they are photolithographically patterned. To achieve better thermoacoustic performance and compatibility with mass micro-fabrication, a method of constructing on-chip grown CNT nanofoams with lithographically defined patterns and vertically driven current mechanism is crucial, which is the objective in this work. Previous thermoacoustic designs focus on

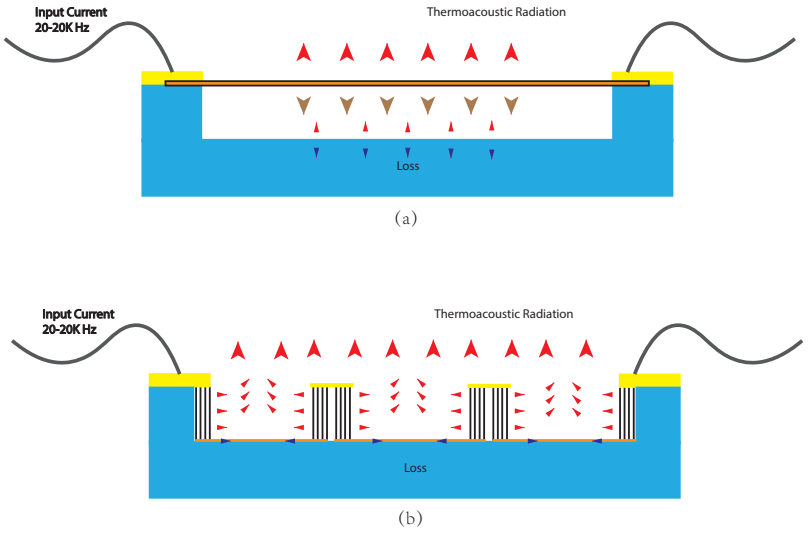


Figure 3.5: Illustration of the difference between 2D and 3D design. (a) Illustrates the 2D design and the less optimal orientation of acoustic emission. (b) Our proposed 3D solution.

employing planar thin film heaters, from which the heat flow is perpendicular to the substrate. 50% of the air expansion is directed towards substrate which can limits their thermoacoustic performance. While we introduce an approach by using vertical thermoacoustic heaters in combination with cavities and patterned openings to enhance the emission of pressure waves. The schematic of planar 2D heater and vertical 3D heater are shown in Figure 3.5.

The 2D planar heater is considered as a open system, it heats up only a thin film of air that is close to the surface of the heater. However, the working principles of a 3D vertical heater array take the advantage of heating up larger volume of air inside the porous heater material. Air expansion accumulates inside the cav-

ities and is eventually released from the the openings forming a strong pressure wave. Due to its semi-closed feature, vertical heater array system is able to direct and focus the thermoacoustic emission, thus improves the thermoacoustic efficiency. Since the heaters are high aspect ratio vertical structures, they occupies less chip area. And in the case of CNT based TA devices, applying vertical CNT nanofoam arrays to construct the vertical 3D heater can avoid the extra steps of fabricating and transferring CNT film. In order to drive

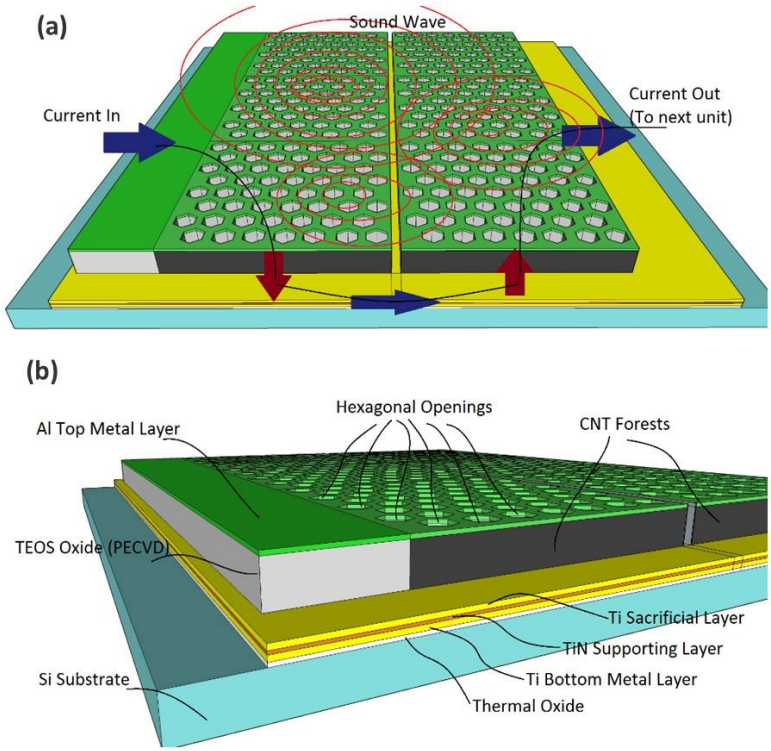


Figure 3.6: A 3D model of our proposed CNT nanofoam design with hexagonal openings for sound emission. (a) Zig-Zag current created by vertically conducting CNT arrays, heating causes air expansion and result in sound emission from the openings. (b) Side view of applied materials in the design.

current through vertically grown CNTs, a top and bottom contact is required. In our design, every two CNT nanofoams arrays are grown on each bottom contact pad with a gap in between as shown in Figure 3.6, thus the electrical connection between the two CNT arrays is bridged by the bottom metal pad. Between each two array unit, the electrical connection is then achieved by the top metal layer. The zig-zag current dissipates joule heating power over the CNT nanofoams and results in air expansion. Hexagonal openings designed for purpose of emitting pressure waves contribute to uniform current distribution and mechanical robustness. High resolution and high efficiency lithography assisted patterning, instead of laser patterning required in fabrication of CNT thin film based devices, provides large freedom on tailoring our CNT nanofoam design into arbitrary shapes and the ability to achieve scalable micro/nano architectures.

The materials applied in our proposed design are as follow:

- **Bottom metal layer:** Sputtered Ti, TiN
- **Structural sacrificial layer:** TEOS oxide
- **3D heater:** LPCVD CNT nanofoam material
- **Top metal layer:** Al

4

Simulation Analysis of the Design

COMSOL multiphysics simulation is used to estimate the performance and assist in the design of the device before fabrication. A 2D thermoacoustic model is simulated for the acoustic performance and a 3D electrical model is built separately for estimating the current distribution. Together with the 2D and 3D model, the our design is considered and described in all the physics that are involved. First, a simulation is built to show the influence of porosity or surface area to volume ratio (SA:V) to the obtained thermoacoustic performance. High SA:V is the motivation for using CNT nanofoam as the heater material. To validate the model of our CNT nanofoam design, we first reproduce a literature benchmark problem of a CNT thin film TA device [24]. The simulation result of the thin film device together with its measurement results in literature are compared to our CNT nanofoam device. The 2D models approximates the cross-section of the devices. As our CNT nanofoam design is in a hexagonal pattern, the 2D model result represent 1/3 of the device performance. Compensation with the heater power is applied to achieve a simulation closer to the real situation. This will be later discussed in section 4.1.2. The CNT nanofoam and CNT thin film possess porosity more than 90%. The material volume is more than 90% occupied by air. Thus in approximation, we consider the volume that is CNT nanofoam and CNT thin film as air in our thermoacoustic 2D model.

4.1. Thermoacoustic Simulation

In this section, two topics are mainly discussed. The influence of SA:V to the thermoacoustic emission and the estimation of the performance on CNT nanofoam TA device.

4.1.1. Influence of Surface Area to Volume Ratio

Among all the previously mentioned thermoacoustic heater materials, we chose CNT nanofoam over metal wires, graphene or other thin films mainly because of its high porosity, more than 90% porous, and its high SA:V. The high porosity of CNT nanofoam results in high SA:V which provides a larger heat exchange interface between air and the heater MWCNTs. This is a desired property which can improve the thermoacoustic efficiency.

A schematic of the 2D model used in our simulation is shown in Figure 4.1. The chip under analysis is located in an air sphere of 2 cm in radius (left). The boundary of the sphere is set to plane wave radiation to approximate the situation of an open field. The area near the chip is assigned to thermoacoustic and solid

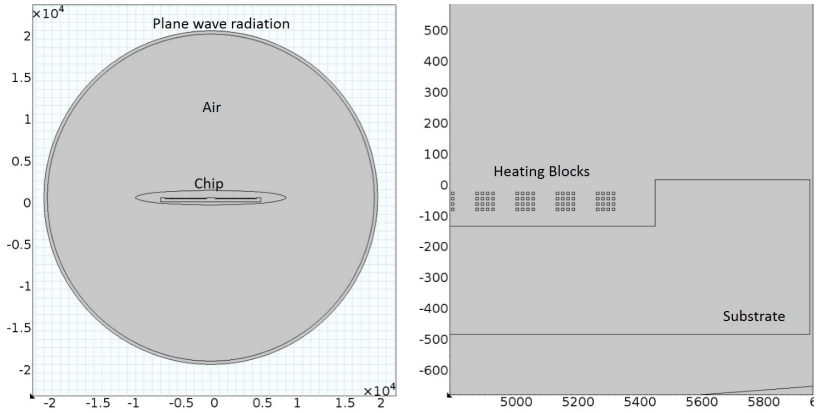


Figure 4.1: 2D Model for thermoacoustic simulation: simulation for different surface area to volume ratio.

interaction physics in which the acoustic field is correlated with heat transfer and mechanical interaction. The ellipse boundary in the model is the boundary between thermoacoustic domain and normal pressure acoustic domain. In the pressure acoustic domain, thermal effect is not accounted for. The substrate of the chip is defined as linear elastic material to interpret the mechanical interaction between air pressure wave and the substrate. A zoomed in view of the model (right) shows the heater squares and substrate. The squares are located in the center in height inside a 150 um deep cavity. Each block is in dimension of 60 um × 60 um and the distance between blocks is 70 um. These dimensions are not related to the real design later on.

The COMSOL simulation below serve as a proof of concept that high SA:V induced by porosity produces higher sound pressure at a same amount of temperature fluctuation that is applied. The SA:V is set into four levels with factor: sf. As shown in Figure 4.2. SA:V factor sf is in value of 3, 5, 7 and 9 which represent the degree of dividing the 60 um border of the main square to construct smaller squares. Obviously that the higher value sf is, the more surface is generated in the same main square. The SA:V value of each sf is calculated to be 888, 1200, 1523 and 1851 /cm respectively.

From the radius of the nanotubes (15 nm) and it's density (10^{10} cm^{-2}), SA:V of the CNT nanofoam in our design can be calculated with equation below, The result is 9.4× 10^4 /cm.

$$SA:V = 2\pi r(cm) \cdot density(cm^{-2}) \tag{4.1}$$

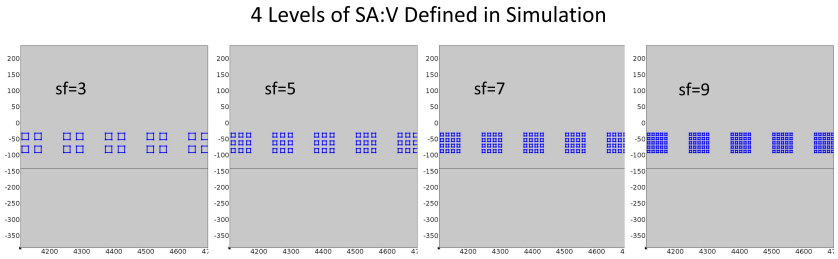


Figure 4.2: An illustration of heater units with different surface area to volume ratio used in the simulations.

A temperature variation boundary condition is assigned to the outline of these squares as the heat source. Here we use Tv = 10 K in the simulation to achieve a reasonable and similar sound pressure level comparing to real devices. The inner part of the small squares are not included into the thermoacoustic component. They are assumed to be lossless boundary heat source in the simulation. A constant frequency analysis at 1 kHz is used in the simulation.

The total pressure field produced by heater squares with sf equals to 3, 5, 7, 9 and the velocity of the air molecules near the heater block is plotted in Figure 4.3. It show that the thermoacoustic emission increases with a increasing SA:V value. At low SA:V condition, the air molecule velocity is lower than simulations with high SA:V. The velocity of air molecules interpret the intensity of air expansion, which result in the acoustic pressure wave. The higher velocity of the air molecules at the boundary of the main heater square is, the higher pressure wave can be generated. With larger surface area to exchange heat in a same volume, air molecules receive more energy from the heater, and tend to expand more. The relationship between SPL and the distance towards the chip is plotted in Figure 4.4.

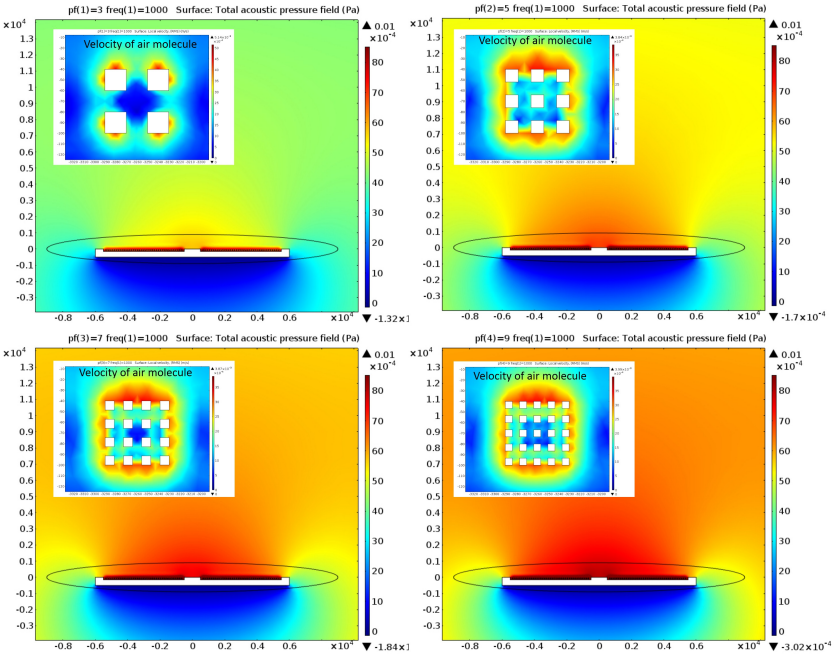


Figure 4.3: Total pressure field (large) and velocity of air near heater (small) at different surface area to volume ratio.

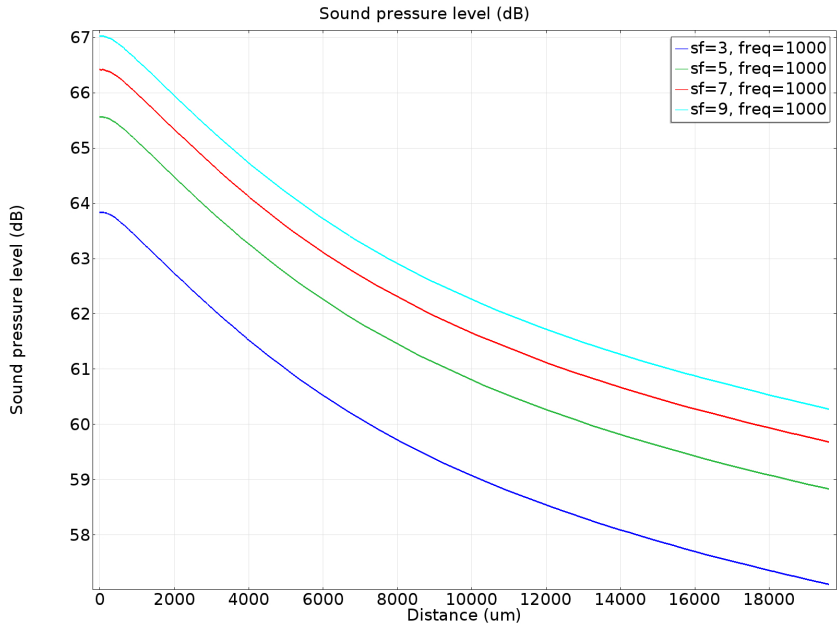


Figure 4.4: SPL vs distance away from the thermoacoustic sound source at different SA:V values.

The above simulation results support that by using heater materials with high surface to volume ratio is an approach to improve the performance of thermoacoustic devices. It indicates that a porous and high SA:V material like CNT nanofoams is able to transfer more heat to air molecules inside the pores and gaps of the bulk block and emits a higher pressure wave on the boundaries of the bulk.

4.1.2. 2D SIMULATION OF CNT NANOFOAM DESIGN

To estimate the potential performance of our design, we simulated the CNT thin film over CNT array device [24] as a comparison. The 2D model of the CNT thin film device and CNT nanofoam device from our design is shown in Figure 4.5. The two designs are simulated in the same material and physics conditions as to compare the difference of their performance. The only change between the 2 model in COMSOL is the geometry. The parameters regarding materials and thermoacoustic and solid interaction physics are the same used in the two models.

Since the CNT thin film device is measured at a distance of 5 cm, the pressure acoustic domain is set to a 5 cm sphere with the boundary condition of plane wave radiation on the border. The thin film is in length of 1.35 cm and the supporting array is 300 um wide and 600 um gap in between. The substrate is in size of 3 cm. Taking the value reported in Xiao's work [9], the thickness of CNT thin film is set to 550 nm. In our CNT nanofoam design, a block which is 15 um in width and 10 um in height is used to represent the cross-section of the nanofoam. On the top of the CNT nanofoam is the Al top metal layer which is 5 um thick and 4 um overlapping on both side of the nanofoam. The opening between nanofoam units is 70 um wide.

For either the CNT thin film and CNT nanofoam is super porous, more than 90% of the volume is filled by air, the bulk material property for the thermoacoustic model of the CNT and air composite is estimated to be the same as air. The space between individual MWCNTs is in the range around 30 70 nm which is at the same scale as the free mean pass of air molecules (68 nm) at 1 atm and 300 K. Thus we consider the heat transfer from CNTs to air is infinitely fast. The temperature of the air follows the CNTs instantly. Substrate is defined as silicon and top metal layer is aluminum.

Volume heat source is assigned to the CNT thin film domain and the CNT nanofoam domain. Parameter Qi is used to define the heating power intensity. Qi has a unit of W/m^3. COMSOL multiphysics automatically take the 2D model into 3D when solving by adding a default z depth of 1 m. But for the 2D simulation, there is no flow along z direction, thus it is a dummy z depth that is used, however in the calculation for Qi, we need to take the default 1 m z depth into account. Qi is then calculated for CNT thin film and CNT nanofoam at a total input power of 0.5 W respectively, $7.75 \times 10^7\ W/m^3$ and $2.87 \times 10^7\ W/m^3$.

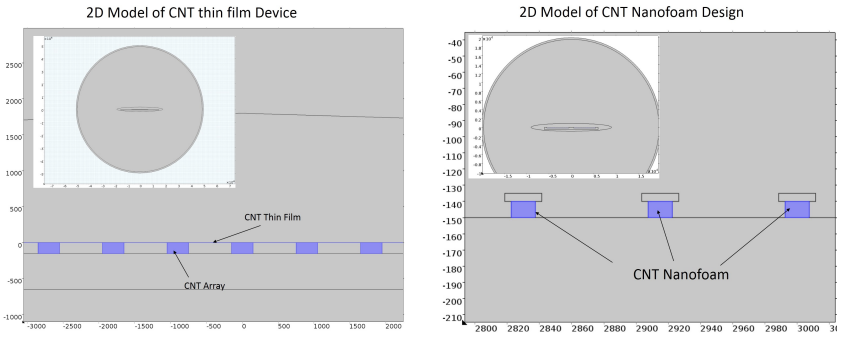


Figure 4.5: The 2D model used to simulated the CNT thin film and our CNT nanofoam device.

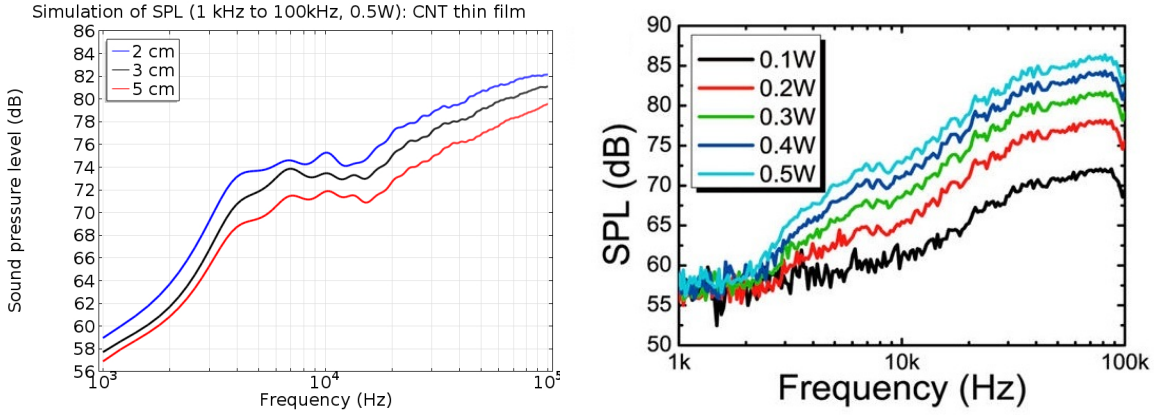
The heat source module in COMSOL supplies the heating power uniformly through out the air medium. However the real process in the physics is that heat flow into air from CNTs which occupies less than 10% volume of the heater system. The different mechanism here induces a mismatch to the experimental result

of the CNT thin film device. This could because of the high porosity of CNT thin film results in a higher local temperature variation than the heater model used in COMSOL. Thus to match the experimental result, a power factor of 7 is applied to modify the heat source power.

The simulation result show the frequency response of sound pressure level of the CNT thin film over CNT array device is shown in Figure 4.6 together with the measurement from Haoming's paper. In the simulation result, the SPL vs frequency curve is plotted at distance of 2 cm 3 cm and 5 cm. The measurement of CNT thin film over CNT array device is carried out at a distance of 5 cm.

The simulation result from our model shows a good match of the SPL curve against frequency. The power factor 7 added to the model has no effect on the shape and trend of the curve, it only increases the amplitude of SPL into a similar range of the measurement results. The COMSOL model is not optimized yet, however the simulation results show several matches to the measurement: 1),SPL vs frequency curve keeps increasing from low frequency (1 kHz) to high frequency (100 kHz) in the simulation, same is observed in the measurement result. 2), Both simulation and measurement result shows a step of the curve near frequency range from 5 kHz to 10 kHz. 3), In the flat step range there are two small peaks in the curve, they appear both in simulation and the measurement. 4),A second flat region of the curve is shown in the measurement near the frequency range from 40 kHz to 80 kHz. Similar but weaker phenomenon shows in our simulation near 40 kHz to 50 kHz range.

From the above analysis of simulation, our model in COMSOL can be used to predict the performance of the CNT nanofoam device qualitatively, but not sufficient to predict quantitatively, optimization on method of interpreting the CNT thin film or nanofoam material in the simulation is the critical point.



(a) (b)

Figure 4.6: Validation of the COMSOL model by matching to literature: (a),Frequency response of a CNT thin film TA speaker at input power of 0.5 W based on our COMSOL model and (b) the measurement result from literature [24].

In the simulation of CNT nanofoam device, due to the hexagonal patterns instead of wires or stripes of the nanofoam, the 2D model is insufficient to describe the real situation in which the center of the hexagonal opening is receiving pressure waves from 3 groups of parallel CNT nanofoam arrays. Thus a factor of 3 is multiplied to the heater power density to compensate. By applying boundary conditions, the performance of the CNT nanofoam design of this work is analyzed. The frequency response of SPL from 1 kHz to 100 kHz is plotted in Figure 4.7. The curve show a much more flat frequency response over the whole spectrum that is simulated. Most the literatures report that their thermoacoustic device measured has a higher sound pressure level emission at higher frequency range. The reason of this difference could be the structure of the heater has an fundamental change in our CNT nanofoam design. Among all the existing designs, nearly all of them are planner heaters with flat thin film or metal wires over porous substrate or cavity. However in our nanofoam

design, we applied the first time vertical volume heater. Current is passing vertically through the MWCNTs and the air expands in the lateral direction in the first place forming the high pressure in the center of the hexagonal opening and then the acoustic waves burst out into the ambient. This special structural design in our device has potential of acting as a acoustic filter.

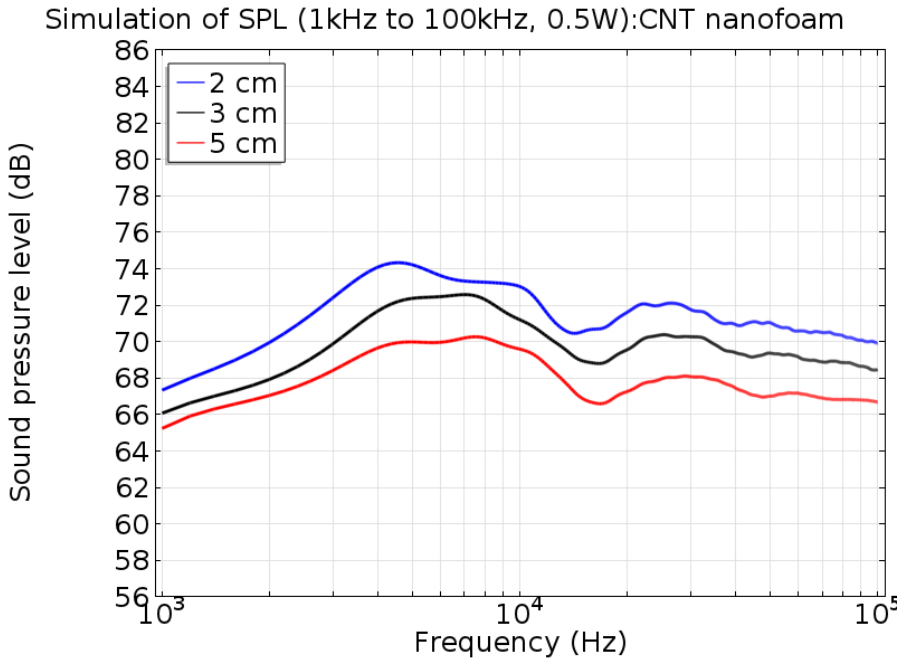


Figure 4.7: Simulative frequency response of SPL of CNT nanofoam device from 1 kHz to 100 kHz at a input power of 0.5 W

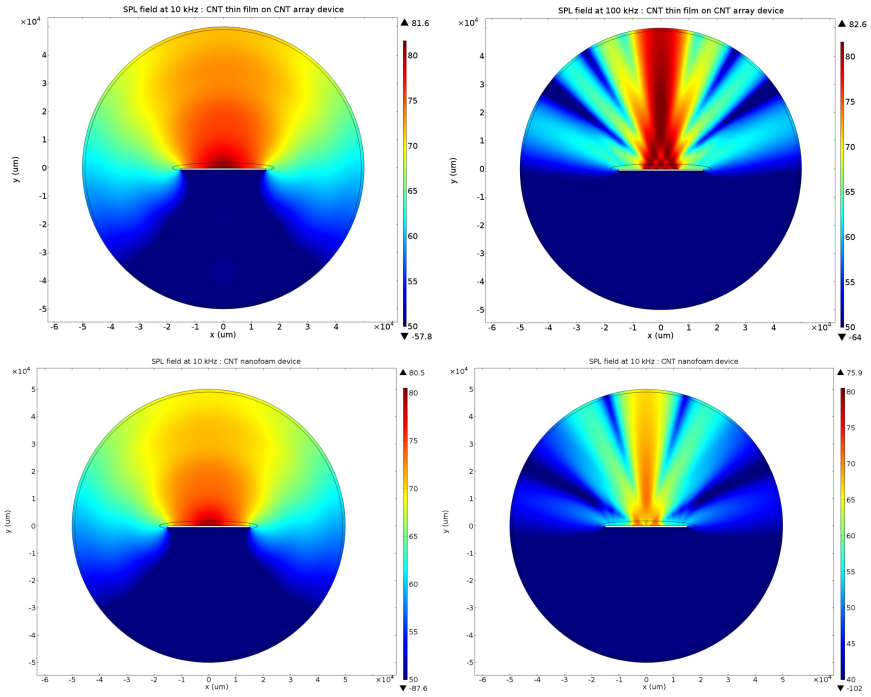


Figure 4.8: Simulative frequency response of SPL of CNT thin film device from 1 kHz to 100 kHz at a input power of 0.5 W

The SPL response at low frequency range of the CNT nanofoam device shows better simulation result than

the CNT thin film, nearly 8 dB higher at 1 kHz. A flatten step also appears in the curve near the frequency range from 5 kHz to 10 kHz. Comparing to the simulation result of the CNT thin film device the shape of the curve is similar but flatten. Plots of the SPL field at 10 kHz and 100 kHz are shown in Figure 4.8. As seen from the plots, the SPL field shows the same pattern of distribution at both low and high frequency for the two device. Both CNT thin film device and CNT nanofoam device emits sound waves in a more focused direction at 100 kHz. The value of sound pressure level increase largely from low frequency to high frequency in the case of CNT thin film planar thermoacoustic sound source. And in our design of CNT nanofoam vertical volume heater the SPL value is less altered from low to high frequencies.

4.2. ELECTRICAL DISTRIBUTION

The 2D thermoacoustic simulations give a pre-evaluation of the performance of the CNT nanofoam design. After the 2D simulations, an 3D model of the device is built to inspect the electrical performance of the device as well. Since the design layout is symmetric, thus the main segment of the design is simulated to interpret the whole device. The 3D model is shown in Figure 4.9. In the zoomed in view of the model, the sandwich structure is consist of top Al metal layer, CNT nanofoam and bottom Ti layer. Overlapping of the Al layer and the 50 nm TiN supporting layer is neglected to simplify the model. Comparing to the Ti pad layer beneath, 50 nm TiN is very thin and induces little influence on the electrical distribution of the design. The overlapping edges of Al can contribute to an increase of conductance which only gives better device performance when included. The worst case situation is considered in the simulation when the input electrical current is driven

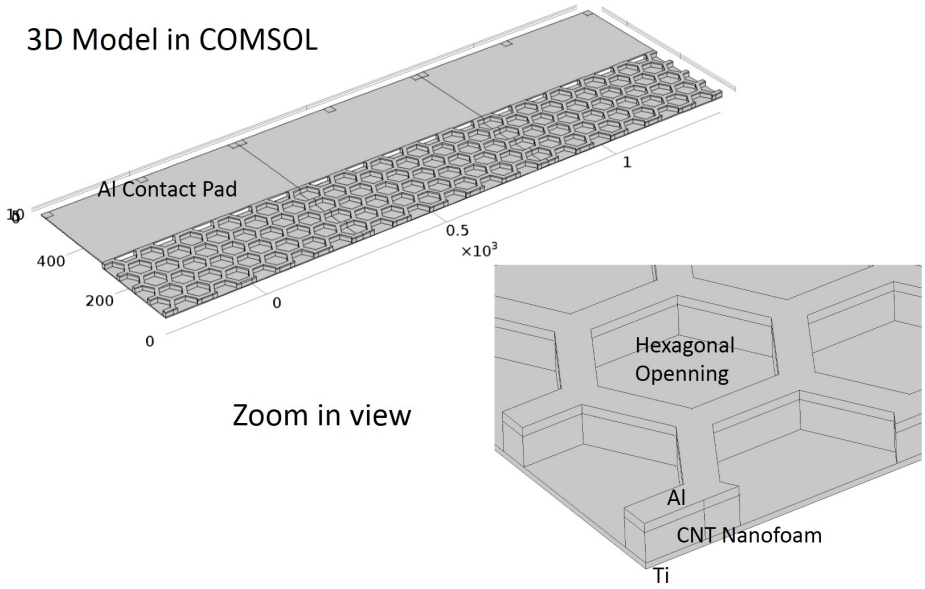


Figure 4.9: The 3D model built in COMSOL to evaluate the current distribution of the nanofoam design

in with a probe. The tip of each probe is in the dimension of 10 um, and for assembling the chip on to a PCB board, Al wire bonds with diameter of 20 um is used to connect each device to the gold pads. Thus the electric current input portal is assigned to a 10 um × 10 um square on the Al pad in the electric model to match the real deice. Ground is assigned to bottom cross-section edge along the Ti pad. The electrical properties of Ti and Al are used from the standard library from COMSOL. However the electric property of CNTs needs to be specified according to our own process and is derived from Figure 3.3.

The simulation result is shown in Figure 4.10. Both current density and voltage distribution is plotted.

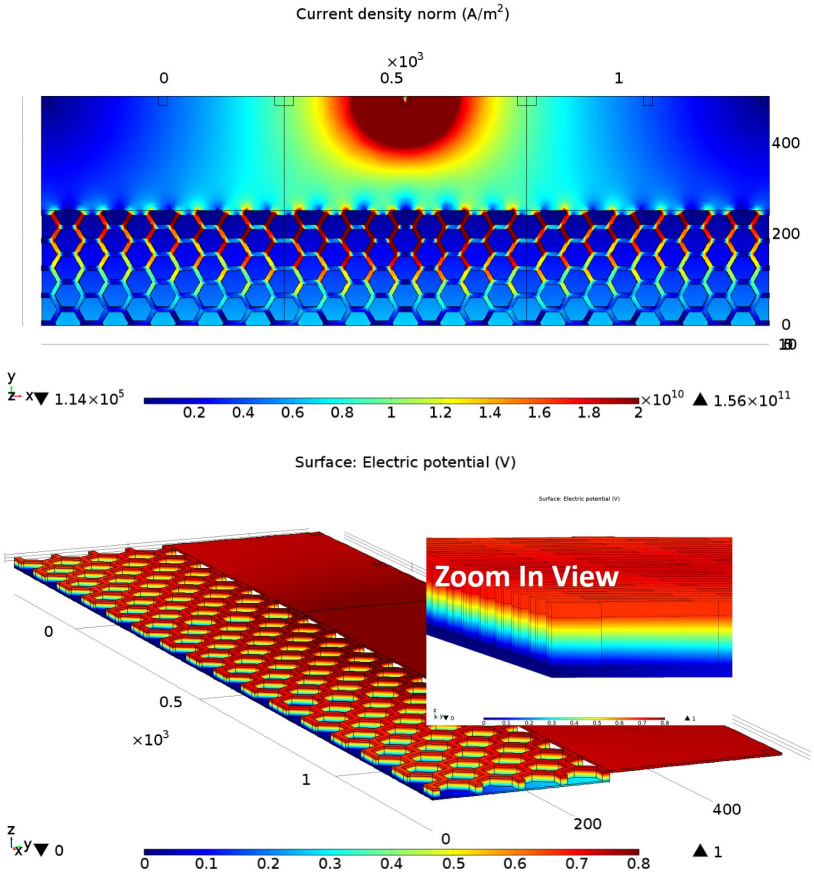


Figure 4.10: Current density and voltage distribution of the nanofoam design at DC

At the edge where current enters the hexagonal patterned area of the device, the current density is around 2×10^{10} A/m^2 in the center and around 1.8×10^{10} A/m^{2}on the edge. This indicates that the current distribution over our design is uniform. And in the 3D plot of voltage distribution, it is shown that the voltage drops mostly over the CNT nanofoams. This means most of the joule heating power is dissipated through the CNTs rather than Al or Ti. According to the simulation result, the overall design has a good electrical current distribution, we can assume that heats are uniformly generated over the whole device area which is essential for an efficient thermoacoustic emission.

4.3. SUMMARY

Our simulation model employs the bulk material approximation to modify CNT thin film and CNT nanofoam materials. Simulation shows a adequate match with measurement from literature. Hence, we applied the model to evaluate our CNT nanofoam thermoacoustic design as a preliminary understanding of the device performance. The simulation result shows a SPL of 72 dB at 3kHz with input power of 0.5 W and measured at distance of 2 cm. Moreover our device shows a flat response over a wide frequency band. The flat frequency response over the audio range is a unique behavior of our device and promising in application.

5

FABRICATION PROCESS OF CNT NANOFOAM TA DEVICE

In this chapter, the details of fabrication process of the novel CNT nanofoam TA device is discussed. Our proposed process approach stress on the cleanroom fabrication compatibility and mass production ability. Our approach sets the objective to have a complete production chain within standard cleanroom facilities. The fabricated CNT nanofoam TA device is shown in Figure 5.1. The chip is wire bonded to a PCB for acoustic measurement. For fabricating the device, it requires 3 layers of masks and each device is fitted to a 6 × 6 mm die on a 100 mm wafer. Some test structures are fabricated along the device as well.

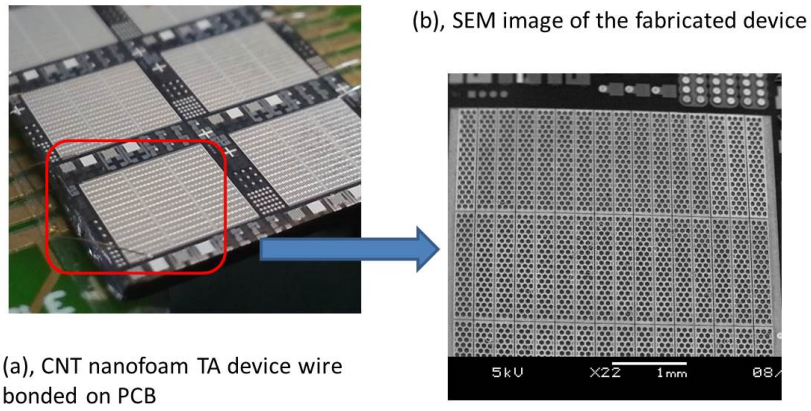


Figure 5.1: The fabrication result of our proposed processing approach

5.1. CRITICAL PROCESS STEPS

The main process steps to construct the designed CNT nanofoam architecture is presented in Figure 5.2 along with SEM images for each steps. The whole fabrication process starts with thermal oxidation of bare silicon wafers. During the thermal oxidation both front side and backside oxide are grown. Under the consideration of the growth rate, to obtain a thick 2 um uniform silicon oxide, we use the temperature of 1100 °C. Front-side oxide layer acts as an adiabatic layer for thermoacoustic purpose. The silicon oxide layer on the backside

can be used later for backside cleaning of Fe. On top of the thermal oxide layer, a stack of Ti/TiN/Ti layer is deposited by sputtering. The first Ti layer at the bottom of the stack ensures a good electrical conduction. The TiN layer in the middle of the stack is used as the support layer for Fe catalyst due to its reasonable conductivity. Another top Ti layer is added for sacrificial purpose. It protects the TiN beneath during previous dry etching step.

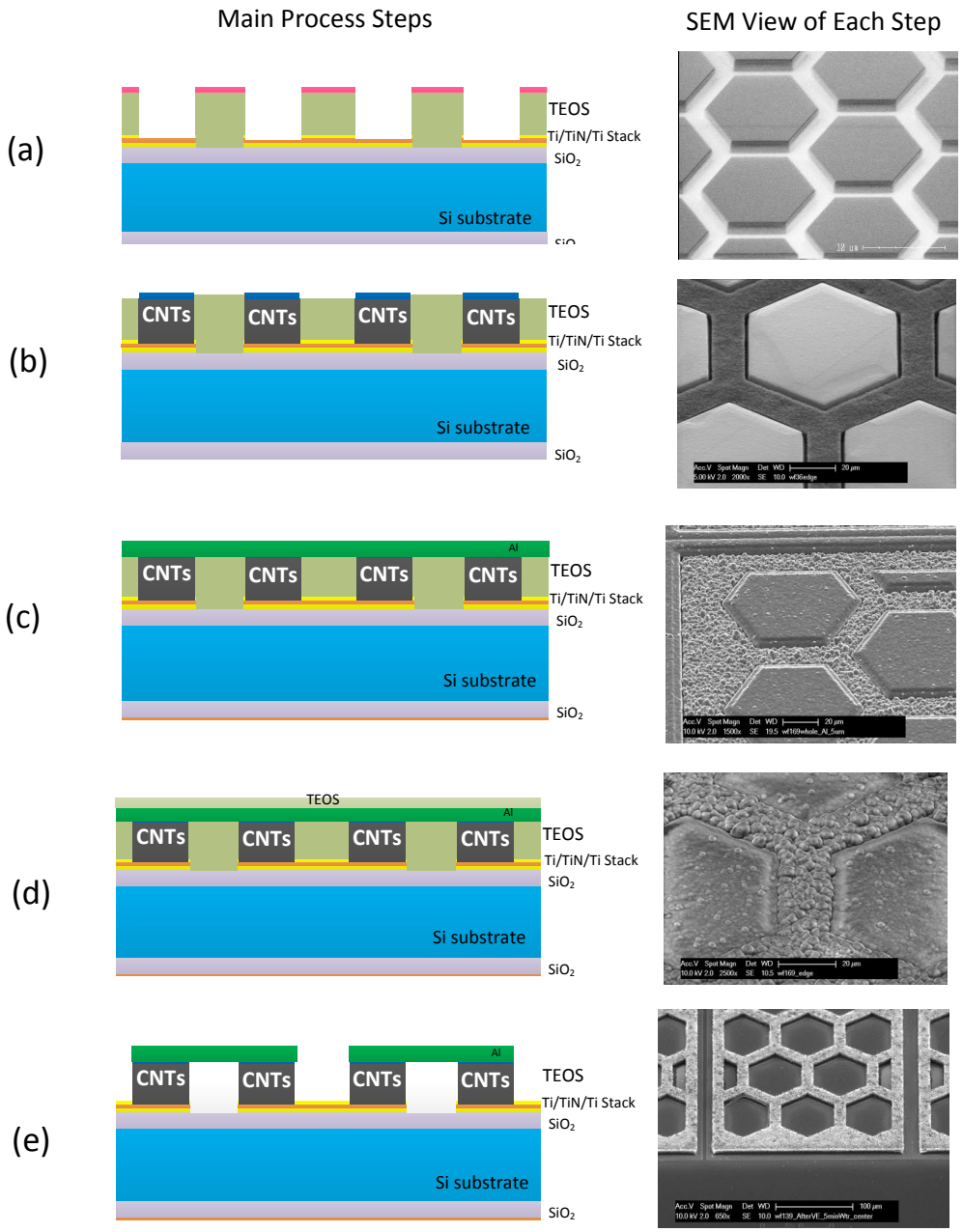


Figure 5.2: The schematic of main process steps and its correlating SEM images.

After the bottom metal layer is patterned, a thick TEOS Oxide is deposited on top by PECVD at a temperature of 350 °C. The TEOS Oxide acts as a structural sacrificial material. Trenches in which CNT nanofoams later grow are etched isotropically through the TEOS Oxide. With TEOS Oxide supporting on the side of CNT foams,top metalization can be achieved.

The accurately patterned CNT growth within TEOS Oxide trenches mainly consists of 3 steps, catalyst deposition, lift-off and grow. A 5 nm thin Fe catalyst layer is deposited on the wafer by evaporation. The photo-resist for masking the TEOS oxide is not removed after the dry-etching step. Thus during Fe deposition, area of TEOS oxide is still covered by the photo-resist. With lift-off process unwanted Fe is removed together with the photo-resist, only the TiN supporting layer at the bottom of trenches is deposited with Fe. Lift-off process is carried out in a ultrasonic bath in NMP. In this way the TEOS area is prevented from Fe contamination and after lift-off they are considered as clean to CMOS process. The CNT growth rate which under conditions of 5 nm Fe catalyst, 50 nm TiN supporting layer and 550 °C LPCVD method is around 1 um/min. This growth rate is within a desirable range for reaching our target height, the height of the nanotubes can be well controlled. The total CNT growth time is approximately 10 min to reach the same height as the TEOS.

After the CNTs growth, Al metalization on top of both CNTs and TEOS is carried out by sputtering. Transport wafers are used in this step to prevent Fe contamination from the backside of the wafer to the equipment stage. The Al metal layer forms both the top connection over contiguous CNT arrays and the contact pads of the device. An excellent connection is desired over the narrow gap between the CNTs area and TEOS oxide area. However, due to different surface condition (CNTs area is porous and rough comparing to TEOS oxide area), the roughness on these two area of Al layer is unbalanced. The large contrast of roughness give rise to a less conformable Al connection over CNTs and TEOS oxide. To make the wafer CMOS compatible again, backside cleaning is needed. By etching away backside thermal oxide, Fe contamination can be removed. Another method is to deposit another Fe isolation layer on the backside of the wafer, for example 50 nm TiN layer.

The pinholes induced by the porosity of CNTs after Al deposition is sealed by an additional TEOS oxide layer. The next step is to pattern the top TEOS/Al layer. Photo-resist coating in this step needs additional caution because of the surface roughness induced by CNTs. Either spray coating or special spin coating for topology is suitable.

When Al is throughly removed from the unwanted area, the etch process lands on TEOS oxide. The last step in the whole process is to remove all the TEOS oxide to release CNTs to ambient air. Considering to sustain CNT nanofoams' property and structure as much as possible, HF vapor etch is used to remove TEOS Oxide instead of any wet process. After the complete fabrication process, the thermoacoustic CNT nanofoam

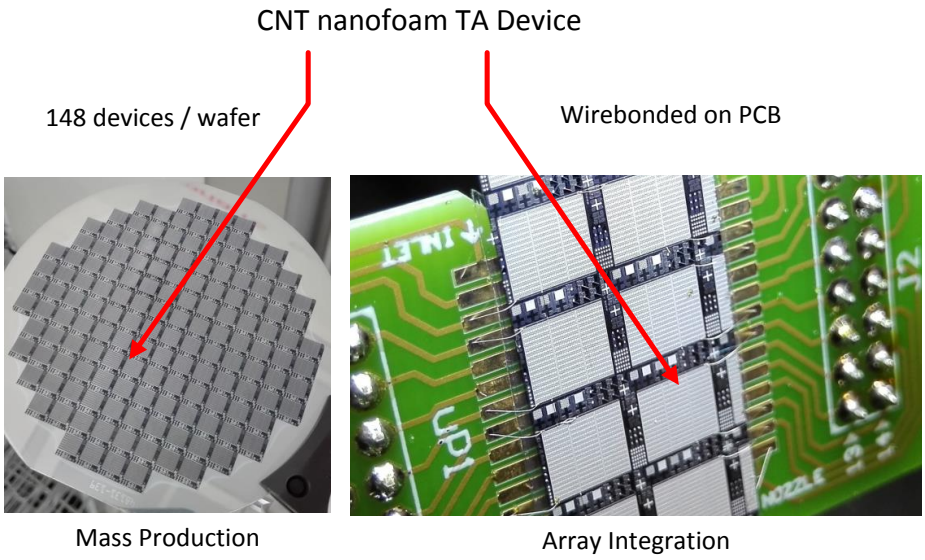
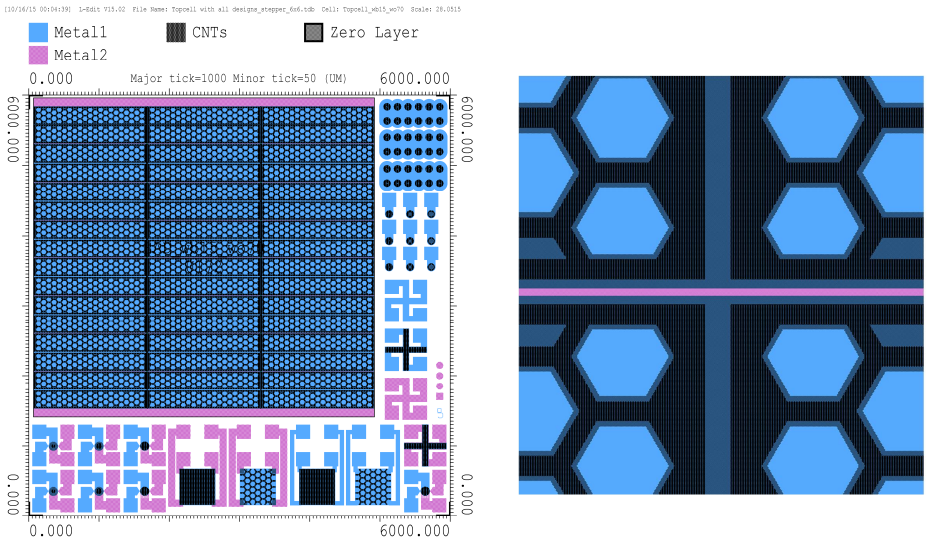


Figure 5.3: A view of the fabricated devices on a wafer and assembled on a PCB. It shows the ability of mass production and integration of our CNT nanofoam design.

devices are obtained as shown in Figure 5.3. On each process wafer, an array of 148 devices is created. A small array of 8 devices are integrated on a PCB board to test. The original process flow gives good result however several challenges are encountered causing imperfection of the fabricated devices.

5.2. MASK FOR LITHOGRAPHY

A mask is designed along with the flow chart before the actual fabrication. The mask layout is designed for 6 × 6 mm dies. Each device layout contains 3 layers of images, Metal-1, CNTs and Metal-2 as shown in Figure 5.4. Metal-1 image is used to define the pattern of the bottom Ti/TiN/Ti metal layer. Each metal-1 pad is 264 um wide, 270 um in pitch in y direction and 4825 um long in x direction. The Al contact pad on the both ends of the device is 125 um wide and 4825 um long. CNTs lines are 15 um in width with hexagonal opening width of 30, 50 and 70 um. Metal-2 image on top of CNTs has a 4 um overlapping while the Metal-1 has a 7 um overlapping with CNTs. The overlapping ensures a reliable process result considering any mismatch induced from lithography. Each CNT array are 250 um wide and with 20 um distance between each other in both x and y direction.



(a) Overall layout (b) Zoom in view

Figure 5.4: Mask designed for the process, consist of 3 different images in black(CNTs), blue(Metal-1) and pink(Metal-2).

5.3. SUMMARY

Our proposed process approach achieved in combining CNT nanofoam 3D heater architecture with standard cleanroom fabrication and the ability of mass production. Patterns of CNT nanofoam is defined by lithography and is scalable. HF vapor etch of sacrificial TEOS oxide is efficient and harmless to CNTs which is a ideal solution to avoid wet process of releasing CNT nanofoams. Fe contamination is prevented in the process which gives our device potential to be integrated with CMOS technology as well. The challenges during processing are discussed in Chapter 6.

6

PROCESS RELATED CHALLENGES

In this chapter, the main challenges during the realization of CNT nanofoam architecture is discussed. Challenges are encountered at different processing steps. The process flow is optimized in order to achieve the ideal structure.

6.1. CHALLENGES OF THE TECHNOLOGY

There exits 3 main challenges in the original process flow which are listed below:

1. Damaged TiN support layer after dry-etching of TEOS oxide, due to non-uniform deposition of thick TEOS oxide and varying etch rate of TEOS oxide.
2. Large gaps between CNTs and TEOS oxide cause Al deposition on the side wall of CNT nanofoams.
3. Ti layer exhibits a bad adhesion in HF vapor etch.

The non-uniformity induced by TEOS oxide deposition and dry etching leads to a severe over etch of Ti sacrificial layer on the edge of the wafer which caused ion bombardment of TiN beneath. It is found that Ti layer is less passive when oxide etching exhaust are in presence. The imperfect isotropic dry etch creates trenches which are not ideally 90° and the TEOS oxide is etched together with Ti sacrificial layer in BHF(1:7). Thus a large gap between TEOS oxide and the grown CNT nanofoam is formed. Unlike trenches on a flat, smooth and non-porous surface (>0.5 um thick Al sputtering is needed for closer a 1 um wide trench), it requires >5 um Al to close a CNT-TEOS gap which is 2 um in width. The reaction between HF vapor and SiO_2 produces H_2O. Water accumulation at angular and shadowed regions of the device caused acceleration of etch rate and damage of Ti bottom metal layer. The thermal oxide beneath Ti layer suffer from significant under etch due to water accumulation and result in the lift-off of a whole device area during the required over etch. Schematics of the main challenges and corresponding SEM images are shown in Figure 6.1

To solve the challenges, the process flow is optimized with several extra steps. In Figure 6.2 the simplified flow chart concerning the main optimized steps are illustrated. To protect TiN layer from ion bombarding, 2 techniques are applied to improve the procedure. First, a soft landing recipe is used in the end of the etching procedure. And moreover, an extra 50 nm SiC layer is deposited as a protection layer for Ti sacrificial layer. An extra masking layer of SiN or SiC is added on top of TEOS oxide. SiN and SiC is passive in BHF(1:7).The masking layer stays after the lift-off process. the overhanging edges covers the gap after CNTs are grown. An

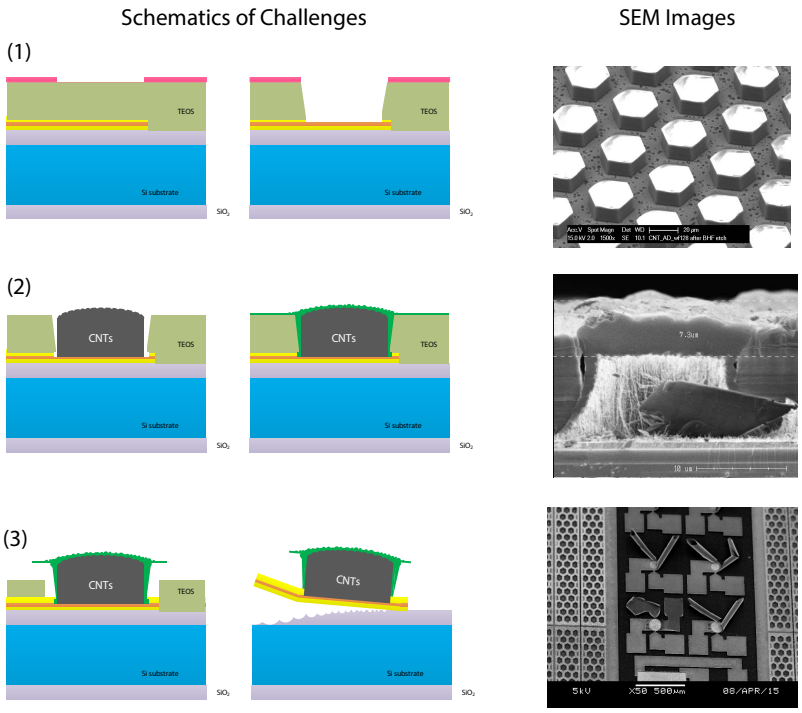


Figure 6.1: Critical steps that lead to challenges in fabrication

extra PECVD TEOS oxide layer is deposited specially to close pinholes due to its better step coverage than sputtering. The extra oxide layer can be easily removed in the last steps, it is suitable for this purpose. The thermal oxidation process in the beginning is removed from the flow for better adhesion of Ti on Si substrate in HF vapor etch. In addition, a 50 nm thin layer of SiC is deposited onto the Ti/TiN/Ti stack to protect Ti the water accumulation during HF vapor etch.

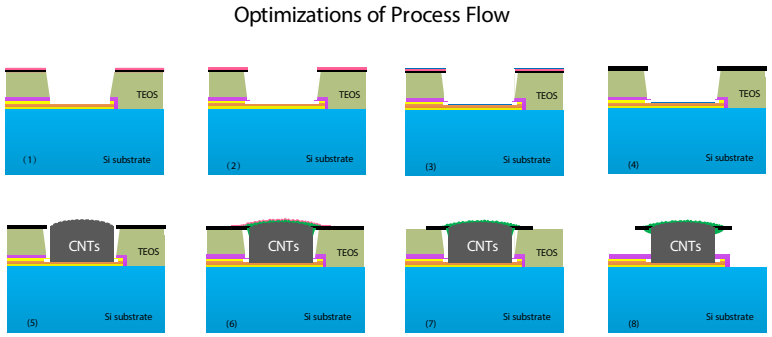
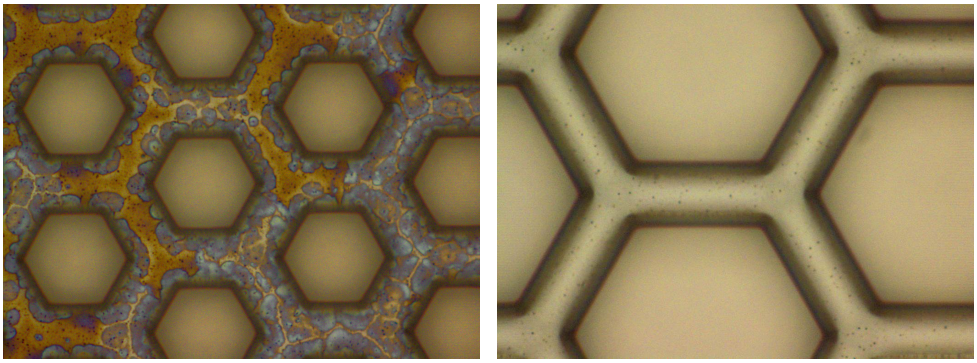


Figure 6.2: Optimized processing steps to solve the challenges: SiC protection layer for bottom Ti metal pad and masking layer on top of TEOS oxide to close the gap

6.2. PROTECTION OF TiN SUPPORTING LAYER

Dry etching of 10 um TEOS oxide structural layer is required to obtain the trenches in which CNTs are grown later. For this process Drytek 384T plasma etcher is used. Due to the limitation of equipment, etch rate of TEOS oxide in the Drytek standard oxide recipe with fluoride plasma differs from center to edge of the wafer. The quality of the TiN supporting layer is essential for uniform and high quality CNT growth. Dry etching process of TEOS oxide has a possibility to damage the TiN layer. Although TiN layer is not being

etched in the fluoride plasma, once exposed to the ion bombarding the surface condition TiN is changed. For the protection of TiN layer, the Ti sacrificial layer during the over etch should maintain a uniform quality, a comparison between the bad result of Ti layer and a desired condition is shown in the optical microscopy in Figure 6.3. When the TiN layer is completely exposed in the plasma, aligned CNT nanofoam can no longer

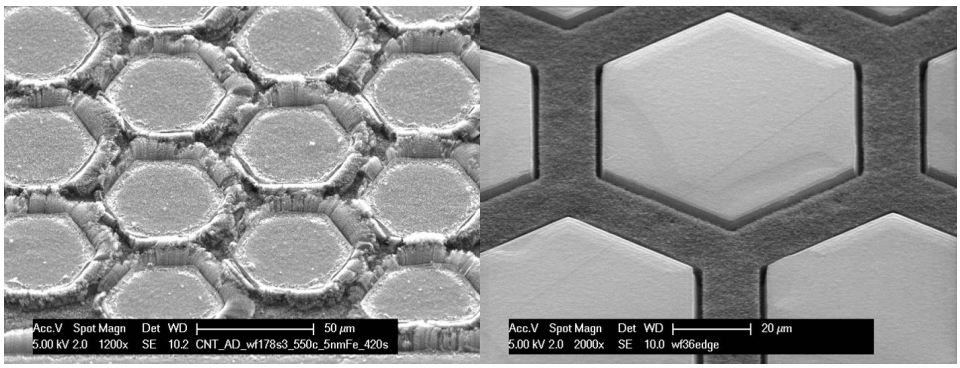


(a) Damaged Ti sacificial layer

(b) Desired condition of Ti sacrificial layer after dry etching

Figure 6.3: The undesired damage and desired condition of Ti sacrificial layer after dry etching under optical microscope.

grow on it. Figure 6.4 shows how CNTs grow on a partly damaged TiN supporting layer. From Figure 6.4a, it can be seen that the edges of the trench bottom shows an accelerated growth rate of CNTs and poor growth rate in the center. The CNT nanofoam is arbitrary in growth rate and growth direction. It is not able to be fabricated into our desired thermoacoustic device. For obtaining good quality CNT nanofoam as shown in Figure 6.4b, 2 techniques are applied in the process, soft landing at low power and etch in short time cycles. Details can be found in Appendix B.3. Soft landing provide a lower power of ion bombarding which can lead to a higher selectivity of Ti. Pure Ti layer known to be passive in the dry etching recipe, exhibit an accelerated damage with the presence of silicon oxide. The exhaust produced by the reaction between fluoride and SiO_2 has an effect on sensitivity of Ti in the etching environment. Thus Pumping cycles keeping a lower level of exhaust at the bottom of the trench can protect the Ti layer.



(a) Damaged TiN layer

(b) Good quality TiN layer

Figure 6.4: SEM images of CNTs grown on damaged TiN and good quality TiN layer

6.3. TI LAYER LIFTED OFF IN HF VAPOR ETCH

The patterned hexagonal openings on Al layer allows the final removal of the remaining TEOS oxides in HF vapor. Al layer is passive in the HF vapor because of the native oxide. Wet etching is avoided, due to possible

sticking and collapsing of CNT bundles. HF vapor etch is highly selective to TEOS oxide.In the original design, the thermal oxide layer beneath the Ti/TiN/Ti stack acts as an isothermal layer. The maximum thickness of this thermal oxide layer is 2 um, and the minimum dimension of a Ti/TiN/Ti pad is around 250 um, thus the under-etch of the thermal oxide layer is not significant to lift-off the device. However, from the experiment result, the Ti layer is lifted off the substrate. The etching process produces H_2O which accumulates every etch cycle. The presence of H_2O together with HF vapor will both etch oxide and Ti. Thus at region such as underneath the Ti/TiN/Ti pad, H_2O easily accumulate and less easy to be carried away during purge. The porous property of CNT nanofoam allows HF vapor to reach the bottom and etch laterally once the top window is opened. Thus the bottom metal layer is exposed to HF vapor in a very early stage shown as in Figure 6.5. This leads to the detachment of Ti layer in the end. The ultimate target of this step is to have sufficient over-etch

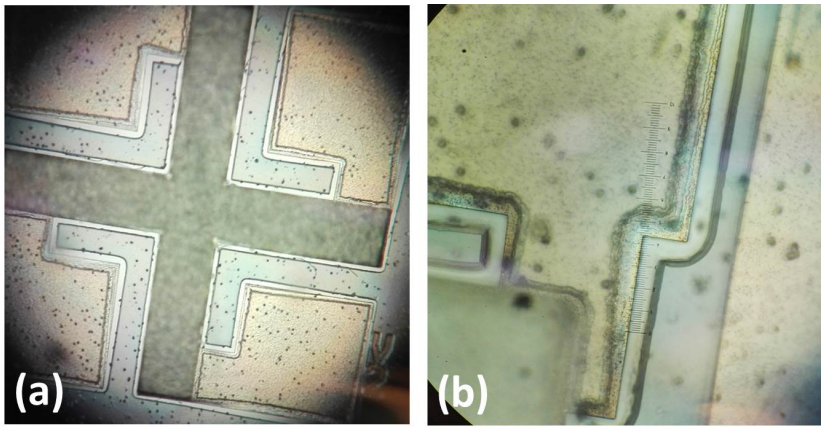
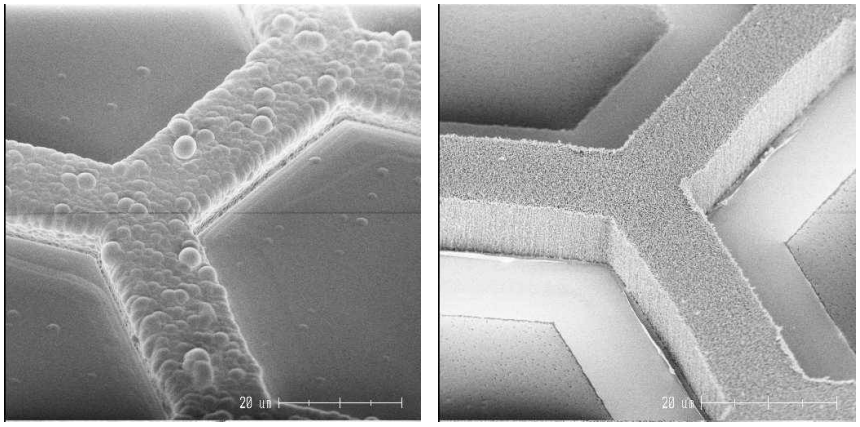


Figure 6.5: The accelerated HF vapor etch due to water accumulation, viewed under optical micro scope.

for removing all the TEOS oxide while having all the other parts, CNTs nanofoam, Al layer and Ti/TiN/Ti layer maintained. A 50 nm thick SiC is able to protect the bottom metal layer. The SEM images in Figure 6.6 present CNT nanofoam that is covered by TEOS oxide and CNT nanofoam that is released with HF vapor etch under sufficient over etch. The bottom metal layer is well protected.



(a) CNTs sealed by PECVD TEOS oxide (b) Overetch of TEOS oxdide in HF vapor

Figure 6.6: SEM images when SiC protective layer is used. With the SiC protective layer the bottom metal layer can be well protected.

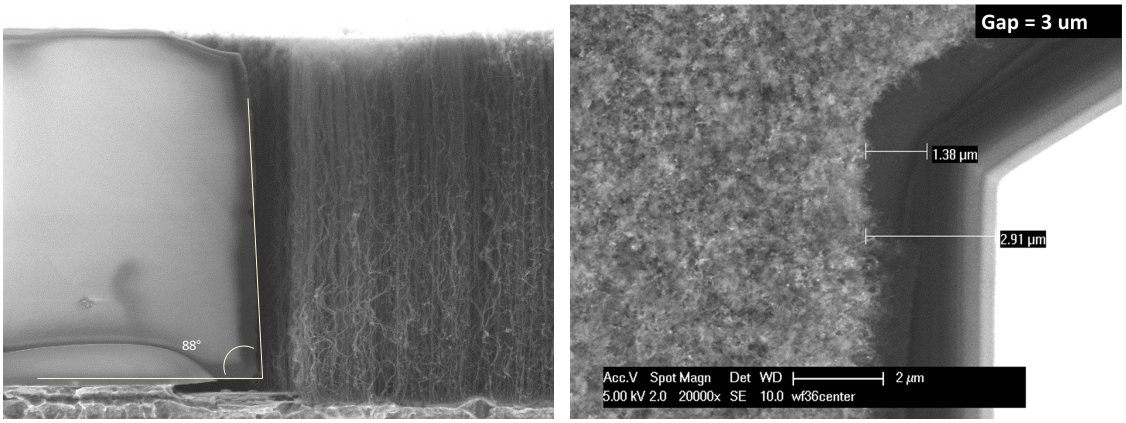
The main procedure of processing of this thesis project is as described above, optimization of the process is done by debugging several major challenges.A concern is that CNTs bundles have the potential of absorbing

HF vapor and result in degassing afterwards. A degassing test of HF is needed to ensure safely usage of the device. Method like extra heating up of the device in vacuum can help to degas.

6.4. GAP BETWEEN CNTS AND TEOS OXIDE

The large gap between CNT nanofoams and TEOS oxide structural layer is a critical challenge to achieve the desired heater structure. Several correlated issues make the removal of the gap a difficult task. The gap is directly caused by three facts, one is that the profile of TEOS oxide side wall exhibits an offset from the desired 90°. The second fact is that BHF(1:7) used to remove Ti sacrificial layer etches TEOS oxide which then enlarges the gap. The third fact is that for protecting the TEOS oxide area from Fe contamination, lift-off procedure of photo-resist is applied to remove unwanted Fe. According to the mechanism of evaporation, shadowed area, under the photo-resist is not able to receive catalyst. Based on these 3 facts, gaps between CNT nanofoam and TEOS oxide become significant. For closing a 2~3 um gap, thick Al more than 5um is in need. Sputtered Al is deposited into the gaps and sabotages the thermoacoustic advantages of CNT nanofoams. The ideal situation is to have no Al covering the side of CNT nanofoams.

The angle measured is approximately 88° in Figure 6.7a, thus in case of 10 um thick TEOS oxide, the top wideth of the gap attributed by the dry etching profile alone is 350 nm by calculation. However in some severe cases, angel of 81.3 ° as calculated from the measurement in Figure 6.7b. To remove the Ti sacrificial



(a) Cross-section profile of the etched side wall of TEOS oxide

(b) Top-down view of the gap

Figure 6.7: SEM images of the CNT-TEOS gaps

layer thoroughly, at least 8 minutes of wet etch in BHF(1:7) is required for a 500 nm Ti sacrificial layer, this process can remove approximately 2 um TEOS oxide that can largely increase the gap width. A substitutive etchant of BHF(1:7) is HF 0.55 % which has a more aggressive etching to Ti and etches TEOS oxide slower than BHF. However samples which employ the HF 0.55% to remove Ti sacrificial layer, exhibits an limited height of CNTs. SEM images can be found in Figure A.3 about this issue. BHF(1:7) tends to give a better TiN supporting layer for Fe deposition and CNT growth. Fe catalyst is deposited by evaporation for an accurate control of thickness which is critical for the growth rate. To get rid of the gaps between the CNT nanofoam and the TEOS oxide, a masking layer which is highly selective in the BHF(1:7) bath is added on top of TEOS oxide layer. SiC and SiN are materials well known as stable and strong in micro-fabrications. They both possess low etch rate in BHF and can be removed later by plasma dry etching. For this masking layer deposition we choose PECVD over LPCVD carbide or nitride. Although LPCVD gives better quality layers, it requires higher temperature. Considering that there is TEOS oxide layer beneath, high temperature process of more than 550°C is avoided. Two sets of experiments for constructing the masking layer are as follow, 1). A masking

layer of 1 um thick SiN and SiC are deposited by PECVD at 400°C. 2). Masking layer of SiC with thickness of 100 nm, 200 nm, 300 nm and 400 nm are deposited.

The SiN layers give rise to an issue that the AZ9260 photo-resist peels off from the wafer during the Ti sacrificial layer etching in BHF(1:7). Photo-resist shows good adhesion on SiC, however SiC masking layer of 1 um thick suffers from stress. Photos of these issues are included in Figure A.5.

To explore further, the second set of test is carried out to identify a suitable thickness for SiC that can withstand the stress without any cracks. It is found that thickness from 100 nm to 400 nm maintains its uniformity. However, they all exhibit the problem that the overhanging edges are broken off.

In Figure 6.8, SEM images of samples employing SiC masking layer of different thickness are presented. The average gap width is narrowed down to 1.5 um which is improved. However all of them suffers from broken edges. It is observed that with a thicker layer of SiC mask layer, less amount of broken edge happens. The result proves that the concept of using a masking layer to eliminate the gap between CNT nanofoam and TEOS oxide is possible and promising, the question left is to find a better material choice or an optimized SiC deposition. The candidate materials can be TiN, Al_2O_3 and Mo. Top metalization is important for forming

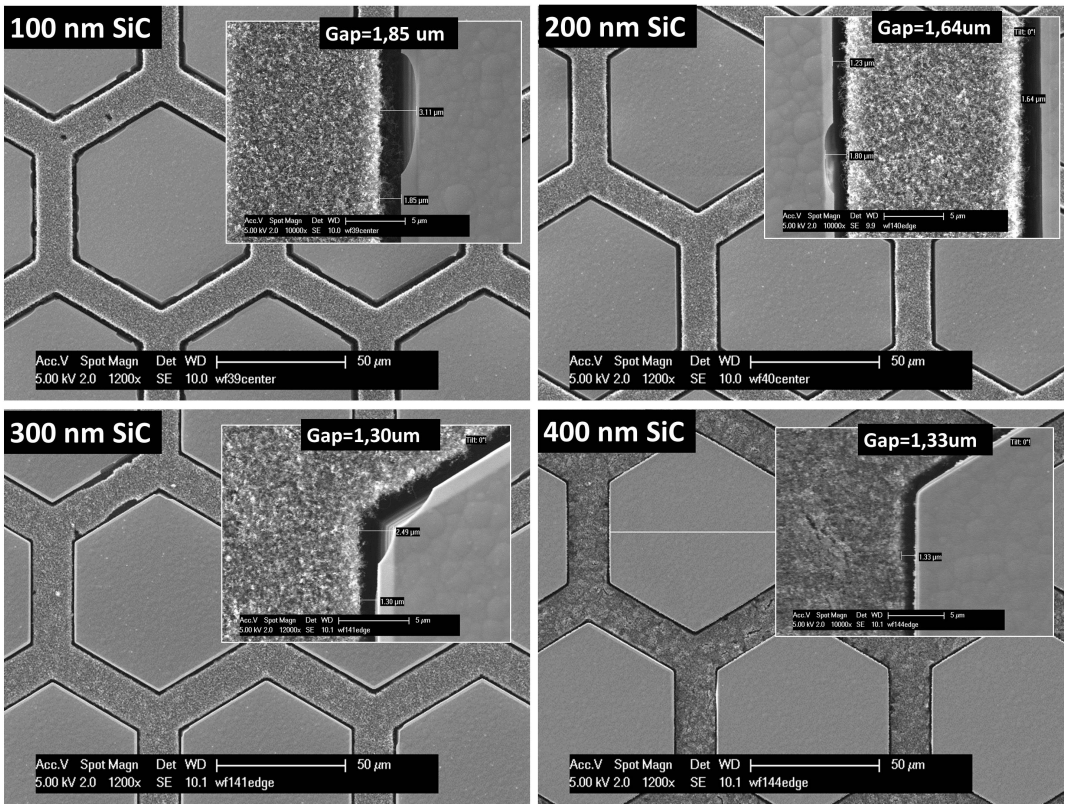


Figure 6.8: Different thickness of SiC masking layer, 100 nm, 200 nm, 300 nm and 400 nm, used to close the CNT-TEOS gap

an electrical connection. The quality of the top metal layer has an influence on the current distribution and the total resistance of the device. The thickness of the top metal layer affects the thermal capacitance of the device. Thus a thin and conformable Al layer is the ultimate target for the metalization step. Ideally, after metalization, CNT areas are sealed. However the gaps between CNT nanofoams and TEOS oxide give challenges to encapsulate the top of porous nanofoams completely with a thin layer of Al. Since the nanofoams are more than 90% porous, any pin holes will allow the air trapped inside the foam to expand out if heated. During the process of baking after the coating photo-resist, these trapped air creates bubbles inside the photo-resist shown in Figure A.4. The solution is to seal the CNTs area with an extra TEOS oxide layer. PECVD TEOS oxide

has a better step coverage than sputtered Al and can be removed in the HF vapor etch easily. In Figure 6.9 the ability of Al and TEOS oxide to seal the porous surface is illustrated. Image (a) is taken on a sample with 5 um Al deposited on the wafer and image (b) shows the situation which uses only 4 um TEOS oxide.

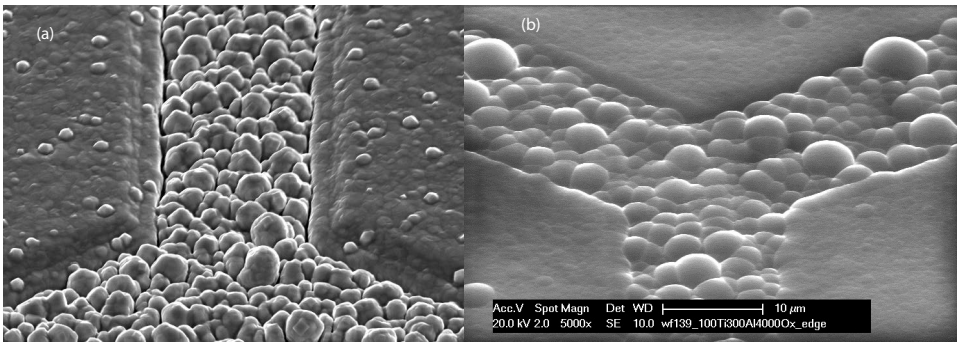


Figure 6.9: A comparison between the ability of Sputtered Al and PECVD oxide to seal gaps and pinholes. a),With 5 um Al sputtered on CNTs. b),With 4 um PECVD oxide deposited on CNTs

6.5. SUMMARY

Challenges in respect of protecting TiN layer and bottom Ti layer are well solved with mini-cycles of soft landing in dry etching and 50 nm SiC protective layer. The one remaining challenge is to close the TEOS-CNT gap completely. Improvements have been made by employing SiC masking layer. The processing results show several undesired issues regarding stress built up in SiC layers. The TEOS-CNT gaps give rise to sidewall Al deposition of CNT nanofoams. The gap induced influence on our fabricated device performance will be discussed in Chapter 7.

7

MEASUREMENT AND CHARATERIZATION

In this chapter, measurement results in the aspects of material property, electrical and acoustic performance is discussed. Raman spectroscopy is used to inspect the quality of CNTs at different conditions along the process flow: 1), as grown, 2), etched in HF vapor with TEOS oxide coverage. Electrical measurement of the I-V curve of the device is carried out on a Cascade probe station with precision semiconductor parameter analyzer. And in the end, an acoustic measurement setup using high precision microphone and network analyzer together with the test device located inside a sound proof chamber is built and some preliminary acoustic characterization comparing with electrodynamic and piezoelectric sound source is carried out.

7.1. RAMAN SPECTROSCOPY CHARACTERIZATION

To characterize the quality of CNTs with Raman spectroscopy, the ratio between D peak and G peak in the spectrum is the main indicator. The D peak is defect related and the G peak interpret the Raman active mode of graphitic materials. The lower I_D/I_G is, the better crystallized the CNTs are. To determine the crystal quality in a more accurate way other peak ratios, such as G'/G, D+G/G, 2G/G, 2D'/G, D/G' can be involved. In the characterization with Raman spectroscopy, 514 nm wave length laser is used. It is important to use always the same wave length laser in the measurement, since the D/G peak ratio is dependent on the wave length of the incident laser as well. With the 514 nm laser, D peak appears at 1350 cm^{-1} and G peak appears at 1582 cm^{-1}.

The measurement results of Raman spectrum of the CNT nanofoam at different process steps is shown in Figure 7.1. The I_D/I_G has a value of 1.31 (averaged by 3 measurements in the center of the wafer) with as grown CNT nanofoams. As in the process, post steps after CNT growth such as PECVD TEOS oxide sealing (400 °C)and HF vapor etch is applied to the CNT nanofoams, these steps can have effect on the CNTs crystal property. An I_D/I_G of 1.41 is measured at the same region in the center of wafer. As the ratio of the D peak (defect) and G peak increased after the post processing steps, it indicates that the post process has introduced more defects into the carbon nanotubes. And since the I_D/I_G value of the as grown CNTs and the CNT nanofoam at the end of the process is close (7.6% increase), we conclude that there is no destructive effect from our process to the CNT nanofoam property. In addition the value of I_D/I_G in our measurement matches with literatures [42] under the same conditions to grow CNTs (50 nm TiN support layer, 5 nm Fe catalyst, 550 °C).

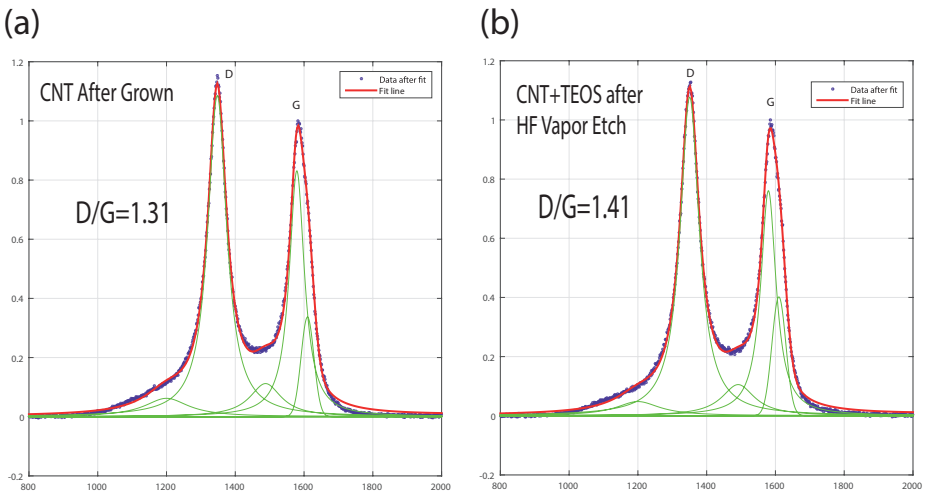


Figure 7.1: Raman spectrum of CNTs at two different process steps, as grown and after HF vapor etch.

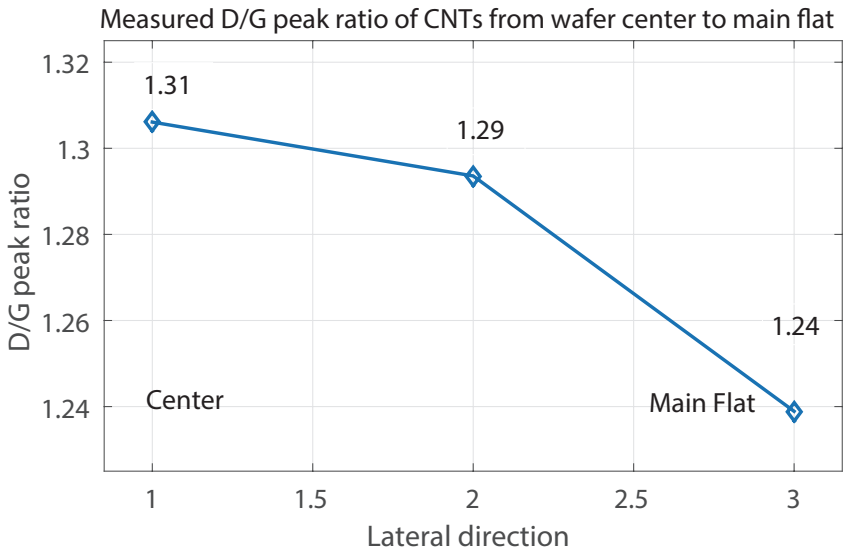


Figure 7.2: Raman Spectrum of CNTs at different locations of the sample

Raman spectrum is measured along different position, center, middle and edge near main flat, on the wafer to inspect the uniformity in crystal quality of the grown CNTs. The quality and growth rate of CNTs are sensitive to temperature. The non-uniform distribution of temperature on the wafer stage can result in the non-uniform growth of CNT nanofoams. The edge of the wafer near the main flat is taken into consideration here. When placing the wafer on the stage, the main flat is near the thermometer. The measurement result show a trend that the crystal quality of the grown CNTs increase (D/G peak ratio drops) from center towards the main flat edge in Figure 7.2. SEM images shown in the Figure 7.3 are taken at 3 different location referred to the main flat of the wafer, far side edge (secondary flat), center and near the main flat.

The SEM images show that on the far side on the wafer from the main flat, CNTs appear to have the poorest quality, and are the shortest. Moving towards to main flat region the CNT nanofoams become taller and more uniform in height. This indicates that the growth rate of CNTs is higher near the main flat. Since this non-uniformity does not have any radiative distribution features over the wafer (all edge dies are poor, center dies are good in quality), but shows a strong dependent on where the thermometer is closer to the wafer, therefore

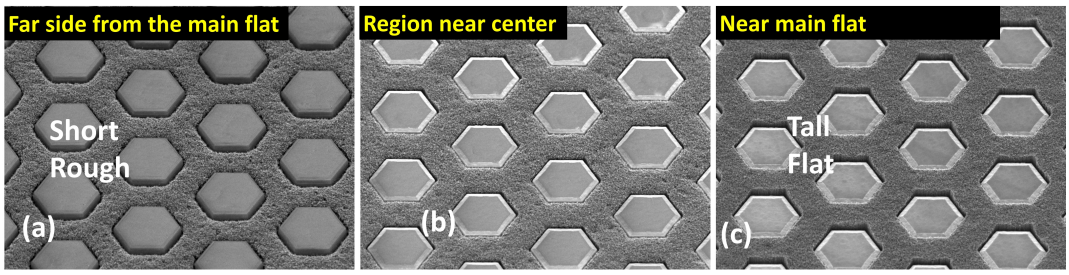
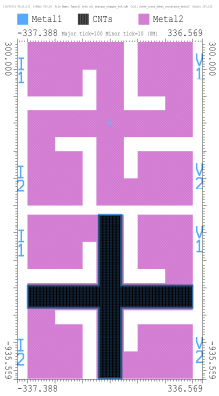


Figure 7.3: Non-uniformity of CNT growth over wafer scale

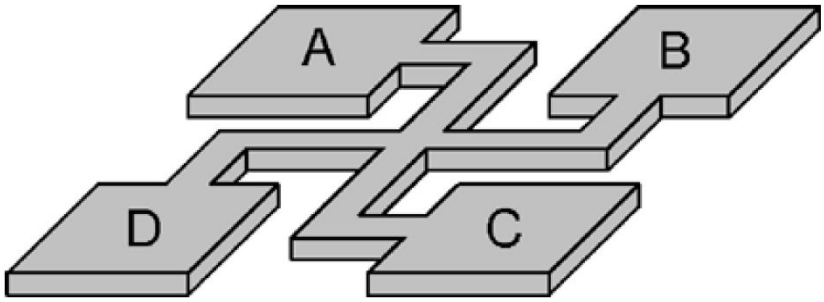
it is mainly induced by the temperature gradient on the sample stage during the growth rather than other previous process steps.

7.2. ELECTRICAL CHARACTERIZATION

The electrical measurement is carried out on a probe station with precision semiconductor parameter analyzer. Some Greek cross structures [43], shown in Figure 7.4, are fabricated together with our CNT nanofoam TA device to monitor the sheet resistance of Al layer. Greek cross structure are both constructed on top of TEOS oxide and CNTs. Since Al layer is sputtered on top of CNTs in our design to provide lateral electrical conduction, it is interesting and essential to characterize the actual sheet resistance of the Al layer on top of CNT nanofoam thus to inspect how much the material property is influenced.



(a) Greek Cross structure used to measure sheet resistance of Al on TEOS oxide and CNTs



(b) A schematic of the greek cross test structure. [44]

Figure 7.4: Greek test structure for measuring the sheet resistance of Al in the fabricated device.

The measured I-V curves of the two different Greek cross structure are shown in Figure 7.4. The relationship between current and voltage is linear and it is shown that the Al layer sputtered on CNT nanofoams are more resistive than Al layer on TEOS oxide. Sheet resistance of the two: Al_TEOS and Al_CNT can be derived with Equation (7.1) below:

$$R_s = f \cdot \frac{\pi R}{ln(2)} [\Omega/\square] \tag{7.1}$$

where f is the form factor related to the geometrical asymmetry of the sheet. For a homogeneous and uniform film f equals to 1. From the I-V cures obtained from measurement on Al Greek cross structures in Figure 7.5, the R of Al_TEOS and Al_CNT are 2.01 $\times 10^{-3}\Omega$ and 1.23 $\times 10^{-3}\Omega$. Then R_s of both situation at an Al thickness of

5 um is calculated to be 9.11 $\times 10^{-3}\Omega$ and 5.57 $\times 10^{-3}\Omega$ respectively. Thus the sheet resistance of the Al layer is influenced by the CNTs beneath. CNTs nanofoam has a porous surface, the sputtered Al atoms form a rough surface on top of CNTs. Al accumulates on tips of the nanotubes and grow into small bumps which grows in size when thicker Al is deposited. This rough surface condition causes a reduction of the effective thickness of the Al sputtered which induces a higher sheet resistance to the Al layer. The R_s of Al_{CNT} increase by 1.64 times of the standard Al layer that means the effective thickness of the sputtered Al on CNTs is 3 um.

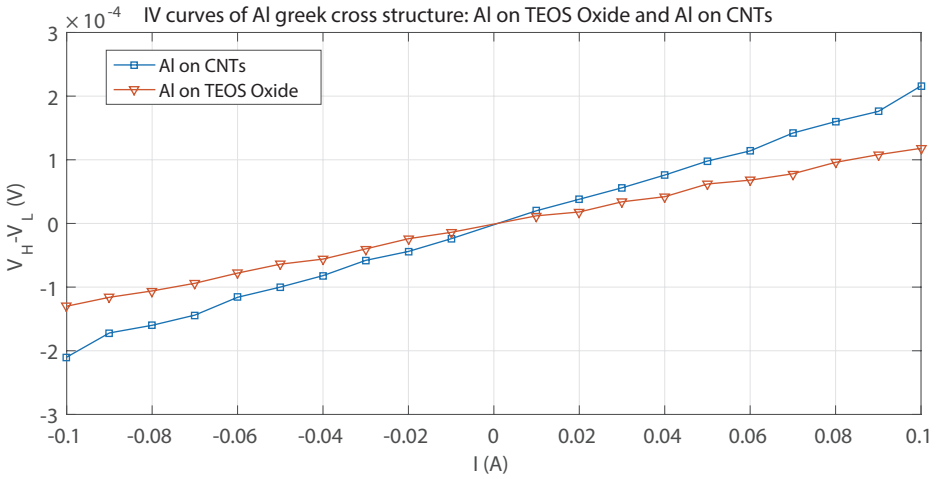


Figure 7.5: The I-V curves of the Al greek cross structure both fabricated on TEOS oxide and CNT nanofoams

Seven devices from the edge near secondary flat of wafer to center of the wafer is measured for their I-V curves. The sample used in the measurement is 1/4 of the whole wafer, shown in Figure 7.7a, The I-V characterizations of all the devices under test shows a linear curve as plotted in Figure 7.6. The linear behavior of the curve indicate that our device is mainly a resistive component, it also proves that the CNT nanofoam is metallic rather than semi-conductive. In addition, a deviation of the I-V curve is observed among various devices.

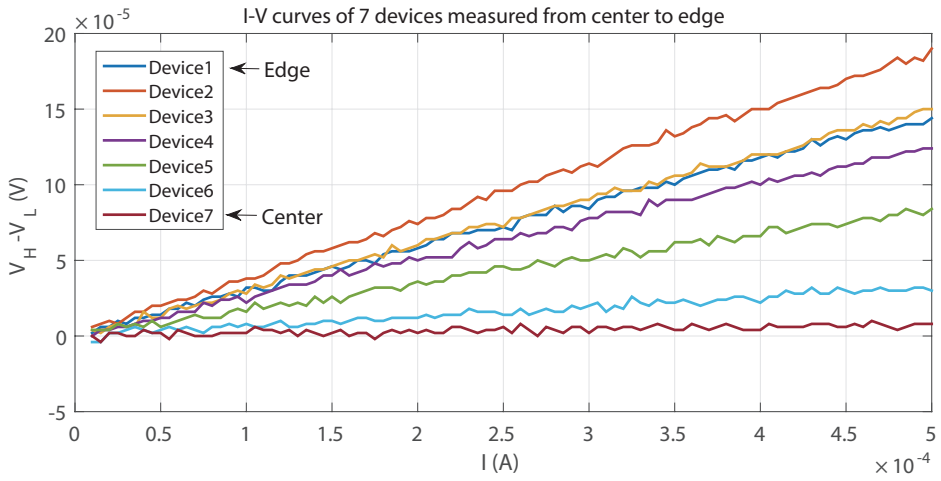
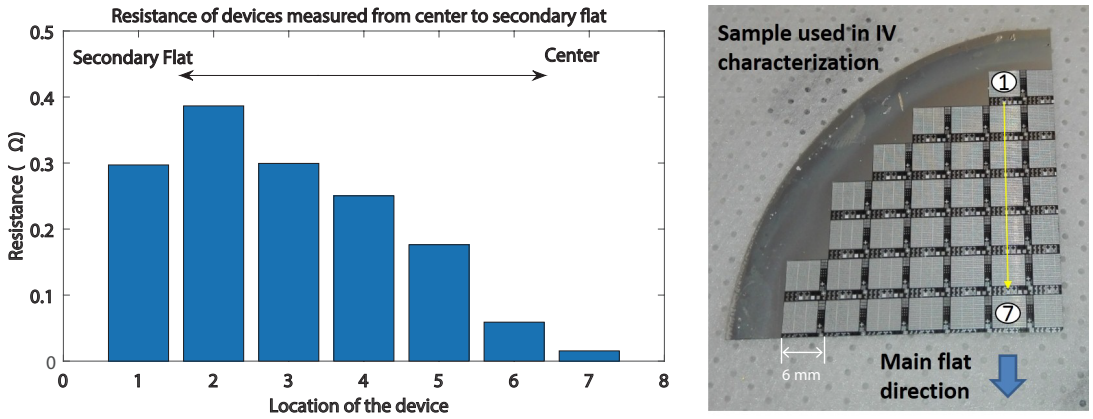


Figure 7.6: I-V characterization of the fabricated devices

The resistance of each device is obtained from the I-V curves and shown in Figure 7.7. The resistance increases from 0.02 Ω up to 0.38 Ω from center to the edge which is nearly 20 times. As mentioned before that the crystal quality of CNTs show poorer Raman spectrum result at the far side edge of the wafer from the main

flat than the center. These poorly grown CNTs result in the non-uniformity of the resistance measured over devices at different locations. In the poorly grown CNT nanofoams, the MWCNTs array is less aligned in the vertical direction and there exists more interconnecting joints between individual MWCNTs. The joints of the nanotubes are mostly rich in defects and increase the scattering of carriers which gives a higher resistivity.



(a) Resistance variation.

(b) Chip layout on wafer.

Figure 7.7: The resistance variation from wafer center to edge.

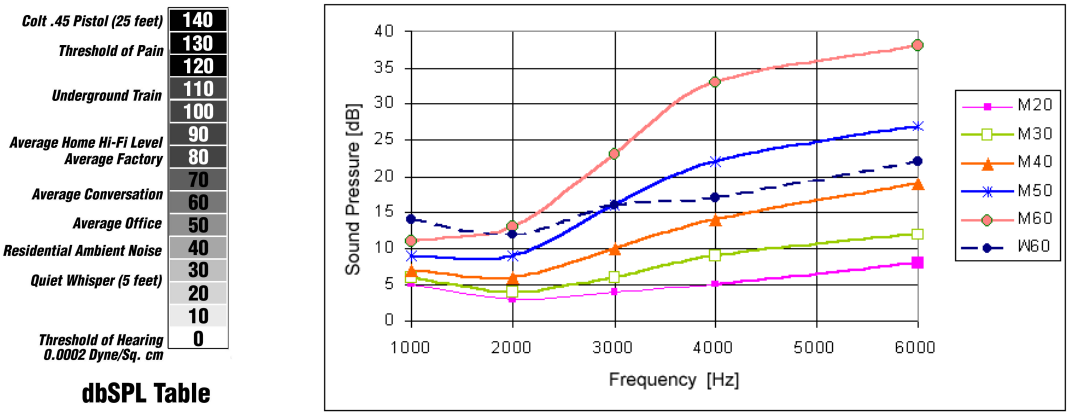
From the hexagonal pattern, we can calculate the ratio between the area occupied by CNT nanofoam and the Ti pad area of each array in our design to be 32.3%. For the pad dimensions is 250 um × 4825 um, the area of the pad is 1.21×10^{-6} m^2. Thus the area of each CNT nanofoam array is 3.90 $\times10^{-6}$ m^2. By using Fe catalyst at temperature of 550 °C the resistivity of MWCNTs bundles is around 2 $m\Omega\cdot cm$, referred from Figure 3.3. And the height of CNTs is around 10 um. So the resistance of each CNT nanofoam array is then determined to be 0.5 $m\Omega$. The total design is consist of 16 arrays in series. Thus the expected total resistance of our TA device in in around 8 $\times10^{-3}$ Ω.

By comparing the theoretical value and the measurement result of the device resistance, conclusion is that the Al deposition on the side wall of the CNT nanofoams does not have a significant effect on the electrical property of the whole device. The current is mainly conducted through the CNT bundles. The reason are as follow: 1), Since the Al deposition on the nanofoam side wall act as a resistor in parallel with the CNT bundle, in the case of a dominating bypass current through the Al, the resistance of the whole device should be decreased. However the measurement shows the opposite. 2), As the the devices at the opposite edge of the main flat, for example device 2 in Figure 7.7a, suffer from the poor CNT quality, CNTs are shorter and the gaps between CNTs and TEOS oxide layer is more obvious. It is then more Al deposition in the gap and short in height attribute to more decrease in resistance. However, device 2 has the highest resistance.

Thus in the fabricated devices, the CNT nanofoam is still the thermoacoustic heater, however the Al covering the side can block the air expansion and still a huge drawback.

7.3. ACOUSTIC CHARACTERIZATION

The acoustic measurement setup consist of a network analyzer, sound proof chamber, high precision microphone, TA chip under test and a preamplifier of the microphone is shown in Figure 7.9. Hp 4395A network analyzer (1) supplies the input signal to the TA CNT nanofoam chip. The high precision microphone used here is Earthworks QTC50 (4) which has a sensitivity of 30 mV/Pa. The specifics of the Earthworks QTC50 can be found in Section (B.2). The CNT nanofoam chip (3) is fixed at a location 2 cm away from the microphone inside a sound proof chamber (2). A Preamplifier, earthworks microphone preamp 1022 (5), is in between



(a) Table of SPL

(b) Threshold

Figure 7.8: Introduction to the sensation for SPL and the frequency and age dependent human-hearing threshold [45]

the network analyzer and the microphone to amplify the signal. The sound proof chamber is decorated with sound absorption foams to keep the noise level low inside. Both the microphone and the device under test is fixed on stable clamps.

The acoustic measurement carried out in literatures to characterize TA device is mainly the SPL spectrum. A SPL spectrum interprets the capability of a sound source to produce sound waves at certain frequencies. The amount of electric power needed to reach sufficient value of SPL can also be obtained from the measurement. A microphone and speaker pair with completely flat frequency response can reproduce the natural sound source without change in all the frequency components. However the nowadays mainstream acoustic components like electrodynamic or piezoelectric speakers suffer from mechanical resonance peaks. The state of the art TA designs (planar heaters) unfortunately produce low amplitude SPL in low frequency range, they do not possess a flat frequency response over the audio band.

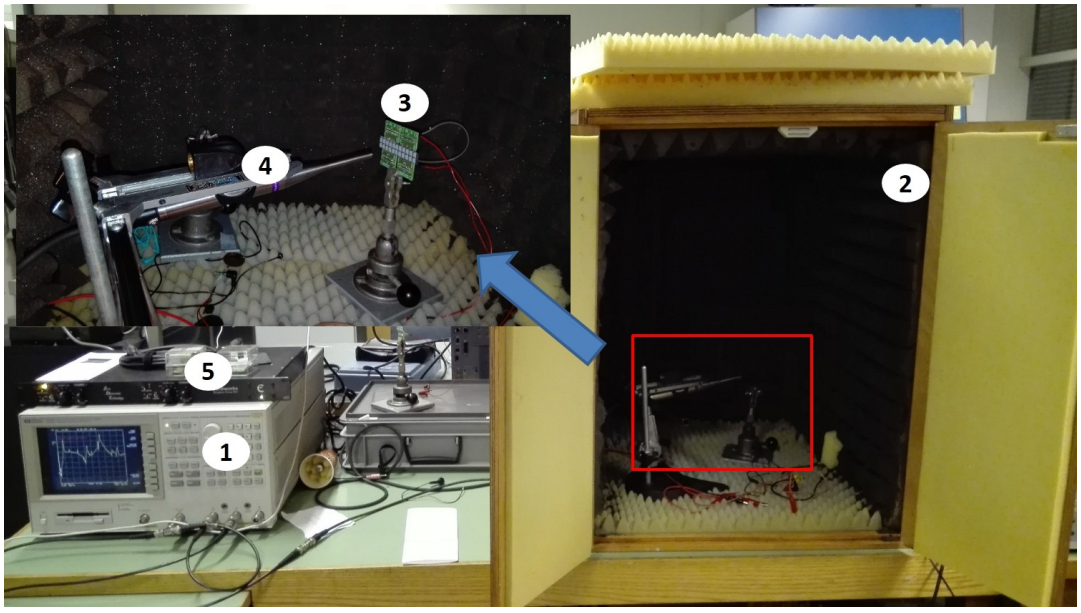


Figure 7.9: A demonstration of the measurement setup used to characterize acoustic performance of sound sources

To compare with our CNT nanofoam thermoacoustic chip, an normal earphone representing electrodynamic sound source and a commercial piezoelectric speaker are tested. The input signal driven into the test

devices is set at 3 power levels of the network analyzer, 5dBm, 10dBm and 15dBm. The unit dBm (decibel-milliwatts) is defined as the power ratio in decibels (dB) of the measured power referenced to one milliwatt (mW). Thus 5 dBm, 10 dBm and 15 dBm equal to 3.2 mW, 10 mW and 32 mW. The input signal is directly feed back to the network analyzer as a reference power level. Network analyzer measures the A/R value in dB, R represent the power of reference signal (input of the speakers) and A represents power of output signal from the microphone preamp. From the measured value of A/R, the voltage from the microphone can be determined. With the sensitivity of the microphone (30 mV/Pa) the acoustic pressure received by the microphone can be calculated. The SPL can be derived from Figure 7.2 below:

$$SPL\,(dB) = 20 \cdot \log_{10}\left(\frac{P}{P_0}\right) \tag{7.2}$$

P is the measured sound pressure from the microphone and P_0 is the reference of sound pressure which is the hearing threshold of human ear, 20 μPa. Equation (7.3) for deriving the sound pressure P from the measurement is given below:

$$P = s^{-1} \cdot V_r \cdot 10^{\left(\frac{MD-G}{20}\right)} \tag{7.3}$$

In Equation (7.3), s is the sensitivity of high precision microphone used in the measurement, for Earthworks QTC50 s= 30 mv/Pa. V_r is the reference voltage. The output of the network analyzer which provides the input signal for the speakers is connected to its reference port. MD represents the measurement data. The network analyzer save the data that is shown on the display and the reference level in terms of dB on the display is usually not 0 dB. Thus to obtain MD, the reference dB level of the display should be subtracted from the raw data. G is the gain of the preamplifier. The gain used in our measurement is 5 dB. V_r at power of 5 dBm, 10 dBm and 15 dBm is in value of 402 mV, 707 mV and 1260 mV at an output impedance of 50 Ω. The different impedance of the devices under test can induce possible mismatch to the voltage value which need further correction or include a power amplifier between source of the network analyzer and the sound sources.

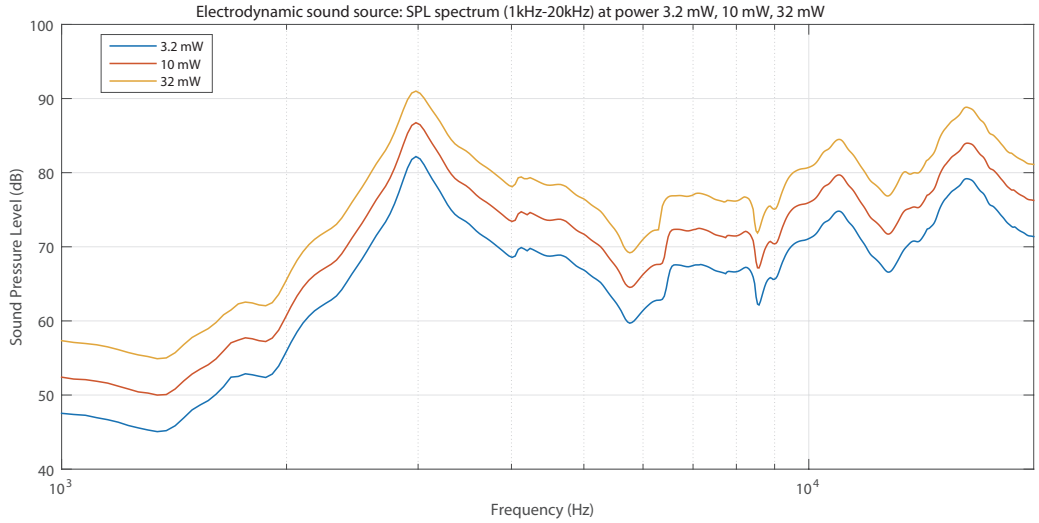


Figure 7.10: The SPL frequency response of a commercial electrodynamic sound source from 1 kHz to 20 kHz at different power levels, 5 dBm (3.2 mW), 10 dBm (10 mW) and 15 dBm (32 mW). SPL increases linearly with the input power (dBm).

The SPL spectrum measured from the electrodynamic (ED) earphone is shown in Figure 7.10. A frequency range from 1 kHz to 20 kHz is swept and the earphone is placed at a distance of 2 cm away from the microphone. Power applied in the measurement are 3.2 mW, 10 mW and 32 mW (converted from dBm). The

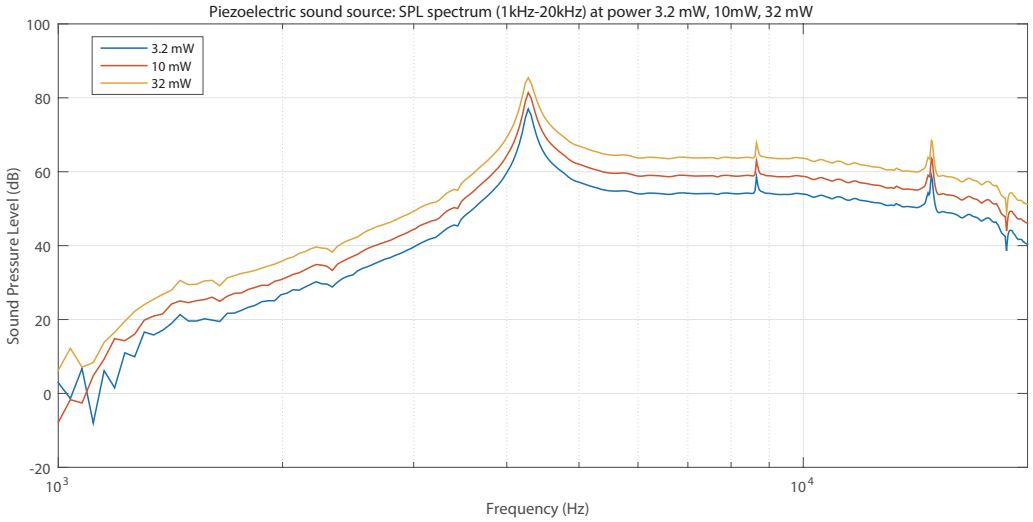


Figure 7.11: The SPL frequency response of piezoelectric sound source, at power of 3.2 mW, 10 mW and 32 mW. Piezoelectric mechanism result in multiple resonance peaks and low performance at low frequency range.

maximum power the network analyzer can generate is 32 mW. The result shows that the electrodynamic earphone has a first order resonance peak at 3 kHz. The increasing input power at step of 5 dB results in the same amount of increase in the measured SPL. Figure 7.11 shows the measurement results of the piezoelectric (PE) speaker. Comparing to the ED earphone, PE speaker has very poor performance at low frequency and a strong resonance peak at 4.2 kHz, other higher orders of resonance peaks appear at 8.6 kHz and 15 kHz. The resonance peaks of PE speaker is very sharp compared to ED earphone.

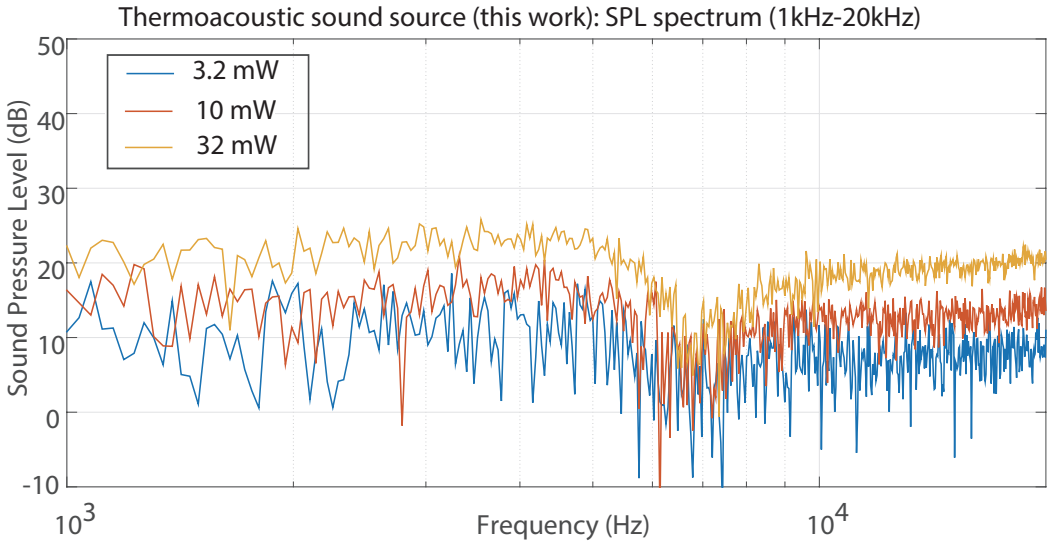


Figure 7.12: The SPL frequency response of thermoacoustic sound source (this work). The SPL response is noisy as shown due to the low sound pressure detected is near the self noise level of the Microphone.

Compared to either PE or ED speakers, TA devices require more power consumption due to its low efficiency. Electrical power from hundreds of mW up to several W is applied to drive TA devices. With the input power of 32 mW, our TA chip produce weak but distinguishable sound. The measurement result of SPL spectrum of the CNT nanofoam device is given in Figure 7.12. The spectrum is noisier at low input power and less noisy in the case of high input power. Because the SPL produced by CNT nanofoam device is close to the

noise level of the measurement environment and is in the range of the microphone's self noise level (22 dB in SPL), the spectrum shown in Figure 7.12 is noisy. For a better characterization of our device, an wide band power amplifier is required to supply more power to the device. However the spectrum that is measured, although noisy, shows a flat frequency response at both low frequency range and high frequency range. A decrease of SPL appear at 7 kHz.

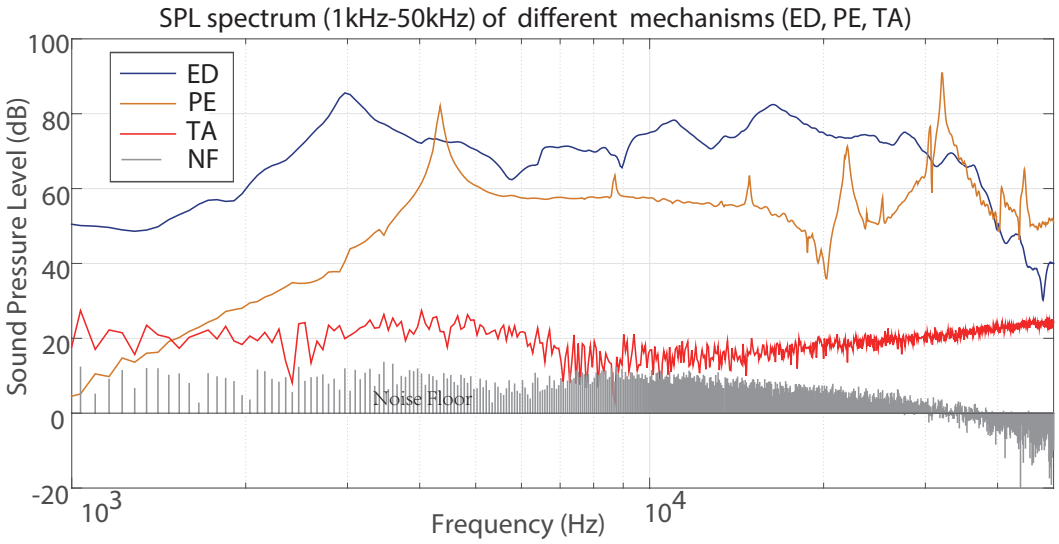


Figure 7.13: Comparison of ED,PE and TA SPL vs frequency (1 kHz to 50 kHz), the SPL frequency response show a wide band flat behavior

A wider frequency band from 1 kHz to 50 kHz is explored, shown in Figure 7.13. From 20 kHz up, SPL of ED earphone drops down significantly. For PE speaker, resonance peaks appear intensively from 20 kHz to 50 kHz. The spectrum of CNT nanofoam TA device shows no resonance peaks and an continuously increasing trend of SPL from 10 kHz to 50 kHz. At frequency range from 1 kHz to 10 kHz, noise floor is close to the performance of CNT nanofoam TA device since there are more low frequency components in the ambient. As the sweep goes up into the ultrasonic range, noise is much less, and the TA spectrum shows a 25 dB up from the noise floor at 50 kHz.

7.4. SUMMARY OF DEVICE PERFORMANCE

Raman spectroscopy of CNTs before and after the post processing steps shows a slightly decrease of quality which can be responsible to the increase of device resistance compared to the theoretical value. The variation of device resistance is severe over the processed wafer. It gives evidence that the process has non-uniformity concerning CNT growth. The measurement of sheet resistance of Al on CNTs shows that the rough interface with CNTs increases the resistance. However the impact is not critical to our design. Due to a low power capability from the network analyzer, maximum 15 dBm (32 mW), the detected thermoacoustic emission is weak. In literatures, power of 1 W usually used for the thermoacoustic devices. In comparison with the performance of TA devices listed in Table 1.1, we normalize the device performance (20 dB at 3 kHz, 10 mW, 2 cm) to an input power of 1 W, measured at 3 cm distance and 3 kHz. Assumptions that sound pressure has linear relationship with distance^{-1} and power. The normalized SPL is around 37 dB which shows that our device has a performance similar to Al film on polymide device [46].

8

CONCLUSION AND OUTLOOK

8.1. CONCLUSION OF THIS WORK

Currently, electrodynamic speakers are composed of many different parts which require assembly after fabrication. Henceforth, the current state of the art technology is not very cost-effective nor suitable for mass-production. However, wafer-level micro-fabrication technology offers scalability since it is a parallel and batch fabrication process which doesn't require assembly steps. The thesis objective is to produce a speaker utilizing the thermoacoustic effect and to employ wafer-level micro-fabrication technology to create a sound source device which is cost effective and suitable for mass production. Our proposed process has achieved 148 devices per wafer, 25 wafers per batch. The whole fabrication cycle is nearly 1 week in our small research facility. A total amount of 14800 devices which potentially delivers 7400 pairs of headphones can be fabricated per month. The mass-fabrication of future thermoacoustic headphones is valuable and profitable.

In this thesis, efforts were made to develop an innovative vertical 3D heater approach for creating an energy efficient, micro-fabrication compatible, thermoacoustic sound source with flat frequency response based on novel LPCVD CNT nanofoam micro/nano architectures. COMSOL simulation with bulk material approximation of CNT thin film and CNT nanofoam is found to be adequate to predict the thermoacoustic performances. In addition, by employing standard cleanroom technologies, CMOS compatible thermoacoustic chips are fabricated on 4-inch silicon wafers and arrays of devices are wire-bonded and assembled on to a PCB. In the end, electrical properties and acoustic performance of the PCB assembly are characterized with high precision measurement tools. The main conclusions of this thesis are as follows:

COMSOL simulation of CNT nanofoam TA device

COMSOL simulation results show that by utilizing heater materials with higher SA:V ratio in a thermoacoustic chip improves the efficiency of sound wave emission. Bulk material approximation of CNT thin film and CNT nanofoam applied in the simulation model is proved to be suitable for predicting the thermoacoustic performance in the frequency range from 1 kHz to 100 kHz. Comparing to the recent 2D thin film thermoacoutic designs, our proposed 3D vertical heater design approach with CNT nanofoam presents a flat frequency response, higher thermoacoustic efficiency at low frequency range,1 kHz to 5 kHz.

Cleanroom fabrication

The proposed fabrication methods achieved a full cleanroom compatibility, scalability and ability of mass fabrication which is crucial advantages over other CNT based designs. The fabrication employs thin film

technologies for material deposition, lithography to define designed patterns and multiple etch techniques. The CNTs are 10 um in height, with Ti bottom metal layer of 1 um thick and Al top metal layer of 5 um thick. Sputtering is used to obtain the metal layers and LPCVD is used to grow CNTs. The CNT growth rate under conditions of 50 nm TiN support layer, 5 nm Fe catalyst at temperature of 550 °C is measured to be 1 um/min which is suitable for accurate height control. HF vapor etch applied to remove the sacrificial TEOS oxide layer is proved to be harmless to CNT nanofoams and effective in removing the surrounding oxide completely.

Challenging processing issues including protection of TiN, preventing bottom metal lift-off in HF vapor etch were optimized and offered better fabrication result. The critical challenge of our proposed process is to narrow down the gap between CNT nanofoam and TEOS oxide. Al sputtering used for top metalization deposits Al inside the gap. This introduced imperfection to the final devices compared to the ideal design model. For optimization of this flaw, a strategy using SiC masking layer is studied. Thick SiC layer of 1 um is proved to have severe stress built up after CNT growth and result in overall cracks. A group of SiC masking layer thickness is studied up to 400 nm which had no crack issues but encountered with breaking off of overhanging edges.

Electrical characterization

Resistance is characterized over 7 devices at different locations on the sample. The measured resistance of devices near the center of the wafer shows a better match with the theoretical value. A non-uniformity in accordance with non-uniform CNT growth in respect of quality and height is observed. Based on the measured resistance, Al deposition in the gap is not dominating the electrical property of the CNT nanofoam device. The current is mostly conducted through CNTs. The linear IV measurement show that the final device is resistive and the central dies with good quality CNTs has a resistance around 0.02 Ω. Measurement on greek cross structure indicates that Al thin film over CNT nanofoam has an 63% higher sheet resistance than Al on TEOS oxide, 2.01 $\times 10^{-3}\Omega$ over CNTs and 1.23 $\times 10^{-3}\Omega$ over TEOS oxide respectively.

Acoustic characterization

Audible sound that can be detected by human ears is generated by our CNT nanofoam device. In comparison with electrodynamic and piezoelectric sound source, our TA device has shown a promising flat frequency response. Our test device array with 8 devices connect in sires has achieved a SPL around 20 dB at input power of 10 mW, frequency of 3 kHz and distance of 2 cm. Base on the measurement result, an SPL of 37 dB normalized to a 1 W input power, 3kHz, distance of 3 cm can be achieved by our device. The flat frequency response of the fabricated device matches with our simulation, however the acoustic emission is around 30 dB lower than the simulation. This deviation from the ideal design can be caused by the Al deposition on the side wall of CNT nanofoams which blocks the air expansion.

8.2. RECOMMENDATION FOR FUTURE DEVELOPMENTS

- Masking layer technique is a promising approach to eliminate the gap between CNTs and TEOS oxide. More materials need to be explored. Material properties such as good adhesion on TEOS oxide, deposition temperature lower than 500 °C, high stiffness and strength, easy to be etched, thermal stability at 550 °C and chemically stable in the gas environment used to grow CNTs are the critical features.

- The approach to construct the 3D vertical CNT nanofoam heater in this design requires TEOS oxide sacrificial layer which limits the aspect ratio of CNTs and has processing challenge with the gap to the CNT nanofoam. Future designs can focus on simpler approaches to create the top electrical connection, for an example techniques can be applied to change the growth direction of CNT bundles to form a connection between 2 bundles.

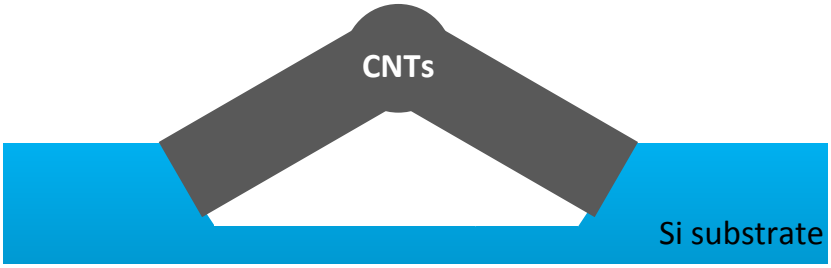


Figure 8.1: Self connection made by as grown CNT bundles, in this way further top metalization is not needed

- The 3D vertical heater design approach for thermoacoustic devices has shown its potential on ultra flat frequency response over wide range. The architecture of the heater array, whether it is an open system (2D planar) or a close system, has an influence on the frequency response of a TA device. Future works of exploring more 3D vertical heater structures and combining vertical and planar heaters in one design for frequency compensation is recommended.
- Our proposed fabrication process can scale down to construct a large array of acoustic units on a small surface area. This feature is suitable for the application of controlled phase arrays to sweep sound beams in space. It can contribute to indoor localized audio experience, directional sound emission, ultra high precision sound field reproduction, audio enhancement for virtual reality products.
- The proposed CNT nanofoam design has potential to be a microphone as well by employing the reverse of thermoacoustic physics. With special design of the structure, the incident pressure waves can be accumulated inside the cavities thus altering the air molecule density and velocity near the CNT nanotubes which can potentially induce changes of resistance.
- Our proposed fabrication approach can be used to construct CNT nanofoam heaters inside a microchannel to heat up and evaporate fluid. The nano dimension of CNTs can result in nano scale bubbles. It can be potentially used as the heater for micro thrusters.

A

APPENDIX-A

A.1. A BRIEF HISTORY OF SOUND SOURCE

Before any form of electrical speakers are invented, horns were the earliest equipment for audio amplification. Horns can normally be found together with phonograph which is driven mechanically. The magnification of amplification of a horn is very much limited. Thomas Edison, Magnavox, and Victrola all developed advanced and well-performing horns from 1880 to the 1920's. The horns occupied the market for more than 40 years until a good performance standard electrodynamic loudspeaker which uses a magnetic field to move a coil or magnet that is connected to a diaphragm was first built.

The exploration of electrodynamic loudspeaker begins much earlier than its practical application. In 1861, a simple type of electronic loudspeaker was developed by Johann Philipp Reis, a teacher at Friedrichsdorf, Germany. The speaker was crudely able to reproduce noise and just an experiment. In 1876, Alexander Graham Bell also tried to produce a speaker based on Reis's work. At this time in history there was not enough base knowledge in physics and material engineering to allow Bell or any other inventor the ability to successfully produce an electrodynamic loudspeaker. The need to amplify sound and telegraph signals over long distance did help spur the development of amplifiers, which is an important component of audio systems later on. From 1877 onwards, The idea of the electromagnetic coil driven speaker is formulated by Werner Von Siemens, he used it with input signals of DC transients and telegraphic signals. He had no way to amplify sound to create a useful speaker, but he theorized that this could eventually be done. Between 1877 and 1921, Various inventors and engineers played with the idea of the electrodynamic loudspeaker but could only create rough distorted sounds. There was no way to electrically amplify the signal to create very loud sounds. The industry continued to rely on more advanced horns to create amplification.

C.W. Rice of General Electric and E.W. Kellogg of AT&T worked together in Schenectady, New York to develop the modern speaker and first electric amplification system. They created a working prototype in 1921. Rice and Kellogg solved the final problems which led to a nice crisp sound. Previous attempts to make the loudspeaker created an unacceptable muffled sounding audio. This muffled sound was not good enough to compete with the horn which was well established in the market. Rice and Kellogg were able to fully understand the reproduction of all the frequencies which are necessary to create an accurate audio sound. Their prototype had enough of a dynamic range in frequencies to be better than the horn, while possessing the ability to greatly increase loudness (dB). In 1925 they filed for patents and made a speech in St. Louis to the

AIEE. After several years of work they perfected it as the first commercial product of its kind called the Radiola Loudspeaker #104. The speaker was produced under the company name of RCA.

A.2. NOVELTY

A detailed comparison of our proposed design with other CNT based TA device are included below:

- **CNT thin film over CNT arrays** [24]
  Difference: 1), The heating source is CNTs thin film on a lateral plane, which is 2D plannar TA device. Although aligned CNTs are used to provide vertical current from substrate, it does not serve as the heater. In our design, we use vertically aligned CNTs as heating source, our design is a 3D TA device. 2), Our design requires no CNT transfer nor laser patterning. 3), Our design has top and bottom metallization to anchor CNTs while their design has no anchoring of CNTs which induces less robustness compared to our design. 4), Our design is compatible with cleanroom fabrication and their's are not.
  Similarity: 1), Both use CNTs as heat material. 2), Both are on-chip devices.

- **CNT thin film** [9, 23]
  The CNT Thin Film TA Device induced by Xiao, et al. is known to be transparent, flexible, stretchable, and can be tailored into any shape and size, freestanding or on any insulating surfaces.
  Difference: 1), We use vertically grown CNTs as a heater which is a 3D design, with top metallization of the CNTs to create out of plane zigzag current flow. However, CNT thin film device proposed by Xiao, L. is a 2D design. The air volume affected by thermoacoustic effect is limited; 2), Our device is scalable with cleanroom technology, patterns are achieved by lithography and requires no additional process of fabricating CNT thin film, nor transferring CNTs films. 3). The CNT TA device by our approach focus on improving the acoustic performance, power efficiency and compatibility with low cost mass production, different from the CNT thin film device, we plan to develop transparency and flexibility when major challenges are desirably solved. Similarity: 1), Both use CNTs as the heating material.

- **CNT thin film** [10]
  Based on the findings of the CNT thin film device, CNT thin yarn device is then proposed by Wei, Y. et, al. This design developed an on-chip device with CNT thin films patterned by laser beam and then condensed into yarns in an atomization bath. Further to improve the performance, the silicon substrate is patterned and coated for purpose of thermal isolation. The device is finally packaged with a CQFP64N casing. They report a power efficiency (sensitivity) of 48 dB/mW with a 9.5mm x 9.5mm chip packed inside a normal earphone. Commercial earphone performance requires ˜100dB/mW. The thin yarn device is thus 17 times more power consuming.
  Comparing with our design: 1), CNT thin yarn device is still a 2D design, while we introduce 3D zigzag current driving CNT TA device. 2), CNT thin film fabrication, transfer, tailoring, atomization are required with CNT thin yarn device, while our design doesn?t have above costly additional steps. 3), Devices are fabricated directly on one Si wafer in our design, unlike the thin yarn 2D device which require wafer to wafer transfer and assemble. Similarity to our design: 1), Both use CNTs as the heating material; 2), Both are on chip devices with feasibility of packaging.

- **CNT forest and CNT sponge** [16]
  CNT forest and CNT sponge designs are mentioned in this paper by Aliev. As described, CNT forest and CNT sponge are 3D nanostructure and are believed to have larger heat exchange interface. These devices are made in a way less compatible with cleanroom fabrication process, lack the ability of scaling

and patterning but cost effective. The power efficiency (sensitivity) however is much lower than CNT thin film devices, around 40dB lower at 3kHz by rough calculation.

Difference: 1), Bulk (continuous large area of forest and sponge) CNT TA devices are in fact quasi-3D design, the current flow is not directed to out-of-plane routes, unlike our design. 2), Bulk CNT TA devices proposed by Aliev have no patterning features, while our design stress on free air passages (hexagonal openings) to easily release the pressure waves. 3), Similar with CNT thin film and thin yarn TA devices, the bulk CNT designs have exposed CNTs on the device surface, however with our design CNTs are anchored by metal layers, the surface of the device are covered with Al layer, which gives our device better robustness and makes it more user/environment friendly. 4), Bulk designs are not on-chip devices and not compatible with mass production, unlike our design. Similarity: 1), Both use CNTs as the heating material; 2), Use as grown CNTs.

A.3. COMPLETE SCHEMATICS OF PROCESS FLOW

- The original design of process flow:

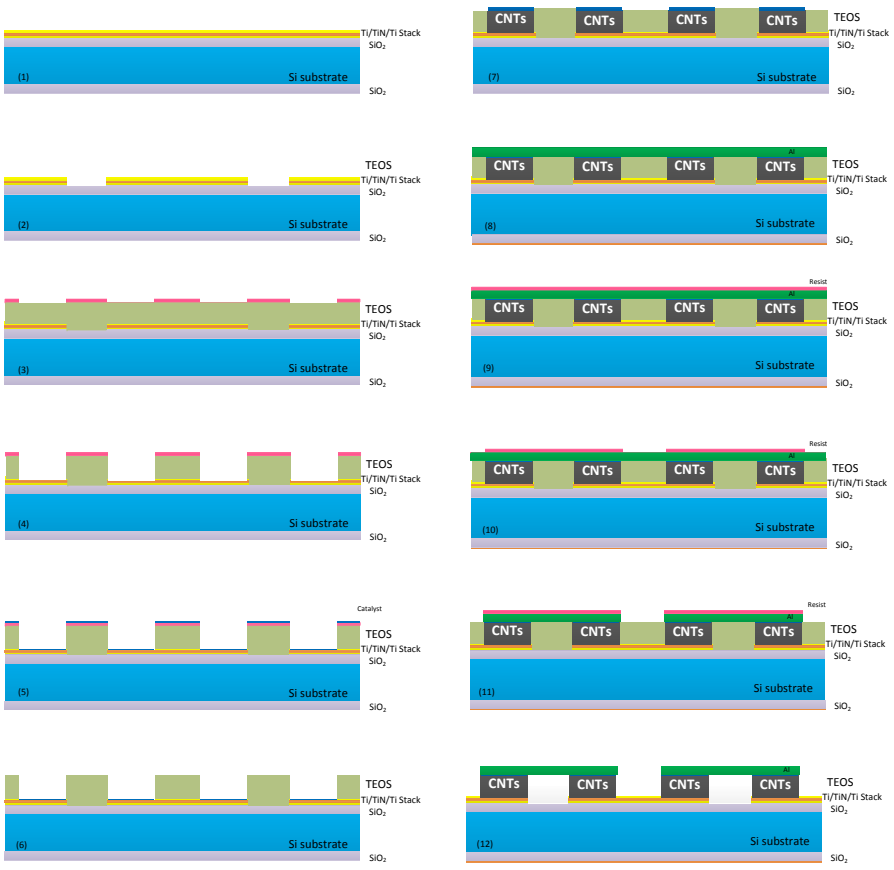


Figure A.1: A simplified schematic of the original process flow

- The optimized design of process flow to solve the encountered challenges:

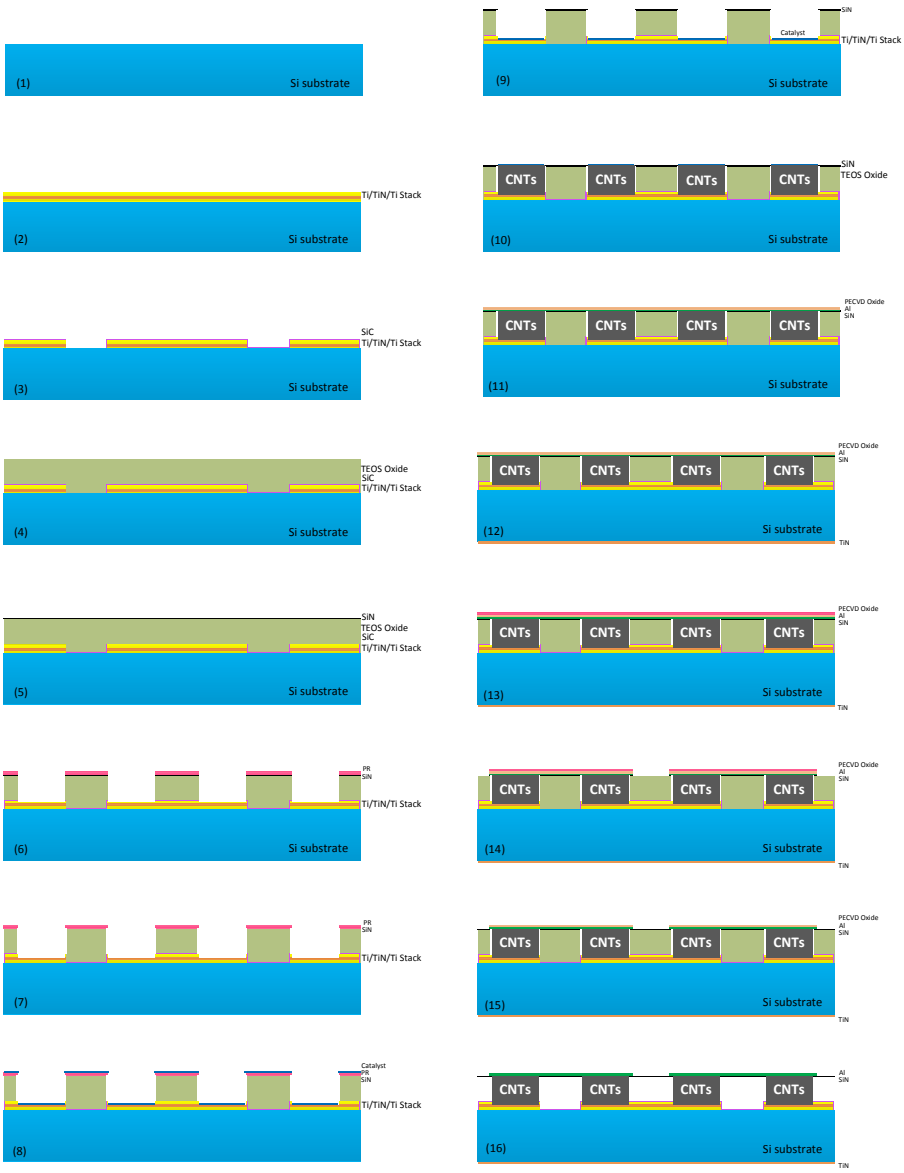


Figure A.2: A simplified schematic of the optimized process flow

A.4. SUPPLEMENT FOR PROCESS RELATED ISSUES

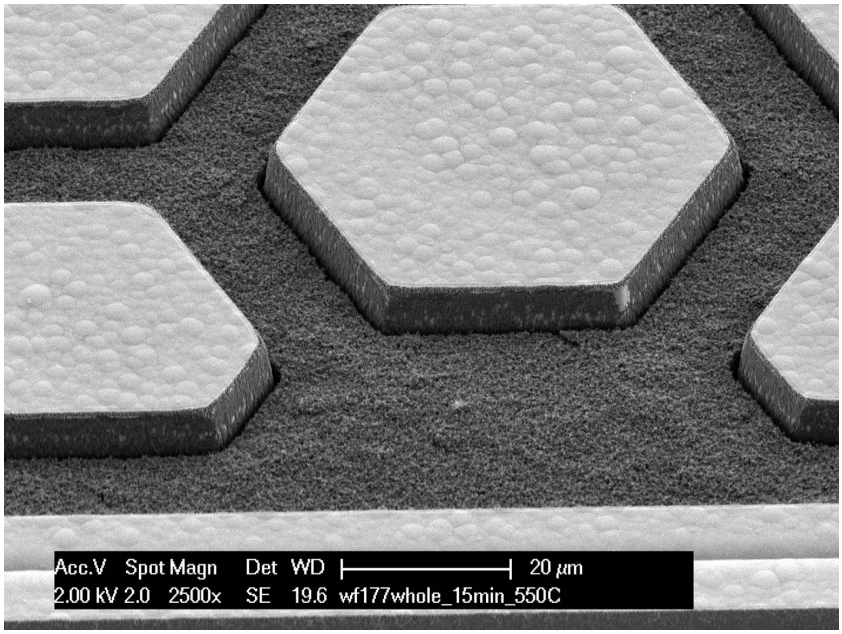


Figure A.3: Height limitation of CNTs after applying HF(0.55%) to remove Ti sacrificial layer, amorphous carbon is formed on top of the CNTs, the wafer is processed for 15 mins with an expected height of 15 um, however it stopped grow at a early stage, this can be caused by the HF(0.55%) bath which has changed the surface condition of TiN.

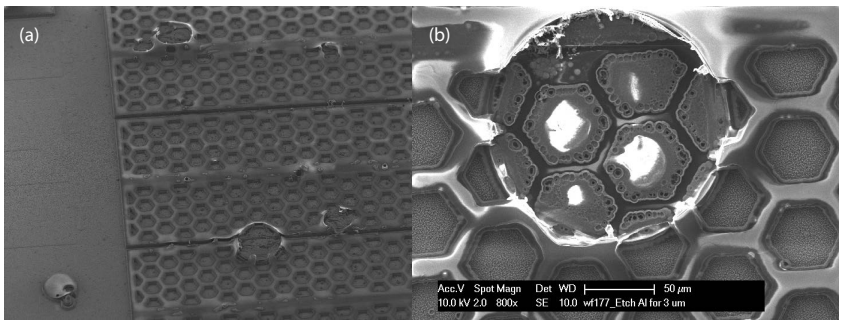


Figure A.4: The bubbles inside photo-resist that are produced by the air expansion from CNTs when heated, it is catastrophic issue since re-coating requires removal of the photo-resist, either plasma striping or ultrasonic bath in NMP to remove photo-resist can damage the CNTs. It is recommended to put thick enough TEOS oxide to seal 100% before coating

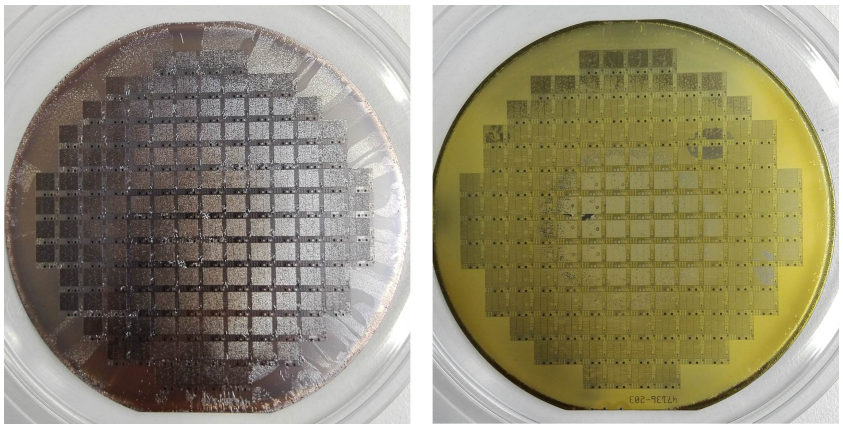
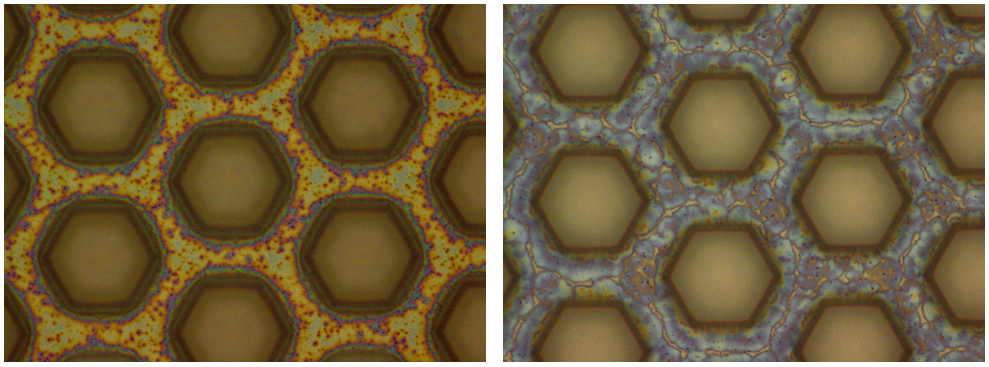


Figure A.5: (Left), wafer with 1 um thick SiC masking layer after CNT growth which is cracked all over the wafer, (Right), Bad adhesion of photo-resist after long steps of dry-etching on SiN masking layer



(a) Oxide residue which is preferablely to be removed completely in the TEOS oxide dry etching, since the residue can increase the time to remove all Ti sacrifial layer beneath which can enlarge the TEOS-CNT gap.

(b) The damaged Ti layer shows a blue color that is quite different from the oxide residue, an uniform non-damaged Ti layer is prefered during the dry etching since any damage of Ti layer as shown in the image has protential to cause the damage of TiN as well.

Figure A.6: The difference of remaining oxide and damaged Ti sacrificial layer under optical microscope.

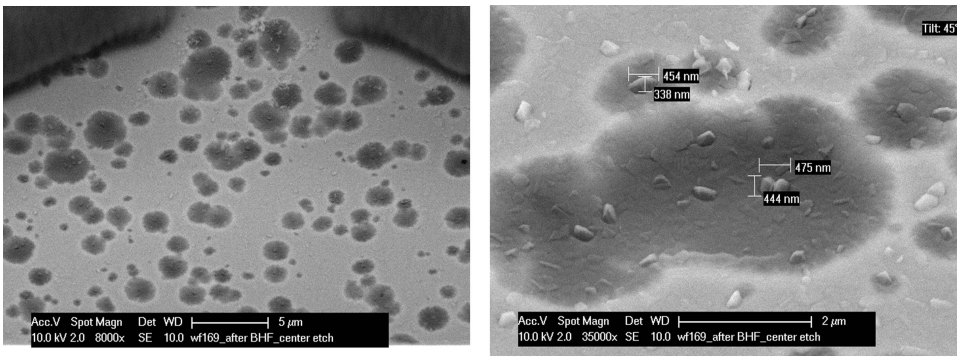


Figure A.7: SEM images of damages on TiN layer, black dots. This damage is not catastrophic, CNTs can still grow on the TiN if the dots density is not too high, however the growth on the dots are largely affected which can result in doted pattern in the grown CNTs as well.

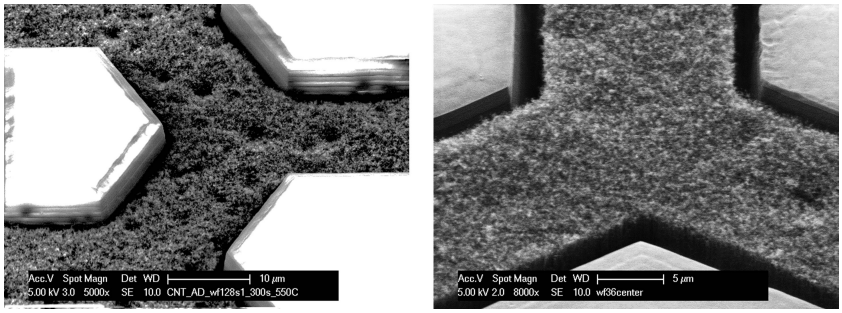


Figure A.8: (left), non-uniform growth caused by dots on TiN layer, as observed that the height of CNTs at the dots are much lower and result in holes in the nanofoam, (right), the desired flat and uniform CNT nanofoam grown on good quality TiN.

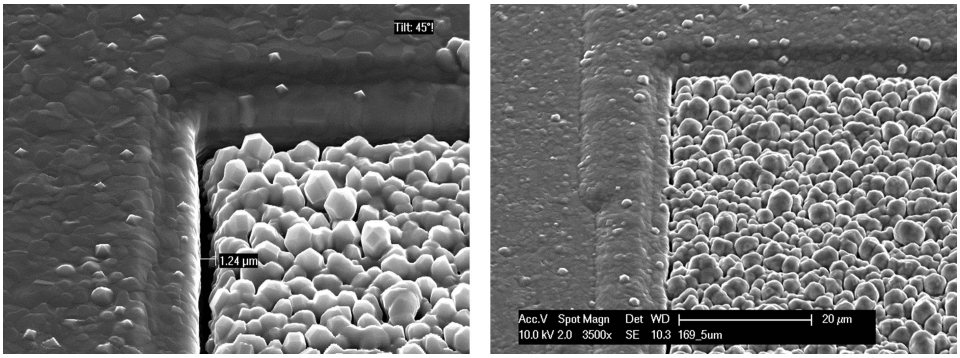


Figure A.9: SEM images showing 3 um Al sputtered on CNTs (left) and 5 um Al sputtered on CNTs (right), this shows the step coverage is not sufficient to close the TEOS-CNT gap and pinholes. It is expected from the images that 10 um Al is required to obtain uniform surface.

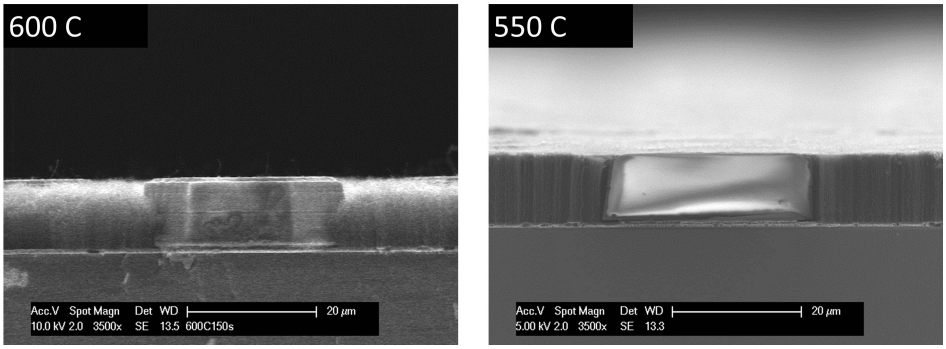


Figure A.10: CNTs grown at 550 °C and 600 °C, 550°C result in more uniform height of CNTs, and 600°C gives a more aggressive growth and less accurate and conformable height control.

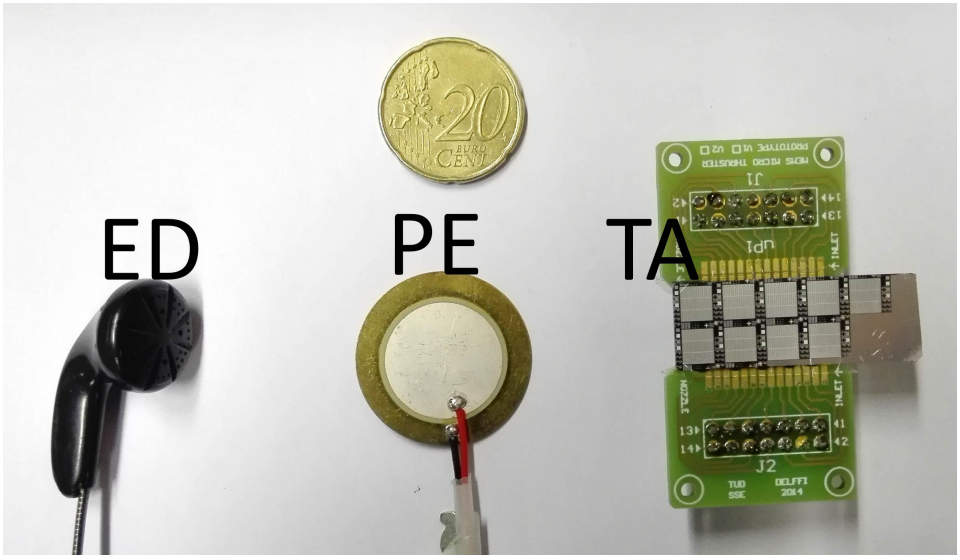


Figure A.11: Devices under test in the acoustic measurement, from left to right is the electrodynamic device, piezoelectric device and our TA device. They have approximately the same device area.

B

APPENDIX-B

B.1. RECIPES USED IN THE PROCESS

Table B.1: Standard Oxide Etch in DRYTEK TRIODE 384T

Recipe Name	StdOxide	Etched material	SiO_2 or TEOS
STAB.(SECs)	15	GAS EVAC.(SECs)	5
C_2F_6 Flow(CC)	36	CHF_3	144
He Pressure (T)	12.00	Pressure (mT)	180
RF Power (W)	300		

Table B.2: Sodt-landing Oxide Etch in DRYTEK TRIODE 384T

Recipe Name	StdOxide	Etched material	SiO_2 or TEOS
STAB.(SECs)	15	GAS EVAC.(SECs)	5
C_2F_6 Flow(CC)	36	CHF_3	144
He Pressure (T)	12.00	Pressure (mT)	180
RF Power (W)	100		

The difference between the soft-landing recipe and the standard recipe is the RF power that maintains the plasma. In soft-landing recipe power of 1/3 of the standard recipe is used. However to start the plasma, the standard recipe is in need, thus the soft-landing procedure is consist of 2 steps. First step is to start the plasma with 300 W for min 3 seconds, and then lower the RF power to 100 W to maintain the plasma environment.

Table B.3: Recipe to Etch SiC

Recipe Name	SIC-CDB	Material	SiC
Helium BR (Torr)	9.5±5%	Pressure (mT)	50±10%
Oxygen (sccm)	20±5%	SF_6 (sccm)	20±5%
RF Power (W)	50±20%	ICP Power (W)	500±20%

Table B.4: HF Vapour Etch Recipes

Recipe Name	Pressure(torr)	HF(sccm)	EtOH	N_2	Regulator	ER(A/min)	Uniform(R/2x%)
Recipe1	125	190	210	1425	7.75	143	2.9%
Recipe2	125	310	350	1250	7.75	473	5.2%
Recipe3	125	525	400	1000	7.75	1086	3.4%
Recipe4	125	600	400	910	7.75	1321	1.3%
Recipe5	125	720	325	880	7.75	1599	1.3%

In HF vapor etch, recipe5 is used for its sufficient etch rate.

B.2. Specification of Earthworks QTC50

Frequency Response: 3 Hz to 50 kHz ± 1.5dB
Polar Pattern: Omni-directional
Sensitivity: 30 mV/Pa (-30.5 dBV/Pa)
Power Requirements: 48 V Phantom, 10 mA
Max Acoustic Input: 142 dB SPL
Output: XLR (pin 2+)
Output Impedance: 100 Ω, balanced (50 Ω ea. pin 2 and 3)
Min Output Load: 600Ω between pins 2 and 3
Noise: 22dB SPL equivalent (A weighted)

B.3. Flowchart

The flowchart used in our process is provided in Appendix-B, start from next page.

Flowchart: EC1962

1. COATING AND BAKING

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas,
spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **Co – Zero Layer** (resist thickness: 1.400 µm).

2. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.
Follow the operating instructions from the manual when using this machine.
Use **COMURK mask**, the correct litho job **epi0.0** (14 marks for only stepper) and the correct exposure energy (140mJ/cm^2).

3. WAFER NUMBERING

Keep track on all wafers by the numbers at the main flat. Wafers that is without numbers can be numbered by scratching the photoresist near the flat.

4. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using
Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development program: **Dev - Single Puddle**.

5. INSPECTION: LINEWIDTH

Visually inspect the wafers through a microscope, and check the linewidth. No resist residues are allowed.

6. PLASMA ETCHING OF ALIGNMENT MARKS

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch program may not be changed !

Use sequence **URK_NPD a**nd set the platen temperature to **20 °C** to etch **120nm** deep ASM URK's into the silicon.

7. CLEANING PROCEDURE: TEPLA + HNO_3 100% and 65%

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1

Cleaning	**10 minutes** in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	**10 minutes** in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. Use wet bench "HNO_3 (65%)" and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

8. Ti/TiN/Ti deposition

Use the TRIKON SIGMA sputter coater for the deposition of the Ti and TiN metal layer on the process wafers.
The target must exist of 100% Ti.
Follow the operating instructions from the manual when using this machine.

Use recipe Ti_1000nm_TiN_50nm(DEP_B), 350C to sputter a 1.0 ± 0.2 µm thick layer of Ti, followed by reactively sputtering a 0.050 µm thick layer of TiN (to prevent oxidation of Ti). Add dummy wafers inbetween as required. Temperature = 350 °C. Use Ti_inbetween module for target clean after TiN reactive sputtering.

Test wafer: sputter Ti_500nm_TiN_50nm at 350C.

Perform a target clean and deposit an additional 500 nm of Ti (500nm @350C) to act as sacrificial layer. The Sac layer is used to protect TiN layer from the overetch of TEOS for around 5mins.

PLAN B: If the thick Ti sac layer dosen't work, we can do a combination of a bit wet etch of the TEOS and remove the Ti; Or do a pre-etch around 1-2 um only to the central part of the wafer(dry-etch), remove the resist and then coat the 6um resist for dry etch again. Or Just put the devices in the central region.

Visual inspection: the metal layer must look shiny.

9. COATING AND BAKING

Use the EVG 120 Coater/developer to coat the wafers with resist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95degC for 90 seconds.
Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use Coating Program "CO-3012-2.1um" .
2.1um thick resist layer for etching 1.55um thick Ti/TiN/Ti stacks.

10. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic waferstepper.

Follow the operating instructions from the manual when using this machine.
Use Mask(box460, slot8): **EC1962_V1**.
Reticle ID: **3X3**
Litho job: **DIE6x6_9IMGS** (User_data/jobs/diesize_6mm).
Exposure energy: **320 mJ/cm^2**.

11. DEVELOPMENT

Use the EVG 120 wafertrack to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 degC for 90 seconds, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds.
Always check the temperature of the hotplates first.

Use development program: **Dev - Single Puddle**.

12. Inspection of wafers after development. Make sure all lines are open.

13. Ti/TiN/Ti Etching

Use the Trikon Ωmega 201 plasma etcher to etch Ti /TiN/Ti stacks.
Follow the operating instructions from the manual when using this machine.
The process conditions of the etch and passivation program may not be changed!

Use sequence **TiNTiSVO** to etch Ti/TiN/Ti stacks at a platen temperature of 25 °C, the etch rate of TiN is around half of Ti layer.

TIME 2:05 min+ 5 seconds over etch (for 1000nm50nm500nm stack). In the recipe, change only the main etching time.

14. SiO_2 thickness measurement

There are large areas in this design, which SiO_2 thickness can be measured directly, don't need to add test wafers.
The thickness of the Oxide measured in this step must be smaller than the ones measured in **step.9.**

15. Use Tepla to remove the resist + Clean the wafers with 99%HNO_3(Metal).

16. DEPOSITION OF 5um TEOS. (Deposition rate is aound 3.785nm/s.station, 7 stations in total)

Use the Novellus PECVD reactor to deposit a **5 µm** thick TEOS-based silicon oxide.
Follow the operating instructions from the manual when using this machine.

Use **recipe xxxnmTEOS at 350°C.** Change the deposition time (**seconds per station**) according to logbook.

For all process wafers.
Time per stage: 188.68s
TEOS total thickness: 5um

17. Measurement of TEOS thickness.

Use program **NovellusStdTEOS on Si** to measure thickness of TEOS. And calculate the deposition rate: $\mathbf{R_{new}}$.
(The reflection property of Ti is almost the same as Si. Measure at the area with Ti underneath)

18. DEPOSITION OF 5um TEOS.

Use the Novellus PECVD reactor to deposit a **5 µm** thick TEOS-based silicon oxide.
Follow the operating instructions from the manual when using this machine.
Use **recipe xxxnmTEOS at 350°C. Change the deposition time (seconds per station) according to logbook.**

For all process wafers.
Time per station: 188s (Adjust the time here according to $\mathbf{R_{new}}$)
TEOS total thickness: 10um

19. Repeat step 18 and 19 to obtain thicker layer.
For thicker layer uniformity and stress could be an issue

20. Cleaning before SiC deposition.

Cleaning 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO3 (100%)" and the carrier with the red dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 M□.

Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

21. SiC Deposition

Use Novellus PECVD to deposit SiC masking layer.
Recipe: LS800_2 (deposition rate: 10nm/s)

22. COATING AND BAKING
Coating should be done immediately after Mo deposition to ensure wafers are clean, standard cleaning line process is not possible with Mo on the surface.

Processing will be performed on the EVG 120 wafer track automatically:
Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.
The splashing ring need to be removed before the coating process of AZ9260.

Use Coating Program "AZ9260 resist, co-syr-9260-6um, selectivity is around 3.
For all process wafers: 6um.
Wait for 15min after coating the 6um AZ9260 resist before exposure.
Clean the backside with acetone if the recipe has no EBR. Because it is a thick resist layer, there will be resist on backside after coating.

23. INSPECT THE BACKSIDE OF WAFERS
Inspect if there is resist on the backside of the wafers. Clean the backside with acetone and cotton stick before going into stepper.

24. ALIGNMENT AND EXPOSURE
Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use **EC1962_V1 from Box 460**, Recticle ID: **3x3.**
Job:
DIE6x6_9IMGS
IMG3(30um),
IMG4(50um),
IMG5(70um).

and Follow the suitable exposure energy **600mJ/cm^2** for 6um AZ9260 resist on the logbook.
Wait also for 15mins after the exposure.

25. DEVELOPMENT
Manual development with AZ400K developer. AZ400K(1:2) approximately 90 s.

26. INSPECTION: LINEWIDHT AND OVERLAY
Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

27. Dry etch SiC in Trikon Omega dry etcher

Recipe: SiC_cdb
Etch rate: 284 nm/min

28. Plasma Etching of TEOS Oxide: CNT patterns.
Use the Drytek 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
a). Use program **stdoxide**, etch time as 1min/cycle, calculate the etch rate $\mathbf{R_{teos}}$ (around 11.5nm/s).
b). Etch for **12** cycles.
c). Use program **plsoxide,** copy as **MagwegDY**, set 2 min/cycle for soft landing, etch rate is expected to be 1/3 of R_{teos}. Etch for **4** cycles.
d). Inspect all wafers, if residue remains, continue with 1 min/cycle with soft landing recipe.

29. Sacrificial layer Removal
Use BHF(1:7) to remove Ti Sacrificial layer. Time is around **8 mins.** It is safer to etch in steps and inspect.
Go into Tikon to remove the surface tension first.
(Etching of Ti in 0.55% HF is really fast and not good with CNT growth, observed CNT growth stop around 10um with 15um deep TEOS trench in wf174, BHF is believed to be better solution to remove Ti sac layer)

30. CATALYST DEPOSITION

Use the CHA Solution e-beam evaporator to deposit 5 nm **Fe** directly on the TiN surface.
Use dedicated contaminated shields!

31. LIFT-OFF @ SAL

Perform lift-off procedure with NMP. Put the liquid in a beaker and use the ultrasonic bath for 10-15 mins.
Change the liquid after a few wafers.

32. RINSE & DRY @ SAL

Rinse the wafers in DI and dry using manual dryer **with special Cu chuck.**

33. INSPECTION @ SALAB

Visually inspect the wafers through a microscope, check if catalyst layer remained on surface.
Put paper under wafer and throw away paper after use.

34. CNT GROWTH

Use the AIXTRON BlackMagic Pro to grow CNTs using **LPCVD at 550°C.**

Use recipe: lpcvd_subref_waittemp_v3_550
Recipe includes an activation step (3 min) in H_2 environment at 550 or 600 °C, followed by CNT growth using 700/50 sccm H_2/C_2H_2 at 80 mbar for 10 minutes. Check growth rate with 1 test wafer, make 4 samples out of it. **600 s** results in approximately 10um CNTs. Due to uniformity and metallization considerations, it is better to use **600~660s**.
Use contaminated reactor interior!

35. SEM of CNT height
Make some SEM photos of the top view, side view and cross-section view of the CNTs
(*For samples, attach them with carbon tape on a carrier wafer; for whole wafers, use the cross section holder which is considered as contaminated, should see **no gaps** between the CNTs and Mo masking layer.*)

36. METALLIZATION @ Class 100
Use the TRIKON SIGMA sputter coater for the deposition of the Ti and Al metal layer on the process wafers.
The target must exist of 100% Ti.
Follow the operating instructions from the manual when using this machine. **Use a dedicated transport wafer(with grooves) to prevent contamination!**

Use recipe Ti_100nm_350 to sputter a 0.100 ± 0.1 µm thick layer of Ti @ **25 °C (1 kW)** followed by AlSi_2000nm_stack_RT @ **50 °C**. The objective is to obtain conformable deposition of Al.

Visual inspection: the metal layer must look shiny.

37. SEM INSPECTION OF AL METALLIZATION
To proceed to next steps, there must be no gaps between CNTs area and TEOS area.

38. COATING AND BAKING
Use the manual coater with Cu chuck to coat the front side with 3 µm of SPR3017M photoresist and perform a hard bake at 100°C. Use dedicated Cu chuck and a dummy wafer underneath during the bake.

39. BACKSIDE CLEANING
Remove any Fe contamination from the backside. Use 10% HNO_3 to etch Fe from backside for 5 minutes @SAL.

40. Use BHF(1:7) solution in SAL to strip backside oxide, etch for 5 minutes. Remove solution after process.
Dry using Si chuck after backside contamination removal!

41. CLEANING PROCEDURE: ACETON + HNO_3 100% (METAL) (@SAL)

Acetone	Dissolve the photoresist in acetone at 40°C. Time = ± 1 minute. Use wet bench "aceton" and the carrier with the two red dots.
Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 (100%) metal"and the carrier with the red and yellow dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

42. COATING AND BAKING
Processing will be performed on the EVG 120 wafer track automatically:
this includes a HMDS (hexa methyl disilazane) treatment with nitrogen carrier gas , the coating with Shipley SPR 3027 resist (spin velocity 3430 rpm ; spin time 30 s) , and prebaking for 1,5 minute at 95 °C.

Follow the instructions specified for this equipment, and always check the temperature of the hotplate first.

Use Coating Program “CO-SPR3027-3.1 um” (resist thickness: 3.080 µm at 48% RV).

43. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Mask: **EC1962_V1**,
Job: **DE6x6_9IMGS, (IMG6, 7, 8)**
Exposure energy E = 420 mJ/cm^2.

44. DEVELOPMENT

After exposure a post-exposure bake at 115 °C for 1,5 minute is performed on the EVG 120 wafer track, followed by a development step using Shipley MF322 developer (Dev-SP) and a postbake at 100 °C for 1,5 minute . Follow the instructions specified for this equipment, and always check the temperature of the hotplates first.
Use development program “Dev- SP”.

45. INSPECTION: LINEWIDTH AND OVERLAY

Under optical microscope overlay can be well observed, the roughness difference of Al on CNTs and TEOS ensures a clear observation.

46. Al and Ti etching

Use the Trikon Ωmega 201 plasma etcher to etch titanium and aluminium. **During this step all CNT bundles are covered by both a metal layer and the photoresist!**
Follow the operating instructions from the manual when using this machine.
The process conditions of the etching and passivation program may not be changed!

Use sequence AL5_350 at a platen temperature of 25 °C.

SEM inspection after Al and Ti etching.

47. CLEANING PROCEDURE: Tepla + HNO_3 100% (METAL)

Plasma strip Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1.

(Aceton will not work as a resist exposed to a plasma cannot be removed by aceton easily. If you want to do this wet, use NMP (clean, not the lift-off bottle) for a few minutes at 70 °C, or use tepla.)

Cleaning 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature.
Use wet bench "HNO_3 (100%) metal”and the carrier with the red and yellow dot.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

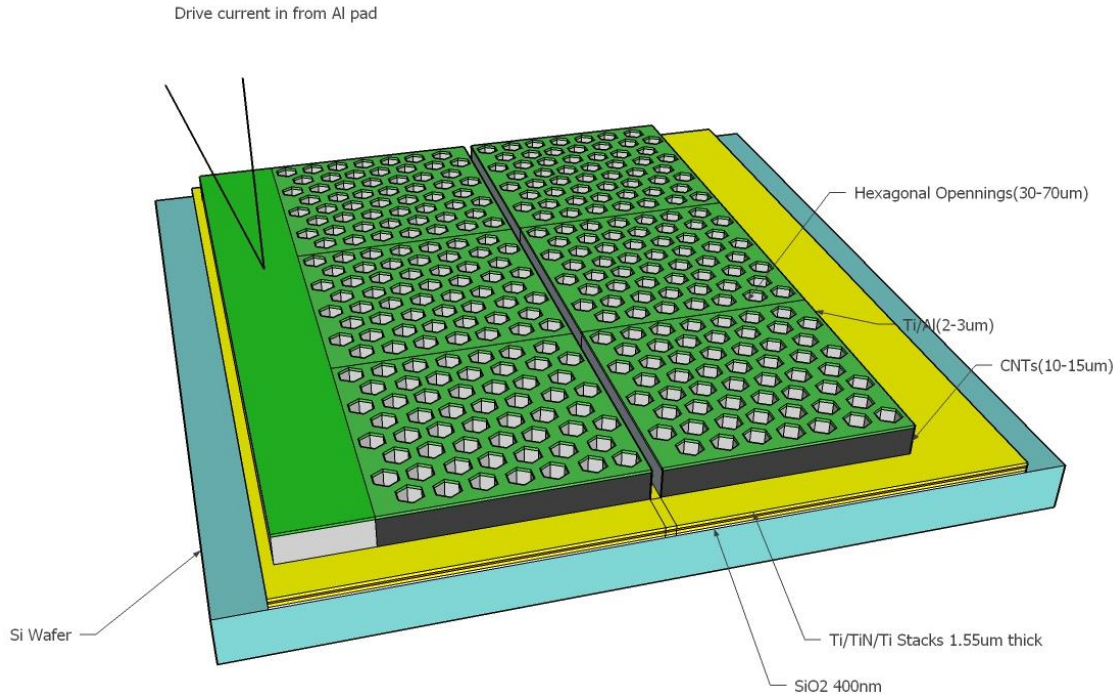
Drying Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a black dot.

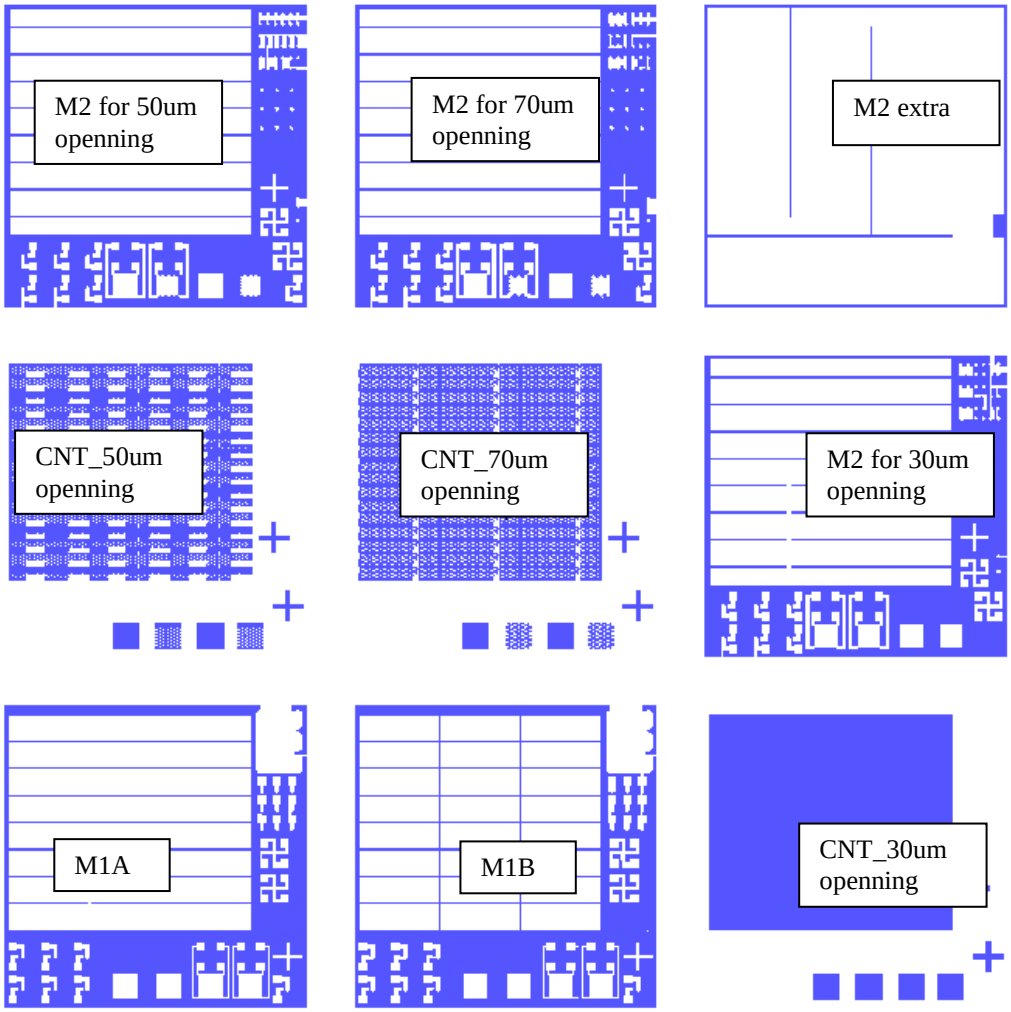
48. HF vapour Etching of remaining TEOS, to expose the CNTs.

Use recipe 5, 6 min/cycle, 6+1 cycles (1 cycle for over etch), etch rate is nearly 1682 nm/cycle.

49. SEM Inspection.

50. MEASUREMENTS.




M2 for 50um openning
M2 for 70um openning
M2 extra
CNT_50um openning
CNT_70um openning
M2 for 30um openning
M1A
M1B
CNT_30um openning

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