

On the Design of Unilateral Dual-Loop Feedback Low-Noise Amplifiers With Simultaneous Noise, Impedance, and IIP3 Match

Mark P. van der Heijden, *Student Member, IEEE*, Leo C. N. de Vreede, *Senior Member, IEEE*, and Joachim N. Burghartz, *Fellow, IEEE*

Abstract—This work describes the theory and design of a nonenergetic dual-loop feedback low-noise amplifier (LNA) that provides maximum unilateral gain and simultaneous noise and impedance matching conditions. The dual-loop feedback is implemented in the form of transformer current-feedback and inductive series feedback (emitter degeneration). The current-feedback transformer is also used to neutralize the base-collector capacitance (C_{bc}), by combining it with a properly dimensioned shunt admittance at the collector output. The result is a single-transistor unilateral-gain amplifier with high isolation and good stability, eliminating the need for a cascode stage and thus enabling the use of a lower dc-supply voltage. For the complete LNA, simple design equations are derived for the unilateralization, noise, and impedance matching requirements. Finally, second-harmonic tuning at the source improves the linearity without compromising the simultaneous noise and impedance match. To verify the presented theory, a 900-MHz hybrid Si BJT LNA has been implemented, which achieves 1.3-dB noise figure, 15-dB gain, -55 dB isolation, and $+10$ dBm IIP3 using a conventional double poly transistor, consuming $I_C = 2.5$ mA at $V_{CE} = 1.5$ V.

Index Terms—Linearity, low noise amplifier (LNA), negative feedback amplifier, noise matching, radio-frequency integrated circuit design, Si-SiGe analog circuit design, third-order distortion, third-order intermodulation distortion (IM3).

I. INTRODUCTION

THE MARKET for modern wireless communication systems, like UMTS and WLAN, demands linear low-noise amplifiers (LNAs) operating at low dc bias conditions. The use of low supply voltages (~ 1 V) becomes even more important when considering analog/RF and digital circuitry on the same die, from both cost and packaging considerations. In order to meet these requirements, various LNA implementations and topologies have been studied in the past [1]–[3]. From these results, nonenergetic feedback seems to be the best solution to arrive at the minimum noise figure (F_{\min}) of the active device under input impedance matched conditions. For this reason, the cascode LNA with inductive series feedback (ISF) in Fig. 1 is quite often favored due to its low noise, high linearity, and simplicity. A modification to this circuit by means of transformer

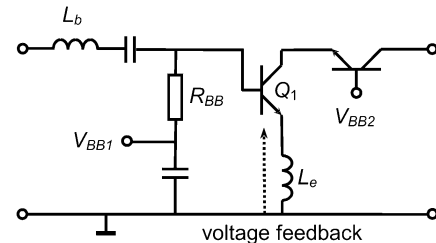


Fig. 1. Cascode LNA with inductive series feedback.

feedback [4], offers some advantages over ISF in terms of stability and gain at lower current levels. However, also for the configuration in [4], a tradeoff still exists between linearity, gain, and current level. To overcome these limitations, recently new circuit techniques were introduced to improve the linearity of bipolar transistors at low current levels by proper even harmonic control through the use of out-of-band terminations [5], [6]. These latter techniques, based on the controlled cancellation of third-order intermodulation (IM3) products, offer more circuit design freedom to avoid tradeoffs in bias and linearity.

The aim of this work is to provide an LNA design solution, which combines unilateral gain, simultaneous noise, impedance, and input third-order intercept-point (IIP3) matching, while operating the transistor at a low current and dc-supply voltage. Note that by fulfilling these goals, maximum performance is obtained for a given device for all specifications without any compromise.

First, Section II discusses the design aspects of a unilateralized dual-loop feedback (DLF) LNA, which provides an exact simultaneous noise and impedance match. The feedback topology combines nonenergetic transformer current feedback (TCF) [7] and classical ISF. In addition, the current-feedback transformer can be used to neutralize the undesired negative feedback through the collector-base capacitance (C_{bc}), resulting in a unilateral single-transistor amplifier with excellent output-to-input isolation [8], [9]. Note, that such an amplifier can provide unconditional stability and maximum unilateral power gain ($G_{TU,\max}$) [10], which is beneficial to meet the gain requirements at low dc-currents. Section III illustrates how the proper out-of-band terminations are chosen for optimum linearity. Finally, Section IV gives an experimental verification of the presented theory using a 900-MHz LNA design with a discrete Philips BFG425W Si BJT. In conclusion, the measured results are ranked with other published data.

Manuscript received December 16, 2003; revised May 14, 2004. This work was supported by Philips Semiconductors, Nijmegen, The Netherlands.

The authors are with the Laboratory of High-Frequency Technology and Components, Delft University of Technology, 2600 GB Delft, The Netherlands (e-mail: m.p.vanderheijden@ewi.tudelft.nl).

Digital Object Identifier 10.1109/JSSC.2004.833759

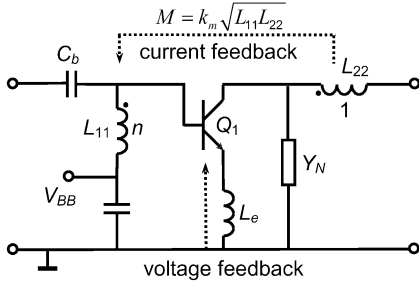


Fig. 2. Dual-loop feedback LNA with unilateralization.

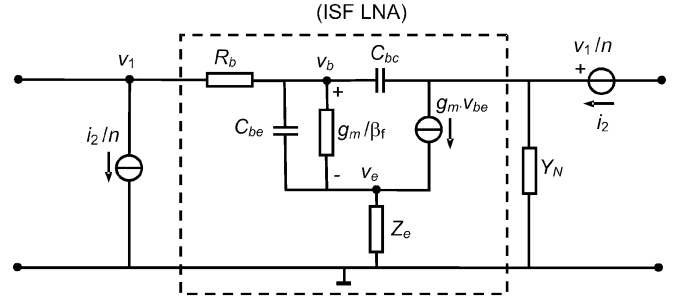
II. UNILATERAL DUAL-LOOP FEEDBACK LNA

Fig. 2 shows the proposed LNA, which consists of two negative-feedback paths around a common-emitter (CE) stage. Current-feedback is applied via a transformer, consisting of two weakly magnetically coupled inductors L_{11} and L_{22} , having a magnetic coupling coefficient k_m . The secondary inductance L_{22} senses the current in the collector branch and feeds back a smaller current to the base node via the primary inductor L_{11} . Series feedback is applied through inductor L_e , which senses the emitter current and induces a voltage in series with the base-emitter voltage. Since both voltage and current at the input are now defined as a result of the feedback action, the input impedance can be controlled by properly dimensioning the transformer turn ratio n and L_e . Knowing n , the condition for unilateralization can be satisfied by using a properly dimensioned neutralizing admittance Y_N . The previous conditions allow us to obtain an exact simultaneous noise and impedance match for our unilateral amplifier. Section II-A defines the condition for unilateralization and associated $G_{TU, \max}$ of the DLF LNA. Section II-B analyzes the noise behavior of the neutralized LNA, and defines the required conditions for simultaneous noise and impedance matching.

A. Condition for Unilateralization

Unilateralization is defined as any method that nullifies the reverse transfer parameter of a general two-port network [8]. Fig. 2 shows how we implement in our design the unilateralization, by combining a feedback transformer with an ISF LNA and a neutralization admittance Y_N (to be defined later). When the transformer ratio n and Y_N are properly dimensioned; the reverse feedback through C_{bc} is neutralized. We can obtain this condition by using the k -parameter representation (see the Appendix) for the calculation of the overall network. Note that this matrix representation is particularly useful here, since the transformer is shunt-connected to the input and series-connected with the output of the ISF LNA. The transformer k -parameters, including the approximations for an ideal transformer ($L_{11} \rightarrow \infty$ and $k_m = 1$), are

$$\begin{aligned} k_{11} &= \frac{1}{sL_{11}} \approx 0 & k_{12} &= \frac{1}{n} \\ k_{21} &= \frac{-1}{n} & k_{22} &= s(1 - k_m^2)L_{22} \approx 0 \end{aligned} \quad (1)$$

Fig. 3. Small-signal equivalent circuit of the dual-loop feedback LNA with neutralization admittance Y_N .

where k_m is the magnetic coupling factor, and the effective transformer turn ratio is given by

$$n = \frac{1}{k_m} \sqrt{\frac{L_{11}}{L_{22}}} \quad (2)$$

Fig. 3 shows the ac equivalent circuit of the DLF LNA with the circuit elements of an ideal transformer.

By summing the k -matrix of the transformer with the k -matrix of the ISF LNA, we can write down the general condition for unilateralization [8] in terms of the y -parameters of the ISF LNA and the transformer turn ratio n :

$$k_{12(L)} = \frac{y_{12(L)}}{y_{22(L)}} = -k_{12(TF)} = -\frac{1}{n} \quad (3)$$

in which subscript (L) denotes the ISF LNA core and (TF) the transformer. The admittance parameters $y_{12(L)}$ and $y_{22(L)}$ are calculated in the Appendix and are given by

$$\begin{aligned} y_{12(L)} &= \frac{-sC_{bc}}{1 + R_b(Y_i + sC_{bc})} \\ y_{22(L)} &= \frac{sC_{bc}(1 + R_b(Y_m + Y_i))}{1 + R_b(Y_i + sC_{bc})} \end{aligned} \quad (4)$$

If we neglect R_b in (4) and omit Y_N for now, we obtain $y_{22(L)} \approx -y_{12(L)}$, yielding a turn ratio $n \approx 1$ in order to satisfy the condition for unilateralization in (3). However, for gain, noise, and impedance matching, it is desirable to maintain freedom in the choice of n . We obtain this freedom by adding a neutralizing admittance Y_N to $y_{22(L)}$, which makes n an independent variable. We now solve for Y_N by replacing $y_{12(L)}$ in (3) with $y_{12(L)} + Y_N$, yielding

$$Y_N = \frac{sC_{bc}(n - 1 - R_b(Y_i + Y_m))}{1 + R_b(Y_i + sC_{bc})} \approx sC_{bc}(n - 1). \quad (5)$$

Condition (5) can be satisfied by connecting a shunt capacitance at the output of the transistor, yielding a very broadband unilateral gain stage with comparable isolation and gain properties as found for the traditional ISF cascode LNA. For this reason, the input impedance Z_{IN} of the unilateralized LNA no longer depends on the loading conditions at the output, since no undesired feedback occurs through C_{bc} . As a result, this significantly simplifies the simultaneous noise and impedance match requirements, which are examined in Section II-B.

Since our LNA is now neutralized, we can use the expressions for unilateral power gain as a figure of merit for the maximum

achievable power gain [9]. Normally, $G_{TU,\max}$ is expressed in terms of s -parameters [10], however, for this work it is more convenient to express it in terms of the y -parameters of the neutralized LNA [see (27) in the Appendix]:

$$G_{TU,\max} = \frac{|y_{21(U)}|^2}{4 \cdot \text{Re}(y_{11(U)}) \cdot \text{Re}(y_{22(U)})}. \quad (6)$$

Note that this gain definition is only valid for an unconditionally stable amplifier. Therefore, the stability criteria for unilateral gain should be satisfied:

$$\text{Re}\{y_{11(U)}\} > 0 \text{ and } \text{Re}\{y_{22(U)}\} > 0. \quad (7)$$

These criteria are in general satisfied for the unilateral LNA, as can be observed from (27). Equation (6) can be used in the design procedure to find the optimum combination of L_e and n to achieve maximum gain at the design frequency for a given dc power supply.

B. Noise Analysis

The noise parameters of the DLF LNA can be calculated with the noise correlation computation method [11]. The Appendix describes the required steps and the subsequent simplifications needed to arrive at the expressions presented in this section. Doing so, we can write the equivalent noise conductance G_n , the optimum noise impedance Z_{OPT} , and the minimum noise figure F_{\min} from (37)–(40) as follows:

$$G_n = \frac{g_m}{2} \left(\frac{1}{\beta_f} + \frac{\omega^2}{\omega_T^2} \right) \quad (8)$$

$$Z_{\text{OPT}} = \frac{1}{G} \sqrt{\frac{1}{\beta_f} + 2RG \left(1 + \frac{1}{2}RG \right)} + j \left(\frac{\omega}{G\omega_T} - \omega L_e \right) \quad (9)$$

$$F_{\min} = 1 + \frac{1}{\beta_f} + G(R + R_{\text{OPT}}) \quad (10)$$

$$\text{where } R = R_b + R_e \text{ and } G = g_m \left(\frac{1}{\beta_f} + \frac{\omega^2}{\omega_T^2} \right) \quad (11)$$

$$\text{and } \omega_T = \frac{g_m}{(A_e(C_{Te} + C_{Tc}) + \tau_f g_m)} \quad (12)$$

in which the transconductance $g_m = A_e J_C / V_T$ depends on the current density J_C , the emitter area A_e , and the thermal voltage V_T . C_{Te} and C_{Tc} are the base-emitter and collector-base depletion capacitances per unit area, and τ_f is the forward transit time. Note that the transformer turn ratio does not appear in (8)–(10). As a result, these equations are also valid for the traditional ISF cascode LNA. When considering F_{\min} , we observe from (10) that it does not depend on A_e , but only on J_C , the technology parameters and ω , since G is proportional and R is inversely proportional to A_e . However, when we consider F_{\min} at higher frequencies as function of J_C , a shallow minimum appears in relation with ω_T of the device. Consequently, the optimum current density ($J_{C,\text{opt}}$) related to this minimum in F_{\min} , can be

found by solving the derivative of $\partial F_{\min} / \partial J_C = 0$, yielding [12]

$$J_{C,\text{opt}} = \frac{\omega(C_{Te} + C_{Tc})V_T}{\sqrt{\frac{1}{\beta_f} + (\omega\tau_f)^2}}. \quad (13)$$

The current density optimum for F_{\min} is normally used as a starting point in the design of LNAs. However, its shallow nature allows some deviation without too much penalty on the minimum noise figure [12]. Consequently, our first design step is to determine $J_{C,\text{opt}}$. By fixing this current density, we can control the collector current by increasing A_e . Doing so, we can set the real part of the optimum noise impedance ($\text{Re}\{Z_{\text{OPT}}\} = R_{\text{OPT}}$) to an appropriate value (e.g., 50 Ω). The next step is to arrive at a simultaneous noise and impedance match. For the cascode with ISF we can match the real part of the input match ($\text{Re}\{Z_{\text{IN}}\} = R_{\text{OPT}}$, by making $L_e \cong R_{\text{OPT}}/\omega_T$ [2]. Through this selection of L_e , we almost automatically obtain for the ISF cascode a close approximation of $\text{Im}(Z_{\text{IN}}) = -\text{Im}(Z_{\text{OPT}})$, which represents the remaining requirement for the imaginary part of the simultaneous noise and impedance match. Finally, we cancel out the reactance of the input capacitance by using an inductor L_b in the base (see Fig. 1). From the above it is clear that the selection of L_e plays a dominant role in satisfying the matching conditions; however, the choice of L_e also influences the gain of the ISF LNA. Consequently, too high values of L_e must be avoided in order to obtain sufficient gain for the LNA stage. From this discussion, it is clear that more freedom in fulfilling the matching and gain requirements is highly desirable in the optimization of the overall performance of the LNA. Therefore, we will now consider the dual-loop feedback LNA.

Earlier, we found that the noise parameters of the DLF LNA are identical to that of the ISF cascode LNA. For this reason, we only have to consider the input impedance matching condition, which is given by

$$Z_{\text{IN}} = \frac{1}{y_{11(U)}} \cong \frac{n^2}{n^2 + \frac{\omega_T^2}{\omega^2}} \left\{ r_e \frac{\omega_T^2}{n\omega^2} + L_e \omega_T + R + j \left[\omega L_e \left(1 + \frac{\omega_T^2}{n\omega^2} \right) - \frac{1}{\omega(C_{be} + C_{bc})} \right] \right\}. \quad (14)$$

Note that Z_{IN} now depends both on the transformer turn ratio n and the emitter inductance L_e . We can solve for $Z_s = Z_{\text{in}}^* = Z_{\text{OPT}}$ in order to obtain an exact simultaneous noise and impedance match. From (14) we observe, that we can reduce L_e by selecting a lower value of n (more current feedback), illustrating the higher design freedom, while the gain can still be improved by applying unilateralization. Setting n to infinite yields again the original input impedance of a conventional ISF LNA (no current feedback) [2].

C. Comparison Cascode and Dual-Loop Feedback LNA

To illustrate the benefits of the proposed DLF LNA, we compare the traditional ISF cascode LNA and the neutralized DLF

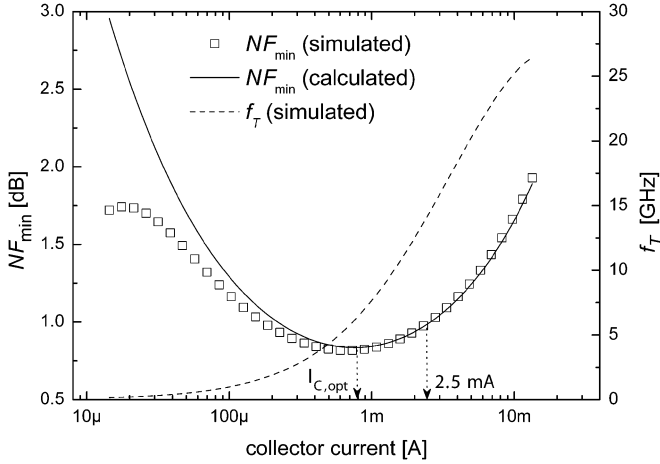


Fig. 4. Minimum noise figure (NF_{\min}) and cut-off frequency (f_T) as function of collector current I_C for the unscaled BFG425W biased at $V_{CE} = 1$ V.

LNA using the device model of the Philips BFG425W double-poly transistor without the package and bondpad parasitics [13]. The cascode LNA is biased from a 2-V supply voltage and the DLF LNA from a 1-V supply voltage, which is still sufficient to prevent any saturation of the transistors. Fig. 4 shows the simulated F_{\min} at 900 MHz and f_T as function of I_C of the nonscaled transistor together with the calculated F_{\min} from (10). The optimum J_C is indicated in the plot, but can also directly be calculated from (13). To provide a good comparison, we scaled up the device 3.8 times in order to set $R_{OPT} = 50 \Omega$ at $I_C = 4$ mA. For these bias conditions, the cascode LNA requires an emitter inductance $L_e = 1.1$ nH and a base inductor $L_b = 8$ nH to satisfy $Z_S = Z_{in}^* \approx Z_{OPT}$. Note, that a collector shunt resistor of 2 k Ω is needed in order to stabilize the cascode LNA. On the other hand, to satisfy $Z_{in}^* \approx Z_{OPT}$; the DLF LNA requires $L_e = 0.55$ nH with a transformer turn ratio $n = 13$. Then the primary inductor $L_{11} = 12$ nH is used together with $C_b = 8$ pF to match the LNA to 50Ω (see Fig. 2). Knowing L_{11} and n , the transformer can be optimized with (2). A high turn ratio can be achieved by making the magnetic coupling factor k_m small (e.g., 0.3), yielding for the secondary inductor $L_{22} = 0.25$ nH. Finally, we calculate with (5) the neutralization capacitance: $C_N = 3.8$ pF, which is connected between collector and ground.

Fig. 5 shows the maximum available power gain (MAG) and reverse transmission parameter s_{12} in decibels as a function of frequency for both LNAs, which are unconditionally stable over the whole band. In terms of gain and isolation, the performance is comparable, since both designs behave unilaterally (eliminating the Miller effect). However, the MAG of the DLF LNA will be somewhat lower due to the slightly lower current-gain of the stage, given by

$$\alpha_{DLF} = \frac{-i_2}{i_i} = \frac{-y_{21}(U)}{y_{11}(U)} \cong \frac{-n}{1 + j\frac{\omega}{\omega_T}n} \quad (15)$$

compared to the cascode LNA with a current gain of $\alpha_{ISF} \cong j\omega_T/\omega$. Fig. 6 shows the noise figure and input return loss as function of frequency for both LNAs.

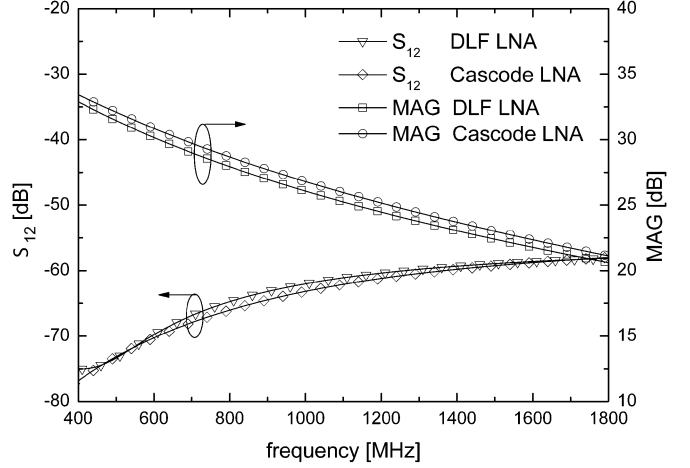


Fig. 5. Reverse transmission (s_{12}) and maximum available power gain (MAG) as function of frequency for the inductive series-feedback cascode LNA and the DLF LNA.

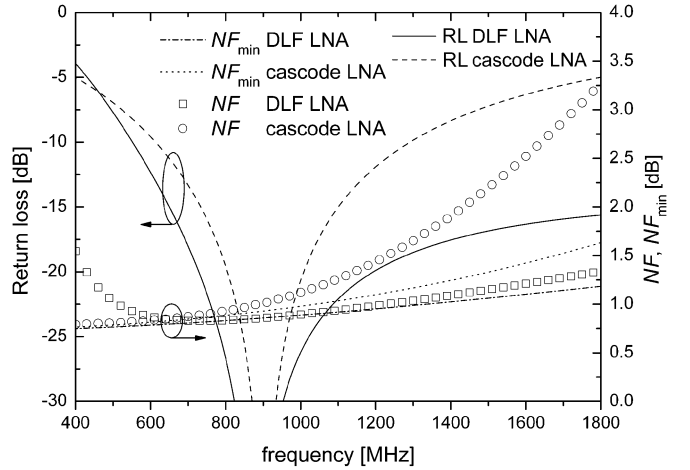


Fig. 6. Return loss, noise figure (NF), and minimum noise figure (NF_{\min}) as function of frequency for the inductive series-feedback cascode LNA and the DLF LNA.

Both topologies have their minimum around 900 MHz; however, the DLF amplifier outperforms the cascode LNA in terms of bandwidth of the simultaneous noise and impedance match, making it an interesting candidate for multiband or ultra-wide-band applications. This wide-band behavior can be explained by the fact that the input impedance is controlled by two feedback paths, yielding a more broadband impedance response, well known from negative-feedback amplifier design theory [7].

III. LINEARITY OPTIMIZATION

Recently, new design techniques were introduced for the linearization of bipolar transistor stages, which are based on the use of proper even harmonic terminations [5], [6]. The following nonlinear analysis shows how we obtain the required optimum out-of-band terminations for IM3 cancellation. The technique is based on the fact that the distortion at lower current levels of bipolar transistors is purely dominated by the nonlinear collector current, which depends exponentially on the base-emitter voltage.

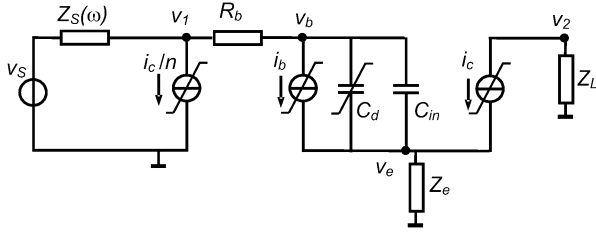


Fig. 7. Simplified large-signal model of the DLF LNA.

A. Nonlinear Analysis

Fig. 7 shows the equivalent circuit diagram for the nonlinear analysis. Our analysis includes the Taylor series expansion of the collector current i_c up to the third order.

The nonlinear base current i_b and the base-emitter diffusion capacitance C_d depend linearly on i_c via the dc-current gain β_F and the forward transit time τ_F , respectively. In addition, as a result of the current feedback; a current source (i_c/n) appears at the input, which also tracks linearly with i_c . The total source impedance connected to the external base node (v_1) is defined as $Z_s(\omega)$. The load impedance Z_L is not taken into account in the analysis, which is a fair assumption since the LNA stage is unilateral. To calculate the optimum out-of-band source terminations of this network, we use the expressions for IM3 as defined in [5], which state that the magnitude of IM3 is proportional to a factor $|\varepsilon(\Delta\omega, 2\omega)|$, given by

$$\varepsilon(\Delta\omega, 2\omega) = g_{m3} - \frac{2g_{m2}^2}{3} \left[\frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)} \right] \quad (16)$$

where $\Delta\omega = \pm(\omega_1 - \omega_2)$ and $\omega \approx \omega_1 \approx \omega_2$, which is valid for small $\Delta\omega$. The Taylor coefficients of the nonlinear collector current up to the third-order are defined as

$$g_m = \frac{I_C}{V_T} \quad g_{m2} = \frac{g_m}{2V_T} \quad g_{m3} = \frac{g_m}{6V_T^2}. \quad (17)$$

The first term in $\varepsilon(\Delta\omega, 2\omega)$ is responsible for the direct third-order nonlinearity and the second term describes how the second-order nonlinearity mixes with the fundamental signal again, producing an indirect third-order nonlinearity. The parameter $g(\omega)$ depends on the circuit model of the LNA (Fig. 7), which can be calculated using Volterra series analysis, yielding

$$g(\omega) = \frac{1 + j\omega[Z_s(\omega) + R_b + Z_e(\omega)]C_{in}}{Z_s(\omega)/n + \left(\frac{1}{\beta_F} + j\omega\tau_F\right)[Z_s(\omega) + R_b + Z_e(\omega)] + Z_e(\omega)} \quad (18)$$

in which C_{in} is the combined depletion capacitance of the base-emitter and base-collector junctions. We can achieve cancellation of the direct and indirect third-order nonlinearity by finding the proper baseband and second-harmonic source impedances $Z_S(\Delta\omega)$ and $Z_S(2\omega)$, which make $\varepsilon(\Delta\omega, 2\omega) = 0$. Note that in this analysis $Z_S(\Delta\omega) \approx 0$, since the impedance of L_{11} is negligible for small $\Delta\omega$, and therefore, $g(\Delta\omega)$ can be approximated by

$$g(\Delta\omega) = \frac{1}{r} \approx \frac{1}{R_e + R_b/\beta_F}. \quad (19)$$

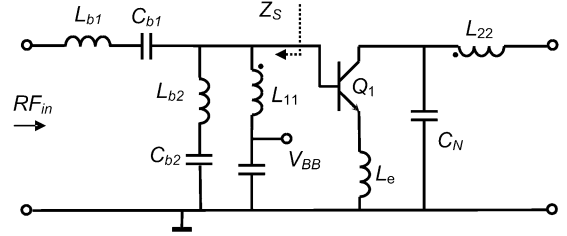


Fig. 8. Proposed circuit implementation of the unilateralized DLF LNA with a dedicated source network for simultaneous noise, impedance, and IIP3 matching conditions.

In this way, $g(2\omega)$ can be solved by setting $\varepsilon(\Delta\omega, 2\omega) = 0$ in (16) and by substituting the Taylor coefficients and $g(\Delta\omega) = 1/r$ given in (17) and (19), respectively:

$$g(2\omega) = \frac{2g_m^2 r}{1 - g_m r}. \quad (20)$$

We can now calculate the second-harmonic source impedance $Z_S(2\omega)$ by equating (20) and (18), yielding

$$Z_S(2\omega) = \frac{1 + (R_b + Z_e(2\omega))[j\omega - g(2\omega)(1/\beta_F + j\omega\tau_F)] - g(2\omega)Z_e(2\omega)}{g(2\omega) \left(\frac{1}{n} + \frac{1}{\beta_F} + j\omega\tau_F \right) - j\omega C_{in}}. \quad (21)$$

As a consequence of ($Z_S(\Delta\omega) \approx 0$), the required impedance at the double frequency for IM3 cancellation is inductive with a small real part, which has to be provided by the input matching network of our LNA.

B. Design of the Complete Matching Network

Fig. 8 shows the implementation of the complete unilateralized DLF LNA as discussed in Section II-C.

The input-matching network has been adapted to combine the second-harmonic termination with the fundamental noise and impedance match at the fundamental. The series resonator consisting of C_{b1} and L_{b1} presents the correct reactance to compensate for the imaginary part of the noise and impedance match and presents high impedance at the second harmonic. The shunt resonator, consisting of C_{b2} and $L_{b1} + L_{11}$, presents an open at the fundamental and by adjusting L_{b1} and L_{11} we can tune the second-harmonic termination for IIP3. Fig. 9 shows a Smith chart with lines of constant IIP3, combined with the trajectory of the source impedance, swept from the fundamental up to the second harmonic frequency.

The IIP3 for a distribution of 20% in n and 10% in I_C is shown in Fig. 10(a) and proves to be rather insensitive for the turn ratio n . Fig. 10(b) shows the IIP3 as function of frequency for two different Q values of the second-harmonic input-matching network. Note that also for more moderate Q values, the linearity improvement is still significant.

Although in this DLF LNA, the proposed design method for IM3 cancellation proves to be rather robust, IM3 cancellation techniques, in general, require a constant transconductance (g_m) of the active device. For this reason, PTAT biasing of the LNA core must be considered. Finally, it is obvious that if one aims for perfect cancellation, an accurate circuit implementation is required.

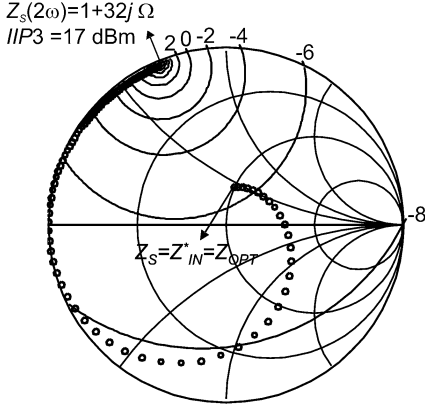


Fig. 9. Simulated constant IIP3 contours as function of second-harmonic source impedance $Z_s(2\omega)$ at 1.8 GHz together with the source impedance, swept from 900 MHz to 1.8 GHz for the LNA of Fig. 8 biased at $V_{CE} = 1$ V and $I_C = 4$ mA.

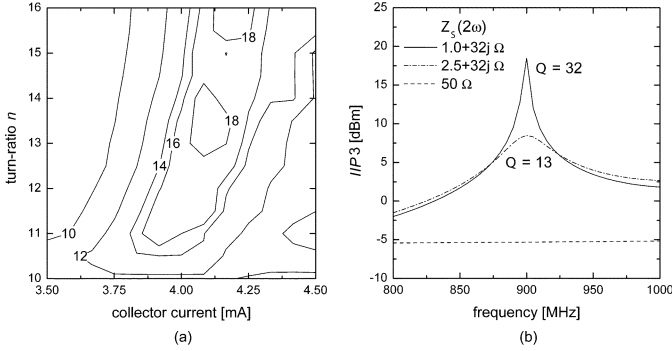


Fig. 10. (a) Constant IIP3 contours in dBm as function of n and I_C at 900 MHz. (b) The IIP3 as function of frequency for two different Q -factors of the second-harmonic source termination, biased at $I_C = 4$ mA with $n = 13$.

IV. EXPERIMENTAL RESULTS

In support of the previously introduced theory, here we describe the design and implementation of a 900-MHz hybrid DLF LNA based on a discrete Philips BFG425W transistor as shown in Fig. 11. The circuit was implemented using Rogers 4003 with a substrate height of $h = 813 \mu\text{m}$ and a relative dielectric constant $\epsilon_r = 3.38$. The LNA was intended to demonstrate the use of shunt feedback in conjunction with unilateralization and out-of-band terminations for IM3 cancellation. The inductive emitter degeneration was considered to be fixed by the transistor package and PCB board, and therefore, not fully optimized.

A. Design of the LNA

Since we did not have the freedom to scale up the device, I_C was set to 2.5 mA, which is slightly higher than the optimum current density for F_{\min} . This value was chosen in order to improve on the gain and matching conditions without too much penalty on the noise performance (see Fig. 4). To indicate the optimum circuit solutions for this transistor under these bias conditions, we can plot contours of constant $G_{TU,\max}$ and F as function of n and L_e , as shown in Fig. 12(a) and (b). We also indicated the forbidden areas in the plots, since certain combinations of n and L_e require the real part of the neutralizing admittance Y_N to be negative. This requirement, of course, cannot be fulfilled with passive components, and is therefore considered as an invalid circuit solution.

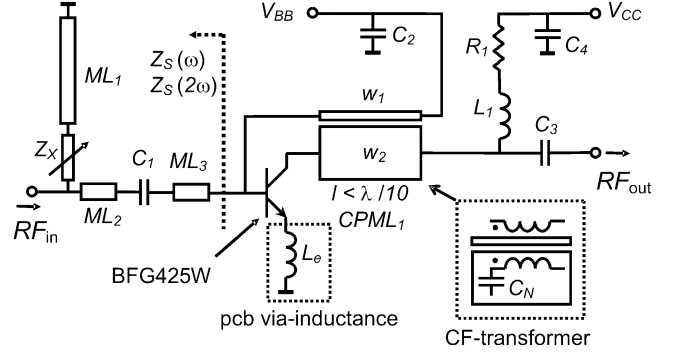


Fig. 11. Hybrid circuit design of the 900-MHz unilateral transformer DLF LNA.

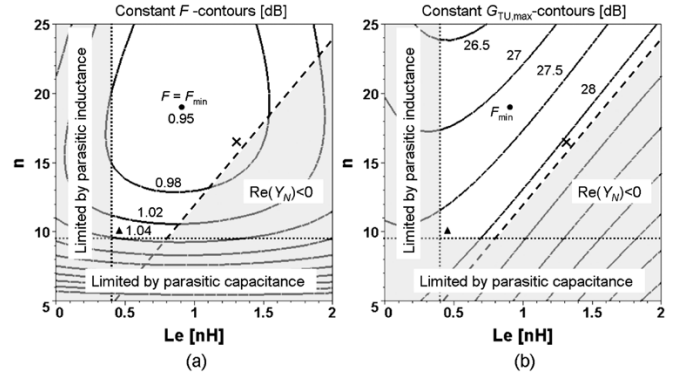


Fig. 12. (a) Calculated constant noise figure contours and (b) constant unilateral power gain ($G_{TU,\max}$) contours of the BFG425W at 900 MHz as function of emitter inductance (L_e) and transformer turn ratio (n), biased at $V_{CE} = 1.5$ V, and $I_C = 2.5$ mA.

The points for optimum noise figure (dot) and highest unilateral gain with good noise figure (cross) are both indicated in Fig. 12(a) and (b). Furthermore, the minimum L_e is 0.4 nH, due to the inductance of the transistor's package and the ground via of the printed circuit board. The minimum n is bounded by the transistor's parasitic collector substrate capacitance, bondpad capacitance, and package capacitance.

Based on practical implementation considerations we have selected in this design $n = 10$ and $L_e = 0.4$ nH [indicated by the triangle in Fig. 12(a) and (b)]. This is a small deviation of the absolute optimum, but still provides a very good noise and gain performance. Since n and L_e are now fixed, Y_N can be calculated and was found to be $Y_N = 100 \mu + j1.84$ S, which can be approximated by a neutralizing capacitance $C_N = 325$ fF. Now, instead of using a discrete transformer, which behaves rather nonideal at these frequencies, the CF transformer is implemented by a coupled line segment ($CPML_1$), which is more accurate in its implementation (Fig. 11). The length l of the $CPML_1$ is shorter than $\lambda/10$, in order to approximate a lumped-element transformer over all the frequencies of interest. Since we require a high turn ratio, the secondary winding of the transformer must have a relatively low inductance and the lines should be weakly coupled. This is accomplished by making the width w_2 of $CPML_1$ large and using a relatively large spacing between the lines. Doing so, we found that in this way there is no need for a discrete capacitor C_N , since the width of the line provides the required shunt capacitance by itself. The $CPML_1$ section is optimized using the Momentum simulator

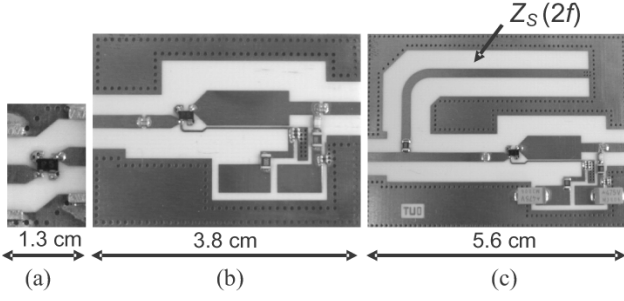


Fig. 13. (a) A discrete BFG425W. (b) The unilateral DLF LNA without out-of-band terminations and (c) with second-harmonic source termination $Z_S(2f)$.

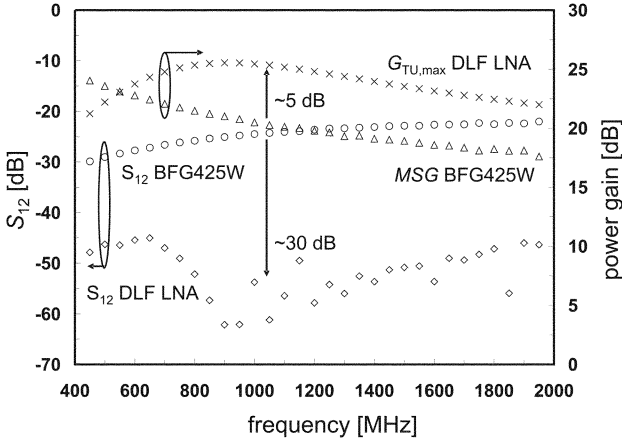


Fig. 14. Measured power gain and isolation as function of frequency of the transformer DLF LNA and BFG425W transistor, biased at $V_{CE} = 1.5$ V, and $I_C = 2.5$ mA.

in ADS in order to obtain the best noise and impedance match at 900 MHz and unilateralization up to 2 GHz., which also includes the second harmonic frequency.

The next step is the design of the input and output matching networks. The LNA input has been matched to $50\ \Omega$ at the fundamental frequency, by the combination of C_1 , the $50\text{-}\Omega$ μ strip line ML_3 , and the inductance of the primary winding of the CF transformer (w_1 of $CPML_1$). The output matching consists of L_1 and R_1 , which are intended for gain control and does not necessarily provide a match to $50\ \Omega$. The capacitor C_4 acts like an RF short up to 2 GHz to bypass the biasing circuitry.

The last step is the implementation of the second-harmonic source impedance $Z_S(2\omega)$, which was calculated using (21) and here is determined by $50\text{-}\Omega$ μ strip lines ML_1 – ML_3 , a small tuning impedance Z_X , and C_1 (see Fig. 11). The microstrip line ML_1 is a short-circuited $\lambda/4$ stub at 900 MHz in order to isolate this line from the fundamental input match. At 2ω , Z_X is effectively shorted to ground and is used in combination with ML_2 , ML_3 , and C_1 to provide the correct magnitude and phase of $Z_S(2\omega)$ for optimum IIP3. The phase of $Z_S(2\omega)$ can be adjusted by the choice of Z_X .

B. Measured Results

Three circuits have been implemented and evaluated in terms of their small-signal S -parameters, noise, and linearity. Fig. 13(a) shows the bare discrete BFG425W, which is used as a reference for the isolation data. Fig. 13(b) and (c) shows the

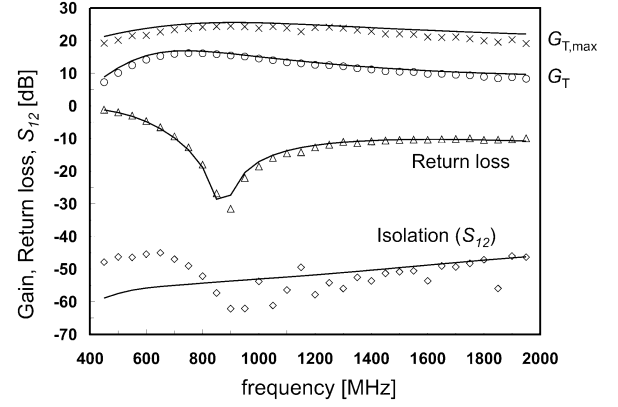


Fig. 15. Measured (symbols) and simulated (solid lines) power gain, input return loss and isolation versus frequency of the DLF LNA, biased $V_{CE} = 1.5$ V, and $I_C = 2.5$ mA.

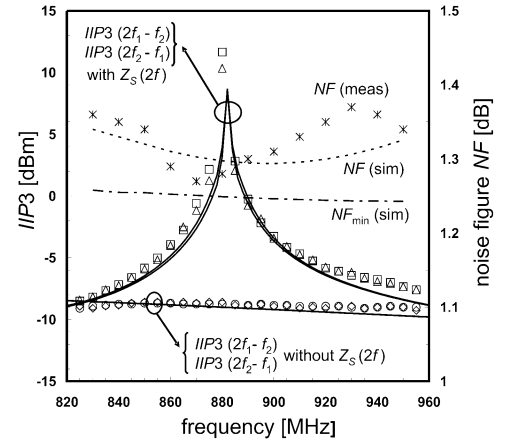


Fig. 16. Measured (symbols) and simulated (solid lines) IIP3 and noise figure (NF) versus frequency of the transformer DLF LNA biased at $V_{CE} = 1.5$ V and $I_C = 2.5$ mA with and without second-harmonic source termination.

DLF LNA without and with second-harmonic source tuning, respectively.

Fig. 14 shows the maximum transducer power gain $G_{T,max}$ and isolation versus frequency for the DLF LNA [Fig. 13(b)], compared to the maximum stable gain (MSG) and isolation of the reference device when biased at 2.5 mA at 1.5 V. Note the remarkable improvement of 30 dB for the isolation and 5 dB for the gain at the design frequency, demonstrating the benefits of unilateralization. Fig. 15 shows the measured (symbols) and simulated (solid lines) transducer gain G_T , $G_{T,max}$, isolation, and input return loss versus frequency of the DLF LNA when biased at 2.5 mA at 1.5 V. Note that unilateralization is based on cancellation of undesired feedback, therefore, the presence of even the smallest parasitic will already cause deviation from the simulated S_{12} . However, careful design yielded an isolation of more than 55 dB at 900 MHz, while an improvement of +25 dB is guaranteed from 800 to 2000 MHz. This means that the amplifier stage behaves close to unilateral for the fundamental up to the second-harmonic frequencies. The maximum transducer power gain under perfect output match conditions is found to be $G_{T,max} = 25$ dB. However, in our experiment, the gain was set to 15 dB at 900 MHz by tuning L_1 and R_1 , since the IIP3 outside the frequency point of cancellation mainly depends on gain of the LNA via the relation $IIP3 = OIP3 - G_T$ (in decibels).

TABLE I
COMPARISON OF STATE-OF-THE-ART LNAs

WORK	TECHNOLOGY	FREQ [GHz]	GAIN [dB]	NF [dB]	IIP3 [dBm]	P _{IDB,IN} [dBm]	I _{DC} [mA@V]	DRM	LFM
This work	Si BJT	0.88	15.8	1.3	+10	-9	2.5 @1.5	290	2.7
[5]	Si BJT	2	16	1.7	+16	**	5 @2.7	245	2.9
[16]	0.5um SiGe BiCMOS	0.88	15.7	1.4	+10.3	**	3.9 @3.0	89.5	0.9
[16]	0.5um SiGe BiCMOS	0.88	16.3	1.5	+12.2	-10	7.7 @3.0	74.3	0.7
[17]	SiGe HBT	2.14	16	1.2	+8.4	-10	8@3.0	36	0.3

(**not specified)

The NF has a minimum of 1.28 dB at 870 MHz and is 1.3 dB at 900 MHz. The NF of the reference device (which is not noise matched) at 870 MHz is 1.5 dB for the same bias conditions.

Fig. 16 shows the measured (symbols) and simulated (solid lines) IIP3 as function of the center frequency with $\Delta f = 1$ MHz. $Z_S(2\omega)$ was tuned by Z_X yielding an optimum IIP3 of 10 dBm at 880 MHz for, e.g., a CDMA receiver application. The other curve shows the IIP3 level without ML_1 and Z_X , for which $Z_S(2\omega)$ is only determined by C_1 and ML_3 . In that case, $Z_S(2\omega)$ is close to 50 Ω . It demonstrates that the IIP3 can be optimized quite accurately for a specific frequency using this method. However, a more frequency independent IM3 cancellation is possible, but requires a more sophisticated integrated implementation of the out-of-band terminations. Table I summarizes the performance of various state-of-the-art LNAs, where DRM is a dynamic range merit [14] defined as $OIP3/[(NF - 1) \cdot P_{DC}]$ and LM is linearity figure of merit [15] defined as $IIP3/P_{DC}$.

V. CONCLUSION

A new design approach for LNAs is presented in order to meet the requirements for gain, linearity, and minimum noise figure at a minimum of dc power dissipation. Unilateralization and current feedback are combined in order to obtain simultaneous noise and impedance match at low current levels with unilateral gain. The high isolation ensures well-controlled optimum out-of-band termination for high linearity, which do not depend on the output termination of the LNA. A 900-MHz hybrid Si BJT LNA is constructed to verify the theory presented. The LNA achieves 1.3-dB NF, 15-dB gain, -55-dB isolation, and +10-dBm IIP3 (at 880 MHz) with 2.5 mA of current at 1.5-V collector voltage, which is state-of-the-art compared to other reported works.

APPENDIX

The k -parameter representation of a network relates the input voltage and output current to the input current and output voltage, given by

$$\begin{pmatrix} I_1 \\ V_2 \end{pmatrix} = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix}. \quad (22)$$

Fig. 17 shows the equivalent circuit of the inductively degenerated CE stage (ISF LNA) with transformer current feedback. The y -matrix of the ISF LNA is given by

$$[Y_{(L)}] = \begin{bmatrix} \frac{Y_i + sC_{bc}}{1 + R_b(Y_i + sC_{bc})} & \frac{-sC_{bc12}}{1 + R_b(Y_i + sC_{bc})} \\ \frac{Y_m - sC_{bc21}}{1 + R_b(Y_i + sC_{bc})} & \frac{R_b sC_{bc12}(Y_m - sC_{bc21})}{1 + R_b(Y_i + sC_{bc})} + sC_{bc} \end{bmatrix}. \quad (23)$$

The circuit representation in Fig. 17 and its y -parameters in (23) may look slightly different than one is used to, since we make a distinction between the collector-base transcapacitances $C_{bc12} = C_{bc21} = C_{bc}$, and the input and output capacitances $C_{bc11} = C_{bc22} = C_{bc}$, resulting in two voltage-dependent capacitive current sources at the input and the output of the intrinsic devices and two lumped capacitors. This is done to clarify the assumptions we make later in our noise analysis. In (23), R_b is the base resistance and Y_i and Y_m are the input-admittance and transadmittance of the intrinsic inductively degenerated CE stage, expressed as

$$Y_i = \frac{Y_{be}}{1 + Z_e(g_m + Y_{be})} \quad Y_m = \frac{g_m}{1 + Z_e(g_m + Y_{be})} \quad (24)$$

where g_m is the transconductance, and Y_{be} and Z_e are the input admittance and the emitter impedance of the CE stage, given by

$$Y_e = \frac{g_m}{\beta_f} + sC_{be} \quad Z_e = R_e + sL_e, \quad (25)$$

where β_f is the ac current gain, C_{be} is the base-emitter capacitance, and R_e is the emitter resistance of the CE stage. We can solve for Y_N by substituting the y -parameters of (23) in (3), yielding

$$Y_N = \frac{n \cdot sC_{bc12} - sC_{bc}[1 + R_b(Y_i + sC_{bc} + sC_{bc12}(Y_m - sC_{bc21}))]}{1 + R_b(Y_i + sC_{bc})}. \quad (26)$$

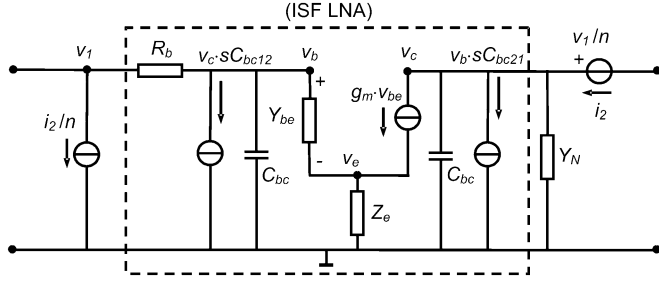


Fig. 17. Equivalent circuit of the DLF LNA with unilateralization admittance Y_n .

When condition (26) is satisfied, we can calculate the following y -matrix for the unilateral DLF LNA:

$$[Y(U)] = \begin{bmatrix} \frac{Y_i + sC_{bc} + (Y_m - sC_{bc21})/n}{1 + R_b(Y_i + sC_{bc})} & 0 \\ \frac{Y_m}{1 + R_b(Y_i + sC_{bc})} & \frac{n \cdot sC_{bc12}}{1 + R_b(Y_i + sC_{bc})} \end{bmatrix}. \quad (27)$$

Noise calculations of networks involving multiple feedback loops can be best calculated using the noise correlation matrix computation method in [11]. The full noise analysis of the DLF LNA was performed using Maple VIII. Although, in principle no neglect has to be made whatsoever, doing so would result in unworkable equations. For this reason, we have to make some minor simplifications, while maintaining good accuracy and insight in the noise behavior. Consequently, we neglect the influence of the transmission zero created by sC_{bc21}/Y_m in $y_{21}(L)$ and $y_{11}(U)$, since it only affects the noise behavior close to the cut-off frequency of the active device. Furthermore, we neglect the transcapacitance C_{bc12} , since its influence was neutralized and here only appears in the output admittance $y_{22}(U)$ of the unilateral LNA. These assumptions lead to the overall simplification that the transcapacitances are set to zero for the noise computation $C_{bc12} = C_{bc21} = 0$, while the shunt capacitances C_{bc} are taken into account. In fact, this can be considered as a Miller approximation for the noise calculation. Note that such assumption is common practice in the noise computation of cascode-based LNAs [2], [12], which also behave unilaterally. The simplifications above have almost no effect on the accuracy of our noise computations, as has been verified by very extensive simulations for the practical design case.

Fig. 18 shows the simplified equivalent circuit for the noise analysis. The four noise sources in Fig. 18 are given by

$$\begin{aligned} \overline{v_{nb}^2} &= 4kTR_b\Delta f & \overline{v_{ne}^2} &= 4kTR_e\Delta f \\ \overline{i_{nb}^2} &= 2qI_B\Delta f & \overline{i_{nc}^2} &= 2qI_C\Delta f \end{aligned} \quad (28)$$

where k is Boltzmann's constant, T is the absolute temperature, and q is the elementary charge. By applying the required noise correlation matrix transformations we arrive at the following

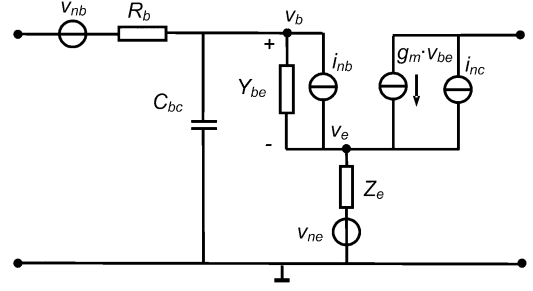


Fig. 18. Simplified equivalent circuit of the unilateral DLF LNA to be used in the noise analysis.

equivalent voltage and current noise sources at the input of the neutralized DLF LNA:

$$\begin{aligned} v_{n,eq} &= v_{nb} + v_{ne}(1 + sR_bC_{bc}) \\ &\quad + i_{nb}(R_b + Z_e(1 + sR_bC_{bc})) \\ &\quad + i_{nc} \left(\frac{1 + sR_b(C_{be} + C_{bc}) + sZ_eC_{be}(1 + sR_bC_{bc})}{g_m} \right) \end{aligned} \quad (29)$$

$$\begin{aligned} i_{n,eq} &= v_{ne}sC_{bc} + i_{nb}(1 + sZ_eC_{bc}) \\ &\quad + i_{nc} \left(\frac{sC_{be}(1 + sZ_eC_{bc}) + sC_{bc}}{g_m} \right). \end{aligned} \quad (30)$$

We observed that we can also neglect the terms $(1 + sR_bC_{bc})$ and $(1 + sZ_eC_{bc})$, which further reduces the complexity of the expressions and by setting $s = j\omega$, we obtain the following for $v_{n,eq}$ and $i_{n,eq}$:

$$\begin{aligned} v_{n,eq} &\approx v_{nb} + v_{ne} + i_{nb}(R_b + Z_e) \\ &\quad + i_{nc} \left(\frac{1}{g_m} + j\frac{\omega}{\omega_r}(R_b + Z_e) \right) \end{aligned} \quad (31)$$

$$i_{n,eq} \approx i_{nb} + i_{nc} \frac{j\omega}{\omega_T}. \quad (32)$$

From (31) and (32), we can calculate the noise correlation parameters [11], yielding

$$\begin{aligned} c_{uu^*} &= 2kT \left(2(R_b + R_e) + \frac{g_m}{\beta_f} |R_b + Z_e|^2 \right. \\ &\quad \left. + g_m \left| \frac{1}{g_m} + \frac{j\omega}{\omega_T}(R_b + Z_e) \right|^2 \right) \end{aligned} \quad (33)$$

$$\begin{aligned} c_{ui^*} &= 2kT \left(\frac{g_m}{\beta_f} (R_b + Z_e) \right. \\ &\quad \left. - g_m \frac{j\omega}{\omega_T} \left[\frac{1}{g_m} + \frac{j\omega}{\omega_T}(R_b + Z_e) \right] \right) \end{aligned} \quad (34)$$

$$\begin{aligned} c_{iu^*} &= 2kT \left(\frac{g_m}{\beta_f} (R_b + Z_e)^* \right. \\ &\quad \left. + g_m \frac{j\omega}{\omega_T} \left[\frac{1}{g_m} - \frac{j\omega}{\omega_T}(R_b + Z_e^*) \right] \right) \end{aligned} \quad (35)$$

$$c_{ii^*} = 2kT \left(\frac{g_m}{\beta_f} + g_m \frac{\omega^2}{\omega_T^2} \right). \quad (36)$$

Finally, we can calculate the noise parameters [11], given by

$$G_n = \frac{c_{ii}^*}{4kT} \quad (37)$$

$$Y_{OPT} = G_{OPT} + jB_{OPT} \\ = \sqrt{\frac{c_{ii}^*}{c_{uu}^*} - \left(\text{Im}\left(\frac{c_{ui}^*}{c_{uu}^*}\right)\right)^2} \\ + j\text{Im}\left(\frac{c_{ui}^*}{c_{uu}^*}\right) \quad (38)$$

$$Z_{OPT} = R_{OPT} + jX_{OPT} \\ = \frac{c_{uu}^*}{c_{ii}^*} (G_{OPT} - jB_{OPT}) \quad (39)$$

$$F_{min} = 1 + \frac{\text{Re}\{c_{ui}^*\}}{2kT} + 2G_n R_{OPT} \quad (40)$$

and calculate the noise figure F as

$$F = F_{min} + \frac{G_n}{R_S} |Z_{opt} - Z_S|^2. \quad (41)$$

ACKNOWLEDGMENT

The authors wish to acknowledge R. Jos and F. van Straten of Philips Semiconductors, Nijmegen, The Netherlands, and M. Spirito of TU Delft, The Netherlands, for their support and inspiration.

REFERENCES

- [1] F. Iturbide-Sánchez, H. Jardón-Aguilar, and J. A. Tirado-Méndez, "Comparison of different high-linear LNA structures for PCS applications using SiGe HBT and low bias voltage," *Electron. Lett.*, vol. 38, no. 12, pp. 536–538, June 2002.
- [2] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high-frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1430–1439, Sept. 1997.
- [3] Adiseno, M. Ismail, and H. Olsson, "A wideband active-feedback low-noise converter for multiband high-linearity low-IF wireless receivers," in *Proc. IEEE BCTM*, Sept. 2001, pp. 131–134.
- [4] J. R. Long and M. A. Copeland, "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communications systems," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1438–1448, Dec. 1995.
- [5] V. Aparin and C. Persico, "Effect of out-of-band terminations on intermodulation distortion in common-emitter circuits," in *IEEE MTT-S Dig.*, June 1999, pp. 977–980.
- [6] M. P. van der Heijden, H. C. de Graaff, and L. C. N. de Vreede, "A novel frequency-independent third-order intermodulation distortion cancellation technique for BJT amplifiers," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1176–1183, Sept. 2002.
- [7] E. H. Nordholt, *Design of High-Performance Negative-Feedback Amplifiers*. New York: Elsevier, 1983.
- [8] C. C. Cheng, "Neutralization and unilateralization," *IRE Trans. Circuit Theory*, vol. CT-2, pp. 138–145, June 1955.
- [9] S. J. Mason, "Power gain in feedback amplifier," *IRE Trans. Circuit Theory*, vol. CT-1, pp. 20–25, June 1954.
- [10] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*. Upper Saddle River, NJ: Prentice-Hall, 1984.
- [11] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990.
- [12] O. Shana's, I. Linscott, and L. Tyler, "Frequency-scalable SiGe bipolar RF front-end design," *IEEE J. Solid-State Circuits*, vol. 36, pp. 888–895, June 2001.
- [13] NPN 25 GHz Wideband Transistor, Product Information. Philips Semiconductors, Eindhoven, The Netherlands. [Online]. Available: <http://www.semiconductors.philips.com/pip/BFG425W>
- [14] N. King and A. Victor, "Enhanced wireless circuit performance with SiGe technology," *IBM MicroNews*, vol. 5, no. 1, 1999.
- [15] L. E. Larson, "Silicon bipolar transistor design and modeling for microwave integrated circuit applications," in *Proc. IEEE BCTM*, Sept. 1996, pp. 142–148.
- [16] V. Aparin, E. Zeisel, and P. Gazzero, "Highly linear SiGe BiCMOS LNA and mixer for cellular CDMA/AMPS applications," in *IEEE RFIC Conf. Tech. Dig.*, June 2002, pp. 129–132.
- [17] J. Lee *et al.*, "The design of SiGe HBT LNA for IMT-2000 mobile application," in *IEEE MTT-S Dig.*, vol. 2, June 2002, pp. 1261–1264.



Mark P. van der Heijden (S'00) was born in Ben-thuizen, The Netherlands, in 1976. He received the B.S. degree in electrical engineering from The Hague Polytechnic, The Hague, The Netherlands, in 1998, and the PD.Eng. degree in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2000. He is currently working toward the Ph.D. degree in electrical engineering.

He joined the Laboratory of Electronic Components, Technology and Materials, in the Department of Information Technology and Systems, Delft University of Technology, in 1998. From 1998 to 2000, he worked on isothermal characterization of MOST devices and power amplifier design for linearity. Currently, his research interests include the RF front-end design of linear and low-noise Si-(Ge) bipolar and BiCMOS circuits for wireless communication equipment.

Mr. Van der Heijden received an honorable mention in the student paper competition at the IEEE 2001 International Microwave Symposium for his work on LDMOS power amplifier linearization.



Leo C. N. de Vreede (M'00–SM'04) was born in Delft, The Netherlands in 1965. He received the B.S. degree in electrical engineering from the Hague Polytechnic in 1988. He received the Ph.D. degree from Delft University of Technology in 1996.

In 1988, he joined the Laboratory of Telecommunication and Remote Sensing Technology of the Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he was involved in the characterization and physical modeling of CMC capacitors. From 1990 to 1996, he worked on modeling and design aspects of HF silicon IC's for wide-band communication systems. In 1996, he was appointed as Assistant Professor at the Delft University of Technology working on the nonlinear distortion behavior of bipolar transistors at the device physics, compact model, as well as the circuit level, at Delft Institute of Microelectronics and Submicron Technology (DIMES). In the winter season of 1998–1999, he was a guest of the High-Speed Device group at the University of San Diego, La Jolla, CA. In 1999, he became an Associate Professor, responsible for the Microwave Components Group of the Delft University of Technology. His current interest is technology optimization and circuit design for improved RF performance and linearity.



Joachim N. Burghartz (M'90–SM'92–F'02) received the M.S. degree from the RWTH Aachen, Germany, in 1982 and the Ph.D. degree from the University of Stuttgart, Germany, in 1987.

In 1987, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY. He first worked there on selective epitaxial growth of silicon and related applications. From 1989 to 1992, he worked on high-speed Si and SiGe bipolar integration processes and was with the IBM team that pioneered IBM's SiGe technology. From 1992 to 1994, he was partly responsible for the development of a 0.15- μm CMOS technology at IBM's Advanced Silicon Technology Center, East Fishkill, NY. In 1994, he returned to Yorktown Heights and made original contribution to the integration of radio-frequency (RF) spiral inductors and other passive components on silicon substrates and also worked on RF circuit design. In 1998, he became a full Professor at TU Delft in the Netherlands, where he set up a research program in high-frequency silicon technology. Since 2001, he has been the Scientific Director of the research institute DIMES at TU Delft. He has published more than 200 papers in reviewed journals and technical conferences, and he holds 13 U.S. patents.

Dr. Burghartz is an IEEE Distinguished Lecturer. He served on several IEEE conference committees, including IEDM and BCTM, and of ESSDERC. Currently, he is an associate editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.