Controller-Hardware-in-the-Loop Validation of MPC for Radial-Mesh HVDC Systems

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Keywords: Controller hardware-in-the-loop (CHIL); Dispatch center; HVDC grids; Model predictive control (MPC); Real-time simulation

Abstract

The rapid expansion of offshore wind and solar is placing increasing pressure on transmission infrastructure, challenging energy security, sustainability, and affordability. In response, global policy initiatives are advancing high-voltage direct current (HVDC) “express energy highways” to efficiently transfer bulk renewable power. Voltage-source converter (VSC)-based multi-terminal HVDC (MT-HVDC) grids offer a scalable offshore solution but require advanced control to manage their fast nonlinear dynamics and low inertia. This paper presents a real-time control and dispatch framework for a five-terminal radial-mesh VSC-MMC HVDC grid. A model predictive control (MPC) strategy is developed, automatically coded from Simulink, and deployed on a real-time target for controller-hardware-in-the loop (CHIL) validation using an RTDS® simulator. The setup includes dynamic braking resistors, DC breakers, and integrated human–machine and dispatch interfaces for real-time tuning and supervisory control. Comparative testing under power setpoint changes and AC/DC fault scenarios shows that the proposed MPC achieves more accurate active and reactive power tracking with lower overshoot, improves damping of post-fault oscillations, and enables seamless coordination between local and system-level operations. These results confirm the practical feasibility and operational resilience of MPC-based control for future offshore MT-HVDC systems.

1 Introduction

The global power system is rapidly transitioning due to the integration of variable renewable energy sources (VRES) such as offshore wind and solar PV. By 2050, renewables are projected to supply approximately 80% of global electricity demand [1]. However, large-scale adoption is challenged by the mismatch between generation sites and consumption centers, straining existing transmission infrastructure. To address this, transnational “energy highways” based on high-voltage direct current (HVDC) technology are being developed. European initiatives under the EU Green Deal envision multi-terminal HVDC (MT-HVDC) grids to connect offshore wind hubs to onshore networks [2]. VSC-based MT-HVDC systems enable flexible power routing, support black-start capability, and reduce transmission losses. Germany and the Netherlands plan to deploy offshore hubs such as Heide and NordWest to integrate up to 70 GW of North Sea wind by 2045 [2].

This evolution introduces new technical challenges. HVDC grids are dominated by power-electronic converters, which reduce system inertia and introduce nonlinear, fast dynamic behaviors [3]. Ensuring system stability, equitable power sharing, and resilience under disturbances—especially DC faults, which escalate rapidly due to the absence of natural current zero-crossings, requires more advanced protection and control methods than traditional proportional–integral (PI) controllers [4]. PI controllers can regulate only one variable at a time; consequently, research has shifted towards nonlinear control methods capable of regulating multiple variables within safe boundaries and constraints [5]. However, there is no standard procedure for selecting among nonlinear controllers, and the choice must be tailored to the application requirements. One promising approach is Model Predictive Control (MPC) [5–8], which utilizes optimization and constraints to define control. Both direct and indirect MPC formulations are particularly appealing for systems dominated by power-electronic converters [9]. They have been applied to Modular Multilevel Converter (MMC) units for fast mitigation (within milliseconds) of frequency excursions caused by sudden active power imbalances in low-inertia power systems [10]. Nevertheless, few studies have examined MPC implementation for large-scale real-time simulators [11, 12].

The increasing complexity of HVDC systems necessitates real-time simulation platforms that can emulate electromagnetic transients (EMT) and perform hardware-in-the-loop (HIL) validation. Digital twin (DT) environments replicate full-scale grid behavior, supporting realistic testing of control and protection strategies [13]. HIL enables integration with actual grid components or replicas using standard or experimental protocols [14]. Projects like InterOPERA [15] aim to standardize interfaces and procedures for future European MT-HVDC systems through multi-vendor HIL testing.

This paper presents a real-time control and dispatch framework for a five-terminal radial-mesh VSC-MMC HVDC grid using model predictive control (MPC). A detailed EMT model is implemented on RTDS©, including DC protection devices and dynamic braking. The MPC is tuned

https://doi.org/10.1049/icp.2026.2278

on a single-terminal system, auto-coded from Simulink, and deployed via Aurora for CHIL validation. A Simulink-based HMI enables live tuning and monitoring, while a web-based dashboard facilitates operator interaction and integrates live wind data. Benchmarking against PI and earlier MPC schemes under power steps and AC/DC faults shows improved dynamic response, reduced overvoltages, and faster recovery, validating the MPC's effectiveness for resilient offshore HVDC control.

2 HVDC Grid Testbed Description

This study uses a five-terminal HVDC grid model (Figure 1) inspired by future European offshore networks. It includes two offshore converters (CSA2, CSA3) connected to 2 GW wind farms at 220 kV AC, and three onshore stations (CSA1, CSA4, CSA5) connected to 380 kV AC grids. All converters are bipolar half-bridge MMC VSCs rated at ±525 kV. CSA5 operates as the slack terminal regulating the DC voltage. Control loops follow the generic MMC structure shown in Figure 2, and system parameters are listed in Table 1.

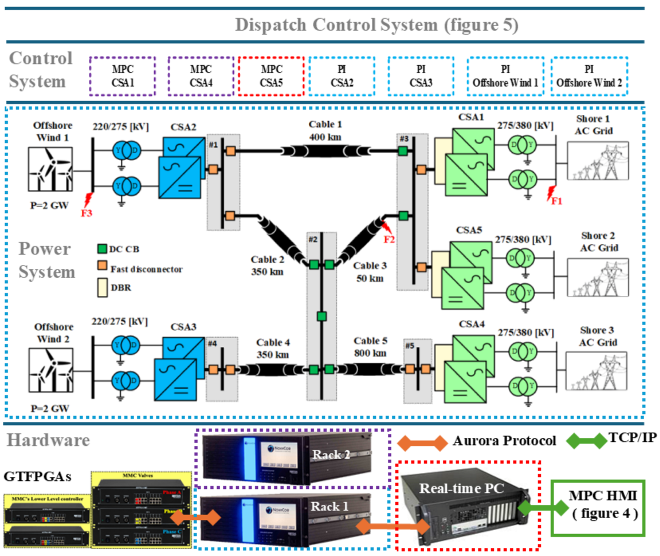

Fig. 1: 5-Terminal HVDC grid representation in RTS with CHIL and dispatch control system.

The bipolar five terminals are connected through three long submarine cables (350–400 km) and two shorter land cables (50 km and 800 km), modeled using frequency-dependent line models to capture propagation delays and high-frequency transients. Onshore stations are equipped with dynamic breaking resistors (DBRs) that activate in the event of DC overvoltage to absorb excess energy. The network also includes five DC switching stations: two employ fast voltage-assisted resonant DC breakers for fault interruption, while the remaining three use high-speed disconnectors for post-fault reconfiguration.

The full HVDC grid runs in real-time on an RTDS® simulator. Most converters use average-value VSC models (Type 5), except CSA1, which uses a detailed switching model (Type 4) for increased fidelity. Offshore wind farms are represented by Type 4 equivalent models, with real wind speed data injected via TCP/IP from North Sea sites [17]. This high-fidelity testbed supports comprehensive CHIL validation of the MPC strategy for realistic steady-state and fault scenarios.

Table 1 Control Modes and System Parameters of the HVDC Testbed

Parameter	Converters		
	CSA5	CSA2–A3	CSA1–A4
Active power [MW]	2000	2000	2500
Control mode	Vdc–Vac	Vac–f	P–Vac
Reactive power [MVAR]	–	–	–
Number of submodules per arm	240	200	240
MMC arm inductance [mH]	25	49.7	25
Transformer leakage reactance [pu]	0.18	0.15	0.18
AC point of common coupling voltage [kV]	380	220	380
DC-link voltage [kV]		±525	
Rated power [MVA]		2000	
Capacitor energy per submodule (SM) [MJ]		30	
MMC arm resistance [Ω]		0.544	
Rated voltage/current per SM [kV/kA]		2.5 / 2	
AC converter bus voltage [kV]		275	
Wind farm PCC voltage [kV]		66	

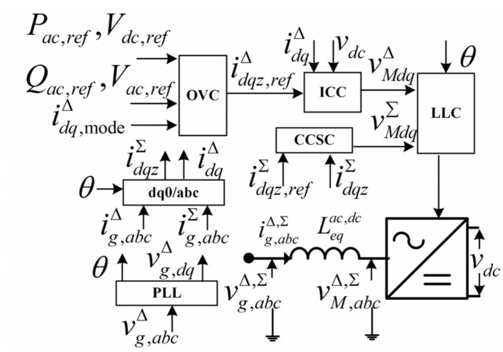

Fig. 2: Generic block diagram representation of MMC converter control loops. Implementation details are in [16].

3 Model Predictive Control Design

3.1 Analytical MMC Model

A decade of development in the modelling of MMCs has led to an accurate MMC non-linear model [12, 16]. The dynamics of the MMC can be formulated by using two components, Σ and Δ, which represent the DC and AC characteristics of the converter, respectively. By applying the Clarke-Park transformation, the Σ and Δ ac components are translated into the stationary $dq-$frame given in [18] and sumerised here:

$$\frac{d}{dt}(\vec{i}^{\Delta}_{dq}) = \frac{\vec{v}^{\Delta}_{Mdq} - (\omega L^{ac}_{eq} J_2 + R^{ac}_{eq} I_2)\vec{i}^{\Delta}_{dq} - \vec{v}^{G}_{dq}}{L^{ac}_{eq}}, \tag{1a}$$

$$\frac{d}{dt}(\vec{i}^{\Sigma}_{dq}) = -\frac{\vec{v}^{\Sigma}_{Mdq} + (R_{arm} I_2 - 2\omega L_{arm} J_2)\vec{i}^{\Sigma}_{dq}}{L_{arm}}, \tag{1b}$$

$$\frac{d}{dt}(i^{\Sigma}_{z}) = \frac{v_{dc}}{2L_{arm}} - \frac{v^{\Sigma}_{Mz} + R_{arm}\, i^{\Sigma}_{z}}{L_{arm}}. \tag{1c}$$

The definition of the zero-sequence component current is given with the equation (1a). Its physical importance is actually its influence on the DC current since $i_{dc} = 3i^{\Sigma}_{z}$.

$$\mathbf{A} = \text{diag}_{8\times8}\begin{cases} \mathbf{A}_{11} = -\frac{R_{arm}}{L_{arm}},\ \mathbf{A}_{12} = 2\omega,\ \mathbf{A}_{21} = -2\omega \\ \mathbf{A}_{22} = -\frac{R_{arm}}{L_{arm}},\ \mathbf{A}_{33} = -\frac{R_{arm}}{L_{arm}},\ \mathbf{A}_{38} = \frac{0.5}{L_{arm}} \\ \mathbf{A}_{44} = -\frac{R^{eq}_{ac}}{L^{eq}_{ac}},\ \mathbf{A}_{45} = -\omega,\ \mathbf{A}_{46} = -\frac{1}{L^{eq}_{ac}} \\ \mathbf{A}_{54} = \omega,\ \mathbf{A}_{55} = -\frac{R^{eq}_{ac}}{L^{eq}_{ac}},\ \mathbf{A}_{57} = -\frac{1}{L^{eq}_{ac}} \end{cases} \tag{4}$$

$$\mathbf{B} = \text{diag}\left\{-\frac{1}{L_{arm}},\ -\frac{1}{L_{arm}},\ -\frac{1}{L_{arm}},\ \frac{1}{L^{ac}_{eq}},\ \frac{1}{L^{ac}_{eq}},\ 0,\ 0,\ 0\right\}$$

3.2 Formulation of MPC

The *dq*-frame mathematical model of the MMC is represented by equations (1a), and is rewritten in a matrix discrete form which given in [12]

The augmented state in [12]is defined as $\Delta\vec{x}(k) = \vec{x}(k) - \vec{x}(k-1)$, where $\vec{x}(k) \in \mathbb{R}^8$ indicates the system state vector at k^{th} instant and $\vec{x}(k-1)$ indicates the vector of states for the previous sampling instance $k-1$. Similarly, the augmented input is defined as $\Delta\vec{u}(k) = \vec{u}(k) - \vec{u}(k-1)$, where $\vec{u}(k)$ represents the system inputs at k^{th} instant and $\vec{u}(k-1)$ indicates the past inputs. The vector $\vec{x} = \left[i^{\Sigma}_{d}, i^{\Sigma}_{q}, i^{\Sigma}_{z}, i^{\Delta}_{d}, i^{\Delta}_{q}, v^{G}_{d}, v^{G}_{q}, v_{dc}\right]^{T}$ represents state variables, while $\vec{u} = \left[v^{\Sigma}_{Md}, v^{\Sigma}_{Mq}, v^{\Sigma}_{Mz}, v_{Md}, v_{Mq}\right]^{T}$, with $\vec{u} \in \mathbb{U} = [-1.1, 1.1]^5 \subset \mathbb{R}^5$, represents system inputs.

The future control sequence is represented by $\Delta\vec{u}(k) \in [-1, 1]^5 \subset \mathbb{R}^5$, which is determined by solving the optimal control problem, and minimizing the objective (cost) function, subjected to the equality and inequality constraints:

$$\begin{aligned} \min_{\Delta\vec{u}} J = \sum_{j=1}^{N_p-1} \|\vec{x}_m(k+j|k)\|^2_{\mathbf{Q}} + \left\|\vec{\Delta u}\right\|^2_{\mathbf{R}} + \\ I_d e(k) + \|\vec{x}_m(k+N_p|k)\|^2_{\mathbf{Q_{LQR}}}, \end{aligned} \tag{3}$$

$$\text{subject to } \mathbf{M}\vec{\Delta u} \leq \vec{b},$$

$$\vec{x}_m(k+j|k) = \vec{r}(k) - \vec{y}_m(k|k)$$

Here, $\mathbf{Q} \succeq 0$ and $\mathbf{R} \succ 0$ are weighting matrices, and $N_p = 20 \in \mathbb{I}^{+}$ is the prediction horizon. For variables $\vec{x}_m(k)$, vector $r(k) \in \mathbb{R}^8$ is a reference signal. The matrix $\mathbf{M}$ and vector $\vec{b}$ define the rate and amplitude constraints applied to the control inputs [18]. In practice, modeling inaccuracies and measurement noise introduce an error term $e(k)$, representing the deviation between the measured and predicted outputs at the k^{th} time step. This disturbance is incorporated into the objective function using the weighting matrix $I_m \succ 0$.

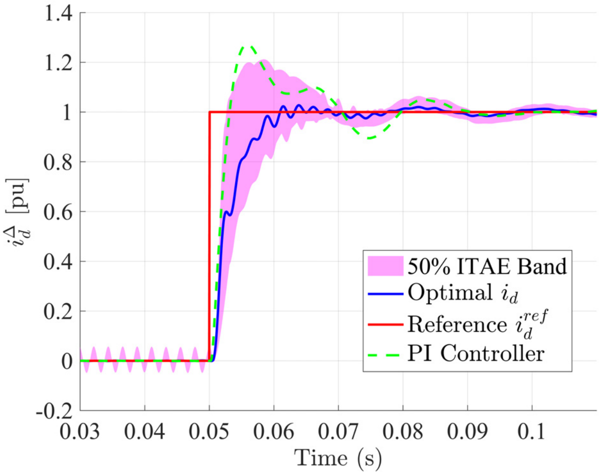

Fig. 3: i^{Δ}_{d} responses within 50% of optimal ITAE, comparison of optimal i_d value, its reference and PI controller output.

Optimal values for T_s and N_p are identified by evaluating 1000 combinations (see Algorithm 1), selecting the configuration with the minimum ITAE. The best case for $T_s = 20\,\mu s$, and $N_p = 70$, yields RMSE = 0.0626, IAE = 0.0046, ISE = 0.0020, ITAE = 4.13×10^{-4}, and ITSE = 1.01×10^{-4}. Its step response is benchmarked against a PI controller with 50% higher ITAE in Figure 3.

Algorithm 1 Tuning of T_s and N_p for MPC via ITAE Minimization

Input: $T_s \in \{5{:}5{:}100\}$, $N_p \in \{5{:}5{:}250\}$
Initialize: minITAE $\leftarrow \infty$
for each T_s **do**
  for each N_p **do**
    Update Simulink model with (T_s, N_p)
    Auto-generate C code and run RTDS©
    Perform step test, collect $y(t), y_{\text{ref}}(t)$
    Compute metrics: RMSE, IAE, ISE, ITAE, ITSE
    if no fault and ITAE < minITAE **then**
      Store current T_s, N_p; update minITAE
    end if
  end for
end for
Output: Optimal T_s, N_p with lowest ITAE

4 Real-Time Implementation and CHIL Setup)

4.1 Controller Hardware-in-the-Loop Configuration

Figure 1 shows the setup of the Controller Hardware-in-the-Loop (CHIL) system. The controller is deployed on a real-time PC, referred to as a *soft-DSP*, which serves as a PC-based real-time platform for power electronic control. The control loop operates at a high sampling rate of up to 20 kHz over a high-speed serial communication link.

The real-time PC acts as the control target for computation-intensive tasks and is capable of executing control algorithms with real-time performance up to 16 kHz. It is built on an x64 Intel i5 processor running a real-time Linux operating system. This setup enables reliable and deterministic execution of advanced control algorithms, such as MPC, under realistic timing constraints. Communication between the soft-DSP controller and the RTDS© simulator is established using the Aurora protocol over fiber-optic links. This high-speed, low-latency protocol enables the continuous exchange of measured variables and control references. The controller receives real-time measurements from RTDS© for each pole of the converter station, namely, i_d^{Σ}, i_q^{Σ}, i_z^{Σ}, i_d^{Δ}, i_q^{Δ}, v_d^G, v_q^G, and v_{dc}, and computes control actions, namely, v_{Md}^{Σ}, v_{Mq}^{Σ}, v_{Mz}^{Σ}, v_{Md}, and v_{Mq}, which are sent back within each sampling interval.

The CHIL configuration shown in Figure 1 enables closed-loop interaction between the simulated HVDC system in RTDS© and the physical controller executing the MPC algorithm. This setup validates the real-time feasibility, stability, and responsiveness of the proposed control strategy.

Figure 4 illustrates the validation results for four different controller implementations: PI control, MPC-CBuilder, MPC-rtt, and LMPC-rtt. The PI and MPC-CBuilder controllers are executed entirely within the RTDS© environment. In particular, the MPC-Cbuilder runs at a main simulation timestep of 70 μs. CBuilder, part of the RTDS© software suite, allows users to write custom control algorithms in C code, which are compiled and integrated as black-box models in the simulation. The PI controller, by contrast, uses standard library models provided within the RTDS© environment.

The MPC-rtt and LMPC-rtt controllers are compiled and deployed on the real-time PC shown in Figure 1. The LMPC-rtt refers to a Laguerre-based MPC from [18], while the MPC-rtt corresponds to the proposed MPC design introduced in this study, implemented on a soft-DSP. The closed-loop control via MPC-rtt experiences an overall latency of approximately three simulation timesteps, amounting to roughly 210 μs.

The Figure 4 shows a comparison for a step change in the i_d^{Δ} reference current, and the tracking performance of each controller is evaluated in terms of accuracy and response time. As shown in the figure, MPC-Cbuilder offers a better response with a faster settling time among all the MPCs, whereas PI control exhibits overshoot. The MPC-rtt and LMPC-rtt provide slower responses due to the latency of the signals.

5 Real-Time Interface Architecture

A unified real-time interface has been developed for monitoring and controlling the five-terminal VSC-HVDC system during CHIL testing. It integrates a Simulink-based Human–Machine Interface (HMI) for controller-level interaction and a web-based Dispatch Control Center (DCC) for system-level supervision. The HMI enables real-time tuning and signal visualization via data exchange between the controller running on a real-time PC and the engineering PC. Meanwhile, the DCC features a browser-based frontend and a Python-based backend interfaced with the RTDS© simulator via TCP/IP. As shown in Figure 5, the dashboard provides real-time plots, terminal-specific views, and control setpoints, while the backend also supports live integration of external data such as wind forecasts. Together, the HMI and DCC enable closed-loop tuning, operator control, and CHIL-based validation within a digital twin framework.

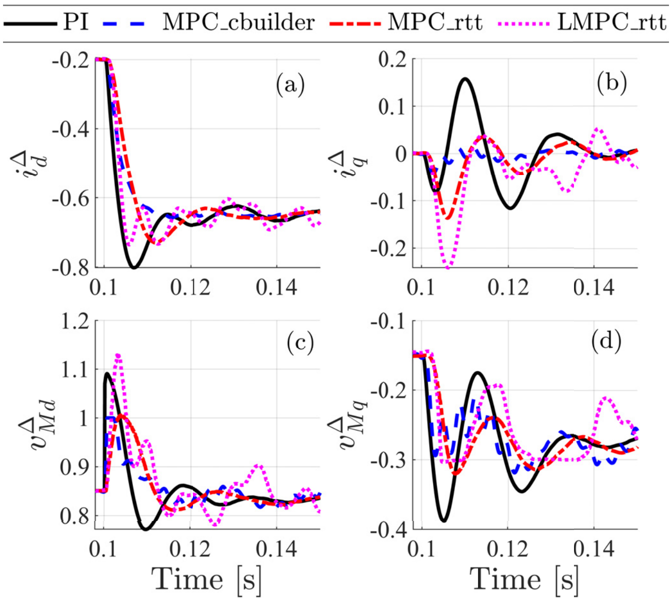

Fig. 4: Comparison of PI, MPC-Cbuilder, MPC-rtt, and LMPC-rtt controllers in tracking a step change in i_d^{Δ} and impact on controller input and output.

6 Simulation Results and Discussion

In this section, only the results from the CSA1 converter station are presented due to page limitations. The observed trends are representative of the overall system behavior, and the performance of the controllers at other terminals follows similar patterns. The section evaluates the steady-state, transient, and fault ride-through performance of four controller implementations: PI, MPC implemented within RTDS© using C-builder (*MPC-Cbuilder*), proposed MPC implemented in Real-time PC (*MPC-rtt*), and Laguerre MPC implemented in Real-time PC (*LMPC-rtt*).

6.1 Steady-State and Reference Change Tests

Figure 6 compares the tracking performance of all four controllers for a large step change in active power setpoint (from -750 MW to -2400 MW). In Fig. 6(a), the pole-to-pole DC voltage $V_{\mathrm{dc,CSA1}}$ falls to about 900 kV immediately after the step. This sudden dip in DC voltage reflects the imbalance caused by the increased power transfer. The slack converter (CSA5) subsequently adjusts its output to restore the DC link

Fig. 5: Web-based dashboard showing terminal-specific data, live plots, and control elements.

voltage to its nominal value. Concurrently, the positive pole DC current $I_{\mathrm{dc,CSA1P}}$ rises sharply under all controllers to supply the higher power (Fig. 6(b)).

All controller implementations successfully track the new active power reference, as seen by the similar $P_{\mathrm{ac,CSA1}}$ responses in Fig. 6(c). The active power quickly reaches the new setpoint with minimal steady-state error, indicating adequate controller tuning. However, the controllers differ in their reactive power response: the PI and *LMPC-rtt* responses exhibit larger deviations and slower settling in $Q_{\mathrm{ac,CSA1}}$, whereas *MPC-Cbuilder* and *MPC-rtt* limit the reactive power overshoot and recover more quickly (dashed lines in Fig. 6(c)). This behavior implies that the proposed MPC-based controllers achieve better decoupling of active and reactive power control. In other words, by directly optimizing the d- and q-axis currents, the MPC schemes minimise the cross-coupling between P and Q.

These findings show that the proposed MPC controllers (*MPC-Cbuilder* and *MPC-rtt*) maintain tighter control over P_{ac} and Q_{ac} simultaneously.

6.2 Disturbance and Fault Ride-Through Performance

6.2.1 Positive pole-to-ground DC fault: Figures 7 and 8 illustrate the system and controller responses during a positive pole-to-ground fault at the terminal of Cable 3 (between CSA1 and CSA3). The fault occurs at $t = 0.100$ s and is cleared at about $t = 0.120$ s. In Fig. 7(a), the DC voltage $V_{\mathrm{dc,CSA1}}$ drops to roughly 990 kV immediately when the fault is applied. Simultaneously, the positive pole current $I_{\mathrm{dc,CSA1P}}$ rise to 3 kA and reduces after that. This reduction of current is because the DC circuit breaker (DC CB) commutes the fault current into its injection and energy-absorption branches after fault interruption. Once the breaker interrupts the fault current, the series-connected surge arrester causes a brief overshoot in the DC voltage (Fig. 7(a)). Thereafter, the DC bus undergoes a damped oscillation at approximately 450 Hz, corresponding to the resonance between the DC reactor and the injection-branch capacitor of the CB. This oscillation is well damped in all cases after fault clearance. During this disturbance, the slack converter (CSA5) helps restore the DC link and balance the pole voltages.

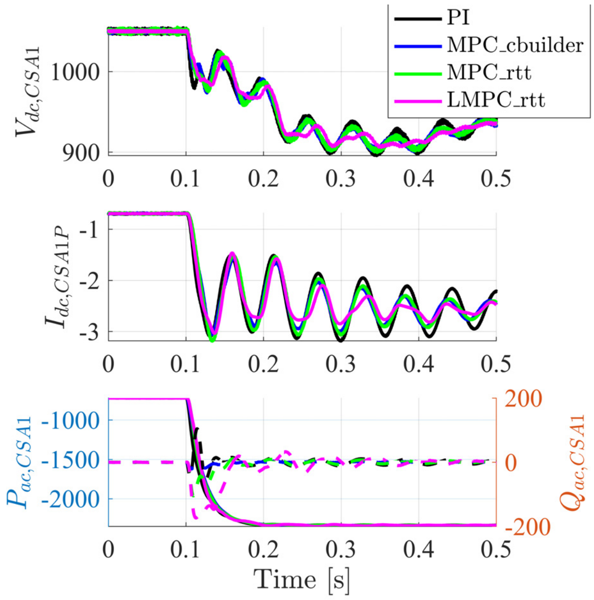

Fig. 6: Comparison of PI, MPC-Cbuilder, MPC-rtt, and LMPC-rtt controllers under a large active power reference step: (a) pole-to-pole DC voltage ($V_{dc,CSA1}$ in kV), (b) positive pole DC current ($I_{dc,CSA1P}$,in kA); (c) active power ($P_{ac,CSA1}$, solid, in MW) and reactive power ($Q_{ac,CSA1}$, dashed, in MVAr) measured at the AC point of connection of CSA1.

Figure 8 shows the converter controller inputs and outputs during the DC fault. The direct-axis current deviation $i_d^{\triangle}$ (Fig. 8(a)) and the quadrature-axis deviation $i_q^{\triangle}$ (Fig. 8(b)) peak at about -0.65 pu and -0.40 pu respectively for all controllers. The controllers respond by adjusting their voltage references ($v_{Md}^{\triangle}$ and $v_{Mq}^{\triangle}$ in Figs. 8(c,d)). During the DC fault, all controller has similar performance. However, the MPC-based controllers command slightly smaller overshoots in pole voltage, reflecting the reduced current error.

In summary, the *MPC-rtt* controllers exhibit slightly fault ride-through performance on the DC side to PI, as seen in both the system-level and controller-level responses.

6.2.2 Onshore Three-phase AC fault : Figure 9 and Fig. 10 present the response to a three-phase fault at CSA1's AC point

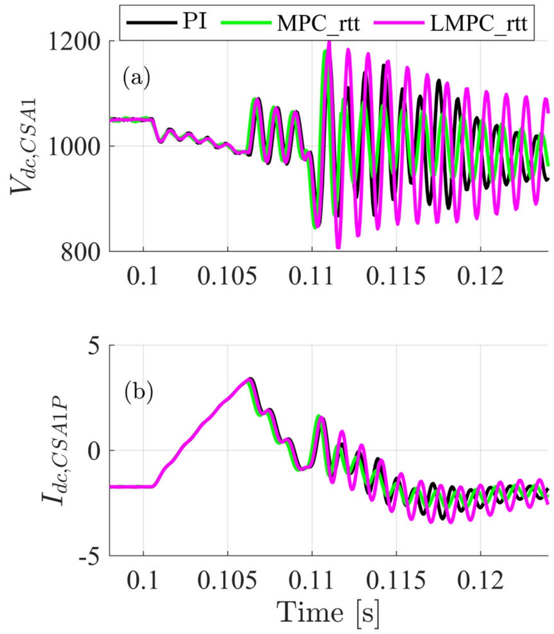

Fig. 7: System performance during a positive pole-to-ground DC fault at the terminal of Cable 3 (between CSA1 and CSA3): (a) pole-to-pole DC voltage ($V_{dc,CSA1}$, in kV), (b) positive pole DC current ($I_{dc,CSA1P}$, in kA) at CSA1.

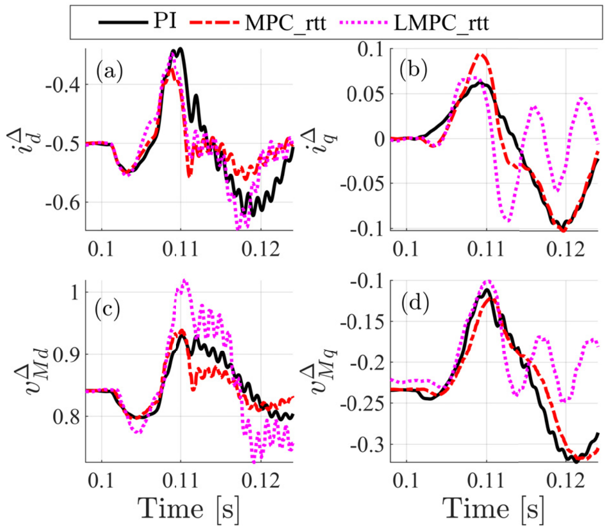

Fig. 8: Impact of a positive pole-to-ground fault at the terminal of Cable 3 on controller input and output signals for PI, MPC-Cbuilder, MPC-rtt, and LMPC-rtt controllers.

of connection (occurring at 0.100 s and cleared at 0.200 s). During this fault, the AC voltages collapse, so the converter momentarily stops active power injection. In the DC side (Fig. 9(a) and (b)), $V_{\mathrm{dc,CSA1}}$ dips slightly and $I_{\mathrm{dc,CSA1P}}$ spikes as the controller reacts. The key difference among controllers appears in the transient behavior of d-axis current $i_d^{\triangle}$ (Fig. 10(a)). Under PI control, $i_d^{\triangle}$ deviates to about -2.0 pu and takes longer to settle. In contrast, *MPC-Cbuilder* and *LMPC-rtt* limit the peak deviation to roughly -1.5 pu and stabilize by

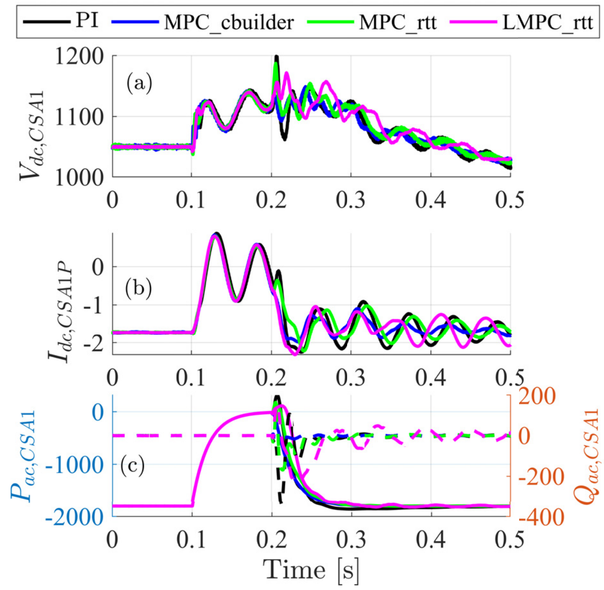

Fig. 9: Controller performance during a three-phase fault at the AC point of connection of CSA1: (a) pole-to-pole DC voltage ($V_{dc,CSA1}$, in kV) (b) positive pole DC current ($I_{dc,CSA1P}$, in kA) at CSA1; (c) active power ($P_{ac,CSA1}$, solid lines, in MW) and reactive power ($Q_{ac,CSA1}$, dashed, in MVAr) at CSA1.

about 0.150 s after fault clearing. Their corresponding voltage commands ($v_{Md}^{\triangle}$ and $v_{Mq}^{\triangle}$ in Fig. 10(c,d)) exhibit reduced overshoot and return to steady-state quicker (by roughly 0.120 s).

As a result, the AC active and reactive power (Fig. 9(b)) recover faster under MPC: the deviations are smaller and they return to pre-fault values within about 0.1 s. The DC link voltage and current (Fig. 9(a)), as well as the AC RMS voltage and phase current (Fig. 9(c)), also settle back to normal levels by about 0.3 s. These observations indicate that predictive control improves fault ride-through capability by anticipating the fault impact and reducing the excursion in the converter currents. In summary, MPC achieves a cleaner transient during the AC fault, with smaller overshoots in both controller currents and converter outputs than the PI.

7 Conclusion

This paper has presented a real-time control and dispatch framework for a five-terminal VSC-HVDC grid, validated through controller-hardware-in-the-loop (CHIL) experimentation. A key contribution is the design and real-time implementation of a model predictive control (MPC) strategy, which is auto-coded and deployed on a real-time target, enabling fast and coordinated control of a radial-mesh HVDC system that integrates offshore wind power and protection elements. A web-based dispatch interface further enables operator-level interaction and system monitoring.

CHIL tests under representative scenarios—including large power setpoint changes and AC/DC fault events—revealed several critical insights: (i) the proposed MPC achieves accurate active/reactive power tracking with reduced overshoot

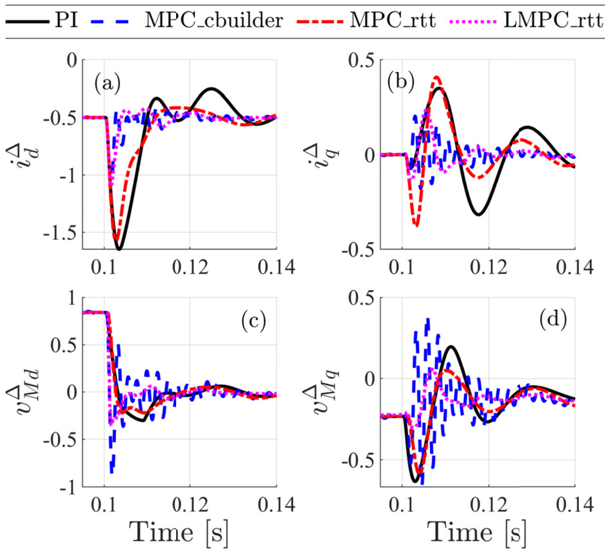

Fig. 10: Impact of a three-phase fault at the AC PoC of CSA1 on controller input and output signals for PI, MPC-Cbuilder, MPC-rtt, and LMPC-rtt controllers.

versus PI controllers, (ii) it effectively damps post-fault oscillations to enhance fault ride-through performance, and (iii) it supports coordinated operation with supervisory interfaces. These findings demonstrate the potential of MPC for improving resilience and reliability in multi-terminal HVDC grids.

Future work will extend this platform toward physical hardware-in-the-loop testing with actual converter and protection devices, scale the control approach to larger HVDC networks, explore adaptive and decentralized MPC strategies, and integrate market-based dispatch mechanisms for real-time operation.

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