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A Wide-Dynamic-Range Photovoltaic Energy Harvester With Adaptive Power-Scalable MPPT Control and Direct Power-to-Digital Converter

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***Abstract*—This article presents a photovoltaic energy harvester (PVEH) that achieves high maximum power point tracking (MPPT) efficiency and power conversion efficiency across a 100 000× input power dynamic range (DR) (from 10 μW to 1 W). Wide-dynamic-range operation is challenging due to the inherent tradeoff between MPPT accuracy and controller power consumption. To address this, an adaptive power-scalable MPPT scheme is proposed, employing a direct power-to-digital converter (PDC) that eliminates the need for current sensing, analog multipliers, or lookup tables (LUTs). The PDC utilizes an equivalent power comparison technique, minimizing its power consumption. The MPPT controller autonomously scales its power, consuming minimal energy in low-irradiation conditions while maintaining high tracking accuracy and speed in high-irradiation conditions. Furthermore, a multiple-counting technique mitigates comparator noise and settling errors. Implemented in a 180-nm CMOS process, the harvester achieves a peak MPPT efficiency of 99.9% and maintains >98% across the entire range, representing a 10× improvement in DR over prior art. It also achieves a competitive power conversion efficiency of >82% (peak of 92%) over the same DR.**

***Index Terms*—Buck–boost converter, Internet of Things (IoT), maximum power point tracking (MPPT), photovoltaic energy harvesting, power management, power-scalable design, power-to-digital converter (PDC), wide dynamic range (DR).**

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I. Introduction

PHOTOVOLTAIC energy harvester (PVEH) often serves an important role for enabling self-sustaining, maintenance-free Internet of Things (IoT) nodes [1], [2], [3] deployed in outdoor environments. The ultimate objective of a PVEH system is to maximize the energy extracted from photovoltaic (PV) cells under vastly fluctuating irradiation conditions. This translates into two critical and concurrent efficiency metrics for the power management integrated circuit (IC): high maximum power point tracking (MPPT) efficiency (η_{MPPT}) to ensure the PV cell operates near its optimal point, and high-power conversion efficiency (η_{CONV}) to minimize losses within the harvester itself. Achieving both simultaneously across a wide input power dynamic range (DR), from moonlight to full sunlight, remains a challenge.

The expansion of the DR is fundamentally hampered by inherent tradeoffs between precision, speed, and power overhead. Existing MPPT strategies can be broadly categorized, each with its own limitations in wide DR operation. Fractional open-circuit voltage (FOCV) methods [2], [3], [4], [5], [6], [7] are simple but suffer from periodic energy-harvesting interruption and inherent inaccuracy due to their reliance on pre-characterized lookup tables (LUTs), which are sensitive to process, voltage, and temperature (PVT) variations. Perturb-and-observe (P&O) methods [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21] are more accurate but necessitate input power measurement. Prior implementations of power measurement incur significant overheads: pulse-integration power detectors [4], analog multipliers followed by analog-to-digital converters (ADCs) [9], and pulse-based multipliers [10], which either consume excessive power that degrades η_{CONV} in low-irradiation (LI) conditions or only offer a high η_{MPPT} over a limited DR. While voltage and current sensing circuits [1], [8] enhance MPPT accuracy, they also introduce additional circuit complexity and power overhead. High-precision MPPT techniques with sufficient tracking speeds are essential, as implemented in [10] and [11], they improve the tracking accuracy at specific input power but introduce energy overhead at lower input power in the LI condition, limiting the DR for >85% η_{CONV} to only ~ 6×. Moreover, as input power increases in high irradiation (HI), the limited bandwidth of MPPT further constrains the DR for

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>98% η_{MPPT} to only 9× and 5×. Other studies have explored minimizing the MPPT controller's power consumption by using LUTs [4], [12], [13]. Notably, Hung et al. [12] achieve an impressive 1000× DR for >85% η_{CONV} and 10 000× DR for >98% η_{MPPT}. However, its dependence on LUTs compromises robustness over PVT and aging variations.

Consequently, the development of a PVEH system with wide DR, high efficiency, and inherent robustness remains unresolved. The core challenge lies in creating an MPPT controller whose power consumption and performance can adapt to the input power level, without relying on any external references.

This article is an extended version of [22]. We present a buck–boost PVEH that overcomes the above limitations by introducing a fully integrated, adaptive power-scalable MPPT scheme. The proposed system eliminates the need for explicit voltage/current sensors, analog multipliers, ADCs, or pre-characterized LUTs. Instead, it employs a direct power-to-digital converter (PDC) that enables a P&O algorithm where the power consumption of the entire MPPT controller automatically scales, from 10 μW to 1 W, with input power.

The key contributions of this work are given as follows.

1) A novel direct power-to-digital conversion technique based on a digital controlled oscillator (DCO) and an equivalent power comparison algorithm, which enables accurate power measurement without power-hungry analog blocks, reducing the PDC's power consumption.
2) An adaptive power-scalable MPPT architecture where the bias currents of critical circuits are autonomously adjusted based on the input power level. This ensures minimal quiescent power at LI for high η_{CONV} and sufficient speed/accuracy at HI for high η_{MPPT}.
3) A multiple-counting technique to mitigate the effects of comparator noise and settling errors, ensuring >98% η_{MPPT} across the entire DR.

The remainder of this article is organized as follows. Section II details the overall system architecture and its operating principle. Section III introduces the MPPT control strategies and algorithms. Section IV presents the circuit-level implementation of the proposed PDC and the power-scaling mechanism. Section V presents the measurement results, validating the system's performance against the state of the art. Finally, Section VI concludes this article.

II. System Architecture and Operating Principle

A. Top-Level System Architecture

Fig. 1 depicts the overall architecture of the proposed PV energy harvester, designed to maximize both power conversion and MPPT efficiency across an ultra-wide input power range. The system is built around a single-inductor buck–boost converter, chosen for its ability to regulate the output voltage irrespective of whether the PV panel voltage is above or below the battery voltage, a common scenario under varying environmental conditions.

The converter employs pulse frequency modulation (PFM) [23] using a hysteresis controller at the input and operates in the discontinuous conduction mode (DCM) [23] with a

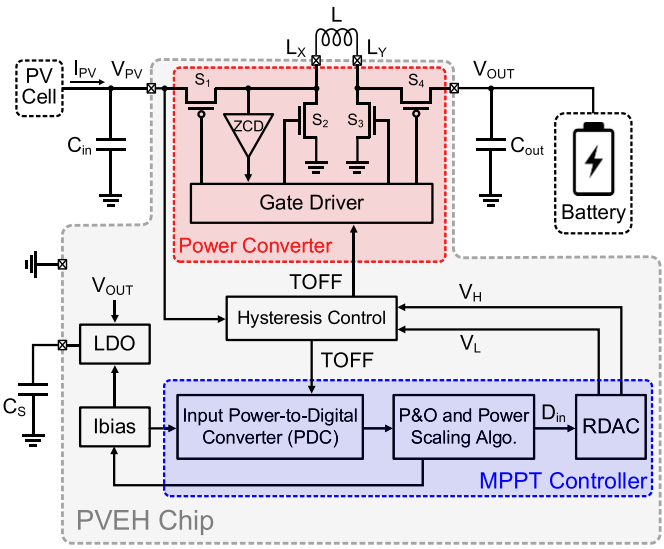


Fig. 1. Overall architecture of the proposed PVEH with adaptive power-scalable MPPT controller.

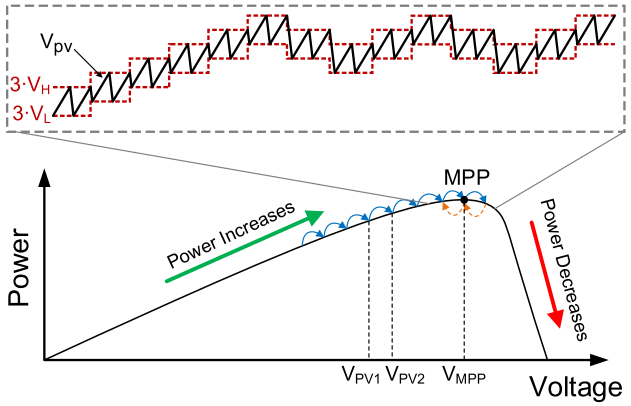


Fig. 2. P&O algorithm and converged V_{PV}.

dedicated zero-current detection (ZCD) circuit [23], which will be introduced in detail later. This leads to a converter switching frequency proportional to the input PV current, minimizing switching losses especially in LI conditions.

The core innovation lies in the adaptive power-scalable MPPT controller, which forms a closed-loop control system around the power converter. This controller is comprised of three primary blocks.

1) A PDC that directly measures the input power.
2) An asynchronous digital state machine that executes the MPPT and power-scaling algorithm.
3) An RDAC that sets the operating voltage of the PV cell.

The primary control variable is the PV voltage V_{PV}. A hysteretic controller regulates V_{PV} within a programmable hysteresis window defined by an upper bound V_H and a lower bound V_L. The MPPT controller's objective is to dynamically reposition this hysteresis window to center on the true maximum power point voltage (V_{MPP}). It achieves this by comparing the input power at two different voltage setpoints (V_{PV1} and V_{PV2} in Fig. 2) in consecutive measurement cycles

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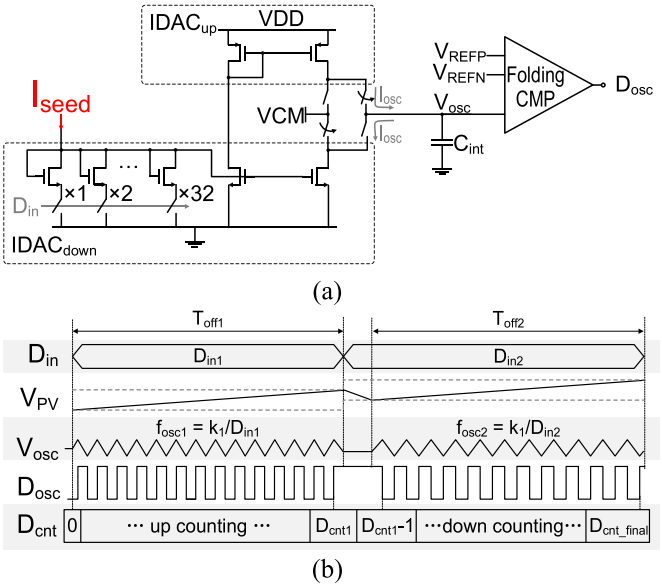


Fig. 3. Working principle of the PDC. (a) DCO with a current divider IDAC. (b) Timing diagram.

and accordingly adjusting the digital code D_{in} of the RDAC to change V_H and V_L.

B. Principle of Direct Power-to-Digital Conversion

The key to the wide DR MPPT operation is the PDC, which translates the input power P_{in} directly into a digital value without intermediate, high-overhead analog processing. Its operation is grounded in the fundamental relationship between the converter's OFF-time and the input power.

Throughout this article, T_{off} denotes the time duration of the converter's OFF-phase, while T_{off} refers to the digital control signal that is high during this phase. During the OFF-time (T_{off}) of the buck–boost converter, the inductor is disconnected from the PV cell, allowing the input capacitor C_{in} to be charged by the PV current I_{PV}. T_{off} is defined by C_{in} and I_{PV} through a fixed voltage window $V_{HYS} = V_H - V_L$

$$T_{\text{off}} = \frac{V_{HYS} \cdot C_{in}}{I_{PV}}. \tag{1}$$

Starting from the definition of input power, $P_{in} = V_{PV} \cdot I_{PV}$, and substituting I_{PV} from (1), we obtain

$$P_{in} = V_{PV} \cdot \frac{V_{HYS} \cdot C_{in}}{T_{\text{off}}}.$$

Rearranging this equation reveals the key insight for direct power measurement

$$\frac{1}{P_{in}} = \frac{T_{\text{off}}}{V_{PV} \cdot V_{HYS} \cdot C_{in}}. \tag{2}$$

Equation (2) demonstrates that the quantity $T_{\text{off}} \cdot (1/V_{PV})$ is directly proportional to $1/P_{in}$ for a constant V_{HYS}. In practice, V_H and V_L are programmable via the RDAC, but the proportionality relationship remains valid for each fixed setting. Therefore, the core task of the PDC is to measure this specific composite quantity.

The proposed PDC accomplishes this by employing a DCO-based integrator and an upcounter/downcounter, as shown in Fig. 3. Since the hysteresis window boundaries V_H and V_L are set by the digital code D_{in} of the RDAC, and V_{PV} is regulated within this window, the system possesses direct knowledge of its digital representation. The DCO is configured such that its oscillation frequency f_{osc} is proportional to $1/D_{in}$, and hence to $1/V_{PV}$. By counting the number of oscillations D_{cnt} occurring within a single T_{off} period, the PDC produces a digital output given by

$$D_{cnt} = f_{osc} \cdot T_{\text{off}} \propto \frac{1}{V_{PV}} \cdot T_{\text{off}} \propto \frac{1}{P_{in}}. \tag{3}$$

Thus, D_{cnt} serves as a direct digital representation inversely proportional to the input power.

While this principle is mathematically sound, a straightforward circuit implementation would be very power-consuming as it would require a current DAC (IDAC) with a large, static seed current (I_{seed}) to support the highest DCO frequencies, undermining system efficiency at low input power. The solution to this critical challenge, the equivalent power comparison technique, along with other system-level strategies for robustness and power scaling, will be detailed in Sections III and IV.

III. MPPT Control Strategies and Algorithms

This section details the key control strategies and algorithms that enable the system to achieve high efficiency across the 100 000× DR. These strategies address the fundamental challenges of power consumption, precision, and robustness that arise when operating from 10 μW to 1 W.

A. Equivalent Power Comparison

A direct implementation of the principle described in Section II-B would require a power-hungry IDAC. This is because, to measure $T_{\text{off}}/V_{\text{PV}}$ according to (3), the DCO must oscillate at a frequency $f_{\text{osc}} \propto 1/V_{\text{PV}}$. At low PV voltages, this demands a very high f_{osc} to maintain sufficient counting resolution within a short T_{off}. Generating such high frequencies necessitates a large bias current [I_{seed} in Fig. 3(a)], which would dominate system power consumption under LI conditions and severely degrade η_{CONV}.

To overcome this, we propose an equivalent power comparison scheme. The key insight is that the P&O algorithm does not require the absolute value of input power P_{in}; it only needs to correctly determine the sign of the power difference between two measurement cycles, i.e., $P_{\text{in2}} - P_{\text{in1}}$, where P_{in1} and P_{in2} correspond to PV voltages set by digital codes D_{in1} and D_{in2}, respectively.

From (2), we know $1/P_{\text{in}} \propto T_{\text{off}}/V_{\text{PV}}$. Therefore, comparing P_{in1} and P_{in2} is equivalent to comparing the quantities $T_{\text{off1}}/V_{\text{PV1}}$ and $T_{\text{off2}}/V_{\text{PV2}}$. The proposed technique avoids generating a DCO frequency proportional to $1/V_{\text{PV}}$ by cross-coupling the digital control codes between measurement cycles, as illustrated in Fig. 4.

During the first measurement cycle (with PV voltage set by D_{in1}), instead of setting $f_{\text{osc1}} \propto 1/D_{\text{in1}}$, we program the DCO

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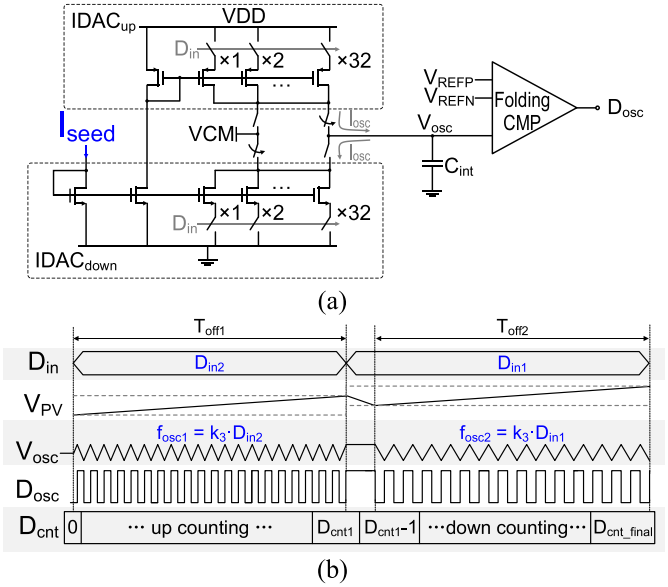


Fig. 4. Proposed PDC with the equivalent power comparison technique. (a) DCO schematic. (b) Timing diagram.

frequency to be proportional to the other code: $f_{\text{osc1}} = k_3 \cdot D_{\text{in2}}$. The resulting oscillation count is $D_{\text{cnt1}} = f_{\text{osc1}} \cdot T_{\text{off1}} = k_3 \cdot D_{\text{in2}} \cdot T_{\text{off1}}$. Conversely, during the second cycle (with PV voltage set by D_{in2}), we set $f_{\text{osc2}} = k_3 \cdot D_{\text{in1}}$, yielding $D_{\text{cnt2}} = k_3 \cdot D_{\text{in1}} \cdot T_{\text{off2}}$.

The upcounter/downcounter integrates these counts, counting up during the first cycle and down during the second. The final decision variable is their difference

$$\begin{aligned} D_{\text{cnt,final}} &= D_{\text{cnt1}} - D_{\text{cnt2}} \\ &= k_3 \cdot (D_{\text{in2}} \cdot T_{\text{off1}} - D_{\text{in1}} \cdot T_{\text{off2}}). \end{aligned} \tag{4}$$

Substituting (1) and noting that $D_{\text{in}} \propto V_{\text{PV}}$, (4) simplifies to

$$D_{\text{cnt,final}} = \alpha \cdot \left(\frac{V_{\text{PV2}}}{I_{\text{PV1}}} - \frac{V_{\text{PV1}}}{I_{\text{PV2}}} \right)$$

where α is a positive constant. The polarity of this expression is mathematically equivalent to the polarity of $\beta \cdot (V_{PV2} \cdot I_{PV2} - V_{PV1} \cdot I_{PV1}) = \beta \cdot (P_{in2} - P_{in1})$, where β is a positive constant.

Therefore, a positive $D_{\text{cnt,final}}$ indicates that the operating point set by D_{in2} yields higher power, and vice versa. This provides the exact information needed for the P&O algorithm.

This scheme eliminates the need for the DCO to generate high frequencies at low V_{PV}. The frequency in each phase is now set by a digital code proportional to D_{in}. Consequently, the IDAC's seed current I_{seed} can be reduced dramatically. This scheme reduces the PDC's power consumption by approximately 30× compared to a straightforward implementation of (3).

B. Adaptive System Power-Scaling Scheme

Maintaining high η_{CONV} at LI and high η_{MPPT} at high HI necessitates that the power consumption of the MPPT controller scales with the input power P_{in}. A fixed-power controller would either dominate system losses at LI or provide insufficient speed and accuracy at HI.

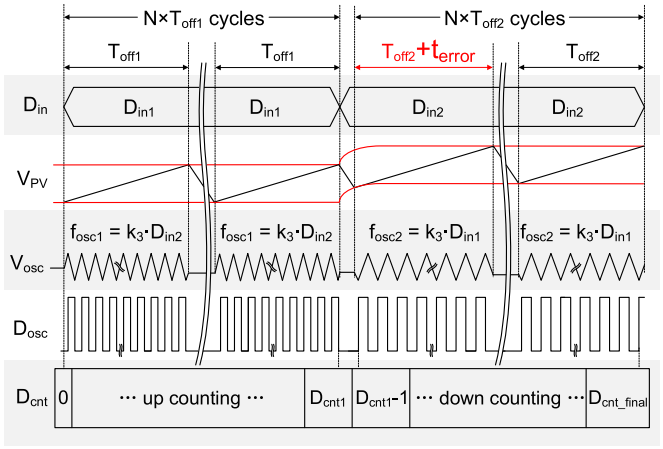


Fig. 5. Proposed multiple-counting technique.

This work implements an adaptive power-scaling scheme that logarithmically divides the input power range into six distinct power regions. The scaling process is fully autonomous, and no external references are needed. The digital output D_{cnt1} from the PDC, obtained via the equivalent power comparison algorithm, serves as the primary indicator for determining the current power region. The underlying control logic is given as follows. If D_{cnt1} is too large, indicating that the DCO oscillation frequency is excessively high relative to the present T_{off} or P_{PV} condition, leading to unnecessary power consumption in the PDC. Consequently, the power-scaling algorithm reduces the system bias current, including the DCO's seed current I_{seed}. Conversely, if D_{cnt1} is too small, the algorithm increases the system bias current to ensure sufficient speed and accuracy. Through this feedback mechanism, D_{cnt1} is regulated to settle within an optimal range for each region, thereby ensuring that the system bias current is precisely tailored to the current input power level. At the end of each measurement cycle, the system uses this D_{cnt1} value to configure the bias currents for most analog circuitry (such as comparators, IDACs, and LDOs) for the subsequent MPPT cycle.

The adaptive power-scaling scheme enables the MPPT controller to operate effectively beyond its native DR. Without scaling, the fixed-bias controller would have a limited DR due to the tradeoff between power consumption and bandwidth. The proposed scheme extends this to 100 000× by autonomously adjusting bias currents to match the instantaneous input power level, effectively "tuning" the controller's performance characteristics across the range.

C. Multiple-Counting Technique

To achieve >98% η_{MPPT}, non-idealities that become significant at the extremes of the DR need to be mitigated. The primary sources of error are comparator noise and RDAC settling error. The low-power DCO makes the oscillation count D_{cnt} susceptible to corruption by thermal noise in the comparator. At high P_{in}, the short T_{off} periods become comparable to the finite settling time of the RDAC when switching V_H and V_L. The hysteresis window settling during T_{off} introduces a significant error in T_{off}, as shown in Fig. 5.

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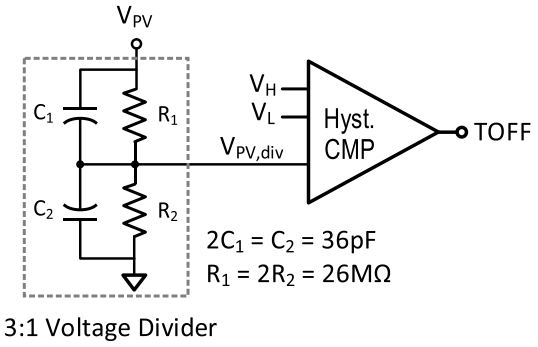


Fig. 6. Block diagram of the hysteretic controller.

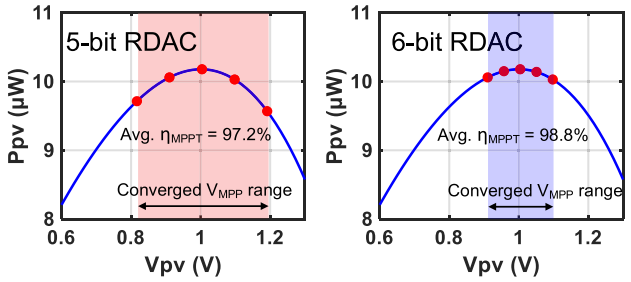


Fig. 7. Simulated converged V_{MPP} range with 6- and 5-bit RDAC.

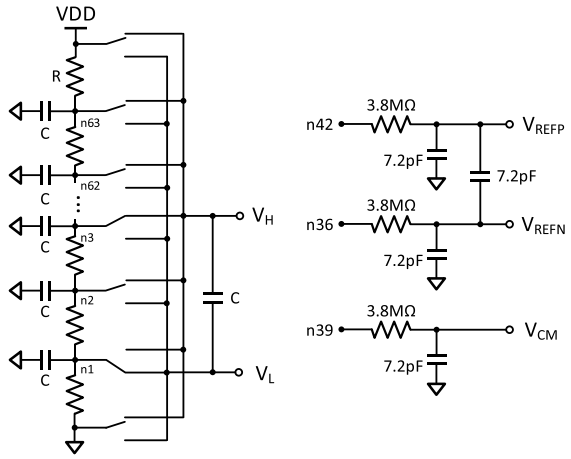


Fig. 8. Simplified schematic of RDAC.

Rather than attempting to reduce the analog settling time, which would require higher bias currents and larger devices, a multiple-counting technique is employed. The system accumulates oscillation counts over a fixed number (N) of consecutive T_{off} periods for each voltage setpoint before computing $D_{\text{cnt,final}}$. The value of N is switched from 4 to 16 when entering the highest power region (>0.1 W). This accumulation increases the effective integration time by a factor of N, reducing the impact of both random noise and systematic settling errors, thus ensuring robust and accurate tracking across the entire DR.

IV. Circuit Implementation

This section details the transistor-level implementation of key building blocks, each designed with specific attention to the stringent requirements of wide DR operation, balancing precision, speed, and power consumption.

A. Hysteretic Controller

The hysteretic controller, which regulates the PV voltage within a programmable window, is architected around two core components: a voltage divider and a hysteresis comparator, as shown in Fig. 6. The voltage divider scales down the high V_{PV} to a level compatible with the comparator's input range. The hysteresis comparator then compares this scaled-down voltage against two programmable reference thresholds, V_H and V_L, which are generated by the RDAC. The output of this comparator directly controls the power switches of the buck–boost converter, maintaining V_{PV} within the hysteresis band, as dictated by the MPPT algorithm.

A capacitive voltage divider scales down the PV voltage V_{PV} for the hysteresis comparator. This topology is chosen because the capacitors not only minimize static power loss but also provide a high-speed AC path, ensuring that the regulated V_{PV} can be rapidly presented to the comparator. High-resistance poly resistors (total 39 MΩ) are connected in parallel with the capacitors to establish the initial DC bias at the internal node. The divider ratio is set to 3:1, which accommodates the comparator's input range while preserving sufficient voltage resolution.

As shown in Fig. 2, the PV voltage V_{PV} under P&O control converges to an oscillation spanning three steady states, covering a total range of 2× the hysteresis window. Note that one hysteresis window in terms of the actual PV voltage corresponds to $3 \cdot V_{HYS} = 3 \cdot (V_H - V_L)$, which also represents 3×4 LSBs of the RDAC. The actual V_{MPP} of the PV cell varies from 1 to 2 V across a 10 μW–1 W power range. To ensure >98% η_{MPPT} at the smallest V_{MPP}, a 6-bit RDAC resolution is selected, as a tradeoff between circuit complexity and voltage quantization error, as shown in Fig. 7. At low input power, this quantization directly governs the steady-state V_{PV} ripple and thus sets a fundamental limit on the achievable MPPT efficiency, as reflected in the measured roll-off at low V_{MPP}.

The RDAC produces the hysteresis window boundaries V_H and V_L for the hysteretic control, and is implemented by a 6-bit resistor ladder, as shown in Fig. 8. In addition, the internal tap voltages of the resistor ladder are utilized to generate other essential reference voltages, including V_{REFP}, V_{REFN}, and the common-mode voltage V_{CM} for the folding comparator within the PDC. The unit resistor is designed with a value of 325 kΩ, striking a balance between the speed required for voltage settling and the need for minimal static power dissipation. To enhance stability and suppress transient glitches during V_H and V_L switching, a decoupling capacitor C of 1.2 pF is integrated at each major internal node of the resistor ladder. This ensures that a stable reference voltage is always presented to the comparators. During MPPT operation, the RDAC code changes by only 1 LSB per tracking step. Simulations indicate a settling time of ~200 ns for such a 1 LSB step. This fixed settling delay becomes a significant fraction of the short T_{off}

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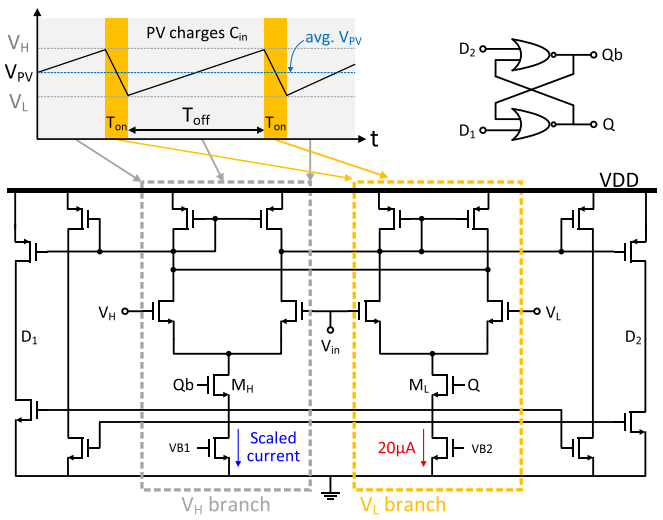


Fig. 9. Simplified schematic of hysteresis comparator.

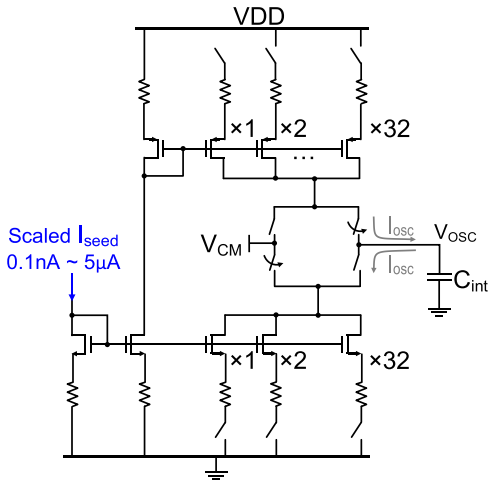


Fig. 10. Simplified schematic of IDAC in PDC.

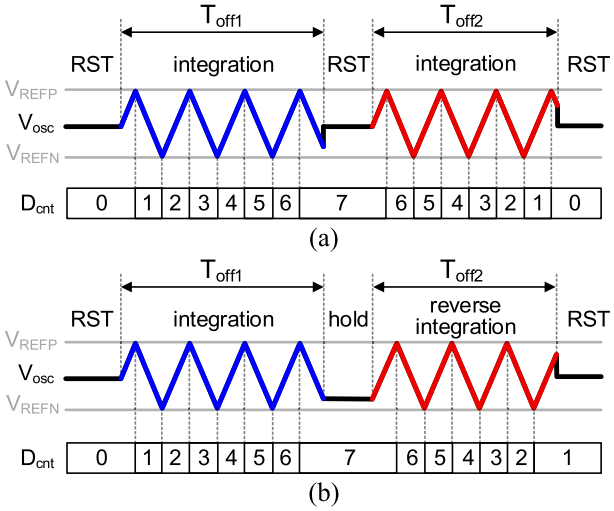


Fig. 11. Simplified waveform of PDC with (a) reset before T_{off2} and (b) hold and reverse integration scheme.

periods at high input power, necessitating the use of multiple-counting (N = 16) to average out the resultant error.

As shown in Fig. 9, the hysteresis comparator is divided into two comparison branches: one compares the upper reference voltage V_H with the input voltage V_{in}, and the other compares the input voltage V_{in} with the lower reference voltage V_L. The branches are switched via transistors M_H and M_L. During the T_{off} period, M_H is turned on, connecting the branch that compares V_H and V_{in}. When V_{PV} reaches V_H, the comparator output toggles and controls the power converter to enter the T_{on} period, where M_L is turned on, connecting the branch that compares V_{in} and V_L. When V_{PV} decreases to V_L, the comparator output toggles again and controls the power converter to enter T_{off}.

Due to the short T_{on} ($\sim$ 1 μs) and the steep slope of V_{PV}, the bias current of the V_L branch is set to 20 μA to ensure sufficient response speed. The T_{off} duration varies with the PV input power (from 1.7 μs to 0.1 s), and the slope of V_{PV} changes accordingly. Therefore, the bias current of the V_H branch also scales with the system's power scaling, ranging from 0.8 nA to 20 μA. Note that although the bias current of the V_L branch remains 20 μA even at 10-μW input power, thanks to the long T_{off} duration, the duty cycle of the V_L branch's averaged current consumption is only 0.5 nA.

B. Power-to-Digital Converter

The PDC serves as the core circuit that physically implements the equivalent power comparison algorithm described in Section III-A. The DCO in PDC generates a clock signal whose frequency is programmed by the digital code D_{in}. It consists of three key components: a programmable IDAC, an integration capacitor C_{int}, and a folding comparator. As shown in Fig. 10, the IDAC charges and discharges C_{int} with a current proportional to D_{in}, generating a linear ramp voltage at the internal node V_{osc}. To mitigate the impact of parasitic and leakage, C_{int} is set to 32 pF.

As shown in Fig. 11(a), if C_{int} is reset after each T_{off} period, the PDC may fail to resolve a difference between the results of T_{off1} and T_{off2}. To address this, a hold and reverse integration scheme is introduced, as depicted in Fig. 11(b), which improves the resolution of the power comparison.

To ensure that all transistors in the IDAC remain in saturation across the 100 000× input power range, the voltage swing of V_{osc} is bounded between V_{REFP} = 656 mV and V_{REFN} = 562 mV. As the input power varies from 10 μW to 1 W, the switching frequency of the power converter ranges f_{sw} from 10 Hz to 600 kHz. To accommodate this wide operating range, the unit bias current of the IDAC is designed to be scalable from 0.1 nA to 5 μA, enabling the DCO oscillation frequency to correspondingly vary from 400 Hz to 27 MHz. With multiple-counting, $4 \cdot f_{osc} > 100 \cdot f_{sw}$, ensuring the PDC to distinguish 1% power difference.

Degeneration resistors are employed in the IDAC to enhance current linearity and reduce noise under HI conditions, where precision is critical due to the short T_{off}. Although the effectiveness of degeneration diminishes under LI conditions as bias currents decrease, the linearity and noise requirements for

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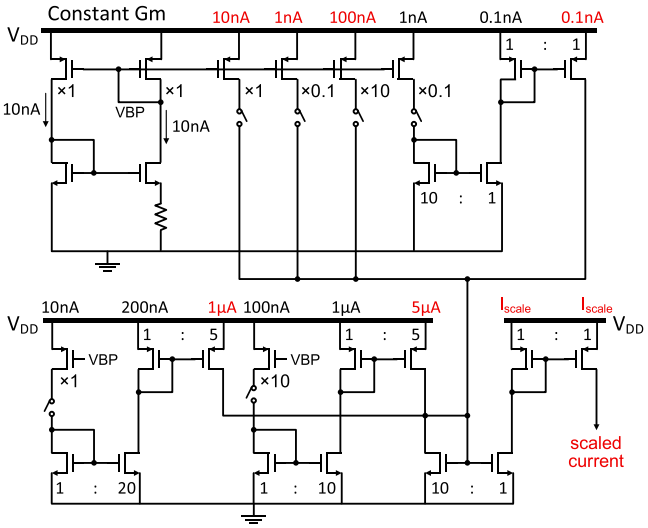


Fig. 12. Simplified schematic of bias generator.

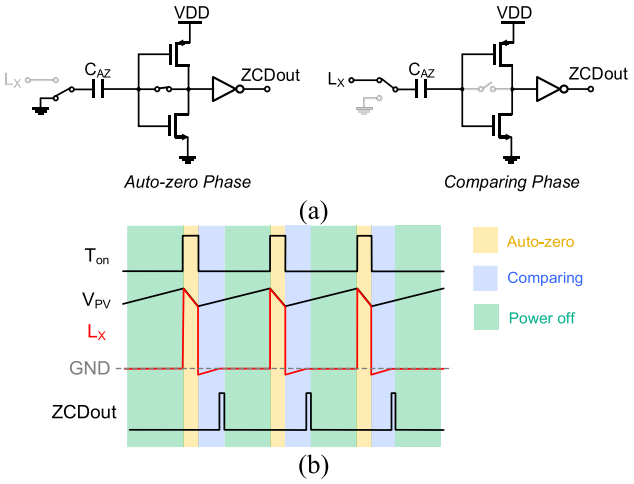


Fig. 13. Auto-zero inverter-based ZCD. (a) Simplified schematic and (b) timing diagram.

the IDAC are concurrently relaxed owing to the significantly longer T_{off}.

The folding comparator adopts the similar topology as the hysteresis comparator in Fig. 9. In contrast, the folding comparator utilizes a single, power-scalable tail current that is shared by both comparison paths. It continuously compares V_{osc} against two fixed internal thresholds (V_{REFP} and V_{REFN}). Each time V_{osc} crosses a threshold, the comparator toggles its output and reverses the ramp, thereby generating a triangle wave whose frequency f_{osc} is directly proportional to the IDAC current and hence to the input digital code. This structure achieves the required $f_{osc} \propto D_{in}$ relationship in a power-efficient manner. The IDAC's reference current I_{seed} and the folding comparator's tail current I_b are autonomously adjusted by the power-scaling scheme, ensuring that the circuit meets the required speed specifications across different power regions while consistently operating at the minimum necessary power consumption.

The upcounter/downcounter performs the integration and comparison of the power samples (Fig. 3). The final value $D_{cnt,final}$ is directly equivalent to the result of (4) in Section III-A. Its sign bit determines the subsequent action of the MPPT state machine, steering the hysteretic control voltage in the correct direction to search for the maximum power point.

C. Bias Generator

A conventional constant-g_m bias generator [24] serves as the core reference for the entire system, as shown in Fig. 12, producing a stable 10-nA reference current across PVT variations. This reference current is subsequently mirrored and scaled to establish six distinct system bias current levels that support the adaptive power-scaling scheme: 0.1 nA, 1 nA, 10 nA, 100 nA, 1 μA, and 5 μA. Each level corresponds to one of the six logarithmic power regions, enabling the analog circuitry, including the comparators, IDACs, and the oscillator in the PDC, to operate at the minimum power necessary to meet the speed and noise requirements at a given input power. The bias distribution network employs digitally controlled current mirrors to select the appropriate bias level based on D_{cnt1}, ensuring optimal efficiency across the 100 000× DR.

The maximum current level of 5 μA is determined by the need to keep all transistors in the comparators' input pairs in the saturation region across all six bias levels. The transistor sizes are optimized for matching and layout symmetry, making it impractical to resize for higher currents. Post-layout simulations confirm that the 5-μA current is the upper limit for maintaining saturation with the chosen sizes.

This scaling sequence results in a 2× reduction in the maximum achievable f_{osc} compared to a hypothetical 10× step to 10 μA. This limits the maximum f_{osc} to ~27 MHz, an intentional "underdesign" in analog bandwidth that is compensated digitally by extending the multiple-counting technique to 16× from 4×, effectively trading digital integration time for analog power and speed.

D. ZCD Circuit

The ZCD employs an auto-zeroed inverter-based comparator [25], as shown in Fig. 13. During T_{on}, the inverter's offset and flicker noise are stored on a capacitor C_{AZ}. During T_{off}, the comparator is enabled to detect the zero-crossing of the inductor current through the voltage at the node L_X. The inverter is immediately powered down after detection until the next cycle. This duty-cycled operation, combined with auto-zeroing, results in an average power consumption of only 8 nW in the lowest power region.

E. System LDO

An on-chip LDO [26] is implemented to provide a clean and stable supply for both analog and digital circuits. As shown in Fig. 14, the LDO powered by the output battery voltage (V_{OUT} = 1.5 ~ 3.3 V) is designed to deliver a regulated output of 1 V and remains stable under all load conditions. To minimize quiescent power consumption, the LDO's bias current is also made scalable. It is dynamically adjusted by the system's power-scaling controller, ensuring optimal balance

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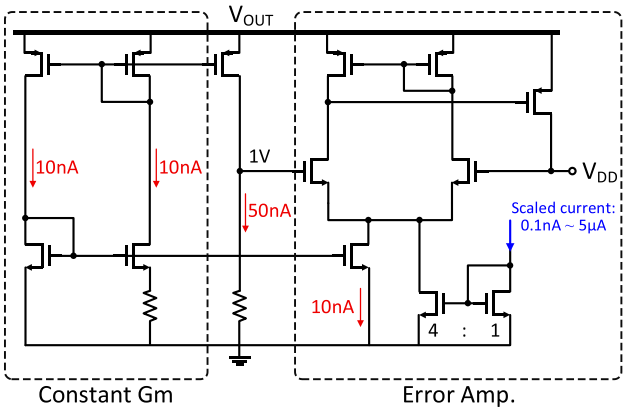


Fig. 14. Simplified schematic of LDO.

between transient response and quiescent current at different operating points.

F. Power Stage

As shown in Fig. 1, the buck–boost converter integrates four power switches: two PMOS transistors (S_1 and S_4) serving as the high-side switches and two NMOS transistors (S_2 and S_3) as the low-side switches. The gate drivers for S_1 and S_2 are powered from the input voltage V_{PV}, while those for S_3 and S_4 are driven from the output voltage V_{OUT}. This configuration ensures robust switching operation without requiring additional voltage supplies. To minimize conduction loss and maintain high-power conversion efficiency across the wide DR, all switches are optimized for low ON-resistance. Under the minimum available gate drive voltages, V_{PV} = 1 V and V_{OUT} = 1.5 V, S_1 and S_2 achieve an ON-resistance of approximately 50 mΩ, and S_3 and S_4 achieve about 30 mΩ.

G. Power-Scaling Simulation

The power converter operates in PFM mode, which intrinsically supports power scalability. As the input power increases, the switching frequency rises accordingly, leading to a natural scaling of both switching and conduction losses with the power level. This inherent loss behavior, combined with the proposed adaptive power-scalable MPPT control, establishes a fully power-scalable energy-harvesting system capable of sustaining high efficiency over the 100 000× input power range.

Fig. 15 shows the simulated power consumption of the MPPT controller versus P_{in}. To ensure stability during bias current switching, hysteresis is incorporated into the region-switching logic, preventing chattering or dead loops caused by circuit settling errors during system bias current switching.

As the simulated power loss breakdown in Fig. 16 illustrates, this scheme ensures that the controller's overhead power is minimized across the entire DR. Notably, even with the power-scaling scheme active, the MPPT controller's power consumption remains the dominant portion of the total system loss at low P_{in}, yet it becomes negligible at high P_{in}, validating the effectiveness of the proposed approach.

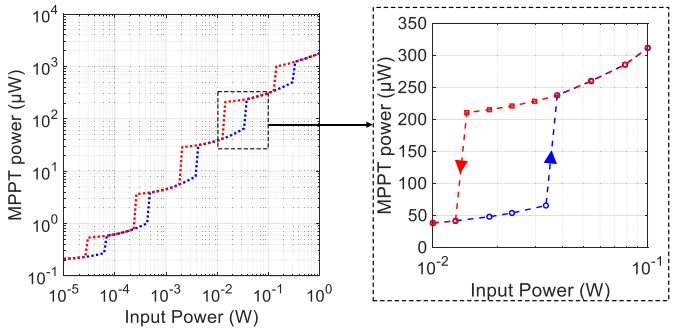


Fig. 15. Simulated MPPT power versus input power.

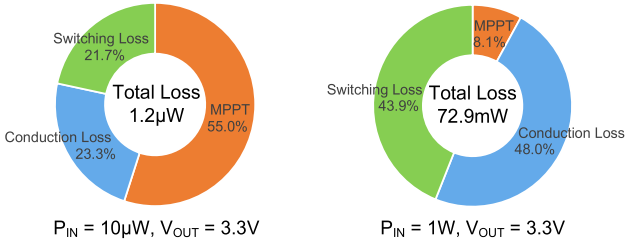


Fig. 16. Simulated power loss at different input power levels.

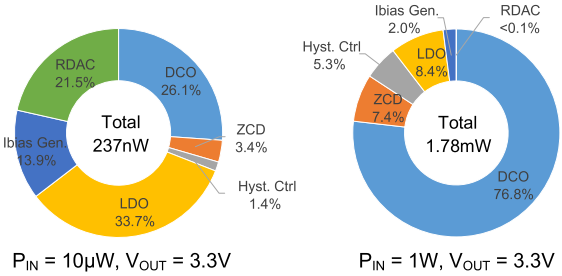


Fig. 17. Simulated MPPT power distribution at different input power levels.

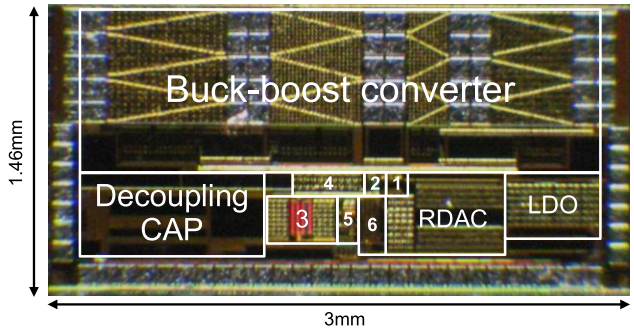
A detailed power breakdown is shown in Fig. 17. It should be noted that the MPPT circuit power consumption does not scale linearly with the bias current. Apart from some blocks, such as bias generators and RDAC, whose power cannot be easily scaled, the power consumption of comparators also depends on the system switching frequency. Specifically, for input power < 100 μW, the current consumption of the MPPT circuit is dominated by the LDO biasing circuit, bias generator, and RDAC, while the power consumption of other analog blocks is negligible thanks to power scaling. At 1 W, the DCO power dominates due to the short T_{off}, which requires the DCO folding comparators to deliver high bandwidth and low noise to ensure high MPPT efficiency.

H. Stability Summary

The wide-dynamic-range operation with adaptive power scaling introduces specific stability considerations.

To prevent chattering or unstable oscillations when the input power drifts near a region boundary, the power-scaling controller employs digital hysteresis in its region-switching logic. This ensures that a transition occurs only when the

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1. ZCD
2. Hysteresis control
3. DCO
4. Input voltage divider
5. Ibias generator
6. Synthesized digital block (MPPT algorithm)

Fig. 18. Die micrograph.

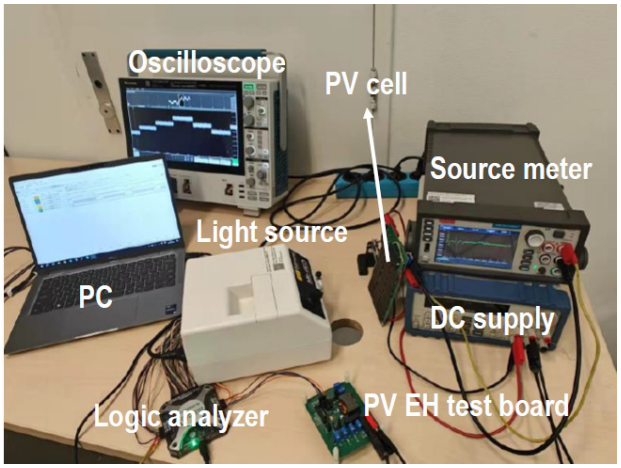


Fig. 19. Test setup.

power indicator D_{cnt1} exceeds (or falls below) the threshold, providing a stable transition between bias current levels.

The P&O algorithm is guaranteed to converge stably under the condition that the voltage-perturbation step is sufficiently small relative to the PV panel's *PV* curve. In this design, the perturbation step is fixed at 1 LSB of the 6-bit RDAC, which meets this condition across the entire input power range.

The system employs a self-starting constant-g_m bias generator that initializes reliably from the battery voltage V_{OUT}.

In summary, the architecture is designed to maintain stability. The following measurement results demonstrate that these measures are effective in practice.

V. Measurement Results

The proposed PV energy harvester was fabricated in a standard 180-nm CMOS process. A die micrograph is shown in Fig. 18, occupying a total area of 4.38 mm^2 (3×1.46 mm). Fig. 19 shows the test setup, the light source is manually adjusted, and a commercial PV cell (KXOB25-05 $\times$ 3F) with a total surface area of 80 cm^2 was used to provide precisely controlled input power spanning from 10 μW to 1 W, enabling comprehensive evaluation across the entire target DR.

Fig. 20 shows the measured transient waveforms of V_H, V_L, and V_{PV}. As observed, the switching frequency of the power converter adapts to the irradiation level, and the system successfully hunts for and settles near the new maximum power point (V_{MPP}) following an irradiation change. The small steady-state oscillation aroundV_{MPP} is inherent to the P&O algorithm and confirms its proper operation.

The measured power conversion efficiency (η_{CONV}) and MPPT efficiency (η_{MPPT}) are plotted in Figs. 21 and 22,

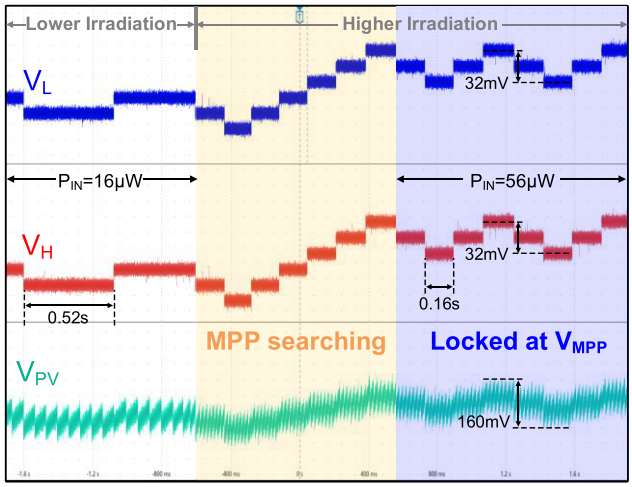


Fig. 20. Measured transient waveform with irradiation changing.

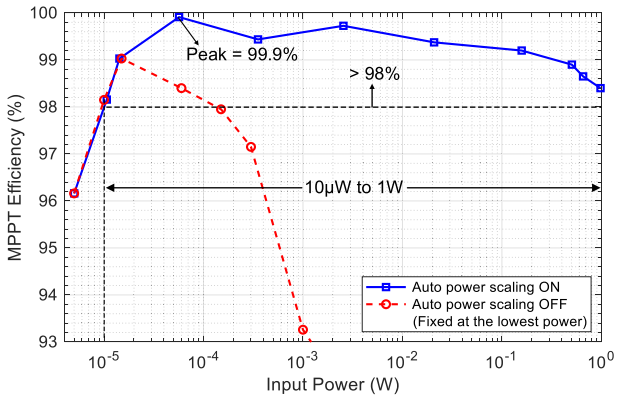


Fig. 21. Measured MPPT efficiency.

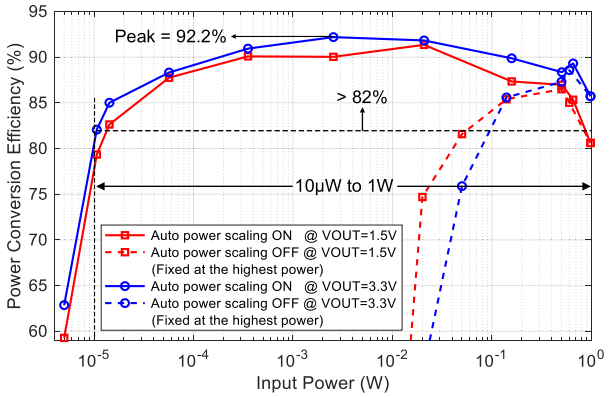


Fig. 22. Measured power conversion efficiency.

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TABLE I
COMPARISON WITH THE STATE OF THE ARTS

	TPEL'21 [10]	JSSC'21 [4]	TCAS-II'22 [13]	SSCL'22 [28]	VLSI'22 [12]	JSSC'24 [27]	**This Work**
Process	180nm	350nm	180nm	180nm	180nm	180nm	180nm
Power Stage	Boost	Boost	Boost	Buck-Boost	Buck-Boost	Boost	Buck-Boost
C_{IN}	–	10µF	20µF	–	10µF	10µF	10µF
L	47µF	10µH	82µH	10µH	10µH	–	10µH
MPPT Type	P&O	FOCV + P&O	P&O	P&O	FOCV	P&O	P&O
Using LUT	No	Yes	Yes	No	Yes	No	No
Continous MPPT	Yes	No	Yes	Yes	No	No	Yes
V_{IN} (V)	0.6–1.15	0.5– 2.4	0.2–1.5	0.2–1.5	1– 5.2	0.15–1.8	1–3
V_{OUT} (V)	1.2–1.8	3.5	3.3	0.6–1.8	3.5	2.2, 3	1.5–3.3
Peak η_{MPPT}	99.3%	99.9%	–	95%	99%	99.5%	99.9%
Peak η_{CONV}	94.7%	92.6%	93.6%	87%	96.5%	88%	92%
P_{IN} Range for η_{MPPT} > 98%	0.6mW–5.4mW* **(9×)**	4mW–0.9W* **(225×)**	–	N.A.	150µW–1.5W* **(10,000×)**	2mW–10mW* **(5×)**	10µW–1W **(100,000×)**
P_{IN} Range for η_{CONV} > 85%	0.85mW–5.4mW* **(6×)**	40mW–835mW* **(21×)**	0.5µW–50mW* **(100,000×)**	4mW–10mW* **(2.5×)**	1.5mW–1.5W* **(1,000×)**	9mW–50mW* **(5.6×)**	14µW–1W **(71,400×)** **@V_{OUT}=3.3V**

* Estimated from data/graph

respectively. The harvester achieves a peak η_{CONV} of 92%, maintaining efficiency above 82% across the entire 100 000× DR. Simultaneously, it reaches a peak η_{MPPT} of 99.9%, remaining above 98% over the same DR.

A comprehensive performance comparison with recent state-of-the-art energy harvesters is summarized in Table I. This work eliminates the need for periodic energy-harvesting interruption and LUTs, enhancing robustness against PVT variations. The proposed design achieves a 10× wider DR for >98%η_{MPPT} compared to prior arts, and a 444× wider DR among P&O-based implementations while maintaining highly competitive peak efficiencies. Furthermore, it sustains >82% power conversion efficiency (with a peak of 92%) across the entire operating range.

VI. CONCLUSION

This article presents a digital-intensive PVEH system that achieves both high η_{MPPT} and η_{CONV} across a wide input power DR, employing a direct input PDC and an adaptive power-scalable MPPT scheme without any external references such as an LUT. The proposed PVEH achieves >98% η_{MPPT} across a 100 000× DR, as well as a competitive η_{CONV} of >82% across the same DR.

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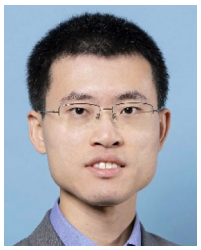
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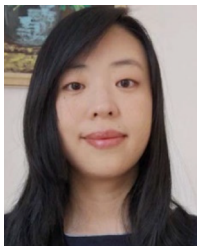
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