A 0.25mm^2 Resistor-Based Temperature Sensor with an Inaccuracy of 0.12°C (3σ) from -55°C to 125°C and a Resolution FOM of 32fJK^2

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19.2 A 0.25mm² Resistor-Based Temperature Sensor with an Inaccuracy of 0.12°C (3σ) from -55°C to 125°C and a Resolution FOM of 32fJ·K²

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Temperature sensors based on Wheatstone bridges, e.g. [1,2], have recently achieved higher resolution and greater energy efficiency than conventional BJT-based sensors [3]. However, this comes at the expense of area, making them less attractive in industrial applications. This paper presents a Wheatstone-bridge sensor that uses a zoom-ADC architecture to reduce area (by 3× over [2]) and achieve state-of-the-art energy-efficiency for an integrated temperature sensor. After a 1st-order fit and a systematic non-linearity correction [2,4], it also achieves state-of-the-art inaccuracy: 0.12°C (3σ) over the full military temperature range (–55°C to 125°C).

An energy-efficient way of reading out a Wheatstone bridge (WhB) is by directly connecting it to the virtual ground established by the 1st integrator of a single-bit continuous-time delta-sigma modulator (CTΔΣM) [1,2]. A single-ended model of this system is shown in Fig. 19.2.1 (left). For maximum sensitivity, the chosen bridge resistors R_p and R_n have positive and negative temperature coefficients, respectively. The modulator's single-bit DAC consists of a resistor R_{DAC} that can be connected either to V_{DD} or GND depending on the bitstream state. The resulting current I_{DAC} compensates for the bridge output current I_{sig} such that the average error current (I_{err}) flowing into the modulator's 1st integrator is zero. As the operating range of the sensor increases, however, the magnitudes of I_{sig} and I_{err} both increase. A large integration capacitor C_{int} (180pF in [2]) is then required to constrain the swing of the 1st integrator.

As shown in Fig. 19.2.1 (right), using a multibit DAC decreases the magnitude of I_{err}, and thus the required size of C_{int}. As a further advantage, the current consumption of the active integrator can also be reduced, thus improving the energy efficiency of the sensor. Due to their relatively large temperature sensitivity and low voltage dependency, a silicided p-poly (s-p-poly) resistor R_p and a non-silicided n-poly resistor R_n are used in the WhB. Their values, R_p = 100kΩ and R_n = 80kΩ, are chosen to restrict $|I_{sig}|$ to < 7μA over PVT. In a compromise between DAC area and that of C_{int}, a 3b DAC made from non-silicided n-poly elements (R_{DAC}= 960kΩ) was chosen.

To further reduce area, the CTΔΣM was realized as a 2nd-order zoom-ADC, since this only requires a single comparator to drive a multibit DAC, as shown in Fig. 19.2.2. The ADC digitizes the ratio $X = I_{sig}/(2I_{DAC})$ (full range from –4 to 4) in two steps. First, a coarse 3b SAR conversion determines the integer part n of X. During this phase, the loop filter is used as a preamplifier by resetting its capacitors before each bit conversion. The fractional part μ is then determined by a single-bit 2nd-order incremental conversion, using reference currents of $(n-1)\cdot 2I_{DAC}$ and $(n+1)\cdot 2I_{DAC}$ to achieve over-ranging and absorb coarse-conversion errors [5].

The 2nd-order CTΔΣM employs a feedforward architecture, with a compensating zero realized by including R_{ff} in the feedback path of the 2nd integrator. Since I_{err} is now quite small, the 1st integrator is based on an energy-efficient current-reuse OTA, rather than the two-stage opamps used in [1,2]. It achieves 80dB gain over PVT, and uses high-V_T transistors to achieve good output swing (~0.9Vpp) [6], as shown in Fig. 19.2.3 (top left). Pole-zero compensation is implemented by inserting $R_{com} \approx 1/g_m$ in series with C_{int}, which improves the stability of the modulator. As in [2], the OTA is chopped at the sampling frequency (fs = 500kHz) to suppress its offset and 1/f noise of the 1st integrator. From simulations, the OTA dissipates 22μW at room temperature (RT), which is ~60% of the sensor's total power. In order to accommodate the swing of the 1st integrator, the 2nd integrator is based on a source-degenerated telescopic OTA, which consumes only 3μW.

Non-linearity is a key challenge for multibit ADCs. For the proposed zoom-ADC, the two major contributors are R_{DAC} mismatch and the non-linearity of the1st-integrator. Although the former can be mitigated by dynamic element matching (DEM), e.g. data-weighted averaging (DWA), dealing with the latter is more challenging. It is caused by the nonlinear variation of the input impedance ($\sim 1/g_m$) of the 1st integrator with I_{DAC}, and leads to step errors of ~0.1°C at coarse code transitions (Fig. 19.2.3, top right). However, the use of over-ranging means that, in principle, the same ADC result can be obtained from either of two adjacent coarse codes, e.g. *n* and *n+1*. Noting that the resulting errors then have opposite polarity, improved linearity can be achieved by segment averaging, i.e. averaging the result of two conversions centered on adjacent coarse codes (Fig. 19.2.3, bottom right). Although a 2nd-order modulator will remain stable over its full DAC range for DC signals, its quantization noise will increase rapidly at the extremes. To avoid this, the second conversion is only based on an adjacent coarse code if the expected result lies within 95% of the DAC's range. From simulations, the residual non-linearity is then less than 0.02°C, which is well below the measured inaccuracy of the sensor.

The prototype sensor is realized in a 0.18μm CMOS process (Fig. 19.2.7). It consumes 52μA from a 1.8V supply, and occupies 0.25mm². About 45% of the area is occupied by the WhB and the DAC, and about 30% by the capacitors (2×45pF) of the 1st integrator. For flexibility, the DWA and SAR logic were implemented off-chip. Simulations show that an on-chip realization would dissipate only 0.7μW and occupy 0.005mm².

19 samples from one wafer were mounted in ceramic DIL packages and characterized in a temperature-controlled oven. To minimize temperature drift during the measurements, the sensors were mounted in good thermal contact with a large aluminum block. After segment averaging, the sensor output vs. temperature is shown in Fig. 19.2.4 (left). After a 1st-order fit and a systematic non-linearity correction [2,4], the sensor achieves an inaccuracy of 0.12°C (3σ), from –55°C to 125°C, as shown in Fig. 19.2.4 (bottom right). Without segment averaging, the step errors due to OTA non-linearity can be clearly seen (Fig. 19.2.4, top right).

FFTs of the sensor's bit-stream outputs are shown in Fig. 19.2.5 (top) for different types of DEM. Although barrel-shifting DEM is simpler than data-weighted averaging (DWA), it elevates the sensor's noise floor. With DWA, the sensor achieves a thermal-noise-limited resolution of 260μK_{rms} in a 5ms conversion time (Fig. 19.2.5, bottom). This is not affected by segment averaging (2.5ms/segment). Furthermore, the use of a multibit DAC makes the sensor fairly robust to clock jitter: simulation shows that 40ps (rms) jitter corresponds to only a 5% increase in thermal noise power. The sensor's 1/f noise (10Hz corner frequency) is mainly due to the n-poly resistors used in the WhB and DAC [4]. At RT, the sensor achieves a supply sensitivity of 0.02°C/V from 1.6 to 2V.

In Fig. 19.2.6, the performance of the proposed temperature sensor is summarized and compared with other energy-efficient sensors. It is 3× smaller than [2], and achieves higher energy efficiency. In fact, its resolution FOM (32fJ·K²) is even lower than that of a recent MEMS-based sensor [7]. Notably, for a resistor-based sensor, it is also capable of operating over the full military temperature range (–55°C to 125°C). Over this range it achieves a similar relative inaccuracy as [2], which, however, only operates over the industrial temperature range (–40°C to 85°C).

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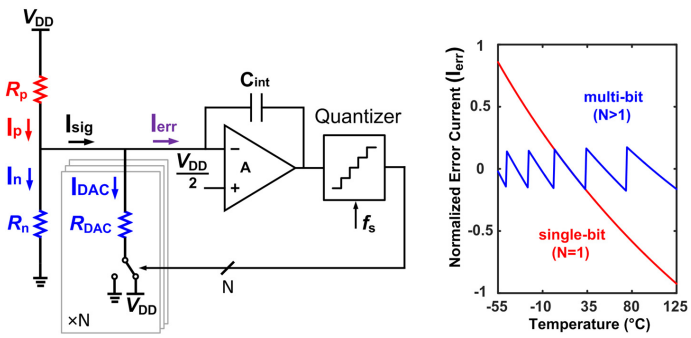

Figure 19.2.1: ΔΣ readout of a Wheatstone-bridge temperature sensor (left), error current I_{err} over temperature (right).

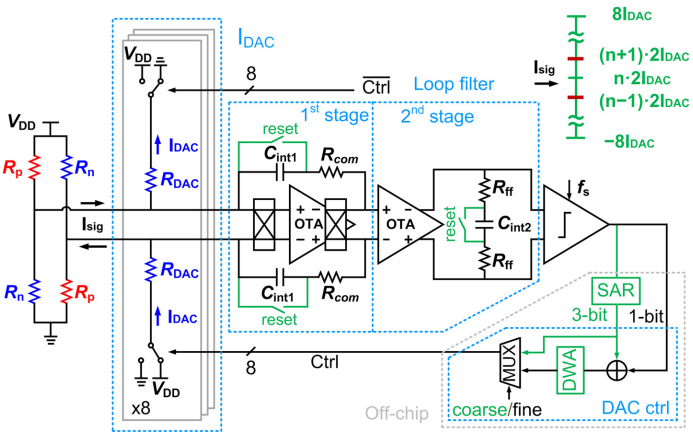

Figure 19.2.2: System block diagram of the proposed sensor.

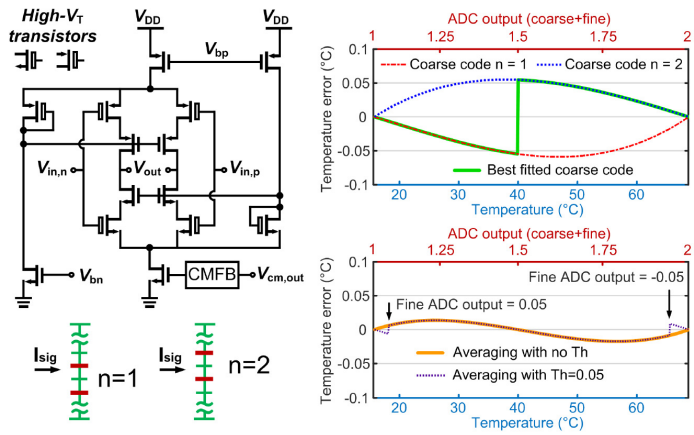

Figure 19.2.3: Current-reuse OTA (top left), zoom-ADC levels (bottom left), simulated error due to OTA non-linearity (top right), and after segment averaging (bottom right).

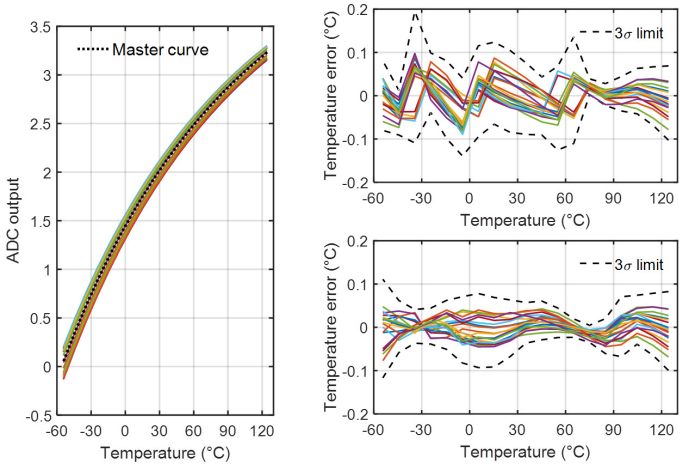

Figure 19.2.4: Sensor characteristic (left), temperature error after a 1st-order fit and fixed non-linearity correction, without and with segment averaging (top & bottom right).

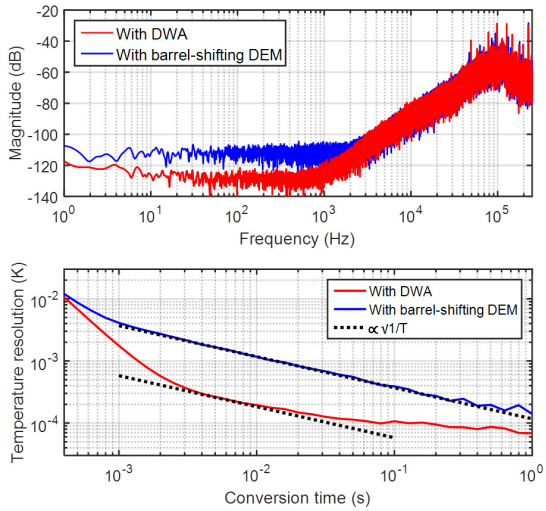

Figure 19.2.5: PSD of the sensor output bitstream (top), resolution vs. time plot (bottom).

	This work	[7]	[2]	[4]	[1]	[6]
Sensor type	**Resistor WhB**	Dual-MEMS Resonator	Resistor WB	Resistor WhB	Resistor WhB	BJT
CMOS Technology	**0.18µm**	0.18µm	0.18µm	0.18µm	0.18µm	0.16µm
Area [mm2]	**0.25**	0.54	0.72	0.72	0.43	0.16
Temperature range	**-55°C to 125°C**	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 125°C	-70°C to 125°C
3σ inaccuracy [°C] (Trimming points)	**0.12 (2[a])**	--	0.07 (2[a])	0.1 (2[a])	0.4 (2[b])	0.06 (1)
Power consumption [µW]	**94**	13000	160	180	65	7
Conversion time [ms]	**5**	5	5	10	0.1	5
Resolution [mK]	**0.26**	0.02	0.41	0.16	10	15
Resolution FOM [fJ·K²][c]	**32**	40[d]	130	49	650	7300

[a] 1st-order fit. [b] 1-point trim with 1st-order fit, min-max.
[c] Energy / Conversion × (Resolution)². [d] MEMS die + CMOS readout IC.

Figure 19.2.6: Performance summary and comparison with previous work.

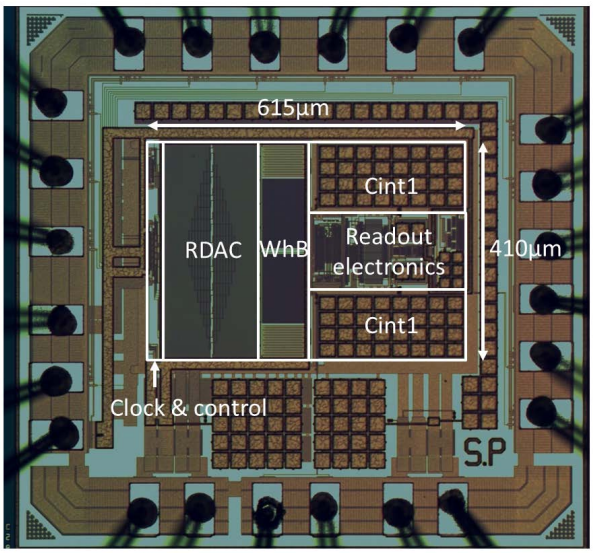

Figure 19.2.7: Die micrograph of the fabricated temperature sensor.

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