"Single-Pin" Integrated Crystal Oscillators

ERNST H. NORDHOLT AND CORLEX A. M. BOON

Abstract — **Oscillator configurations for integrated circuit (IC) applications where the quartz resonator can be connected between one pin of the IC and ground are presented. Excellent performance and good designability are obtained by applying negative feedback around a high-gain amplifier circuit and by including a symmetrical limiter in the feedback loop. The feedback mechanism provides an inherent buffering against load variations. Implementation examples in bipolar technology are discussed. A simple model for the negative impedance at the crystal port reveals the methods for avoiding parasitic oscillations due to the shunt capacitance of the crystal. The performance of a semicustom integrated oscillator with a simple structure is simulated and measured. In this oscillator a novel start-up technique is employed that ensures a stable and reliable start-up behavior.**

I. Introduction

THE increasing complexity of integrated circuits (IC's) together with the wish to restrict the number of pins and peripheral devices to a minimum has stimulated the demand for oscillators where the quartz resonator can be connected between a single pin of the IC and ground. The single-pin technique introduces the risk of undesired oscillator signal injection elsewhere in the IC because the crystal current may cause voltage drops across the internal ground connection in the IC before it is returned to the ground pin. When used in sensitive systems, a careful layout is therefore required.

This paper presents a systematic and hierarchical approach to the design of reliable, stable and accurate single-pin crystal oscillators for IC applications. This design approach is based on the simultaneous application of both positive and negative feedback loops around a high-gain amplifier circuit. The feedback mechanism yields a well-defined value of the negative input resistance at the resonator port and provides an inherent buffering action against load variations, parameter variations in active devices and supply voltage variations.

It will be shown that four fundamentally different basic configurations exist. In these configurations, various methods can be used for defining the amplitude of the output signal. A very simple technique is introduced here using a symmetrical voltage or current limiter in the feedback network. Though this technique may give some degradation in noise performance, it highly favors the designability.

Manuscript received February 28, 1989; revised March 3, 1989. This paper was recommended by Associate Editor C.A.T. Salama.

The authors are with the Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands.

IEEE Log Number 8932875.

One oscillator type which has been integrated on a semicustom 400-MHz bipolar array will be discussed in some detail including the methods that can be used for avoiding overtone oscillations and parasitic oscillations due to the shunt capacitance of the crystal. Moreover, a new technique is presented for obtaining a reliable start-up behavior even in the case of drive-level dependent series resistances in the crystal.

II. Basic Configurations for Single-Pin Crystal Oscillators

The realization of a well-defined negative resistance that compensates for the losses in a quartz resonator requires the application of both a negative and a positive feedback loop around a high-gain amplifier circuit. For finding suitable negative-resistance configurations we will model the high-gain amplifier circuit as a nullor, similar to negative-feedback amplifier modeling [1]. The transfer properties of a nullor are characterized by a transmission matrix with value zero:

$$U_i = 0, I_i = 0.$$

The symbol used for the nullor is shown in Fig. 1.

A different method to express these properties is in terms of transfer parameters, being the reciprocals of the transmission parameters A, B, C, and D. These transfer parameters are defined as follows.

voltage-gain factor: $\mu = 1/A = (U_o/U_i)I_o = 0$

transadmittance: $\gamma = 1/B = (I_o/U_i)U_o = 0$

transimpedance: $\zeta = 1/C = (U_o/I_i)I_o = 0$

current-gain factor: $\alpha = 1/D = (I_o/I_i)U_o = 0.$

One can think of a nullor as an ideal op. amp. with both floating input and floating output ports (operational floating amplifier, OFA) [2]. All transfer parameters are infinite. By using dual-loop feedback around a nullor two out of the four transmission parameters of a feedback amplifier can be accurately fixed, the other two remain zero.

The input or output impedance of the amplifier configurations with two feedback loops can be determined accurately by the elements in the feedback network. In general the input and output impedance of two-ports in terms of

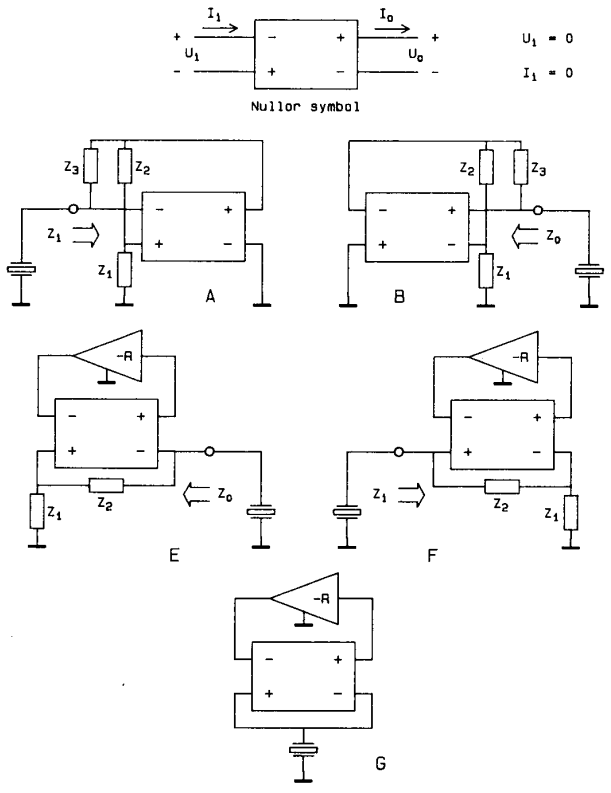


Fig. 1. Basic configurations for single-pin crystal oscillators.

TABLE I
TRANSMISSION PARAMETERS OF DUAL FEEDBACK LOOP CONFIGURATIONS

Configuration	Transmission Parameters				Z_i	Z_o
A	A	0	C	0	A/C	0
B	0	0	C	D	0	D/C
C	A	0	0	D	AZ_l/D	DZ_s/A
D	0	B	C	0	B/CZ_l	B/CZ_s
E	A	B	0	0	∞	B/A
F	0	B	0	D	B/D	∞

the transmission parameters can be written as

$$Z_i = \frac{AZ_\ell + B}{CZ_\ell + D}; \quad Z_o = \frac{B + DZ_s}{A + CZ_s}$$

where Z_ℓ and Z_s are the load and the source impedance, respectively. Making an inventory of all possible combinations with two feedback loops, we find six configurations. Table I gives their properties.

In order to realize the negative resistances dependent exclusively on the transmission parameters of the configuration, we can use configurations $A, B, E,$ and F. One of the transmission parameters will be negative and the other positive.

Since for optimum accuracy the crystal should be used at its series resonance, a voltage should be forced to it and its current should be sensed and amplified. This requires negative shunt feedback at the port where the quartz resonator is to be connected. A positive-feedback in series with this port then realizes the required open stable, negative resistance.

For practical reasons only feedback networks with impedances and active devices will be considered. It should be noted that theoretically the best performance can be realized by employing non-energic feedback networks, similar to negative feedback amplifiers.

Fig. 1 shows the four basic configurations with a one-side grounded crystal that meet the above mentioned requirements. Two configurations need an inverting transimpedance in one loop in order to realize the required positive feedback. Only in the first configuration the output of the nullor is grounded at one side. This means that a one-side grounded load can be connected in either parallel or series with these output terminals without any influence on the oscillation conditions. When practical amplifier circuits are used instead of the nullor, an inherent buffering is obtained. The other configurations do not have this property. The buffering action can be only obtained for floating loads.

A fifth configuration G can be derived from both configurations E and F. The negative feedback loop that fixes the voltage-gain and the current-gain factors, respectively, is replaced by a unity feedback loop, thereby converting—depending on the initial point of view—either of these factors to unity.

III. AMPLITUDE STABILIZATION

One method to fix the amplitude in an oscillator is the use of an averaging automatic-gain control (AGC). The realization of such an AGC, however, requires an amplitude measurement and the design of a low-pass filter in such a way that bouncing effects are avoided. Although excellent phase-noise properties can be obtained in such a "linear" oscillator, this method is not very attractive for IC applications.

The next best solution uses a memoryless symmetrical nonlinear device in one of the branches of the feedback network. The absence of memory effects is desirable for avoiding amplitude dependent time delays in the oscillator loop and thus for generating an accurate frequency. Limiter symmetry is desirable since it causes noise aliasing only from frequency bands near to the odd harmonics and not from dc and even harmonics. By making the negative resistance magnitude not much larger than necessary for sustaining oscillations under worst-case conditions, the noise aliasing can be kept acceptable.

The reason why oscillators, according to this concept, can offer such a good performance is that the amplifier circuit can operate in its linear region. This means that the crystal is always terminated with a well-controlled impedance in contrast to oscillators where the amplitude limiting is determined in the amplifier circuit itself.

Fig. 2 shows some one- and two-port implementations of symmetrical nonlinearities together with their transfer functions. The memory effects can be kept reasonably small for example by using Schottky diodes. These limiter circuits can be used in one of the branches of the feedback

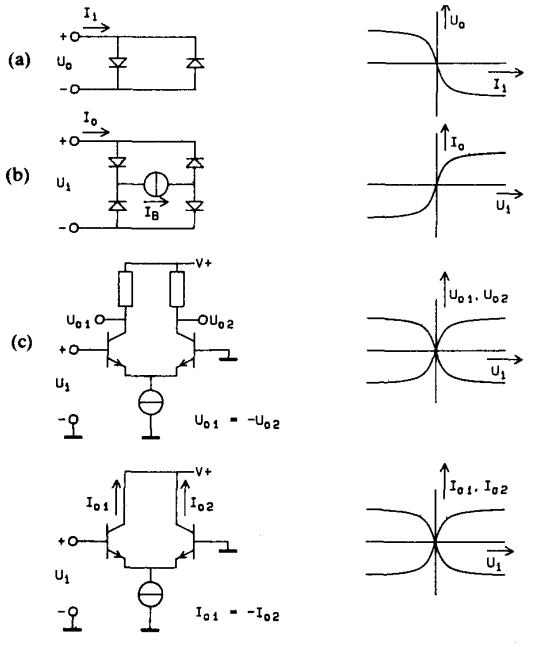


Fig. 2. Implementation examples of one- and two-port limiters for oscillators (a) One-port voltage limiter. (b) One-port current limiter. (c) Two-port voltage limiter. (d) Two-port current limiter.

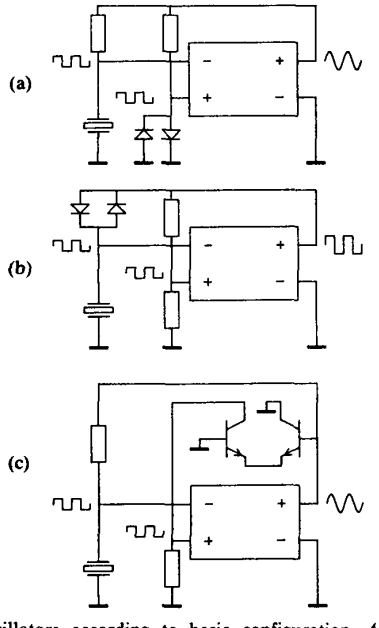


Fig. 3. Oscillators according to basic configuration *A* with various types of limiters.

network dependent on the type of output signal required for optimally driving a load in a certain application. Either sinewave or square-wave voltages or currents may be obtained. As an example, Fig. 3 shows where these limiter types can be inserted in the basic oscillator configuration *A*.

The above considerations deal with the first steps in the selection of a suitable oscillator configuration and form

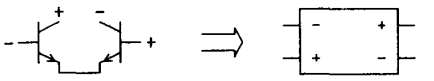


Fig. 4. Differential pair as a simple approximation of the nullor.

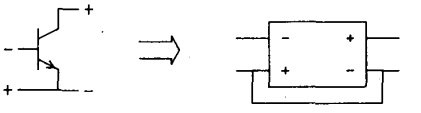


Fig. 5. Single transistor as an approximation of a nullor with two common terminals.

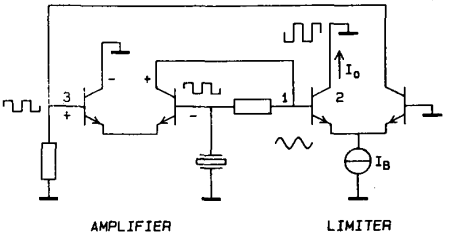


Fig. 6. Basic implementation of an oscillator according to configuration *A* with a two-port current limiter in the positive feedback path.

the basis for actual circuit design, no matter what kind of implementation technology is available. In the next section we will present some implementation examples of single-pin crystal oscillators in bipolar technology. Implementations in technologies like CMOS and BIMOS would basically realize the same functions but might look very different.

IV. Basic Oscillator Implementation in Bipolar Technology

In the implementation of high-performance oscillators the use of lateral p-n-p transistors in the signal path, because of their inferior transfer properties, should be avoided. The most simple implementation of the amplifier circuit as represented by the nullor symbol in the previous section is the differential pair as depicted in Fig. 4. Only the signal path is shown. Apart from the required tail current source, additional provisions are needed for proper biasing. We will assume here that the intended bias currents and voltages are present: the circuitry needed for this purpose will not be made explicit.

An even simpler amplifier circuit can be used for the implementation of configuration *G*. Since two terminals are in common, a single transistor according to Fig. 5 may be used.

With such simple implementations of the amplifier circuit substantial deviations from the ideal nullor behavior will occur, resulting in substantial currents and voltages at the input of the amplifier circuit. However, oscillators with these simple circuits will not easily show parasitic oscillations and will offer acceptable solutions in many situations. We will now present some basic oscillator circuits with the above simple nullor approximations.

Fig. 6 shows the signal path of an oscillator based on configuration *A* which uses a differential pair limiter ac-

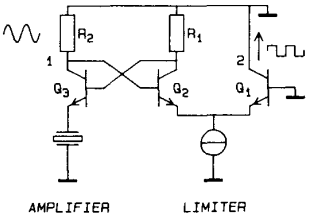


Fig. 7. Signal-path diagram of a crystal oscillator according to basic configuration G. The amplifier consists of only one transistor. The required inverting voltage limiter is realized with a simple differential pair.

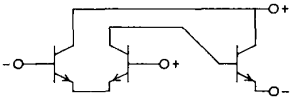


Fig. 8. Amplifier circuit with increased gain by cascading a differential pair with an additional single transistor.

cording to Fig. 3(c). At output terminal 1 a well-buffered sine-wave voltage is available, whereas a buffered square wave current can be obtained from the collector of the limiter stage (terminal 2). The square wave voltage at node 3 approximately equals the voltage that is supplied to the crystal, provided that the differential pair of the amplifier remains in its linear operating range.

The signal path of a crystal oscillator according to the basic configuration G is depicted in Fig. 7. The amplifier circuit consists of only one transistor (Q_3). The required inverting transimpedance is realized with a two-port voltage limiter in the form of a simple differential pair (Q_1 and Q_2). At node 1 a sinewave voltage is present. Since there is no buffering, it should not be supplied directly to a load. A buffered squarewave current is available at the collector of the differential pair which is more or less isolated from the oscillator loop, same as in Fig. 6.

The amplifier circuit can provide a better approximation to the nullor as the gain is increased. The optimum way of expanding the amplifier circuit with additional stages for achieving optimum performance with respect to noise, linearity, and speed is no different from that for amplifiers [1]. The use of a second stage in the amplifier circuit for example opens the possibility of optimizing the noise match to the crystal independent of the crystal drive level. In one-stage oscillators this is only possible by using a transformer.

A simple though useful extension of the amplifier circuit is shown in Fig. 8, where a single transistor has been used in cascade with a differential pair input stage. Collector and emitter of the output transistor are used as the inverting and non-inverting output terminals.

Using this amplifier circuit, the implementation of oscillator circuits according to configuration A is straight forward. One circuit, using a voltage limiter in the positive feedback loop is schematically shown in Fig. 9. Biasing arrangements are omitted again. The voltage across the diode limiter will have a peak value of about 0.7 V. This value is much too large to supply it directly to a crystal.

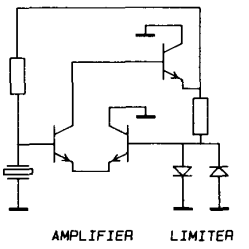


Fig. 9. Signal-path diagram of an oscillator according to configuration A with a voltage limiter in the positive feedback path.

Moreover, excessive bias currents would be needed in the output stage to keep the amplifier in its linear operating range. Therefore, only a fraction of the diode voltage should be supplied to the crystal.

Many other implementation examples can be given. However, generating such a catalogue of oscillator circuits would not contribute to the insight in an oscillator design strategy. It is left to the reader to construct other oscillators according to the rules presented in these first two sections.

V. Influence of the Finite Bandwidth of the Amplifier Circuit

Until now, we have disregarded the influence of the finite bandwidth of the amplifier circuit and of the shunt capacitance of the crystal. In this section, we will investigate the influence of these effects on the oscillator performance.

For the purpose of obtaining insight in the behavior of the negative impedance as a function of the time constants in the amplifier circuit, we can advantageously use an alternative reading [1] of Blackman's formula:

$$Z_i = Z_{i\infty} \frac{-A\beta_o}{1-A\beta_o} \cdot \frac{1-A\beta_{sc}}{-A\beta_{sc}}$$

where $Z_{i\infty}$ is there input impedance in the ideal situation where the amplifier circuit behaves as a nullor. $A\beta_o$ and $A\beta_{sc}$ are the loop transfer functions for the situations where the port at which Z_i is to be determined is open or short circuited, respectively. We can evaluate these loop transfer functions separately, and apply the root locus rules to find the singularities of Z_i. As an example we will apply this procedure to the basic oscillator circuit of Fig. 7.

When the port at which the negative impedance occurs is first short circuited, we easily find a circuit diagram as shown in Fig. 10. Assuming that the switching differential pair is in equilibrium, the loop consists of two cascaded stages and the two most dominant poles in the loop can easily be determined. Both these poles are determined by the input impedance of a stage shunted by a resistance (R_1 and R_2, respectively). The low frequency-loop gain $A\beta_{sc}$ approximately equals

$$A\beta_{sc} \simeq g_{m1} g_{m2} R_1 R_2,$$

where g_{m1} and g_{m2} are the transconductances of the

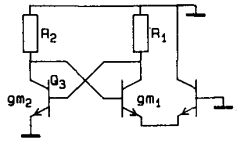


Fig. 10. Feedback loop for the determination of $A\beta_{sc}$.

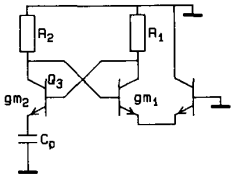


Fig. 11. Feedback loop for the determination of $A\beta_o$.

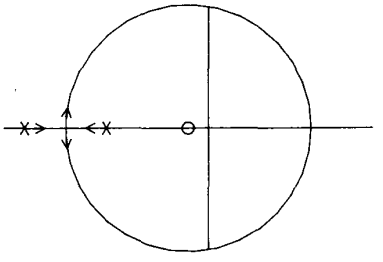


Fig. 12. Root locus for the loop of Fig. 11.

stages. Now, the roots of $1 - A\beta_{sc}$, which are zeros of the negative impedance are found by applying the root-locus rules. Because of the positive feedback, one of the roots will be positioned in the left-half plane, the other in the right-half plane. Both will be so remote from the origin that their influence on the negative impedance is not relevant. Note that the positions of these zeros do not depend on any impedance in parallel with the negative impedance port. Next, the negative resistance port will be left open for the determination of $A\beta_o$. The signal path for this situation is shown in Fig. 11. In this case, the parasitic capacitance of the crystal plays an important role. It causes a zero and a pole in the loop transfer function. The pole position is determined by the transconductance of the amplifier circuit and the shunt capacitance C_p. Apart from this pole, the loop transfer function has the same number of poles as $A\beta_{sc}$, but they may be in slightly different positions because of the interaction with the parasitic capacitance. Taking only the most dominant pole into account, we find the roots of $1 - A\beta_o = 0$ from a root locus as depicted in Fig. 12. The positive feedback forces the poles in the direction of the imaginary axis. Dependent on the actual loop gain value and the start positions of the poles, the circuit may become unstable with possible parasitic oscillations as a result. So, even in the case of a combination of a very simple amplifier circuit, which causes one dominant pole in the loop transfer function, and a memoryless limiter, the second pole introduced by the crystal shunt capacitance may jeopardize the HF stability.

For the design of an oscillator with maximum stability, the dominant pole of the amplifier circuit should be as far

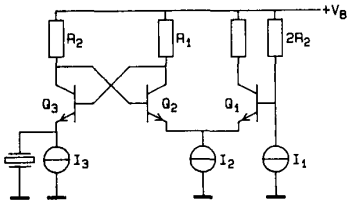


Fig. 13. Implementation of a crystal oscillator according to Fig. 7.

as possible from the origin, given the loop gain that is needed for reliable starting oscillations. Large influences on this pole position of parasitic capacitances like for example collector-to-substrate capacitances should therefore be avoided.

In the amplifier circuit of Fig. 8 the dominant pole is determined largely by such parasitic capacitances at the base of the output transistor. An oscillator with this amplifier will therefore be more sensitive to a shunt capacitance at the negative impedance port than an oscillator with the simple amplifier of Fig. 7.

This section has presented only qualitative considerations on the design of stable crystal oscillators. The next section will discuss an actual design, developed on the basis of these considerations, in more detail.

VI. Actual Design of a Bipolar Integrated Single-Pin Crystal Oscillator

In the previous sections we have shown how the basic configuration of a high performance single-pin crystal oscillator was found and we have discussed some aspects of the design of the amplifier circuit. It would take us too far to investigate all performance aspects. For example the noise behavior of these types of "negative-feedback" oscillators will be discussed elsewhere [4]. It suffices here to state that, in general, oscillators with an amplifier circuit that operates in its linear mode and with a feedback network that accomplishes a symmetrical limiting action will produce more noise than well-designed oscillators with an averaging AGC and less than oscillators with an amplifier circuit that operates highly nonlinear.

The oscillator configurations presented here have an important advantage. They offer the possibility of realizing a proper noise match to the crystal roughly independently from the power level at which the crystal is operated. The amplifier circuit, however, should consist of at least two stages to realize this situation. Unfortunately, it is more difficult in this situation to ensure HF stability.

In the case of moderate side-band noise requirements as in most consumer applications, there is no reason to aim at ultimate performance. The amplifier circuit can then be built with a single transistor or a single differential pair as in the examples from the previous section. We will consider the practical design aspects of such a simple oscillator here.

Fig. 13 shows an implementation example of the oscillator of Fig. 7. The amplifier transistor Q_3 has a somewhat negative collector-to-base voltage, which of course restricts

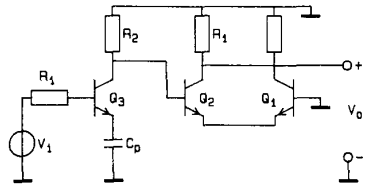


Fig. 14. The feedback loop of Fig. 13 for the determination of the poles and zeros in $A\beta_o$.

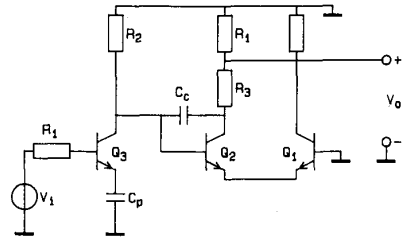


Fig. 15. Improved stability by increased capacitive load of Q_3.

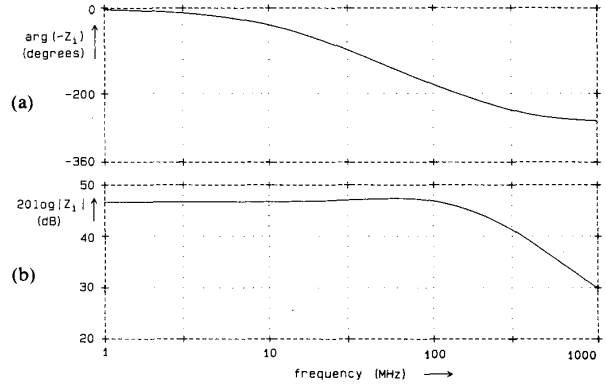


Fig. 16. Simulated input impedance of the oscillator of Fig. 13; input port shunted with $C_p = 5$ pF. (a) Phase response of $-Z_i$. (b) Amplitude response of Z_i.

the amplitude of the sinewave at the collector to some hundreds of millivolts. However, this is sufficiently large to operate the differential pair as a switch. The addition of an emitter follower at the input of the amplifier transistor would increase the linear output range of the amplifier circuit.

The amplitude of the square wave at the collector of Q_2 should be such, that when this voltage is supplied to the crystal (with some loss due to the finite output resistance of Q_3), the peak current in the crystal does not exceed the bias current in Q_3. Since the series resistance of the crystal is in the order of 50 Ω, the peak voltage should be very small if low-power operation of the crystal is required.

Let us assume that the oscillator should run at a total supply current of 1 mA divided over the current sources as: $I1 = 250\ \mu A$, $I2 = 250\ \mu A$, and $I3 = 500\ \mu A$ and that the series resistance of the crystal can range from 50 to 100 Ω. The design problem then reduces to the choice of $R1$ and $R2$ such that the voltage at the collector is a sinewave at all possible values of the crystal series resistance, the differential pair acts as a switch for all these values and transistor Q_3 remains in its linear region.

In order to keep transistor Q_3 in its linear operating range, the peak signal current in this transistor must be kept below 0.5 mA. At the minimum value of the crystal series resistance, we find that $R1$ should be smaller than about 400 Ω. As an example we select a value of 200 Ω which leads to a peak voltage at the crystal of about 12.5 mV and a peak crystal current of 250 μA. In order to guarantee oscillations the loop gain should exceed unity. With the value chosen for $R1$, we obtain $g_{m1}^{*}R1 = 0.5$ (where g_{m1} is the transconductance of the differential pair), and therefore $R2$ should have a value of more than 300 Ω, in the case where the series resistance of the crystal has its maximum value. Selecting a value of 600 Ω, the dc voltage drop across $R2$ amounts to 300 mV. The maximum peak voltage will not exceed 150 mV, so that Q_3 will not be driven into saturation. The sinewave voltage will be sufficiently large, also in the case of the maximum crystal series resistance to operate the differential pair as a switch. The negative resistance at the input port has a value of about -250 Ω in this case. So, oscillation is possible for series resistances up to 250 Ω.

The above design considerations disregard the frequency behavior of the negative impedance. We will now in some detail investigate the factors that may influence stability. For this purpose we model the part of the loop transfer function $A\beta_o$ that determines the pole and zero positions as in Fig. 14. The amplifier transistor Q_3 is shown, driven from the collector resistance of Q_2 and loaded by the input impedance of the differential pair which, because of its very low voltage gain, is assumed to operate unilaterally. The capacitances that dominate in the transfer function of this circuit are the parasitic capacitance C_p and the emitter–base capacitance C_{be}. These capacitances, together with the values of $R1$, $g_e = qI/kT$ and r_b determine the positions of the singularities. The transfer function has the form:

$$H(p) = \frac{p\tau}{1 + p\frac{c}{\omega_n} + p^2\frac{1}{\omega_n^2}}.$$

With given values of C_p and C_{be}, the damping can be increased by reducing the values of r_b and $R1$. The value of $R1$ can be reduced by increasing the current in the switching differential pair. The value of r_b can be kept small by using a well-designed transistor.

An increase of the capacitive load of Q_3 is another method to improve stability, since it reduces the loop gain increase caused by the shunt capacitance C_p. One effective method of increasing this capacitive load is shown in Fig. 15, where an additional resistor $R3$ and a capacitor C_c are used for this purpose. A drawback of this method is a larger error in the oscillation frequency due to an increased phaseshift at the resonance frequency.

Figs. 16–18 show the SPICE simulated behavior of the crystal oscillator to be realized in a bipolar process with an f_T of about 400 MHz. Transistor Q_3 has two base con-

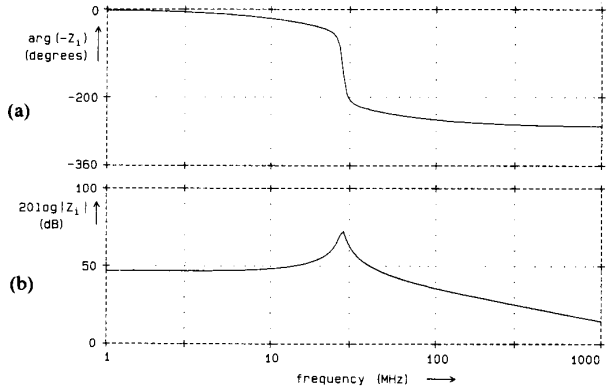


Fig. 17. Simulated input impedance of the oscillator of Fig. 13; input port shunted with $C_p = 30$ pF. (a) Phase response of $-Z_i$. (b) Amplitude response of Z_i.

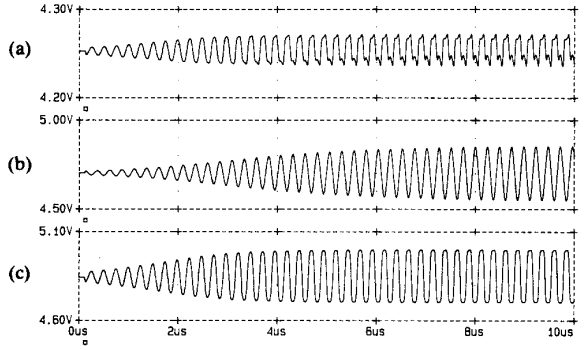


Fig. 18. Simulated signals of the oscillator of Fig. 13. (a) Voltage at the resonator. (b) Voltage at the collector of Q_3. (c) Voltage at the collector of Q_1.

tacts, resulting in a base resistance of about 100 ohms. Its base–emitter capacitance amounts to 7 pF. The compensation capacitance C_c is not explicitly present and $R3$ equals 1 kΩ. Fig. 16 shows the frequency dependency of the phase and magnitude of the input impedance measured at the negative-impedance port when this port is shunted by a 5-pF capacitance (this is about the value of the parasitic capacitance of the crystal). Fig. 17 shows similar plots for the case where C_p has a value of 30 pF. The behavior as predicted in Section V is obtained. It is seen that the poles of the negative impedance are close to the imaginary axis in the latter case.

In order to evaluate the start-up behavior of a crystal oscillator, very large simulation times are required. Therefore, the oscillation behavior was simulated with SPICE using a series LC oscillator with a Q of about 50 and a series resistor of 100 Ω (equal to the maximum crystal series resistance). Fig. 18 shows the start of the oscillations in response to a pulse voltage in series with the resonator. The waveforms at the crystal and at the collectors of Q_2 and Q_3 are shown. There is no sign of any parasitic instability.

The simulation has been repeated with a shunt capacitance of 30 pF. Such a high value is very unlikely to occur because normally a capacitance of some tens of picofarads

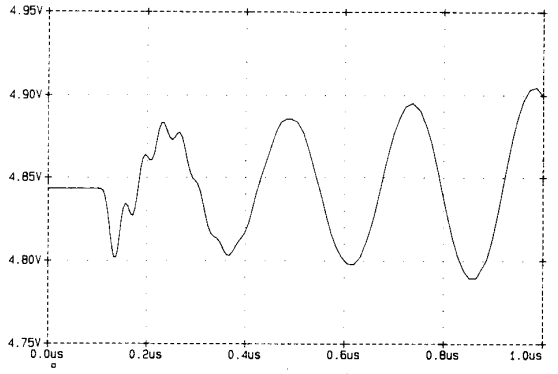


Fig. 19. Simulated signal with $C_p = 30$ pF. Resonance phenomena occur in the first periods.

will be inserted in series with the crystal to bring the frequency at its specified value. Fig. 19 shows the simulation result. It is seen that resonance phenomena occur in this case, but they fade away quickly, and the oscillator reaches its stable mode.

VII. A New Method for Obtaining Reproducible and Reliable Start-Up Behavior

One problem occurring in crystal oscillators which has not been given much attention in the past, is that the start-up behavior highly depends on the way in which some initial energy is supplied to the crystal. The supply of energy depends on the way the supply voltage is built up, on the actual implementation of the bias circuitry and on the amount of random noise supplied to the crystal. The use of large bypass capacitors for the supply voltage may lead to unreproducible start-up behavior and as a consequence to problems with testing. Instead of analyzing the causes for this behavior, we will introduce a technique in this paper that accurately controls the start-up behavior.

In the case where the crystal series resistance is drive-level dependent, the oscillation start-up might stick at a very low-power level when low values of the loop gain are involved. Crystal manufacturers normally recommend loop gain values that correspond to a negative resistance value of at least 10 times the maximum crystal series resistance for guaranteed start-up.

In order to realize a reliable start-up behavior with a much lower loop gain value, which benefits the noise performance, a well-controlled amount of energy should be supplied to the crystal, once the supply voltage has reached such a value that the state of the oscillator circuit is suitable for generating an oscillation signal. In the circuit of Fig. 13, this can be achieved by keeping the current I2 equal to zero until the supply voltage has reached a value of a few volts, and then generating the required current value by firing a Schmitt trigger. The transient is well defined in this way and a well defined voltage step is supplied to the crystal. The start-up behavior is made highly reproducible and reliable. An implementation example for the complete oscillator is shown in Fig. 20.

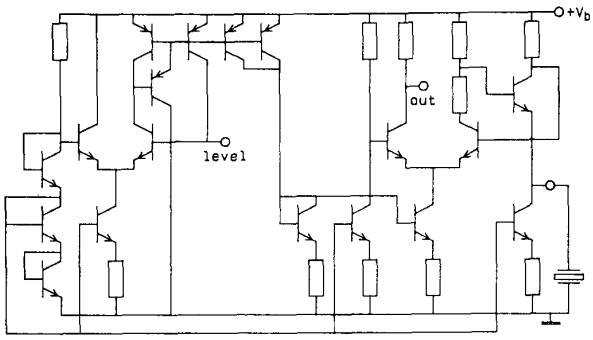


Fig. 20. Circuit diagram of a crystal oscillator with a Schmitt-trigger start-up control circuit.

The circuit of Fig. 20 has been integrated and tested with a large number of 4-MHz crystals, including several samples which have been rejected by the manufacturer for reasons of unacceptable drive-level dependency or low Q values. In all situations a reliable start of the oscillator was obtained.

In the case where the start-up circuit was omitted, the reproducibility of the start-up behavior was very poor.

VIII. Conclusions

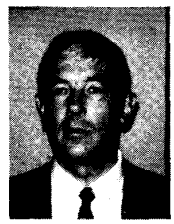
In this paper we have presented the basic configurations of crystal oscillators that need only one IC pin for the connection of the crystal. Such oscillators require a negative input impedance at the resonator port, which can be obtained by the application of a negative as well as a positive feedback loop around an active part. One of the loops includes a limiter circuit that accurately fixes the signal amplitude. Such oscillators can either generate sinewave or square-wave voltages or currents, thereby inherently providing a buffering action.

Oscillators of these types are susceptible to parasitic oscillations due to the parasitic shunt capacitance of the crystal. A simple model for the negative impedance reveals the methods for stability improvement.

Several implementations of crystal oscillators in bipolar technology were discussed. The performance of one version with a very simple structure was simulated and measured. In order to obtain a reliable start-up behavior, a novel start-up circuit was used in combination with this circuit. Even in the case of crystals that were rejected by the manufacturer, a very stable and reliable start-up behavior could be obtained. Parasitic oscillations were effectively eliminated in this circuit for shunt capacitances up to at least 30 pF.

References

[1] E. H. Nordholt, *Design of High-Performance Negative-Feedback Amplifiers*. Amsterdam, The Netherlands: Elsevier, 1983.
[2] J. H. Huijsing, "Integrated circuits for accurate linear analogue electric signal processing," Ph.D. dissertation, TU Delft, Delft, The Netherlands, June 1981.
[3] B. M. Oliver, "The effect of circuit non-linearity on the amplitude stability of *RC*-oscillators," *HP J.*, vol. 11, nos. 8–10, pp. 1–8, 1960.
[4] C. A. M. Boon, "Design of high-performance negative-feedback oscillators," Ph.D. dissertation, TU Delft, Delft, The Netherlands, Sept. 1989.



Ernst H. Nordholt received the Master's degree in electrical engineering from the Delft University of Techology, The Netherlands, in 1969. He received his Ph.D. degree in 1980. In the same year he became a member of the staff of the Electronic Teaching Lab. of that University and one year later he was appointed head of that lab. After some years of teaching electronic practice, he changed his activities to research on systematic design approaches for analog electronic functions. In 1977 he joined the Electronic Research Lab. in order to prepare a doctoral thesis. In 1986 he founded together with three colleagues a consultancy company Catena Microelectronics, Delft, where he is presently the general manager. His research interests are in the area of analog electronic circuits and integrated radio systems.

Corlex A. M. Boon received the Master's and Ph.D. degrees in electrical engineering from the Delft University of Technology, The Netherlands, in 1978 and 1989, respectively. Afterwards he became a research assistant at the University, where he was involved in oscillator design. In 1984 he joined the Philips group and is currently employed by Hollandse Signaalapparaten B.V. There his main interests lie in the design of customized power supplies and sonar equipment.