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Toth, Nandor G.; Tang, Zhong; Someya, Teruki; Pan, Sining; Makinwa, Kofi A.A.

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# A PNP-Based Temperature Sensor With Continuous-Time Readout and $\pm 0.1$ °C ( $3\sigma$ ) Inaccuracy From $-55$ °C to $125$ °C

Nandor G. Toth<sup>1</sup>, Graduate Student Member, IEEE, Zhong Tang<sup>2</sup>, Member, IEEE, Teruki Someya, Member, IEEE, Sining Pan<sup>3</sup>, Member, IEEE, and Kofi A. A. Makinwa<sup>1</sup>, Fellow, IEEE

**Abstract**—This article describes a PNP-based temperature sensor that achieves both high energy efficiency and accuracy. Two resistors convert the CTAT and PTAT voltages generated by a PNP-based front-end into two currents whose ratio is then digitized by a continuous-time (CT)  $\Delta\Sigma$ -modulator. Chopping and dynamic-element-matching (DEM) are used to mitigate the effects of component mismatch and  $1/f$  noise, while the spread in  $V_{BE}$  and in the ratio of the two resistors is digitally trimmed at room temperature (RT). Fabricated in a  $0.18$   $\mu\text{m}$  CMOS process, the sensor occupies  $0.12$   $\text{mm}^2$ , and draws  $9.5$   $\mu\text{A}$  from a supply voltage ranging from  $1.7$  to  $2.2$  V. Measurements on 40 samples from one batch show that it achieves an inaccuracy of  $\pm 0.1$  °C ( $3\sigma$ ) from  $-55$  °C to  $125$  °C, and a commensurate supply sensitivity of only  $0.01$  °C/V. Furthermore, it achieves high energy efficiency, with a resolution Figure of Merit (FoM) of  $0.85$   $\text{pJ}\cdot\text{K}^2$ .

**Index Terms**—Bitstream-controlled (BSC) dynamic-element-matching (DEM), continuous-time (CT)  $\Delta\Sigma$ -modulator, current-mode readout, PNP-based temperature sensor, resistor ratio self-calibration.

## I. INTRODUCTION

**B**JT-BASED temperature sensors are widely used since they can achieve high accuracy after a single temperature trim [1]. Readout architectures based on switched-capacitor (SC)  $\Delta\Sigma$ -modulators [2], [3], [4], [5] can achieve inaccuracies below  $0.2$  °C ( $3\sigma$ ) from  $-55$  °C to  $125$  °C after a room temperature (RT) trim. However, their sampling ( $kT/C$ ) noise reduces their resolution and energy efficiency. Readout architectures based on continuous-time (CT)  $\Delta\Sigma$ -modulators do not suffer from sampling noise and thus achieve lower noise

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Nandor G. Toth and Kofi A. A. Makinwa are with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: N.G.Toth@tudelft.nl).

Zhong Tang was with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands. He is now with Vango Technologies Inc., Hangzhou 310053, China.

Teruki Someya was with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands. He is now with SiTime Japan, Tokyo 108 0075, Japan.

Sining Pan was with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands. He is now with the School of Integrated Circuits, Tsinghua University, Beijing 100084, China.

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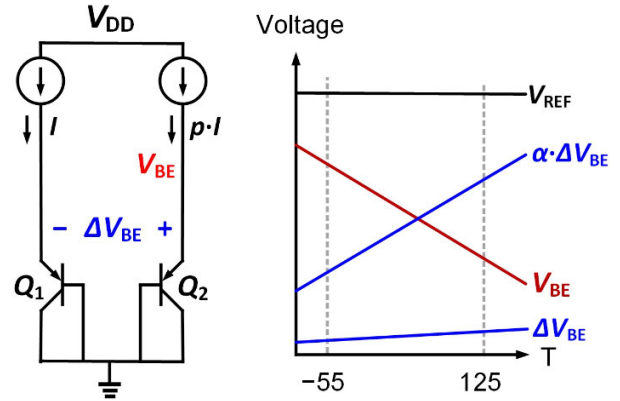


Fig. 1. Voltage-readout of a PNP-based front-end.

and better energy efficiency [6], [7]. However, they have not yet been able to match the accuracy of their SC counterparts.

Fig. 1 illustrates the basic operating principle of a PNP-based temperature sensor. Two PNPs biased at a current ratio  $p$  are used to generate the following voltages:

$$V_{BE} = n_e \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) \quad (1)$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = n_e \frac{kT}{q} \ln(p) \quad (2)$$

where  $n_e$  is the PNP's nonideality factor,  $k$  is the Boltzmann's constant,  $q$  is the unit electron charge, and  $I_C$  and  $I_S$  are the PNP's collector- and saturation-current, respectively. As shown in Fig. 1, the temperature dependence of the base-emitter voltage  $V_{BE}$  is complementary to absolute temperature (CTAT), while that of  $\Delta V_{BE}$  is proportional to absolute temperature (PTAT). By multiplying  $\Delta V_{BE}$  by a constant factor  $\alpha$  and adding this to  $V_{BE}$ , a temperature-independent bandgap reference voltage can be made. This can then be used to generate a linear function of absolute temperature

$$\mu_{\text{lin}} = \frac{\alpha \cdot \Delta V_{BE}}{\alpha \cdot \Delta V_{BE} + V_{BE}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{\text{ref}}} \quad (3)$$

To achieve high accuracy, the spread in the various variables in (3) must be minimized. The spread in  $V_{BE}$ , which is mainly due to the spread of  $I_C$  and  $I_S$ , can be mitigated by a room-temperature PTAT trim [8], while offset errors in the readout of  $V_{BE}$  and  $\Delta V_{BE}$  can be reduced to the microvolt-level by various combinations of chopping, auto-zeroing, and correlated double sampling [2], [3], [5]. The accurate implementation of the ratios  $\alpha$  and  $p$  is also important. Their spread must typically be less than  $0.01\%$  to ensure

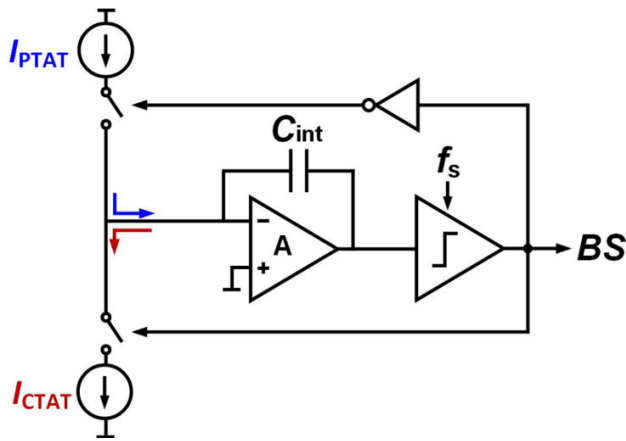


Fig. 2. Current-mode readout of a BJT-based temperature sensor.

that the resulting errors are less than  $0.1^\circ\text{C}$ . In sensors based on SC  $\Delta\Sigma$ -modulators,  $\alpha$  is usually defined by the ratio of the capacitors used to sample  $V_{BE}$  and  $\Delta V_{BE}$ , respectively, while  $p$  is set by a current-mirror ratio. High accuracy can then be readily achieved with the help of dynamic element matching (DEM) [9]. Although the resolution of SC  $\Delta\Sigma$ -modulators is limited by  $kT/C$  noise, this can be mitigated by using large sampling capacitors and/or a large oversampling ratio (OSR). However, this comes at the expense of power and/or longer conversion times. As a result, their energy efficiency, as expressed by their resolution FoM [10], has remained stubbornly steady at around a few  $\text{pJ}\cdot\text{K}^2$  [1].

Alternatively, BJT-based sensors can be read out by CT  $\Delta\Sigma$ -modulators, which do not suffer from sampling noise [11]. However, their accuracy is often limited by the spread of  $\alpha$ , since the effectiveness of DEM will now be limited by switching transients. In [6], which achieves a state-of-the-art resolution FoM of  $0.19 \text{ pJ}\cdot\text{K}^2$ ,  $\alpha$  is determined by static resistor ratios. In [7],  $\alpha$  is also defined by resistor ratios, but the use of a large resistor array and DEM results in an inaccuracy of  $\pm 0.15^\circ\text{C}$  ( $3\sigma$ ) from  $-45^\circ\text{C}$  to  $130^\circ\text{C}$ , and a FoM of  $3.6 \text{ pJ}\cdot\text{K}^2$ . In [12],  $\alpha$  is defined by the gain of a capacitively-coupled instrumentation amplifier (CCIA). By calibrating this gain, an inaccuracy of  $\pm 0.13^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  is achieved, and a FoM of  $5.4 \text{ pJ}\cdot\text{K}^2$ .

In this article, an extended version of [13], a PNP-based temperature sensor that achieves both high accuracy and energy efficiency is presented. Its readout architecture is based on a CT  $\Delta\Sigma$ -modulator that balances currents proportional to  $V_{BE}$  and  $\Delta V_{BE}$ , respectively. Current-mirror and BJT mismatch is mitigated by DEM, while resistor-ratio mismatch is mitigated by a low-cost self-calibration scheme. As a result, the sensor achieves a FoM of  $0.85 \text{ pJ}\cdot\text{K}^2$  and an inaccuracy of  $\pm 0.1^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  after room-temperature calibration.

The rest of the article is organized as follows. Section II describes the operation of current-mode BJT-based temperature sensors and Section III discusses their design challenges. Section IV describes the design of the proposed sensor and its error-reduction techniques in detail. The circuit implementation is discussed in Section V. Section VI presents the measurement results and compares them to the state-of-the-art. The article ends with some conclusions.

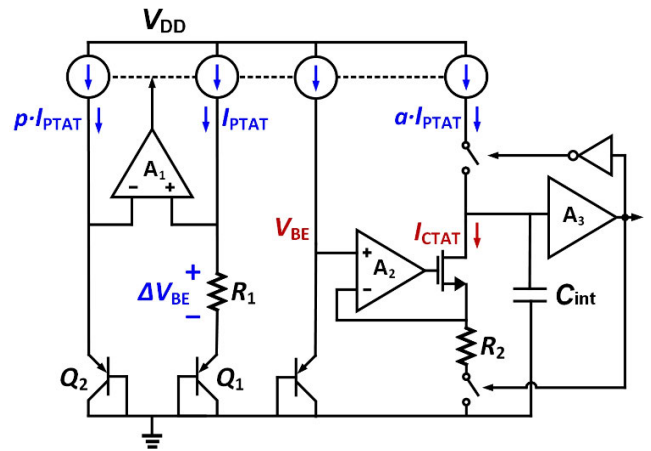


Fig. 3. Simplified schematic of the current-mode front-end used in [7].

## II. CURRENT-MODE READOUT

Fig. 2 illustrates the basic operation of a PNP-based temperature sensor with a current-mode readout circuit. The temperature-dependent voltages,  $\Delta V_{BE}$  and  $V_{BE}$ , are converted into the currents  $I_{PTAT}$  and  $I_{CTAT}$ , respectively, which are applied to a first-order CT  $\Delta\Sigma$ -modulator. Depending on the modulator's bitstream output (BS), either  $I_{CTAT}$  or  $I_{PTAT}$  will be integrated by a capacitor  $C_{int}$ . Over several cycles, the total integrated charge contributed by  $I_{CTAT}$  and  $I_{PTAT}$  will be balanced, and so the bitstream average  $\mu$  will be a digital representation of temperature. As a result,  $\mu \cdot I_{CTAT} = (1 - \mu) \cdot I_{PTAT}$  and so  $\mu = I_{PTAT} / (I_{CTAT} + I_{PTAT})$ . As in (3), a linear function of temperature can then be obtained by appropriately scaling  $I_{PTAT}$  and  $I_{CTAT}$ .

A simplified schematic of the front-end of the design reported in [7], is shown in Fig. 3.  $I_{PTAT} = \Delta V_{BE} / R_1$  is generated by using an opamp  $A_1$  to force  $\Delta V_{BE}$  over a resistor  $R_1$ , while  $I_{CTAT} = V_{BE} / R_2$  is generated by using a second opamp  $A_2$  to force  $V_{BE}$  over a second resistor  $R_2$ . These currents are then applied to the duty-cycle modulator formed by  $C_{int}$  and a Schmitt trigger  $A_3$ , whose output controls the DAC switches. By properly scaling the resistors, the duty cycle of the modulator's output will be a linear function of temperature. However, a high-frequency counter is required to digitize its duty-cycle modulated output. Furthermore, two low-offset high-gain opamps are required to accurately generate  $I_{PTAT}$  and  $I_{CTAT}$ .

A simpler front-end is shown in Fig. 4, which does not require an additional opamp to generate  $I_{CTAT}$ . As suggested in [14],  $I_{CTAT}$  is generated by applying  $V_{BE}$  to the positive terminal of the opamp ( $A_2$ ) that also implements the first integrator of a current-balancing modulator.  $V_{BE}$  is then copied to its virtual ground and forced over  $R_2$ . Charge balancing is achieved by using the modulator's output BS to regulate  $I_{PTAT}$ . Although the bitstream average  $\mu$  is not a linear function of temperature, it remains a linear function of  $V_{BE} / \Delta V_{BE}$ , as will be shown in Section IV, and so can be readily linearized in the digital backend [4].

## III. MAIN ERROR SOURCES

In the target 180 nm process, the available PNPs are parasitic devices, which can only be biased via their emitters.

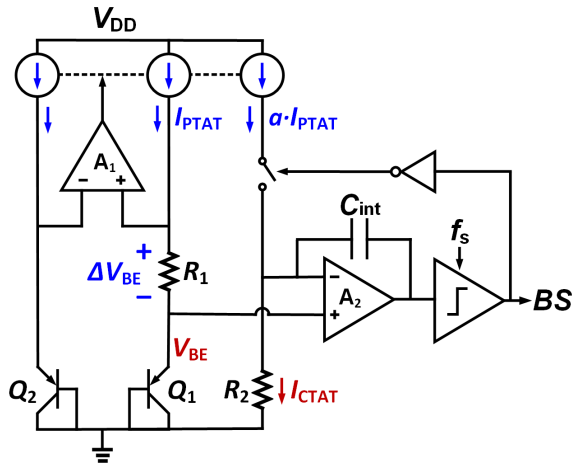


Fig. 4. Basic circuit diagram of the proposed front-end.

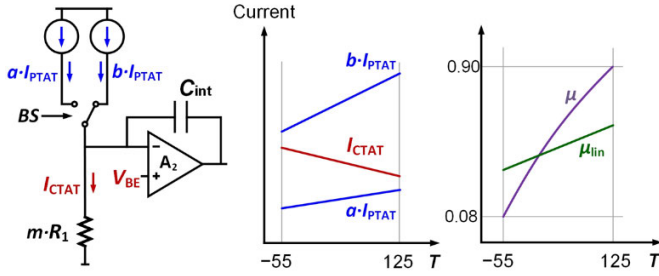


Fig. 5. Simplified circuit diagram with a dual-level IDAC, and the resulting currents versus temperature.

Their current gain  $\beta$  is low ( $\sim 3$ ) and spreads, which decreases the accuracy of the resulting collector currents, and hence that of  $V_{BE}$  [15]. Taking the finite  $\beta$  of the PNPs into account,  $V_{BE}$  can be expressed as

$$V_{BE} = n \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right) = n \frac{kT}{q} \ln\left(\frac{I_{PTAT}}{I_S} \frac{\beta}{\beta + 1}\right). \quad (4)$$

Although most of the spread in  $V_{BE}$  can be corrected by a PTAT trim [8], the temperature dependence of  $\beta$  will give rise to a residual error. Simulations show that this results in a worst-case corner spread of  $\pm 0.15$  °C from  $-55$  °C to  $125$  °C, which represents an upper bound on the sensor's inaccuracy. Since the relation between  $\beta$  and the collector current is quite constant, however, the collector-current ratio  $p$  ( $=7$  in this work) is well-defined, and so the corresponding spread in  $\Delta V_{BE}$  is only  $\pm 0.02$  °C over the same temperature range.

As can be seen from Fig. 4, the voltage drop across  $R_1$  is the sum of  $\Delta V_{BE}$  and the input voltage of the bias amplifier  $A_1$ . As a result, both its finite dc gain  $A_{OL}$  and offset  $V_{os}$  will limit the accuracy of  $I_{PTAT}$  according to

$$I_{PTAT} = \frac{\Delta V_{BE} + V_{os}}{R_1 \left(1 + \frac{1}{g_m R_1 A_{OL}}\right)} \quad (5)$$

where  $g_m$  is the transconductance of the current source that biases  $Q1$ . For  $p = 7$  and  $g_m R_1 = 0.2$ ,  $A_{OL} > 77$  dB and  $V_{os} < 3$   $\mu$ V are required to ensure that their respective error contributions are less than  $0.01$  °C ( $\sigma$ ) at RT. In a similar manner, the input voltage of  $A_2$  will cause errors in  $I_{CTAT}$ .

To keep these below  $0.01$  °C ( $\sigma$ ),  $A_{OL} > 65$  dB and  $V_{os} < 40$   $\mu$ V are required. These requirements are more relaxed than those on  $A_1$ , since the temperature sensitivity of  $V_{BE}$  ( $-1.9$  mV/K) is much larger than that of  $\Delta V_{BE}$  ( $0.17$  mV/K).

Errors in the collector current ratio  $p$  and the DAC current ratio  $a$  (see Fig. 4) cause errors in the PTAT current  $I_{PTAT,ADC}$  that is applied to the modulator

$$I_{PTAT,ADC} = \frac{\Delta V_{BE}}{R_1} \left(1 + \frac{\Delta a}{a} + \frac{1}{\ln(p)} \frac{\Delta p}{p}\right). \quad (6)$$

Here  $\Delta a/a$  and  $\Delta p/p$  represent the mismatch in the respective current-mirror ratios. For an error of  $0.01$  °C ( $\sigma$ ) at RT,  $\Delta a/a < 60$  ppm ( $\sigma$ ) and  $\Delta p/p < 130$  ppm ( $\sigma$ ) are required. Such tight matching cannot be achieved by good layout alone and thus necessitates the use of DEM or calibration. To make  $I_{CTAT}$  similarly accurate,  $\Delta m/m < 60$  ppm ( $\sigma$ ) is required, where  $m$  is the resistor ratio  $R_2/R_1$ . In this work, as will be discussed in the following section, it was decided to mitigate resistor-ratio errors by calibrating  $m$  rather than using DEM.

#### IV. PROPOSED SENSOR TOPOLOGY AND TECHNIQUES

This section discusses the architectural choices and error-correction techniques used in this work. First, the design of the DAC and the choice of system coefficients are discussed. Then, the dynamic error-correction techniques necessary to achieve high accuracy are introduced, along with a novel scheme to calibrate the mismatch in  $R_2/R_1$ . Finally, the implementation of a voltage calibration scheme is discussed.

##### A. DAC Design and Coefficient Scaling

As shown in Fig. 4, a current-balancing readout can be implemented by using the BS of the CT  $\Delta\Sigma$ -modulator to control a current-DAC that switches between  $0$  and  $I_{PTAT}$  to balance a continuous current  $I_{CTAT}$ . As shown in Fig. 5, however, better use of the modulator's dynamic range can be achieved by using a two-level current-DAC whose output switches between two levels:  $a \cdot I_{PTAT}$  and  $b \cdot I_{PTAT}$ . With this scheme, the bitstream average  $\mu$  can be expressed as

$$\mu = \frac{b}{b-a} - \frac{1}{(b-a)m} \cdot \frac{V_{BE}}{\Delta V_{BE}}. \quad (7)$$

With  $p = 7$ , the choice of  $a = 1$ ,  $b = 4$ , and  $m = 6$  results in a  $\mu$  that varies in a non-linear fashion from  $0.08$  to  $0.90$  from  $-55$  °C to  $125$  °C (see Fig. 5), and thus uses  $82\%$  of the modulator's dynamic range. With  $X = V_{BE}/\Delta V_{BE}$ ,  $\mu$  can then be expressed as

$$\mu = \frac{4}{3} - \frac{X}{18}. \quad (8)$$

Since  $\mu$  is a linear function of  $X$ , a PTAT trim of  $V_{BE}$  can be implemented by performing a simple offset trim on  $\mu$  in the digital domain [4]. As shown in Fig. 5, a linear function of temperature  $\mu_{lin}$  can then be obtained by rewriting (3) as follows:

$$\mu_{lin} = \frac{\alpha}{\alpha + X} = \frac{\alpha}{\alpha + 24 - 18\mu}. \quad (9)$$

This can be converted into an output in °C by simply computing  $D_{out} = A \cdot \mu_{lin} - B$ , where  $A$  and  $B$  are fitting parameters.

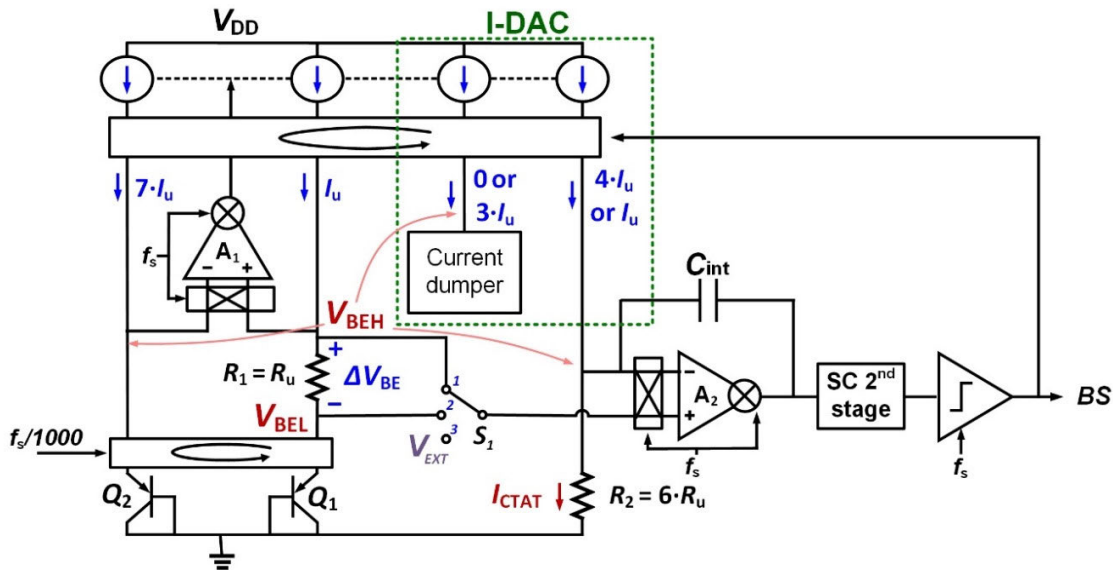


Fig. 6. Block diagram of the full sensor including dynamic error-correction techniques.

### B. Dynamic Error-Reduction Techniques

A more detailed block diagram of the proposed sensor is shown in Fig. 6. The offset and  $1/f$  noise of  $A_1$  and  $A_2$  are mitigated by chopping them at the sampling frequency  $f_s$ . Since the output spectrum of a  $\Delta\Sigma$ -modulator has notches at multiples of  $f_s$ , this choice of frequency prevents quantization noise folding.

As discussed in Section II, the current ratios  $p$ ,  $a$ , and  $b$  should have errors below 100 ppm ( $\sigma$ ). To realize this, the four current branches shown in Fig. 6 are implemented by 12-unit current sources, whose mismatch and  $1/f$  noise are mitigated by DEM. One unit source biases  $Q_1$ , seven bias  $Q_2$ , while 4 are used to implement the two-level DAC. To avoid intermodulation between the bitstream and the DEM sequence, a bitstream-controlled (BSC) DEM scheme is employed [16]. As shown in Fig. 7, this involves the use of two barrel-shifting registers to control the DEM switches: one which is clocked when  $BS = 0$  ( $SR_0$ ) and one which is clocked when  $BS = 1$  ( $SR_1$ ). In this way, each DEM state occurs with equal frequency, irrespective of the bitstream sequence, thus avoiding quantization noise folding.

The mismatch between the two PNPs, which would otherwise cause spread to  $\Delta V_{BE}$ , is also mitigated by DEM. Since their  $1/f$  noise corner is well below 10 Hz, they are swapped at  $f_s/1000$ , which results in negligible quantization noise folding.

### C. Transient Error Reduction

In a CT  $\Delta\Sigma$ -modulator, the switching transients of the DAC will also be integrated by the first stage, which may cause significant errors and ISI. To minimize such transients, unused DAC elements are switched to  $V_{BEH}$  by connecting them to a BJT-based current dumper (see Fig. 6). Since the virtual grounds of  $A_1$  and  $A_2$  are also at  $V_{BEH}$ , all 12 current sources are switched between the same voltage levels, which further minimizes DEM-related switching transients.

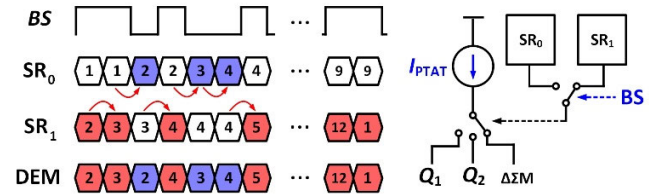


Fig. 7. Implementation of BSC DEM.

### D. Resistor Ratio Calibration

As discussed in Section III, the error in the resistor ratio  $m = R_2/R_1$  should be less than 100 ppm ( $\sigma$ ), which cannot be achieved by precise layout alone. This would be difficult to achieve with DEM, since the voltage drops across  $R_1$  and  $R_2$  are quite different, leading to large switching transients during DEM transitions due to the charging and discharging of their parasitic capacitances. In this work, resistor mismatch is mitigated by digitizing  $m$  and then correcting its spread in the digital domain. This is done by performing two conversions with the first integrator's virtual ground connected to either  $V_{BEL}$  or  $V_{BEH} + \Delta V_{BE}$  (see Fig. 6). The difference  $\Delta\mu$  in the resulting bitstream averages is then

$$\Delta\mu = \frac{1}{m(b-a)} \frac{(V_{BEH} + \Delta V_{BE}) - V_{BEL}}{\Delta V_{BE}} = \frac{1}{m(b-a)} \quad (10)$$

where  $b$  and  $a$  are current ratios, whose accuracy is guaranteed by DEM. As a result, the resistor ratio  $m$  can be accurately determined. Any mismatch can then be digitally corrected with the help of the following equation:

$$\mu_{\text{calibrated}} = \frac{\mu - \frac{4}{3}}{18 \cdot \Delta\mu} + \frac{4}{3}. \quad (11)$$

However, (10) only holds if  $V_{BE}$  and  $\Delta V_{BE}$  are constant during the two conversions, which in turn means that both thermal noise and ambient temperature drift will cause calibration errors. Detecting mismatch errors below 100 ppm requires the

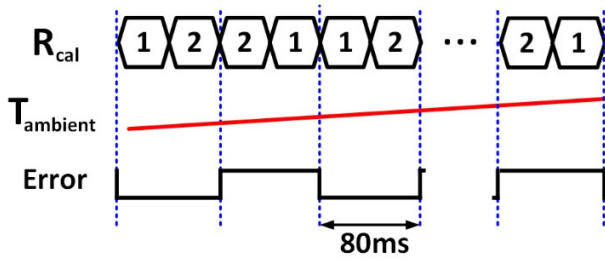


Fig. 8. Alternating differential resistor-calibration measurement.

ambient temperature to be stable to within 1.5 mK, and the modulator's resolution to be below 0.5 mK ( $\sigma$ ). To relax the stringent requirements on temperature stability, the calibration is split up into ten pairs of short (40 ms) conversions, which are performed in alternating order, as shown in Fig. 8. This method cancels  $\Delta\mu$  errors caused by linear temperature drift. The resistor ratio can then be determined in 0.8 s without an external reference, making it a low-cost calibration.

### E. Voltage Calibration

As described in [17], voltage calibration is a low-cost alternative to a temperature trim. It involves digitizing  $\Delta V_{BE}$  by performing a  $\Delta\Sigma$ -conversion in which  $V_{BE}$  is replaced by a known external voltage  $V_{EXT}$ , which is chosen to be approximately equal to the expected  $V_{BE}$  (see Fig. 6). The exact temperature of the die can then be determined from (2) and used to perform a temperature trim.

The accuracy of voltage calibration is limited by the spread in the PNP's nonideality factor ( $n_e$ ), which causes errors in the temperature estimated from  $\Delta V_{BE}$ . However, compared to a traditional temperature trim, in which an external temperature sensor must be brought into thermal equilibrium with the die, this scheme only requires a voltage reference and can be performed in two conversions (80 ms), making it a fast and low-cost trimming technique.

## V. CIRCUIT IMPLEMENTATION

### A. Front-End

A more detailed schematic of the proposed front-end is shown in Fig. 9. As discussed above, DEM is used to mitigate the mismatch of the PNPs and the PMOS current sources. To avoid bias current errors due to the IR drops across the DEM switches, Kelvin connections are used to connect PNP/ $R_1$  pairs to the current sources and the bias opamp  $A_1$  [7]. A multiplexer is then used to connect the appropriate  $V_{BE}$  to the modulator, depending on the DEM ( $S_{DEM}$ ) and  $R_{CAL}$  states. The emitter-current ratio  $p = 7$  is established by 8 cascoded PMOS current sources, which are biased in strong inversion ( $g_m/I_D = 4$ ) to maximize their initial matching and reduce their thermal noise contribution to  $I_{PTAT}$  [18]. Their high  $r_{out}$  ( $>40$  G $\Omega$  at RT) ensures that small changes in their drain voltages, as occur during resistor and voltage calibration, result in negligible current errors. As discussed above, the current sources are then incorporated in a BSC-DEM scheme, which ensures that the error due to their residual mismatch is

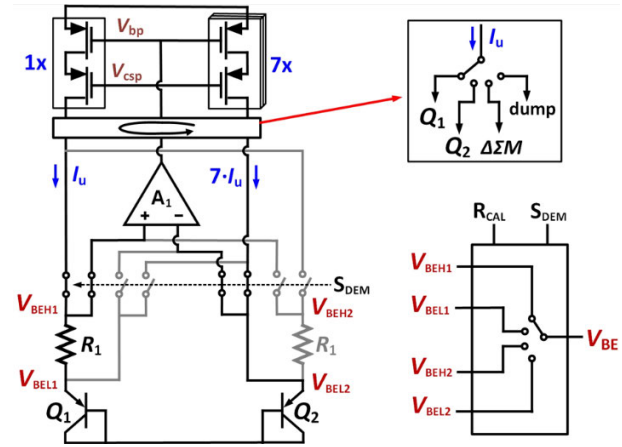


Fig. 9. Circuit diagram of the front-end and the  $V_{BE}$  switches.

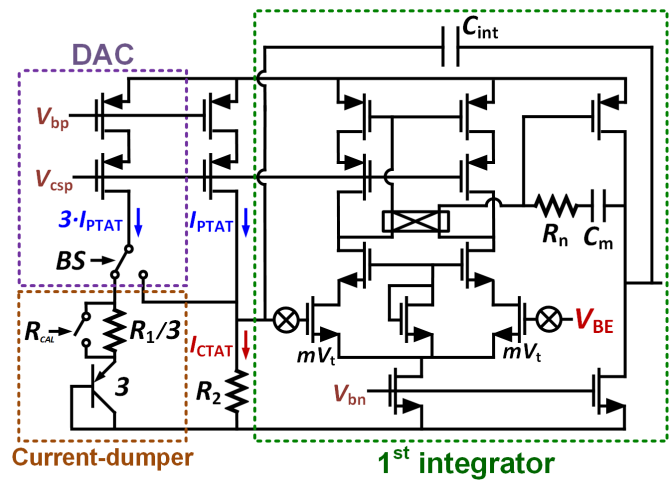


Fig. 10. Circuit diagram of the DAC and first integrator.

negligible ( $<5$  mK). This is implemented by connecting each of the current sources to a 1:4 multiplexer.

Opamp  $A_1$  is implemented as an energy-efficient telescopic amplifier with an NMOS input pair. Its tail current is  $6 \cdot I_{PTAT}$ , which ensures that its thermal noise contribution to  $I_{PTAT}$  is similar to that of  $R_1$ . The amplifier has an  $A_{OL}$  of 83 dB over PVT, which satisfies the requirements described in Section II. Furthermore, it has a GBW of 220 kHz at RT, which ensures that the error due to switching transients is below 30 mK.

### B. $\Delta\Sigma M$

A current-input CT- $\Delta\Sigma$  modulator is used to digitize the signals in the front-end. A second order loop filter is implemented for a good compromise between the required OSR and design complexity. The  $\Delta\Sigma M$  is clocked at 50 kHz over a conversion time of 40 ms, realizing an OSR of 2000. This ensures that the quantization noise power is at least 10 dB lower than the thermal noise power over the temperature range.

Fig. 10 shows a circuit diagram of the implemented DAC and first integrator. Both the DAC and the first integrator reuse the PTAT current generated in the front end. The current dumper consists of three parallel PNPs in series with a resistor  $R_1/3$  that is shorted during resistor calibration. In this way,

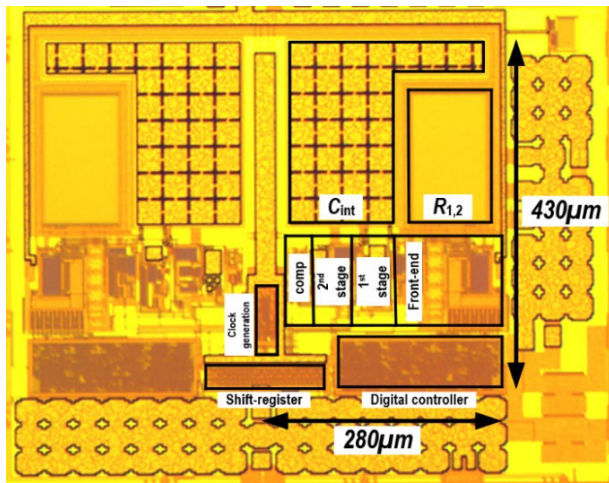


Fig. 11. Micrograph of the die.

the dumper voltage is set to  $V_{BEH}$  and  $V_{BEL}$  during normal operation and resistor calibration, respectively.

The first integrator's OTA must source/sink the output current of the DAC, while also providing high dc gain and GBW. To achieve this, it was realized by a two-stage Miller-compensated amplifier. Like  $A_1$ , the first stage is a chopped telescopic cascode amplifier. Both  $A_1$  and  $A_2$  use input pairs based on medium- $V_t$  NMOS devices to ensure that their tail transistors remain in saturation at high temperatures, when their input common-mode voltage ( $=V_{BEH}$ ) is low ( $\sim 450$  mV). Since  $A_2$  has relaxed noise requirements, the current in the first stage of  $A_2$  is  $3\times$  lower than in  $A_1$ . The second stage is a PMOS common-source stage biased at  $4.5 \cdot I_{PTAT}$ . The OTA has an  $A_{OL}$  of  $>110$  dB over PVT and a GBW of 600 kHz, which ensure that errors due to switching transients are below 20 mK. It is stabilized by a Miller capacitor  $C_m$  ( $=680$  fF) and a nulling resistor  $R_n$  ( $=165$  k $\Omega$ ). The current signals are integrated on  $C_{int}$  ( $=60$  pF), which ensures that the voltage swing at the output of  $A_2$  is less than 0.6 V over PVT.

The second integrator is an area-efficient SC circuit, whose  $kT/C$  noise is attenuated by the high voltage gain of the first integrator. It dissipates  $4\times$  less power and occupies  $11\times$  less area than the first integrator.

## VI. MEASUREMENT RESULTS

The proposed temperature sensor was fabricated in a standard  $0.18 \mu\text{m}$  CMOS process. Two sensors were realized on each die, thus enabling the use of differential measurements to cancel ambient temperature drift [19]. As shown in Fig. 11, each sensor occupies  $0.12 \text{ mm}^2$ , most of which is taken up by capacitors and resistors. All digital control signals are generated on-chip from a 200 kHz primary clock. For flexibility, the nonlinearity removal and  $\text{sinc}^2$  decimation filter are implemented off-chip.

### A. Power Consumption

Each sensor draws  $9.5 \mu\text{A}$  from a 1.7 V supply. Fig. 12 shows a breakdown of the corresponding power dissipation, with  $f_s = 50$  kHz. The front end dissipates the most power,

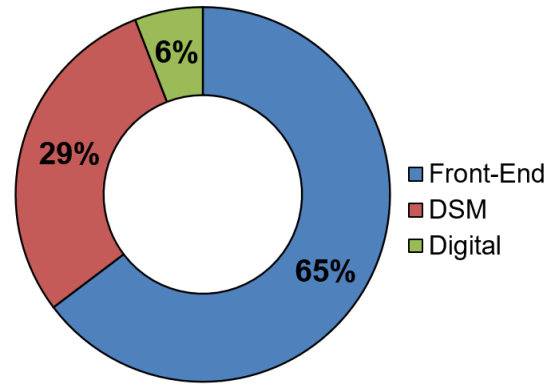


Fig. 12. Power distribution of a sensor.

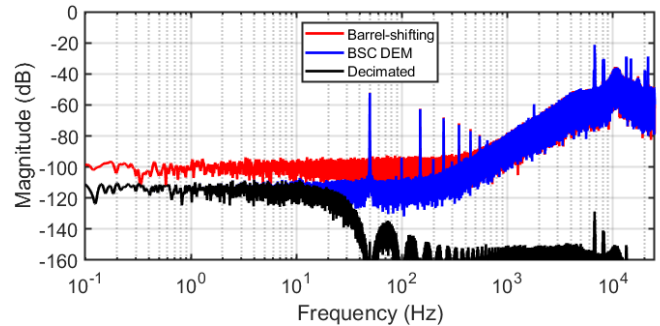


Fig. 13. FFT of the bitstream.

followed by the  $\Delta\Sigma\text{M}$ , and the digital logic. A version of the sensor with an on-chip decimation filter, a polynomial-based nonlinearity removal, and an SPI interface were also made [5]. The required digital circuitry occupies  $0.04 \text{ mm}^2$  and dissipates  $0.98 \mu\text{A}$  at RT, increasing the area and power by 33% and 10%, respectively.

### B. FFT and Resolution

Fig. 13 shows an FFT of the bitstream when the modulator is operating in free-running mode. It exhibits second order quantization noise shaping, with a  $1/f$  noise corner well below 100 mHz. Compared to the use of barrel-shifting DEM, the use of BSC-DEM does a better job of mitigating quantization noise folding. The remaining in-band tones are due to the BJT DEM and are suppressed by the notches of the  $\text{sinc}^2$  decimation filter. As can be seen in Fig. 14, the sensor becomes quantization noise limited for conversions shorter than 10 ms. It achieves a thermal-noise limited resolution of 1.1 mK (rms) in 40 ms, resulting in a resolution figure of merit (FoM) of  $0.85 \text{ pJ}\cdot\text{K}^2$ .

### C. Extracted Resistor Ratios

Fig. 15 shows a histogram of the normalized resistor ratio of all 40 measured samples. Its spread has a standard deviation of 450 ppm, which agrees well with mismatch simulations. These indicate that to achieve the required 60 ppm ( $\sigma$ ) mismatch, a resistor area of  $1.6 \text{ mm}^2$  would have been required, thus validating the use of resistor-ratio calibration.



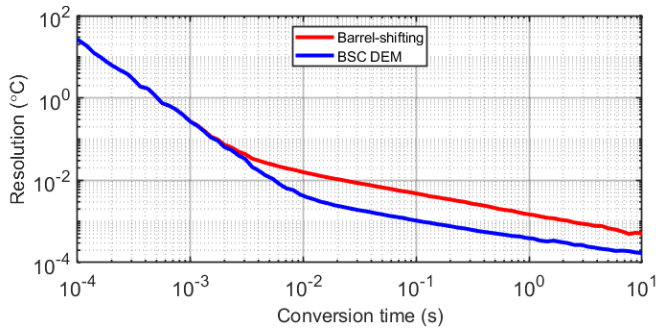


Fig. 14. Temperature resolution plotted versus conversion time.

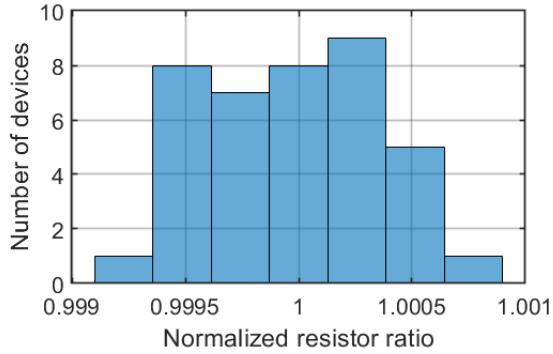


Fig. 15. Histogram of the normalized resistor ratios extracted from 40 sensors.

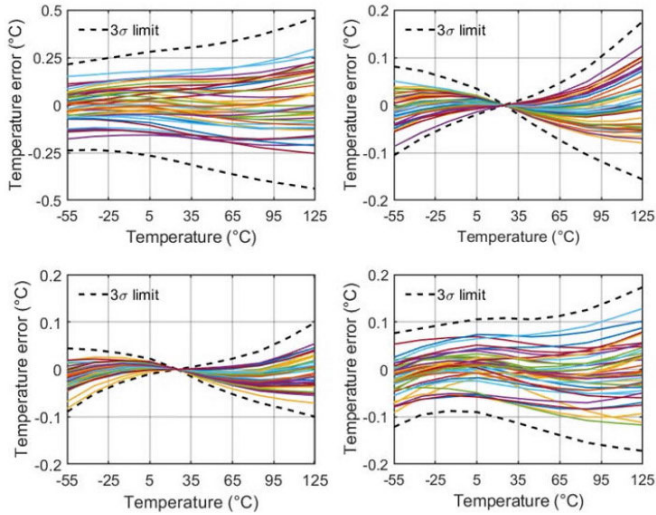


Fig. 16. Temperature spread of 40 sensors before trimming (top left), with RT trim (top right), with RT trim and resistor-ratio calibration (bottom left), with voltage- and resistor-ratio calibration (bottom right).

**D. Accuracy Measurements**

To determine the sensor’s accuracy, 40 sensors on 20 dies were characterized in a temperature-controlled oven, with the samples mounted in close thermal contact with a calibrated pt-100 thermistor. The batch-calibrated inaccuracy using the linearization technique discussed in Section IV-A is shown in Fig. 16 (top left). The sensor achieves an inaccuracy of  $\pm 0.45\text{ }^\circ\text{C}$  ( $3\sigma$ ), with a residual nonlinearity of  $\pm 0.015\text{ }^\circ\text{C}$  ( $\alpha \approx 11.44$ ). This improves to  $\pm 0.17\text{ }^\circ\text{C}$  ( $3\sigma$ ) after a RT trim (see Fig. 16, top right). After applying resistor-ratio calibration,

TABLE I  
ACCURACY-IMPROVEMENT TECHNIQUES

| CHOP       | CM DEM     | BJT DEM    | R-CAL      | Trimmed Inacc. ( $3\sigma$ ) <sup>1</sup> |
|------------|------------|------------|------------|---|
| <b>OFF</b> | ON         | ON         | ON         | $\pm 8.5\text{ }^\circ\text{C}$           |
| ON         | <b>OFF</b> | ON         | ON         | $\pm 4.0\text{ }^\circ\text{C}$           |
| ON         | ON         | <b>OFF</b> | ON         | $\pm 0.37\text{ }^\circ\text{C}$          |
| ON         | ON         | ON         | <b>OFF</b> | $\pm 0.15\text{ }^\circ\text{C}$          |
| ON         | ON         | ON         | ON         | $\pm 0.10\text{ }^\circ\text{C}$          |

<sup>1</sup>12 samples

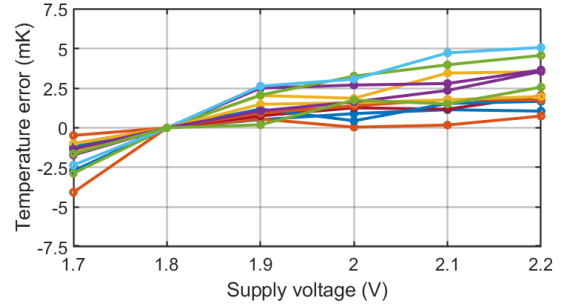


Fig. 17. Power supply sensitivity of 12 samples.

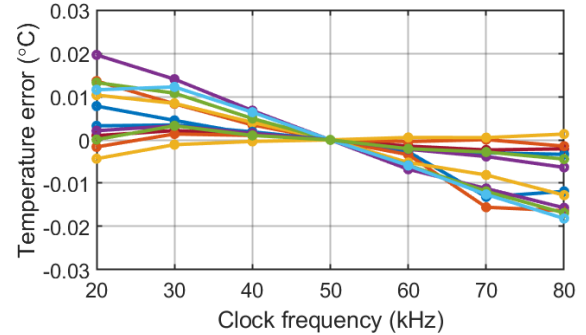


Fig. 18. Clock frequency sensitivity of 12 samples.

TABLE II  
BATCH TO BATCH VARIATION OF THE SENSOR AND BATCH CALIBRATION PARAMETERS

| Parameters                    | Batch 1                          | Batch 2                          |
|-------------------------------|----------------------------------|----------------------------------|
| $A$                           | 690.723                          | 691.017                          |
| $B$                           | 287.088                          | 287.093                          |
| $\alpha$                      | 11.44                            | 11.44                            |
| $n_e$                         | 1.00538                          | 1.00532                          |
| Untrimmed Inaccuracy          | $\pm 0.45\text{ }^\circ\text{C}$ | $\pm 0.78\text{ }^\circ\text{C}$ |
| 1-pt. Trimmed Inaccuracy      | $\pm 0.10\text{ }^\circ\text{C}$ | $\pm 0.10\text{ }^\circ\text{C}$ |
| Voltage-Calibrated Inaccuracy | $\pm 0.17\text{ }^\circ\text{C}$ | $\pm 0.22\text{ }^\circ\text{C}$ |

the target inaccuracy of  $\pm 0.1\text{ }^\circ\text{C}$  ( $3\sigma$ ) is achieved (see Fig. 16, bottom left). Replacing the temperature trim with low-cost voltage calibration increases the inaccuracy to  $\pm 0.17\text{ }^\circ\text{C}$  ( $3\sigma$ ) (see Fig. 16, bottom right), which is sufficient for many applications. Table I summarizes the effectiveness of each

TABLE III  
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

|   | JSSC'17<br>[4]                       | SSCL'22<br>[20]                     | ISSCC'14<br>[7]                      | ASSCC'19<br>[12]                     | ISSCC'23<br>[5]                      | ISSCC'20<br>[6]                     | This work   |
|---|--------------------------------------|-------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|---|
| <b>Sensor type</b>  | PNP                                  | NPN                                 | PNP                                  | NPN                                  | PNP                                  | NPN                                 | <b>PNP</b>  |
| <b>Architecture</b>   | DT $\Delta$ $\Sigma$                 | DT $\Delta$ $\Sigma$                | DCM                                  | CT $\Delta$ $\Sigma$                 | DT $\Delta$ $\Sigma$                 | CT $\Delta$ $\Sigma$                | <b>CT<math>\Delta</math><math>\Sigma</math></b>               |
| <b>Technology</b>   | 0.16 $\mu$ m                         | 0.18 $\mu$ m                        | 0.18 $\mu$ m                         | 0.18 $\mu$ m                         | 0.18 $\mu$ m                         | 0.11 $\mu$ m                        | <b>0.18<math>\mu</math>m</b>                                  |
| <b>Chip area [mm<sup>2</sup>]</b>   | 0.16                                 | 0.058                               | 0.8                                  | 0.35                                 | 0.25                                 | 0.2                                 | <b>0.12</b>   |
| <b>Supply current [<math>\mu</math>A]</b>   | 4.6                                  | 0.17                                | 55                                   | 5.5                                  | 0.81                                 | 550                                 | <b>9.5</b>  |
| <b>Supply voltage [V]</b>   | 1.5 to 2                             | 1.25                                | 1.25                                 | 1.6 to 2.2                           | 0.95 to 1.4                          | 1.125                               | <b>1.7 to 2.2</b>   |
| <b>Supply sensitivity [<math>^{\circ}</math>C/V]</b>                              | 0.01                                 | 0.07                                | 0.1                                  | 0.01                                 | 0.2                                  | -                                   | <b>0.01</b>   |
| <b>Temperature range</b>  | -55 $^{\circ}$ C to 125 $^{\circ}$ C | -15 $^{\circ}$ C to 85 $^{\circ}$ C | -45 $^{\circ}$ C to 130 $^{\circ}$ C | -40 $^{\circ}$ C to 125 $^{\circ}$ C | -55 $^{\circ}$ C to 125 $^{\circ}$ C | -35 $^{\circ}$ C to 95 $^{\circ}$ C | <b>-55<math>^{\circ}</math>C to 125<math>^{\circ}</math>C</b> |
| <b>3<math>\sigma</math> Inaccuracy [<math>^{\circ}</math>C] after a 1-pt trim</b> | $\pm 0.06^2$                         | $\pm 0.15$                          | $\pm 0.15^2$                         | $\pm 0.13^{2,3}$                     | $\pm 0.15$                           | -                                   | <b><math>\pm 0.1</math></b>                                   |
| <b>Relative inaccuracy [%]</b>  | 0.07                                 | 0.3                                 | 0.17                                 | 0.16                                 | 0.17                                 | -                                   | <b>0.11</b>   |
| <b>Resolution [mK]</b>  | 15                                   | 15                                  | 3                                    | 1.67                                 | 1.8                                  | 0.65                                | <b>1.1</b>  |
| <b>Conversion time [ms]</b>   | 5                                    | 50                                  | 2.2                                  | 218                                  | 128                                  | 0.72                                | <b>40</b>   |
| <b>Resolution FoM<sup>1</sup> [pJK<sup>2</sup>]</b>                               | 7.8                                  | 2.3                                 | 3.6                                  | 5.4                                  | 0.34                                 | 0.19                                | <b>0.85</b>   |

<sup>1</sup>FoM = Energy / Conversion  $\times$  (Resolution)<sup>2</sup> <sup>2</sup>After systematic non-linearity removal <sup>3</sup>After ADC gain and offset calibration

accuracy improvement technique on the trimmed inaccuracy of 12 samples. Among all the techniques applied, chopping shows the largest improvement, followed by current mirror DEM and BJT DEM, respectively. Resistor-ratio calibration has a small, but still significant, effect on the measured inaccuracy.

#### E. Power Supply and Clock Frequency Sensitivity

Fig. 17 shows the power supply sensitivity at RT of 12 samples as  $V_{DD}$  varies from 1.7 to 2.2 V. The average PSS is 0.01  $^{\circ}$ C/V, which is at par with the state-of-the-art.

Fig. 18 shows the sensor's sensitivity at RT to changes in clock frequency. As the clock frequency increases from 20 to 80 kHz, its sensitivity to switching transients increases. An average clock frequency sensitivity of 0.3 mK/kHz is found, which indicates that switching-transient related errors were successfully minimized.

#### F. Batch-to-Batch Measurements

The batch-to-batch accuracy was investigated by measuring sensors from different wafers and applying the same batch coefficients. Using the coefficients from batch 1 ( $\alpha$ ,  $A$ , and  $B$ ) results in a maximum untrimmed inaccuracy of  $\pm 0.95$   $^{\circ}$ C ( $3\sigma$ ) (see Fig. 19, top), which improves to 0.14  $^{\circ}$ C after resistor-ratio calibration and a RT trim (see Fig. 19, middle). Replacing the temperature trim with voltage calibration using the non-ideality factor ( $n_e$ ) obtained from batch 1 results in a maximum batch-to-batch inaccuracy ( $3\sigma$ ) of 0.22  $^{\circ}$ C (see Fig. 19, bottom). Table II shows the optimized batch parameters for both batches and the resulting inaccuracies. Averaging these parameters and applying them to both batches results in worst-case untrimmed, trimmed, and voltage-calibrated inaccuracies ( $3\sigma$ ) of 0.65  $^{\circ}$ C, 0.12  $^{\circ}$ C, and 0.20  $^{\circ}$ C, respectively.

#### G. Comparison to the State-of-the-Art

Table III summarizes the performance of the proposed sensor and compares it with that of other state-of-the-art

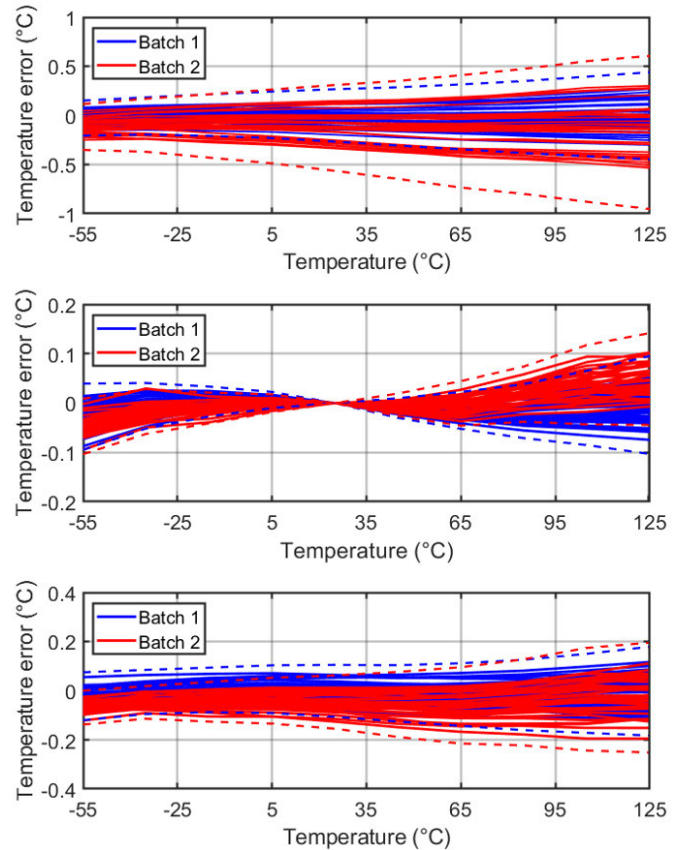


Fig. 19. Untrimmed inaccuracy of 2 batches (top), after resistor calibration and a temperature trim (middle), and after resistor- and voltage-calibration (bottom).

BJT-based temperature sensors that achieve similar accuracy (RIA < 0.2%) and/or energy efficiency [1]. The proposed sensor demonstrates excellent all-around performance, achieving both high accuracy and energy efficiency (see Fig. 20), while also achieving state-of-the-art power supply sensitivity and occupying only a small area.

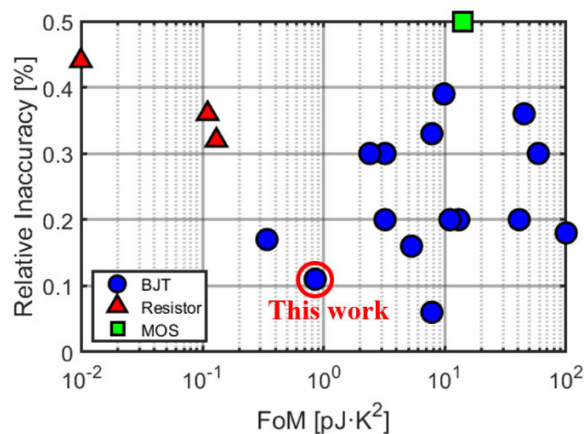


Fig. 20. FoM versus RIA after a 1-pt trim for state-of-the-art CMOS temperature sensors.

## VII. CONCLUSION

This work proposes a current-mode BJT-based temperature sensor employing a CT readout. The front-end and readout circuits were designed to achieve high energy efficiency. High accuracy is achieved by employing chopping and DEM to mitigate component mismatch, as well as a novel resistor-ratio self-calibration technique. Fabricated in a  $0.18\ \mu\text{m}$  process, the sensor occupies  $0.12\ \text{mm}^2$  and draws  $9.5\ \mu\text{A}$  from a  $1.7\ \text{V}$  supply. It achieves a resolution FoM of  $0.85\ \text{pJ}\cdot\text{K}^2$  and a 1-point trimmed inaccuracy of  $0.1\ \text{°C}$  ( $3\sigma$ ) from  $-55\ \text{°C}$  to  $125\ \text{°C}$ . This performance makes the sensor competitive with the state-of-the-art in terms of area, power supply sensitivity, energy efficiency, and accuracy.

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## REFERENCES

- [1] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Aug. 2023. [Online]. Available: [http://ei.ewi.tudelft.nl/docs/TSensor\\_survey.xls](http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls)
- [2] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a  $3\sigma$  inaccuracy of  $\pm 0.1\ \text{°C}$  from  $-55\ \text{°C}$  to  $125\ \text{°C}$ ," *IEEE J. Solid-State Circuits*, vol. 12, no. 40, pp. 2805–2815, Dec. 2005.
- [3] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of  $\pm 0.15\ \text{°C}$  ( $3\sigma$ ) from  $-55\ \text{°C}$  to  $125\ \text{°C}$ ," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.
- [4] B. Yousefzadeh, S. H. Shalmany, and K. A. A. Makinwa, "A BJT-based temperature-to-digital converter with  $\pm 60\ \text{mK}$  ( $3\sigma$ ) inaccuracy from  $-55\ \text{°C}$  to  $+125\ \text{°C}$  in  $0.16\text{-}\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, Apr. 2017.
- [5] Z. Tang, S. Pan, and K. A. A. Makinwa, "23.5 A sub-1 V 810 nW capacitively-biased BJT-based temperature sensor with an inaccuracy of  $\pm 0.15\ \text{°C}$  ( $3\sigma$ ) from  $-55\ \text{°C}$  to  $125\ \text{°C}$ ," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 22–24.
- [6] S. H. Shalmany et al., "A  $620\ \mu\text{W}$  BJT-based temperature-to-digital converter with  $0.65\ \text{mK}$  resolution and FoM of  $190\ \text{fJ}\cdot\text{K}^2$ ," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 70–72.
- [7] A. Heidari, G. Wang, K. A. A. Makinwa, and G. Meijer, "A BJT-based CMOS temperature sensor with a  $3.6\ \text{pJ}\cdot\text{K}^2$ -resolution FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 224–225.

- [8] G. C. M. Meijer, "An IC temperature transducer with an intrinsic reference," *IEEE J. Solid-State Circuits*, vol. SSC-15, no. 3, pp. 370–373, Jun. 1980.
- [9] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 6, pp. 795–800, Dec. 1976.
- [10] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Procedia Eng.*, vol. 5, pp. 930–939, Jan. 2010.
- [11] M. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. Huijsing, "A CMOS temperature sensor with a  $3\sigma$  inaccuracy of  $\pm 0.5\ \text{°C}$  from  $-50\ \text{°C}$  to  $120\ \text{°C}$ ," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers. ISSCC*, 2003, pp. 200–488.
- [12] R. K. Kumar, H. Jiang, and K. A. A. Makinwa, "An energy-efficient BJT-based temperature-to-digital converter with  $\pm 0.13\ \text{°C}$  ( $3\sigma$ ) inaccuracy from  $-40$  to  $125\ \text{°C}$ ," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 107–108.
- [13] N. G. Toth, Z. Tang, T. Someya, S. Pan, and K. A. A. Makinwa, "A BJT-based temperature sensor with  $\pm 0.1\ \text{°C}$  ( $3\sigma$ ) inaccuracy from  $-55\ \text{°C}$  to  $125\ \text{°C}$  and a  $0.85\ \text{pJ}\cdot\text{K}^2$  resolution FoM using continuous-time readout," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Feb. 2023, pp. 358–360.
- [14] M. Eberlein and H. Pretl, "A current-mode temperature sensor with a  $\pm 1.56\ \text{°C}$  raw error and duty-cycle output in  $16\ \text{nm}$  FinFET," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.
- [15] M. A. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS*. Dordrecht, The Netherlands: Springer, 2006.
- [16] M. A. Pertijs and J. H. Huijsing, "A sigma-delta modulator with bitstream-controlled dynamic element matching," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Sep. 2004, pp. 187–190.
- [17] M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa, and J. H. Huijsing, "Voltage calibration of smart temperature sensors," in *Proc. IEEE Sensors*, Oct. 2008, pp. 756–759.
- [18] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.
- [19] S. Pan and K. A. A. Makinwa, "A  $0.25\ \text{mm}^2$ -resistor-based temperature sensor with an inaccuracy of  $0.12\ \text{°C}$  ( $3\sigma$ ) from  $-55\ \text{°C}$  to  $125\ \text{°C}$ ," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3355, Dec. 2018.
- [20] T. Someya, V. van Hoek, J. Angevare, S. Pan, and K. Makinwa, "A  $210\ \text{nW}$  NPN-based temperature sensor with an inaccuracy of  $\pm 0.15\ \text{°C}$  ( $3\sigma$ ) from  $-15\ \text{°C}$  to  $85\ \text{°C}$  utilizing dual-mode frontend," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 272–275, 2022.



**Nandor G. Toth** (Graduate Student Member, IEEE) was born in Delft, The Netherlands, in 1997. He received the B.Sc. and M.Sc. degrees in electrical engineering from the Delft University of Technology, Delft, in 2018 and 2021, respectively, where he is currently pursuing the Ph.D. degree.

His research interests include mixed-signal design and smart sensors.



**Zhong Tang** (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 201 and 2020, respectively.

From 2019 to 2020, he was a Visiting Ph.D. Student with EEIC Group, Eindhoven University of Technology, Eindhoven, The Netherlands. From 2020 to 2023, he was a Postdoc Researcher with Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands. He is currently an Analog IC Designer with Vango

Technologies Inc., Hangzhou. He has authored or coauthored over 30 technical articles, including seven from the IEEE International Solid-State Circuits Conference (ISSCC) and five from the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC). His research interests include precision analog and mixed-signal integrated circuits.

Dr. Tang was a recipient of the Outstanding Doctoral Thesis Award of the Chinese Institute of Electronics in 2022 and the Best Speaker Award of Workshop on IC Advances in China (ICAC) 2024.



**Teruki Someya** (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from the University of Tokyo, Tokyo, Japan, in 2013, 2015, and 2018, respectively.

From 2018 to 2019, he was with Tokyo Institute of Technology as a Postdoc Researcher with the Department of Electrical and Electronic Engineering. From 2019 to 2022, he was a Postdoc Researcher with Electronic Instrumentation Laboratory, TU Delft. He is currently with SiTime Japan G.K., Tokyo. His research interests include low-

power sensor readout circuits, and low-noise frequency synthesizers.



**Sining Pan** (Member, IEEE) received the B.Sc. degree in electronic engineering from Tsinghua University, Beijing, China, in 2013, and the M.Sc. and Ph.D. degrees (cum laude) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016 and 2021, respectively.

He was a Post-Doctoral Researcher with the Electronic Instrumentation Laboratory, Delft University of Technology. In 2022, he joined the School of Integrated Circuits, Tsinghua University, as an Assistant Professor. He has authored and coauthored over 30

technical articles, including 13 from ISSCC and ten from IEEE JSSC. His research interests include smart sensors, CMOS frequency references, and Delta-Sigma modulators.

Dr. Pan was a recipient of the ADI Outstanding Student Designer Award in 2019 and the IEEE SSCS Predoctoral Achievement Award in 2020. He serves as a Technical Committee Member for ASSCC.



**Kofi A. A. Makinwa** (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands. Since 1999, he has been at the Delft University of Technology, where he is an Antoni van

Leeuwenhoek Professor and the Head of the Microelectronics Department. He has authored or coauthored over 20 books, 350 technical articles, and 30 patents. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors.

Dr. Makinwa was the Analog Subcom chair of ISSCC, and has served on the program committees of several other IEEE conferences. He has also been a distinguished lecturer of the Solid-State Circuits Society and an elected member of its Adcom. He is currently a member of the executive committee of the VLSI symposium and a co-chair of the Advances in Analog Circuit Design (AACD) workshop and the IEEE Sensor Interfaces Meeting (SIM). He is the co-recipient of 18 best paper awards from the JSSC, ISSCC and VLSI symposium, among others. In 2023, at the 70th anniversary of ISSCC, he was recognized as its all-time top contributor. He is a member of the Royal Netherlands Academy of Arts and Sciences.