# Orientation-and-Location Controlled Single-Grain TFTs on Glass Substrate

PROEFSCHRIFT

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aan de Technische Universiteit Delft,
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voorzitter van het College voor Promoties,
in het openbaar te verdedigen

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# Chapter 1

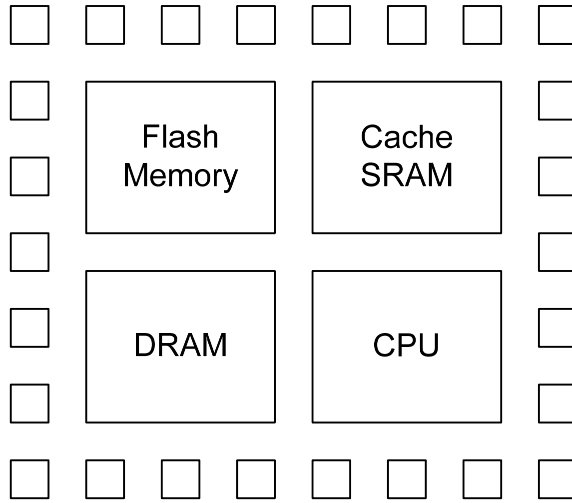
# Introduction

## 1.1 Overview of TFT technologies

Integrated Circuits (IC) chips are essential in every corner of modern society, from credit card security chips to sensors and controllers in large airplanes. Most of these chips are fabricated on single-crystalline Si wafers since single-crystalline Si is considered as defect free material and devices fabricated on single-crystalline Si wafer show good mobility, subthreshold swing value and uniformity, on/off ratio and stability under electrical and thermal stress.

Over the last 50 years, the performances of the ICs have been greatly improved by a faster speed, less power consumption and downscaling of the dimensions of ICs, which is described by Moore's law. However, the continuous downscaling of the minimum dimensions on the ICs will come to an end when they are below 10nm either due to physical limitations[1)] or high costs of the process[2)]. So, further improvement of conventional 2D IC is limited. Moreover, in modern IC designs, the speed of ICs is not only limited by the transistors, but also by the interconnects between transistors which caused the IC delay[3)]. It has been proposed to build IC in different layers and make interconnects between the layers which are called 3D ICs. Fig.1.1 shows a structure of traditional 2D ICs and 3D ICs. For conventional 2D IC, the blocks of different functions ICs are located far from each other when compared with 3D ICs. This requires longer wires to connection for 2D ICs which results in longer IC delay. For 3D ICs, active devices are fabricated in different layers and then vertically stacked. Thus the

integration density can be improved by having additional active layer. Moreover, the shorter interconnects of 3D ICs will further increase the speed of IC by reducing IC-delays which in turn reduce the power consumption.



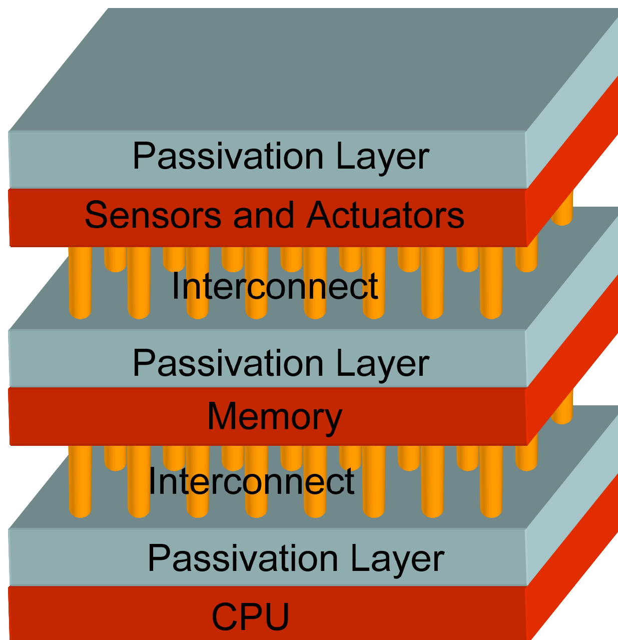




Fig.1.1 Structure of a 2D IC and 3D IC

Moreover, in traditional 2D ICs, it is difficult to integrate sensors and actuators which normally require MEMS technology and are not compatible with standard IC process. However, for 3D ICs, each layer can be processed separately by deposition passivation layer in between. Therefore, more functions can be integrated within one chip. Different technologies have been reported to fabricate 3D ICs. 3D packaging (system on chip) or wafer-level stacking is one of them by bonding the wafers[2)]. However, on the one hand, this technology is limited because of the high costs involved in single die handling. On the other hand, the reliability of the devices is poor due to either the mechanic damage during bonding or the etching process during thinning the Si wafer. Another way to fabricate 3D IC is monolithically by deposition and crystallization each active layer. The challenge is the quality of each active layer. As we known, most IC chips today are fabricated on single-crystalline Si wafers which are considered as defect free material. On the one hand, if the active layer is not single-crystalline layer, the performance of active device will be seriously deteriorated. For example, if the active layer has lots grain boundaries, the field effect mobility will decreased with increased value of subthreshold swing and leakage current. Moreover, if the surface and in-plane orientation of the active layer is random, it will result in variation in the field effect mobilities of electron and holes. On the other hand, it requires achieve high quality active layer at a low temperature to prevent “heat damage” to the active layer underneath. To epitaxially grown defect free Si layer, it requires process temperature above 950$^{o}$C. However, at 950$^{o}$C, the diffusion of dopants will be enhanced and the active device in the underneath layer will be destroyed.

Another limitation is in the field of flat panel displays driven by active matrix thin film transistors (TFT). High mobility TFT has attracted lots of interest to integrate controllers, sensors and functional circuits on displays which is called System-on-Glass (SOG). Fig.1.2 shows the structure of SOG which integrates displays with functional circuit blocks such as CPU, memories, sensor and actuators and RF circuits. By doing so, the thickness and total weight of the electronic device are greatly reduced which are very attractive for customers. It is possible to fabricate SOG by wafer transfer technology[4)]. However, the cost is too high due to its complicated process to

protect active layer of transistors during polishing and bonding the wafer on glass.

Thin film transistors (TFT) are commonly used to fabricate Si devices over a large area in LCD factories by direct depositing the active layer to fabricate transistors. In LCD factories, transistors are fabricated directly on glass over a large area (>100 inches) while in IC fabs transistors are fabricated on Si wafers with diameters up to 12 inches. So the cost to make an IC is hundred times more per unit area in standard IC fabs compared to LCD factories. Due to its low process cost as mentioned before, TFTs are very attractive to directly fabricate System-on-Glass and 3D-ICs. Originally, TFTs are widely used as switches in Liquid Crystal Displays, drivers for OLED, X-ray image sensors, SRAM. Recently, with the development of high mobility channel material of TFT, to fabricate System-on-Glass[3)] by TFT has attracted lots of new interest due to its low fabrication cost. Moreover, TFT technology is a good candidate to fabricate 3D ICs in a monolithic way. Each layer of 2D transistors is fabricated directly by TFT technologies and passivation layer is deposited in between. The interconnects between different active layer are made by making contact holes and filling with metal instead of mechanical bonding. Therefore, the advantages of fabricating 3D ICs by TFT technology over wafer bonding technology are easy integration, lower cost, and compatible with standard IC process. However, the major challenge to further applying TFT technologies to 3D-ICs and System-on-Glass is the performance of the transistors, especially field effect mobility of the transistors. The active layer to fabricate thin film transistors normally incorporate grain boundaries which will act as trap states for electrons and holes. Therefore, the field effect mobility is seriously deteriorated. Moreover, the surface and in-plane orientation of the active layer is random which will cause a large variation in field effect mobilities of transistors. Therefore, the uniformity of the devices is poor when compared with single-crystalline layer.

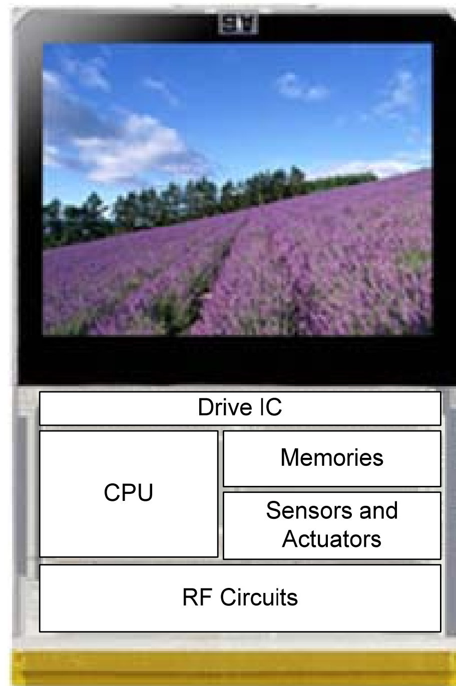



Fig.1.2 Structure of System-on-Glass

### 1.2 α-Si TFTs

Hydrogenated amorphous silicon was first used as a active channel material to fabricate TFTs for switches of LCD. Also α-Si is widely used as low cost solar cell material. The advantage of α-Si is the low temperature process (below 100$^{o}$C), good uniformity and low cost. However, the disadvantage of α-Si is its poor stability and low field effect mobility due to the large amount of dangling bonds which acts as recombination states of electrons and holes. The devices show considerable threshold voltage shift during operation. The low field effect mobility of α-Si TFT (~1cm$^2$/VS) constraints future application for OLED or high performance circuits.

## 1.3 Oxide semiconductors

Transparent conductive oxides are unique materials due to the fact that they are both electrically conductive and visually transparent. Initially, they are widely used as simple passive electrical or optical coatings, such as in antistatic coatings, touch display panels, solar cells, flat panel displays and optical coatings. Transparent conductive oxides such as indium-tin oxide (ITO) and ZnO have found applications as electrical interconnections and as window electrodes in flat panel displays and solar cells.

Recently zinc oxide has attracted lots interest in the application as channel material for TFTs. Single-crystal $InGaZnO_4$ TFT with mobility of 80 $cm^2/Vs$ and amorphous $InGaZnO_4$ TFT with mobility of $20cm^2/Vs$ have been reported. The advantages of ZnO based TFTs are higher mobility when compared with a-Si and better uniformity when compared with poly-Si. However, the lower mobility of ZnO TFTs when compared with poly-Si limits its further application for high performance ICs, such as RF circuits, logic circuits, analog amplifies etc.

## 1.4 Poly-Si TFTs

The motivation of using polycrystalline silicon (poly-Si) as channel material for TFTs is the higher field effect mobility ($50\sim300cm^2/Vs$) than that of α-Si which means that for the same on-current, the size of the poly-Si TFT is much smaller than that of α-Si. This results in higher aperture ratio and higher resolution for displays. Also the driver circuits can be integrated peripherally on displays due to the increased mobility of poly-Si TFT. Poly-Si TFT also shows better stability than that of α-Si TFT and it does not show threshold voltage shift under electrical stress. The high mobility and high electrical stability of poly-Si TFTs are very suitable for OLED switches which require TFTs with high drive current and good electrical reliability.

However, for small grain ($<1\mu m$) poly-Si TFT, the disadvantage is the low mobility ($<100Vs/cm^2$) due to dense grain boundaries inside and between grains in the channel region. The grain boundaries act as trap states

which decrease the field effect mobility of electrons and holes. For large grain (>1μm) poly-Si TFT, the disadvantage is the poor uniformity of the motilities due to the fact that location of the large grain size is random. Although there are several technologies to control the location of the large grains, the orientations of the large grains are still random.

In order to deposit high quality poly-Si, several technologies are proposed: direct deposition by CVD (Chemical Vapor Deposition); solid phase crystallization of α-Si by high temperature thermal annealing (>600°C) or MILC (metal induced lateral crystallization); liquid phase crystallization by laser crystallization such as zone melting regrowth (ZMR), and excimer laser annealing (ELA).

Laser crystallization of α-Si film can produce high performance poly-Si. However, if the laser energy is below complete melt (CM) of the a-Si film, the grains are small (<1μm) and the mobility is low (<100cm$^2$). If the laser energy is above CM, large grains (>1μm) are formed and the mobility can up to 300cm$^2$. However, the large grains are randomly located and the orientations of the grains are random which result in a high variation of the field effect mobilities.

*To improve the uniformity, one solution is to control the location of grains and different location controlled grain technologies are proposed. Location controlled poly-Si improves the uniformity in TFTs to some extent; however the uniformity is still not satisfying because the orientations of the grains are still random.*

## 1.5 Location controlled single grain TFTs by μ-Czochralski process (grain filter)

Location control of grain boundaries can improve the uniformity of poly-Si TFTs, especially if the grain is large enough to cover the active channel region of TFT. Such kind of TFTs is called Single-Grain TFTs (SG-TFT). The SG-TFT shows promising device performance which approaches that of SOI. Several techniques have been proposed: Sequential Lateral Solidification (SLS), CW-laser lateral crystallization (CLC), phase

modulated excimer laser annealing (PMELA) and μ-Czochralski. The μ-Czochralski has been first developed in the DIMES laboratories, TUDelft and the work of this thesis has been built on μ-Czochralski process. This process has many advantages over other processes, such as it can control the position of grains, it has higher electron and hole mobility than poly-Si and the device shows better reliability under electrical stress than poly-Si.

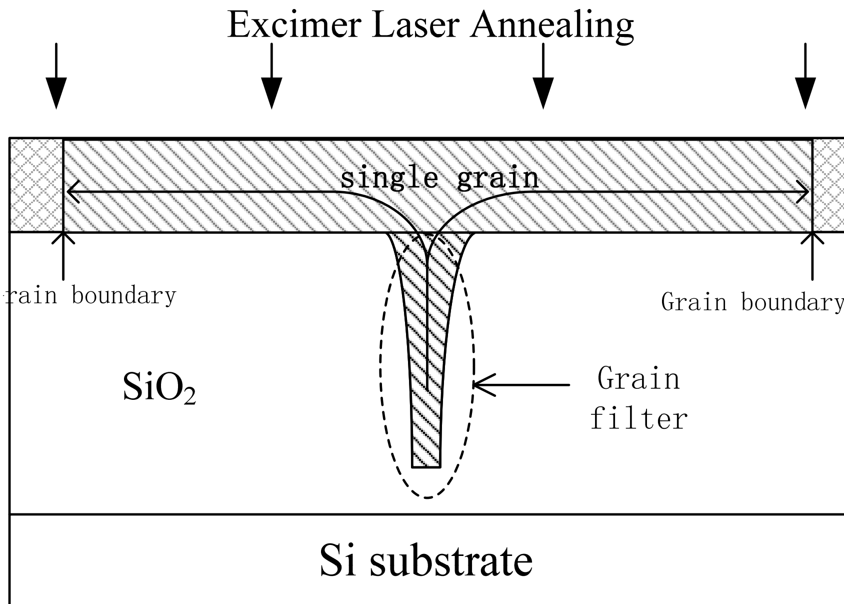



Fig. 1.3 Cross sectional structure of μ-Czochralski process (grain filter)

Figure 1.3 shows the cross section of the μ-Czochralski (grain filter). First, holes with diameter of 100nm wide and depth of 1μm are made inside $SiO_2$ by plasma etching and depositing second oxide. Then 250 nm a-Si was deposited by low pressure chemical vapor deposition (LPCVD). After that, the film was exposed by excimer laser. During excimer laser irradiation, explosive crystallization occurs first and propagates from the surface into the grain filter, producing small poly-Si grains inside the deep and narrow holes (grain filter). Then the secondary melt starts from the surface into the grain filter. The small poly-Si grains inside the grain filter has not been melted and act as seed layer. During solidification, large grains have

epitaxially grown on the poly-Si seed layer. Ideally, the grain filter should be narrow and deep enough so that one poly-Si seed layer can be "selected" during the epitaxial growth of the grain. During solidification, the grains start to grow vertically as well as laterally from the seed layer inside the grain filter. Lateral growth can continue until the liquid in the growth front reaches the critical supercooling temperature of nucleation. The location of the grains can be controlled by the grain filter.

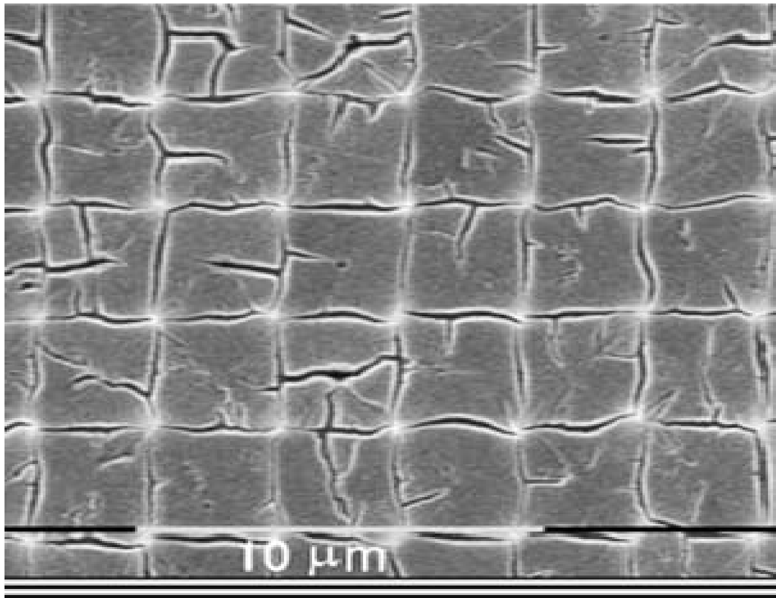



Fig. 1.4 SEM picture of location controlled grains by μ-Czochralski process (the sample have been etched to make the grain boundaries clear)

Figure 1.4 shows the SEM picture of location and orientation controlled grains. Uniform square grains with side length of 3μm have grown in predetermined positions. The TFTs fabricated inside location controlled single grain show a mobility of 600cm$^2$/Vs which is comparable with SOI. However, one challenge of the μ-Czochralski process is that the variations of the TFTs are more than 23%. The large variations in the TFTs further limit the average mobility of TFTs. This is because the mobilities of electron and hole depend on the crystal orientation of Si due to different effective mass.

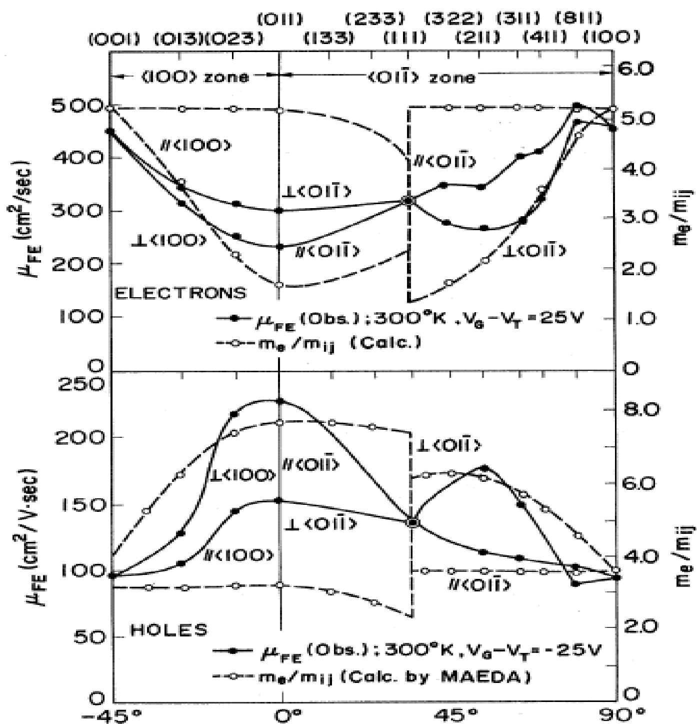



Fig. 1.5 Mobility dependence on the orientation[4]

Fig. 1.5 shows the dependence of the mobility on different orientations. It shows that different orientation of crystals have different electron and hole mobility. For field effective electron mobility, (001) oriented crystal with current flow perpendicular or parallel to <011> orientation has highest field effect electron mobility of 500cm$^2$/Vs while (011) oriented crystal with current flow parallel to <011> direction has lowest field effect electron mobility of 200cm$^2$/Vs. For field effective hole mobility, (011) surface oriented crystal with current flow perpendicular or parallel to (011) direction has highest field effect hole mobility of 250cm$^2$/Vs while (001) surface oriented crystal with (011) in-plane has lowest field effect hole mobility of 100cm$^2$/Vs. Fig 1.3 also shows that the variation in mobilities is higher than 40% with different surface crystal orientation and current flow directions. The seed crystals inside grain filter comes from explosive growth which has random orientation. Thus the grains epitaxial grown on these seed crystals have random orientation. Fig. 1.6 shows the EBSD mapping of grains after

μ-Czochralski process. From Fig.1.6, it has been observed that the orientations of the grains are random after μ-Czochralski process.

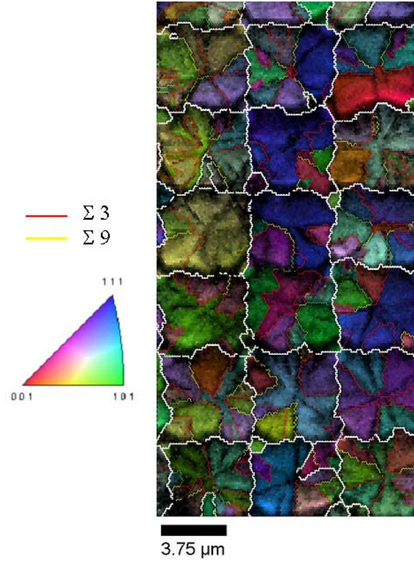



Fig. 1.6 EBSD mapping of grains after μ-Czochralski process.

## 1. 6 Motivation and Organization of this thesis

The goal of this thesis is to find and grow oriented seed crystals inside the grain filter to control the orientation of the single crystalline grains during μ-Czochralski process and fabricate orientation-and-location controlled SG TFTs with high field effect mobility and high uniformity. The thesis is organized as follows:

**Chapter 2 (111) oriented Si grown on (1000) $InGaZnO_4$ (IGZO)** will introduce different technologies to grow (0001) IGZO film on yttrium-stabilized zirconium (YSZ) or glass substrate. And epitaxial growth (111) oriented Si on (0001) oriented IGZO film has been performed.

**Chapter 3 (110) and (100) oriented poly-Si seed layer fabricated by Metal Induced Lateral Crystallization** will describe a new method to

grow both (110) and (100) poly-seed layer by metal induced lateral crystallization which has not been reported before.

**Chapter 4 (110) and (100) Orientation-and-Location Controlled Single Si Grain TFT without seed substrate** will describe how to fabricate (100) and (110) SG-TFTs by using MILC as seed layer on amorphous substrate ($SiO_2$). A novel process to remove Ni contamination has also been developed. A new process to reduce Ni contamination of MILC to a record low level so far will be proposed. The performance of orientation and location controlled SG-TFTs surpasses that of SOI which is very promising to fabricate high performance IC circuits on any substrate. Moreover, the orientation and location controlled SG-TFTs have shown excellent reliability under electrical stress which is comparable with single-crystalline Si MOSFET.

**Chapter 5 Location Controlled Single-Grain Ge TFTs Grown on MILC Si layer by μ-Czochralski process** will describe the challenges in Ge MOSFETs and propose a novel process by Single-Grain Ge on MILC Si seed layer combined with μ-Czochralski process. Also a novel device structure of SG Ge TFT will be proposed. World record Ge performance with high mobility and high on/off ratio has been achieved.

**Chapter 6 Conclusions and Recommendations** concludes the thesis with a summary and suggestions for future research.

# Chapter 2

# (111) oriented Si grown on (1000) $InGaZnO_4$ (IGZO)

In order to control the orientation of a single-grain, it is important to grow a seed layer inside the grain filter hole. (100), (110) and (111) are three major orientations of Si which are widely used to fabricate IC in today's IC fabs. Fig.2.1 shows the structure under consideration. In this chapter, it is proposed to grow $InGaZnO_4$ (IGZO) inside the grain filter as seed layer in order to control the orientation of single-grain Si to (111). In this way, the uniformity of mobility of single-grain TFTs can be improved. If successful, it is possible to fabricate high performance TFTs inside (111) oriented single-grains directly on glass.

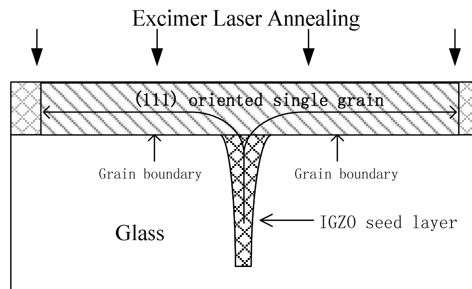



Fig.2.1 the structure of μ-Czochralski process

## 2.1 Introduction

Transparent conductive oxides are unusual materials due to the fact that they are both electrically conductive and visually transparent. They are widely used as simple passive electrical or optical coatings, such as in antistatic coatings, touch display panels, solar cells, flat panel displayers and optical coatings. Transparent conductive oxides such as indium-tin oxide (ITO) and ZnO have found applications as electrical interconnections and as window electrodes in flat panel displays and solar cells.

Recently many groups have reported various aspects of the development of zinc oxide based transparent transistors. Recently Nomura et.al[1)] demonstrated single-crystal $InGaZnO_4$ (IGZO) TFT with mobility of 80 $cm^2/Vs$, compared with 0.3 to 2.5$cm^2/Vs$ for ZnO based transparent transistors. Therefore IGZO attracts a lot of interest in applications for thin film transistor application due to its higher mobility and better uniformity compared with a-Si. Although the mobility is still lower than polycrystalline Si, the material exhibits good uniformity ~2% due to the fact that the channel material is single crystal without grain boundaries. It was also reported that the IGZO on glass substrate can easily be textured to [0001][2)]. This makes IGZO to be a good candidate as a seed layer for Si epitaxially grown for low temperature process.

In this chapter, it has been demonstrated that (111) oriented Si can epitaxially grown on a [0001] IGZO substrate. It has also been demonstrated that [0001] polycrystalline IGZO can be grown on $SiO_2$ by excimer laser crystallization at room temperature.

## 2.2 [0001] oriented single crystal $InGaZnO_4$

Single crystalline IGZO films have been deposited at the Tokyo Institute of Technology. Hereby I summarize the structure and major process steps of the deposition a single crystalline IGZO. Fig.2.2[(1)] shows a cross section structure of the $InGaZnO_4$. $InO_2^-$ analayers and $GaO(ZnO)_5^+$ blocks are alternately stacked along the <0001> axis. The layers are similar to those of

ITO and Ga doped ZnO, in which carrier doping is controlled by the amount of Ga.

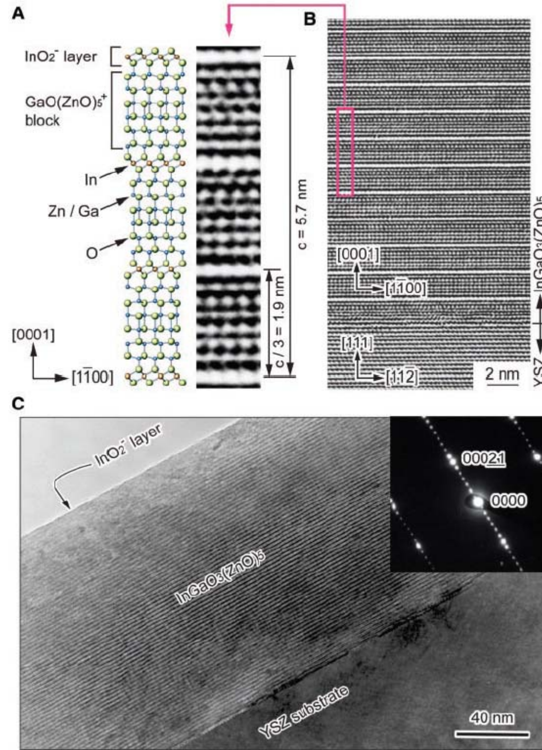



Fig.2.2 Structure of $InGaZnO_4$ (1)

This is because the $In_2O_3$ layer may work as a blocking barrier for oxygen out diffusion and thereby suppresses the formation of oxygen vacancies. Therefore it is easier to maintain the material in stoichiometry and control the carrier concentration down to the intrinsic level in a single crystal.

In order to fabricate single-crystalline IGZO, pulsed laser deposition (PLD) was first used to deposit a 2 nm-thick ZnO epitaxial layer at 700$^{o}$C on a (111) single-crystal yttrium-stabilized zirconium (YSZ) substrate as the template. YSZ is a special glass which has a higher melting temperature (1600$^{o}$C) compared with normal $SiO_2$ based glass substrate (<600$^{o}$C). Then 120-nm-thick $InGaZnO_4$ layer is deposited at room temperature. Next this layer is crystallized into [0001] single crystalline phase at 1400C during 30

min. During this anneal process, the structure was covered with a YSZ plate to suppress the evaporation of film components.

Fig.2.2 b-c shows cross sectional HRTEM images of IGZO thin film grown on YSZ (111) by reactive solid-phase epitaxy. Periodic stacking of the $InO_2^-$ layer and the $GaO^+(ZnO)_5$ block is clearly visible, which is also confirmed in the electron diffraction image. Single-crystalline film is formed over the entire observation area. The topmost layer of the film is the $InO_2^-$ layer.

## 2.3 [0001] oriented polycrystalline IGZO by excimer layer on $SiO_2$

Highly uniform [0001] $InGaZnO_4$ (IGZO) can be grown directly on YSZ glass substrate. It was also reported that the ZnO on glass substrate can easily be textured to [0001][(2)]. However, the crystallization temperature is 1400$^o$C which is not suitable to fabricate crystalline IGZO TFTs on flexible substrate for displays due to its low temperature process requirement (<150$^o$C). Excimer laser annealing (ELA), which can raise the temperature of IGZO films in a very short time (20ns), is effective to crystallize IGZO films without damage to the substrate. Since the crystallization time is very short during excimer laser annealing, few oxygen vacancies are generated which is very promising for fabricating high performance TFTs. The required YSZ glass (melting temperature >1600$^o$C) as seed layer which limits the application on normal glass substrate (<600$^o$C). Thus it is proposed to crystallize the IGZO film by excimer laser annealing on $SiO_2$ at room temperature.

Fig.2.3 shows the cross section: 1000nm $SiO_2$ is thermally grown on $SiO_2$ to isolate the film from Si substrate and prevent heat diffusion into substrate during excimer laser annealing. Then 50nm IGZO film is deposited by sputtering at room temperature. IGZO films were deposited in a gas mixture of argon and oxygen. The ratio of $O_2$ to Ar is 1:19. The RF power is 70W. The total gas pressure during the deposition is 0.55Pa. The samples are irradiated by a single shot XeCl excimer laser ($\lambda$=308nm). The distance between the target and the substrate was 75cm. The energy density of excimer laser is 600mJ/cm$^2$, 800mJ/cm$^2$ and 1000mJ/cm$^2$. The pulse width

is 20ns. The width and the length of the laser shot was 450 nm and 350 nm respectively. The irradiation was carried out at room temperature in vacuum chamber.

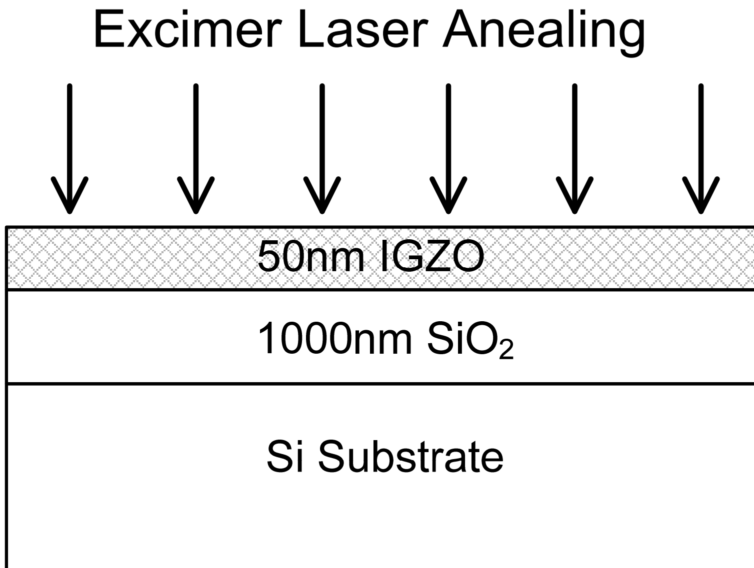



Fig.2.3 Structure of cross section

Fig.2.4 shows an X-Ray diffraction (XRD) analysis of excimer laser crystallized IGZO film. For the film thickness of 50 nm, no diffraction peaks due to the presence of IGZO crystals were observed at laser energy densities less of 600 $mJ/cm^2$, which suggests that the IGZO films remained amorphous in this laser energy range. In contrast, when the laser energy density was 800$mJ/cm^2$, diffraction peaks appeared, which indicated that the sample has been crystallized. From these results, it can be concluded that the crystallization threshold energy density for the 50 nm IGZO film was around 800$mJ/cm^2$. At laser energy of 1000$mJ/cm^2$, IGZO periodic diffraction peaks of (003), (006), (009), (0012), (0015), and (0018) has appeared which suggests that IGZO films with (001) surface orientation has been achieved. Also a $Zn_2SiO_4$ phase has been found which indicates that Zn silicate has been formed at interface between IGZO and $SiO_2$ film.

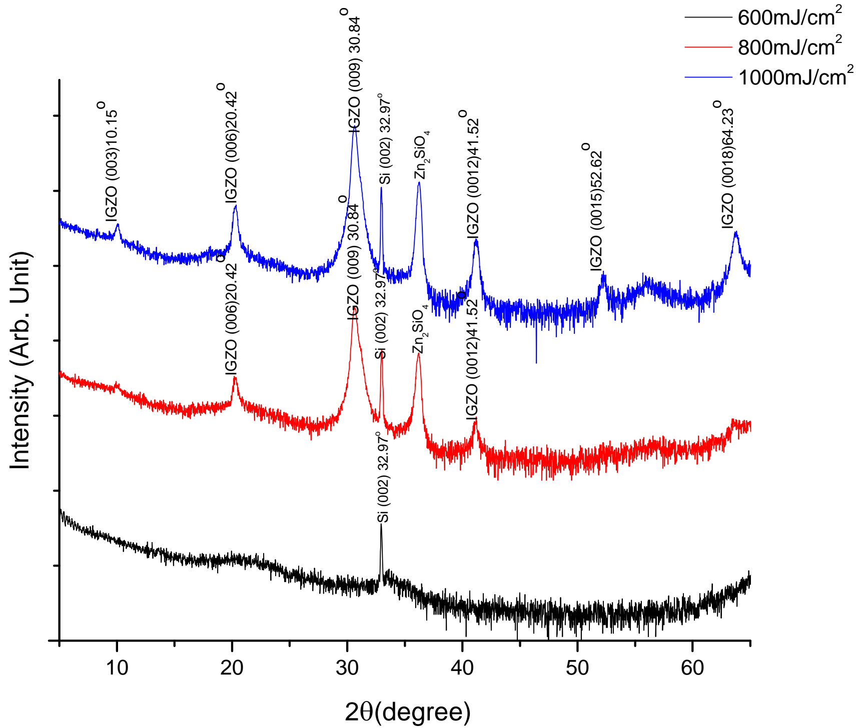
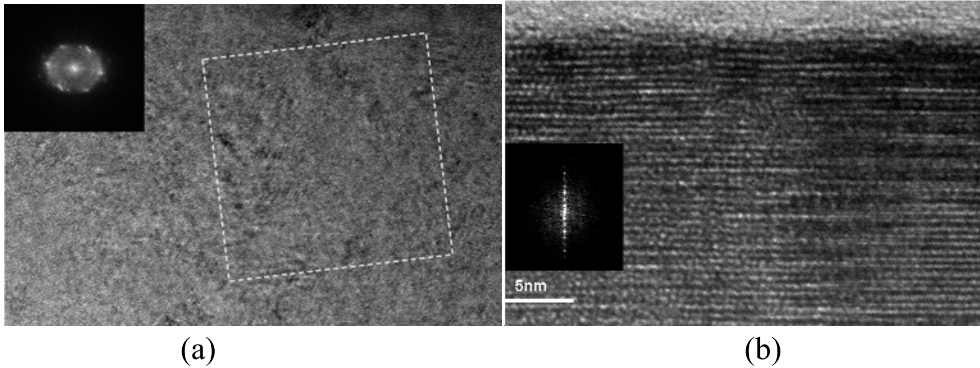



Fig.2.4 XRD measurements of IGZO film before and after ELC

Fig.2.5 (a)-(b) shows the Transmission Electron Microscopy (TEM) image of the IGZO films after excimer laser irradiation at energy of 600mJ/cm$^2$ and 1000mJ/cm$^2$ respectively. From the diffraction pattern and TEM image at low laser energy of 600mJ/cm$^2$ (Fig.2.5-a), it has been seen that the orientation of the film is random with grain boundaries. However, from the diffraction pattern and TEM image at the laser energy of 1000mJ/cm$^2$ (Fig.2.5-b), no defect structure such as grain boundary and dislocation over the entire film has been observed. The diffraction pattern shows that the film has (001) orientation which was correspondent with XRD result in Fig.2.4. The higher laser energy heat the IGZO film up to the crystallization temperature at which (001) oriented IGZO film has grown.




(a) (b)

Fig. 2.5 Transmission Electron Microscopy image of IGZO film after ELC

## 2.4 Epitaxial grown (111) oriented Si on [0001] IGZO

Conventional (111)-oriented solid-phase epitaxial growth[(3)-(5)] has been achieved by utilizing lattice-matched epitaxy during thin-film growth as long as the lattice misfit is less than 8%. On the other hand, J. Narayan et.al[(6)-(7)] has showed that a large lattice misfit relative to the substrate can still grow epitaxial layers, which is called 'domain matching epitaxy (DME)', where integral multiples of the lattice constants make a good lattice matching between the substrate and the over-grown layer[(8)]. DME occurs preferably if the surfaces of the substrate and the film have similar crystal structures (i.e. similar atomic configurations) and the chemical bonds between the substrate and the film is not so strong, which is the case for e.g. ionic crystals such as oxides. Many systems with a large misfit have been grown by DME[(9)-(13)]. This gives possibility that Si can grown epitaxially on a substrate even with a large lattice misfit >8%.

The DME is also the mechanism of epitaxial grown Si on IGZO. The lattice mismatch between Si and c-IGZO is larger than 20%, (111) oriented Si can still epitaxially grow on (0001) oriented c-IGZO by domain matching epitaxy (DME) [(8)]. Fig. 2.8 shows the crystal structure of the Si / c-IGZO sample. The InO2– layers and the $GaO(ZnO)_5^+$ blocks are alternately stacked along the (0001) axis. The (111) oriented Si surface has a three-fold rotational symmetry (a=0.3829nm). Moreover, the surface symmetry of

(0001) oriented c-IGZO (a=0.3299nm) is trigonal with a three-fold rotational symmetry. Epitaxial growth of Si (111) on c-IGZO (0001) occurs via matching 6 periods of Si and 7 periods of IGZO. This makes IGZO to be a good candidate as a seed layer for (111) Si epitaxial growth at a low temperature process.

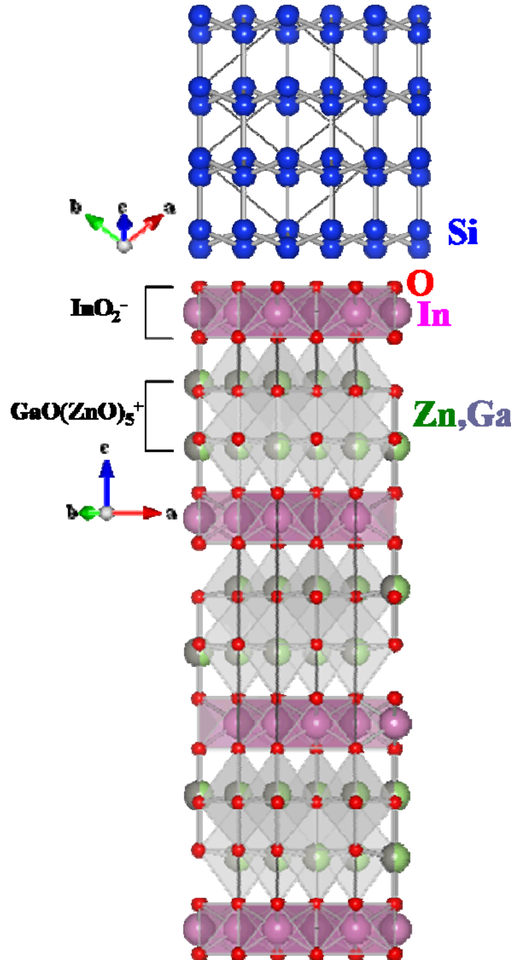
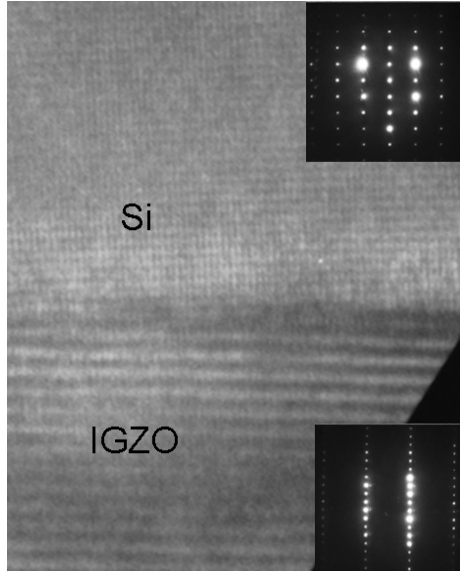



Fig. 2.6 Crystal structures of IGZO and Si

150 nm thick Si layer was deposited by physical vapor deposition (PVD) at 450°C on single-crystalline IGZO. Then the sample is annealed in a furnace at 950°C to crystallize the Si film. Fig. 2.7 shows a cross-sectional TEM image of the sample. With a lattice misfit of > 20% for Si epitaxy over

c-IGZO (0001), it is beyond the critical strain (8%) of conventional lattice matching. However, epitaxial growth of Si on c-IGZO is demonstrated by the concept of domain matching epitaxy. The diffraction pattern indicated that (111)-oriented Si is grown epitaxially on (0001)-oriented c-IGZO.




.Fig.2.7 TEM cross section of Si epitaxial growth on c-IGZO

A Philips XL50 SEM equipped with an EDAX- TSL Crystal EBSD system was used for EBSD analyses. The EBSD measurements were performed at an accelerating voltage of 25 kV with the spot size of 6nm. Pseudo-Kikuchi patterns were integrated for 0.03s, and the step for orientation mapping was about 0.2 μm step in each analysis point. The backscattered electrons from a Kikuchi pattern can be indexed to generate a unique description of the local orientation. The samples were tilted $75^{o}$ during the EBSD measurements. Fig. 2.8 (a) shows an EBSD mapping of the surface orientation of the Si film on the c-IGZO in the area of 1.2 x 1.5 $um^2$. It has been observed that the film has (111) orientation and no grain-boundary is found inside. Fig. 2.8 (b) shows a 001 pole figure and an inverse pole of the Si film. In the pole figure, one group of (111) orientation has been observed, which means that the in-plane orientation control has also been achieved.

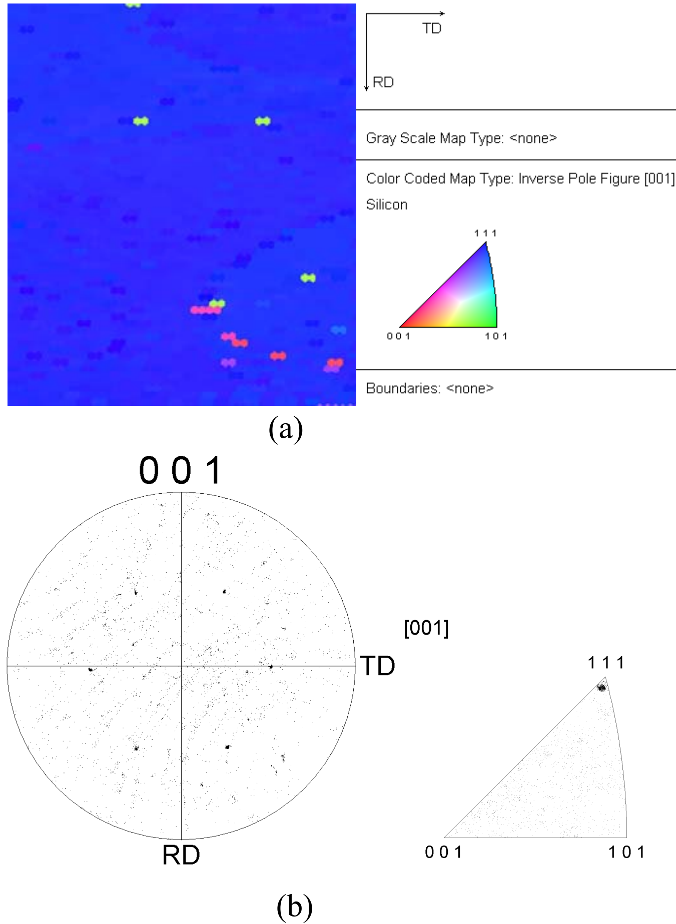



Fig. 2.8 Pole figure and inverse pole figure of Si by EBSD mapping

## 2.5 Conclusions and future research

In conclusion, it has been demonstrated that (111) single-crystal Si can epitaxially grow on an $InGaO_3(ZnO)_5$ layer by domain matching epitaxy (DME). By matching 6 planes of the Si with 7 planes of c-IGZO, it is possible to grow (111)-oriented crystal Si on (0001) c-IGZO substrate. The epitaxial temperature in this work is 950$^o$C. This suggests that the crystallization can be done by liquid phase crystallization (excimer laser) at

room temperature. However due to ablation of a-Si during the excimer laser irradiation, the process was not succeeded thus far.

It has also been demonstrated that [0001] IGZO films can not only grow on YSZ glass at 1100$^{o}$C by solid phase epitaxy but also on amorphous substrate such as $SiO_2$ by excimer laser crystallization at room temperature.

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# Chapter 3

# (110) and (100) Oriented Poly-Si Seed Layer Fabricated by Metal-Induced-Lateral-Crystallization (MILC)

It has been demonstrated that (111) oriented Si can epitaxial grown on IGZO. In this chapter, a new method to grow both (100) and (110) Si seed layer by Metal Induced lateral Crystallization (MILC) will be proposed which has not been reported before.

### 3.1 Motivation of this chapter

Fig.3.1 shows the motivation of this chapter. It is proposed to grow MILC inside the grain filter as seed layer in order to control the orientation of single-grain Si to (110) or (100). By controlling the orientation of single-grain to (110) or (100), the uniformity of mobility of single-grain TFTs can be improved. On the other hand, it is possible to fabricate (110) oriented PMOS which has highest hole mobility and (100) oriented NMOS which has highest electron mobility on same glass substrate.

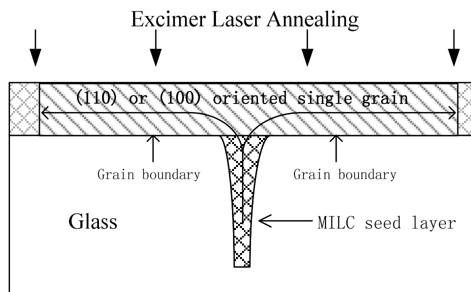


Fig.3.1 the structure of the motivation of this chapter

### 3.2 Introduction of MILC

Metal Induced lateral crystallization (MILC) can reduce the temperature of solid phase crystallization and decrease the time of crystallization. Ni first diffuses vertically and forms NiSi at temperature below 350°C. After annealing above 500°C, the NiSi changes into $NiSi_2$ silicides with <111> orientation due to small crystal mismatch[1)~3)] and the silicides will propagate laterally in all directions around the Ni pattern and crystallize film into needle like grains. Fig.3.2 (a)~(b) shows that (011) surface oriented crystal is perpendicular to four types of <111>. During lateral crystallization, due to the limited thickness of the film, only needles with direction parallel to the film can dominate the growth[3)] (Fig.3.2 (c)). Thus the surface orientation of MILC is (011)[3)]. Needles with other surface orientations are expected to

disappear during lateral growth. So this makes MILC a good candidate as seed crystal to control the orientation during μ-Czochralski process. However, during MILC process, Ni atoms have been trapped inside the MILC region[4)] which will be used as active channel region for TFT. Ni atoms increase the conductivity at the off-state of the TFT, therefore the leakage current is increased. Ni contamination in the film increases the off-current of TFT which limits its further application. In the next chapter, a novel process to remove Ni contamination in the device channel region will be proposed by etching away Ni contaminated MILC poly-Si layer and keeping MILC poly-Si only in the deep and narrow holes (grain-filter) as seed layer for laser crystallization.

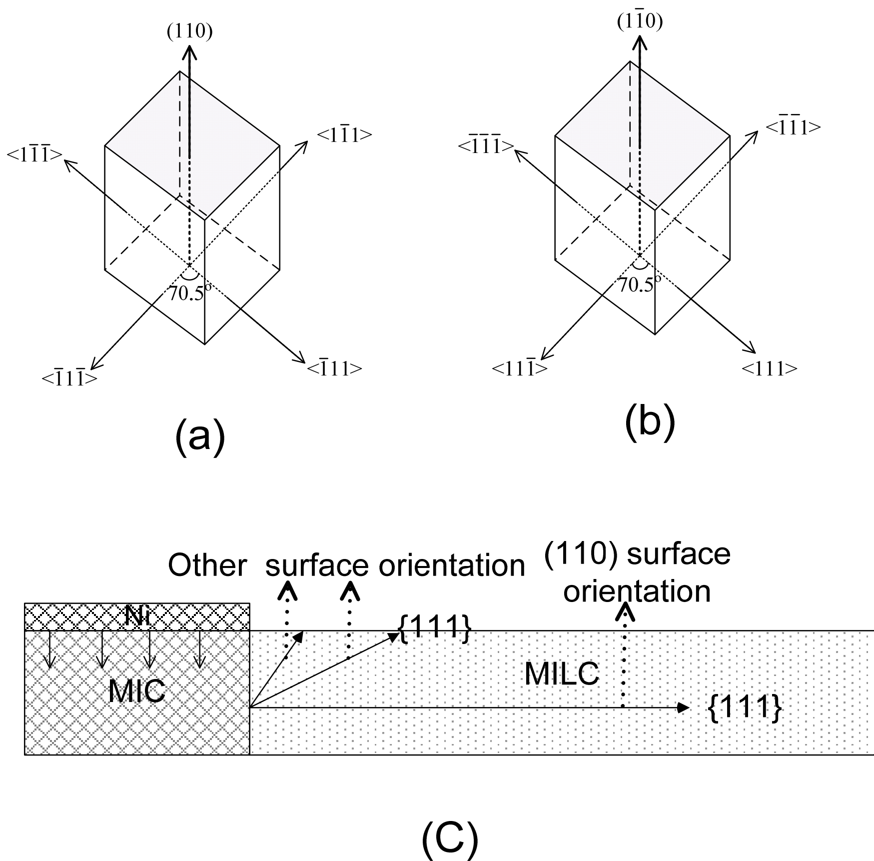


Fig.3.2 Schematic explanation of the MILC orientation

**3.3 Stress Induced (110) and (100) orientation control by MILC by Metal Induced Lateral Crystallization (MILC)**

It has been observed[5)~6)] that MILC can produce not only (110) oriented Si but also (100) oriented Si. Ni and Si first form NiSi after annealing at a temperature below 500°C[7)]. After the sample is further annealed above 500°C, NiSi changes into $NiSi_2$ which dominate the lateral crystallization. Reaction NiSi+Si→$NiSi_2$ is known to result in a total volume contraction of ~12%[8)]. This contraction will result in tensile stress in the film. The stress distribution depends on the pattern of the Ni which forms silicides. Fig.3.3 shows simulation of the stress distribution in X-Y plane. The Young's Module of the a-Si is $(6.2\pm2.5)*10^{11}$ dyn/cm$^2$. The Poisson ratio (υ) of the a-Si is 0.22. Using these values, 1Gpa tensile stress has been applied to a rectangle shaped pattern of 20μm*30μm which is the area for Ni deposition and the origin of the tensile stress. The stress value is set arbitrate in order to see the stress distribution over the whole area. And it has been assumed that Ni forms silicides uniformly inside the rectangle at the beginning. From simulation, it shows that the tensile stress is higher at the corner than along the side of the rectangle.

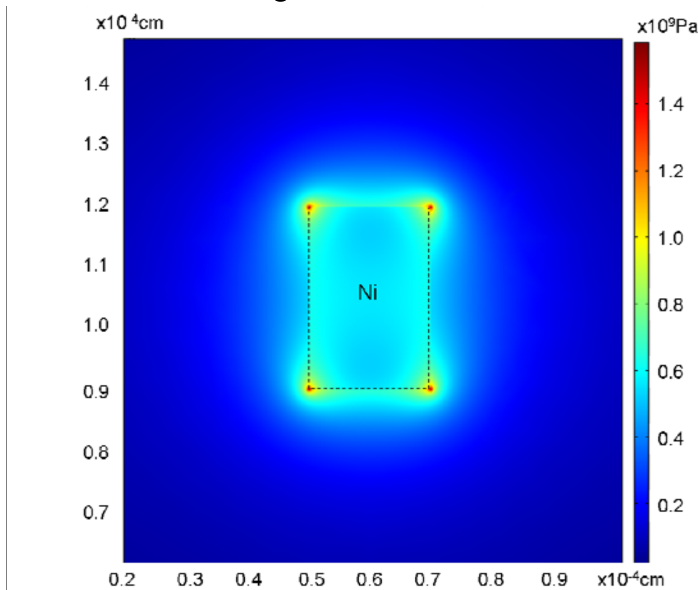


Fig.3.3 Simulation of the stress distribution after MILC

To verify this simulation, MILC sample is prepared in the following ways: 250-nm-thick amorphous Si was deposited on 100nm $SiO_2$ by low pressure chemical vapor deposition (LPCVD) at 545°C using pure $SiH_4$. Then 400-nm-thick $SiO_2$ was deposited by plasma-enhanced chemical vapour deposition and patterned for Ni deposition. 10-nm-thick Ni was sputterred by physical vapor deposition (PVD) and pre-annealed at 450°C in vacuum for 15mints to form NiSi. Unreacted Ni and $SiO_2$ were etched away by 50% $H_2SO_4$ and BHF consequentially. The sample is further annealed in the furnace at 600°C for 4 hours. During this time, NiSi changes into $NiSi_2$ and MILC poly has formed.

Fig.3.4 is a microscope picture of micro-Raman measurement position. It has been observed that Raman shift at the corner is lower than that away from the corner which indicates that the Ni corner induces a higher tensile stress. The result is in agreement with the stress simulation which is shown in Fig.3.3. I calculated the tensile stress difference from Raman shift by using the relation: $\sigma$ (Pa) = $\Delta\omega$ ($cm^{-1}$)$*5*10^8$ =250MPa [9].

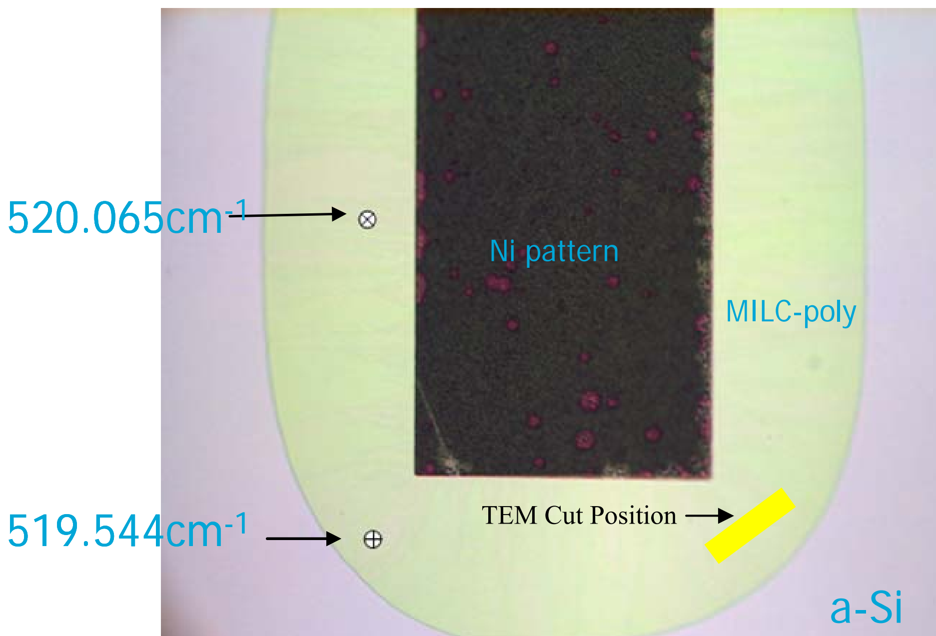


Fig.3.4 Microscopic picture of the Raman measurement position

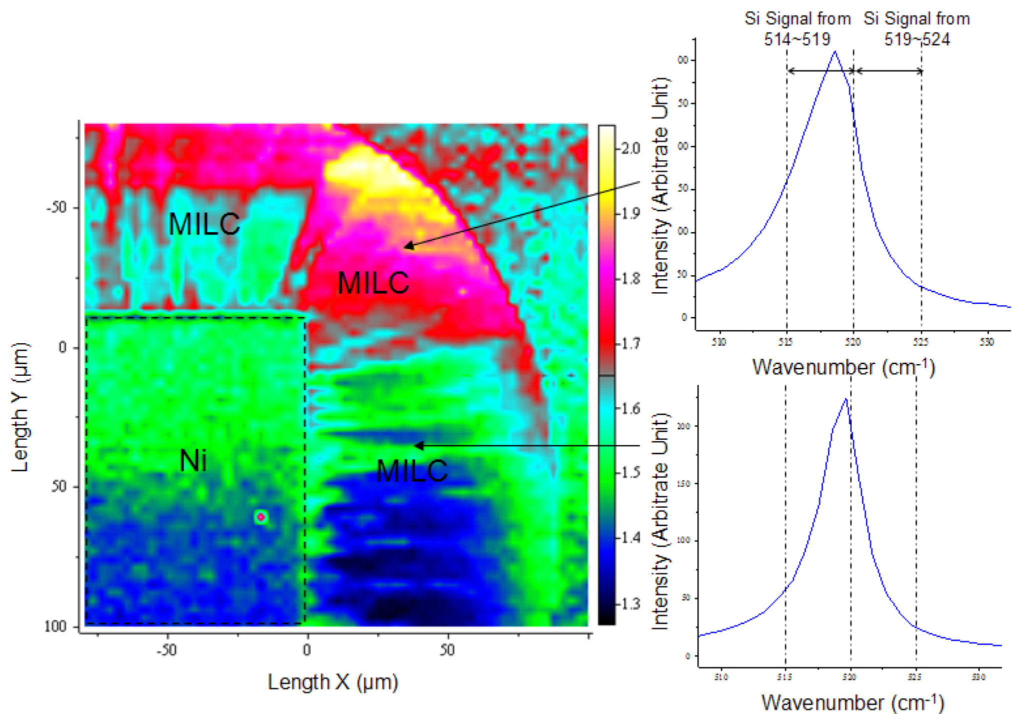


Fig.3.5 Raman mapping of the stress

Intrinsic Si which is stress free has a signal of 519.55 $cm^{-1}$. And if the Si signal is below 519.55 $cm^{-1}$, the Si has tensile stress. On the other hand, if the Si signal is above 519.55 $cm^{-1}$, the Si has compressive stress. The Si peak of the Raman shift is normally from 514.33$cm^{-1}$ to 524.76$cm^{-1}$. The right part of Figure 3.5 shows the Raman measurement of the MILC region, at the Ni corner and at the side of Ni. It is difficult to calculate the peak of the Raman shift over a large area because I have to calculate the peak of Raman signal intensity from every point of measurement. So, in order to map the stress distribution over a large area, I averaged the integration of the Si signal 1) from 514.33 to 519.55 $cm^{-1}$ and 2) from 519.55 to 524.76 $cm^{-1}$. Then I plot the ratio of the Si signal averaged from 514.33 - 519.55 $cm^{-1}$ to that from 519.55 - 524.76 $cm^{-1}$. If the ratio is higher than 1, it means that the intensity of Si signal from 514.33 to 519.55 $cm^{-1}$ is higher than that from 519.55 to 524.76 $cm^{-1}$ which indicates the peak of Raman shift is in the region from 514.33 to 519.55 $cm^{-1}$ and tensile stress has induced (see figure 3.4 (b)). The higher the ratio, the higher tensile stress is induced. On the

other hand, if the ratio is less than 1, compressive stress is induced. The higher ratio at the corner indicates higher tensile stress. Figure 3.4(a) shows Raman microscope mapping of Si stress by plotting the ratio of Si signal averaged from 514.33 - 519.55 $cm^{-1}$ to that from 519.55 - 524.76 $cm^{-1}$. The ratio of the Si signal is higher at the corner of rectangular Ni pattern than that at the side of rectangular Ni pattern which means the tensile stress at the corner of rectangular Ni pattern is higher than at the side of rectangular Ni pattern.

### 3.4 Helmholtz free energy (F):

In this session, Helmholtz free energy will be introduced and used to explain the growth of (100) and (110) oriented Si by MILC due to different tensile stress.

The Helmholtz free energy is a thermodynamic potential which measures the "useful" work obtainable from a closed thermodynamic system at a constant temperature and volume. For such a system, the negative of the difference in the Helmholtz energy is equal to the maximum amount of work extractable from a thermodynamic process in which temperature and volume are held constant. Under these conditions, it is minimized at equilibrium. Changes in free energy can be used to judge whether changes of state can occur spontaneously. Under constant temperature and volume, the transformation will happen spontaneously, either slowly or rapidly, if the Helmholtz free energy is smaller in the final state than in the initial state—that is, if the difference in the free energy ($\Delta F$) between the final state and the initial state is negative. Equation2.1 shows the relationship between the strain and final free energy[10)]:

$$F = F_o + E_{strain} \qquad 2.1,$$

Where $F$ is final free energy, $F_0$ is free energy without strain and $E_{strain}$ is the free energy change due to strain

The absolute value of the difference in free energy between c-Si and a-Si, $\Delta F$[11)] is

$$\Delta F = \left| F^{c\text{-}Si} - F^{a\text{-}Si} \right| = \Delta F_0 - \Delta E_{strain} \qquad 2.2,$$

Where $F^{a-Si}$ and $F^{c-Si}$ are Helmholtz free energies of a-Si and c-Si respectively, $\Delta F_0$ is the absolute value of the difference of Helmholtz free energy in which strain energy is not taken into account and $\Delta E_{strain}$ is the difference of strain energy introduced by MILC process. $\Delta F$ is the driving energy of crystallization under stress. $\Delta E_{strain}$ can be positive, which means that $\Delta F$ is smaller than the driving energy $\Delta F_0$ under no stress condition, and the crystallization is suppressed. The crystallization occurs slowly when the introduced stress does not relax. When $\Delta F$ is larger than $\Delta F_0$, the introduced stress relaxes similar to the case of strain-anneal method because relaxation of stress $E_{strain}^{c-Si} = 0$, that is , $\Delta E_{strain} < 0$. It has been reported that the MILC process introduces tensile stress[8)], which means $\Delta E_{strain} < 0$. Therefore the temperature of the MILC process can be lower than that of pure thermal crystallization[1)~3)].

Moreover, the nucleation rate N and the growth rate of a nucleus u are given by equation 2.4, 2.5 respectively [(10)]:

$$N \propto \exp\left( -\frac{F_a + \Delta F_r^*}{k_B T} \right) \qquad 2.3$$

$$u \propto \exp\left( -\frac{F_a}{k_B T} \right) \left\{ 1 - \exp\left( -\frac{\Delta F}{k_B T} \right) \right\} \qquad 2.4$$

Where $F_a$ is the activation energy for the transfer of Si atoms from amorphous phase to crystal phase and $F_a >> E_{strain}$ . $\Delta F_r^*$ is the energy necessary for the radius of a c-Si particle to grow larger than the critical radius $r^*$, and it is expressed by equation 2.5 when the shape of a c-Si particle is a sphere[11)].

$$\Delta F_r^* = \frac{16\pi\sigma^3}{3\Delta F^2} \qquad 2.5$$

Although it is difficult to calculate the absolute free energy since it depends on the atomic structure, annealing temperature, film thickness,

stress etc, it has been simulated by others[11] that there is dependence of the orientation on the relative change of free energy. Fig.3.6 is taken from ref.11 which shows the relationship between different orientations and the free energy during secondary growth of Si. It has been shown that in order to have (100) or (001) orientation during crystallization, higher free energy is required when compared to (110). And (111) requires lowest free energy. From Equation 2.2, 2.5, it can be seen that the tensile stress can increase the free energy and increase the grain size. Thus I suggest the grains with specific crystallorgraphic orientations are favored by strain-energy-density-minimization[12].

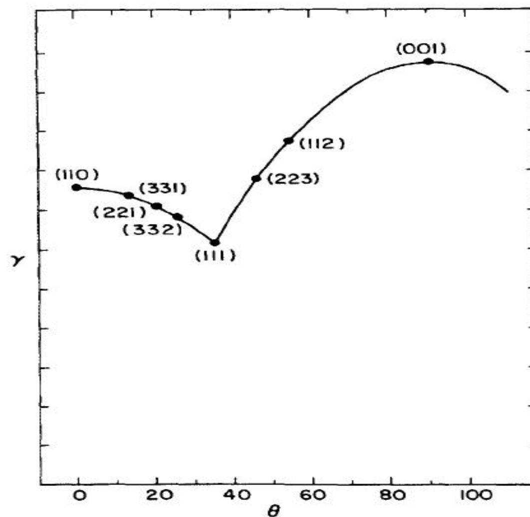


Fig.3.6 Free energy as a function of orientation [3]

In the first step needles with {111} orientation grow in all direction along the film near the corner of MIC region, thus the film is crystallized with random surface orientation (Fig.3.7a)); In the second step the needles with surface orientation of (001) are favored at the corner of rectanglar Ni pattern due to the higher tensile stress resulting into recrystallization of the film with (001) surface orientation (Fig.3.6b). The needles with surface orientation of (110) are favored at the side of rectanglar Ni pattern due to less stress (Fig.3.6c). In the final step, the (001) oriented needles are reflected by the top and bottom of the film which leads to the propagation of

(001) oriented needle along the film. At meantime, (110) oriented needles grow parallel along the film. Thus it can be concluded that the needles with different orientation are favored due to different tensile stress at the corner of rectanglar Ni pattern and at the side of rectanglar Ni pattern. And needles with (001) orientation keeps growing along the film by being reflected at the bottom and surface of the film while needles with (011) orientation grow parallel along the film.

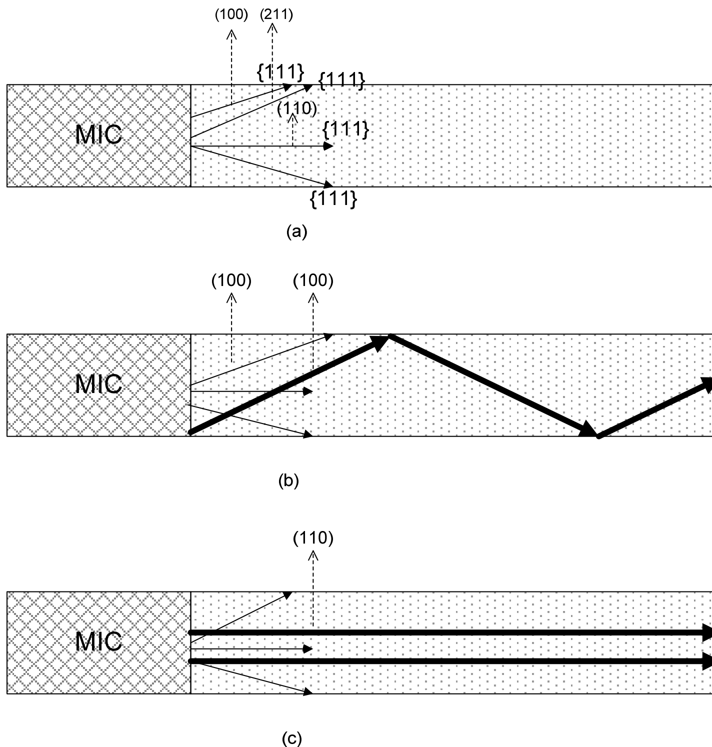


Fig.3.7 Mechanism of different orientation control by MILC

This mechanism is supported experimentally by EBSD measurement. Fig.3.9 is an EBSD mapping of the MILC region at the corner of rectangular Ni pattern. It can be seen that the orientation starts to change from (110) (green) to (100) (red). Cross sectioned the sample at the corner of the Ni pattern has been prepared to further investigate the details of the orientation at the Ni corner. Fig 3.10 shows TEM bright field images of the cross section of MILC poly-Si at the corner and its diffraction pattern. The

position of TEM cut is shown in fig 3.9. The electron-diffraction pattern indicates that orientations of the MILC crystallites are (001), (106) (105) and (117), which are all in (100) directions within 10 degree misorientation. From Fig. 3.8 it can be concluded that (100) oriented Si grows from the corner of the rectangular Ni pattern while (110) oriented Si grows from the side of rectangular Ni pattern.

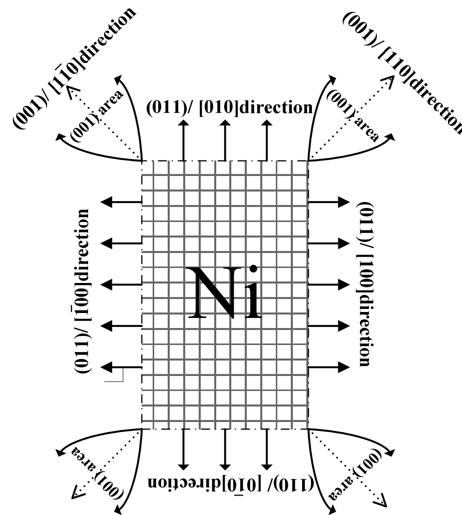


Fig.3.8 Structure of different oriented poly-Si grown byMILC

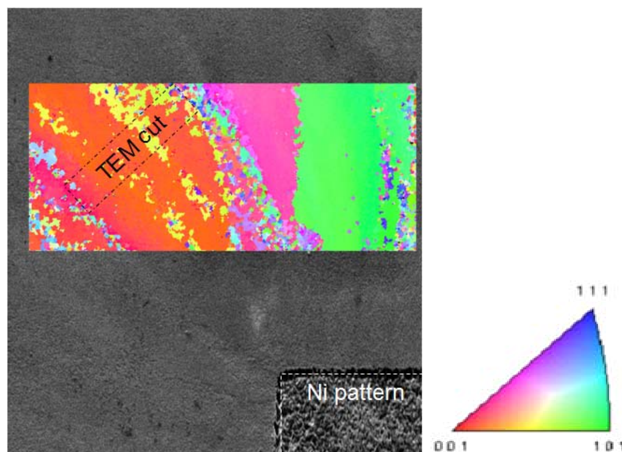


Fig. 3.9 EBSD mapping of rectanglar Ni pattern

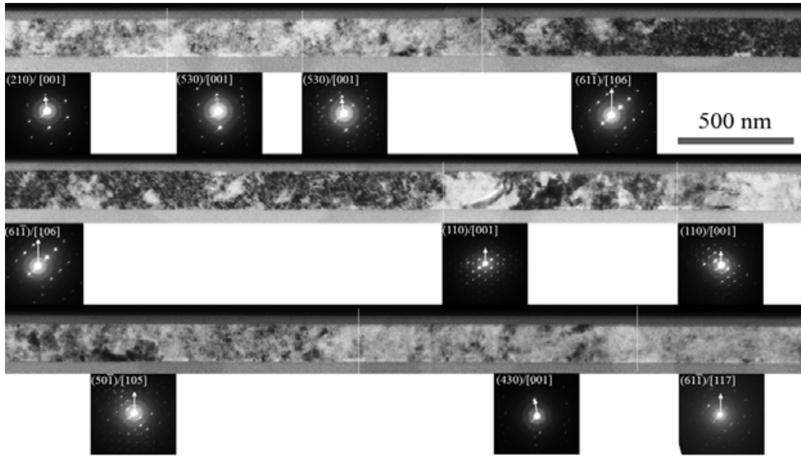


Fig. 3.10 TEM cross section image of the MILC at the corner of Ni pattern (The diffraction pattern at each location is shown below the TEM cross section.)

In order to obtain (100) orientation over large area, a multi-trangle Ni pattern has been designed. Fig.3.11 is an EBSD mapping of MILC poly. Light gray triangles are Ni deposition region. The remaining area is MILC polysilicon. EBSD mapping has only been done for the colored area. It can be seen that the (100) orientation grows explosively from the tips of the nickel triangles. Between the tips of the triangles there is still a small portion of (110) polysilicon which is caused by lower tensile stress during the MILC process.

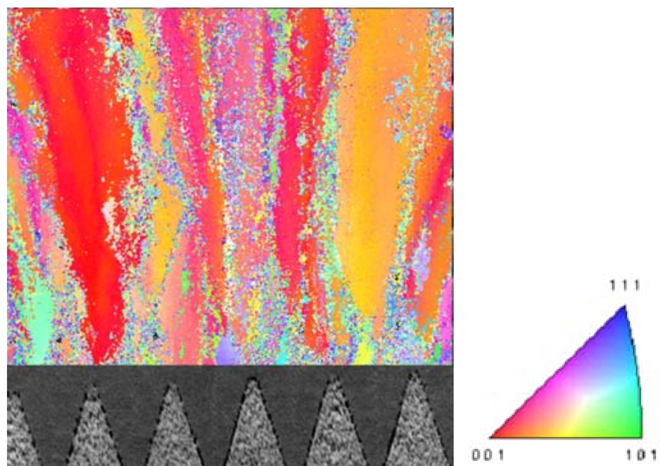


Fig.3.11 EBSD mapping of MILC polysilicon.

### 3.5 Conclusions

It has been shown that (100) and (110) oriented Si can be grown by Metal Induced Lateral Crystallization by designing special patterns to control the tensile stress. However, an important issue in the MILC process is Ni contamination. It has been reported that TFT leakage currents increase dramatically already by 2 orders of magnitute with a Ni concentration of 1ppm. Therefore a new process reducing the Ni contamination to record low level has been developed. This procees is described in the next chapter.

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# Chapter 4

# (110) and (100) Location and Orientation Controlled Single Si Grain TFT without seed substrate

In chapter 3, it has been demonstrated that MILC can produce (110) and (100) poly-Si layer on a glass substrate. However, the MILC process introduces Ni contamination which will increase the leakage current of device considerably and deteriorates the reliability of the devices under electrical stress. In this chapter, a novel process to remove Ni contamination in the device channel region will be first developed by etching away Ni contaminated MILC poly-Si layer and keeping MILC poly-Si only in the deep and narrow holes (grain-filter) as seed layer for laser crystallization. Next a new a-Si layer is deposited and laser crystallization is performed afterwards. During laser crystallization (110) and (100) oriented single Si grains are epitaxially grown on the MILC seed layer inside the grain-filter holes. By designing the nickel pattern, orientation- and location- controlled single-grain Si TFTs with one single orientation have been fabricated. The electron and hole mobilites of orientation-and-location controlled SG-TFT surpasses that of SOI. At the same time the spread in the TFT mobilities have been improved. The orientation- and location-controlled SG TFT shows remarkable stability under electrical stress which is comparable with single-crystalline MOSFET.

## 4.1 (110) and (100) oriented single Si grains by combining MILC and μ-Czochralski process

### *4.1.1 Grain filter and MILC process*:

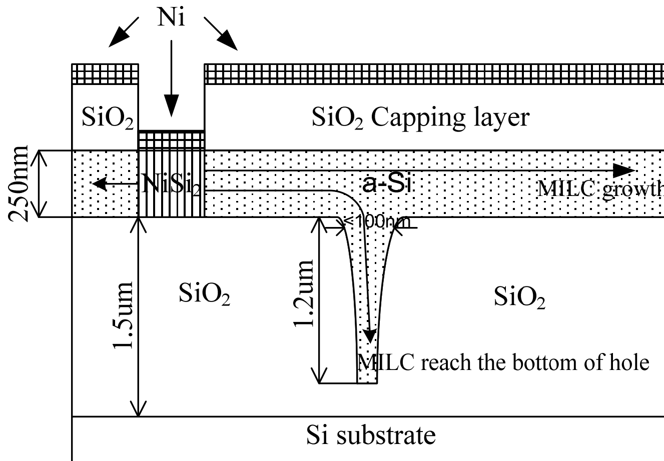



Fig. 4.1.1 schematic cross section of the MILC structure

Figures 4.1.1 show the sample structure used in this study. First, 750nm $SiO_2$ was grown by thermal oxidation on a Si wafer and patterned into grids of 1μm holes by reactive ion etching (RIE). Subsequently, a $SiO_2$ layer was deposited by plasma enhanced chemical vapor deposition (PECVD) using tetraethylorthosilicate (TEOS) and oxygen at 350$^{o}$C. After this process, the diameter of the large cavity was decreased to 100 nm. Then 250 nm a-Si was deposited by low pressure chemical vapor deposition (LPCVD) using $SiH_4$ at 545$^{o}$C. 300 nm thick $SiO_2$ was deposited by PECVD as a capping layer and window was opened by RIE for Ni sputtering. After the deposition of 10nm thick Ni by physical vapor deposition (PVD) at 50$^{o}$C, the wafer was directly preannealed in the vacuum chamber at 500$^{o}$C for 20 min in order to form Ni silicides. Subsequently, Ni was removed by a mixture of sulfuric acid and water peroxide ($H_2SO_4$: $H_2O_2$=1:1). Then the sample was further annealed at 600$^{o}$C for 4 h in $N_2$ ambient for MILC. As the distance of lateral crystallization by MILC can be as long as 60μm and the maximum total length of the grain filter is 30μm. Thus the nickel deposition position is designed to be 20μm away from the grain-filter matrix to ensure on the one

hand that the array is fully crystallized and at the other hand the array is not too close to the nickel area.

Figure.4.1.2 shows a cross sectional TEM image of a grain filter area after MILC (before excimer laser irradiation). It can be observe that a hole, whose width is approximately 100 nm and whose depth is approximately 1µm, was formed and the Si film is completely crystallized by MILC.

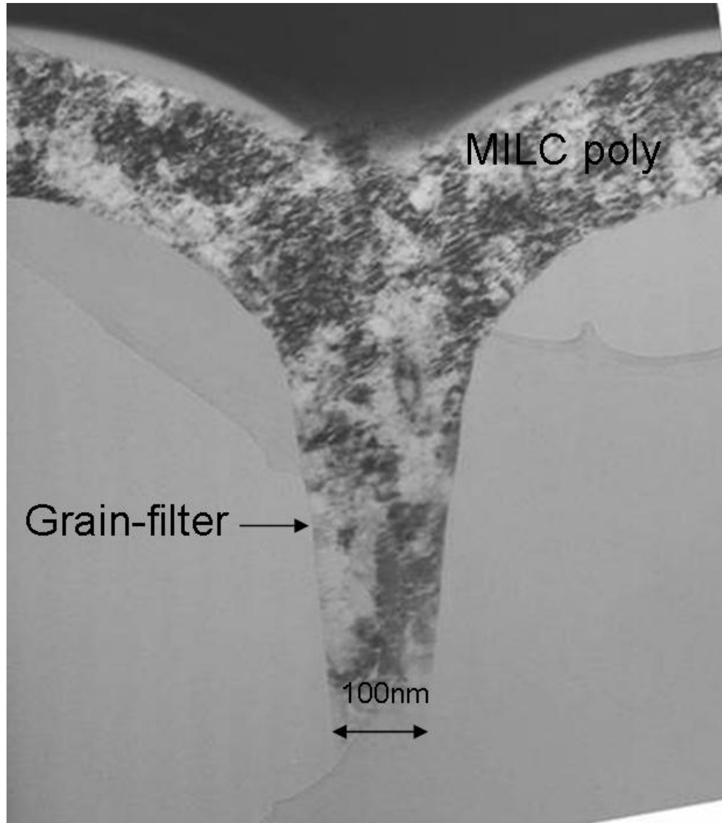



Fig.4.1.2 TEM cross section of grain filter after MILC

The (100) or (110) orientated poly-Si seeding layer was selected, using the orientation dependence on the position with respect to the Ni pattern[1)], by positioning the grain filter near the corner or the side of the Ni pattern, respectively. Fig. 4.1.3 shows the planar view of the grain filter with respect to the Ni pattern. For the (100) orientation, the corner was repeated on a line with a Ni pattern of multi-triangular shape to increase the area of the (100)

oriented grains (Fig. 4.1.3 (a)). For the (110) orientation, grain filter was positioned at the side of rectangular shape Ni pattern (Fig. 4.1.3 (b)).

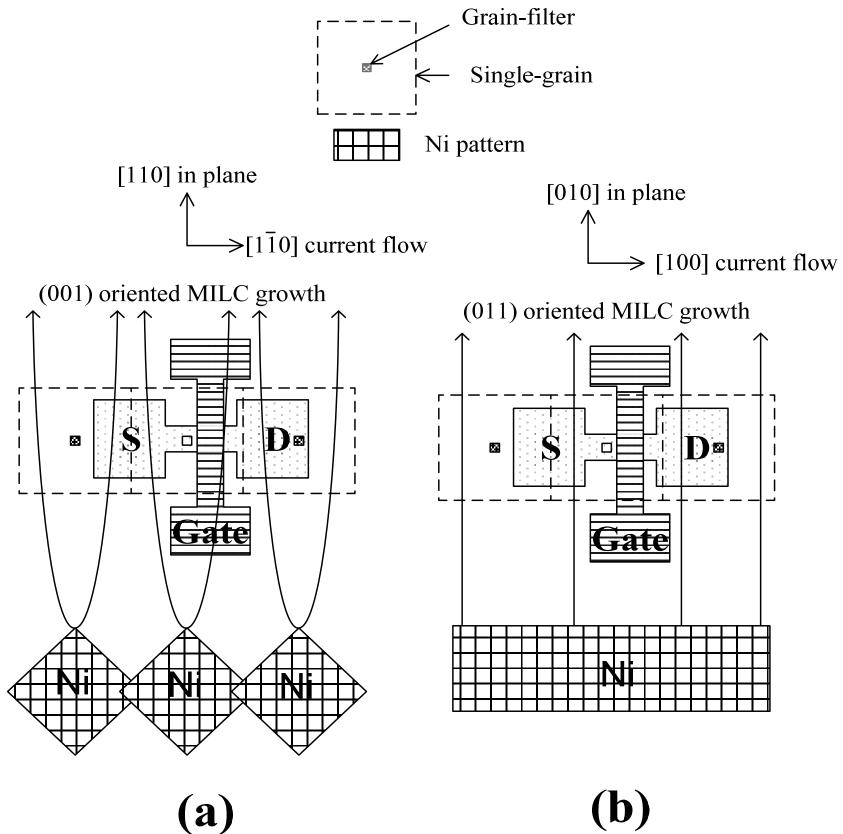



Fig.4.1.3 Planar view of Ni pattern design for (100) and (110) single-grain TFT

*4.1.2 Ni removal process*: Then the 250nm MILC poly-Si layer was etched away by dry etching while keeping the MILC poly-Si inside the grain-filter as a seed (Fig.4.1.4). After that, a 2nd a-Si layer with a thickness of 250nm was deposited by LPCVD and the sample was crystallized by excimer-laser with laser energy density of 1500mJ/cm$^2$.During laser irradiation, (100) or (110) oriented grains epitaxially grew from the seed in the grain filter (Fig.4.1.5).

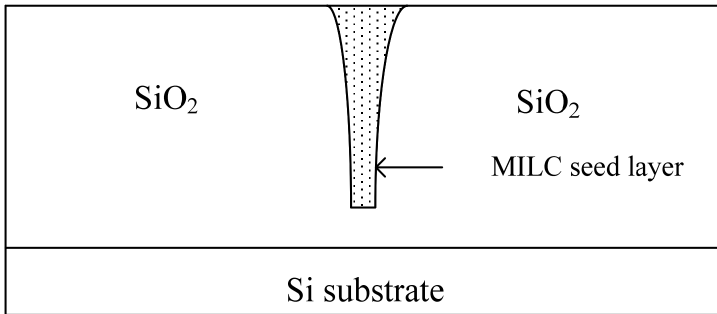



Fig.4.1.4 Cross section of the structure: etch away Ni contaminated layer

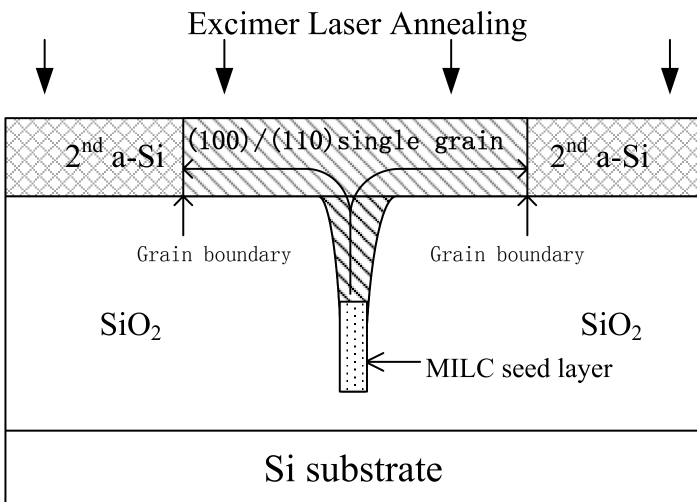



Fig.4.1.5 Cross section of the structure: Deposition new Si layer and grown (100)/ (110) oriented single-grains by laser crystallization

Figure.4.16 plots the pole-figure of EBSD of the location-controlled grains, which is shown in SEM image, grown from the grain filters positioned at the corner (a) and the side (b) of the Ni area. It can be seen that both surface and in-plane orientation of (100) and (110) were obtained for the grains at the corner (a) and the side (b) respectively. The (100) oriented grains have the in-plane orientation of [110] along the direction perpendicular to the

multi-triangle shaped Ni pattern, while the (110) oriented grains have [100] along the direction perpendicular to the side of rectangular shaped Ni pattern. Fig.4.1.7 shows SIMS measurement of Ni concentration after MILC and after laser crystallization. Without "Ni removal process", Ni concentration was $10^{20}$ /cm$^3$, $10^{17}$ /cm$^3$ and $10^{18}$ /cm$^3$ in the MIC, MILC and growth front region respectively. However, after removal the Ni contaminated poly-Si layer, deposition a new a-Si layer and laser crystallization, "Ni removal process", Ni concentration was greatly reduced below the detection limit of SIMS ($5 \times 10^{15}$ /cm$^3$).

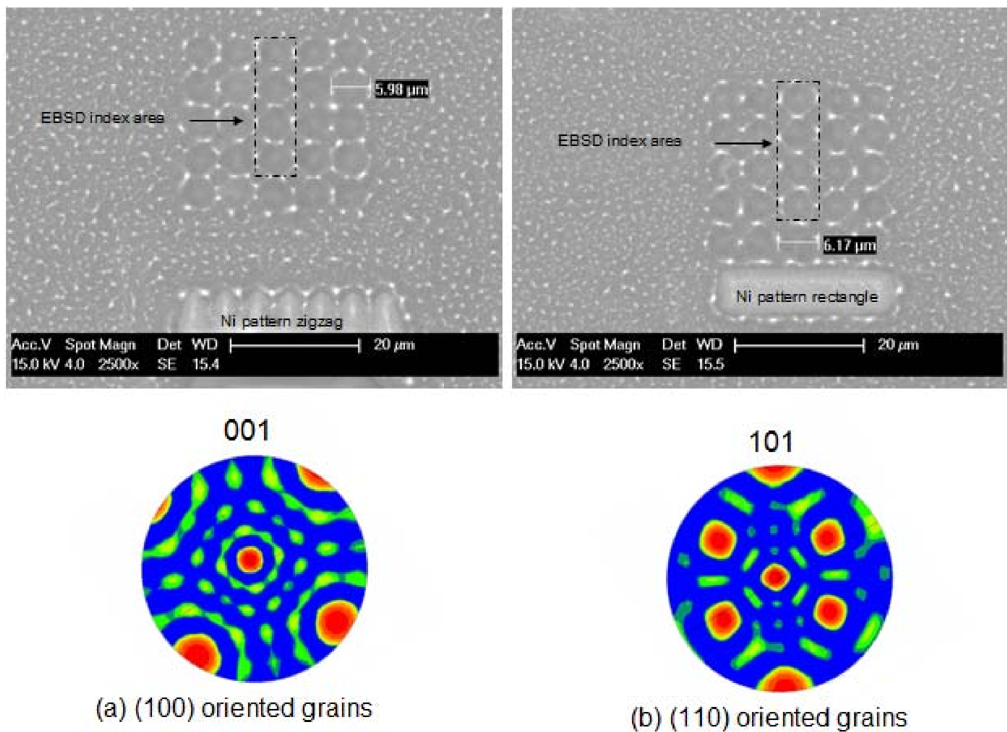



Fig.4.1.6 SEM and pole-figure of (100) and (110) oriented single grains after laser crystallization

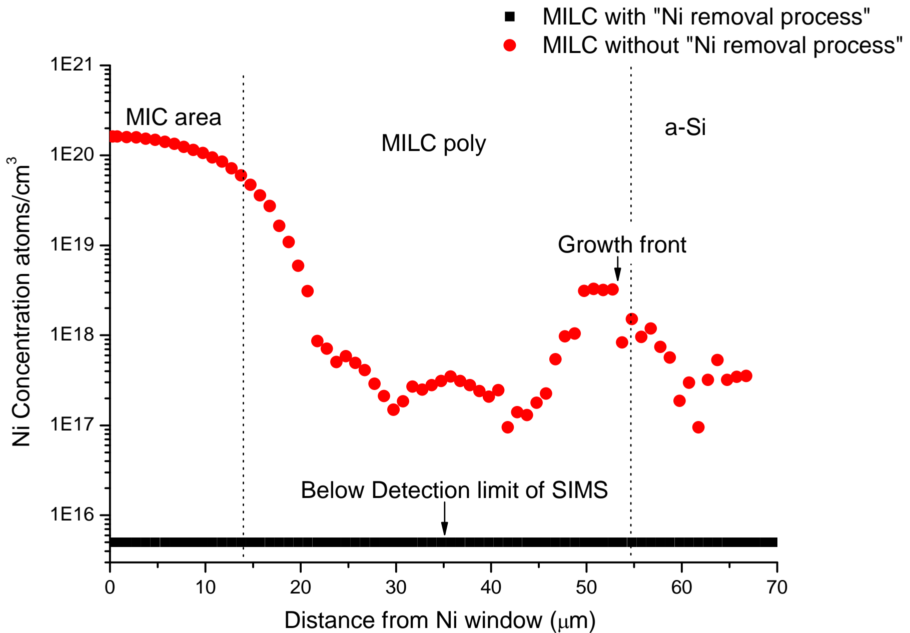



Fig.4.1.7 SIMS measurement of Ni concentration after MILC with/without "Ni removal process"

## 4.2 (100) and (110) Single Grain (SG) TFTs:

Fig.4.2.1 shows the cross section of SG-TFT. After pattering the Si into islands, a 68nm thick $SiO_2$ was deposited as a gate oxide by ICP-PECVD at 250°C. After that, it was annealed at 400°C in $H_2$ to passivate interface defects. The source and drain were doped with $10^{16}$ions/cm$^2$ by phosphorous implantation at 30keV for n-channel and $10^{16}$ ions/cm$^2$ by boron at 20keV for p-channel. The dopants are activated by excimer laser at 300mJ/cm$^2$. The channel width and length was 2μm for p- and n- channel TFTs. The SG-TFTs with (100) surface orientation has the current flow direction of $[1\bar{1}0]$ while the TFTs with (110) orientation has the flow direction of [100] (Fig.4.1.3).

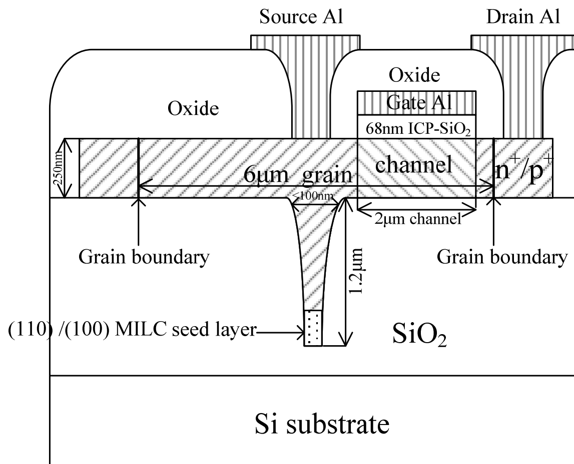



Figure 4.2.1 Cross section of (110) and (100) SG TFT

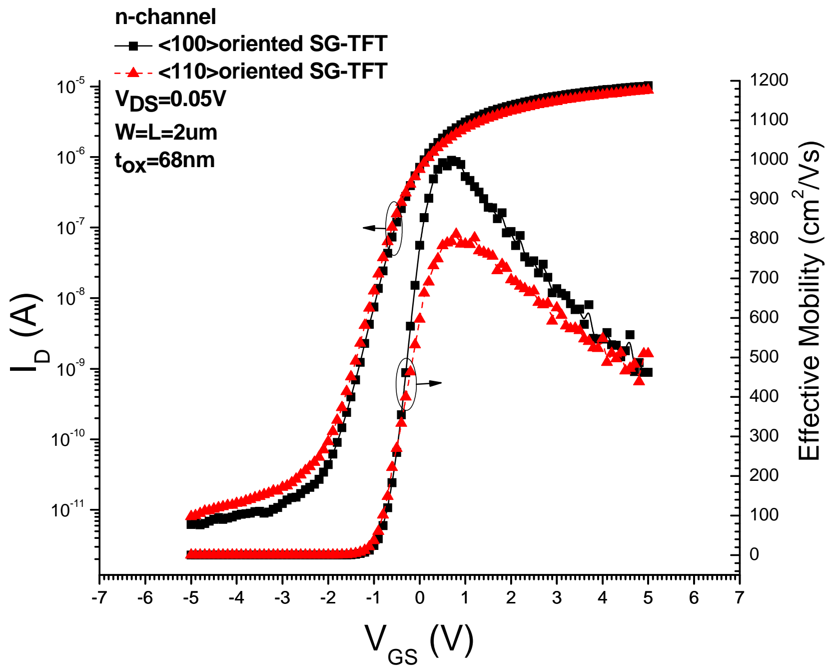



Figure. 4.2.2 Transfer characteristics for n-channel SG TFTs

Figures 4.2.2 shows the transfer characteristics for n- and Figure 4.2.3 shows transfer characteristics for p-channel SG-TFTs. For n-channel (Figure 4.2.2), the (100) SG-TFTs show a high mobility of 998cm$^2$/Vs, while the (110) SG-TFTs show a mobility of 811cm$^2$/Vs.

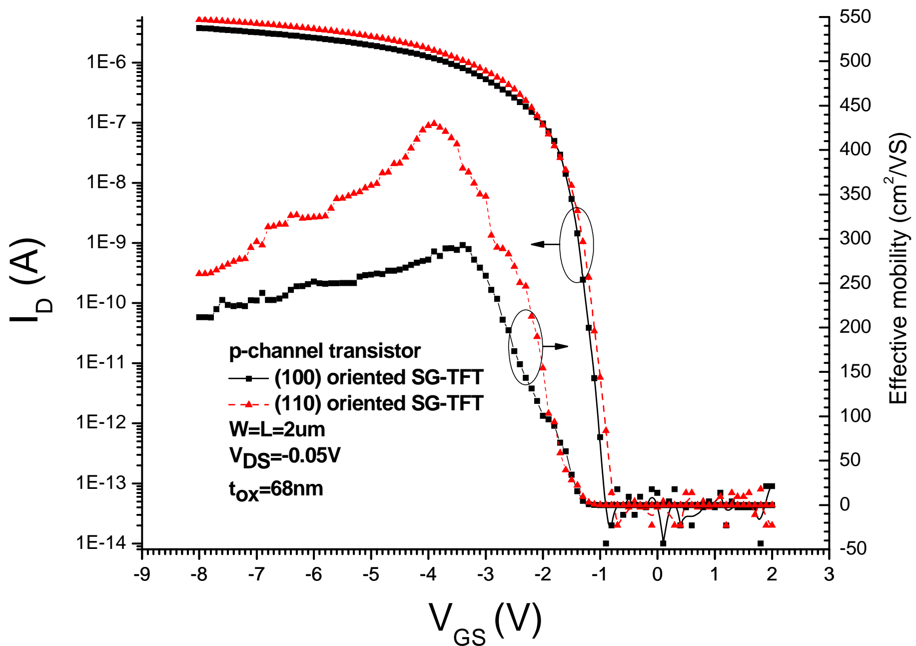



Figure 4.2.3 Transfer characteristic of p-channel SG TFTs

For the p-channel (Figure 4.2.3), the (110) SG-TFTs show a high mobility of 429cm$^2$/Vs while the (100) SG-TFTs show a slightly lower mobility of 292cm$^2$/Vs. The mobility dependence on the orientation reflects very well the calculated effective mass dependence on the orientations[2)]. An advantage of the process in this study over the conventional SOI technology is that an optimum mobility for n- and p-channel transistors on a single-wafer without seed substrate can be realized, by the (100) and (110) orientation control, respectively. Figure 4.2.4 shows the output characteristic for the n- and p-channel SG-TFTs.

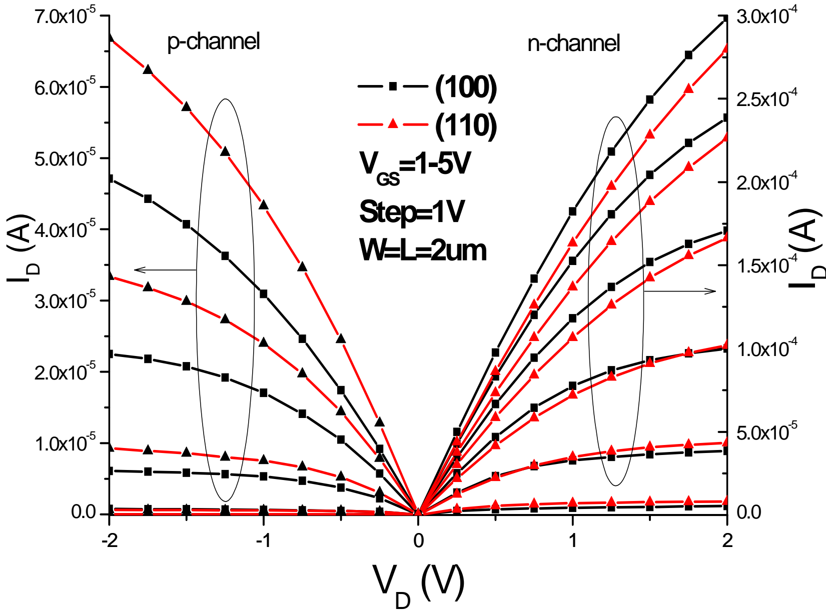



Figure 4.2.4 Output characteristic of SG TFTs

Table.1 summarizes the n-/p-channel device performance of (110) and (100) SG-TFTs. It can be seen for both n- and p-channel that the leakage current is below 100pA and is the same as for SG-TFTs without MILC process[1)]. This confirms the results of our SIMS measurements that Ni contamination is neglectable. For n-channel, (110) SG-TFT shows much higher leakage current (81pA) than (100) SG-TFT (6.2pA) which I suggest is due to more electron tunneling of (110) orientation than that of (100) orientation. However, for p-channel device, the leakage current of (100) SG-TFT (0.09pA) is slightly higher than that of (110) SG-TFT (0.02pA). This will be further investigated in the following sections concerning the reliability of (100) and (110) SG-TFTs. Also for n-channel device, the S value of (110) SG-TFT is 0.021V/dec higher than that of (100) SG-TFT which suggests more interface states for (110) SG-TFTs. For p-channel, the S value of (110) SG-TFT is only 0.009V/dec lower than that of (100) SG-TFTs.

| TFT | (100) MOS | (110) NMOS | (100) PMOS | (110) PMOS |
|---|---|---|---|---|
| $\mu_{FE}$ $cm^2/Vs$ | 998 | 811 | 292 | 429 |
| Vth (V) | -0.2 | -0.2 | -1.6 | -2.1 |
| S (V/dec) | 0.385 | 0.406 | 0.104 | 0.095 |
| $I_{on}$ (μA) | 10 | 9 | -3.8 | -5.2 |
| $I_{leak}$ (pA) | 6.2 | 81 | 0.09 | 0.02 |

Table.1 Summary of device characteristics

Figure 4.2.5 shows statistical analysis of the (100) and (110) SG-TFTs, together with randomly oriented SG-TFTs[3)] and SOI-TFTs with (100) orientation for a comparison. The average electron mobility of SOI is 727$cm^2$/Vs and the average hole mobility of SOI is 250$cm^2$/Vs. The higher electron and hole mobilities of SG-TFT than that of SOI are due to the tensile stress inside the grains during quick solidification[4)]. It can be seen that the uniformity of the SG-TFTs in this study has been improved owing to fixing both surface and in-plane orientation, when compared with the randomly oriented SG-TFTs. The mobility spread (One σ value) is around 8% for the (100) n-channel and (110) p-channel SG-TFTs, which are approaching those of the SOI counterpart (3%).

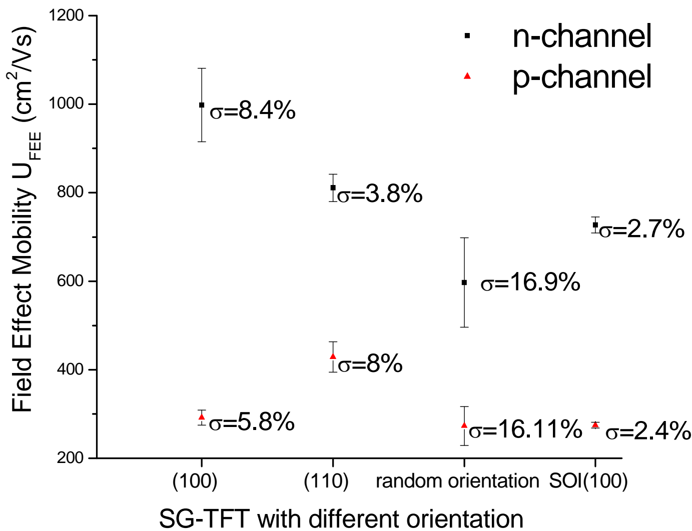



Figure 4.2.5 Comparison and Statistical analysis mobilities of (100) and (110) SG-TFTs (One σ value)

## 4.3 Electrical Reliability of (100) and (110) Orientation and Location Controlled Single Si Grain TFTs

### 4.3.1 Introduction

The performance of location and orientation controlled SG TFT surpass the performance of SOI. It will be very promising that SG-TFT can be applied to fabricate RF circuits, CPU, memories, 3D ICs, and drive-circuits for OLED. However, integrated circuit (IC) with SG-TFTs requires high reliability of SG TFT. In this chapter, the location and orientation controlled SG TFT will be tested under different electrical stress. Hot carrier effects, floating body, short channel effects will be addressed in detail.

**Hot Carrier effects** Hot carrier effects often happen when the drain is electrically stressed. Hot carriers are generated close to the drain region where the electric field is highest. The hot carriers can be injected into the gate oxide, generate trap states and accumulate at the bottom of the channel region and act as the base current of a parasitic bipolar transistor to increase positive drain current.

**Floating body effects** In TFTs and in SOI MOSFETs, the active channel is usually electrically isolated. The channel is not directly contacted, which results in floating-body effects.

One of the floating body effects is the kink effect. The kink effect is caused by injection of holes into the floating channel. The holes are generated by impact ionization in the high electric field near the drain. The electrical field of the depletion region forces the holes into the channel. The substrate potential increases because of the accumulation of the holes, result in the decrease of threshold voltage and the increase of drain current.

Besides the kink effect, the floating body causes a parasitic bipolar transistor action. When sufficient holes are injected in the floating substrate, the source-substrate junction gets forward biased. This results in electrons to be injected from the source (emitter) through the substrate (base) and collected in the drain (collector). The parasitic bipolar transistor forces an extra drain current, which in turn increases additional impact ionization. The feed forward action causes a breakdown of the TFT.

**Short channel effects** Short channel effects happen when the channel length becomes comparable to the size of the depletion region of the drain. Due to the extension of the depletion areas of the drain and source under the gate, the effective length of the channel decreases. This shorter channel influences the threshold voltage, the drain current, the subthreshold swing etc.

In the short channel MOSFET the charge in the depletion area becomes less because of the extension of the drain depletion area. The total charge in the depletion area thus becomes smaller and threshold voltage decreases.

The barrier height for channel carriers at the edge of the source near the surface is lowered by the drain electric field as the channel length becomes shorter. This increases the number of carriers injected into the channel from the source. As a result, the drain current increases.

The subthreshold swing increases with shorter channel lengths. At a given voltage, if the depletion charge decreases, the surface potential increases. This results in a smaller depletion capacitance for shorter channel lengths, which results in a larger subthreshold swing.

**Bulk defects and Grain boundaries**

Due to the amorphous substrate and low temperature process, polycrystalline Si or hydrogenated amorphous silicon usually has a lot of defects. These defects in the silicon will introduce active trap states in the band gap. These trap states can trap carriers and act as intermediate state between the conduction and valence bands and increase probability for generation or recombination processes. Also at grain boundaries, the periodical lattice is disrupted and lots of defects generated. These defects act as extra trapping states.

### 4.3.1 Fabrication of (110) and (100) SG-TFTs

The (110) and (100) single-grain TFTs is fabricated inside a location and orientation controlled single-grain by metal induced lateral crystallization and μ–Czochralaski process.

After pattering the Si grains into islands, a 80nm thick $SiO_2$ was deposited as a gate oxide with PECVD by TEOS at 350°C. After that, it was annealed at 400°C in $H_2$ to passivate interface defects. The source and drain were doped with $10^{16}$ ions/cm$^2$ by phosphorous implantation at 30keV for n-channel. Then the dopants are activated by excimer laser at 300mJ/cm$^2$. The channel width and length was 2μm for n- channel SG-TFTs. The SG-TFTs with (100) surface orientation has the current flow direction of $[1\bar{1}0]$ while the TFTs with (110) orientation has the flow direction of [010]. The process difference with the previous chapter is that TEOS is used as gate oxide instead of ICP $SiO_2$.The TFTs which uses TEOS as gate oxide shows a slightly lower mobility than that uses ICP due to the higher interface density of TEOS, TEOS has a better step coverage and the breakdown voltage of TEOS is higher than that of ICP due to higher temperature process.

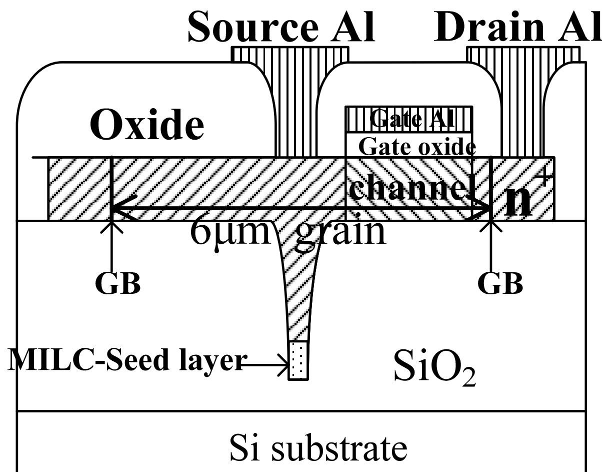



Fig. 4.3.1 Cross section of (100) and (110) SG-TFTs structure

**4.3.2 Initial status of the device**

Fig.4.3.2 shows the statistic variation of the (100) and (110) SG-TFT, random oriented SG-TFT and SOI. The uniformity of the TFTs have been improved due to (100) and (110) orientation control, when compared with

the randomly oriented SG-TFTs. The mobility variation is around 7% for the (100) n-channel and 3.7% (110) n-channel TFTs, which are approaching those of the SOI counterpart. For n-channel, the (100) TFTs show a high mobility of 732cm$^2$/Vs, while the (110) TFTs show a mobility of 630cm$^2$/Vs before electrical stress. Both the uniformity and mobility is improved compared with SG-TFTs without orientation control (random orientation) which indicates the reliability improvement. It shows that the mobility is a little bit decreased when compared with (100) and (110) SG TFTs fabricated by ICP $SiO_2$ in the previous chapter. This is probably due the fact that TEOS will have higher interface states between gate oxide and active channel region than ICP. However, the uniformity of the devices is almost same.

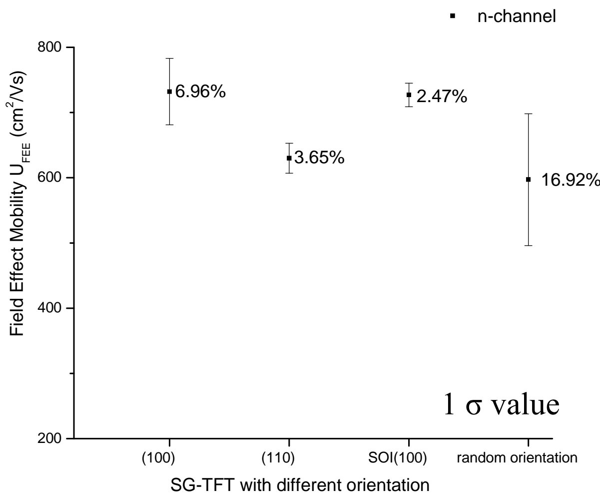



Fig.4.3.2 Comparison and Statistical analysis of the (100) and (110) SG-TFT, random oriented SG-TFT and SOI (One σ value)

### 4.3.3 Reliability of the Device under different electrical Stress

***I. Positive Gate Bias:***

Fig.4.3.1 and 4.3.2 show the transfer characteristic of (110) and (100) n-channel device under 6V gate bias, respectively, with a drain voltage of

0.05V for 100s and 1000s. The electrical field across the gate is 0.88MV/cm. After the gate is stressed with a voltage of 6V for 100s and 1000s, for n channel, no positive shift has been observed for both (110) and (100) SG-TFT. The mobilities of (110) and (100) SG-TFTs have not been deteriorated. The subthreshold swing (S) and the off-current for (110) and (100) SG-TFTs have been slightly increased. Those are different than poly-Si[5)]. The S of (100) SG-TFT is more stable than (110) under positive gate bias which is same as single crystalline Si[6)]. The leakage current has increased more for (100) SG-TFT than (110) SG-TFT. Moreover, the $V_{th}$ has a negative shift. Thus it can be concluded that hot holes injection in the gate oxide, accompanied by acceptor states generation at upper half of the bandgap at the interface[7)].

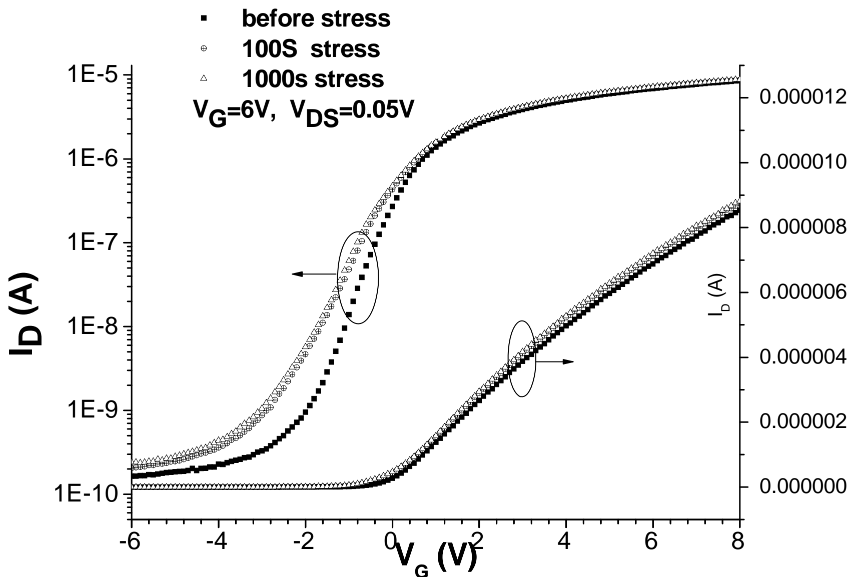



Fig.4.3.1 Transfer characteristic of (110) n-channel device under 6V gate bias with drain voltage of 0.05V

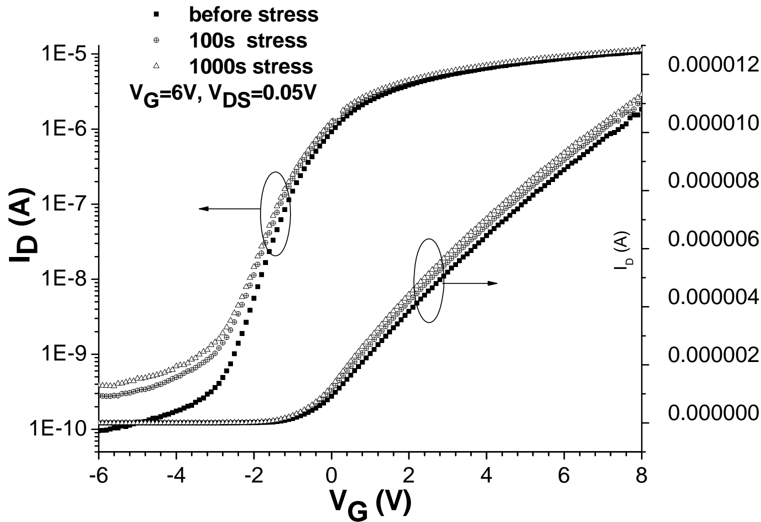



Fig.4.3.2 Transfer characteristic of (100) n-channel device under 6V gate bias with drain voltage of 0.05V

***II. Positive drain bias effect after gate bias***

After the (110) and (100) n-channel device is stressed on gate, 9V bias has been put consequentially on drain with gate voltage of 2V on the same device. Fig.4.3.4 and 4.3.5 show the transfer characteristic of (110) and (100) n-channel device under 9V drain bias with $V_G$ of 2V for 10s, 100s and 1000s. With the drain bias stress, subthreshold swing is improved from 0.726V/dec to 0.630V/dec and from 0.871V/dec to 0.630V/dec for (100) and (110) SG-TFTs, respectively. Also leakage current has decreased and a slightly positive shift of $V_{th}$ has been observed. Based on the experiment results, it can be concluded that the positive shift of $V_{th}$ is due to hot electrons generated by the high electrical field[8)] around drain recombining with the trapped hot holes generated by the previous gate bias stress. And the improvement of S and leakage current is due to self heating[9)] which passivate the interface defects during electrical stress.

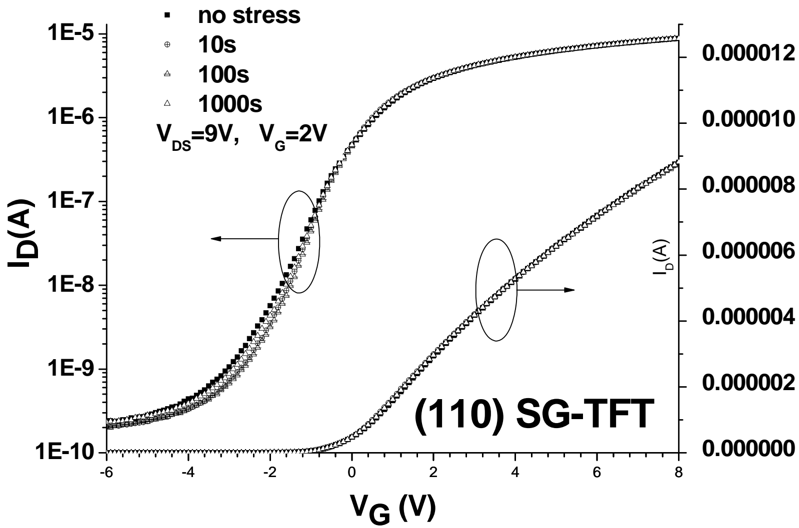



Fig. 4.3.4 Transfer characteristic of (110) n-channel device under 9V drain bias for 10s, 100s and 1000s

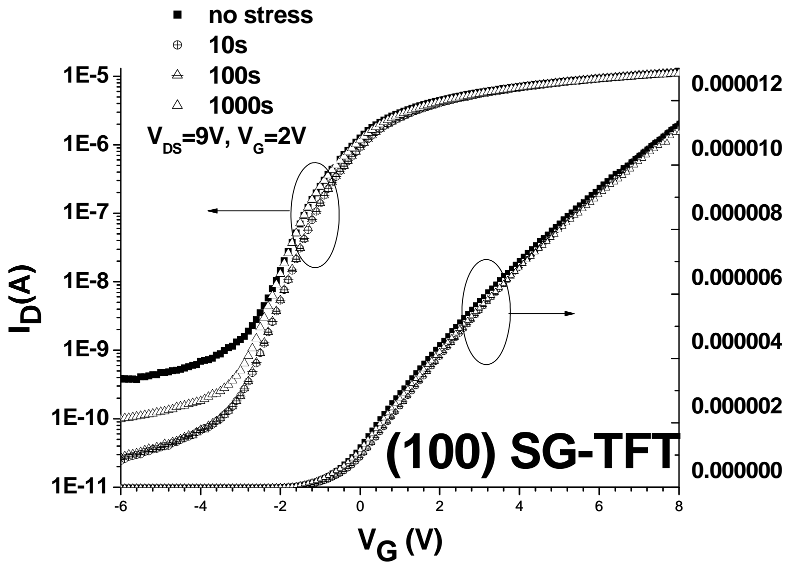



Fig. 4.3.5 Transfer characteristic of (100) n-channel device under 9V drain bias for 10s, 100s and 1000s

***III. Positive drain bias effect under different voltage:***

To further investigate the effect of hot electrons effect caused by high electrical field around the drain, voltages of 12V, 15V, 20V, 25V and 30V have been applied on drain with gate voltage of 2V for 1000s on new device which has not been stressed under positive gate bias. From Fig.4.3.6, neither $V_{th}$ shift nor S deterioration below 25V drain bias stress has been observed. A negative $V_{th}$ shift together with deteriorate S has been observed when the drain voltage is higher than 25V. Leakage current and on current has also increased under 30V drain bias. These are due to generation of electron-hole pairs by impact ionization under high drain voltage[10).

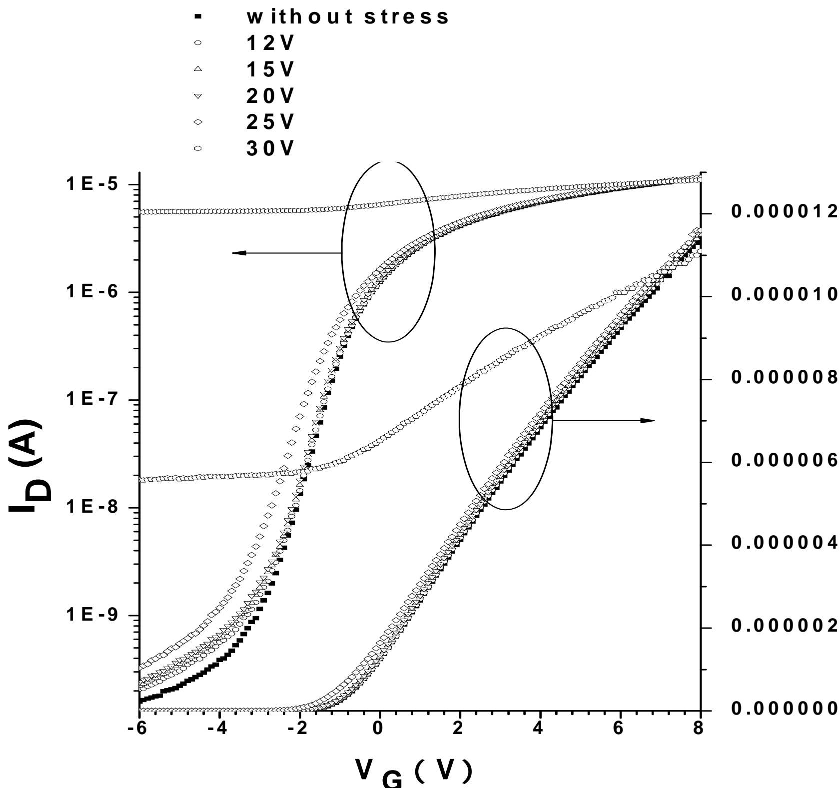



Fig.4.3.6 Transfer characteristic of n-channel device under different drain bias for 1000s

To further investigate the impact ionization, output characteristic have been measured. Fig.4.3.7 shows the kink effect in the output characteristic of the device before stress. The kink current is indicated at high drain bias.

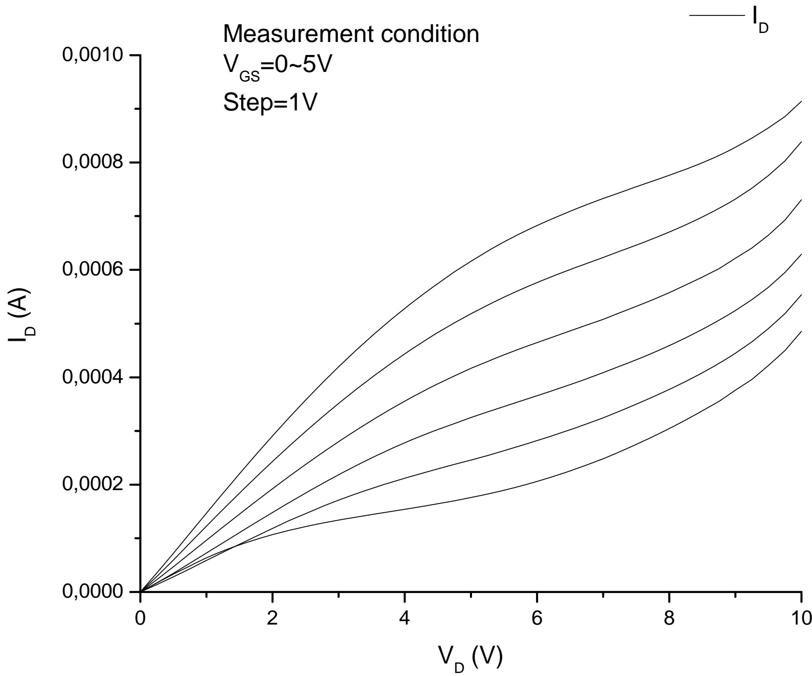



Fig. 4.3.7 Kink effect in the output characteristics

Fig.4.3.8 (a)-(d) show the effect of the drain bias stress on the kink current measured under different gate voltage. The stress condition is that the drain is biased with different voltages (0~20V) with VGS of 2V for a fixed time of 1000s. The high electrical field caused by drain bias stress enhances impact ionization. As a result, the kink current increases which correspondent to the red solid line circle in Fig.4.3.8 (a)-(d). Also it can be seen that the difference of the kink current before and after stress decreases as gate voltage increases. This is due to the high gate voltage decrease the depletion region by the drain bias which decreases the collection of electron-hole pairs by impact ionization[10)]. Moreover, at high drain voltage,

trap states have been generated which enhances the recombination rate and as a result the kink current decreases (see the black dash circle in Fig.4.3.8 (a)-(c)).

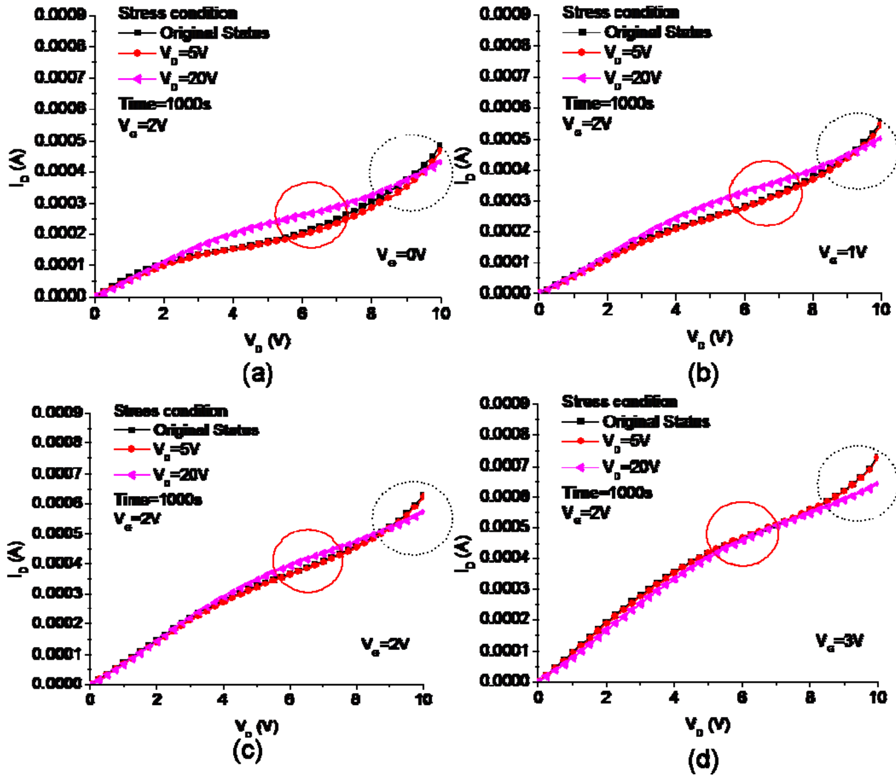
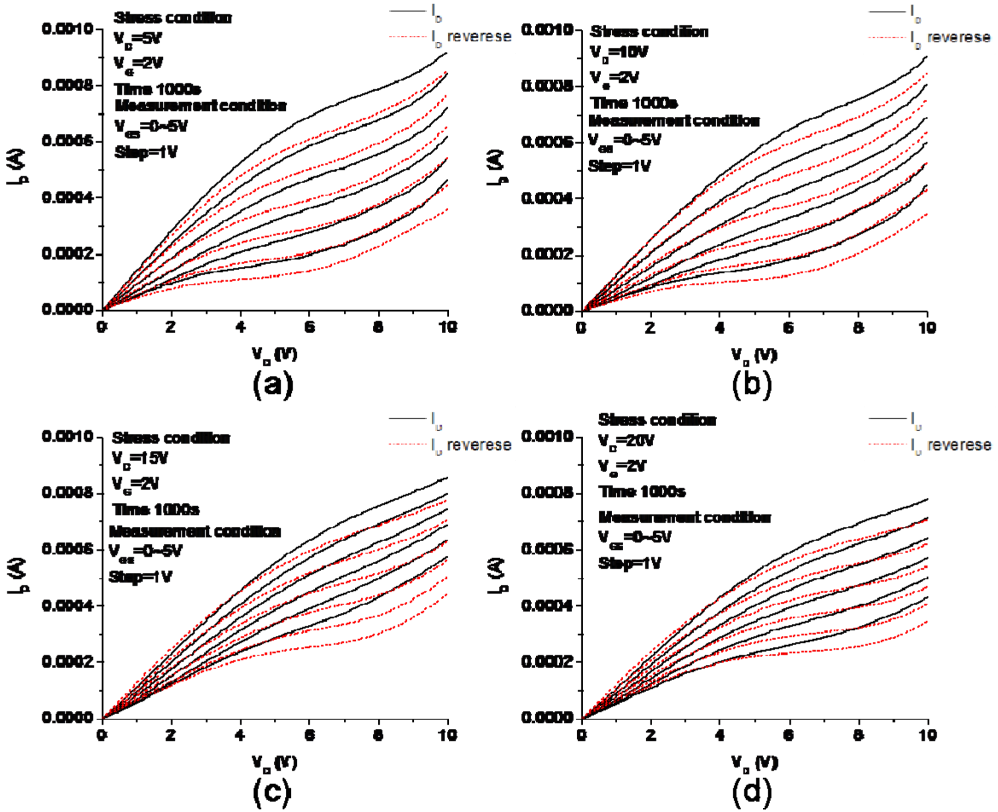



Fig.4.3.8 (a)-(d) the effect of the drain bias stress on the kink current measured under different gate voltage

In order to investigate the trap states created at the drain side, the "asymmetry measurement" has also been performed. For a normal mode, the $I_D$-$V_D$ characteristic has been obtained by defining the drain, gate, and source electrodes same as in the stress condition. In the reverse mode, the definitions of source and drain were exchanged. As it can be seen from Fig.4.3.9 (a)-(d), the devices shows asymmetry output characteristics after

different drain stress. In saturation mode, the drain current is high in normal mode than in reverse mode.




4.3.9 Asymmetry output characteristics after different drain stress

This is explained by Fig.4.3.10 Under saturation, the influence of interface trap states in the pinch-off region is suppressd[11)]. Additionally, the interface trap states are generated at drain region due to high drain bias. Thus the suppression of the interface states induced by the pinch-off region in the normal mode doesn't affect the drain current. However, in the reverse mode, the source and drain has been exchanged and the interface states is outside the pinch off region which reduces the drain current.

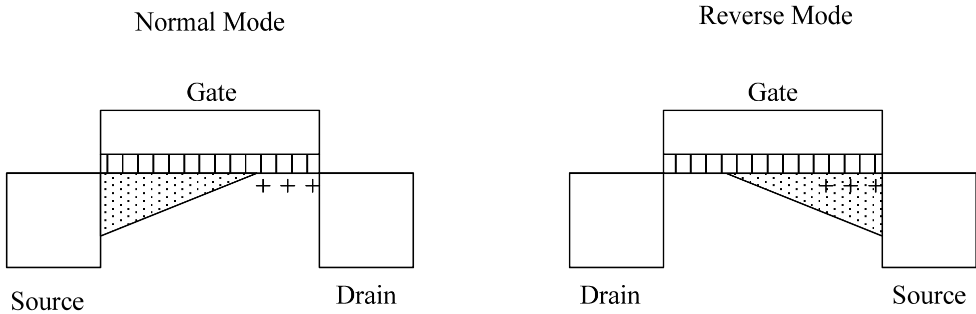



Fig. 4.3.10 Schematic of TFT in saturation mode

Fig. 4.3.11 shows the transfer characteristic of the device in the linear mode after drain is stressed with 20V after 1000s. The drain current is slightly higher in the reverse mode than in the normal mode.

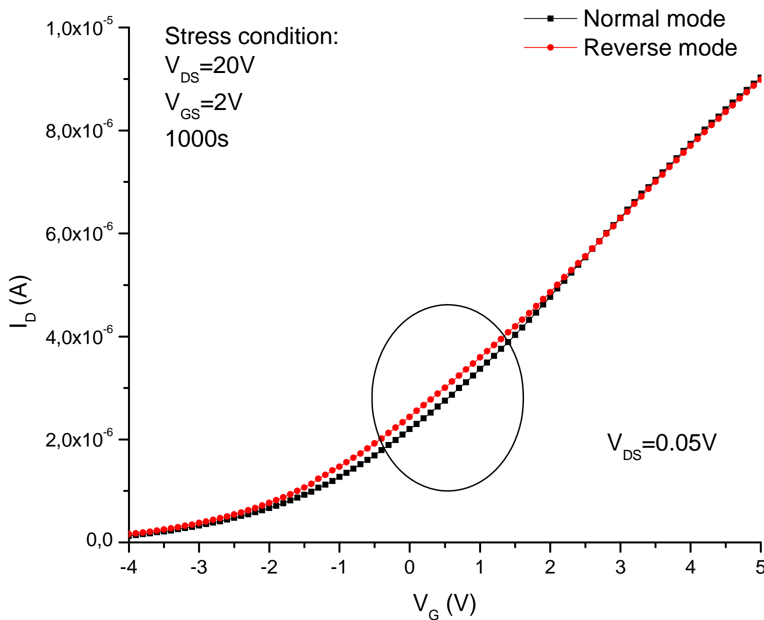



Fig. 4.3.11 Transfer characteristic of the device in the linear mode after drain is stressed

This is explained in Fig. 4.3.12. When the device is in linear mode, the channel is inverted from source to drain. Carrier transport is disturbed by the interface trap state generated by high drain bias. The carrier density is higher than the traps. The interface trap state rapidly decrease as the carrier density increases[11),12)]. And the carrier density is slightly higher in the source than in the drain due to the positive bias of $V_{DS}$. Therefore, the drain current is higher in the reverse mode than in the normal mode (see the black solid circle in Fig.4.3.11).

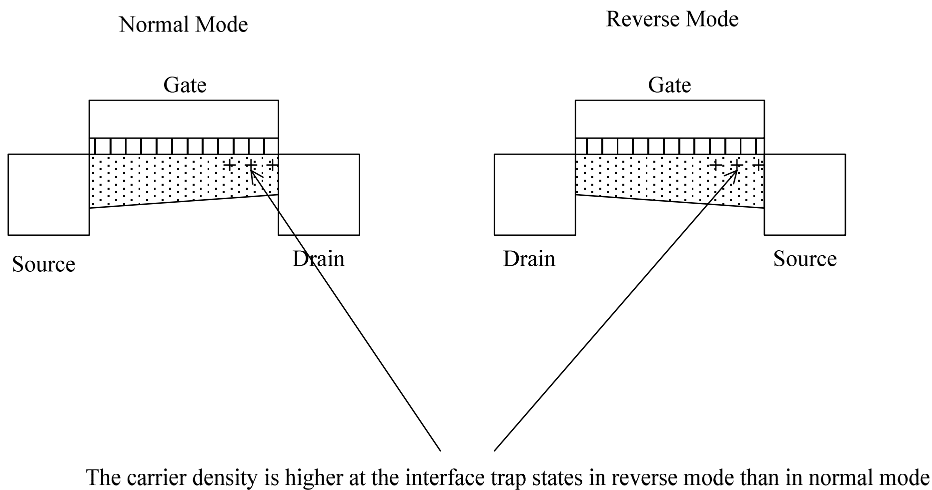



Fig. 4.3.12 Schematic of Device under linear mode

***IV. Negative gate bias effect***

Furthermore, the stress experiment by negative gate bias (off-state) has been performed. Fig.4.3.13 and Fig.4.3.14 show (110) and (100) n-channel device under gate voltage of -10V with drain voltage of 0.05V for 100s and 1000s. From Fig.4.3.13 and Fig.4.3.14 it shows that until 100s only positive shift of transfer characteristic for (110) and (100) n- channel due to electrons tunneling into oxide from source and drain. And S has been deteriorated from 0.722V/dec to 0.792V/dec and from 0.617V/dec to 0.738V/dec for (110) and (100) n- channel after 1000s stress. Leakage current has deteriorated from 40nA to 70nA only for (110) SG-TFT after 1000s stress. $V_{th}$ has a positive shift of 0.3V and 0.6V for (110) and (100) respectively.

With increasement of stress time under high gate negative bias, more electrons can gain enough energy tunneling from drain to channel and generated trapped states at mid-gap[13]. And (110) SG-TFT has higher leakage current increase than (100) after negative gate bias.

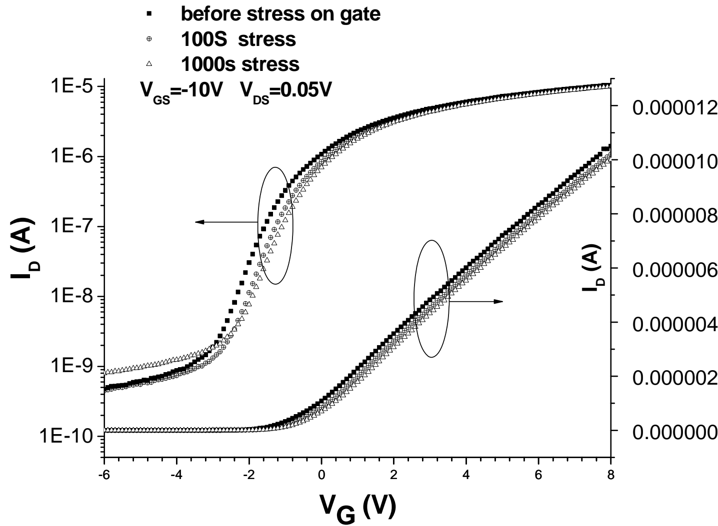



Fig.4.3.13 Transfer characteristic of (110) n-channel device under negative gate bias 10V and drain voltage of 0.05V

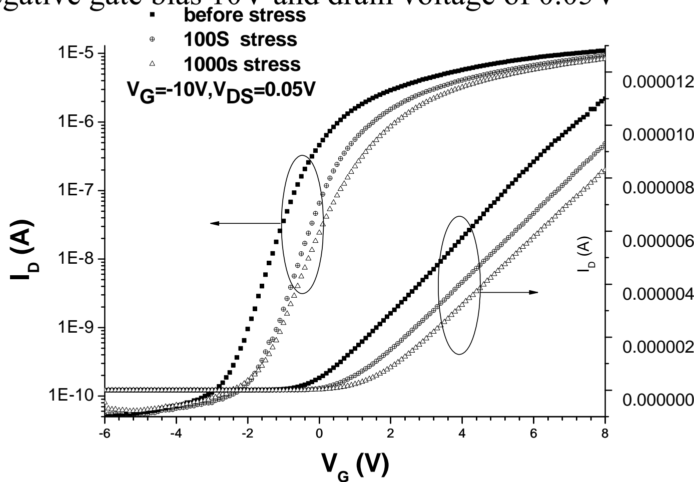



Fig.4.3.14 Transfer characteristic of (100) n-channel device under negative gate bias 10V and drain voltage of 0.05V

### *V.Summary mobility and S change under different electric stress*

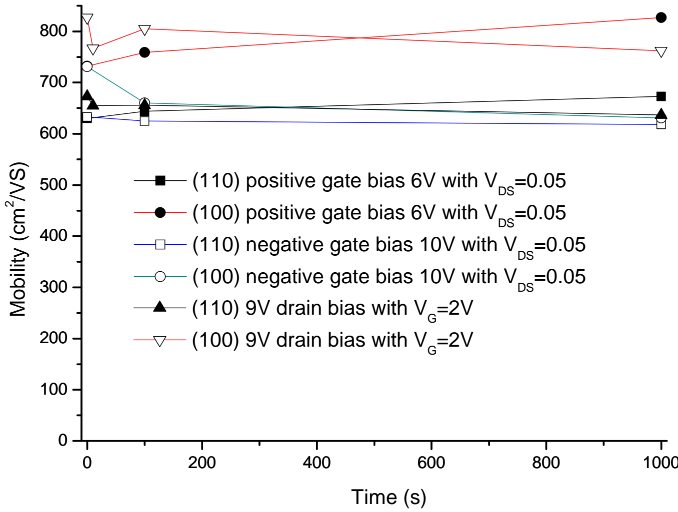



Fig.4.3.15 Mobility of (100) and (110) n-channel device after different stress conditions

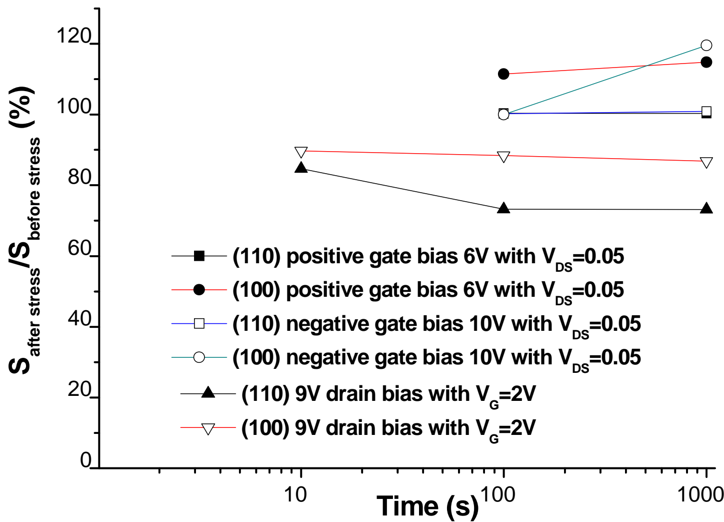



Fig.4.3.16 Subthreshold change of (100) and (110) n-channel device after different stress conditions

Fig. 4.3.15 and 4.3.16 summarize the mobility and S change under different stress conditions. Based on these result, it can be concluded that hot holes caused deterioration of device and negative shift of $V_{th}$ by positive gate stress while hot electrons caused deterioration of device and positive shift of $V_{th}$ by drain bias and negative gate bias.

## 4.4 Conclusions

High performance SG-TFTs of which the mobility surpasses SOI performance have been achieved. This is done by a combination of both (100) and (110) surface and in-plane orientation-controlled Si grains through the MILC poly-Si as a seed and the μ–Czochralski process. The field-effect mobility of n-channel transistor is 998cm$^2$/Vs for (100) SG-TFTs and 811cm$^2$/Vs for (110) SG-TFTs. The Field-effect mobility of the p-channel transistor is 292cm$^2$/Vs for (100) SG-TFTs and 429cm$^2$/Vs for (110) SG-TFTs. Therefore this process is highly suitable for the monolithic integration of memories, analog, and RF circuits on a glass substrate (below 600$^o$C).

(100) and (110) n-channel SG-TFTs under positive gate stress, drain stress and off-state stress have been investigated. Under positive gate stress, hot holes dominate the deterioration of device with a negative shift of the $V_{th}$. Under positive drain bias, hot electrons dominate the deterioration of the device with a positive shift of the $V_{th}$. Kink effect has been observed in the output characteristic at high drain voltage. The higher voltage of drain stress enhances impact ionization which induces the kink current increases. At higher drain bias, interface trap states at the drain side have been created which in turn decrease the kink current. “Asymmetric” output characteristics have also been observed after drain bias. The asymmetric performance confirms that the interface traps are generated at drain side. Under negative gate bias, electrons tunneling through the drain to channel dominate the deterioration of the device with a positive shift of the $V_{th}$. SG-TFT shows more stable performance than poly-Si TFT under different stress conditions.

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# Chapter 5

# Location Controlled Single-Grain Ge TFTs Grown on MILC Si layer by μ-Czochralski process

Ge has been considered as a promising channel material due to its higher field effect mobility than that of Si. However, there are challenges that limit the Ge application in today's IC process. In this chapter, it will be proposed to epitaxial grow single grain Ge on (100) Si seed layer which is proposed in chapter 3. Capping oxide during excimer laser annealing is used to improve interface property between oxide and Ge channel by melting native Ge oxide during excimer laser annealing. Source and drain is doped with Si and activated with excimer laser annealing to suppress fast dopants diffusion into channel region and apply tensile stress to further increase mobility.

## 5.1 Introduction

The limitations of silicon are becoming more evident. Since the 90nm technology node, manufacturers have used silicon germanium (SiGe) source and drain regions, silicon carbide (SiC), and other methods to strain the silicon channel. Strain engineering has already delivered substantial performance improvements, and most manufacturers' roadmaps expect strain engineering to be the main route to performance improvement in future technology generations as well. However it is still not clear how much strain can help.

Germanium (Ge) is one option. Ge has a long history in the semiconductor industry. Ge has a smaller bandgap than that of Si. It has electron mobility of 3900cm$^2$/Vs, compared to 1350 cm$^2$/V-sec for silicon, while Ge's hole mobility of 1900cm$^2$/Vs is the highest of any known semiconductor[1)]. In fact, the first bipolar transistors and integrated circuit were fabricated by Ge. Germanium readily forms an alloy with silicon, silicon germanium (SiGe), which has been used in strain engineering for years. However, Si replaces Ge quickly and becomes dominate in today's IC technology due to the superior properties of silicon dioxide, not only as an insulation layer between multilayer but also as a high quality gate capacitance. However, engineers are now reconsidering as a future channel material which substitutes Si.

The first challenge of Ge MOSFET is lack of a gate oxide with good interface properties. Germanium's native oxide, GeO, which is unstable and water-soluble, is inevitably formed even high K material [(2)~(4)] or $GeO_2$ [(5)~(7)] is applied. The desorption of GeO will generate a lot of interface defects which will decrease the mobility and increase the subthreshold swing of MOSFET.

The second challenge for Ge MOSFETSs is the material's smaller bandgap of 0.7eV, compared to 1.1eV for silicon. The smaller gap effectively lowers the energy barrier between n-type and p-type materials, facilitating band-to-band tunneling and leakage at junctions. This leakage may ultimately limit the scalability of Ge transistors.

The third challenge for Ge MOSFET is dopant activation. Due to the low solubility of dopants such as phosphorous, arsenic, etc, the dopants will

diffuse into channel region very fast at a very low activation temperature, resulting in a low on/off ratio.

μ-Czochralski process provides a solution for Ge MOSFET. Capping oxide is deposited before excimer laser crystallization. During the excimer laser crystallization, the surface temperature can reach 1100$^{o}$C in 500ns which is enough to melt the Ge native oxide. Meanwhile location controlled single-grain Ge is epitaxially grown on Si seed layer. High tensile stress is formed which helps to increase the mobility. The source and drain is formed by doped Si and activated by excimer laser. Intrinsic Ge layer is added between source and channel region as well as between drain and channel region as a "diffusion barrier" to prevent dopants diffusion into channel region.

## 5.2 Location controlled Single-Grain Ge TFT

Figure 5.1 (a)-(e) show the cross section of the fabricated device: the (001) oriented Si seed has been first fabricated inside a cavity (1.2μm deep, 100nm wide) in 1.5μm $SiO_2$ by metal induced lateral crystallization (MILC) which has been reported in chapter 2: (Fig.5.1 (a)-(b)). The seed of polycrystalline Si was separated from the Si substrate with a 800nm $SiO_2$. Then a 250nm thick a-Ge layer was sputtered at a substrate temperature of 450$^{o}$C. Then a 50nm thick SiO2 layer was deposited by TEOS-PECVD at 350°C, as a capping layer for the excimer laser crystallization (ELC) and also as a part of the gate insulator (Fig.1(c)). Then the sample was crystallized by an excimer laser (λ=308nm, t=180ns) with a substrate temperature of 450$^{o}$C (Fig.1 (d)). The laser irradiation energy was varied from 600mJ/cm$^2$ to 900mJ/cm$^2$. During the laser crystallization, Ge grains epitaxial grew from the (001) oriented Si seed (Fig.5.1 (c)). After patterning the Ge into islands with the capping oxide, a 40nm additional $SiO_2$ was deposited by the TEOS PECVD. The total thickness of the gate oxide is 90nm. Then a 250nm thick a-Si was deposited as a poly-gate by LPCVD at 545$^{o}$C and implanted with $10^{16}$cm$^{-2}$ phosphorous and $10^{16}$cm$^{-2}$ boron for n-/p- channel TFTs, respectively (Fig.5.1 (d)).

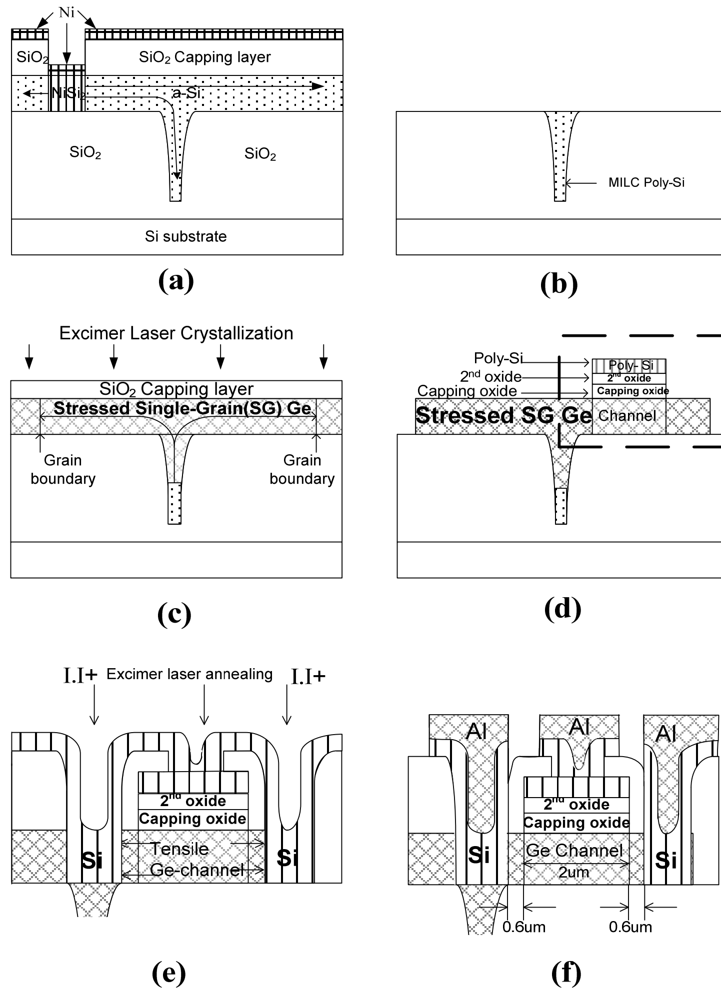


Fig. 5.1 (a)-(e) Cross sectional structure of fabricated device

Then the dopants were activated by the excimer laser annealing (ELA) with energy density of 300mJ/cm$^2$ at room temperature. The poly-Si and the gate $SiO_2$ were etched with a gate mask. After deposition of passivation $SiO_2$, contact holes for source and drain were opened. The Ge at source and drain region was etched away, leaving a 0.6μm offset of intrinsic Ge by anisotropic plasma etching (Fig.5.1 (e)). A 250nm thick a-Si was then

deposited in the opening as source and drain by the LPCVD and implanted with $10^{16}cm^{-2}$ of phosphorous and $10^{16}cm^{-2}$ of boron for n- and p-channel, respectively. Then the dopants were activated by ELA with an energy density of $300mJ/cm^2$ at room temperature (Fig.5.1 (e)). The channel width and length was 2µm for p- and n-channel TFTs. The intrinsic Ge offset suppresses dopants diffusion into the channel during the excimer laser annealing (Fig.5.1 (e)). After deposition and patterning Al pads, the sample was annealed at $400^{o}C$ in $H_2$ to passivate interface defects (Fig.5.1 (f)).

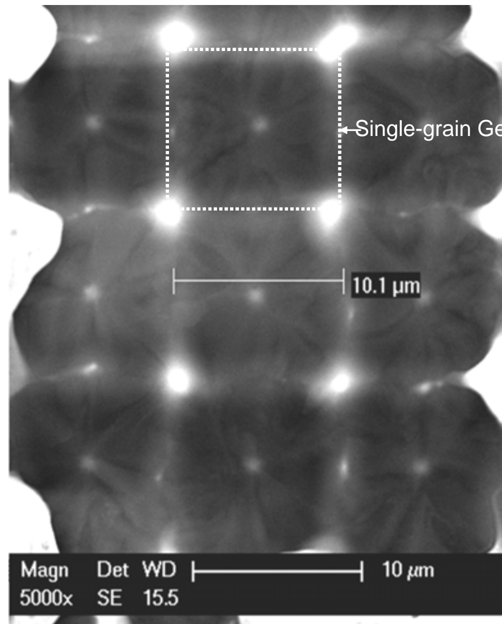


Fig. 5. 2 SEM picture of 3x3 matrix of Ge grains at predetermined positions

Figure 5.2 shows the SEM picture of Ge grains after the ELC. Ge grains with a size of 10µm have been obtained at pre-determined positions. Figure 5.3 shows the Raman spectrum of the SG Ge and single-crystalline Ge wafer as a reference. The peak of SG-Ge is at a lower wave number than that of intrinsic Ge by $3.812cm^{-1}$ which suggests high tensile stress is formed inside the SG-Ge during ELC.

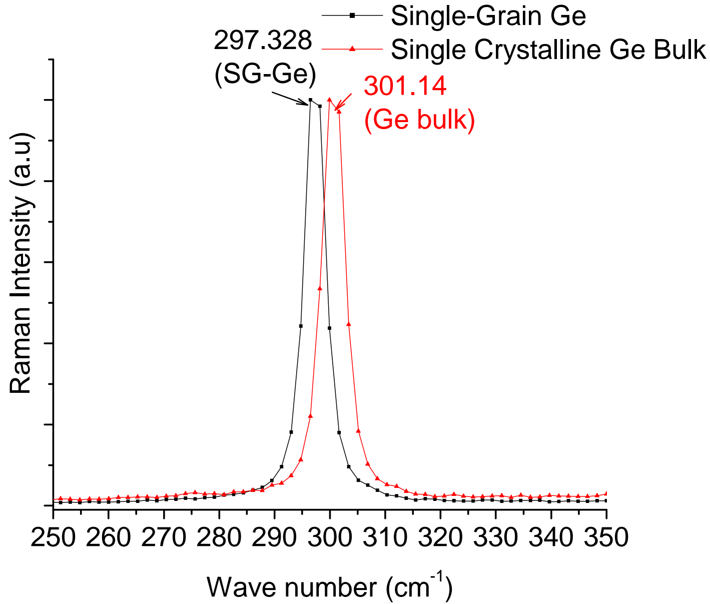


Fig. 5.3 Raman spectrum of single-grain Ge and single-crystalline Ge wafer

Figures 4 and 5 show transfer characteristics for n- and p-channel SG Ge TFTs, respectively. For n-channel, SG Ge TFT shows an effective mobility of 3337cm$^2$/Vs with a high on/off ratio of $10^8$ at $V_{DS}$=0.1V. For p-channel, SG Ge TFT shows an effective mobility of 1719 cm$^2$/Vs with a high on/off ratio of 107 at $V_{DS}$=0.05V. The S value for n- and p-channel SG TFT is 0.19/dec and 0.17V/dec, respectively. The mobility was calculated by the transconductance (gm) at $V_{th}$. The high mobility and the low S value suggest that a good interface property between the Ge channel and the gate $SiO_2$ was achieved due to melting of the GeO during ELC.

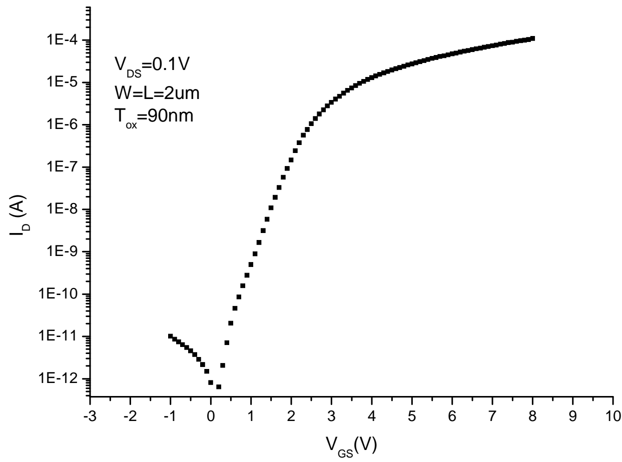


Fig. 5.4 Transfer characteristics of the n-channel SG-TFTs at room temperature

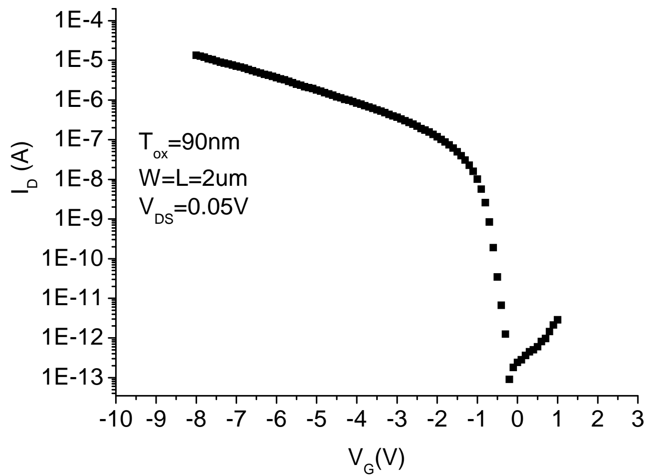


Fig. 5.5 Transfer characteristics of the p-channel SG-TFTs at room temperature

According to our transient temperature simulation, which is shown in Fig.5.6, the surface temperature of the Ge film can reach 1100°C at 180ns. The temperature is high enough to melt the GeO and form Ge-$SiO_2$ bonding there.

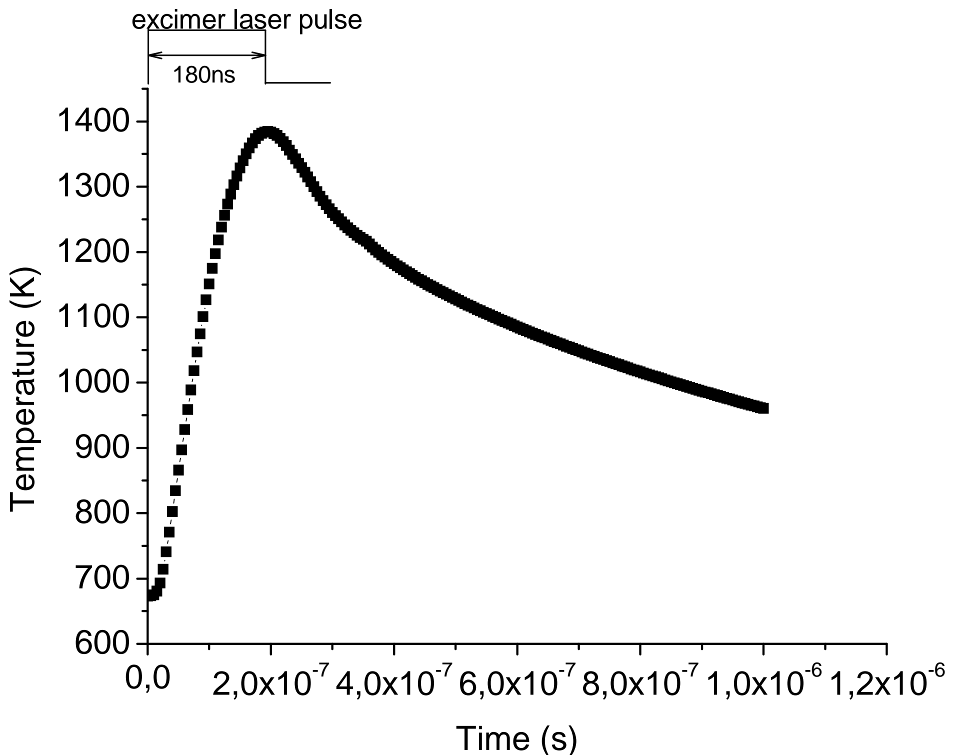


Fig.6 Simulation of surface temperature of the Ge during excimer laser crystallization

Fig.5.7 and Fig.5.8 show output characteristic of n- and p-channel devices. For both n- and p- channel devices, the current increases super linearly without break-down and do not show saturation property.

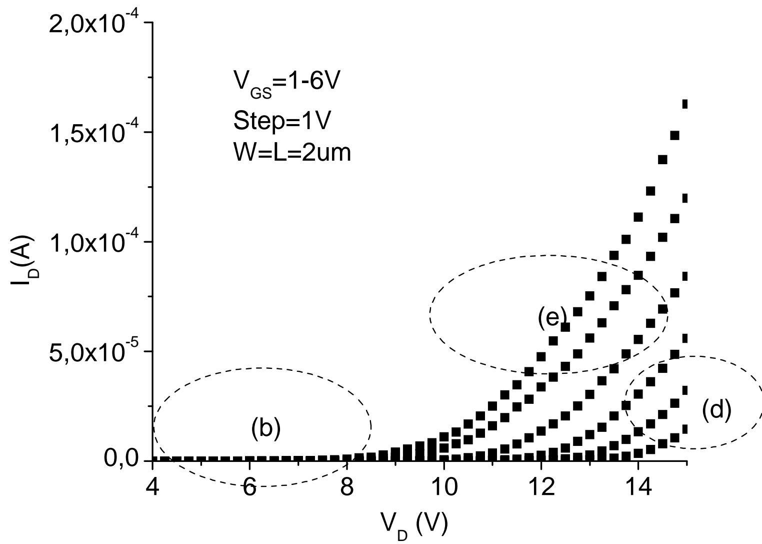


Fig.5.7 Output characteristic of the n-channel transistor at room temperature

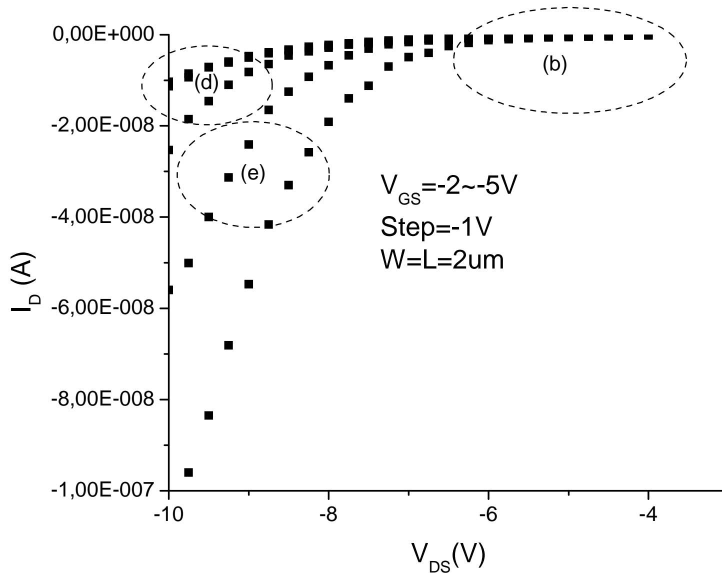


Fig.5.8 Output characteristic of the p-channel transistor at room temperature

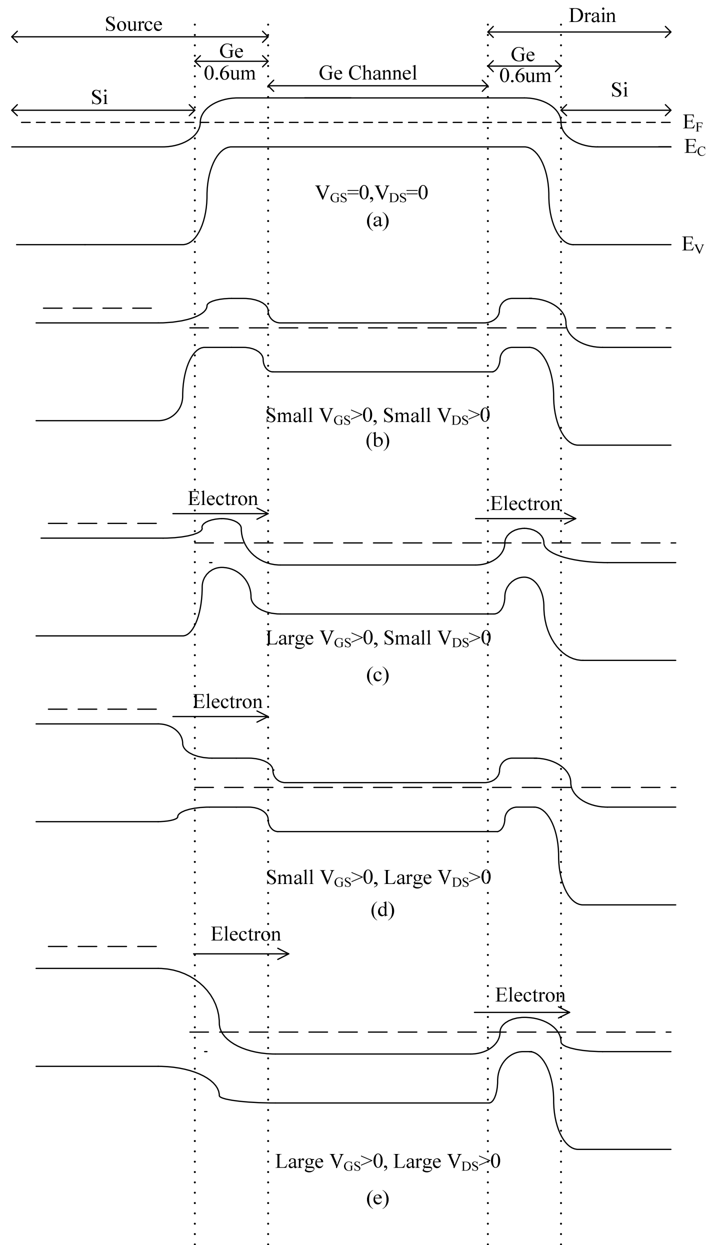


Fig.5.9 Band diagram of the n-channel Ge SG-TFT (a) $V_{GS}$=0, $V_{DS}$=0; (b) Small $V_{GS}$>0, Small $V_{DS}$>0; (c) Large $V_{GS}$>0, Small $V_{DS}$>0; (d) Small $V_{GS}$>0, Large $V_{DS}$>0; (e) Large $V_{GS}$>0, Large $V_{DS}$>0;

This is explained by the band diagram in Fig 5.9. At a low $V_{DS}$, by increasing the $V_{GS}$, the barrier between the Ge channel and the Si at the source becomes so low that electrons can be emitted through the intrinsic Ge barrier into the channel (Fig.5.9 (b) and Fig.5.7 (b)). The electron flow is hindered by the potential barrier at the Ge offset at the drain. By increasing the $V_{GS}$, the electrons are collected at the drain region due to the lowered barrier at the Ge offset at the drain (Fig.9(c)). By further increasing the $V_{DS}$, the strongly forward biased source junction emits a lot of electrons which are collected by the drain and result in high $I_D$ (Fig.5.9 (e) and Fig.5.7 (e)). The off-current was $10^{-12}$A and $10^{-13}$A for n-channel and p-channel respectively which suggest that the dopants diffusion into the Ge channel were suppressed by the Ge offset.

## 5.3 Conclusions

High performance SG Ge TFTs have been fabricated with high mobility, low off current and small S. The high mobility is due to tensile stress in the Ge channel region and a high quality interface property. The high performance SG-TFTs are attractive for application in high speed and low power electronics on a large area substrate.

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# Chapter 6

# Summary and Recommendations

## 6.1 Conclusions

This thesis focuses on growing different seed layer into grain-filter holes in order to control the orientation of the single-grain during μ-Czochralski process on glass substrate. The orientation control of single grain TFT improves the uniformity greatly. Moreover, the orientation controlled SG TFTs show superior performance when compared with SOI. Furthermore, the devices also show remarkable reliability under different electrical stress. Finally, Single-Grain Ge TFTs grown on MILC seed layer show fantastic performance which surpasses all the other single-crystalline based Ge devices so far.

**Chapter 2** proposed to use IGZO as seed layer to have (111) orientation control. (111) oriented Si has epitaxial grown on (0001) IGZO substrate successfully.

**Chapter 3** described a new approach to grow both (100) and (110) oriented Si by Metal-Induced-Lateral crystallization (MILC). The mechanism of growing (100) orientated Si is due to high tensile stress at the corner of rectangular Ni pattern. And (110) oriented Si grows from the side of rectangular Ni pattern.

**Chapter 4** proposed a novel process to reduce Ni contamination below SIMS detection limit. (100) and (110) oriented single-grain TFT has been

fabricated by combining MILC and μ-Czochralski process. Field-effect mobility of n-channel transistor is 998cm$^2$/Vs for (100) SG-TFTs and 811cm$^2$/Vs for (110) SG-TFTs. Field-effect mobility of the p-channel transistor is 292cm$^2$/Vs for (100) SG-TFTs and 429cm$^2$/Vs for (110) SG-TFTs. The orientation and location controlled SG TFT shows remarkable stability under different electrical stress. This process is very promising to integrate high performance RF circuits, logic circuit and memories directly on glass substrate.

Chapter 5 described a new technique to fabricate Ge transistors with world record high mobility and on-off ratio. By using capping oxide during laser crystallization, the GeO is melted and interface between gate oxide and Ge channel region has been improved. By replacing Ge with doped Si at source and drain, high tensile stress has been introduced and mobility has been greatly increased. Moreover, the dopants diffusion from source and drain to channel region has been suppressed. Therefore, a high on-off ratio has been achieved.

## 6.2 Recommendations

This thesis has opened an opportunity for the integration of different oriented SG-TFT direct on glass substrate with a process temperature under 600$^o$C. Based on the work done and the experience gained during the past four years, I would like to make the following suggestions for future research.

1. The process temperature of (100) and (110) oriented SG-TFTs. At this moment, the process temperature of (100) and (110) oriented SG TFTs is 600$^o$C. This is mainly limited by the MILC process. However, in principal the process temperature can be further lowered. One way is to use electric field during MILC process which can lower the process temperature below 500$^o$C. Another way is to use laser annealing during MILC process which can further lower the process temperature to room temperature.

2. In this thesis, it has been demonstrated that (111) oriented Si can epitaxial grow on (0001) IGZO film. However, it is difficult to grow (0001) IGZO film inside the grain filter holes due to the following challenges: 1) the IGZO film is normally deposited by sputtering which is difficult to fill the grain filter holes; 2) IGZO film is not compatible in standard IC fabs even in back-end process due to the contamination issues

3. In this thesis, it has been shown that it is very promising to fabricate high performance Ge transistor by excimer laser. However, in this thesis, it has been only demonstrated Ge tunneling device which shows no saturation effect due to lack off pinch-off region. In general, it is possible to apply laser annealing technology in fabricating single-crystalline Ge MOSFET. The excimer laser can be used to reduce interface defects and activate dopants in a short time. Moreover, the Si at source and drain can be epitaxially grown by CVD method to remove the defects between S/D Si and Ge channel.

# Summary

**Title: Orientation and Location Controlled Single-Grain TFT on Glass Substrate**
*By: Tao Chen*

Location controlled single-grain TFT by μ-Czochralski process has attracted a lot of interest due to its high field effect mobility which is comparable to SOI. However, the major challenge is the random orientation of the grains due to the lack of seed layer to control the orientation. This will result in poor device uniformity and limit its further application such as 3D-ICs or System-on-Glass. This thesis presents different methods to control the orientation of single-grains. The proposed methods can achieve grains with (111), (110) and (100) orientations. (100) and (110) single-grain TFTs shows not only high electron and hole mobilities, but also high uniformity which approaches to that of SOI. Moreover, the devices show more stable performance than poly-Si TFTs under different electrical. Single-Grain Ge TFTs by μ-Czochralski process shows better device performance than traditional Ge MOSFET fabricated on single-crystalline Ge wafer. It is also very promising to fabricating Ge MOSFET by μ-Czochralski process due to its unique process.

**Chapter 1** provides an overview of different TFT technologies and the challenges associated with location-controlled single-grain TFT by the μ-Czochralski process. By studying the limitation of continuous downscaling the device dimension, it has been explained how the μ-Czochralski process can be used for future 3D-ICs and System-on-Glass. The challenges on μ-Czochralski process for these applications are brought out and the motivation of this thesis is proposed.

**Chapter 2** proposes to epitaxial grow (111) oriented Si on (0001) oriented InGaZnO (IGZO). Their advantages and drawbacks are extensively discussed. The mechanism has been addressed. Also to grow (0001) oriented InGaZnO on $SiO_2$ has been proposed by applying excimer layer.

**Chapter 3** described a new approach to grow both (100) and (110) oriented Si by Metal-Induced-Lateral crystallization (MILC). The mechanism of growing (100) orientated Si is due to high tensile stress at the corner of rectangular Ni pattern. And (110) oriented Si grows from the side of rectangular Ni pattern. However, the proposed method will introduce Ni contamination problems.

**Chapter 4** proposed a novel process to reduce Ni contamination below SIMS detection limit. (100) and (110) oriented single-grain TFT has been fabricated by combining MILC and μ-Czochralski process. Field-effect mobility of n-channel transistor is $998cm^2/Vs$ for (100) SG-TFTs and $811cm^2/Vs$ for (110) SG-TFTs. Field-effect mobility of the p-channel transistor is $292cm^2/Vs$ for (100) SG-TFTs and $429cm^2/Vs$ for (110) SG-TFTs. The orientation and location controlled SG TFT shows remarkable stability under different electrical stress. This process is very promising to integrate high performance RF circuits, logic circuit and memories directly on glass substrate

**Chapter 5** described a new technique to fabricate Ge transistors with world record high mobility and on-off ratio. By using capping oxide during laser crystallization, the GeO is melted and interface between gate oxide and Ge channel region has been improved. By replacing Ge with doped Si at source and drain, high tensile stress has been introduced and mobility has been greatly increased. Moreover, the dopants diffusion from source and drain to channel region has been suppressed. Therefore, a high on-off ratio has been achieved.

**Chapter 6** presents the conclusions and recommendations of this research. The most important conclusion is that the orientation- and location-controlled single-grain TFT can achieve high performance devices, which are superior to SOI. By making use of these devices, it is promising to fabricate 3D-ICs monolithically.

# Samenvatting

**Title: Orientation and Location Controlled Single-Grain TFT on Glass Substrate**
*By: Tao Chen*

Locatie gecontroleerd een-kristal TFT fabricage door middel van μ-Czochralski processen heeft veel aandacht vanwege the hoge veld effect mobiliteit welke vergelijkbaar is met die van SOI. Echter, de grootste uitdaging is de willekeurige oriëntatie van de kristallen tengevolge van het gebrek aan controle over de oriëntatie van de kiem lagen. Dit resulteert in een s;echte uniformiteit van de componenten en beperkt mogelijk toepassing zoals 3D-IC's of systeem-op-glas. Dit proefschrift presenteert verschillende methode om de oriëntatie van een-kristallen te controleren. Met de voorgestelde methoden kunnen een-kristallen met (111), (110) en (100) orientatie worden gemaakt. (100) and (110) een-kristal TFTs vertonen niet alleen een hoge elektron en gat mobiliteit, ook de uniformiteit is hoog, deze benaderd de mobiliteit van die van SOI componenten. Bovendien vertonen een-kristal TFTs in vergelijking met poly-si TFTs een meer stabiele werking onder verschillende elektrische belastingen. Een-kristal Ge TFTs gefabriceerd met het μ-Czochralski proces vertonen een betere component gedrag dan conventioneel Ge MOSFETs die zijn gefabriceerd op een mono-kristallijn Ge wafer. Het is daarmee veel belovend om Ge MOSFETs te fabriceren met behulp van het μ-Czochralski proces.

**Hoofdstuk 1** geeft een overzicht van de verschillende TFT technologieën en de uitdagingen die zijn gerelateerd aan de locatie-gecontroleerde een-kristal TFT gefabriceerd met behulp van μ-Czochralski proces. Met een Studie over de beperkingen van het continue verkleinen van component afmetingen wordt verklaard hoe het μ-Czochralski proces kan worden ingezet voor toekomstige 3D-ICs en systeem-op-glas processen. In dit hoofdstuk worden ook de uitdagingen voor het μ-Czochralski process en daarmee de motivatie

voor het onderzoek gepubliceerd in dit proefschrift behandeld.

**Hoofdstuk 2** beschrijft de mogelijkheid om (111) georiënteerd Si epitaxiaal te groeien op (0001) georiënteerd InGaZnO (IGZO). De voor en nadelen worden uitgebreid behandeld en het mechanisme wordt besproken. De mogelijkheid om (0001) georiënteerd IGZO op $SiO_2$ te groeien door middel van excimeer laser wordt voorgesteld.

**Hoofdstuk 3** beschrijft een nieuwe benadering voor de groei van (100) en (110) georiënteerd Si door middel van metaal-geïnduceerd-laterale Kristallisatie (MILC). De groei van (100) georiënteerd Si wordt gedreven door de hoge trekspanning op de hoeken van een rechthoekig Ni patroon. Het (110) georiënteerd Si groeit vanuit de randen van het rechthoekig Ni patroon. Echter, deze methode kan problemen veroorzaken in verband met Ni gerelateerde verontreinigen.

**Hoofdstuk 4** behandelt een nieuw proces om de Ni verontreiniging te reduceren tot waarden beneden de SIMS detectie limiet. (100) en (110) georiënteerd een-kristal TFTs zijn gefabriceerd met een combinatie van MILC en μ-Czochralski processen. De veldeffect mobiliteit van de n-kanaal transistor is 998 $cm^2/Vs$ voor de (100) SG-TFT en 811 $cm^2/Vs$ voor de (110) SG-TFT. De veld effect mobiliteit voor de p-kanaal transistor is 292 $cm^2/Vs$ voor de (100) SG-TFT en 429 $cm^2/Vs$ voor de (110) SG-TFT. De oriëntatie en locatie bepaalde SG-TFT vertonen een opmerkelijke stabiliteit onder verschillende elektrische belastingen. Daarom is dit proces veelbelovend voor de integratie van hoog kwalitatieve RF schakelingen, logische schakelingen en geheugens direct op glazen substraten.

**Hoofdstuk 5** beschrijft een nieuwe techniek waarmee Ge transitoren zijn gefabriceerd met s‘werelds hoogste mobiliteit en aan-uit verhouding. Door de toepassing van een afscherm oxide tijdens de laser-kristallisatie wordt het GeO gesmolten en de overgang tussen gate-oxide en Ge kanaal gebied verbeterd. Door in de source en drain gebieden het Ge te vervangen door gedoteerd Si wordt een hoge trek spanning geïntroduceerd waardoor de mobiliteit belangrijk is verbeterd. Bovendien wordt de doopstof diffusie vanuit het source en drain gebied naar het kanaal gebied onderdrukt. Hierdoor is een hoge aan-uit verhouding gerealiseerd.

**Hoofdstuk 6** presenteert de conclusies en aanbevelingen van dit onderzoek. De meest belangrijkste conclusie is dat de oriëntatie- en plaats bepaalde een-kristal TFTs een hoge kwaliteit bezitten welke superieur is ten opzichte van SOI. Door gebruik te maken van deze componenten is het veelbelovend om 3D-IC monolithisch te integreren.

# About the author

Tao Chen was born in Shanghai, China, in 1983. He received the B.S. degree in Microelectronics from Fudan University, Shanghai in 2005, and the M.S. degree in Electronics Engineering from Delft University of Technology in 2007, Delft, Netherlands, where he continued to work toward the Ph.D. degree within the Laboratory of Electronic Components, Technology and Materials (ECTM) of Delft Institute of Microsystems and Nanoelectronics. Since April 20011, he joined NXP semiconductors and worked as “Senior Process Reliability Engineer”.

His research interests include low-temperature (<100˚C) high-performance TFTs for flexible substrate applications, location- and orientation-controlled Si single-grain TFTs, oxide semiconductors, and single-grain Ge TFTs.

# List of Publications

## Journal papers

1. **T. Chen**, R. Ishihara and Kees Beenakker: "Location and Crystallographic-Orientation Control of Si Grains through Combined MILC and μ-Czochralski process", *Jpn. Jounal of Applied Physics (JJAP), VOL 47, NO 3, 2008*

2. **T. Chen**, R. Ishihara and Kees Beenakker: "High Quality SiO2 Deposited at 80°C by Inductively Coupled Plasma Enhanced CVD for Flexible Display Application", *Electrochemical and Solid State Letters (ESSL), VOL 13, NO 8, pp J89-J91, 2010*

3. **T. Chen**, R. Ishihara and Kees Beenakker: "Location- and orientation-controlled (100) and (110) Oriented Single-Grain Si TFTs without Seed Substrate," *IEEE Transactions on Electron Devices, DOI: 10.1109/TED.2010.2055510,VOL57,ISSUE 9,pp2348-2352*

4. **T. Chen**, R. Ishihara and Kees Beenakker: "Hot Carriers Effect and Tunnelling Effect of Location and Orientation Controlled (100) and (110) Oriented Single-Grain Si TFTs without Seed Substrate" *IEEE Transactions on Electron Devices*, *VOL58, ISSUE 1, pp216-223 2011*

5. **T. Chen**, R. Ishihara and Kees Beenakker: "Solid-phase epitaxial growth of (111)-oriented Si film on $InGaO_3(ZnO)_5$ buffer layer" *Journal of Material Science, Materials in Electronics*, DOI: 10.1007/s10854-010-0237-1

6. **T. Chen**, R. Ishihara and Kees Beenakker: "High performance Single-Grain Ge TFT on Glass substrate" *Submitted to Transactions on Electron Devices,*

7. **T. Chen**, Meng-Yue Wu, Ryoichi Ishihara, Kenji Nomura, Toshio Kamiya, Hideo Hosono and C.I.M Beenakker: "Excimer Laser Crystallization of $InGaZnO_4$ on $SiO_2$ substrate" *Submitted to Journal of Material Science, Materials in Electronics*,

8. **T. Chen**, Meng-Yue Wu, Ryoichi Ishihara, Kees Beenakker: "Stress nduced Orientation Control By Metal Induced Lateral Crystallization" *To be Submitted to Journal of Applied Physics*,

# International Conferences

1. **T. Chen**, R. Ishihara, Kees Beenakker: "High Performance Single-Grain Ge TFTs without Seed Substrate" *IEEE International Electron Device Meeting (IEDM), Session 21, paper 1, San Fransisco, USA, 2010*

2. **T. Chen**, R.Ishihara, Kees Beenakker: "Integrated High Performance (100) and (110) Oriented Single-Grain Si TFTs Without Seed Substrate" *IEEE International Electron Device Meeting (IEDM), Session 8, Paper .1, pp179-182, Baltimore, USA, 2009*

3. **T. Chen**, R. Ishihara, Kees Beenakker: "Reliability of (100) and (110) Oriented Single-Grain Si TFTS without Seed Substrate" *IEEE International Reliablity Physics Symposuim (IRPS), 3F3.4, pp42-345 California, USA, 2010*

4. **T. Chen**, R. Ishihara, Kees Beenakker: "Stress Induced Orientation control by MILC", *214th Electro Chemical Society, TFT 9, 2285, Hawaii, USA, 2008*

5. **T. Chen**, R. Ishihara, Kees Beenaker: "Epitaxially grown [111] oriented Si film on a crystalline $InGaO_3(ZnO)_5$ substrate", *International Workshop on Active-Matrix Flatpanel Displays and Devices (AMFPD '09), L4, Nara, Japan, 2009*

6. **T. Chen**, R. Ishihara and Kees Beenakker: "Highly Uniform Single-Grain Si TFTs Inside (110) Orientated Large Si Grains" *Proceedings of 15th International Display Workshop (IDW), SID, AMD5-4L pp1599-1600, Niigata, Japan 2008*

7. **T. Chen** and R. Ishihara: "High quality $SiO_2$ Deposited under $100^oC$ by Inductively Couples Plasma Enhanced CVD" *International Workshop on Active-Matrix Flatpanel Displays and Devices (AMFPD '08), 43, pp 49, Tokyo, Japan, 2008*

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10. R. Ishihara, A. Baiano, **T. Chen**, J. Derakhshandeh, M.R. Tajari Mofrad, M. Danesh, N. Saputra, J. Long and C.I.M. Beenakker "Single Grain Si TFTs for RF and 3DICs" 2009 *International Conference on Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors (ULSIC vs. TFT), Xian, China*

11. R. Ishihara, J. Derakhshandeh, M.R. Tajari Mofrad, **T. Chen** and C.I.M. Beenakker "
Monolithic 3D-ICs with Single Grain Si TFTs" *Proceedings of Active-Matrix and Flat Panel Displays 2009, Tokyo, Japan*

12. Nobu Matsuki, Ryoichi Ishihara and **Chen Tao** *et al* "Local electrical properties of coincidence site lattice boundaries in location-controlled silicon islands by scanning capacitance microscopy" *International Workshop on Active-Matrix Flatpanel Displays and Devices(AMFPD07), PP 251-253, Kobe, Japan 2007*

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