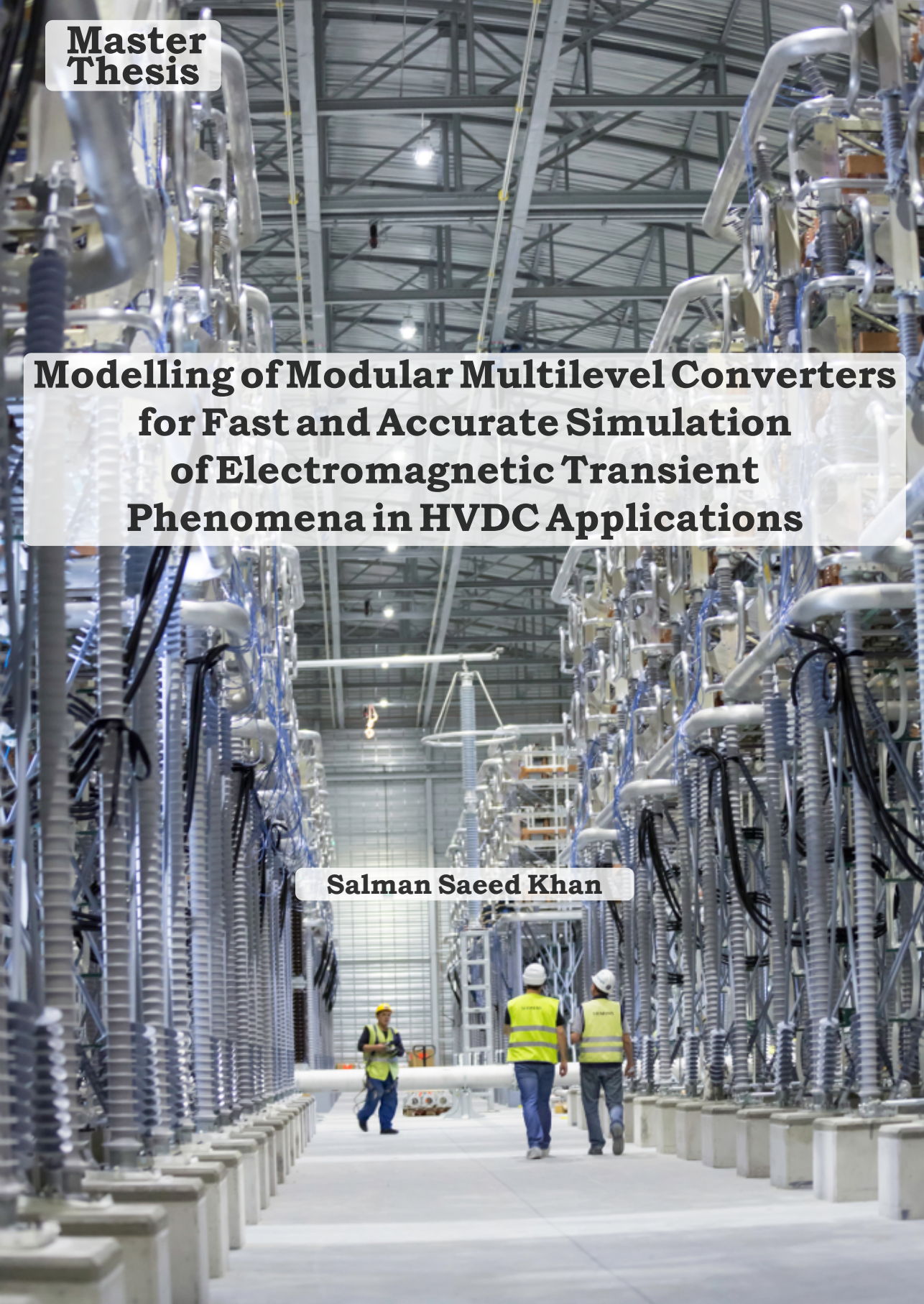
Master Thesis

Modelling of Modular Multilevel Converters for Fast and Accurate Simulation of Electromagnetic Transient Phenomena in HVDC Applications



Salman Saeed Khan

Cover Page image:
Converter hall of a converter station of the HVDC transmission link between France and Spain:HVDC Plus IGBT converter modules for 1000 MW.
Siemens Press Picture (Reference Number: IM2015040624EMEN)

Modelling of Modular Multilevel Converters for Fast and Accurate Simulation of Electromagnetic Transient Phenomena in HVDC Applications

By

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in partial fulfilment of the requirements for the degrees of

Master of Science,
Electrical Engineering,
Delft University of Technology.

Master of Science,
Technology-Wind Energy,
Norwegian University of Science and Technology.

European Wind Energy Master
Erasmus Mundus MSc programme

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Abstract

Modular multilevel converters (MMC) are gradually becoming the technology of choice in high-voltage direct current (HVDC) power transmission for grid integration of large-scale offshore wind farms and multi-terminal HVDC transmission schemes. Each phase of an MMC HVDC terminal consists of several hundreds of identical submodules that switch a module capacitor in and out of the circuit to synthesize near perfect sinusoidal ac voltages. This operation requires sophisticated control and modulation techniques. Furthermore, the design of converter, validation of control system and operational planning requires robust simulation models. To precisely model the switching operation in the converters electromagnetic transient solvers are employed. These solvers utilize numerical integration methods and nodal analysis to resolve the system in time domain.

However, the design of MMC poses a computational challenge to the classical electromagnetic transient simulations techniques. Independent operation of submodules necessitates explicit their modeling, which leads to hundreds of nodes and semiconductor devices in the equivalent models. This time-varying topology with hundreds of nodes leads to the excessive computational load on the electromagnetic transient solvers. To address this, existing literature proposes numerous efficient equivalent models for MMC based on submodule/arm's Thevenin's equivalence, switching function or average representations. The desired equivalent models for EMT studies are expected to reproduce internal and external dynamics of the converter in stationary and transient conditions. However, many of the existing models in literature lack the capability to capture the *blocked* state of operation of submodules, which finds application in the dc fault operation of the converter. Furthermore, with an extensive collection of proposed models, existing literature lacks an independent collective objective comparison of proposed models, which enable suitable selection of model based on the simulation needs.

In light of these requirements, this thesis presents a comprehensive review and enhances models from the existing literature. Moreover, using PSCAD/EMTDC simulations the proposed models are evaluated against the detailed model of the converter regarding accuracy and computational load. The simulations confirm the ability of enhanced models to capture the dynamics of converter under stationary and severe transient conditions. Furthermore, based on the simulation methods and results, the thesis addresses limitations of the proposed models and presents recommendations for their simulation applications.

In addition to the specific focus on electromagnetic transient simulation models, the thesis further aims to serve as a tutorial for the MMCs technology. Therefore the thesis presents a detailed account of MMC operation, and its associated control and modulation system.

Index Terms — High-voltage direct current (HVDC), Modular multilevel converters (MMC), Thevenin's equivalent model, Switching function models, Average value models, Electromagnetic transients.

Acknowledgment

First and foremost, I would like to express my profound gratitude to my supervisors, Prof. Elisabetta Tedeschi, NTNU Trondheim and Prof. Pavol Bauer, TU Delft. Their expertise and continuous guidance made this work possible.

Furthermore, I am grateful to Dr. Jon Are Suul, co-supervisor, for his valuable insight on the topic. In addition, I would like to acknowledge the valuable suggestions from Dr. Raymundo Torres (NTNU), Dr. Muhammad Jafar (DNV GL) and Minos Kontos (TU Delft).

I would also like to express my sincere gratitude to Dr. ir. Henk Polinder, Prof. Olav B. Fosso, and Linda Gaffel for the administrative support throughout the masters. Specials thanks are due to the Erasmus EWEM program for the financial support of my masters. Moreover, I would especially thank all of my friends in Delft and Trondheim for making the last two years memorable.

Above all, I would like to thank my parents, Saeed Khan and Shahida Khan, for their relentless support in every step of my life.

Salman Saeed Khan

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List of Acronyms

AC	Alternating Current.
APOD-PWM	Alternative Phase Opposition Disposition PWM.
AVM	Average Value Model.
C-PWM	Multi-carrier PWM methods.
CCC	Capacitor Commutated Converter.
CCSC	Circulating current suppression control.
CHB	Cascaded H-bridge Converter.
CIGRE	Conseil International des Grands Reseaux Electriques.
CSC	Current Source Converter.
CTL	Cascaded Two-Level Converter.
DC	Direct Current.
DIM	Detailed Ideal Model.
DLG	Double Line to Ground.
DQ	Direct-Quadrant.
DSBC	Double Star Bridge Cell.
DSCC	Double Star Chopper Cell.
EIM	Equivalent Ideal Model.
EMC	ElectroMagnetic Compatibility.
EMF	ElectroMotive Force.
EMT	ElectroMagnetic Transients.
EMTDC	ElectroMagnetic Transients for DC.
EMTP	ElectroMagnetic Transients Program.
FACTS	Flexible AC transmission system.
FBSM	Full Bridge Sub Module.
FCC	Flying Capacitor Converter.
FFT	Fast Fourier Transform.
HBSM	Half Bridge Sub Module.
HVAC	High Voltage Alternating Current.
HVDC	High Voltage Direct Current.
IGBT	Insulated-gate bipolar transistor.
ISM	Isolated sub-module model.

KCL	Kirchhoff's current law.
KVL	Kirchhoff's voltage law.
LCC	Line Commutated Converter.
LTI	Linear time invariant.
LU	Lower Upper.
LVRT	Low Voltage Ride Through.
MMC	Modular Multilevel converter.
MO	Modulus Optimum.
NLC	Nearest Level Control.
NLM	Nearest Level Modulation.
NPC	Neutral Point Clamped converter.
NVC	Nearest Vector Control.
OHL	Over Head Lines.
PCC	Point of Common Coupling.
PD-PWM	Phase Disposition PWM.
PGDC	Pole to Ground DC.
PI	Proportional Integral.
PLL	Phase-Locked Loop.
POD-PWM	Phase Opposition Disposition PWM.
PPDC	Pole to Pole DC.
PSCAD	Power System Computer Aided Design.
pu	per unit.
PWM	Pulse Width Modulation.
RMS	Root Mean Square.
SCR	Short Circuit Ratio.
SDBC	Single Delta configured Bridge Cell.
SFM	Switching Function Model.
SHE	Selective Harmonic Elimination.
SIL	Surge Impedance Loading.
SLG	Single Line to Ground.
SM	Sub Module.
SO	Symmetric Optimum.
SPICE	Simulation Program with Integrated Circuit Emphasis.
SSBC	Single Star configured Bridge Cell.
SSSL	Steady-State Stability Limit.
STATCOM	Static compensator.
SVM	Space Vector Modulation.

THD	Total Harmonic Distortion.
VBC	Voltage Balancing Control.
VSC	Voltage Source Converter.
ZVRT	Zero Voltage Ride Through.

List of Symbols

$\eta_{SM_i(\phi\pm)}[t]\&\beta_{SM_i(\phi\pm)}[t]$ Switching functions for SM operation.

$\overline{P_{ac_\phi}}$ Average power on ac side.

$\overline{P_{dc_\phi}}$ Average power on dc side.

$B_{(\phi\pm)}[t]$ Block Index.

C Sub-module's Capacitance.

C' Line/Cable per unit length shunt capacitance.

$D1$ HBSM upper diode.

$D2$ HBSM lower diode.

E_{MMC} Nominal stored energy in MMC.

G' Line/Cable per unit length shunt conductance.

L Arm reactance.

L' Line/Cable per unit length inductance.

L_g Converter transformer reactance.

N Number of sub-modules in an arm..

$P_\phi^\Delta(t)$ Difference of instantaneous power flow in positive and negative arms.

$P_\phi^\Sigma(t)$ Sum of instantaneous power flow in positive and negative arms.

$P_{\pm_\phi}(t)$ Instantaneous power flow in an arm.

R Arm resistance.

R' Line/Cable per unit length resistance.

$T1$ HBSM upper IGBT.

$T2$ HBSM lower IGBT.

$\hat{k}_\phi$ Current modulation index.

$\hat{m}_\phi$ Voltage modulation index.

ϕ subscript indicates the phase leg of converter.

$\pm$ subscript addresses the arms of a phase leg.

$e_{\phi}(t)$ Internal emf.

i subscript refers the position of sub-module in an arm.

$i_{Harm.\phi}^{\Sigma}(t)$ Harmonics in circulating current.

$i_{(\phi\pm)}$ Arm current.

$i_{SM}/i_{SM_i(\phi\pm)}$ Current in sub-module.

$i_{ac_{\phi}}(t)$ AC Current.

$i_{circ_{\phi}}$ Circulating current.

$i_c/i_{c_i(\phi\pm)}$ Current in sub-module's capacitor.

$i_{dc_{\phi}}$ DC component in arm current.

i_{dc} DC current.

$i_{diff_{\phi}}$ AC current component in an arm.

$n_{(\phi\pm)}(t)$ Insertion Index.

$v_{c_{\phi\pm}}^{\Sigma}$ Cumulative capacitor voltage in an arm.

$v_c/v_{c_i(\phi\pm)}$ Sub-module capacitor voltage.

$v_{(\phi\pm)}$ Voltage inserted in an arm.

$v_{SM}/v_{SM_i(\phi\pm)}$ Voltage inserted by sub-module.

$v_{ac_{\phi}}(t)$ AC Voltage.

$v_{circ_{\phi}}$ Arm voltage due to circulating current.

v_{dc} Voltage across dc terminals.

$v_{leg_{\phi}}$ Voltage inserted in a phase leg.

$i^{0}{}_{ac}(t)$ Zero-sequence component in ac current.

1

Introduction

This introductory chapter serves to state the background, the motivation behind the work, primary objectives and defines the layout of the Thesis.

1.1. Motivation and Past Work

Changing climate conditions, limited fossil fuel resources and ever increasing global thirst for energy, demand for major transformations in the energy landscape. In the last century, electric power has gradually evolved as the primary medium of energy for household and commercial consumption. With electricity sector accounting for around 24.6% of global greenhouse gas emissions [3], international treaties [1, 2, 4], summarized in table 1.1, are pushing for reduced dependency on fossil fuels and deployment of renewable energy sources. An eco-friendly electrical generation with renewable resources, e.g. hydro, the wind and solar, offers a clean and sustainable solution to the energy demand. However, integration of these resources into the traditional AC power grid poses various challenges. In most cases, renewable assets are concentrated in remote areas. In particular, for off-shore

Table 1.1: Climate Change: International Treaties and Targets

Treaty	Targets
Kyoto Protocol	"Stabilization of greenhouse gas concentrations in the atmosphere..."[1]
EU 20-20-20	20% cut in greenhouse emissions, 20% energy from renewables and 20% increase in energy efficiency *(Targets for the year 2020)*
COP-21	"Holding the increase in the global average temperature to well below $2^{\circ}C$..."[2]

wind farms, long distance submarine power cables are required for water crossings. Transmission of bulk power over long distances especially via underground and sub-sea cables turns out to be a challenging task for high-voltage alternating current (HVAC) transmission, where the innate reactance of overhead lines or cables tend to limit power transmission capability. In addition to this, integration of intermittent renewable assets, such as wind energy, with weak AC links presents additional problems.

An alternative for HVAC is high-voltage direct current (HVDC) transmission which unaffected by reactive elements of line, has theoretically no limit on transmission distance and provides a controllable mode of transmission. However, HVDC requires converters at both ends to convert from AC to DC and vice versa. Historically absence of reliable and efficient converters has been the bottleneck in the development of HVDC. Nevertheless, the recent invention of DC/AC cascaded modular multilevel converters by Lesnicar and Marquardt [5–8], offers an efficient and economically viable solution for grid integration of remote resources and bulk power transfer. This converter topology with its inherent modular and scalable configuration promises to mitigate the limitations of existing dc-ac converter technologies and is gradually becoming the choice for HVDC converters.

Modular multilevel converters (MMC) are becoming the technology of choice in HVDC power transmission for grid integration of large-scale offshore wind farms and multi-terminal HVDC transmission schemes. Each phase of an MMC HVDC terminal can consist of several hundreds of identical sub-modules that switch a module capacitor in and out of the circuit at different times to synthesize the required ac-side voltage waveform. This operation requires sophisticated control and modulation techniques. Besides this, the application-specific design of converter system presents a need for its accurate modeling and computer simulation together with the associated power system, which is essential for efficient design, validation of complex control systems, and operational planning. In power electronic systems, switching operation is integral and the prime source of transients in the system. Therefore for MMCs, Electromagnetic transients (EMT)-type solvers are utilized for the simulations. These solvers employ the solution method proposed by Dommel [9] that uses the trapezoidal rule of integration and Bergeron's method [10] for representation of lumped and distributed circuit elements in the form of time-varying current sources and conductances respectively. With this equivalent representation, step by step time domain solution of the system is obtained using nodal analysis. However, due to the non-linear characteristics of semiconductor devices and subsequent time-dependent topology, power electronic systems tend to be computationally intensive with this solution method [11, 12].

In conventional thyristor and IGBT based converters, individual valves are composed of series-connected semiconductor devices which operate simultaneously and for purposes of EMT modeling behave as a single component. To the contrast, MMCs for HVDC applications employ hundreds of sub-modules with an independent operation. Therefore, MMC simulation with explicit modeling for each semiconductor device has an enormous computational load.

To address the need for efficient MMC models existing literature presents several levels of equivalent representation. Fast and accurate simulations of EMT phenomena require models that capture all of the operating modes of the converter and allow for the natural development of its dynamics.

Such efficient models from the existing literature include:

- A simplified average model for the steady-state and dynamic behavior of MMC was investigated first by Teeuwsen [13]; however the article provides little detail on the model itself.
- Based on the *nested fast and simultaneous method* [14], Gnanarathna et al. [15] proposed an equivalent detailed model for MMC where all sub-modules in an arm are modeled with their Thevenin's equivalence. This model offers superior computational speed while retaining information for each sub-module. However, this representation does not inherently capture *blocked state* of operation of sub-modules. References [16–24] validate and present enhanced versions of this detailed equivalent model. Similar to this, Xu et al. [25] proposed an accelerated model, which partitions sub-modules from the rest of the system and mimics the interconnection with dependent sources. Reference [23, 26] validate and present enhanced versions of this model.

  Both of these representations split the computation associated with individual sub-module/arm and rest of the system. Thus, they exploit the computational efficiency of solving numerous small matrices or a set of algebraic equations instead of one large matrix and drastically increase the computational speed.
- Switching functions models for MMC are presented in [27–31]. Articles [28–30] utilize state-space formulation which is computationally intensive and not suitable for fault studies in an HVDC system. While articles Adam et al. [31] proposes a generalized switching function model that uses binary functions to model the individual operation of sub-modules with high computational efficiency.
- To address the need for very fast modeling representation, various simplified average models for MMC have been proposed in the literature [18, 32–47]. Articles [18, 32–34] extend the classical average modeling technique for 2/3-level converters [48] to MMC and represent its terminal dynamics using controlled sources; articles [35, 36] presents enhanced versions of this model, capable of simulating blocked state of operation. References [37, 38] reduce MMC to an equivalent buck-boost circuit. These representations do not inherently model internal dynamics of the converter and lack natural development of its internal and external dynamics,which are governed by arm currents, and sub-module capacitors, and therefore are only suitable for the stationary operation of the converter.

  Furthermore, articles [39, 40] present continuous models of converter based on state-space formulation and differential equation respectively; articles [41, 42] extends the latter model for the modeling capability of the *blocked* state.

These existing models provide a faithful representation of the terminal behavior of

converter. However, these models do not inherently capture all operating states of converter but instead, utilize fictitious diodes and switches to mimic *blocked* state of operation. Furthermore, the literature lacks an independent collective comparison of the equivalent models.

Therefore, this thesis aims to enhance and develop MMC equivalent representations that model all states of operation and provide a thorough review and objective comparison, regarding relative accuracy and computational efficiency, of the models that are suitable for EMT studies.

1.2. Objective

This thesis is aimed towards gaining insight in of modular multilevel converters for high-voltage direct current applications. The prime objective is to develop computationally efficient models for modular multilevel converters for simulation of electromagnetic transients.

1.2.1. Specific Objective

- Develop the understanding of operating principles of MMC.
- Investigate various control and modulation techniques for MMC.
- Investigate and develop different levels of simplified equivalent models for MMC.
- Validate proposed models of the converter regarding accuracy and computational speed against a detailed representation.

1.3. Main Contributions

The main contributions of this thesis are:

- Theoretical analysis of MMC: The thesis presents a detail mathematical formulation of internal and external dynamics of converter and optimization of the size of converter components. Furthermore, building on this mathematical formulation the thesis presents an overview of control and modulation techniques.
- Enhancement equivalent models: The primary contribution of this thesis is an independent study of existing equivalent models of MMC and enhancement in these models that enable inherent modeling all operating states of the converter and allow for the natural development of all of its internal and external dynamics under stationary and transient conditions.
- Comprehensive comparison of equivalent models: The thesis presents a detailed comparison regarding accuracy and computation speed of the equivalent models under various operating conditions.

1.4. Report outline

The report is structured as follows:

- Chapter 2 gives an overview of the need for HVDC systems against HVAC and presents a brief account of power converter technologies besides modular multi-level converters.
- Chapter 3 introduces the basic structure of MMC converter, its operating principle and develops a continuous analytical model. Furthermore, circulating currents and capacitor voltage ripple associated with converter arms are analyzed here.
- Chapter 4 provides brief mathematical derivations for optimum sizing of MMC components for given ratings and constraints.
- Chapter 5 provides a brief description of the control techniques for grid-connected converters including voltage balancing and circulating current suppression control methods for MMCs. Furthermore, a linear time-invariant model of MMC is derived and subsequently utilized in optimal tuning of MMC's dc voltage and ac-power flow side controllers.
- Chapter 6 gives a review of modulation techniques for the MMCs.
- Chapter 7 presents a very short account of the operation of MMC under AC and DC fault scenarios.
- Chapter 8 delves into the solution methods for electromagnetic transient simulations. Different levels of EMT models for MMCs from existing literature are derived and enhanced in this chapter.
- Chapter 9 presents and compares PSCAD/EMTDC simulation results for various equivalent models of MMCs under various transient conditions.
- Finally, Chapter 10 completes the thesis with discussion and drawn conclusions.

1.5. Publication

The list of publications from this thesis is as follows:

Conference Presentation: **S. Khan**, J. A. Suul, E. Tedeschi and M. Jafar, "Blocking capability for Switching Function and Average Models of Modular Multilevel Converters", *Environment and Electrical Engineering (EEEIC), 2016 16th International Conference on*, Florence, Italy, 7-10 June, 2016.

2

Background

AC and DC mode of transmission are individually viable for different applications. With generation and consumption in AC, power converters are essential for HVDC transmission. This chapter serves to give a brief account and comparison of HVAC and HVDC transmission. A short overview of the two most frequently used types of power converters is also presented here.

2.1. Modes of Transmission

Power transmission forms the critical link of connecting consumers to generation. Distributed generation and an emphasis to tap into renewable resources are pushing conventional methods of transmission to its limits. This section presents a brief account of the two modes of transmission.

2.1.1. High Voltage Alternating Current Transmission

Conventional high-voltage alternating current (HVAC) transmission systems form the backbone of electric power system. In AC systems, transformers are utilized to step up/down voltages and transfer of energy is achieved by overhead transmission lines or underground/submarine cables. Easy transformation capability, together with generation and consumption of electricity in AC has been the driving forces behind widespread use of AC systems.

For AC, the transmission line is modeled by four parameters i.e. series resistance R', inductance L', shunt capacitance C' and shunt conductance G' which are distributed along the line as illustrated in fig. 2.1. Resistance R' is dependent on conductor's resistivity and dimensions. The skin effect associated with AC tends to make R'

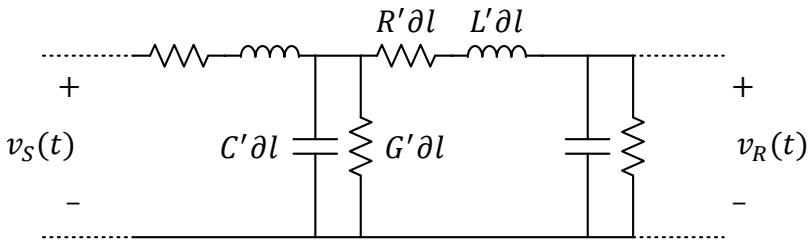


Figure 2.1: Representation of segment of a transmission line / cable

higher than that for a DC system. Series inductance L' in line is attributed to the internal and external magnetic fields. Mutual and ground coupling of conductors results in the parasitic shunt capacitance C'. Insulating medium, dimension and relative position of conductors determine these reactive parameters of line. Shunt capacitance is further affected by the conductor's proximity to the ground. Furthermore, leakage currents between conductors or between conductors and ground give rise to the shunt conductance G'.

Similar to the overhead lines (OHL) parasitic elements are present in underground and submarine cables. However, different structure, arrangement and insulation materials in cables imply a significant difference in values [49]. In comparison to OHL, conductors in cables are relatively closer to each other and the ground. Moreover, cables employ solid or a combination of solid/ liquid dielectrics which have higher permittivity, unlike OHL where the air is the dielectric medium. These conditions subsequently lead to higher shunt capacitance and lower series inductance in cables as compared to OHL.

These parameters characterize the transmission line/cable and define the power transmission capability. For an AC transmission line/cable power carrying capacity is limited by [50]:

1. Steady-state stability.
2. Thermal limits.
3. Voltage limits.

Steady-state stability

The steady-state stability limit (SSSL) is defined as "... maximum power at the receiving end of the circuit that can be transmitted without loss of synchronism if the load is increased in very small steps and if the field currents are changed after each increment of load so as to restore the normal operating conditions (usually constant terminal voltages) [51]". This limit is even applicable to lossless lines. If a system exceeds this power limit, associated machines in the system will lose synchronism.

Table 2.1: Parameters of Cable/Line

	OHL [1]	Submarine Cable[2]
Voltage level (KV)	500	500
$R'(\Omega/Km)$	0.024	0.026
$L'(mH/Km)$	0.87535	0.17507
$C'(nF/Km)$	12.992	286.9
$G'(\Omega^{-1}/Km)$	0	0

The steady state stability limit in an AC transmission lines is given by [50]:

$$P_{max} = \frac{V_R V_S}{Z'} - \frac{A V_R^2}{Z'} \cos(\theta_z - \theta_A) \tag{2.1}$$

where,
$$\begin{cases} \text{Voltage at sending end } = V_S \angle \delta \\ \text{Voltage at receiving end } = V_R \angle 0 \\ \gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} \\ Z' \angle \theta_z = Z_c \sinh(\gamma l) \\ Z_c = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \\ A \angle \theta_A = \cosh(\gamma l) \\ \text{SSS } P_{max} \text{ corresponds to } \delta = \theta_z \end{cases}$$

Figure 2.2 illustrates the impact of line length on SSSL, where P_{max} vs. transmission distance(eq. (2.1)) is plotted for typical values of an OHL and submarine cable table 2.1 with assumption $V_R = V_S$. The plot reveals that power transmission capability of a transmission line decrease with increasing length of the conductor, where cables tend to suffer more drastically with increasing distance.

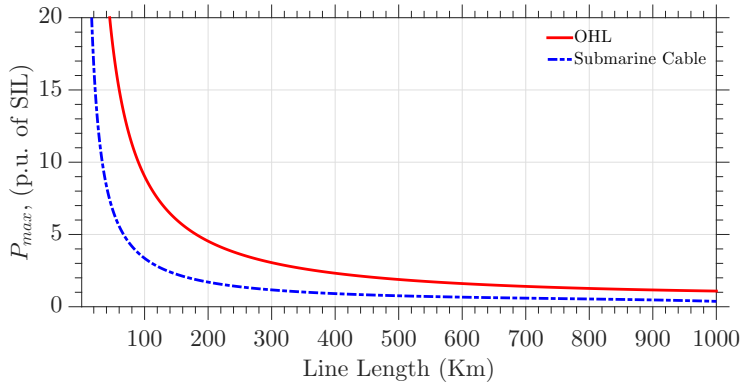


Figure 2.2: Maximum transmission capability of transmission line/cable

[1] Table 7.1 [49]
[2] Table 7.2 [49]

Thermal limits

Losses in the conductor impose thermal limits, to restrict the temperature rise and the subsequent sag in the overhead lines. The resistance of line contributes these losses; which tend to elevate in ac systems, due to the increased magnitude of the current because of the flow of reactive power.

Alternating current implies changing flux in the parasitic inductance, and this leads to consumption of reactive power by the line. Similarly, alternating voltage implies continuous charging and discharging of the parasitic capacitance which leads to the generation of reactive power. The associated reactive power produced by shunt capacitance and consumed by series reactance is given by:

$$Q_c \approx j\omega(C'l)V^2 \qquad Q_l \approx j\omega(L'l)I^2 \tag{2.2}$$

At a resistive load equal to surge impedance loading (SIL) ($\sqrt{\frac{L'}{C'}}$ for a lossless line) the reactive power consumed by parasitic inductance balances reactive power supplied by parasitic capacitance. However, with higher loads line consumes reactive power; similarly, for lower loads, there is net reactive power generation. This flow of reactive power increases the magnitude of current in lines/cables which in turn increases losses and reduces its power carrying capability as imposed by the thermal limits.

Voltage limits

In the transmission system, the voltage drop along the line is also kept within limits and this, in turn, restricts the power carrying capacity. Besides voltage drop across line resistance, reactive power flow tends to disturb the voltage profile along the line. At SIL net reactive power in line equate to zero and the voltage profile along a lossless line is flat. However, for cases when a line is lightly loaded or unloaded the effect of shunt capacitors dominate. Shunt capacitors imply flow of "charging currents" even in absence of load which are given by:

$$I_{charging} \approx j\omega(C'l)V \tag{2.3}$$

Under these conditions, there is a net production of reactive power from the transmission line; this results in a higher magnitude of the voltage at receiving end than the transmitting end. This occurs, as capacitive "charging currents" through line inductance produce a voltage in phase with the voltage at transmitting end; resulting in an increase in voltage along the line. Here both inductance and shunt capacitance contribute to voltage rise, and this voltage rise is shown to be proportional to the square of line length. This effect is known as *Ferranti's effect* after its discoverer Sebastian de Ferranti [52]. To the contrast, when the line is overloaded, parasitic series inductance dominates, and there is a voltage drop along the line.

These over-voltage and under-voltage problem at the receiving end of the line becomes more significant as the line length increases and leads to voltage control problems.

In general, power carrying capacity of short transmission lines ($< 80Km$) are restricted by thermal limits; while loadability of medium length lines ($80-100Km$) are determined by voltage limits and *steady state stability limit* defines the loadability for the long transmission lines ($> 300Km$) [50].

In conclusion, HVAC transmission is plagued by higher line losses, lower power transmission capacity, and voltage control problems. Moreover underground/submarine cables with higher shunt capacitance tend to suffer from excessive reactive power in lines adding to losses, voltage regulation problems and have lower SSSL rendering limited application for long distance transmission. To address these limitations of HVAC reactive compensation in the form of shunt reactors/capacitors is required along the line at regular distances. Furthermore, in ac power flow is dictated by line parameters and network topology and is not controllable. Additional flexible alternating current transmission system (FACTS) devices are required to make power-flow controllable. These supplementary devices add to the cost of the system and are not always feasible for the submarine cables.

2.1.2. High Voltage Direct Current Transmission

HVDC transmission, as the name states use high voltage DC current to transmit power. Direct current implies that transmission capability is unaffected by parasitic reactive elements associated with lines and is, therefore, independent of the length of cable/line. However conversion from ac to dc and dc to ac at transmitting and receiving ends, respectively, requires additional power converters in the system.

Flow of dc current and presence of converters offers various advantages over HVAC transmission as enumerated below [53–56]:

- In DC, two conductors are required for transmission, whereas three phase AC systems utilize at least three conductors. This implies that
  - HVDC offers more power transmission capability over the same network as HVAC. For similar insulation level and cross-sectional area for conductors, DC system provides 40% more power carrying capacity than that of an AC system.
  - HVDC offers a smaller footprint, reducing cost and environmental impact.
- DC systems as stated earlier are unaffected by parasitic inductive and capacitive elements of cable/line. This implies that [54]:
  - There is theoretically no limit on transmission distance.
  - No voltage control problems due to Ferranti's effect.
  - No requirement for reactive compensation along the line.
- Presence of converters on both ends of transmission line implies:
  - High-speed controllability on the power flow.

  - Limits on short-circuit currents, unlike AC where interconnection elevates fault level in the system
  - No restriction of synchronism (frequency or phase angle) on the two AC sides.
- Lower transmission losses with HVDC due to the absence of skin, proximity effect and lower corona losses.
- HVDC links act as "firewall" to propagating and expanding faults in a network [56]. In a conventional system in case of a widespread outage or a "black-out" standby generators are required to bring power plants to operating conditions i.e. "black-start". HVDC due to its ability to isolate cascading faults restrict the extent of black-out. In addition to this, the ability of some HVDC converter technologies to operate in the absence of AC grid give them a potential as "black- starters" i.e. to restore AC network in case of a black-out.

Even with of all of the advantages of DC, historically AC has been the main driving force for transmission of energy. The proliferation of AC over DC is attributed to the ease with voltages can be stepped up or down in AC systems. AC employ transformers to convert voltages to desired levels, whereas such a simple equivalent device is absent for DC systems, which has been the core reasons for the dominance of AC transmission. In the past, solutions available for HVDC converters, either as an interface between AC and DC system or between different level DC-DC systems, have been inefficient, expensive, unreliable and had a much larger footprint. The disadvantages of HVDC systems are mainly contributed to the limitation of power converter technology.

The presence of converters poses:

- Additional losses and costs at the terminals of the HVDC system.
- An additional requirement of filters at terminals to mitigate harmonics from converters. Nevertheless, multi-level converter topological allow filter-less configuration.
- An additional requirement of reactive power compensation at terminals for some power converter technologies.

The absence of reliable and efficient converters has been the bottleneck in the development of HVDC. In addition to this, lack of DC breakers is still a constraint in multi-terminal and network operation for HVDC. This has restricted the use of HVDC in the power system. Nevertheless, due to its unique characteristics, HVDC transmission finds specialized application in [53]:

1. Long distance bulk power transmission.
2. Interconnection of asynchronous systems.
3. Submarine/offshore applications.
4. DC links in AC grid for control of the power flow.

Long distance bulk power transmission is mainly used for connection of remote hydro or solar generation e.g. the 3.0 GW 940-km long HVDC link between *three gorges* and *guangdong* in China [57]. Interconnection of asynchronous systems is meant for back to back connection of two or more independent systems especially links between countries operating at different frequencies. Submarine cables have application in connecting offshore wind farms and in some cases connection of offshore oil/gas platform to shore power. HVDC links in AC grid are primarily used to strengthen the existing grid; the high-speed control offered by HVDC link aids in the stability of an AC system.

2.1.3. HVDC vs. HVAC

As discussed earlier "frequency" associated with AC systems tends to make long distance transmission far more involved than DC. On the other hand, the high cost of converters limits the feasibility of use of HVDC. Therefore, for any long distance transmission, economic analysis is necessary to determine the suitable mode of transmission. Based on this economic evaluation, the term "break-even distance" is introduced, which refers to the transmission distance at which both HVDC and HVAC have equal economic feasibility. For HVDC at break-even distance, lower line costs and lower capitalized cost of losses counterbalance the higher terminal costs, making HVDC as economically viable as HVAC [58].

To determine feasibility of HVDC vs. HVAC for a particular transmission system economic analyses is performed based on the following factors [59]:

1. Terminal Cost.
   The cost of power converters and filters to mitigate harmonics introduced by converter implies higher station cost in HVDC compared to HVAC.

2. Cable/Line Cost.
   The cost of line/cable per unit distance is lower in HVDC compared to HVAC. For similar power transmission capability, HVAC is required to have the higher rating as it suffers from the flow of reactive power and higher losses. Moreover, HVDC requires fewer conductors than HVAC and since DC peak voltage is $\frac{1}{\sqrt{2}}$ times that of AC voltage a lower insulation class is required for the HVDC lines or cables.

3. The value of losses.

An additional requirement of compensator along the line as distances increasing also adds to the cost of HVAC system. Figure 2.3 illustrates cost vs. transmission distance for typical HVAC and HVDC systems.

Technical and economic analyses presented in [60, 61] for offshore wind farms shows that economic break-even distance between HVAC and HVDC is around 35-90 Km. Similarly, for the case of overhead lines break even distance is around 500-800 Km [55].

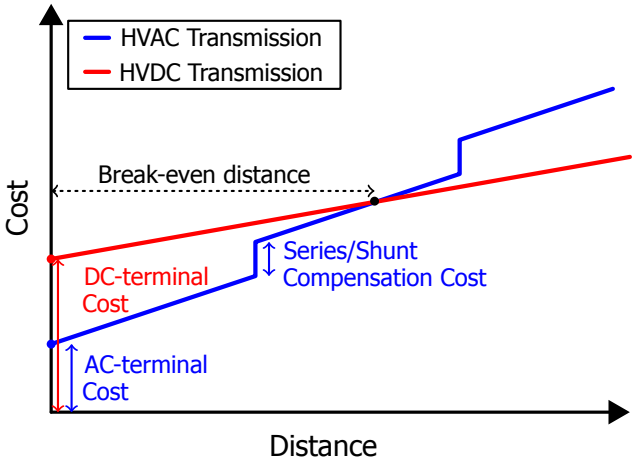


Figure 2.3: AC vs. DC Transmission Cost over distance

2.2. HVDC Converters

With generation and consumer supply at AC voltages, converters are essential for HVDC transmission. HVDC converters date back to late 19th century when rotatory converters i.e. electrical machines were used as mechanical rectifier and inverters. With the invention of mercury arc valve in early 20th century these expensive, inefficient and high maintenance rotary converters were gradually replaced by mercury arc line commutated converters (LCC). Mercury arc valves converters for commercial HVDC transmission were first employed in 1954 for the HVDC link connecting Swedish mainland and the island of Gotland [62]. Development of solid state devices led to the replacement of mercury arc valve by solid state thyristor. Solid state thyristor valves offer various advantages over mercury valves; they are free of poisonous mercury, offers fewer losses and are less susceptible to re-strikes during transient fault events. The first thyristor valves only commercial converter was employed in 1972 by Canadian General Electric and NB Power at Eel River for HVDC transmission [63]. Further research in high power electronics gave way to insulated-gate bipolar transistors which unlike thyristors has the additional ability of controlled turn-off of current. This development led to voltage source converters (VSC), the first HVDC transmission with VSC converters commercial installed in 1997 power between Hellsjön and Grängesberg in Sweden [64].

At present both LCC and VSC are commercially used for HVDC converters, LCC with high power capability is the preferred choice for overhead lines whereas VSC with a smaller footprint and "black-start" capability is preferred for offshore wind farms. For now, HVDC converters are expensive, and the added cost of converters at the transmitting and receiving ends need to be offset by the energy saved due to lower losses, making HVDC financially unviable for short distances.

2.2.1. Current-source/Line-Commutated Converters

Line-commutated means that commutation process is dependent on the line voltage of the associated AC system. Line-commutated converters employ mercury valve or thyristor as the commutation device. The thyristor is a semi-controllable semiconductor device, i.e. a forward biased thyristor can be turned on at desired instant with the gate signal. However, the gate signal offers no control over the turn-off instant, which naturally occurs if the current through thyristor drops below the "holding current".

A six pulse bridge converter illustrated in fig. 2.4 forms the building block for LCC converter. It comprises of two thyristors per phase leg that allow or inhibit the flow of current in synchronized manner to get the desired operation. The term "six" refers to six commutations in converter per cycle, resulting in a pulsed voltage waveform [56]. The waveform on the dc side is made up of line-line voltage pulses and at any instant in time exactly one of the two thyristors in each leg is conducting. Each thyristor conducts for an angle of $\frac{2\pi}{3}$ radians. For HVDC transmission, the inverter end sets the dc voltage whereas rectifier end controls the dc current by regulating the voltage difference. Delay/firing angle (α), i.e. delay of gate pulse from the instant when the thyristor is forward biased, provides control for the thyristor and consequently operation of the converter. For $0 \leq \alpha \leq \frac{\pi}{2}$ converter has rectifier operation and for $\frac{\pi}{2} \leq \alpha \leq \pi - \gamma_{min}$ it works as an inverter.

For HVDC systems mostly used configuration is the twelve pulse bridge arrangement fig. 2.5. This topology comprises of two six pulse bridges, phase shifted by $30°$, connected in parallel on AC and series on the DC side. This configuration eliminates fifth and seventh harmonics [65, 66].

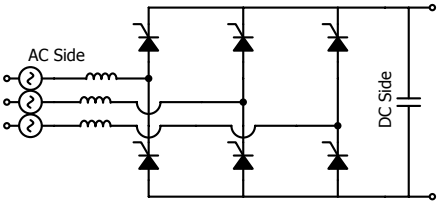


Figure 2.4: Six Pulse bridge converter

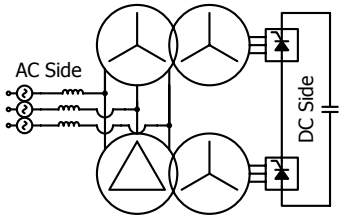


Figure 2.5: Twelve Pulse converter

The limitations of thyristor-based converters and their impact are as follows:

- For the operation of LCC synchronous voltage source is required. This implies that LCC cannot operate in the absence of AC grid and hence doesn't have any "black-start capabilities". Also due to this LCC does not perform well with weak AC grid and requires short circuit ratio (SCR) ≥ 2 i.e. the short circuit capacity from the AC grid $\geq$ two times the converter rating [56].
- LCC only operates at lagging currents. Therefore, the converter consumes reactive power. This reactive consumption varies with load hence switched reactive

compensation is required. This adds to the cost and footprint of the converters limiting its use in offshore transmission.

- LCC converters inject harmonics on the AC and DC side. Therefore, filters are required which again add to cost and footprint of converter restricting its use in offshore transmission.
- Two quadrant operation of LCC i.e. bidirectional voltage and unidirectional current implies that to reverse the direction of power in an LCC based HVDC link voltage polarity on both LCC has to be reversed. This reduces the speed with which power direction can be changed and makes it unsuitable for multi-terminal HVDC system.

Despite these shortcomings, LCC with its technological maturity, higher voltage blocking capability, higher efficiency, lower cost, and reliability makes it the technology of choice for long distance high power transmission via overhead lines.

A variant of LCC is capacitor commutated converter which employs series capacitor bank between the AC side of converter and converter transformer. The advantages of CCC contributed to series capacitors are:

- The series capacitors are the source of reactive power and hence reduce the requirement of reactive compensation for the converter and can operate with leading power factor.
- The converter can perform well even with weak AC grids.

However, CCCs are more expensive and have poor dynamic response under unbalanced conditions [67].

2.2.2. Voltage-Source/Self-Commutated Converters

Development of fully controllable semiconductor like insulated-gate bipolar transistors gave way to the VSC. With IGBTs both the turn-on and turn-off instances are controllable from the gate signal. Schematic of such a VSC-converter is shown below fig. 2.6. Similar to LCC it comprises of three phase legs with AC node in the middle. A capacitor on DC side maintains a constant voltage. There are two semiconductor valves together with anti-parallel diodes per leg. The anti-parallel diode with valve allows for current to change polarity in the converter and is responsible for carrying phase displaced currents for reactive power flow. For high voltage application, each valve (arm) constitutes of a large number of series connected IGBT's and state of the art gate drive circuitry to ensure simultaneous switching. This converter is termed as the two-level converter as the voltage on AC side can only have two level i.e $+U_d, -U_d$.

For VSC AC voltage waveform is obtained through various modulation techniques of which sinusoidal pulse width modulation and space-vector modulations techniques are the most common. These modulation techniques enable converter to synthesize desired amplitude, frequency, and phase for the ac wave-forms which in turn

enables an independent control of real and reactive power in a grid connected system. The current bi-directional capability of self-commutated valves in VSC offers various advantages over LCC. These includes [58, 64, 66]:

- Pulse width modulation [68] carried at high frequency, ensures harmonics are of higher order. This results in reduced requirement of filters in VSC; reducing cost and footprint of the converter station.
- Decoupled control of real and reactive power implies that:
  - VSC does not require reactive power compensation. This reduces cost and footprint of the converter.
  - VSC possess superior voltage stability and transient characteristics.
- VSC can operate in passive systems, i.e. absence of AC grid, and behave in a similar manner to a synchronous generator; i.e. generate frequency and voltages and therefore have a potential use as "black-starters". Compare to conventional black-start methods VSC offers reduced restoration time, safer and smoother recovery process together with lower investment and maintenance cost [69].
- In VSC power flow can be reversed by changing current direction. In multi-terminal HVDC, this allows for reversal of power at any terminal independent of other terminals.
- Unlike twelve pulse LCC converter, there is no requirement of specialized transformers.

On the downside, high switching frequency required by PWM implies greater losses in VSC. Simultaneous switching of series connected switches, stresses imposed on valves at higher voltage require considerations in design and limits the voltage rating of VSC.

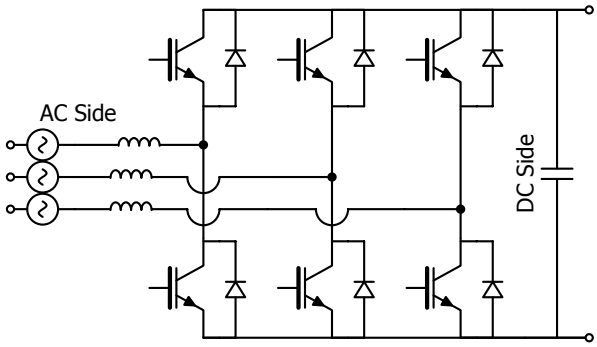


Figure 2.6: Two level Voltage Source Converter

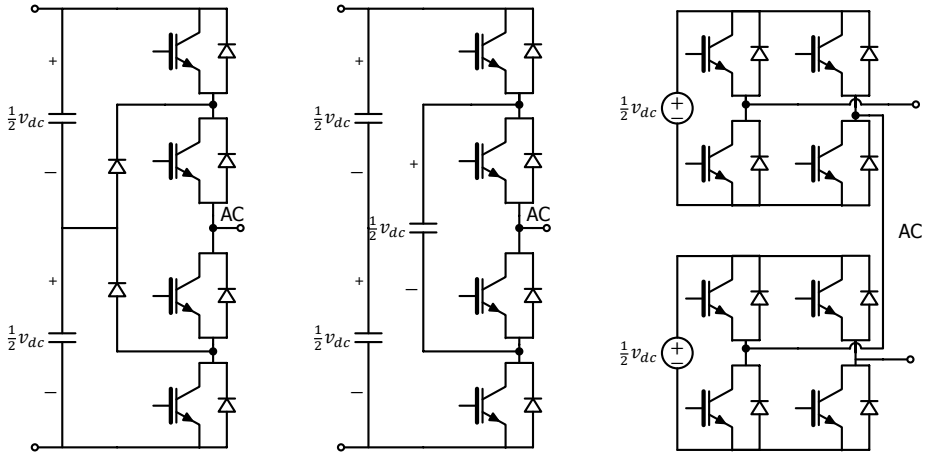
2

Multilevel Converters

Traditionally both CSC and 2-level VSC have an extensive application from HVDC transmission to industrial processes. However to meet the needs of higher voltage and higher power operation these topologies require semiconductors with higher ratings, which are not only expensive but tend to aggravate the shortcomings of these technologies. On power ratings, thyristor-based converters have an advantage over IGBT based VSC. While for VSC's, research has led to the development of multilevel variants of VSC e.g. neutral point clamped converter (NPC), flying capacitor converter (FCC) and cascaded H-bridge converters (CHB) which enable high power capabilities with traditional semi-conductors.

Multilevel converters are defined as, "power-conversion systems composed of array of power semiconductors and capacitive voltage sources that, when properly connected and controlled, generate a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude" and in addition, each phase leg can generate at least three voltage levels [70]. These converters employ traditional medium voltage semiconductors which with complex circuit and control attain higher nominal power. Moreover, this topology results in reduced harmonic content in ac-waveform, increased efficiency, near sinusoidal ac-currents, improved power quality and consequently lower requirement of filtering [70]. Articles [70, 71] present a detailed overview of NPC, FCC, and CHB multilevel converters. Despite the advantages of these multilevel topologies, converters owing to their complex circuit structure and specialized requirements have restricted widespread use of these converters.

Overall, VSC contributed to their "black-start" ability and dynamic voltage control have applications in weak grid systems. Particularly for offshore HVDC systems limited space on platforms benefits from the smaller footprint of VSC.



(a) NPC - 3 levels (b) FCC - 3 levels (c) CHB - 5 levels

Figure 2.7: Classical Multilevel Topologies

3

Modular Multi-Level Converter

MMC is a newly realized topology of VSC and prime interest in this thesis. This chapter describes the design of the converter and its operation.

Recent invention of DC/AC modular multilevel (cascaded) converters by Lesnicar and Marquardt [5–8] and its AC/AC counterpart [72–75] is a breakthrough in high power converters technology. It offers a state of the art solution to limitations of previous converters and is gradually becoming the technology of choice in HVDC power transmission for grid integration of large-scale offshore wind farms and multi-terminal HVDC transmission schemes.

MMC offers various advantages over conventional LCC and VSC. These benefits are attributed to its modular and multilevel configuration and will become obvious from the operating principles explained in the following sections. However to lay stress on the significance of MMC, key advantages as described in [5–7, 76–79] are enumerated below:

- Modular realization:
  - Composed of identical modules, no central element.
    The absence of central storage or dc-link capacitors simplifies the protection against short circuits [5].
  - Scalable to any power or voltage level.
    MMC is scalable to any voltage and power level just by variation in the number of sub-modules.
  - Cheaper mass production - standard components.

- Fail-safe operation - redundant sub-modules.
  During operation, the control algorithm can replace a faulty sub-module with a redundant sub-module. Thereby ensuring continued operation and the failed module can be replaced at scheduled maintenance.

- Multilevel waveform:
  - Low harmonic content - near sinusoidal waveform.
  - Smaller and simpler filters reduced footprint.
    With sufficiently large number of levels, filters are no longer required
  - Reduced switching frequency - lower switching losses.
    With the multilevel configurations, the effective switching frequency equals $2Nf_{sw}$ [80]. This implies a reduced requirement for switching frequency in MMCs. Comparison of switching and conduction losses of semiconductors as investigated in articles ([81, 82]) reveals higher efficiency of MMCs as compared to 2-level VSCs.
  - Individual switches only experience a fraction of DC voltage therefore unlike classical VSC there is no extensive requirement of a series connection of IGBTs.

Furthermore compared to existing multi-level VSC topologies (NPC, FCC, and CHB), MMC modular and multilevel configuration offers superior characteristics:

- MMC's strictly modular design enables its scalability to any number of voltage levels. Whereas in NPC and FCC converters the design complexity significantly increases with the number of levels and therefore traditionally the number of levels in NPC and FCC converters are kept to three and four levels respectively [71].
- Also, unlike NPC and FCC converters, MMCs do not employ dc-link capacitors and consequently offer superior fault characteristics [6].
- CHB converters have the similar modular and multilevel configuration as MMCs. However, this topology requires independent and isolated dc-sources which are traditionally provided by the non-standard multi-pulse transformer[71]. To the contrast, MMC's solely utilize off-the-shelf components.

On the down side, [43, 79, 83]:

- MMCs require more IGBTs and diodes as compared to two-level VSC.
- Each sub-module requires its very own capacitor and therefore, MMCs are less compact.
- Stored energy in MMC is higher than that of two-level VSC or three-level NPCs [79].
- High number of sub-modules requires complex control techniques.

Table 3.1 presents the comparison of MMCs to classical 2-level and multilevel converters regarding topology and components.

Table 3.1: MMCs vs. Classical VSCs

Type of VSC	*Modular*	*Multilevel*	*No. of semiconductor devices/ϕ* [1]	*No. of capacitors/ϕ*	*Off the shelf components*	*Control complexity*	*Comment*
2-Level	✗	✗	SW=2	1	✓	–	–
NPC	✗	✗	SW=$2(M-1)$ CD=$(M-1)(M-2)$	$M-1$	✓	DC-link capacitors voltage balancing	Industrial use limited to 3-levels.
FCC	✓	✓	SW=$2(M-1)$	$\frac{M}{2}(M-1)$	✓	Capacitor voltage balancing	Industrial use limited to 3-levels.
CHB	✓	✓	SW=$2(M-1)$	$\frac{M-1}{2}$	Isolated dc sources	–	–
MMC (HBSM)	✓	✓	SW=$4(M-1)$	✓	✓	SM capacitors voltage balancing	–

MMC with its break-through advantages is being developed by all of the major power converter manufacturers. At present it is being commercialized by Siemens as HVDC Plus [84–86], by ABB as cascaded two-level converter in their existing VSC technology - HVDC Light® [80], by Alstom as HVDC MaxSine® [87] and Mitsubishi electric plans to roll-out their MMC based SVC-Diamond™ in or after the year 2016 [88].

A number of HVDC-links based on MMC are already under operation. These include 85-kilometer Trans-Bay Cable in San Francisco, with power transmission capability of $400MW$ at $\pm 200kV$ developed by Siemens [89]; HVDC link rated at $2000MW$ at $\pm 320kV$ between France and Spain developed by Siemens [90].

However, this converter technology is yet far from its maturity. The complex control and modulation techniques that accompany MMC, which are the driving forces behind many of its advantages, are of key interest in literature. Besides, dynamic modeling of the MMC, which is essential for the assessment of the converter's performance within a power system and the validation of control schemes, are of prime interest in recent studies.

[1] SW = IGBT and anti-parallel diode, CD= Clamped Diode, M= No. of levels.

3.1. Design

MMC converters are based on the ”cascade connection of multiple bi-directional chopper cells or single-phase full-bridge cells” [91]. A three phase MMC comprises of three legs and based on their circuit configuration MMCs can be classified as [91, 92]:

- Single-Star configured bridge cells MMC (SSBC)
- Single-Delta configured bridge cells MMC (SDBC)
- Double-star-configured MMC
  - Double star chopper cells (DSCC)
  - Double start bridge cells (DSBC)

The article ([91]) presents a detailed comparison and application examples of these configurations. However, only *double-star configured MMC (DSCC & DSBC)* permits a common dc-link. Therefore, DSCC and DSBC have an application as HVDC converter and are of interest in this study.

Figure 3.2 illustrates a double-star-configured MMC. Each phase leg of the converter comprises of two arms; that connect dc and ac terminals through N cascaded/series sub-modules (SMs), and an arm reactor (L). Resistance, R, models the losses as-

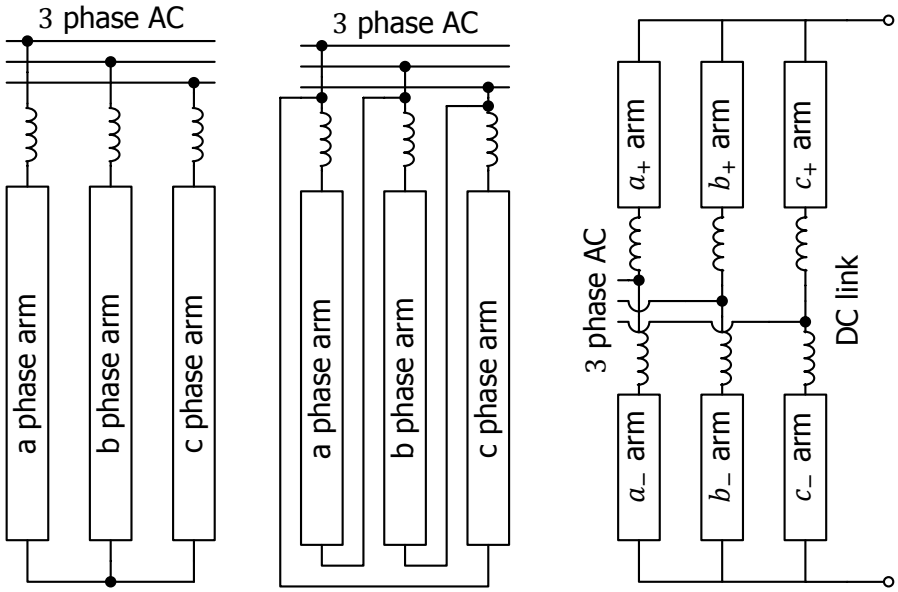


Figure 3.1: MMC - Classification

sociated with each arm and inductance L_g models the converter transformer reactance. Based on the design of sub-modules, double-star configured MMC are split into DSCC and DSBC.

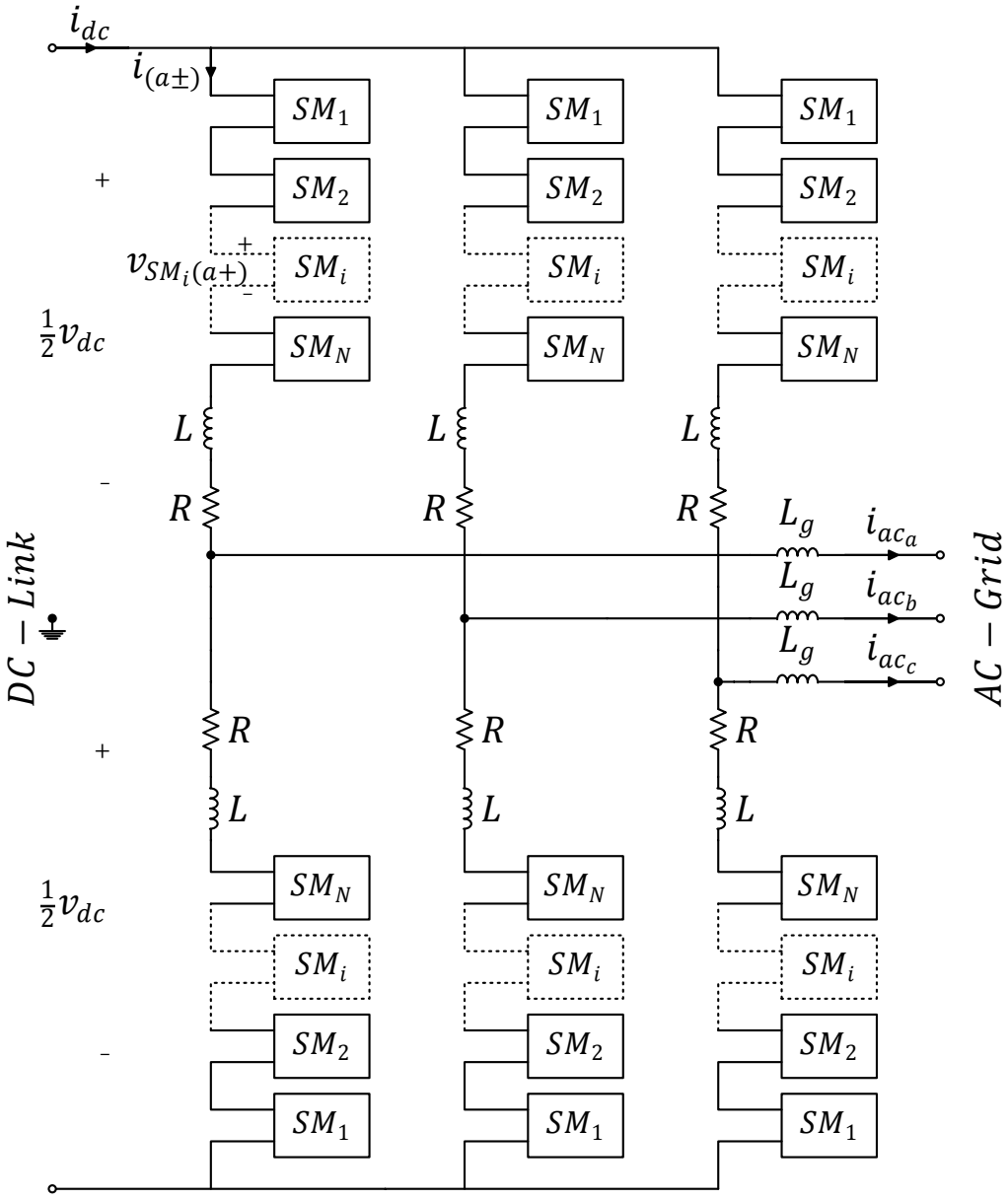


Figure 3.2: Double-star-configured MMC

3.1.1. Sub-Modules

Sub-modules are two terminal devices, composed of an IGBT-based converter and a capacitor. These modules enable the conversion operation of the converter and based on their circuit configuration are categorized as follows.

Half bridge Sub-Module

Half bridge sub-Modules (HBSMs) are chopper cells i.e. they comprise of two IGBTs with freewheeling diodes and a capacitor as illustrated in fig. 3.3. The output voltage from each SM can be the capacitor voltage v_C or $0\ V$. Therefore with this topology, each arm in MMC behaves as a controllable, unipolar voltage source [83]. Table 3.2 describes all possible switching states of the HBSM.

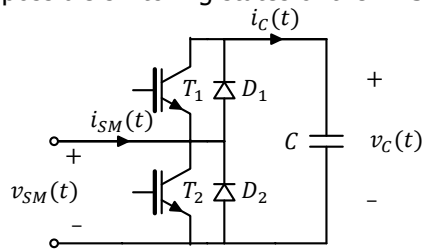


Figure 3.3: Sub-Module Half Bridge

With complementary operation of IGBTS a sub-module can insert v_C (inserted) or $0V$ (bypassed) based on gate signal $(T1, T2)$ irrespective of direction of current. In addition to this, turn off of both switches results in a *blocked state* where freewheeling diodes allow the flow of current and their conduction is dependent on the voltage across and current through them. SM in *blocked* state is *inserted* if arm current is positive with the upper diode (D1) forward biased or is *bypassed* with negative arm current via forward biased lower diode (D2) otherwise the reverse biased diodes lead to chopping of current.

With half-bridge SMs, the converter cannot suppress DC side faults. IGBTs in the half bridge cell are turned off in the case of a dc side fault, but the presence of the freewheeling diode implies that the module behaves like an uncontrolled diode rectifier, and restricts current flow in one of the two potential directions. Therefore, additional components e.g. DC breakers or breakers on the AC feed are necessary for this configuration [83]. Nevertheless *blocked* state of sub-modules prevents discharge of capacitors in case of a dc-side fault, unlike VSC, which adds to fault damage. This topology of sub-modules yields DSCC-MMC which is the focus of this study and here-forth will be simply referred as the *MMC*.

Table 3.2: Operation of Half Bridge Sub-Module

State	T1	T2	v_{SM}	i_{SM}	Capacitor
Inserted	ON	OFF	v_C	> 0	Charging - via Diode D1
				< 0	Discharging - via IGBT T1
Bypassed	OFF	ON	0	> 0	None - bypassed via IGBT T2
				< 0	None - bypassed via Diode D2
Blocked	OFF	OFF	v_C	$i_{SM} > 0$ & $v_{SM}(t-\Delta t) \geq v_C(t-\Delta t)$	Charging - via Diode D1
			0	$i_{SM} < 0$ & $v_{SM}(t-\Delta t) \leq 0$	None - bypassed via Diode D2
			–	$Else$	None and $i_{SM} = 0$

Full bridge Sub-Module

FBSM comprises of four IGBTs with freewheeling diodes and a capacitor as illustrated in fig. 3.4. The output voltage from the module can be the zero, positive of capacitor voltage v_C and negative of capacitor voltage $-v_C$. Hence with full bridge module, each arm/multivalve behaves as a controllable, bipolar voltage source. Table 3.3 describes all possible switching states of the FBSM. With a full bridge configuration, the converter can suppress arm currents in any direction.

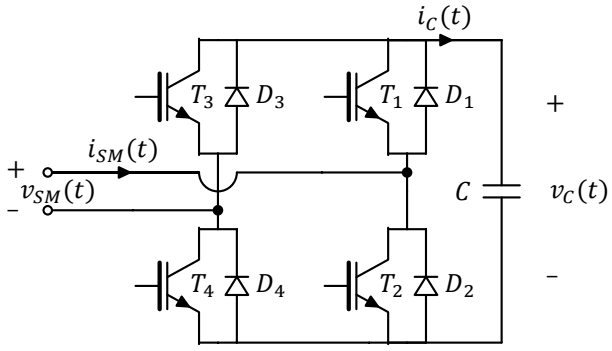


Figure 3.4: Sub-Module Full Bridge

This topology of sub-modules yields DSBC-MMC. Full-bridge operation allows the converter to be utilized as three to single phase converter as investigated in [72–75]. For dc-ac conversion, this converter with its buck and boost function of dc-link voltage allows for greater variation in the dc-link voltage [91]. Also, the ability to switch to reverse polarity aids in mitigation of dc side fault. The reverse polarity voltage contributes as negative back e.m.f. suppressing dc fault currents [17, 93].

Compared to HBSM, FBSM requires twice as many IGBTS and diodes and hence also have higher losses [82]. Besides these half and full bridge other configurations for sub-modules e.g. clamp double [77], three-level FCC/NPC and five-level cross-connected [94] have been proposed. However compared to the rest HBSM employ the least number of IGBTs and diodes, yielding minimal losses and are the SM of choice for HVDC application. Hence, throughout this thesis HBSM configuration is being considered for analysis and simulation.

Table 3.3: Operation of Full Bridge Sub-Module

State	T1	T2	T3	T4	v_{SM}	i_{SM}	Capacitor
+ Inserted	ON	OFF	OFF	ON	v_C	> 0 < 0	Charging - via Diode D1 & D4 Discharging -via IGBT T1 & T4
− Inserted	OFF	ON	ON	OFF	$-v_C$	> 0 < 0	Discharging - via IGBT T2 & T3 Charging - via Diode D2 & D3
Bypassed	OFF	ON	OFF	ON	0	> 0 < 0	Bypassed - via IGBT T2 & Diode D4 Bypassed - via IGBT T4 & Diode D2
	ON	OFF	ON	OFF	0	> 0 < 0	Bypassed - via IGBT T3 & Diode D1 Bypassed - via IGBT T1 & Diode D3

3.2. Operating Principle

This section delves into the operating principles of the MMC and an individual SM. In the subsequent mathematical formulation following notion is followed:

- ϕ indicates the phase leg of converter and $\phi \in \{a, b, c\}$.
- $\pm$ addresses the positive/upper or negative/lower arms of a phase leg.
- i refers the position of sub-module in an arm $i \in \{1, 2, \ldots, N\}$.

3

3.2.1. Sub-Module Operation

As discussed earlier a SM can operate in three different states:

- *Inserted* state
- *Bypassed* state
- *Blocked* state

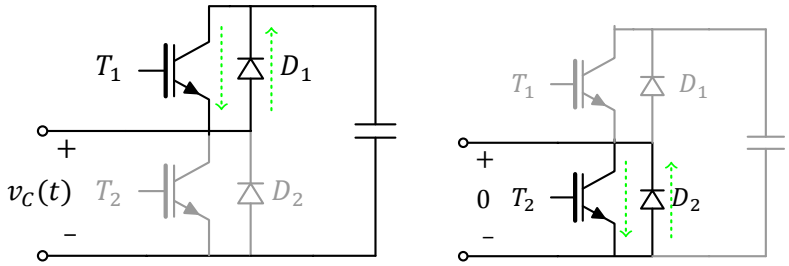
In *inserted* and *bypassed* state upper and lower valve of SM allow bi-directional flow of current, respectively as illustrated in fig. 3.5. Thereby, *inserted* state inserts capacitor across SM's terminal adding voltage in an arm and allow charging/discharging of SM's capacitor. Whereas, *bypassed* state shorts SMs terminal and keeps SM's capacitor isolated. *Inserted* and *bypassed* states are utilized in the nominal operation of the converter and allow control of voltage across a sub-module and its capacitor. The dynamics of an SM in *inserted* and *bypassed* states are described as:

$$v_{SM_i(\phi\pm)}(t) = \eta_{SM_i(\phi\pm)}[t]\ v_{c_i(\phi\pm)}(t) \tag{3.1}$$

$$i_{c_i(\phi\pm)}(t) = \eta_{SM_i(\phi\pm)}[t]\ i_{SM_i(\phi\pm)}(t) \tag{3.2}$$

$$v_{c_i(\phi\pm)}(t) = \frac{1}{C}\int_0^t i_{c_i(\phi\pm)}(t)dt \tag{3.3}$$

$$\eta_{SM_i(\phi\pm)}[t] \in \{0(\text{Bypassed}), 1(\text{Inserted})\} \tag{3.4}$$



(a) Sub-Module Inserted (b) Sub-Module Bypassed

Figure 3.5: SM - Nominal Operation

Where,
- $i_{SM_i(\phi\pm)}$, current in $SM_i = i_{(\phi\pm)}$, current in corresponding arm,
- $i_{c_i(\phi\pm)}$ is the current flowing through SM_i capacitor,
- $v_{c_i(\phi\pm)}$ is the voltage across SM_i capacitor,
- $v_{SM_i(\phi\pm)}$ is the voltage inserted by a SM_i .
- C is the capacitance of a SM's capacitor .

In the *blocked* state of sub-module both IGBTs (T_1,T_2) are turned off, and only diodes ($D1, D2$) based on their conduction state allow the flow of current as illustrated in fig. 3.6. Therefore, based on conduction state of diodes ($D1, D2$) in this state sub-modules can be:

Blocked State:
- Inserted, if $D1$ conducting
- Bypassed, if $D2$ conducting
- Opened, if both $D1$ & $D2$ are not conducting

Blocked state is utilized to prevent discharge of SM capacitors in case of a DC side fault and for charging through start-up resistance. It can be represented by modeling the commutation process of diodes. However, the mathematical formulation in this chapter does not consider the *blocked* state of operation.

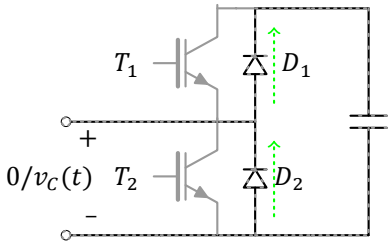


Figure 3.6: Sub-Module Blocked

3.2.2. Arm Operation

Independent and selective control of all SMs implies that each arm acts a variable voltage source; this enables independent control of voltages at AC and DC terminals.

Series/cascaded configuration of all sub-modules in arm imply that MMC's nominal operation (*Inserted & Blocked state only*) can be expressed as:

$$v_{(\phi\pm)}(t) = \sum_{i=1}^{N} v_{SM_i(\phi\pm)}(t) = \sum_{i=1}^{N} \eta_{SM_i(\phi\pm)}[t] v_{c_i(\phi\pm)}(t) \tag{3.5}$$

$$v^{\Sigma}_{c_{\phi\pm}}(t) = \sum_{i=1}^{N} v_{c_i(\phi\pm)}(t) = \sum_{i=1}^{N} \frac{1}{C} \int_0^t \eta_{SM_i(\phi\pm)}[t] i_{(\phi\pm)}(t)\, dt \tag{3.6}$$

Where,
- $v_{(\phi\pm)}$ is the total voltage inserted in an arm.
- $v^{\Sigma}_{c_{\phi\pm}}$ is the total voltage across all capacitor in an arm.

Equation (3.5) shows that with an ideal voltage balancing i.e. constant $v_{c_i(\phi\pm)}$ for all sub-modules, an arm can generate $N+1$ distinct levels of voltages. Unequal distribution of voltage among sub-modules can further enhance the number of distinct levels in arm voltages, but this conflict with the design and control of MMC.

The assumption of instantaneous voltage balancing control that yields ideal voltage balancing among all sub-modules in an arm implies that the time-average of an sub-modules duty-cycle ($\eta_{SM_i(\phi\pm)}$) equals instantaneous insertion index for the arm. *Insertion index* [40, 95, 96] defines the instantaneous average value of $\eta_{SM_i(\phi\pm)}$ i.e. the ratio of sub-modules "inserted".

$$n_{(\phi\pm)}(t) = \frac{1}{N}\sum_{i=1}^{N}\eta_{SM_i(\phi\pm)}[t] \tag{3.7}$$

With this average behavior of all sub-modules in an arm can be equivalently represented as:

$$v_{SM(\phi\pm)} = n_{(\phi\pm)}v_{c(\phi\pm)} \tag{3.8}$$

$$i_{c(\phi\pm)} = n_{(\phi\pm)}i_{(\phi\pm)}(t) \tag{3.9}$$

$$v_{c(\phi\pm)} = \frac{1}{C}\int i_{c(\phi\pm)}dt \tag{3.10}$$

$$n_{(\phi\pm)} \in \{\frac{i}{N} \mid i \in \mathbb{Z} \wedge i \geq 0 \wedge i \leq N\} \tag{3.11}$$

Where, $\begin{cases} v_{C(\phi\pm)} & \text{is the average voltage across SM's capacitor,} \\ i_{C(\phi\pm)} & \text{is the average current flowing through SM's capacitor,} \\ v_{SM(\phi\pm)} & \text{is the average voltage inserted by a SM.} \end{cases}$

Similarly, the average operation of an arm can be represented as:

$$v_{(\phi\pm)} = n_{(\phi\pm)}v^{\Sigma}_{c_{\phi\pm}} \tag{3.12}$$

$$i^{\Sigma}_{c(\phi\pm)} = n_{(\phi\pm)}i_{(\phi\pm)}(t) \tag{3.13}$$

$$v^{\Sigma}_{c_{\phi\pm}} = \frac{N}{C}\int i^{\Sigma}_{c(\phi\pm)}dt \tag{3.14}$$

Where, $i^{\Sigma}_{c(\phi\pm)}$ is the average current flowing through all capacitor.

Identical environment and operation of sub-modules tend to make this average representation reasonably accurate.

Moreover, this average representation of an arm serves as the foundation for the development of a unified analytic model for the MMC in the following section.

3.3. Currents and Voltages in System

To understand dynamics of the converter, develop its control system and optimally size its components, a unified model is an essential requirement. This section aims to develop a mathematical model for MMCs based on Kirchhoff's circuit laws.

3.3.1. Assumptions for analytical modeling of MMC

Before we continue to determine currents and voltages in the system and subsequently develop the unified model for the converter, a few assumptions need to be incorporated to simplify the analysis.

Below is the description of the assumptions, justification of their use and effect on the system variables.

1. The model only considers the nominal operation of the converter i.e. inserted, and bypassed states of sub-modules. Blocked state of converter only finds application in dc fault or startup operation. This operation has little impact on the design of control systems and component sizing. Therefore, for the model derived in this section neglects the blocked state.

2. Here it is assumed that all sub-modules are identical with a perfect voltage balancing across all capacitors of an arm. Therefore, an individual arm is represented by eqs. (3.12) to (3.14). Instantaneous nature of voltage balancing control that ensures voltage across all capacitors is within a defined limit, justifies this assumption.

3. For modeling purposes, it is assumed that switching frequency is infinite, and the voltage on AC side is purely sinusoidal i.e. there are an infinite number of sub-modules [40]. Therefore,

$$v_{ac_\phi}(t) = \hat{v}_{ac}\cos(\omega t + \Phi_\phi) \tag{3.15}$$

   Normally, N is in order of hundreds which is sufficiently large to consider AC voltage as purely sinusoidal. Furthermore, this makes the insertion index as defined in eq. (3.11) a continuous variable between in 0 and 1.

4. It is also assumed that AC side currents are purely sinusoidal. However, three phase currents are not necessarily balanced. Therefore,

$$i_{ac_\phi} = \hat{i}_{ac}\cos(\omega t + \Phi_\phi - \theta) \tag{3.16}$$

   A near sinusoidal AC voltage and high inductance on the AC side tend to justify this assumption.

These assumptions make insertion index a continuous variable and hence the model derived from this is termed as the "continuous" model.

3.3.2. Arm voltages and currents

Unlike LCC or classical VSC, in MMC all arms simultaneously generate voltage waveform and conduct current. This continuous conduction operation principle implies that arm currents in MMC as illustrated in fig. 3.7 is the superposition of three components.

I. Current from the AC side i.e. i_{ac_ϕ}
II. Current from DC side i.e. i_{dc_ϕ}
III. Current circulating between phase legs i.e. $i_{circ_\phi} - i_{dc_\phi}$

} i_{circ_ϕ}

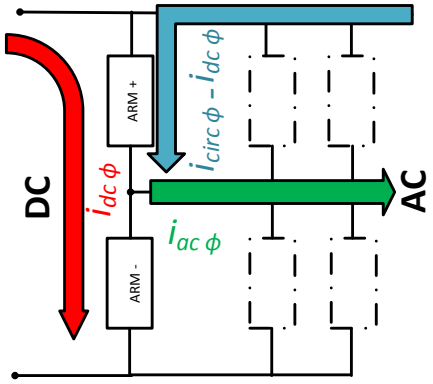


Figure 3.7: Current flow in an arm

Modeling all sub-modules in an arm as a variable voltage source, fig. 3.8 depicts currents and voltages in the converter.

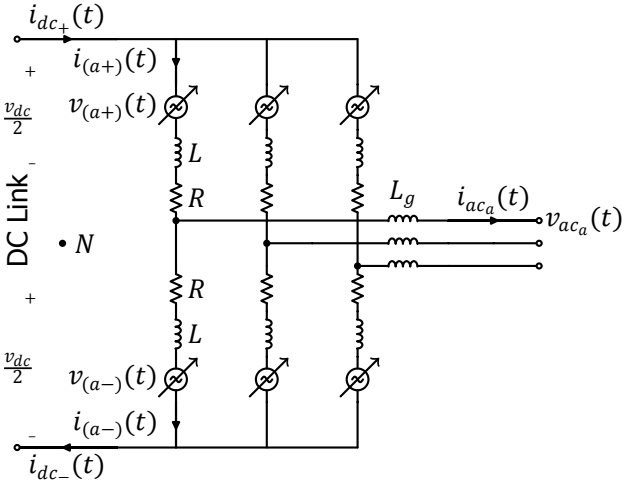


Figure 3.8: MMC - currents and voltages

Applying Kirchhoff's current law (KCL) at the AC side node yields:

$$i_{ac_\phi} = i_{(\phi+)} - i_{(\phi-)} \tag{3.17}$$

where, i_{+_ϕ} and i_{-_ϕ} correspond to the current in upper and lower arm of a phase leg respectively. Similarly KCL and algebraic manipulation yield arm currents as:

$$i_{\phi+} = i_{circ_\phi} + i_{diff_\phi} \tag{3.18}$$

$$i_{\phi-} = i_{circ_\phi} - i_{diff_\phi} \tag{3.19}$$

$$\text{where, } \begin{cases} i_{diff_\phi} & = \frac{1}{2} i_{ac_\phi} \\ i_{circ_\phi} & = \frac{1}{2}(i_{\phi+} + i_{\phi-}) \end{cases} \tag{3.20}$$

Applying Kirchhoff's voltage law (KVL) on the ac side gives:

$$-v_{ac_\phi}(t) - L_g \frac{di_{ac_\phi}(t)}{dt} - Ri_{(\phi+)}(t) - L\frac{di_{(\phi+)}(t)}{dt} - v_{(\phi+)}(t) + \frac{v_{dc}}{2} + v_{NG} = 0 \tag{3.21}$$

$$-v_{ac_\phi}(t) - L_g \frac{di_{ac_\phi}(t)}{dt} + Ri_{(\phi-)}(t) + L\frac{di_{(\phi-)}(t)}{dt} + v_{(\phi-)}(t) - \frac{v_{dc}}{2} + v_{NG} = 0 \tag{3.22}$$

Subtracting eqs. (3.21) and (3.22) and incorporating eq. (3.20) yields:

$$v_{dc} = v_{leg_\phi} + 2v_{circ_\phi} \tag{3.23}$$

where,

$$v_{leg_\phi} = v_{(\phi+)}(t) + v_{(\phi-)}(t) \tag{3.24}$$

$$v_{circ_\phi} = L\frac{d}{dt} i_{circ_\phi}(t) + Ri_{circ_\phi}(t) \tag{3.25}$$

$$\approx L\frac{d}{dt} i_{circ_\phi}(t) \rightarrow R \text{ is negligible compared to } L$$

Summing eqs. (3.21) and (3.22) and incorporating eq. (3.20) yields:

$$v_{ac_\phi} = e_\phi(t) - v_{diff_\phi} + v_{NG} \tag{3.26}$$

$$\text{where, } \begin{cases} e_\phi(t) & = -\frac{1}{2}\left(v_{(\phi+)}(t) - v_{(\phi-)}(t)\right) \\ v_{diff_\phi} & = \frac{1}{2}R\, i_{ac_\phi} + \frac{1}{2}L_{eq}\frac{d}{dt} i_{ac_\phi} \\ & = R\, i_{diff_\phi} + L_{eq}\frac{d}{dt} i_{diff_\phi} \\ & \approx L_{eq}\frac{d}{dt} i_{diff_\phi}(t) \rightarrow R \text{ is negligible.} \\ L_{eq} & = 2L_g + L \\ v_{NG} & = \text{Voltage between dc side neutral } (N) \text{ and ground.} \\ & \quad \text{Summing eq. (3.26) for all phases for a balanced} \\ & \quad \text{system yield } v_{NG} = 0. \end{cases} \tag{3.27}$$

With assumption of purely sinusoidal AC voltage and currents for a balanced system, from eqs. (3.15), (3.16), (3.26) and (3.27) internal e.m.f, $e_\phi(t)$, is expressed as:

$$\begin{aligned} e_\phi(t) &= \hat{v}_{ac}\cos(\omega t + \Phi_\phi) + \frac{L_{eq}}{2}\frac{d}{dt}\hat{i}_{ac}\cos(\omega t + \Phi_\phi - \theta) \\ &= \hat{e}_\phi \cos(\omega t + \Phi_\phi + \alpha) \end{aligned} \tag{3.28}$$

$$\text{Where, } \begin{cases} \hat{e}_\phi &= \sqrt{\left(\hat{v}_{ac} + \frac{\omega L_{eq}\sin\theta}{2}\hat{i}_{ac}\right)^2 + \left(\frac{\omega L_{eq}\cos\theta}{2}\hat{i}_{ac}\right)^2} \\ \tan\alpha &= \frac{\omega L_{eq}\cos\theta\hat{i}_{ac}}{2\hat{v}_{ac}+\omega L_{eq}\sin\theta\hat{i}_{ac}} \end{cases} \tag{3.29}$$

From the eq. (3.23) it can be concluded that:

- For balanced conditions, $v_{dc} - v_{leg_\phi}$ should equate to zero, which results in a constant direct circulating current. Therefore any non-dc component in circulating current stems from imbalance in voltages i.e. $v_{leg_\phi} \neq v_{dc}$.

  Sub-module capacitors in MMC serve as energy storage elements which are continuously charged and discharged. This implies that even with an instantaneous voltage balance control (section 5.2) imbalance in dc link voltage and inserted arm voltages in a leg is inevitable, leading to harmonics in circulating current. These operating conditions further imply that with filters or control schemes can suppress harmonics in the circulating current but cannot be fully eliminated [97].

- Circulating current only depends on the voltage imbalance i.e. $v_{dc} - v_{leg_\phi}$. It is independent of the AC side voltage and current. It induces an equal voltage drop across arm reactors of both positive and negative arms of a phase leg (v_{circ_ϕ}).

- This further reveals the significance of arm reactances L which serve following purposes: [78, 98]:

  - In the case of a voltage imbalance i.e. $v_{leg_\phi}(t) \neq v_{dc}$, additional current flow is expected in each leg. Arm reactance dampens these balancing currents and enables the control system to minimize these currents. The imbalance is attributed to ripple in capacitor voltage and can also occur due to discrepancies in switching instances of sub-modules in the positive and negative arm.

  - It significantly mitigates the effects of external or internal faults in a converter. In the case of a fault, arm reactors limit the rate of current rise to the order of tens of amperes per microsecond [78]. This ensures sufficient time for the protection system to react without causing any damage to the valves.

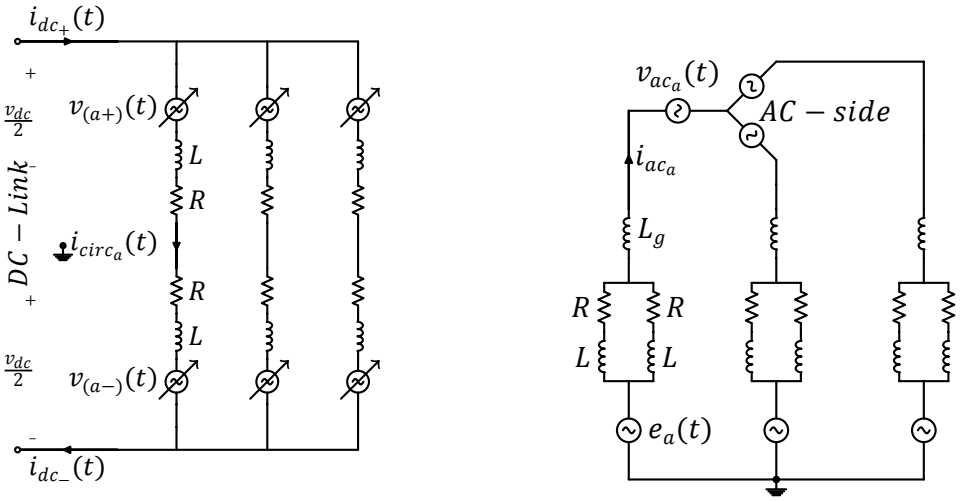
From the eq. (3.26) it can be concluded that [40],

- AC voltage only depends on the differential component of arm current (i_{diff_ϕ}) and difference of voltages on positive and negative arms.

- AC voltage only depends on the differential component of arm current and difference of voltages on positive and negative arms. Arm and converter transformer

inductance appear as internal impedance while the difference of inserted voltages in arms acts as the internal alternating voltage/ back e.m.f for the AC side.

Based on eqs. (3.23) and (3.26) dc (dc voltage/circulating current) and ac side dynamics (ac voltage/current) of the converter are independently controllable and can be separately represented as illustrated in fig. 3.9.



(a) DC side Equivalent Representation

(b) AC side Equivalent Representation

Figure 3.9: MMC Representation

Moreover rearrangement of eqs. (3.23) and (3.26) yields arm voltages in term of dc and ac voltages:

$$v_{(\phi+)}(t) + v_{(\phi-)}(t) = v_{dc} - 2v_{circ_\phi} \tag{3.30}$$

$$v_{(\phi+)}(t) - v_{(\phi-)}(t) = -2e_\phi(t) \tag{3.31}$$

Solution of eqs. (3.30) and (3.31) yields:

$$v_{(\phi+)}(t) = \frac{1}{2}v_{dc} - e_\phi(t) - v_{circ_\phi} \qquad v_{(\phi-)}(t) = \frac{1}{2}v_{dc} + e_\phi(t) - v_{circ_\phi} \tag{3.32}$$

Incorporating eq. (3.32) in eq. (3.12) yields:

$$n_{\phi+}(t) = \frac{\frac{v_{dc}}{2} - e_\phi - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi+}}(t)} \qquad n_{\phi-}(t) = \frac{\frac{v_{dc}}{2} + e_\phi - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi-}}(t)} \tag{3.33}$$

Equation (3.33) gives a generic expression for insertion indices of the positive and negative arm of phase leg that attains desired voltage on AC and dc side. Control of these insertion indices brings about the desired waveform on ac/dc voltages and with appropriate compensation of v_{circ_ϕ} can mitigate parasitic components in

circulating current. Section 6.1 further develops and utilizes this relation for the control of MMC.

Current to/from dc link is given by sum of arm currents on all phase legs i.e. using Kirchhoff's current law on eq. (3.18):

$$i_{dc_+} = \sum_{\phi=a,b,c} i_{(\phi+)} = \sum_{\phi=a,b,c} (i_{circ_\phi} + i_{diff_\phi}) \tag{3.34}$$

Differential current, i_{diff_ϕ}, as seen from eq. (3.20) corresponds to the current on ac side and is purely sinusoidal (section 3.3.1-4). In case of an unbalanced system, it can be represented as sum of zero, positive and negative sequence components and this reduces eq. (3.34) to:

$$i_{dc_+} = \sum_{\phi=a,b,c} i_{circ_\phi} + 1.5 i^0{}_{ac}(t) \tag{3.35}$$

$$\text{Similarly, } i_{dc_-} = \sum_{\phi=a,b,c} i_{circ_\phi} - 1.5 i^0{}_{ac}(t) \tag{3.36}$$

where, $i^0{}_{ac}(t)$ corresponds to zero sequence component in the unbalanced ac system.

Therefore, asymmetric faults on the ac side lead to an imbalance in current on the dc lines which are given by:

$$i_{dc_+} - i_{dc_-} = 3 i^0{}_{ac}(t) = i_{ac_a}(t) + i_{ac_b}(t) + i_{ac_c}(t) \tag{3.37}$$

Nevertheless, converters are usually connected to ac grid via un-grounded Y or Δ transformer with Δ side connected to the converter. In such configurations, infinite impedance for zero sequence currents prevents their flow into the converter for asymmetric conditions in the ac grid. However, asymmetric faults on the converter side of the transformer or in the case of a transformer-less/ grounded transformer configuration path for the flow of zero sequence currents exist which require additional control techniques for the mitigation of the imbalance [99, 100].

Circulating Current, i_{circ_ϕ} corresponds to the current circulating between phase legs and the DC side. As derived in eq. (3.20) circulating current is given by the average of currents in positive and negative arms. They are a result of an imbalance in dc voltage and arm voltages eq. (3.25). Close examination of voltage imbalance in a phase leg, as detailed in chapter A, reveal the presence of harmonic components. Therefore, i_{circ_ϕ} can be expressed as:

$$i_{circ_\phi} = \sum_{n=0}^{\infty} \hat{i}_{\phi,n} \cos(n\omega t + \Phi_{\phi,n}) \tag{3.38}$$

3.3.3. Average Power Balance

With the converter operation in the steady state for an individual phase leg, average power in/out of the phase leg due to circulating current (dc-side) should balance the average power in/out of ac terminal including compensation for losses. For a phase leg average power on AC side, DC side, and losses are given by:

$$\overline{P_{dc_\phi}} = v_{dc}\overline{i_{circ_\phi}} = v_{dc}\ i_{dc_\phi} \tag{3.39}$$

$$\overline{P_{ac_\phi}} = \frac{1}{2}\hat{e}_\phi\ \hat{i}_{ac}\cos(\theta+\alpha) \tag{3.40}$$

$$P_{loss_\phi} = 2i_{dc_\phi}^2 R \tag{3.41}$$

The compensation of losses is either from the dc or the ac side depending on the converter's operation as an inverter or a rectifier. Equating eqs. (3.39) to (3.41) yields:

Inverter Operation

$$\overline{P_{dc_\phi}} = \overline{P_{ac_\phi}} + P_{loss}$$

Solving for i_{dc_ϕ} yields

$$i_{dc_\phi} = \frac{\hat{e}_\phi\ \hat{i}_{ac}\cos(\theta+\alpha)}{v_{dc} + \sqrt{v_{dc}^2 - 4R\hat{e}_\phi\ \hat{i}_{ac}\cos(\theta+\alpha)}} \tag{3.42}$$

Rectifier Operation

$$\overline{P_{dc_\phi}} = \overline{P_{ac_\phi}} - P_{loss}$$

Solving for i_{dc_ϕ} yields

$$i_{dc_\phi} = \frac{\hat{e}_\phi\ \hat{i}_{ac}\cos(\theta+\alpha)}{v_{dc} + \sqrt{v_{dc}^2 + 4R\hat{e}_\phi\ \hat{i}_{ac}\cos(\theta+\alpha)}} \tag{3.43}$$

Neglecting losses in the system this balance of average power on dc and ac side of a phase leg yields:

$$i_{dc_\phi} = \frac{\hat{e}_\phi\hat{i}_{ac}\cos(\theta+\alpha)}{2v_{dc}} = \frac{1}{4}\hat{m}_\phi\hat{i}_{ac}\cos(\theta+\alpha) \tag{3.44}$$

$$\hat{m}_\phi = 2\frac{\hat{e}_\phi}{v_{dc}} \tag{3.45}$$

where, $\hat{m}_\phi$ is voltage modulation index [8]. DC component in circulating current as seen from eq. (3.44) is constant across all phase legs in a balanced system. Using this and eq. (3.35) it is concluded that:

$$i_{dc_\phi} = \frac{1}{3}i_{dc} \tag{3.46}$$

where, i_{dc} is the direct component in current to/from dc-terminals. This yield:

$$i_{circ_\phi} = i_{dc_\phi} + I^{\Sigma}_{Harm.\phi}(t) = \frac{1}{3}i_{dc} + \sum_{n=1}^{\infty}\hat{i}_{\phi,n}\cos(n\omega t + \Phi_{\phi,n}) \tag{3.47}$$

Where a balanced system implies eqs. (3.35) and (3.36)

$$\sum_{\phi=a,b,c} i^{\Sigma}_{Harm.\phi}(t) = \sum_{\phi=a,b,c} \sum_{n=1}^{\infty} \hat{i}_{\phi,n} \cos(n\omega t + \Phi_{\phi,n}) = 0 \tag{3.48}$$

Therefore, circulating current in a phase leg is composed of a two components i.e. dc current to/from dc terminals of MMC and the current circulating between phase legs.

Voltage drop in arm is due to the circulating currents, from eqs. (3.25) and (3.47) is given by:

$$v_{circ_\phi} = L\frac{d}{dt} i_{circ_\phi}(t) = L\frac{d}{dt} I^{\Sigma}_{Harm.\phi}(t) = L\sum_{n=1}^{\infty} n\omega \hat{i}_n \sin(n\omega t + \Phi_{\phi,n}) \tag{3.49}$$

From eqs. (3.16), (3.18) to (3.20) and (3.47) it is concluded that arm currents equate to:

$$i_{(\phi+)} = \frac{1}{3} i_{dc} \left(1 + \hat{k}_\phi \cos(\omega t + \Phi_\phi - \theta)\right) + \sum_{n=1}^{\infty} \hat{i}_{\phi,n} \cos(n\omega t + \Phi_{\phi,n}) \tag{3.50}$$

$$i_{(\phi-)} = \frac{1}{3} i_{dc} \left((1 - \hat{k}_\phi \cos(\omega t + \Phi_\phi - \theta)\right) + \sum_{n=1}^{\infty} \hat{i}_{\phi,n} \cos(n\omega t + \Phi_{\phi,n}) \tag{3.51}$$

$$\hat{k}_\phi = \frac{3}{2}\frac{\hat{i}_{ac}}{i_{dc}} \tag{3.52}$$

where, $\hat{k}_\phi$ is the current modulation index [8]. Incorporating $\hat{k}_\phi$ in eq. (3.44) yields:

$$\hat{m}_\phi \hat{k}_\phi = \frac{2}{\cos(\theta + \alpha)} \tag{3.53}$$

From the above it is concluded that:

- Transmission of real power by the converter results in a dc offset is in the circulating currents.
- DC component in circulating/arm current is constant across all phase legs in a balanced system i.e $i_{dc_a} = i_{dc_b} = i_{dc_c}$ and equate to one-third of the dc current to/from the DC side of MMC.
- $i^{\Sigma}_{Harm.\phi}(t)$ is the current component of circulating current that circulates within the three phase legs. Theses harmonic components in circulating current don't affect the AC and DC sides. However, they are detrimental to the operation of MMC. They enhance the r.m.s value of current flowing through phase legs,

thereby increasing losses and present higher current rating requirement for the converter components [40]. To improve the efficiency of MMC, mitigation of these harmonics is necessary.

- Arm currents as seen from eqs. (3.50) and (3.51) are the superposition of AC, DC current, and harmonics generated in the system as analyzed later. This superposition ensures that current changes it polarity in an arm which is essential to ensure voltage balance across sub-modules. The current changes polarity for around one-third of a cycle [83].

3.3.4. Equivalent Model of a MMC

Based on the *continuous model* all sub-modules in an arm can be represented by an equivalent sub-module with an equivalent capacitance of $\frac{C}{N}$ with voltage $v^{\Sigma}_{c(\phi\pm)}(t)$ where dynamics of the equivalent capacitor are given by eqs. (3.13) and (3.14). Incorporation of eqs. (3.18) and (3.19) in eqs. (3.13) and (3.14) yields:

$$v^{\Sigma}_{c\phi+} = \frac{N}{C}\int n_{(\phi+)}(i_{circ_\phi}(t) + \frac{1}{2}i_{ac_\phi}(t))dt \tag{3.54}$$

$$v^{\Sigma}_{c\phi-} = \frac{N}{C}\int n_{(\phi-)}(i_{circ_\phi}(t) - \frac{1}{2}i_{ac_\phi}(t))dt \tag{3.55}$$

Incorporating eqs. (3.12), (3.18) and (3.19) in eqs. (3.23), (3.26), (3.54) and (3.55) and using eq. (3.35) yields a continuous equivalent state-space model for the MMC as presented below, which is similar to the dynamic model presented in [40, 41].

This model yields internal dynamics i.e. arm voltages, circulating current and external dynamics i.e. ac side voltage and dc line currents, for the MMC for given dc link voltage, ac line currents, and insertion indices.

$$\frac{d}{dt}\begin{bmatrix} i_{circ_\phi}(t) \\ v^{\Sigma}_{c(\phi+)}(t) \\ v^{\Sigma}_{c(\phi-)}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{n_{\phi+}(t)}{2L} & -\frac{n_{\phi-}(t)}{2L} \\ \frac{N}{C}n_{\phi+}(t) & 0 & 0 \\ \frac{N}{C}n_{\phi-}(t) & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{circ_\phi}(t) \\ v^{\Sigma}_{c(\phi+)}(t) \\ v^{\Sigma}_{c(\phi-)}(t) \end{bmatrix} + \begin{bmatrix} \frac{v_{dc}}{2L} \\ \frac{N}{2C}n_{\phi+}(t)\ i_{ac_\phi}(t) \\ -\frac{N}{2C}n_{\phi-}(t)\ i_{ac_\phi}(t) \end{bmatrix}, \tag{3.56}$$

$$\begin{bmatrix} e_{ac_\phi}(t) \\ i_{circ_\phi}(t) \\ v_{(\phi+)}(t) \\ v_{(\phi-)}(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2}n_{\phi+}(t) & \frac{1}{2}n_{\phi-}(t) \\ 1 & 0 & 0 \\ 0 & n_{\phi+}(t) & 0 \\ 0 & 0 & n_{\phi-}(t) \end{bmatrix}\begin{bmatrix} i_{circ_\phi}(t) \\ v^{\Sigma}_{c\phi+}(t) \\ v^{\Sigma}_{c\phi-}(t) \end{bmatrix} + \begin{bmatrix} -\frac{R}{2}i_{ac_\phi}(t) - \frac{L_{eq}}{2}\frac{d}{dt}i_{ac_\phi}(t) \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.57}$$

$$i_{dc_+} = \sum_{\phi=a,b,c} i_{circ_\phi} + 1.5i^0{}_{ac}(t) \tag{3.58}$$

$$i_{dc_-} = \sum_{\phi=a,b,c} i_{circ_\phi} - 1.5i^0{}_{ac}(t) \tag{3.59}$$

In Laplace domain this model is equivalently represented as eqs. (3.60) to (3.62) and depicted as fig. 3.10.

$$I_{circ_\phi} = \frac{V_{dc} - (N_{\phi+}V^{\Sigma}_{c\phi+} + N_{\phi-}V^{\Sigma}_{c\phi-})}{2(Ls+R)} \tag{3.60}$$

$$V^{\Sigma}_{c\phi+} = \frac{N}{sC}N_{\phi+}(I_{circ_\phi} + \frac{1}{2}I_{ac_\phi}) \tag{3.61}$$

$$V^{\Sigma}_{c\phi-} = \frac{N}{sC}N_{\phi-}(I_{circ_\phi} - \frac{1}{2}I_{ac_\phi}) \tag{3.62}$$

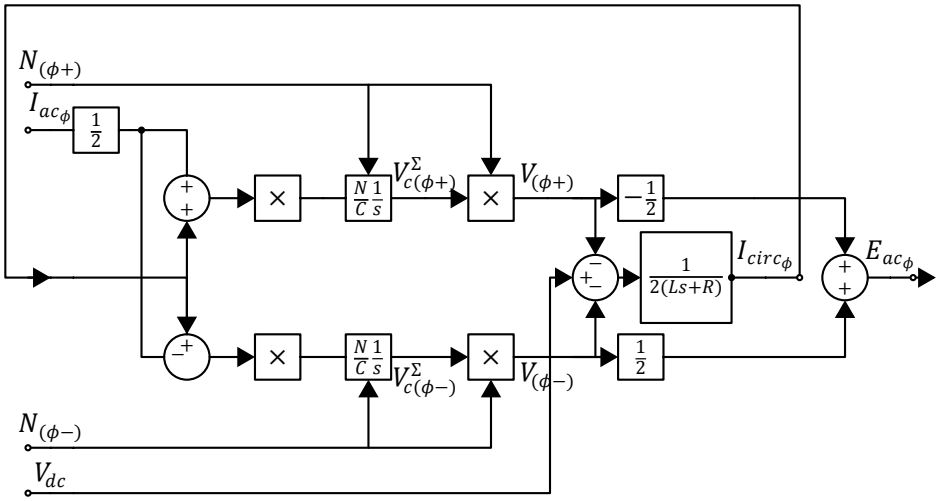


Figure 3.10: State Space Model

Based on this state-space representation unified model of MMC can be represented as fig. 3.11

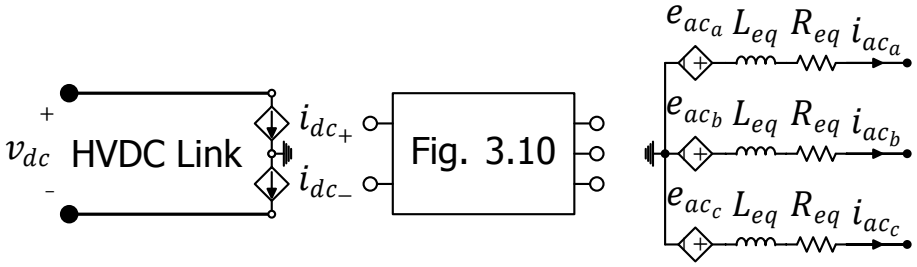


Figure 3.11: State Space Model

This non-linear state-space model gives a lump sum model of MMC with disregard for individual sub-modules. It is based on the assumptions stated earlier and gives

a continuous approximation to MMC operation. The assumptions tend to become more realistic at higher values of N. It is common to have N in order of 100's for HVDC application. Therefore, with higher N the model becomes more accurate and can provide adequate representation for the analysis of the converter. This model is useful for modeling of the steady state operation and design of the system. Since the model does not consider blocked state of operation it is not suitable for dc fault studies.

3.3.5. Instantaneous Power flow

The previous section defined the operation of the MMC and presented a non-linear state-space model. Using the assumption presented earlier and assuming a lossless converter this section derives the instantaneous power associated with the system.

Instantaneous power flow in an arm using eqs. (3.32), (3.50) and (3.51) is given as:

$$P_{+_\phi}(t) = \frac{d}{dt}W^{\Sigma}_{+\phi} = v_{(\phi+)}i_{+_\phi} = (\frac{v_{dc}}{2} - e_\phi - v_{circ_\phi})(i_{circ_\phi} + i_{diff_\phi}) \tag{3.63}$$

$$P_{-_\phi}(t) = \frac{d}{dt}W^{\Sigma}_{-\phi} = v_{(\phi-)}i_{-_\phi} = (\frac{v_{dc}}{2} + e_\phi - v_{circ_\phi})(i_{circ_\phi} - i_{diff_\phi}) \tag{3.64}$$

Sum of instantaneous power in positive and negative arms in a leg is given by:

$$\begin{aligned} P^{\Sigma}_{\phi}(t) = \frac{d}{dt}W^{\Sigma}_{\phi} &= P_{+_\phi}(t) + P_{-_\phi}(t) = (v_{dc} - 2v_{circ_\phi})i_{circ_\phi} - 2e_\phi i_{diff_\phi} \\ &= (v_{dc} - 2v_{circ_\phi})(i_{dc_\phi} + I^{\Sigma}_{Harm._\phi}(t)) - 2e_\phi i_{diff_\phi} \\ &= P^{\Sigma}_{SS_\phi} + P^{\Sigma}_{harm_\phi} \end{aligned} \tag{3.65}$$

Where,
$$\begin{cases} P^{\Sigma}_{SS_\phi} & = P_{dc_\phi} - P_{ac_\phi} = v_{dc}i_{dc_\phi} - 2e_\phi(t)i_{diff_\phi}(t) \\ & = \frac{1}{3}v_{dc}i_{dc} - \frac{1}{2}\hat{e}_\phi\hat{i}_{ac}\{\cos(\alpha+\theta) + \cos(2\omega t + 2\phi + \alpha - \theta\} \\ P^{\Sigma}_{harm_\phi} & = (v_{dc} - 2v_{circ_\phi})I^{\Sigma}_{Harm._\phi}(t) - 2v_{circ_\phi}i_{dc_\phi} \\ & = 2L\left(\frac{1}{3}i_{dc} + \sum_{n=1}^{\infty}\hat{i}_{\phi,n}\cos(n\omega t + \Phi_{\phi,n})\right)\sum_{n=1}^{\infty}\hat{i}_n n\omega\sin(n\omega t + \Phi_{\phi,n}) \\ & +v_{dc}\sum_{n=1}^{\infty}\hat{i}_{\phi,n}\cos(n\omega t + \Phi_{\phi,n}) \end{cases}$$

Sum of instantaneous power in all phase legs is given by:

$$P_{MMC}(t) = \sum_{\phi=a,b,c} P^{\Sigma}_{\phi}(t) \tag{3.66}$$

$$= \sum_{\phi=a,b,c}\left\{P_{dc_\phi} - P_{ac_\phi}\right\} \tag{3.67}$$

$$= P_{dc} - P_{ac} \tag{3.68}$$

From eq. (3.65) it is seen that:

- Average power in a leg equates to zero, and each leg transmits one-third of real power between AC and DC sides. For the operation of the converter as an inverter, capacitors are charged by DC and depleted by the AC current.
- Harmonics and parasitic elements have no influence on the average power in the system but affect the instantaneous power in the leg.

Similarly, difference of instantaneous power in positive and negative arms is:

$$P_{\phi}^{\Delta}(t) = \frac{d}{dt}W_{\phi}^{\Delta} = P_{+_{\phi}}(t) - P_{-_{\phi}}(t) = -2e_{\phi}i_{circ_{\phi}} + (v_{dc} - 2v_{circ_{\phi}})i_{diff_{\phi}} \quad (3.69)$$

$$= -2e_{\phi}i_{dc_{\phi}} + \frac{1}{2}v_{dc}i_{ac_{\phi}} - 2e_{\phi}I_{Harm.\phi}^{\Sigma}(t) - v_{circ_{\phi}}i_{ac_{\phi}} \quad (3.70)$$

$$= P_{SS_{\phi}}^{\Delta} + P_{harm_{\phi}}^{\Delta} \quad (3.71)$$

Where,

$$\begin{cases} P_{SS_{\phi}}^{\Delta} & = -2e_{\phi}i_{dc_{\phi}} + \frac{1}{2}v_{dc}i_{ac_{\phi}} \\ P_{harm_{\phi}}^{\Delta} & = -2e_{\phi}I_{Harm.\phi}^{\Sigma}(t) - v_{circ_{\phi}}i_{ac_{\phi}} \\ & = -\frac{1}{2}\hat{e}_{\phi}\sum_{n=1}^{\infty}\hat{i}_n\cos((n+1)\omega t + \Phi_{\phi,n} + \Phi_{\phi} + \alpha) \\ & \quad -\frac{1}{2}\hat{e}_{\phi}\sum_{n=1}^{\infty}\hat{i}_n\cos((n-1)\omega t + \Phi_{\phi,n} - \Phi_{\phi} - \alpha) \\ & \quad +\frac{1}{2}L\omega\hat{i}_{ac}\sum_{n=1}^{\infty}n\hat{i}_n\sin((n+1)\omega t + \Phi_{\phi,n} + \Phi_{\phi} - \theta) \\ & \quad -\frac{1}{2}L\omega\hat{i}_{ac}\sum_{n=1}^{\infty}n\hat{i}_n\sin((n-1)\omega t + \Phi_{\phi,n} - \Phi_{\phi} + \theta) \end{cases}$$

From eq. (3.69) it can be seen that [40]

- As long as there is no dc component in e_{ϕ} & $i_{diff_{\phi}}$ average value of $P_{SS_{\phi}}^{\Delta}$ equates to zero i.e. the average energy imbalance between arms (W_{ϕ}^{Δ}) is zero.
- Fundamental component in circulating current same as in e_{ϕ}, can leads to a dc component in the product $e_{\phi}i_{circ_{\phi}}$. Similarly presence of fundamental component in $v_{circ_{\phi}}$ as in $i_{ac_{\phi}}$ leads to a change in energy balance between arms. Presence of which influence the the overall energy balance between arms (W_{ϕ}^{Δ}). These dc two components in $P_{harm_{\phi}}^{\Delta}$ are

  1. $-\frac{1}{2}\hat{e}_{\phi}\hat{i}_1\cos(\Phi_{\phi,1} - \Phi_{\phi} - \alpha)$
  2. $-\frac{1}{2}L\omega\hat{i}_{ac}\hat{i}_1\sin(\Phi_{\phi,1} - \Phi_{\phi} + \theta)$

  For these dc to be zero, $\Phi_{\phi,1} - \Phi_{\phi} - \alpha = 90°$ & $\Phi_{\phi,1} - \Phi_{\phi} + \theta = 0$. This is not true as α and θ are coupled by eq. (3.29). Therefore fundamental component in circulating current leads to a difference in average stored energy in positive and negative arms.

3.3.6. Voltage Ripple and Circulating Current

Switching of submodule's capacitor in and out of circuit and flow of fundamental current in an arm implies deviation submodule's capacitor voltage from the desired constant value (i.e. $\frac{v_{dc}}{N}$). This voltage ripple on a submodule's capacitor is the superposition of two components [101] i.e.

- Local ripple component:
  Local ripple component is attributed to switching of a capacitor, such that with bypassed sub-module capacitor voltage remain constant but with inserted state it will increase or decrease depending on the direction of the current. This component is dependent on the modulation technique employed and voltage balancing algorithm. It tends to diminish as switching frequency increases.
- Average ripple component:
  This ripple component is associated with the flow of fundamental current in a capacitor sub-module. This ripple component does not depend on the switching frequency and is the expected ripple with infinite frequency.

The capacitor ripple leads to an imbalance in eq. (3.23) which contributes to harmonics in the circulating current. These additional harmonics, in turn, increase the ripple in capacitor voltage. This coupling of capacitor voltage and circulating current makes the explicit formulation of the voltage ripple complex. To develop understanding the voltage ripple and the circulating current, average voltage ripple across an arm is analyzed i.e. switching frequency is assumed to be infinite. For this analyses method followed in [102] has been adopted.

For starters, it is assumed that the circulating current is purely direct as given by eq. (3.44), which is essential for the transmission of real power. This reduces the expression for instantaneous power in a leg eq. (3.65) to:

$$\begin{aligned} P_{\phi}^{\Sigma}(t) &= \frac{1}{3}v_{dc}i_{dc} - \frac{1}{2}\hat{e}_{\phi}\hat{i}_{ac}\{\cos(\alpha+\theta) + \cos(2\omega t + 2\phi + \alpha - \theta)\} \\ &= -\frac{1}{2}\hat{e}_{\phi}\hat{i}_{ac}\cos(2\omega t + 2\phi + \alpha - \theta) \end{aligned} \tag{3.72}$$

Instantaneous energy in a leg is given by:

$$\begin{aligned} W_{\phi}^{\Sigma} &= \frac{1}{2}C_{leg_{\phi}}v_{leg_{\phi}}^{2} = \frac{C}{2N}v_{leg_{\phi}}^{2} = \int P_{\phi}^{\Sigma}(t)dt \\ &= -\frac{1}{4\omega}\hat{e}_{\phi}\hat{i}_{ac}\sin(2\omega t + 2\phi + \alpha - \theta) + \overline{W^{\Sigma}}_{\phi} \end{aligned} \tag{3.73}$$

where, $\overline{W^{\Sigma}}_{\phi}$ represents the steady state energy stored in all sub-modules of a phase leg [102].

$$\overline{W^{\Sigma}}_{\phi} = \frac{C}{2N}{v_{dc}}^{2} \tag{3.74}$$

This ripple in stored energy results in ripple in arm voltage i.e:

$$v_{leg_\phi}^2 = (v_{dc} + \Delta v_{leg_\phi})^2 = {v_{dc}}^2 - \frac{2N}{4C\omega}\hat{e}_\phi \hat{i}_{ac} \sin(2\omega t + 2\phi + \alpha - \theta) \quad (3.75)$$

Where $\Delta v_{leg_\phi} \ll v_{dc}$, this yields:

$$\Delta v_{leg_\phi} = -\frac{N}{4C\omega}\frac{\hat{e}_\phi}{v_{dc}}\hat{i}_{ac} \sin(2\omega t + 2\phi + \alpha - \theta) \quad (3.76)$$

From eq. (3.23) Δv_{leg_ϕ} correspnds to $(-2v_{circ_\phi})$. Using eqs. (3.25) and (3.76) yield:

$$i_{circ_\phi}(t) = \frac{1}{L}\int -\frac{1}{2}\Delta v_{leg_\phi} dt = \frac{1}{3}i_{dc} + \hat{i}_{\phi,2_1}\cos(2\omega t + \Phi_{\phi,2_1}) \quad (3.77)$$

$$\text{Where, } \begin{cases} \hat{i}_{\phi,2_1} & = -\frac{1}{16}\frac{1}{\omega^2 CL}\frac{N}{v_{dc}}\hat{e}_\phi\hat{i}_{ac} = -\frac{1}{16}\frac{\omega_{res}^2}{\omega^2}\frac{N}{v_{dc}}\hat{e}_\phi\hat{i}_{ac} \\ \Phi_{\phi,2_1} & = 2\phi + \alpha - \theta \end{cases} \quad (3.78)$$

With this additional second harmonic, the above procedure is reiterated to determine the voltage ripple. This yields the instantaneous power in a leg eq. (3.65) as:

$$\begin{aligned} P_\phi^\Sigma(t) = & -\frac{1}{2}\hat{e}_\phi\hat{i}_{ac}\cos(2\omega t + 2\phi + \alpha - \theta) \\ & + 2L\left(\frac{1}{3}i_{dc} + \hat{i}_{\phi,2_1}\cos(2\omega t + \Phi_{\phi,2_1})\right)\hat{i}_{\phi,2_1}2\omega\sin(2\omega t + \Phi_{\phi,2_1}) \\ & + v_{dc}\hat{i}_{\phi,2_1}\cos(2\omega t + \Phi_{\phi,2_1}) \end{aligned} \quad (3.79)$$

Instantaneous energy in a leg is given by:

$$\begin{aligned} W_\phi^\Sigma = & -\frac{1}{4\omega}\hat{e}_\phi\hat{i}_{ac}\sin(2\omega t + \Phi_{\phi,2_1}) \\ & - \frac{2}{3}Li_{dc}\hat{i}_{\phi,2_1}\cos(2\omega t + \Phi_{\phi,2_1}) \\ & - \frac{1}{2}L\hat{i}_{\phi,2_1}^2\cos(4\omega t + 2\Phi_{\phi,2_1}) \\ & + \frac{1}{2\omega}v_{dc}\hat{i}_{\phi,2_1}\sin(2\omega t + \Phi_{\phi,2_1}) + \overline{W^\Sigma}_\phi \end{aligned} \quad (3.80)$$

This yields:

$$i_{circ_\phi}(t) = \frac{1}{3}i_{dc} + \hat{i}_{\phi,2_2}\cos(2\omega t + \Phi_{\phi,2_2}) + \hat{i}_{\phi,4_2}\cos(4\omega t + \Phi_{\phi,4_2}) \quad (3.81)$$

$$\text{Where,} \begin{cases} \hat{i}_{\phi,2_2} & = \hat{i}_{\phi,2_1}\sqrt{(1+\frac{N}{8\omega^2 LC})^2+(\frac{Ni_{dc}}{6\omega C v_{dc}})^2} \\ \Phi_{\phi,2_2} & = 2\phi+\alpha-\theta-\arctan\frac{(1+\frac{N}{8\omega^2 LC})}{(\frac{Ni_{dc}}{6\omega C v_{dc}})} \\ \hat{i}_{\phi,4_2} & = \frac{N}{8\omega C v_{dc}}\hat{i}^2_{\phi,2_1} \\ \Phi_{\phi,4_2} & = 4\phi+2\alpha-2\theta-90^\circ \end{cases} \tag{3.82}$$

This formulation can be reiterated to get further detail on harmonics.

Based on the results above it can be concluded that

- The fundamental current component in converter arms leads to a voltage ripple in SM capacitors with a dominant second harmonic.
- This leads to second and higher harmonics in the circulating current.
- The second harmonic component has a negative sequence.

3.4. Conclusion

In conclusion, this chapter revealed that with independent control of submodules, each arm of an MMC behaves as a variable voltage source, which allows for independent control on all ac-voltages and the dc-voltage. This further enables MMC to operate on unbalanced/distorted voltages on AC/DC side, aiding system's recovery [103].

Furthermore, mathematical formulation presented in this chapter showed that operation of MMC is split into AC and DC side. The AC side operation of MMC as seen from eq. (3.26) and fig. 3.9b is defined by internal e.m.f $e_\phi(t)$ and internal impedance L_{eq} and R. Through appropriate selection of insertion indices and resulting difference of arm voltages, MMC can attain desired voltage on AC side together with desired real and reactive power exchange with the grid if any. Similarly, DC voltage as revealed by eq. (3.23) and fig. 3.9a is also controllable by insertion indices and the resulting sum of arm voltages.

Moreover, this chapter explained the presence of parasitic harmonic components in circulating current which lead to higher losses in the system. In addition to the undesirable effect of circulating current, section 3.3.5 showed that circulating current provides control over internal energy dynamics of the converter. DC component of circulating current regulates energy stored in a phase leg and similarly the fundamental component of circulating current can control energy imbalance in two arms of a phase leg. Techniques can be employed to minimize the imbalance such circulating current only has dc component.

The circuit analyses presented in this chapter serves as the foundation for upcoming sections that examine control and modulations techniques for MMC and their effects on the converter's dynamics.

4

Component Selection

Optimum sizing of component ensures desired performance of MMC within the constraints of cost and size. This chapter investigates the selection of the number of sub-modules, sub-modules capacitance, and arm inductance.

The dynamics of converter as seen in the last chapter are influenced by:

1. Number of Sub-modules
2. Sub-module capacitance
3. Arm reactance

The number of submodules and its capacitance define the stored energy in the converter and arm reactance limits the rate of change of current in case of an imbalance in the system. To attain desired characteristics for the converter, appropriate sizing of these components is a necessary prerequisite.

4.1. Number of Sub-modules

The number of sub-modules for an MMC is dictated by:

- DC link Voltage
- IGBT valve voltage rating
- Allowed total harmonic distortion for the unfiltered ac-voltage

Based on the dc link voltage and IGBT valve rating minimum number of SM in an arm is calculated as:

$$N \geq \frac{v_{dc}}{v_{IGBT_{Rating}}} \tag{4.1}$$

The harmonic content of output ac-voltage among other factors is dependent on the number of SM and the modulation technique utilized for the converter. The number of sub-modules dictates the maximum number of levels in ac voltage waveform, which directly influences the harmonic content.

4.2. Sub-module capacitance

The flow of fundamental current component and dc component in arm implies charging and discharging of sub-module capacitors. This results in voltage ripple, which is dependent on the value of capacitance. The higher the capacitance, the larger is the energy stored and smaller is the ripple; however this adds to cost and size of the sub-module. Therefore, a trade-off between size and cost of the capacitor with allowed voltage ripple is necessary for optimum results. The higher the allowed ripple, the smaller is the required SM capacitance.

For given system ratings and permissible ripple, instantaneous power flow from ac side and dc side in an arm are analyzed to determine the optimal value of capacitance [8]. The analysis assumes perfect imbalance on dc side i.e. circulating current is purely direct, and converter losses are negligible $R \approx 0$. Incorporation of this assumption implies that $v_{circ_\phi} \approx 0$ and simplifies eqs. (3.63) and (3.64) to:

$$P_{+_\phi}(t) = \frac{v_{dc} i_{dc}}{6}\left(1 - \hat{m}_\phi \cos(\omega t + \Phi_\phi + \alpha)\right)\left(1 + \hat{k}_\phi \cos(\omega t + \Phi_\phi - \theta)\right) \quad (4.2)$$

$$P_{-_\phi}(t) = \frac{v_{dc} i_{dc}}{6}\left(1 + \hat{m}_\phi \cos(\omega t + \Phi_\phi + \alpha)\right)\left(1 - \hat{k}_\phi \cos(\omega t + \Phi_\phi - \theta)\right) \quad (4.3)$$

Equations (4.2) and (4.3) reveals that with aforementioned assumptions:

- Average power in an arm over one time-period equates to zero i.e. average DC power in equals average AC power out.
- The stationary points for energy stored in capacitor at a particular voltage modulation index $\hat{m}_\phi$ correspond to:

$$\text{For Positive Arm: } \omega t + \Phi_\phi = \begin{cases} \gamma_{1_+} & = \pi - \arccos\left(\dfrac{1}{\hat{k}_\phi}\right) + \theta \\ \gamma_{2_+} & = \pi + \arccos\left(\dfrac{1}{\hat{k}_\phi}\right) + \theta \end{cases} \quad (4.4)$$

$$\text{For Negative Arm: } \omega t + \Phi_\phi = \begin{cases} \gamma_{1_-} & = \theta - \arccos\left(\dfrac{1}{\hat{k}_\phi}\right) \\ \gamma_{2_-} & = \theta + \arccos\left(\dfrac{1}{\hat{k}_\phi}\right) \end{cases} \quad (4.5)$$

Integrating eqs. (4.2) and (4.3) between these limits yields the ripple in the stored energy.

$$\Delta E_{+_\phi}(t) = \frac{v_{dc} i_{dc}}{6\omega}\left[-\hat{m}_\phi \sin(\omega t + \Phi_\phi + \alpha) + \hat{k}_\phi \sin(\omega t + \Phi_\phi - \theta)\right.$$

$$-\frac{\hat{m}_\phi \hat{k}_\phi}{4}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta)\Big]_{\gamma_{2+}}^{\gamma_{1+}}$$

$$= \hat{k}_\phi \frac{v_{dc} i_{dc}}{3\omega}\left(1 - \frac{1}{\hat{k}_\phi^2}\right)^{\frac{3}{2}} \tag{4.6}$$

$$\Delta E_{-_\phi}(t) = \frac{v_{dc} i_{dc}}{6\omega}\left[\hat{m}_\phi \sin(\omega t + \Phi_\phi + \alpha) - \hat{k}_\phi \sin(\omega t + \Phi_\phi - \theta)\right.$$
$$\left. -\frac{\hat{m}_\phi \hat{k}_\phi}{4}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta)\right]_{\gamma_{2-}}^{\gamma_{1-}}$$

$$= \hat{k}_\phi \frac{v_{dc} i_{dc}}{3\omega}\left(1 - \frac{1}{\hat{k}_\phi^2}\right)^{\frac{3}{2}} \tag{4.7}$$

This corresponds to energy variation in an arm. Instantaneous voltage balance control implies that this variation is equally split between all capacitors. Therefore,

$$\Delta E_{SM}(t) = \frac{\hat{k}_\phi}{N}\frac{v_{dc} i_{dc}}{3\omega}\left(1 - \frac{1}{\hat{k}_\phi^2}\right)^{\frac{3}{2}} \tag{4.8}$$

Voltage ripple in a sub-module is given as:

$$\frac{1}{2}C\left({v_{C_{max}}}^2 - {v_{C_{min}}}^2\right) = \frac{\hat{k}_\phi}{N}\frac{v_{dc} i_{dc}}{3\omega}\left(1 - \frac{1}{\hat{k}_\phi^2}\right)^{\frac{3}{2}} \tag{4.9}$$

Where $v_{C_{max}}$ and $v_{C_{min}}$ are defined as:

$$v_{C_{max}} = \overline{v}_C(1 + \epsilon) \tag{4.10}$$
$$v_{C_{min}} = \overline{v}_C(1 - \epsilon) \tag{4.11}$$

Where ϵ represents allowed variation in voltage from nominal value and $\overline{v}_C = \frac{v_{dc}}{N}$. In addition power from dc side $P_{dc} = v_{dc} i_{dc}$ equals P_{ac}. Incorporating this, eqs. (4.10) and (4.11) in eq. (4.9) gives:

$$C = \frac{N}{6\omega\epsilon v_{dc}^2}\hat{k}_\phi P_{AC_{3\phi}}\left(1 - \frac{1}{\hat{k}_\phi^2}\right)^{\frac{3}{2}} \tag{4.12}$$

Incorporating eq. (3.53) yields

$$C = \frac{N S_{AC_{3\phi}}}{3v_{dc}^2}\frac{1}{\hat{m}_\phi \omega \epsilon}\left(1 - \frac{\hat{m}_\phi^2 \cos^2(\theta + \alpha)}{4}\right)^{\frac{3}{2}} \tag{4.13}$$

From eq. (4.13) it can be seen that value of capacitance is dependent on the number of sub-modules, power in system, dc side voltage etc. Therefore, another variable is introduced that defines nominal stored energy in all capacitors per power rating of system, E_{MMC} [80]. This is given by:

$$E_{MMC} = \frac{1}{S_{AC_{3\phi}}} 6N \left(\frac{1}{2} C \left(\frac{v_{dc}}{N} \right)^2 \right) \tag{4.14}$$

Incorporating eq. (4.14) in eq. (4.13) yields

$$E_{MMC} = \frac{1}{\hat{m}_\phi \omega \epsilon} \left(1 - \frac{\hat{m}_\phi^2 \cos^2(\theta + \alpha)}{4} \right)^{\frac{3}{2}} \tag{4.15}$$

Equation (4.15) can determine the required energy storage per rated power of system for given modulation index eq. (3.45), power factor, the frequency of the system and allowed ripple in capacitor voltage.
For example for a system with modulation index $m = 0.9$, power-factor $\cos\theta = 0.75$, $\alpha \approx 0$ frequency 50 Hz and a maximum ripple of 10% i.e. $\epsilon = 0.1$. E_{MMC} comes out to be $29.5\ J/KVA$. Based on this value capacitors can be appropriately sized using eq. (4.14).

4.3. Arm reactance

Arm reactance and inserted SM capacitor forms a series resonance circuit in the path of circulating current. However, variable nature of equivalent capacitance of arm implies that this resonant circuit is time varying. Analyses of resonant frequencies as presented in [104] and further analyzed in [105] yield following relation for resonant frequencies:

$$\omega_{res}^2 = \frac{N}{LC} \frac{2(n^2 - 1) + \hat{m}^2 n^2}{4n^2(n^2 - 1)} \tag{4.16}$$

where, n corresponds to the order of harmonic and is an even number.

To avoid resonance of circulating current harmonics, systems operating frequency should be higher than the maximum resonant frequency given by eq. (4.16).

As analyzed in sections A.2 and 3.3.6 harmonics are of even order where second order harmonic is the most dominant; ignoring harmonics of the higher-order, maximum resonant frequency in eq. (4.16) corresponds to $n = 2$ & $m = 1$. This yields following constraint on arm inductance and sub-module's capacitance [104, 106].

$$LC > \frac{5N}{24\omega^2} \tag{4.17}$$

5

Control Scheme

Control in converters is essential for its operation and enables the system to attain its desirable characteristics.

The control system in an MMC generates ac and dc reference waveforms that aim to achieve desired power flow and voltage waveforms in the system; while balancing voltage across sub-modules and minimizing unwanted harmonic components in the arm currents. Figure 5.1 illustrates the-the control system for an MMC, which is hierarchized as:

1. Upper level control –
   - Active power control
   - Reactive Power control
   - DC voltage
   - AC voltage
2. Inner level control – Controls voltage distribution among sub-modules
3. Auxiliary operations –
   - Mitigation of circulating current
   - Mitigation of zero sequence currents
   - Fault control

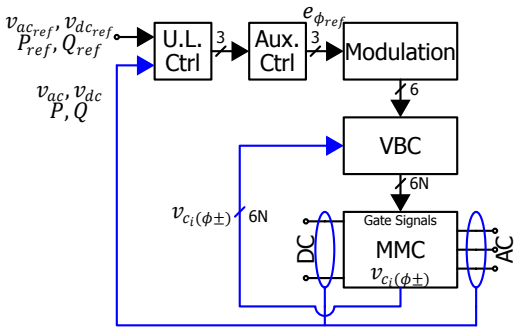


Figure 5.1: Control Schematic for a grid-connected MMC

5.1. Upper level control

The objective of the upper-level control is to determine the reference waveforms for the dc side voltage ($v_{dc_{ref\phi}}$) and internal e.m.f (e_{ref}) to generate desired terminal voltage waveforms and attain desired real/reactive power flow. The MMC with its ability to synthesize AC voltage can operate both with and without AC grid and subsequently the upper-level control system is split as:

- Islanded Control
  With islanded mode of operation, either there is no or a weak grid on the ac side. In such systems, the converter actively controls the frequency and voltages in the system. For this control scheme, internal e.m.f of MMC for desired terminal voltage and load can be calculated from the droop control [107].
- Grid Connected Control
  With this mode of operation, MMC is connected to a strong ac grid. The control with this setup has to ensure synchronization with the grid and attain desired real and reactive power exchange.

Grid connected control can be realized by direct and vector control methods.

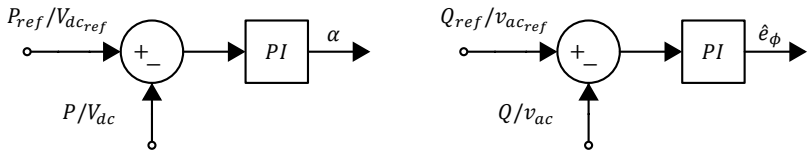
5.1.1. Direct Control

Based on the ac side equivalent representation of MMC fig. 3.9b, power flow between converter and ac system ignoring converter and line losses is given as:

$$P_{ac} = \frac{\hat{v}_{ac}\hat{e}_{\phi}\sin\alpha}{X} \qquad Q_{ac} = \frac{\hat{v}_{ac}^2 - \hat{v}_{ac}\hat{e}_{\phi}\cos\alpha}{X} \tag{5.1}$$

$$\text{where, } X = \omega(L_g + \frac{1}{2}L)$$

From eq. (5.1) it is seen that real and reactive power flow between MMC and AC grid can be controlled by varying magnitude and phase of $e_{\phi}(t)$ with respect to $v_{ac_{\phi}}$. This control scheme utilizes two PI controllers which generate reference values of $e_{\phi}(t)$ and angle α based on the error in rms ac voltage or reactive power and real power or dc voltage receptively as illustrated in fig. 5.2. However, this control strategy due to coupling between eq. (5.1) fails to attain independent control of active and reactive power [108].



(a) Real Power/DC voltage control (b) Reactive Power/AC voltage control

Figure 5.2: Direct control strategy

5.1.2. Vector Control

This control strategy is based on the D-Q synchronous reference frame model of the system and is similar to the vector control for a conventional VSC [109, 110]. The essence of D-Q reference frame's is its ability to convert three phase AC values to two orthogonal dc values. With appropriate transformation vector control can achieve independent real and reactive power as explained below:

$$S = 3v_{ac}i_{ac}^{*} = \frac{3}{2}\left(v_d + jv_q\right)\left(i_d - ji_q\right) = \frac{3}{2}\left(v_d i_d + v_q i_q\right) + j\frac{3}{2}\left(v_q i_d - v_d i_q\right) \quad (5.2)$$

With d-q axis aligned with vector v_{ac} such that $v_d = \hat{v}_{ac}$ & $v_q = 0$, eq. (5.2) is reduced to: $S = \frac{3}{2}v_d i_d - j\frac{3}{2}v_d i_q$. Any additional coupling in d-q components of the system is mitigated by the use of feed-forward control loops [108]. For the transformation and alignment of d-q axis synchronization with the grid is required. This requires precise tracking of the phase of the grid and is accomplished through phase locked loop [111].

MMC linear-time-invariant model

The three phase equations represented ac side of MMC (eq. (3.26)) can be transformed to two phase stationary axis using *Clarke's transformation*.

$$v_{\alpha\beta} = e_{\alpha\beta}(t) - \frac{1}{2}Ri_{\alpha\beta}(t) - \frac{1}{2}L_{eq}\frac{di_{\alpha\beta}(t)}{dt} \quad (5.3)$$

where, $x_{\alpha\beta} = x_\alpha + jx_\beta$. Applying *Park's transformation* i.e. $x_{dq} = x_{\alpha\beta}\, e^{j\int\omega\,\mathrm{d}t}$ to transform from stationary reference frame to rotating reference frame yields:

$$v_{dq}(t) = e_{dq}(t) - \frac{1}{2}Ri_{dq}(t) - \frac{1}{2}L_{eq}\frac{di_{dq}(t)}{dt} + j\frac{1}{2}\omega L_{eq}i_{dq}(t) \quad (5.4)$$

$$\Rightarrow \begin{cases} v_d(t) &= e_d(t) - \frac{1}{2}Ri_d(t) - \frac{1}{2}L_{eq}\frac{d}{dt}i_d(t) - \frac{1}{2}\omega L_{eq}i_q(t) \\ v_q(t) &= e_q(t) - \frac{1}{2}Ri_q(t) - \frac{1}{2}L_{eq}\frac{d}{dt}i_q(t) + \frac{1}{2}\omega L_{eq}i_d(t) \end{cases} \quad (5.5)$$

Transforming eq. (5.5) in Laplace domain yields:

$$V_d(s) = E_d(s) - \frac{1}{2}(R + sL_{eq})I_d(s) - \frac{1}{2}\omega L_{eq}I_q(s) \quad (5.6)$$

$$V_q(s) = E_q(s) - \frac{1}{2}(R + sL_{eq})I_q(s) + \frac{1}{2}\omega L_{eq}I_d(s) \quad (5.7)$$

Equations (5.6) and (5.7) defines the relation between input currents and output voltages and are depicted in fig. 5.3. However, d-q components are coupled because of $0.5\omega L_{eq}I_d$ & $0.5\omega L_{eq}I_q$ terms which are mitigated by the feed-forward technique i.e.

$$\widetilde{E}_d(s) = E_d(s) - V_d(s) - \frac{1}{2}\omega L_{eq}I_q(s) \quad (5.8)$$

$$\widetilde{E}_q(s) = E_q(s) - V_q(s) + \frac{1}{2}\omega L_{eq}I_d(s) \quad (5.9)$$

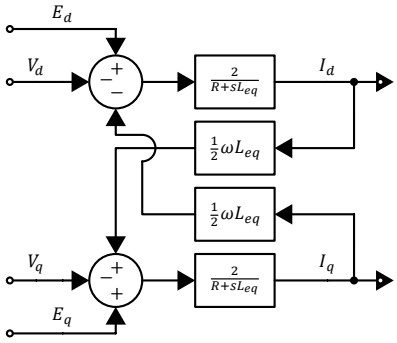


Figure 5.3: D-Q Axis representation of AC side of MMC

Substitution of eq. (5.8) in eq. (5.6) and eq. (5.9) in eq. (5.7) yields independent transfer function for direct and quadrature components:

$$H_{Sys}(s)\begin{cases}\frac{I_d}{\widetilde{E}_d(s)} & = \frac{1}{\frac{R}{2}+\frac{L_{eq}}{2}s} \\ \frac{I_q}{\widetilde{E}_q(s)} & = \frac{1}{\frac{R}{2}+\frac{L_{eq}}{2}s}\end{cases} \tag{5.10}$$

For dc-side the phase legs behave as an equivalent capacitor, C_{eq} as illustrated in fig. 5.4 and the system transfer function can be derived with an assumption of instantaneous balance of power between ac and dc sides of converter i.e.

$$v_{dc}i_{dc} = \frac{3}{2}v_d i_d \qquad \& \qquad i_{dc} - i_L = C_{eq}\frac{dv_{dc}}{dt} \tag{5.11}$$

$$\implies C_{eq}\frac{dv_{dc}}{dt} = \frac{3}{2}\frac{v_d i_d}{v_{dc}} - i_L \tag{5.12}$$

Linearization of eq. (5.12) for small variations around equilibrium state yields [110]:

$$\frac{\Delta V_{dc}}{\Delta I_d} = \frac{K_{dc}}{s\tau_C + \frac{3}{2}\frac{i_{d_0}v_{d_0}}{v_{dc_0}^2}} \qquad \text{where,} \begin{cases} i_{dc_0} = i_{L_0} & i_{d_0} = \frac{2}{3}\frac{i_{L_0}v_{dc_0}}{v_{d_0}} \\ \tau_C = C_{eq} & K_{dc} = \frac{3}{2}\frac{v_{d_0}}{v_{dc_0}} \end{cases} \tag{5.13}$$

By utilizing feed-forward terms eq. (5.13) is reduced to:

$$\frac{\Delta V_{dc}}{\Delta I_d} = \frac{3}{2}\frac{v_{d_0}}{v_{dc_0}}\frac{1}{sC_{eq}} \tag{5.14}$$

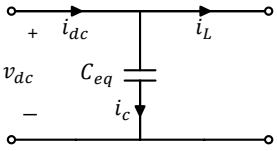


Figure 5.4: DC side representation of MMC

Vector control uses proportional-integral regulators for the control. Optimal controller parameter ensures fast and stable response of the system. Optimal tuning of controllers can be accomplished through heuristic approaches such as ziegler–nichols method [112] or analytical methods such as pole-placement, modulus, and symmetric optimum, etc. For the analytical methods, complete knowledge of the system is a necessary prerequisite. The transfer functions for the system components are given by:

- PI controller - Its transfer function is given by:

$$H_{PI}(s) = K_p \frac{1 + T_i s}{T_i s} \tag{5.15}$$

  where, K_p is the proportional gain, and T_i is the integral time constant.

- Modulations and inner level control - It has an effect of digital controller i.e. sample and hold on the input signal system. This is modeled as:

$$H_{MOD}(s) = \frac{1}{1 + T_e s} \tag{5.16}$$

  The hold time of modulation varies from 0 to up to one switching cycle (T_{SW}), for modeling, the average value of $\frac{T_{SW}}{2}$ is selected.

- System - Equations (5.10) and (5.14) presents linear time invariant (LTI) model for MMC's ac and dc side operation respectively.

Based on these models for system components, following sub-sections provide detail derivation and tuning of MMC's ac and dc side control using the vector control.

AC side control

Based on the vector-control, the power-flow control of inverter end is illustrated in fig. 5.5. This control scheme consists of two cascaded control loops each for the direct and quadrature components. The outer-loop based on the reference and measured values of real power and reactive power/r.m.s AC voltage generate

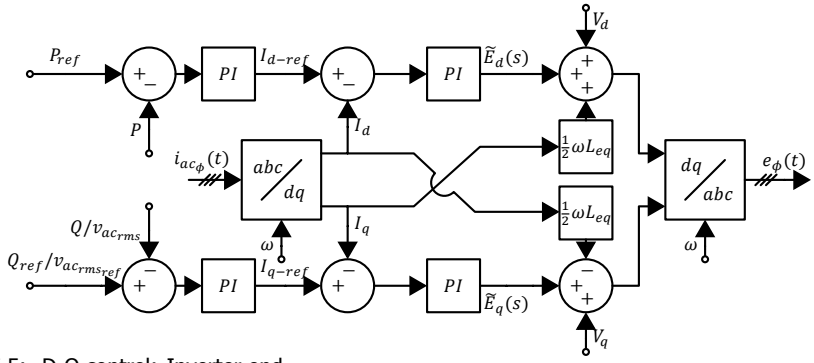


Figure 5.5: D-Q control: Inverter end

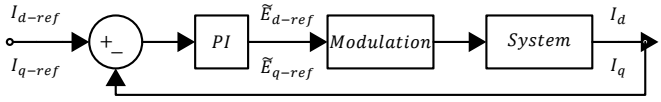


Figure 5.6: Inner current loop tuning

reference values of direct (I_{d-ref}) and quadrature (I_{q-ref}) currents respectively. The inner faster current loops use these reference and measured currents from the system to determine direct and quadrature components of internal e.m.f of MMC. The decoupled inner loops can be represented as in fig. 5.6.

For systems having one dominant (not close to the origin) and multiple minor time constants, optimal controller parameters can be determined through the "modulus optimum" method. The MO method aims to maximize the bandwidth for which the magnitude response of the closed-loop system is equal/close to unity [113]. This is accomplished through pole-zero cancellation and optimal selection of the damping constant for the closed loop system [109, 110].

Open loop transfer function of the inner loop system is calculated as:

$$G_{OL_{ac}}(s) = H_{PI}(s)H_{MOD}(s)H_{Sys}(s) = K_{p_{ac}} \frac{1 + T_{i_{ac}}s}{T_{i_{ac}}s\frac{R_{pu}}{2}\left(1 + \frac{L_{eq_{pu}}}{\omega R_{pu}}s\right)(1 + T_e s)} \tag{5.17}$$

Canceling dominant system pole with zero of PI controller yields,

$$1 + T_i s = (1 + \frac{L_{eq}}{R}s) \implies T_{i_{ac}} = \frac{L_{eq_{pu}}}{\omega R_{pu}} \tag{5.18}$$

With this condition the closed loop transfer function of the system is given by:

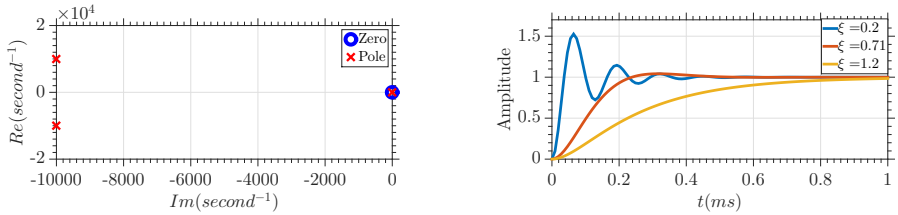
$$G_{CL_{ac}}(s) = \frac{1}{1 + \frac{1}{G_{OL_{ac}}(s)}} = \frac{\omega_m^2}{s^2 + 2\xi\omega_m s + \omega_m^2} \tag{5.19}$$

$$\text{Where, } \omega_m = \sqrt{\frac{2\omega K_{p_{ac}}}{L_{eq_{pu}} T_e}} \quad \& \quad 2\xi\omega_m = \frac{1}{T_e}$$

For modulus optimum the damping factor, ξ is selected as $\frac{1}{\sqrt{2}}$ [113]. This yields:

$$K_{p_{ac}} = \frac{L_{eq_{pu}}}{4T_e\omega} \tag{5.20}$$

Figure 5.7a illustrates the resulting pole and zeros in the closed loop and fig. 5.7b shows the effect of the damping factor on the system's step response. Based on this controller, fig. 5.8 illustrates the response of detailed model of the converter under a step change in I_d. The responses from detailed model corresponds to that of the fig. 5.7b, which not only further validates the control system but also confirms the accuracy of the LTI model of used in the design of the controller.



(a) Pole-Zero plot (b) Step-response for different values of ξ

Figure 5.7: Modulus optimum tuning

The outer PI controller is tuned using trial and error approach. The reference values of $E_d(s)$ and $E_q(s)$ obtained from the controller are transformed back to the stationary reference frame and further utilized in the modulation system.

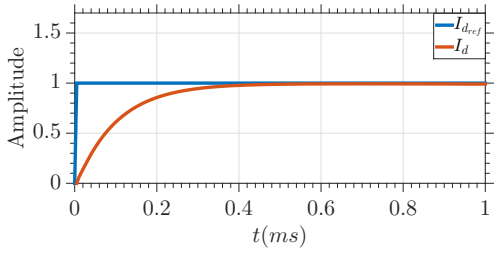


Figure 5.8: Repsonse of step cheange in I_d in detailed model

DC voltage control

Using the linearized model for dc side operation of MMC (eqs. (5.13) and (5.14)), the dc voltage control system for the rectifier end is represented as in fig. 5.9.

The inner tuned control loop is given by eq. (5.19) and this second order transfer function can be approximated by a first order function [110]:

$$\tilde{G}_{CL_{ac}}(s) = \frac{1}{1 + sT_{eq}} \qquad \text{where, } T_{eq} = 2T_e \tag{5.21}$$

Based on this, first order function for inner control loop, open loop transfer function for dc voltage control system is given by:

$$G_{OL_{dc}}(s) = \frac{K_{p_{dc}} K_{DC}}{T_{i_{dc}} \tau_C} \frac{1 + T_{i_{dc}} s}{s^2(1 + sT_{eq})} \tag{5.22}$$

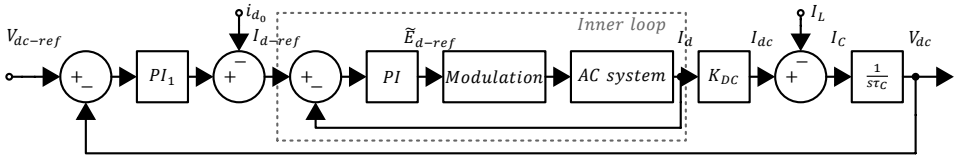
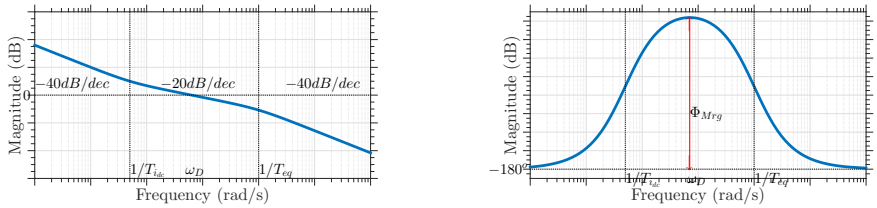


Figure 5.9: DC voltage control system: Rectifier end



(a) Magnitude (b) Phase

Figure 5.10: Bode plot

For this system with a pure integrator, "modulus-optimum" method of pole-zero cancellation is not feasible. In such scenario, the "symmetric optimum" (SO) method [113] can be utilized for optimal selection of controller parameters. This approach similar to the MO aims to attain flat magnitude response for the closed loop system for the largest possible bandwidth. However, in SO this is accomplished by maximization of the phase margin at the crossover frequency.

Maximization of phase margin at crossover frequency yields following parameters for the controller [109, 110]:

$$T_{i_{dc}} = T_{eq}\frac{1+\sin\phi_{Mrg}}{1-\sin\phi_{Mrg}} = T_{eq}a^2 \tag{5.23}$$

$$K_{p_{dc}} = \frac{\tau_C}{K_{DC}\sqrt{T_{eq}T_{i_{dc}}}} \tag{5.24}$$

where, ϕ_{Mrg} is the desired phase margin

Where the recommended value of a is around 3 [109, 110] which yields a phase margin of around $53°$.

5.2. Voltage Balancing control

The objective of voltage balancing control (VBC) is to ensure that capacitor voltage is more or less constant throughout all SMs. This requires instantaneous control, to ensure charging of depleting capacitors and discharging of charged capacitors. Superposition of dc and fundamental current in an arm eqs. (3.50) and (3.51) implies that current through arm changes its polarity. Therefore, within a one-time cycle, there are instants of charging and discharging currents. A calculated approach of insertion and bypassing of SMs can exploit these charging and discharging windows ensuring near voltage balance across all SMs. Below is the description of such techniques.

5.2.1. Capacitor Voltages Ranking Based Approach

With this method voltages across all capacitors are measured at the beginning of switching period and capacitors are ranked in order of their voltages. In a case when arm current is positive, the desired voltage is generated by insertion of sub-modules with the lowest voltage and vice versa [7]. This method ensures charging of capacitors with low voltage and discharging of capacitors with high voltage, thereby balancing the voltage over all capacitors. Besides measurement, the direction of arm currents can be inferred from the change in voltage of an inserted sub-module between two measurements [7]. The increase in voltage of capacitor implies a charging that is positive current and vice versa. This voltage balancing algorithm can be implemented in various ways:

- Fixed sampling frequency: With this approach inserted and bypassed submodules are toggled after a fixed time interval as dictated by the balancing algorithm. This method with a small time interval ensures capacitor voltages are within a tight band however it can lead to higher number of switching operations.
- Fixed band approach: With this method [114] inserted and bypassed submodules are toggled if a submodule's voltage deviates from the pre-defined band.
- Interrupt mode: With this approach, the inserted and bypassed sub-modules are toggled if only if the arm-level modulation dictates a change in the number of sub-modules inserted/bypassed as illustrated in fig. 5.11. This method prevents unnecessary switching operation and is adopted in this study.

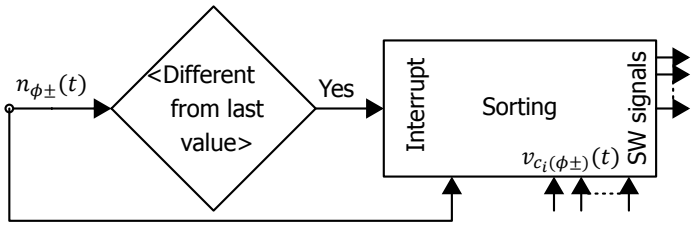


Figure 5.11: Interrupt mode: Capacitor voltage ranking Based VBC

5.2.2. Capacitor voltage balancing loop

This voltage balancing scheme as proposed in [115] for carrier phase shifted PWM generates reference wave for each submodule's using a three-tier control. *Averaging control* controls average capacitor voltage in an arm through circulating current while *balancing control* forces individual capacitor voltage to the reference value and *arm-balancing control* mitigates the difference in average capacitor voltage in positive and negative arms.

This control scheme is only implementable on PWM system and isn't investigated here. Interested readers are directed to references [92, 115–118] for more detail on this control scheme.

5.3. Circulating Current Control

Section 3.3.6 and section A.2 showed the presence of higher order harmonics in the circulating current. Although these harmonics have no significant effect on external characteristics of the converter; their flow tends to increase losses in the system and increase rating requirements for system components. This presents a need for mitigation of these harmonics.

These harmonics can be mitigated either by control of arm voltages or by use of a tuned filters. Article ([80]) proposes the use of a parallel resonant filter in each arm for mitigation of the dominant second harmonic. Article ([119]) presents a detailed analytical analysis for the impact of such filters. However, high voltage reactors are costly [120] and therefore this section is dedicated to control techniques that can mitigate unwanted harmonics in circulating current. Circulating current dynamics are represented by eqs. (3.23) to (3.25), reiterated below for convince.

$$v_{dc}(t) = v_{leg_\phi}(t) + 2v_{circ_\phi}(t) \tag{5.25a}$$

$$v_{leg_\phi}(t) = v_{(\phi+)}(t) + v_{(\phi-)}(t) \tag{5.25b}$$

$$v_{circ_\phi}(t) = L\frac{d}{dt}i_{circ_\phi}(t) + Ri_{circ_\phi}(t) \tag{5.25c}$$

where, v_{circ_ϕ} is the voltage induced in arm reactors due to the flow of circulating current, caused by an imbalance in dc voltage (v_{dc}) and leg voltage (v_{leg_ϕ}).

From eq. (5.25) it can be concluded that by an active compensation in arm voltages ($v_{(\phi\pm)}(t)$) as in eq. (3.32), for the voltage drop caused by circulating current (v_{circ_ϕ}) can mitigate the voltage imbalance and suppress the parasitic harmonics in the circulating current. Furthermore, Section 3.3.6 and section A.2 showed that second order harmonic in circulating current is the most dominant and has a negative sequence.

5.3.1. Synchronous reference frame controller

Based on the aforementioned principles, Tu et al. ([120]) proposes a control scheme for suppression of the dominant second harmonic in the circulating current. This method utilizes a pair of PI controllers that force direct and quadrature components of the second order harmonic, determined via "double fundamental frequency - negative sequence synchronous reference frame transformation", to zero.

The three phase equations representing the circulating current of MMC (eq. (5.25c)) can be transformed to two phase stationary axis using *Clarke's transformation*.

$$v_{circ_{\alpha\beta}} = L\frac{d}{dt}i_{circ_{\alpha\beta}}(t) + Ri_{circ_{\alpha\beta}}(t) \tag{5.26}$$

where, $x_{\alpha\beta} = x_\alpha + jx_\beta$. Park transformation is applied to transform from stationary reference frame to negative sequence double frequency rotating reference frame, i.e. $x_{dq} = x_{\alpha\beta}\ e^{j\int -2\omega\,\mathrm{dt}}$. Incorporating this transformation yields:

$$v_{circ_{dq}}(t) = L\frac{d}{dt}i_{circ_{dq}}(t) + Ri_{circ_{dq}}(t) + 2j\omega Li_{circ_{dq}}(t) \tag{5.27}$$

$$\Rightarrow \begin{cases} v_{circ_d}(t) & = L\dfrac{d}{dt}i_{circ_d}(t) + Ri_{circ_d}(t) - 2\omega Li_{circ_q}(t) \\ v_{circ_q}(t) & = L\dfrac{d}{dt}i_{circ_q}(t) + Ri_{circ_q}(t) + 2\omega Li_{circ_d}(t) \end{cases} \tag{5.28}$$

Transforming eq. (5.28) in Laplace domain yields:

$$V_{circ_d}(s) = (R + sL)I_{circ_d}(s) - 2\omega LI_{circ_q}(s) \tag{5.29}$$

$$V_{circ_q}(s) = (R + sL)I_{circ_q}(s) + 2\omega LI_{circ_d}(s) \tag{5.30}$$

Equations (5.29) and (5.30) defines the relation between circulating currents and voltage imbalance and are depicted in fig. 5.12.

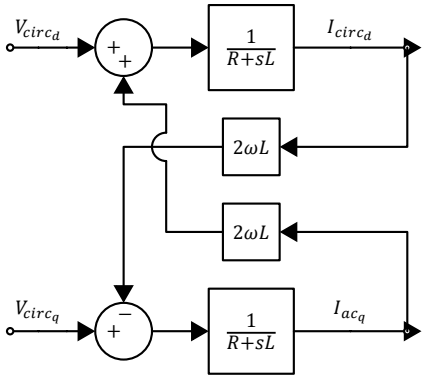


Figure 5.12: D-Q Axis representation of circulating current

However direct and quadrature components are coupled because of $2\omega Li_{circ_q}$ and $2\omega Li_{circ_q}$ terms. To mitigate this cross coupling feed-forward technique is utilized.

$$\widetilde{V}_{circ_d}(s) = V_{circ_d}(s) + 2\omega Li_{circ_q}(s) \tag{5.31}$$

$$\widetilde{V}_{circ_q}(s) = V_{circ_q}(s) - 2\omega Li_{circ_d}(s) \tag{5.32}$$

Substitution of eq. (5.31) in eq. (5.29) and eq. (5.32) in eq. (5.30) yields independent transfer function for direct and quadrature components of second harmonic circulating current. Based on these results separate PI controllers are implemented to suppress these currents to zero. This control scheme is illustrated in fig. 5.13 where reference values ($I_{circ_{d-ref}}, I_{circ_{q-ref}}$) correspond to zero, and the output voltage (v_{circ_ϕ}) is incorporated in insertion indices eq. (3.33).

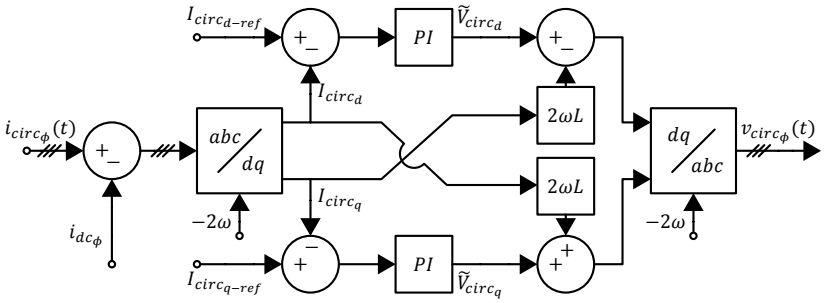


Figure 5.13: Circulating Current Suppression

5.4. Zero sequence current control

As seen in eq. (3.37), zero sequence currents from an unbalanced ac system can propagate to dc side leading to an imbalance in current on positive and negative dc lines. This current component can be eliminated by [99, 100]:

- Coupling converter to ac system un-grounded Y or Δ transformer
  Coupling of the converter to the ac grid through un-grounded Y or Δ transformer with Δ connected on converter side leads to infinite impedance for a flow of zero sequence currents and consequently eliminate their flow.
- Control of arm currents
  For transformer-less configuration or for an asymmetrical fault on converter side of Δ transformer flow of zero sequence currents in the converter is inevitable. These zero sequence currents subsequently lead to an imbalance in dc line currents as seen in eq. (3.37). Nevertheless, MMC with distributed storage allows control over the zero sequence components [100]. This control can be either be incorporated in vector control of converter as detailed in [100] or can be achieved by regulating insertion index in each arm individually as presented in [99].

5.5. Conclusion

This chapter presents a brief review of control techniques required for a grid-connected MMC that ensures desired terminal and internal characteristics. For the design of controllers, a linear-time invariant model of MMC is derived. Based on this model the chapter presents an optimal design of controller to regulate ac/dc voltage waveforms and real/reactive power flow with the AC grid. Furthermore, an account of various voltage balancing techniques, that ensure equal voltage across capacitors in an arm, are presented. Lastly, methods for suppression of unwanted harmonics in circulating current and zero-sequence currents propagating from unbalanced ac-side are discussed.

6

Modulation

Modulation translates the reference values from the control system to the gate signals for individual IGBTs. This chapter presents a brief overview of modulation schemes for modular multilevel converters.

The modulation system for modular multilevel converters enables energy balance in the arms of converter and voltage balancing across individual submodule capacitors. Based on these objectives, the modulation schemes for MMCs are split into two tiers i.e.:

- Arm Level Modulation.
  This level of modulation translates reference values of upper-level and auxiliary control to regulate an individual arm through insertion index or arm energy controllers. The modulation ensures that the inserted voltage in a phase leg, v_{leg_ϕ}, and the arm cumulative capacitor voltage, $v_{c_{\phi\pm}}^{\Sigma}$, correspond to the dc link voltage.
- Module Level Modulation.
  The objective of the module-level modulation is to generate gate signals for each sub-module. These switching patterns define insertion and bypassing of sub-modules, which not only influence the voltage the waveform on ac and dc sides but also control the voltage of a submodule's capacitors. Therefore, this level of modulation needs to conform with the arm-level modulation and the voltage balancing control.

6.1. Arm Level Modulation

The objective of this modulation is to generate insertion indices for all arms of MMC, to achieve desired reference values (i.e. $e_{ref\phi}$, $v_{dc_{ref}}$) as dictated by the controller. Insertion index is the ratio of sub-modules inserted in an arm and consequently defines the voltage inserted by an arm. Therefore, this modulation determines the number of sub-modules "inserted" in positive and negative arms of phase leg.

The generic expression of insertion index as derived in eq. (3.33) is reiterated below:

$$n_{\phi+}(t) = \frac{\frac{v_{dc}}{2} - e_{ref\phi} - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi+}}(t)} \tag{6.1}$$

$$n_{\phi-}(t) = \frac{\frac{v_{dc}}{2} + e_{ref\phi} - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi-}}(t)} \tag{6.2}$$

Different techniques and simplification can be incorporated to determine modulation indices given by eqs. (6.1) and (6.2). Following is the description of such modulations techniques.

6

6.1.1. Direct modulation

Direct modulation is an "ideal open-loop modulation" [40]. It assumes cumulative capacitor voltage of an arm constant and equal to the dc voltage i.e. $v^{\Sigma}_{c_{\phi\pm}} = v_{dc}$ [121]. This further implies that the modulation ignores any voltage imbalance in a phase leg i.e. $v_{circ_\phi} = 0$.

Incorporation of these assumptions and using eqs. (3.28) and (3.45) reduces insertion indices given by eqs. (6.1) and (6.2) to:

$$n_{\phi+}(t) = \frac{1 - \hat{m}_\phi \cos(\omega t + \Phi_\phi + \alpha)}{2} \tag{6.3}$$

$$n_{\phi-}(t) = \frac{1 + \hat{m}_\phi \cos(\omega t + \Phi_\phi + \alpha)}{2} \tag{6.4}$$

In short with this modulation approach, "inserted" sub-modules in the positive and negative arm are varied in a sinusoidal fashion as dictated by ac voltage with a phase difference of 180° and an offset of half of the dc voltage.

However as discussed earlier, the flow of fundamental current through the capacitors implies a voltage ripple. The absence of compensation for the capacitor voltage ripple in this modulation results in a substantial magnitude of circulating currents harmonics; leading to higher losses and higher rating requirement for the components.

6.1.2. Uncompensated Modulation

Uncompensated modulation similar to the direct modulation assumes a constant cumulative capacitor voltage, equal to the dc link voltage ($v^{\Sigma}_{c_{\phi\pm}}(t) = v_{dc}$). However, this modulation utilizes reference values $e_{ref\phi}$ and v_{circ_ϕ} from their respective control loops.

$$n_{\phi+}(t) = \frac{\frac{v_{dc}}{2} - e_{ref\phi} - v_{circ_\phi}}{v_{dc}} \tag{6.5}$$

$$n_{\phi-}(t) = \frac{\frac{v_{dc}}{2} + e_{ref\phi} - v_{circ_\phi}}{v_{dc}} \tag{6.6}$$

In short, this modulation method corrects for the imbalance in dc link voltage and leg inserted voltage but doesn't compensate for varying cumulative capacitor voltage in an arm.

6.1.3. Compensated Modulations

In compensated modulation schemes ([122]), estimated or measured cumulative capacitor voltage is utilized in the calculation of the insertion index to correct for the varying cumulative capacitor voltage in an arm. These methods are explained as follows:

Measured cumulative capacitor voltage

In this closed loop modulation, cumulative capacitor voltage in all arms i.e. $v^{\Sigma}_{c_{\phi\pm}}$ are measured continuously [40]. Based on the desired internal e.m.f $e_{ref\phi}$ and calculated v_{circ_ϕ} insertion indices are computed as:

$$n_{\phi+}(t) = \frac{\frac{v_{dc}}{2} - e_{ref\phi} - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi+}}(t)} \tag{6.7}$$

$$n_{\phi-}(t) = \frac{\frac{v_{dc}}{2} + e_{ref\phi} - v_{circ_\phi}}{v^{\Sigma}_{c_{\phi-}}(t)} \tag{6.8}$$

Direct implementation of this method, leads to instability in capacitor voltages and imbalance in stored energy of positive and negative arms [40, 121]. Nevertheless, based on these measured cumulative capacitor voltages, the total energy controller, that uses PI controllers to regulate total stored energy in a phase leg and imbalance between arms has been proposed and validated in [40].

However, with hundreds of SMs, this method is plagued by delays associated with measurement and communication of signals [95].

Estimated cumulative capacitor voltage

In this control scheme as proposed in [95, 121], estimated cumulative capacitor voltages in an arm are utilized for the calculation of insertion indices. .

To determine the cumulative capacitor voltages the total energy in a phase arm is estimated. For this, it is assumed that circulating current is purely direct current. This purely direct circulating current from eq. (3.42) is given as:

$$i_{circ_{\phi_0}} = \frac{\hat{e}_\phi \, \hat{i}_{ac} \cos(\theta + \alpha)}{v_{dc} + \sqrt{v_{dc}^2 - 4R\hat{e}_\phi \, \hat{i}_{ac} \cos(\theta + \alpha)}} \tag{6.9}$$

$$v_{circ_{\phi_0}} = R i_{circ_{\phi_0}} \tag{6.10}$$

The load current i_{ac_ϕ} is measured at the real time, and value of $\hat{i}_{ac}$ and θ for the fundamental component are determined. With these results and the reference value of e.m.f, stored energy in an arm is estimated by integrating eqs. (3.63) and (3.64).

$$\begin{aligned}\tilde{W}^{\Sigma}_{+\phi} &= \int \left(\frac{v_{dc}}{2} - e_\phi - v_{circ_{\phi_0}}\right)\left(i_{circ_{\phi_0}} + i_{diff_\phi}\right)dt \\ &= \frac{1}{2\omega}\left(\frac{v_{dc}}{2} - R i_{circ_{\phi_0}}\right)\hat{i}_{ac}\sin(\omega t + \Phi_\phi - \theta) - \frac{1}{\omega}\hat{e}_\phi i_{circ_{\phi_0}}\sin(\omega t + \Phi_\phi + \alpha) \\ &\quad - \frac{1}{8\omega}\hat{e}_\phi \hat{i}_{ac}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta) + W^{\Sigma}_{+\phi 0}\end{aligned} \tag{6.11}$$

And similarly,

$$\begin{aligned}\tilde{W}^{\Sigma}_{-\phi} &= -\frac{1}{2\omega}\left(\frac{v_{dc}}{2} - R i_{circ_{\phi_0}}\right)\hat{i}_{ac}\sin(\omega t + \Phi_\phi - \theta) + \frac{1}{\omega}\hat{e}_\phi i_{circ_{\phi_0}}\sin(\omega t + \Phi_\phi + \alpha) \\ &\quad - \frac{1}{8\omega}\hat{e}_\phi \hat{i}_{ac}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta) + W^{\Sigma}_{+\phi 0}\end{aligned} \tag{6.12}$$

where, $W^{\Sigma}_{+\phi 0}$ and $W^{\Sigma}_{-\phi 0}$ are the reference values for total capacitor energies in positive and negative arm receptively. From these estimates, cumulative capacitor voltages are calculated as:

$$\tilde{v}^{\Sigma}_{c_{\phi\pm}} = \sqrt{\frac{2N}{C}\tilde{W}^{\Sigma}_{\pm\phi}} \tag{6.13}$$

The insertion indices are consequently are given by

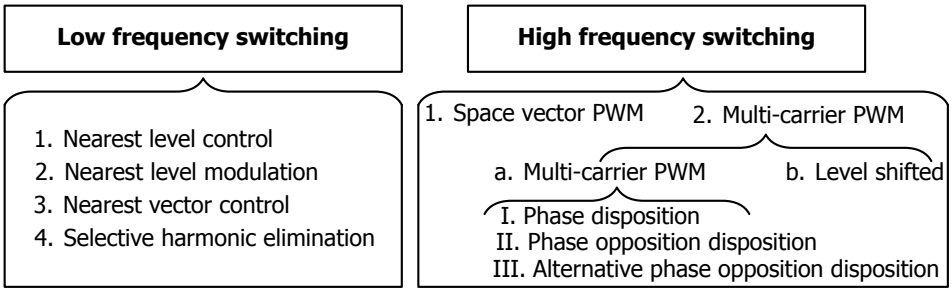
$$n_{\phi+}(t) = \frac{\frac{v_{dc}}{2} - e_{ref\phi} - v_{circ_\phi}}{\tilde{v}^{\Sigma}_{c_{\phi+}}(t)} \tag{6.14}$$

$$n_{\phi-}(t) = \frac{\frac{v_{dc}}{2} + e_{ref\phi} - v_{circ_\phi}}{\tilde{v}^{\Sigma}_{c_{\phi-}}(t)} \tag{6.15}$$

This method provides compensation for variation in the capacitor voltage and mitigates parasitic harmonics in circulating current without incurring additional measurement or communication requirements [95, 121].

6.2. Module Level Modulation

Module level modulations for multilevel converters are an extension of the traditional modulation techniques. In general for multilevel converters, modulations can be categorized into two groups i.e. low-frequency switching methods and high-frequency switching methods [70]. These module level modulation schemes for MMC are classified as follows:



As seen in eq. (3.5) with N sub-modules in an arm, each arm of an MMC can generate $N+1$ levels. However, based on the operation of complementary arms, $N+1$ or $2N+1$ levels can be obtained for the ac-waveform. Therefore, all modulation techniques based for MMC can be further categorized as:

- $N+1$ Level Modulation:
  In this modulation scheme, the arms in a phase leg operate in a complementary manner. The transition from one voltage level to other is accomplished by synchronous commutation in both arms i.e. insertion of a sub-module in one arm and bypassing of a sub-modules in the other arm. The converter with this operation continuously maintains the total number of submodules inserted in a leg to N, ensuring constant voltage on the dc side (ignoring voltage ripple).

- $2N+1$ Level Modulation:
  On the other hand, independent control of positive and negative arms can generate $2N+1$ levels in ac phase voltage. With this operation, arms in a phase leg no longer operate in a complementary fashion. Rather than synchronous switching in positive and negative arms of a phase leg, the transition from one voltage level to other is accomplished by commutation in just one arm [123]. This modulation with increased number of levels in ac-voltage significantly reduces the total harmonic distortion in ac-voltage and current, and the EMI contributed by $\frac{dv}{dt}$. Moreover, switching frequency remains identical to that of the $N+1$ level method. However with this approach, the total inserted sub-modules in an arm are no longer constant which leads to variation in the dc-link voltage contributing to additional components in the circulating currents and voltage spikes across the arm reactors.

The ideal modulation for MMC should attain minimization of switching frequency, capacitor voltage ripple, harmonic distortion in ac-waveform and computational load of modulation itself. Counterpoising nature of these factors implies that all

modulation methods have their pros and cons which will become evident from the description of all of these modulations in the following sub-sections.

6.2.1. Nearest Level Control

Nearest level control [114, 124] is one of the simplest modulation techniques. It directly determines the switching state without any requirement for any carrier waves or complex calculations. The essence of NLC is the approximation of a sinusoidal waveform by an equivalent staircase quasi-sinusoidal wave as illustrated in fig. 6.1. With this modulation, the desired number of inserted sub-modules in an arm are computed by rounding the product of insertion indices as given by the arm level modulator and N i.e. eq. (6.16).

$$N_{ins.\phi\pm} = round\left[Nn_{\phi\pm}(t)\right] \tag{6.16}$$

A change in $N_{ins.\phi\pm}$ triggers the voltage balancing control and gate signals are updated based on the desired number of sub-modules inserted/bypassed and the voltage balancing control. This modulation method for MMC as discussed earlier, based on the operation of positive and negative arms of phase leg can generate $N+1$ level or $2N+1$ level in ac voltage as detailed below:

- $N+1$
  In this case, the product of N and insertion index eq. (6.16) is rounded-up to the nearest integer if its fractional part is greater than 0.5 and vice-versa. This approach with complementary operation in positive and negative arms generates $N+1$ levels with a step size of v_C in ac-waveform while maintaining the total inserted sub-modules inserted in a leg to N. The ac-waveform form with this method deviates up to $0.5v_C$ from the reference signal.
- $2N+1$
  A variant of $N+1$ method as proposed in [125] rounds up in eq. (6.16) when fractional part is greater than 0.25. This implies that commutations in positive and negative arms are no longer synchronous. This leads to $2N+1$ levels in the ac-waveform with half of the step size i.e. $0.5v_C$. However total inserted sub-modules in a leg vary between N and $N+1$. The ac-waveform form with this method deviates up to $0.25v_C$ from the reference signal.

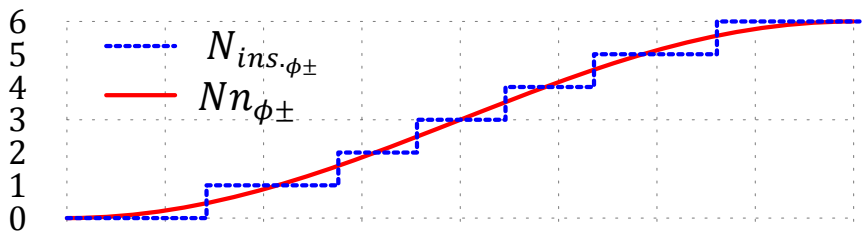


Figure 6.1: Nearest Level Control - 7 Levels

Overall, NLC with a low number of levels produces a poor quality of ac-waveform; making this modulation only effective with a high number of levels. Nevertheless in MMCs with N in order of 100's, the waveform synthesized is adequate, and system benefits from the simple carrier-less implementation.

6.2.2. Nearest Level Modulation

Nearest level modulation (NLM) as proposed in [79, 126] is based on the NLC. However, instead of approximating reference waveform to the nearest level ($N_{ins.\phi\pm}$), this modulation toggles between two nearest voltage levels with a fixed frequency. The converter is switched such that the time average of the two levels over one switching cycle corresponds to the mean value of reference wave over that period. Figure 6.2 illustrates the implementation of NLM. This modulation is implemented without utilizing any carrier waves and tends to become more accurate at a higher switching frequency.

The consecutive nearest levels and duty cycle for the higher level are determined using eqs. (6.17), (6.18) and (6.20):

$$N_{L-ins.\phi\pm}(t) = round_{(floor)}\left[Nn_{\phi\pm}(t)\right] \tag{6.17}$$

$$N_{H-ins.\phi\pm}(t) = N_{L-ins.\phi\pm} + 1 \tag{6.18}$$

The time average of the two levels in one switching cycle should correspond to the mean value of reference wave i.e.

$$[Nn_{\phi\pm}(t)]_{ref-avg} = \frac{1}{T_{SW}}\left(N_{L-ins.\phi\pm}(1 - d_{i_{\phi\pm}})T_{SW} + (N_{L-ins.\phi\pm} + 1)d_{i_{\phi\pm}}T_{SW}\right) \tag{6.19}$$

This yields the duty-cycle for the switching period as:

$$d_{i_{\phi\pm}}(t) = [Nn_{\phi\pm}(t)]_{ref-avg} - N_{L-ins.\phi\pm}(t) \tag{6.20}$$

where, $round_{(floor)}(a)$ operand approximates to the nearest integer less than or equal to a. Reference [127] presents a variant of NLM that yields $2N + 1$ levels in the ac-waveform.

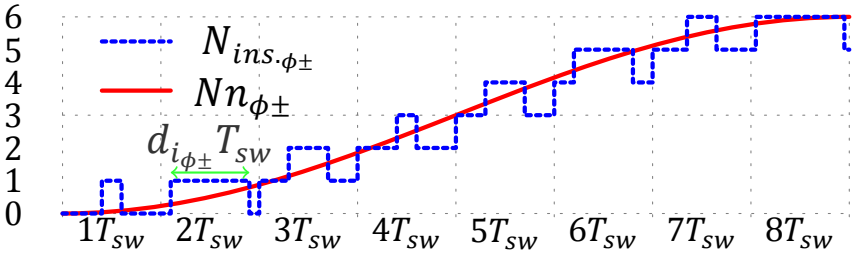


Figure 6.2: Nearest level modulation - 7 Levels

6.2.3. Multi-carrier PWM techniques

Similar to two-level carrier based PWM, the essence of the multi-carrier counterpart is the natural sampling of a single modulating (sinusoidal reference) signal through triangular carrier wave(s). With multi-carrier PWM (C-PWM) each complementary pair of switches in the converter is represented by its individual triangular carrier wave and modulating signal is shared across all switches [128]. Based on the classical technique, the crossing of the modulating signal with a carrier wave implies a change in state for that complementary pair of switches.

C-PWM, as discussed earlier, are split into $N+1$ level and $2N+1$ level methods.

- $N+1$ Level Modulation:
  With the complementary operation of positive and negative arms, this approach generates $N+1$ levels in the output ac-voltage and requires N triangular carrier waves. Each carrier wave in this scheme corresponds to a sub-module in one arm and its complementary counterpart in the other arm of the phase leg.
- $2N+1$ Level Modulation:
  This variant as proposed in [129] requires $2N$ triangular carrier waves, for each sub-module in a phase leg.

For all of the carrier based modulation techniques the parameters that control modulation are [130, 131]:

- Amplitude Modulation Index ($m_{amp.}$)
  The ratio of the amplitude of the modulating signal and the carrier waveforms band.
- Frequency Modulation Index (m_f)
  The ratio of the frequency of carriers (f_c) to that of the modulating signal (f_0) i.e. $m_f = \frac{f_c}{f_0}$
- Phase displacement angle ($\phi_{dis.}$)
  The angle between the modulating signal and the first positive triangular carrier wave.

Intuitively a M level converter requires $M-1$ carrier waves. Based on the spatial distribution of carrier waves multi-carrier PWM Techniques are categorized as [131]:

1. Level shifted carrier PWM method.
2. Phase shifted carrier PWM method.

Level shifted carrier PWM method

This technique as introduced in [130] utilizes $M-1$ carrier waves for a M-level converter. The carrier waveforms have identical peak-to-peak amplitude A_c and frequency and are disposed in such a manner that the contiguous bands fully occupy range between $-\frac{1}{2}(M-1)A_c$ to $\frac{1}{2}(M-1)A_c$. The i_{th} carrier wave is displaced by $(\frac{1}{2}(2i_{th}-M-1))A_c$ from the abscissa. Since there is no restriction on the

phase displacement between the two adjacent triangular carriers, this modulation technique can be sub-categorized as [130]:

- Phase disposition (PD)
  In this method, all of the carrier waves are in phase as illustrated in fig. 6.3. This stacking approach leads to a significant harmonic component at the carrier frequency in the phase waveform; however, these harmonics tend to cancel out in the line-line voltages [101].

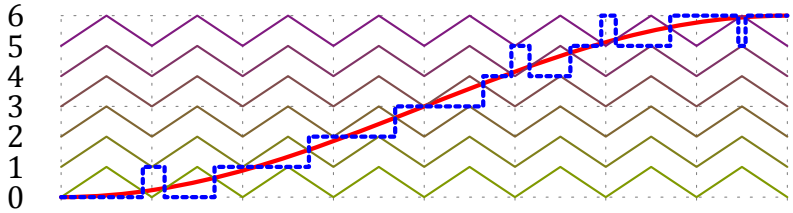


Figure 6.3: Carrier wave-forms for phase disposition PWM - 7 levels

- Phase opposition disposition (POD)
  All carrier waves in positive/negative levels are in phase in their respective groups with a mutual phase displacement of 180° as illustrated in fig. 6.4. With this approach, both phase and line-line voltage waveforms have significant harmonics around the carrier frequency [101].

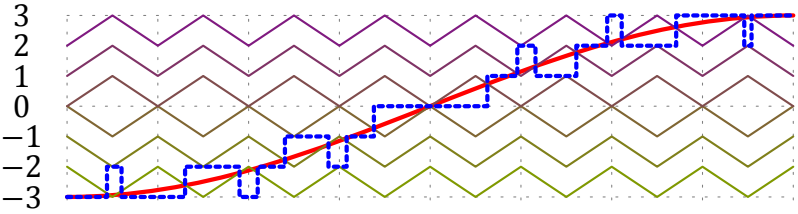


Figure 6.4: Carrier wave-forms for phase opposition disposition PWM - 7 levels

- Alternative phase opposition disposition (APOD)
  Adjacent carrier waves are in phase opposition to each other as illustrated in fig. 6.5. This level and phase shifting scheme has significant harmonics in the sidebands of the carrier frequency [101].

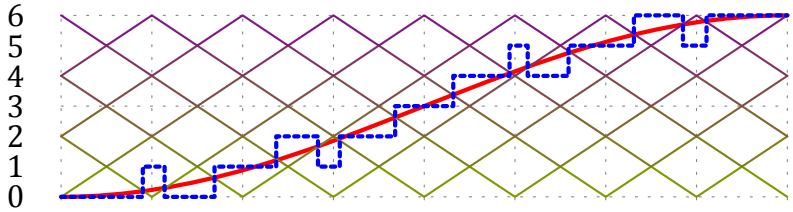


Figure 6.5: Carrier wave-forms for alternative phase opposition disposition PWM - 7 levels

Continuous comparison of the modulating signal and the carrier waveforms generate the switching sequences for the converter. Each waveform corresponds to an active device (sub-module). If the modulating signal is greater than a particular carrier waveform the corresponding active device (sub-module) is switched on (inserted) and if the modulating signal is smaller than a particular carrier waveform the respective active device (sub-module) is switched off (bypassed) [132]. The amplitude modulation index for this modulation is given by [131]:

$$m_{amp.} = \frac{A_0}{0.5(M-1)A_{cpp}} \qquad \begin{cases} A_0 & = \text{Amplitude of modulating signal} \\ A_{cpp} & = \text{Peak-to-peak amplitude of a carrier signal} \end{cases} \tag{6.21}$$

With this modulation, the switching frequency of an individual active device (sub-module) is far less than that of the carrier frequency. However, the total number of switching events in a cycle as investigated in [132] vary with phase displacement angle ($\phi_{dis.}$). The effective switching frequency can be greater than or less than carrier frequency depending upon the phase displacement angle ($\phi_{dis.}$) which can be used to optimize switching frequency for a given $m_{amp.}$ and m_f [132].

Phase-shifted carrier PWM

Similar to the carrier disposition method this modulation technique consists of $M-1$ triangular carrier waves for a M-level converter. These carrier waves are phase shifted from each other by $\frac{360^\circ}{M-1}$ as illustrated fig. 6.6.

For the case where separate carrier waves are used for positive and negative arms phase shift for positive arm sub-modules is given by $\alpha_{i+1} = \alpha_i + \frac{360^\circ}{M-1}$ and negative arms is given by $\alpha_{i+1} = \alpha_i + \frac{360^\circ}{M-1} + \frac{180^\circ}{M-1}$. Comparison of i_{th} carrier waveform with the reference/modulation waves gives the "firing signal" for that sub-module.

The amplitude modulation index for this modulation is given by [131]:

$$m_{amp.} = \frac{A_0}{A_{cpp}} \qquad \begin{cases} A_0 & = \text{Amplitude of modulating signal} \\ A_{cpp} & = \text{Peak-to-peak amplitude of a carrier signal} \end{cases} \tag{6.22}$$

With this modulation, the switching frequency of an individual active device (sub-module) is equal to that of the carrier frequency [131].

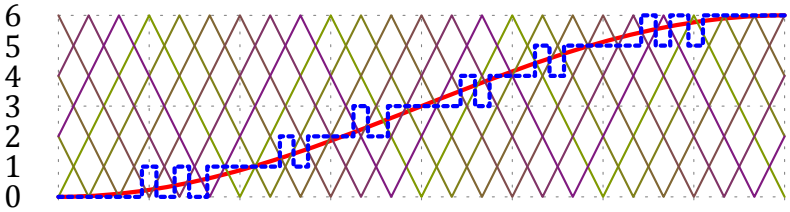


Figure 6.6: Carrier wave-forms for phase-shift PWM - 7 levels

Voltage balance with multi-carrier PWM

As discussed above, for MMC, carrier based PWM can have N or $2N$ carriers where each carrier corresponds to an individual sub-module or a pair of complementary sub-modules in complementary arms. However, identical construction of sub-modules implies that transition from one level to another can be attained from any sub-module. Therefore, carrier waves are not explicitly associated with any sub-module, and this can be utilized in the incorporation of voltage balancing in the modulation.

Voltage balancing algorithm as discussed in section 5.2 can be used to translate the commutation command from PWM to the most appropriate sub-module(s). Reference [128] presents such voltage balancing technique for cascaded H-bridge converter on carrier-based modulation which has been adapted for MMC in reference [133] with phase shift PWM. This technique, although accurate, requires continuous monitoring of all capacitor voltages and adds complexity to the control system.

Circular transposition of carriers as presented in [134, 135] is an alternative for voltage balancing algorithm for carrier disposed PWM method. With this approach, triangular carriers are alternated among sub-modules after every fundamental cycle. This rotation cycle is periodic with a period of N fundamental cycles and is illustrated for phase disposed 9 level PWM (fig. 6.3) in fig. 6.7 . Identical switching sequence implies that this rotation ensures equal charging and discharging of all sub-modules ensuring voltage balance across all capacitors.

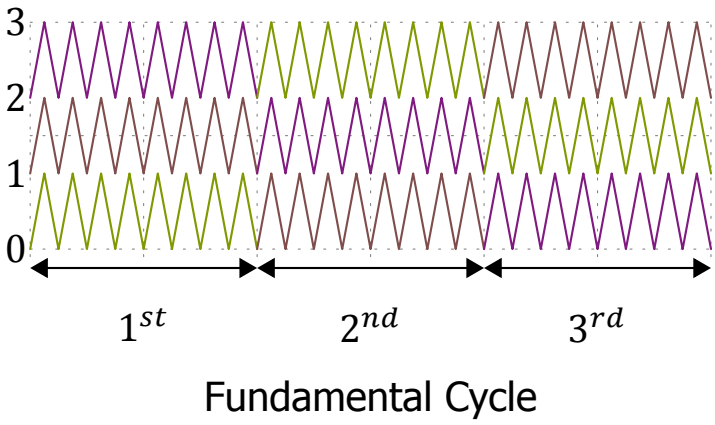


Figure 6.7: Carrier wave-form rotation for phase disposition PWM - 3 levels

Comparison of phase disposed PWM and phase shift PWM of MMC has been presented in [135, 136]. Detailed comparison with $2N+1$ modulation scheme in [135] reveals the superiority of carrier rotated phase disposed PWM over phase shift PWM in terms of total harmonic distortion of the output voltage.

6.2.4. Space-vector domain

Space vector domain based modulation techniques are based on the unified control of all phase legs of the converter. In this modulation, converter's discrete output voltages (for all possible switching states) and the reference waveform are represented in the form of stationary and rotating vectors in a complex plane (α – β plane) as illustrated in fig. 6.8. Using this vectorial representation the desired voltage is synthesized either via nearest vector control or space vector PWM.

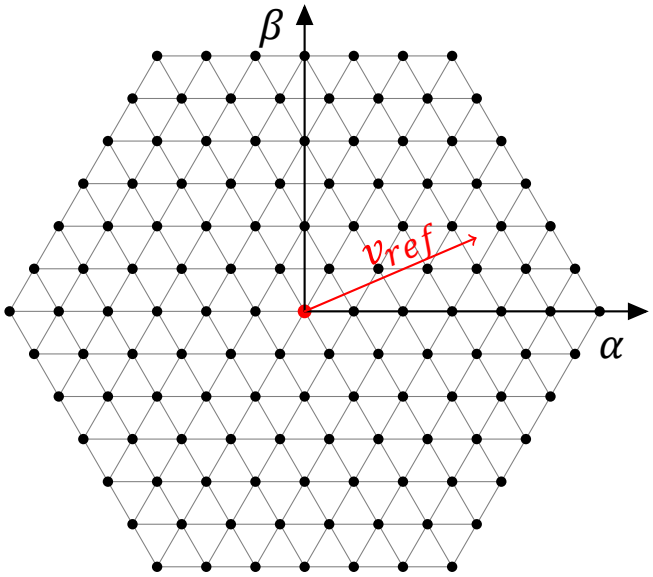


Figure 6.8: Space Vector/ Nearest Vector - 7 levels

Nearest vector control

This modulation method approximates the reference vector with the closest state vector and is the vector domain equivalent of NLC method [71]. Like NLC, this modulation is only suitable for a high number of levels. However, mapping of state vector and identification of nearest vector requires an algorithmic approach and tends to make this modulation far more complex than NLC [70].

Space-vector modulation

In space vector modulation the converter is switched between the three (2D-SVM) or four (3D-SVM) nearest state vectors with calculated dwell times; such that the time average output voltage over one switching cycle corresponds to the reference vector. Articles [5, 7] present the control of 5-level MMC with SVM. However with high number of levels mapping of state-vectors, identification of nearest vector and implementation of SVM tends to become complex

6.2.5. Selective harmonic elimination

The selective harmonic elimination (SHE) method is based on Fourier analysis to eliminate particular harmonics from the output waveform [65]. By introducing notches in the waveform with calculated switching angles, undesired harmonics can be mitigated from the output waveform. This technique yields the desired waveform with minimal switching with firm control on the low order harmonics. Reference [137, 138] present the operation of MMC under SHE-PWM.

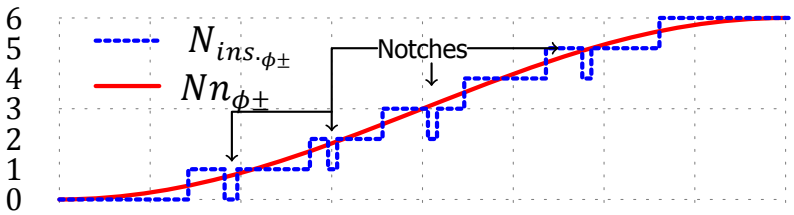


Figure 6.9: Selective harmonic elimination - 7 levels

However, this modulation method tends to become more and more complex with the increasing number of levels, due to the associated higher number of switching angles and their computation. Moreover, the offline computation of switching angle makes SHE only suitable for open-loop or low bandwidth applications [71].

6.3. Conclusion

All of the modulation discussed above are implementable on the MMC, and each offers their advantages and shortcomings. Carrier based PWM techniques tend to have high switching frequency which although reduces harmonic content of ac-waveform, lead to higher losses in the system. Furthermore, this modulation requires carrier waves equal to the number of levels with precise phase or level displacement. This demands for an accurate carrier wave generation which tends to become problematic with a large number of levels [126]. NLM an alternative to PWM can produce high-quality ac-waveform without requiring carrier wave; however this modulation requires higher switching frequency to be effective. SVM and SHE can optimize harmonic content in ac-waveform relative to the switching frequency but tend to suffer from high computational burden especially with the higher number of levels in MMC. NLC and NVC are only viable with a large number of levels where NVC is more complex to implement as compared to NLC.

For HVDC application with a high number of levels, the desired modulation should minimize losses and ensure low implementation complexity. With this criterion, NLC with its simple implementation and low switching frequency emerge as the most suitable. Therefore for this study NLC is considered for the module-level modulation unless otherwise stated.

7

AC & DC Fault Ride through Capability

Grid-connected converters have to comply with grid codes. This chapter is dedicated to MMC's capabilities to ride through ac and dc side disturbances.

Increasing contribution of power in electric network via converter system implies a need for their compliance with grid codes. Grid codes dictate the expected operation of generation units under steady state and transient conditions to ensure system stability. They define operating range for voltage and frequency, real and reactive power control capabilities, fault ride through capabilities, etc. In an HVDC system irrespective of the generating unit, grid-side converter defines the power quality and is accountable for compliance with the grid codes. For grid connected converters THD of a voltage at a point of common coupling (PCC) and fault ride through capabilities are of prime interest [139].

Previous chapters detailed the operation of MMC under steady-state conditions to attain desired real and reactive power exchange and its ability to synthesize near perfect sinusoidal voltages. With a sufficient number of levels, THD with MMC is low enough to remove the requirement of filters. Similarly, converters behavior under grid disturbance or fault conditions is subject to stringent grid codes. This requires that converter not only has to survive faults but ensure minimum impact on the system and provide ancillary services to aid system's recovery. External faults/disturbances in a grid-connected converter can be divided into ac and dc side disturbances.

7.1. AC disturbances

AC side disturbances can lead to voltage sag and swell. Voltage sag (swell) refers to decrease (increase) in fundamental frequency voltage for a short period (0.5 cycle to 1 min). Sags are contributed to short circuit faults, an abrupt increase in the load, etc. Whereas, voltage swells originate from an abrupt reduction in the load. The disturbances on ac grid of converter can be broadly categorized as:

- Balanced Faults
  All phases undergo same voltage drops/swell.
- Unbalanced Faults
  Phases undergo different voltage drops/swell.

During an ac side disturbance, MMC control system through the reference current limiters ensures that currents on ac and dc side of the converter are within their rated limits. This allows for the converter to remain connected to the grid and support it by injection of reactive power for short intervals of fault Moreover after fault clearance, the converter system is expected to return to its pre-fault active power supply in a short interval.

This capability of a system to remain operational for significant voltage drops for order hundred milliseconds, and withstand a recovery period with depressed voltage for a few seconds is termed as the *low-voltage ride through* (LVRT) [140]. Similarly, an ability to operate ability at zero voltage is called zero voltage ride through (ZVRT) [140]. Figure 7.1 illustrates typical LVRT requirements for grid-connected converters. Similarly, high voltage ride through capabilities of a convert can be defined. LVRT is vital as it ensures active compensation for the fault, which otherwise can lead to cascading failure in network leading to a widespread blackout. Reference [141] summarizes and investigates Britain's grid code for ac fault ride through of MMC based HVDC system.

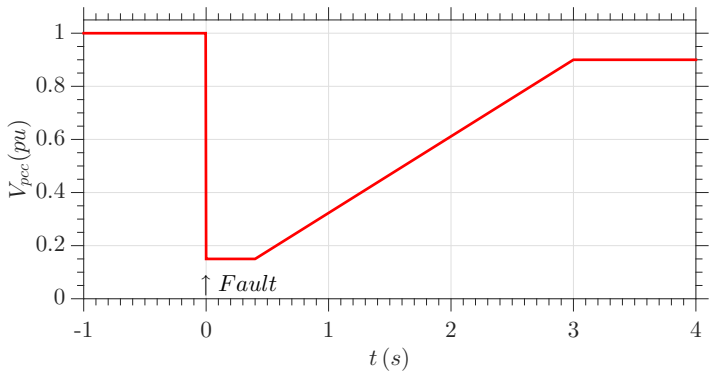


Figure 7.1: Typical LVRT requirements

7.2. DC disturbances

Compared to ac faults, dc faults in a VSC-converter tend to be more severe and lead to high currents in the converter. Faults in dc cables tend to be permanent which result in permanent interruption of power transmission capability, and such case requires permanent shutdown of the converter. On the other side lightning or tree strikes on overhead lines tend to be temporary and can be removed by interrupting current for a short duration, enabling restoration of natural insulation [142]. This temporary interruption of fault can be achieved either by ac or dc breakers. AC circuit breaker takes from 10 to 100ms to interrupt the current; whereas HVDC breakers which are still in the process of development allow for a faster interruption.

In conventional VSCs, discharge of dc link capacitor adds to the fault currents in case of dc faults. MMC with its distributed capacitors, arm reactors and blocking state offer superior fault tolerance and system recovery capabilities as compared to conventional VSC [143, 144]. Arm reactors limit fault current, and the blocked state of SMs inhibit discharge of distributed capacitors which not only reduces damage by fault but enables faster recovery of the HVDC system. However, freewheeling diodes in half-bridge SMs give way to current from the ac-grid to the fault. This presents a need for operation of circuit breakers on the ac or dc-side.

7.3. Conclusion

In conclusion MMC with distributed capacitors, arm reactors and blocking state has superior dc fault tolerance and system recovery capabilities as compared to conventional VSC. Articles [143, 144] presents a detailed comparison of AC and DC fault performance in different VSC including MMC.

8

EMT Modeling

Computer simulations offer a powerful tool to investigate the dynamics of a system and provide a platform for the design of controllers. This chapter delves into modeling techniques for MMCs.

Modeling, a mathematical representation, enables replication of characteristics of a real world system via computer simulation. These simulations provide a platform for the development of design, understanding of operation and postmortem analysis of the system. Simulation is formally defined as:

> "The process of designing a model of a real system and conducting experiments with this model for the purpose either of understanding the behavior of the system or of evaluating various strategies (within the limits imposed by a criterion or a set of criteria) for the operation of the system" [145].

With changing energy landscape, power electronics system such as FACTS and HVDC are finding more frequent applications in the modern power system. New topologies and application specific design of power electronic devices present a need for robust simulation for integrative power electric and electronic systems. Modeling and computer simulation enable efficient design and operational planning for such systems. Besides steady state operation, power systems are subjected to transients; which accompany transition of the power system from one steady state to another due to a physical disturbance. Transients can be caused by external factors such as lightning or by an internal factor such as switching. These transients can lead to over-voltages, over-currents, abnormal waveforms and other unwanted phenomenon causing stressing of the power system and end user equipment. Hence, computer simulation of transients is of paramount importance for a power system.

"The operation of an electrical power system involves continuous electromechanical and electromagnetic distribution of energy among the system components" [145]. Electromechanical devices refer to generators/motors that convert mechanical and electrical energy and electromagnetic energy refers to electric and the magnetic fields associated with inductance and capacitance of system components. Transients affect this energy exchange; consequently, voltages and currents in the system are subject to deviation from their equilibrium state. Based on this, operating conditions of a power system can be classified as [146]:

- *Stationary/Steady state conditions*
  Steady state conditions imply that system under consideration is operating under constant load and topology. Such a system can be modeled by voltage and current phasors in the frequency domain without explicit modeling of the energy exchange.
- *Transients*
  Transients accompany transitions of the power system from one steady state to another. Based on the mode of their generation transients are sub-categorized as electromechanical and electromagnetic transients.
  - *Electromechanical transients*
    These relatively slow transients are attributed to an imbalance in power generation and consumption in a power system and are associated with rotating machines. For example, transient as a result of changing speed of a generator. Stability simulation is performed for analyses of such transients, with an assumption that energy exchange in the system occurs at the power frequency [147]. Such transients are modeled via phasor analysis with mechanical time constants (ac sources of varying rms values) or state space modeling.
  - *Electromagnetic Transients*
    Electromagnetic transients (EMTs) are attributed to reaction of electric and magnetic energy distribution in the system as a result of the change in system topology. Instantaneous changes (e.g. switching, faults, lightning) in system's current and voltage result in this transient. Simulation of these transients requires explicit modeling of the energy exchange in the system.

Although both of these transients coexist, the nature of disturbance tends to make one dominant over another. For power electronic systems, where switching operation is integrals, EMTs dominate in the system. Therefore in this study focused on MMCs, EMTs are of prime interest and subsequent reference to 'transients' is addressed to EMTs only.

8.1. Electromagnetic Transients

In general, electromagnetic transients are triggered by changes in the network topology such as lightning stroke, faults, breaker operation, power electronic devices [147].

Simulation of these transients find application in [148]:

- Design and validation of protective system and control
- Design of HVDC and FACTS systems
- Insulation Coordination
- Power quality studies

Electromagnetic transients decay rapidly, and their local nature implies that for precise simulation of these transients only detailed modeling of EMT sources and the network elements is required. Therefore in the investigation of EMTs power electronic devices, transformers, transmission line, cables are modeled in detail while power stations are simply modeled as ideal voltage sources behind transient/subtransient impedance [147].

8.1.1. Simulation Program

Various software packages are available for the simulation of EMTs, as reported in [148]. Both frequency and time domain solution methods are available for numerical simulation. Each method has its advantages and limitations; however time domain methods have superior capabilities in handling system dynamics, power electronic interface, and transients [149].

Time domain solvers include general *EMT-type* solver to specialized program such as *SPICE*. *SPICE-type* tools allow elaborate models for semiconductor devices and are suitable for detailed analysis of power electronic systems but lacks the capability for a power system integration [148]. On the other side, *EMT-type* packages have relatively simple models for semiconductor devices but provide accurate models for transition lines, transformers, etc.

PSCAD/EMTDC (ElectroMagnetic Transients for DC), EMT-type program specifically developed for HVDC [146], offers the best of both worlds, providing a suitable platform for time domain simulation of integrative power electric and electronic systems and is the choice of simulation program in this study.

Subsequent sections of this chapter provide detail on the solution method adopted by this EMT type software and presents techniques that can be incorporated to enhance the computational speed of MMC modeling.

8.2. Solution Method for EMTs

Electrical components in a power system such as a transformer, transmission line, cable are either modeled as lumped RLC element or as distributed RLC elements. Ordinary differential equations describe lumped systems as a function of time alone. While, distributed elements are defined by partial differential equations as a function of time and space. With this representation, dynamics of a power system can be accurately reproduced using the nodal analysis. Nodal analysis based on the Kirchhoff's current law determines the voltage at each node of the system.

Digital nature of computer solution implies that system is resolved in discrete time space and presents a need for numerical integration techniques for the differential equations. Therefore, EMT-type programs utilize the solution method proposed by Dommel [9] which utilizes the trapezoidal rule of integration for the solution of lumped parameters and Bergeron's method for lossless distributed parameters.

8.2.1. Lumped Circuit elements

Lumped elements are described by ordinary differential equations and EMT solver employ numerical integration techniques such as the trapezoidal rule for their solution. Implementation of this solution method on individual capacitor and inductor is presented as follows [146]:

Inductor

$$v_L(t) = L\frac{d}{dt}i_L$$

$$i_L(t) = i_L(t-\Delta t) + \frac{1}{L}\int_{t-\Delta t}^{t} v_L(t)dt$$

$$= i_{H_L}(t-\Delta t) + G_L v_L(t) \qquad (8.1)$$

$$\begin{cases} G_L & = \frac{\Delta t}{2L} \\ i_{H_L}(t-\Delta t) & = i_L(t-\Delta t) \\ & +G_L v_L(t-\Delta t) \end{cases}$$

Capacitor

$$i_C(t) = C\frac{dv_C(t)}{dt}$$

$$v_C(t) = v_C(t-\Delta t) + \frac{1}{C}\int_{t-\Delta t}^{t} i_C dt$$

$$i_C(t) = i_{H_C}(t-\Delta t) + G_C v_C(t) \qquad (8.2)$$

$$\begin{cases} G_C & = \frac{2C}{\Delta t} \\ i_{H_C}(t-\Delta t) & = -i_C(t-\Delta t) \\ & -G_C v_C(t-\Delta t) \end{cases}$$

Based on results of eqs. (8.1) and (8.2), dynamics of inductor and capacitor are approximated by a time varying current source, determined only by present and last time step information, and a constant resistor determined by the time step of the simulation.

Therefore, with this approach dynamics of any lumped parameter in a power system can be approximated by a simple dc circuit as depicted in fig. 8.1, whose parameters are solely determined by the present and historical information from the last time step alone.

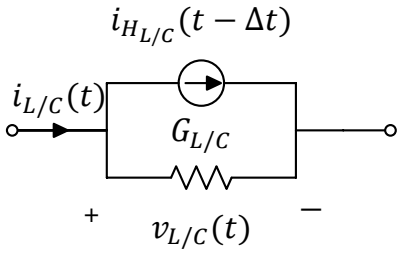


Figure 8.1: EMT Equivalent Representation of lumped elements

8.2.2. Distributed Circuit elements

Distributed circuit elements are described by partial differential equations, as a function of time and space. With an assumption of lossless characteristic, Dommel's solution method ([9]) utilizes Bergeron's Method ([10]) for their exact solution. The implementation of this technique on a distributed model of lossless transmission line is described below [9]:

Voltages and current along a loss-less transmission line, fig. 8.2, are described by:

$$-\frac{\partial i(x,t)}{\partial x} = C'\frac{\partial v(x,t)}{\partial t} \tag{8.3}$$

$$-\frac{\partial v(x,t)}{\partial x} = L'\frac{\partial i(x,t)}{\partial t} \tag{8.4}$$

Their solution yields:

$$v(x,t) = v_+(x-ut) + v_-(x+ut) \tag{8.5}$$

$$i(x,t) = \frac{1}{Z}(v_+(x-ut) - v_-(x+ut)) \tag{8.6}$$

$$\begin{cases} v_+(x-ut)\ ,\ v_-(x+ut) & = \text{Wave propagating in positive and negative direction} \\ u = \frac{1}{\sqrt{L'C'}}\ ,\ Z = \sqrt{\frac{L'}{C}} & = \text{Wave velocity and Surge impedance} \end{cases}$$

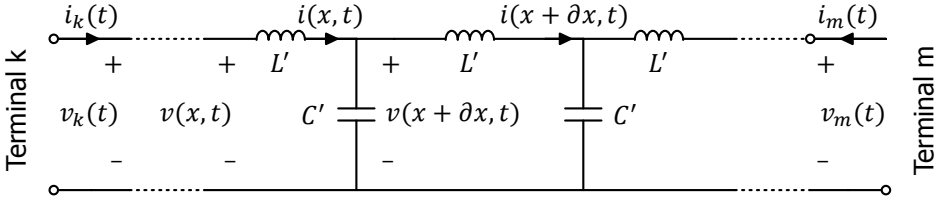


Figure 8.2: Transmission line

Rearranging eqs. (8.5) and (8.6) yields:

$$v_+(x-vt) = \frac{1}{2}(v(x,t) + Zi(x,t)) \tag{8.7}$$

$$v_-(x+vt) = \frac{1}{2}(v(x,t) - Zi(x,t)) \tag{8.8}$$

The wave propagating out from one end at time equal to $t-\tau$ corresponds to the wave reaching the other end at time t, where $\tau = \frac{d}{u}$ corresponds to the travel time along line length d i.e.

$$v_+(0-u(t-\tau)) = v_-(d+ut) \tag{8.9}$$

$$v_-(d+u(t-\tau)) = v_+(0-ut) \tag{8.10}$$

Incorporating eqs. (8.9) and (8.10) in eqs. (8.7) and (8.8) yields:

$$i_k(t) = \frac{1}{Z}v_k(t) + i_{H_k}(t-\tau) \tag{8.11}$$

$$i_m(t) = \frac{1}{Z}v_m(t) + i_{H_m}(t-\tau) \tag{8.12}$$

$$\begin{cases} i_{H_k}(t-\tau) & = -\frac{1}{Z}v_m(t-\tau) - i_m(t-\tau) \\ i_{H_m}(t-\tau) & = -\frac{1}{Z}v_k(t-\tau) - i_k(t-\tau) \end{cases}$$

Therefore, with this approach terminal dynamics of a lossless distributed element in a power system can be precisely determined using a simple dc circuit as depicted in fig. 8.3. The terminal parameters are dictated by present information of the terminal and historical data dating back to the travel time along the element at the other terminal. For lossy distributed elements, lumped resistance is utilized together with this lossless representation [9].

This equivalent representation of distributed elements further leads to topological disconnections in the system [9]. Changes in the system at one end of distributed element only appear on the other end after τ time delay or $\frac{\tau}{\Delta t}$ time steps. This can be exploited in reducing computational load associated with the solution and is further discussed later in this chapter. In addition to Bergeron model PSCAD/EMTDC also provides frequency dependent models that take into account frequency dependence of line/cable parameters.

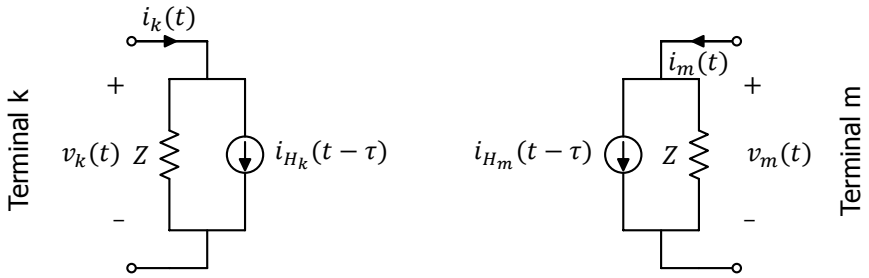


Figure 8.3: Transmission line equivalent representation

In short, with this representation lumped and distributed branches in a network are reduced to time-varying current sources with parallel conductances and using *nodal analyses* are described as [14]:

$$Y_{Br}V_{Br} = I_{H_{Br}} + I_{In_{Br}} \tag{8.13}$$

where $\begin{cases} Y_{Br} & = \text{Branch's Nodal Admittance matrix} \\ V_{Br} & = \text{Branch's node voltages} \\ I_{H_{Br}} & = \text{Time varying Current associated with EMT represenation} \\ I_{In_{Br}} & = \text{Current into the branch} \end{cases}$

Subsequently, this representation can be extended to the entire network, and the power system can be expressed as:

$$Ax(t) = b(t) \tag{8.14}$$

where, $\begin{cases} A & = \text{System Matrix (Admittance)} \\ x & = \text{Unknown variables - Voltages at the nodes} \\ b(t) & = \text{Known variables - History currents \& independent sources} \end{cases}$

For determination of the solution, system variables are initialized at $t = 0$ and linear system of equations i.e. eq. (8.14) is solved to obtain the nodal values at the first time step. This procedure in repeated step by step for every time step with updated history elements and other sources ($b(t)$). The dimension of system matrix (A) corresponds to the number of nodes in the system; hence, bigger the system more is the computational burden in the solution of eq. (8.14).

For power system, admittance matrices are typically sparse, since very few nodes in the network are directly connected to each other. Direct matrix inversion for such systems is not efficient and yields a non-sparse matrix. To exploit the sparsity of system matrix solvers employ optimally ordered LU (lower upper) triangular factorization [150]. This technique yield system matrix as a product of two sparse upper (U) and lower (L) triangular matrices, which offers advantages in storage and computational efficiency [150].

Therefore, solution of eq. (8.14) can be calculated as:

Using matrix inversion:

$$x(t) = A^{-1}b(t) \tag{8.15}$$

Using "LU decomposition":
Decompose A into lower (L) and upper U triangular matrix.

$$LUx(t) = b(t) \tag{8.16}$$

$$\begin{cases} \text{Solve for } z(t)\text{: } Lz(t) & = b(t) \\ \text{Solve for } x(t)\text{: } Ux(t) & = z(t) \end{cases} \tag{8.17}$$

8.3. Power electronics in power system

Power electronic systems are finding increasing application in the power system as HVDC and FACTS systems. Development and design of power converters require different types of studies; these studies can be broadly classified as:

- Component level studies:
  These studies are focused towards electromagnetic transients associated with semiconductor devices and hence require precise and detailed modeled of all elements in the system. The application of these studies includes optimization of component selection to maximize system efficiency, electromagnetic compatibility validation, etc. For these studies, the time range of investigation is on the order of micro to milliseconds.
- System level studies:
  System level studies for HVDC systems are intended at the electromagnetic transients between the converter and the associated AC power system. These studies require in-depth modeling of the converter, control system, and associated power system e.g. nonlinear characteristics of arresters, saturation characteristics of converter transformer [13]. However for such studies, the ac network is confined to a few generators/voltage sources as the focus of the investigation is the converter itself [13]. The applications of these studies include design and validation of control, filter, and protection schemes. For these studies, time-range of investigation is from milliseconds to several seconds.
- Network level studies:
  These studies are focused on dynamic stability studies for the HVDC system within a large ac-network [13]. Electromechanical transients and steady state operation of the converter system are of interest here. These studies include load-flow analyses, design for protections relay, and stability studies for the entire network. For these studies, time-range of investigation is from seconds to several minutes [13].

In comparison to simulation of conventional components of power system, power electronic systems poses various challenges which are contributed to [11, 12, 151]:

- Non-linear characteristics of semiconductor devices.
- Time-varying structure of system due to switching, implying variable system matrix requiring repeated re-triangulation.
- Combination of analog and digital systems.
- Wide range of system time constants.

A wide range of system time constant implies that simulation time step should be sufficiently small, to model accurately small time constants (rapidly changing variable); with adequately large overall simulation time span, to account for large time constants [12]. This implies that simulations are computationally intensive and lead to long execution times.

With the varied objectives for power electronic system studies, traditionally these challenges have been addressed by adopting a hierarchical approach to modeling. That is, based on the objective of study different modeling simplifications can be incorporated into the representation of power electronic system and its components. This hierarchical approach, in general, is split into two broad categories [152]:

- Detailed simulations:
  Detailed models are based on detailed modeling of all system components, providing detailed internal dynamics of the system and are suitable for analyzing the dynamic and transient study of the system.
- Behavior mode simulations:
  They analyze the system level aspects e.g. harmonic content, resonant frequencies, voltage and current distortion associated with the nominal operation of the power electronic device. This study can be realized using a simplified representation of the system, that is based on the input-output relation of the system and are computationally efficient.

8.3.1. Challenges with power electronic simulation

Modeling of semi-conductor devices

Semiconductor devices include diodes, thyristor, IGBTs. The operation of these devices is dictated by external control signals (if any) and current/voltages in the system. These devices have non-linear characteristics, and their operation modifies the topology of the system which requires re-calculation of system matrix and its re-triangulation.

Semiconductor devices can be precisely represented using full physics based models; however for power system studies, such detailed representation for switching transients is of little interest. Therefore, for simulation semiconductors can be represented by simplified representations as detailed below [151, 153]:

- In most modeling methods ideal characteristics for semiconductor devices are assumed i.e. during on-state voltage drop across the switch is zero and during off-state current through the switch is zero. This effect can be incorporated in the system matrix by:
  - Ideal Representation
    Here a semiconductor device is modeled as an ideal switch i.e. infinite resistance or zero current through the device under OFF state and zero resistance or zero voltage drop under ON conditions. This representation is realized by creating and collapsing nodes of the semiconductor device, which in turn changes the dimensions of the system matrix [151]. EMTP utilizes this representation for ideal modeling of semiconductor devices [153].
  - Piece-wise Linear Representation
    Here semiconductor devices are modeled as a bi-value (ON/OFF) resistor which's

value toggles between high and low resistance depending on the state of the device. This approach maintains the dimensions of the system matrix.

- The switching operation can also be modeled by a voltage source between the terminals with zero V or diode drop during ON operation and as a current source with $0A$ during OFF operation. This method maintains the number of nodes and hence the size of the system matrix.

- Compensation Method
  Compensation method as introduced in [154] is used for modeling of nonlinear and time-varying elements e.g. circuit breakers, lightning arrester. With this approach, nonlinear or time-varying elements are modeled as a variable current source. Thevenin equivalence of the linear part of the network is utilized to determine the current in nonlinear/time varying element, either by a simultaneous solution with the piece-wise definition of the element or an iterative approach e.g. Newton-Raphson on the nonlinear analytic relation for the element.

  Semiconductor devices can be accurately modeled with their nonlinear characteristic, and hence compensation method can be utilized for modeling of semiconductor devices.

Variable system matrix

With the operation of a semiconductor device, system matrix is no longer constant and present a need for re-triangulation of the system matrix. This time-varying topology of the system coupled with the frequent nature of switching in converters makes simulation very computationally intensive. To counter the computational load various techniques can be utilized such as [155]:

- Partial LU factorization:
  With partial LU factorization through optimal ordering, the portion of the system with changing topology is repeatedly re-triangularized upon a switching operation; while the remaining system (i.e. without switches) maintains its triangularized matrix [153, 156]. However, for cases where a system has a large number of switches e.g. HVDC converter, complete re-triangulation of the system matrix tends to be more efficient [153, 157].

- Pre-calculation of inverse/LU factors:
  In this technique, inverse/LU factors for system matrix for all possible network configurations are pre-calculated. This approach, especially for power converter systems, utilizes extensive memory.

- Disconnected sub-networks:
  This method of disconnection and sub-networking is proposed by Woodford et al. ([158]) for line commutated converters. This modeling approach disconnects power electronic converter from the system and separately models its operation. The interface between converter's sub-network and ac/dc side of the network is modeled as two nonlinear elements for ac and dc sides. AC voltage and dc current are assumed to be predictable and continuous; while the solution of the

converter's sub-network based on EMT equivalent representation of switches and other components yields current injection in the ac network and voltage on the dc-side as illustrated in fig. 8.4 [158]. However for accurate prediction, this method requires small time step.

Mahseredjian et al. ([157]) extends the compensation method, as discussed earlier for nonlinear circuit elements, to determine the two sets of nonlinear elements using an iterative approach in this disconnected sub-network representation.

- Network partitioning and parallel computation methods:
  The objective of network partitioning is to exploit computational efficiency of the simultaneous solution of a group of relatively small matrix equation as compared to a single large matrix.

  This can be accomplished as follows:

  – Lossless transmission lines lead to the decoupling of the connected system. Therefore, they can be utilized to divide a large into subsystems that can be solved independently.

  – Diakoptics method offers a computationally efficient parallel solution for large sparse systems. Such a method based on node splitting has been proposed in [155].

  – Nested fast and simultaneous solution method as discussed in [14], offer a computationally efficient solution method for large systems by employing the Thevenin or Norton equivalence to subsystems.

PSCAD/EMTDC employs partial LU factorization with optimal ordering. Network branches with switching components are ordered at the bottom of the system matrix and in the case of a switching event system matrix below the node corresponding to smallest node number connected to the switched branch are re-triangularized [146]. Moreover, PSCAD allows splitting of a network into subsystem by use of distributed transmission line or cables [159].

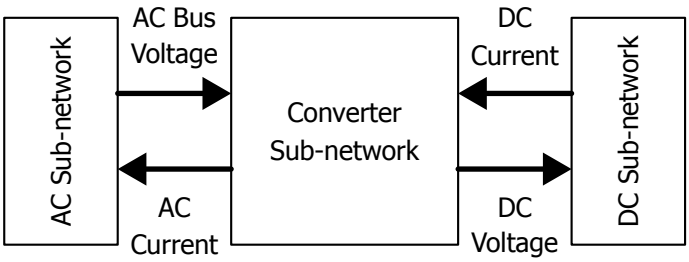


Figure 8.4: Network Splitting

Out of step switching

For semiconductor devices, the state of conduction is dependent on the voltage across and current through them in addition to gate signals. With fixed simulation time-step there is a possibility of out of step switching. Figure 8.5 illustrates the case where current through a diode drops to zero between time t and $t + \Delta t$. Without correction for out of step switching, the solution inaccurately shows the flow of negative current through the diode and moreover leads to spikes and numerical oscillations of voltages and currents in the system [146].

The effects of out of step switching on the solution can be either mitigated by reducing time step or using a detailed representation for the semiconductors that capture the gradual change of device's resistance or can be eliminated by tracking the exact instant of commutation through the use of variable time step or interpolation algorithms.

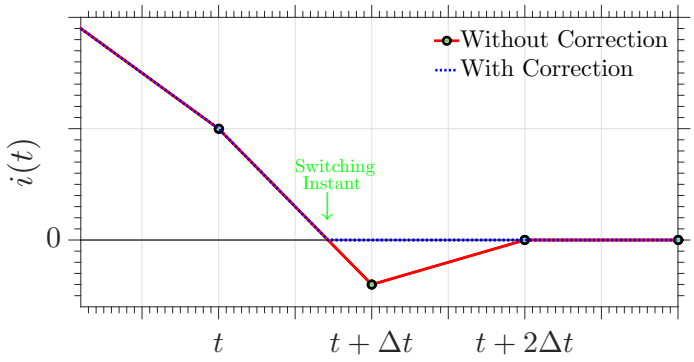


Figure 8.5: Out of step switching (diode)

PSCAD/EMTDC uses the interpolation method to track the switching instances precisely [159]. Solver monitors the state of the switches based on switching signals, voltages, and currents in the system. In the case of a change in a state of a switch the solver interpolates back to the instance of switch operation. The system matrix is updated and is resolved. Additional interpolation/extrapolation are incorporated to re-synchronize to the original time step grids as illustrated in fig. 8.6. Compared to other techniques this method is accurate and computationally efficient [159].

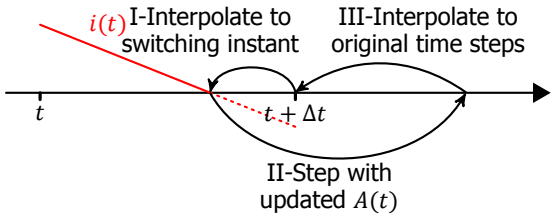


Figure 8.6: Out of step switching: Interpolation method

Numerical oscillation

Even with on-step switching, truncation error of trapezoidal rule can lead to numerical oscillations in the solution. Examples include breaking of inductive currents that lead to oscillation in inductors' voltage or oscillation in capacitor current after voltage connection [160].

This is explained with a case where a switch interrupts currents through an inductor [146]. From eq. (8.1) voltage across inductor using trapezoidal rule is given as:

$$v_L(t) = \frac{2L}{\Delta t}(i_L(t) - i_L(t - \Delta t)) - v_L(t - \Delta t) \tag{8.18}$$

With switch operation at current zero:

$$v_L(t) = -v_L(t - \Delta t) \tag{8.19}$$

This leads to sustained oscillations in inductor voltage. These oscillations do not represent electrical behavior but occur due to approximation in trapezoidal integration method.

These oscillations can be forced to decay by an addition of damping resistor or avoided by use of "critical damping adjustment algorithm" [160] (where the solver switches to the backward-Euler method of integration), interpolation or by use of root-matching modeling techniques [146]. PSCAD/EMTD utilizes half time step interpolation to mitigate chatter [159]. This approach upon detection of chatter interpolates half time step backward followed by a normal time step and then interpolates back to the original time step as illustrated in fig. 8.7 [146].

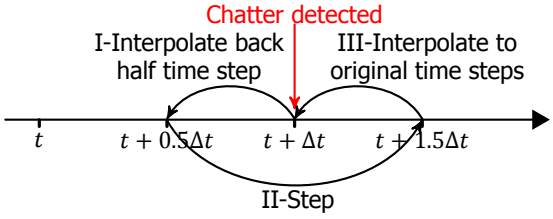


Figure 8.7: Chatter: Interpolation method

8.3.2. Flow Chart of EMT solver

The simplified algorithm for the EMT solver is depicted in fig. 8.8.

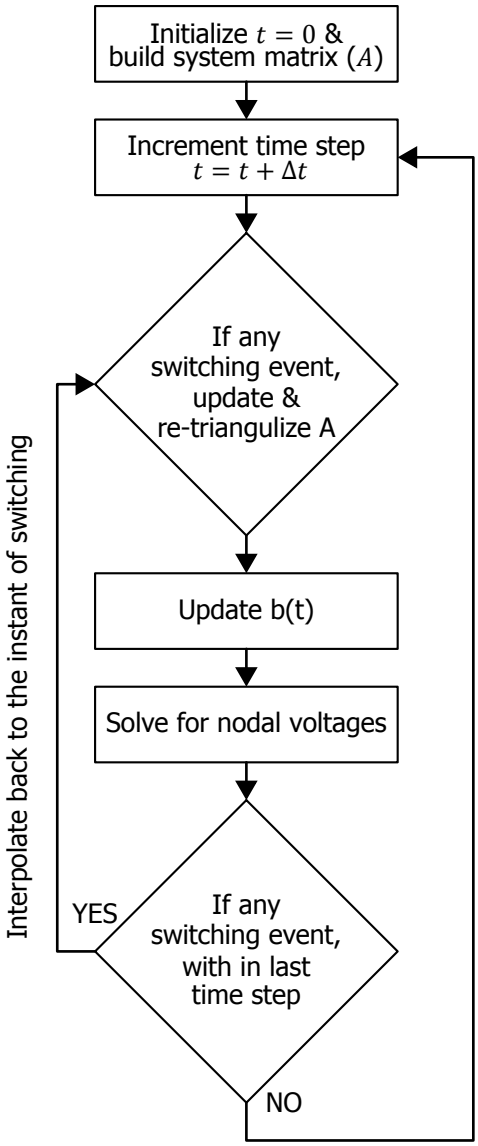


Figure 8.8: EMT solution flow chart

8.4. EMT Solution acceleration methods

Topological disconnections or presence of lossless lines as seen in section 8.2.2 leads to an inherent splitting of networks into subsystems. This can be exploited to minimize dimensions of system matrix leading to higher storage efficiency and increased computational speed. For example, memory storage of system matrix of a system with $10,000$ nodes is 100×10^6 which can be reduced to 20×10^6 by splitting the system into five sub-systems [146] and matrix operations tends to become more computationally efficient with this splitting.

Besides these inherent disconnections, mathematical techniques can be utilized for faster solution of eq. (8.14). The essence of these methods is partitioning of the system into smaller subsystems and solving for these sub-systems individually. These methods include:

- Diakoptics method.
  Diakoptics is a method of solution of linear equations [161]. In this approach, the system is split into smaller subsystem and algebraic manipulations with their independent solution yield the system solution. Large system matrix in network solution with high sparsity and concentration of non-zero near diagonal tends to benefit from this solution approach [161]. The steps for this solution method are summarized as [161]:

  1. Subsystems are solved independently.
  2. Subsystem solutions are combined to yield exact solution of the entire unified system

- Nested Fast and simultaneous method.
  This solution method as proposed by Strunz and Carlson ([14]) splits system into subsystems similar to diakoptics method. However, the solution method involves "generation of electric network equivalents" for subsystems and hierarchization of simulation as parent and child simulations. The steps for this solution method are summarized as:

  1. Parent simulation using nodal analyses and Norton's equivalent of subsystems determines the terminal voltage of child subsystems.
  2. Using these terminal voltages as input, child simulation simultaneously solve sub-systems based on desired solution method e.g. nodal or state space method.
  3. Based on the child simulation solution, sub-systems Norton's equivalent for the parent simulation is updated, and procedure is reiterated for the next time step.

  This approach increases the number of steps in simulation however with reduced dimensions of matrices this simulation approach offers a computational advantage for large systems.

The computational effectiveness of these solution methods is evident with the help of the following examples.

Consider a large system which can be partitioned into g sub-systems as illustrated in fig. 8.9. The system can be represented as:

$$AX = B \tag{8.20}$$

$$\begin{bmatrix} [A_{11}] & [A_{12}] & \cdots & \cdots \\ [A_{21}] & [A_{22}] & \cdots & \cdots \\ \vdots & \vdots & \ddots & \cdots \\ \cdots & \cdots & \cdots & [A_{gg}] \end{bmatrix} \begin{bmatrix} [X_1] \\ [X_2] \\ \vdots \\ [X_g] \end{bmatrix} = \begin{bmatrix} [B_1] \\ [B_2] \\ \vdots \\ [B_g] \end{bmatrix} \tag{8.21}$$

$$\text{Where} \begin{cases} [A_{ii}] & \text{Admittance matrix for subsystem } i \\ [A_{ij}](i \neq j) & \text{Admittance matrix for interconnections} \\ [X_i] & \text{Vector for unknown voltage} \\ [B_i] & \text{Vector for history and other current sources} \end{cases} \tag{8.22}$$

- Direct Solution:
  With this method, the solution requires triangulation of the whole system matrix i.e. $(N) \times (N)$ order matrix.

  The presence of lossless transmission line implies decoupling of the systems in the ends of lines. That is system matrix A can be represented as:

$$\begin{bmatrix} [A_{aa}] & [0] \\ [0] & [A_{bb}] \end{bmatrix} \tag{8.23}$$

  With this case triangulation can is to be performed on two matrices with sizes $(N_{aa} \times N_{aa})$ and $(N_{bb} \times N_{bb})$.

  This is more computationally efficient since:

$$N_{aa} \times N_{aa} + N_{bb} \times N_{bb} \ll (N_{aa} + N_{bb}) \times (N_{aa} + N_{bb}) \tag{8.24}$$

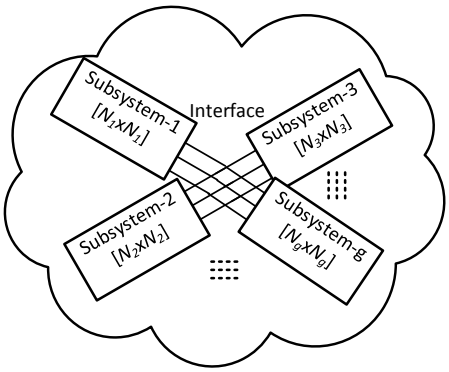


Figure 8.9: System Partitioning

- Diakoptics [161]:
  With this solution method system matrix is split into two matrices i.e.

$$A = \underline{A} + \overline{A} \tag{8.25}$$

where,

$$\begin{cases} \underline{A} \text{ is block diagonal matrix for subsytems} & = \begin{bmatrix} [A_{11}] & [0] & \cdots & \cdots \\ [0] & [A_{22}] & \cdots & \cdots \\ \vdots & \vdots & \ddots & \cdots \\ \cdots & \cdots & \cdots & [A_{gg}] \end{bmatrix} \\ \overline{A} \text{ is matrix for interconnections} & = \begin{bmatrix} [0] & [A_{12}] & \cdots & \cdots \\ [A_{21}] & [0] & \cdots & \cdots \\ \vdots & \vdots & \ddots & \cdots \\ \cdots & \cdots & \cdots & [\ 0\ ] \end{bmatrix} \end{cases} \tag{8.26}$$

Equations (8.20) and (8.25) yields:

$$\underline{A}X + \overline{A}X = B \tag{8.27}$$

$$\sum_{k=1}^{N} \underline{a}_{jk} x_k + \sum_{k=1}^{N} \overline{a}_{jk} x_k = b_j \tag{8.28}$$

Replace $\overline{a}_{jk} x_k$ where $a_{jk} \neq 0$ by a new variable y_i. This yield d new set of linear equations i.e.

$$C_x X = DY \tag{8.29}$$

$$\text{Where} \begin{cases} C_x & = \text{Zero-unit matrix of size } d \times n \\ D & = \text{Diagonal matrix of of size } d \times d \text{ with coefficients } \frac{1}{\overline{a}_{jk}} \\ Y & = \text{column matrix for } d \text{ new variables} \end{cases} \tag{8.30}$$

Using these results:

$$\overline{A}X = C_y Y \tag{8.31}$$

$$\text{Where } \{C_y \quad = \text{Zero-unit matrix of size } n \times d \tag{8.32}$$

Therefore our system of N equation with N unknowns in eq. (8.27) is now represented by $N + d$ equation with $N + d$ variables:

$$\underline{A}X + C_y Y = B \tag{8.33}$$

$$C_x X = DY \tag{8.34}$$

This apparently increases the complexity of the problem as now we have to solve for d more variable.

Rearranging and substituting eqs. (8.33) and (8.34) yields [161]:

$$X = \underline{A}^{-1}B + \overline{D}B \tag{8.35}$$

$$\text{where } \overline{D} = -\underline{A}^{-1}C_y(D + C_x\underline{A}^{-1}C_y)^{-1}C_x\underline{A}^{-1} \tag{8.36}$$

Therefore system eq. (8.20) can be solved using eqs. (8.35) and (8.36). This method involves:

1. Computation of $\underline{A}^{-1}B$ i.e. independent solution of g subsystem that requires triangulation of $[A_{11}], [A_{22}], \cdots, [A_{gg}]]$. The smaller dimensions of these subsystems make matrix operations computationally efficient.
2. Computation of $\overline{D}B$. This involves inversion of $(D + C_x\underline{A}^{-1}C_y)$ order d.

This solution method is particular effective for large systems which can be split into subsystems with few interconnections i.e. lower value of d.

- Nested fast and simultaneous solution method [14]:
  With this solution method as detailed in [14]; in first step "Parent simulation" determines voltages at terminals/interconnections of subsystem i.e.

$$A^{\cap}X^{\cap} = B^{\cap} \tag{8.37}$$

Using the terminal voltages from solution of eq. (8.37), each subsystem is solved by "child simulations" as:

$$[A_{ii}]X_i = B_i - [A_{ik}]X_{ik}^{\cap} \tag{8.38}$$

Based on the results of eq. (8.38) for all sub-systems $A^{\cap}$ is updated in case of a change in topology of any subsystem and next time step is iterated with updated $B^{\cap}$ from sub-systems and other sources.

Furthermore, with these methods in power electronics simulation re-triangulation of matrices and other interpolation handling operations due to switching are performed only on the individual subsystem's matrix rather than the whole system, which offers a tremendous computational advantage for frequent switching systems such as power converters [146, 159].

PSCAD edition allows for subsystem splitting using distributed transmission line or cable connection. However, direct implementation of "diakoptics" and "nested fast and simulations solution methods" in PSCAD requires changes in the solver algorithm, which is not accessible to the user.

Nevertheless, these partitioning schemes can be mimicked by utilizing system equivalents based on these methods in the simulation environment e.g. modeling of a subsystem with its Thevenin or Norton equivalence rather than discrete elements. This solution with multiple smaller matrices or by linear equations rather than one large system matrix offers higher computationally efficiency without loss of accuracy.

8.5. EMT Modeling of MMC

For line commutated and classical voltage source converts, the system comprises of a large number of semiconductor devices. However, all series-connected semiconductor devices in an arm operate simultaneously and for purposes of modeling behave as a single semiconductor device. Therefore, despite the added computational burden of repetitive re-triangulation of system matrix, detailed models for these converters are easily handled by modern computers.

On the other hand, MMC comprises of a large number of sub-modules (in order of hundreds) that operate independently. Independent operation of these sub-modules implies that the system has a large number of semiconductor devices and nodes. With N half bridge sub-modules per arm, the system matrix for converter alone is of $(12N + 5) \times (12N + 5)$ size, there are $12N$ IGBTs and $12N$ diodes. In a case of full bridge sub-modules, the number of IGBTs and diodes increase by a factor of two. In addition to this effective switching frequency is around $2Nf_{sw}$ for a phase leg [80]. Therefore, simulation of MMC as compared to LCC and classical VSC present an enormous computational burden and pose a need for intelligent modeling techniques.

As discussed earlier studies for power electronic system have various objectives which are accomplished by detailed and behavioral simulations. Similarly for MMCs, although a very detailed model can perform all of the studies; huge computational load associated with detailed modeling of MMC needs a smarter approach. This can be achieved by optimally developing the complexity of model based on the requirements of the study with an acceptable computational burden, without losing any relevant information for that particular study.

Therefore, this study based on the representation of semiconductor devices, modeling of sub-modules/arms and simplification of control systems, categories MMC models into various levels. These models can be utilized for their respective studies of converter without loss of any relevant information. This hierarchization of models is listed as follows and details on each representation follow in the coming sections.

- Detailed models
  - Full Physics based models.
  - Detailed IGBT models
- Behavioral models
  - Ideal Model
    - Detailed ideal model
    - Isolated submodule model
    - Thevenin's equivalent Model
  - Switching Function Model
  - Average value model

8.6. Detailed Models

In these models, simulation circuit is built to mimic the topology of the original system. Non-linear characteristics of semiconductor devices (IGBTs and diodes) and parasitic circuit elements are accurately represented here. Based on the representation of semiconductors detailed models are categorized as:

8.6.1. T-I Full Physics based models (CIGRE WB B4-57 Type-1 [162])

In these models semiconductor devices (IGBTs and diodes) are accurately modeled by differential equations or equivalent circuits. This model is the only representation that can accurately assess the switching losses. These models require integration time step in order of nanoseconds [32] and are therefore computationally very expensive; rendering them unsuitable for power system simulations. Based on this representation an individual IGBT is represented as illustrated in fig. 8.10.

8.6.2. T-II Detailed IGBT models (CIGRE WB B4-57 Type-2 [162])

In this representation, non-linear characteristics of semiconductor switches are modeled externally. IGBTs are modeled as an ideal switch together with a series, anti-parallel non-ideal diode and a snubber circuit as illustrated in fig. 8.11 [33]. The diodes mimic the non-linear VI characteristics of a switch and are modeled using classical diode function based on measurements on device or manufacture's data sheet. This model takes into account conduction losses in the system, blocked state of sub-module and internal faults [32].

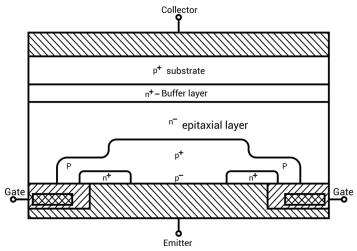


Figure 8.10: IGBT full Physics model [163]

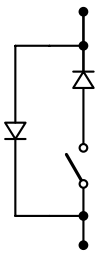


Figure 8.11: Detailed IGBT model

Conclusion Detailed models are the next best thing than to prototype setups and provide the highest accuracy among all simulation models. These models subject to the accuracy of semiconductor representation, provide precise analyses of switching characteristics (i.e. transients associated with switching, turn on, reverse recovery of semiconductor devices), losses in the system and parasitic effects [152, 164]. These models find application in various component level studies e.g.:

- Optimization of component selection to maximize system efficiency.
- Electromagnetic compatibility studies.
- Simulation of transients within switching process.
- Validation of simplified models.

8.7. Behavioral mode simulations

Detailed model with exhaustive representation for semiconductor devices reproduce transients within switching events with high precision. However, these models are plagued by an excessive computational load. Furthermore, for studies at system and network level detailed representation of semiconductor devices is of little added value. Therefore, this presents a need for simplified behavioral models.

Behavioral modeling approach at the expense of accuracy, neglect detailed characteristics of switching events and instead model them as an instantaneous transition by utilizing idealized representations. Based on the representation of semiconductor devices and the solution method simplified models are categorized as follows.

8.7.1. Bi-value resistor Model

This modeling approach utilizes bi-value resistor representation for semiconductor devices i.e. small resistance during their conduction phase and as high resistance when off. According to the manufacturer's data sheets [165], typical values for the on-state resistance of high voltage IGBTs is in order of $m\Omega$ ($\approx 2.5m\Omega$ [166]) and off state resistance in the order of $M\Omega$ ($\approx 82.5M\Omega$ [166]).

Based on this bi-value resistor representation, an IGBT and its freewheeling diode can be illustrated as fig. 8.12 and equivalent resistance is calculated as:

$$R_{eq} = \begin{cases} R_{IGBT_{ON}} \,||R_{Diode_{OFF}} & \text{IGBT ON, Diode OFF} \\ R_{Diode_{ON}}||R_{IGBT_{OFF}} & \text{IGBT OFF, Diode ON} \\ R_{IGBT_{OFF}}||R_{Diode_{OFF}} & \text{IGBT OFF, Diode OFF} \end{cases} \tag{8.39}$$

Where operating states of IGBT is determined by the gate signal, voltage, and current direction; the voltage across the diode and current direction determines its state.

This finite resistance representation of valves keeps the voltages/currents in the system finite, and the intermediate circuit is solvable [152]. It enables system modeling by linear equations, which reduces computational burden and mitigate the convergence problems [152]. Moreover, this modeling approach is suitable for simulation of the large-signal behavior of the system and the functionality of the faster inner control loops [164].

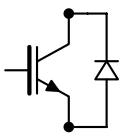


Figure 8.12: IGBT and Diode

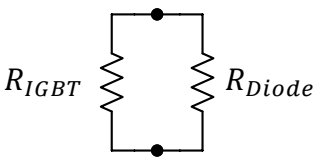


Figure 8.13: Bi-value resistor model

For MMC based on this representation of valves, models are further sub-categorized into three types as detailed in following section, which is based on simplification introduced on sub-modules/arm using Thevenin's/Norton's equivalence.

T-III Detailed Ideal Model

(CIGRE WB B4-57 model Type-3 [162])

In this modeling approach similar to the "detailed models", simulation circuit is built to mimic the topology of the system under investigation. However, here bi-value resistor model is utilized for representation of semiconductor device. This model is implemented in the simulation program by constructing the entire converter topology by discrete elements.

Following description details the construction of system matrix and solution method for an individual arm of an MMC in an EMT solver. This mathematical detail serves to develop the understanding of the EMT program's solution method and is further utilized in the development of simplified models for the converter.

Using the equivalent representation for valves (eq. (8.39)) and EMT equivalent representation of a capacitor fig. 8.1, a half bridge sub-module fig. 3.3 can be simplified as fig. 8.14 and subsequently to fig. 8.15 using the source transformation. Equation (8.40) gives the parameters for this equivalent representation of the SM. The resistance of an individual valve (IGBT & freewheeling diode) is dictated by gating signal, the voltage across and current through it. Therefore, this representation simulates all states of SM operation i.e. inserted, bypassed and blocked.

$$\begin{cases} G_{cEQ} & = \frac{2C}{\Delta t} \\ i_c(t) & = i_{cEQ}(t-\Delta) + G_{cEQ} V_c(t) \\ i_{cEQ}(t-\Delta t) & = -i_c(t-\Delta t) - G_{cEQ} V_c(t-\Delta t) \\ & \\ R_{cEQ} & = \frac{\Delta t}{2C} \\ v_c(t) & = R_{cEQ} i_c(t) + v_{cEQ}(t-\Delta t) \\ v_{cEQ}(t-\Delta t) & = R_{cEQ} i_c(t-\Delta t) + v_c(t-\Delta t) \\ & \\ G_{T1}(t)\ \&\ G_{T1}(t) & \text{Given by eq. (8.39) based on gating signal, voltage across and current in IGBT \& diode.} \end{cases} \tag{8.40}$$

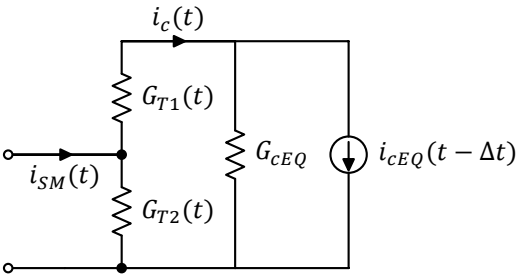


Figure 8.14: SM's Equivalent representation

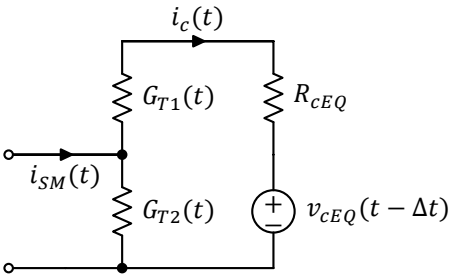


Figure 8.15: SM's Equivalent representation

An arm comprises a series connection of N sub-modules and an arm reactor. Using the representation of fig. 8.14 for a sub-module, the equivalent circuit of an arm is shown in fig. 8.16.

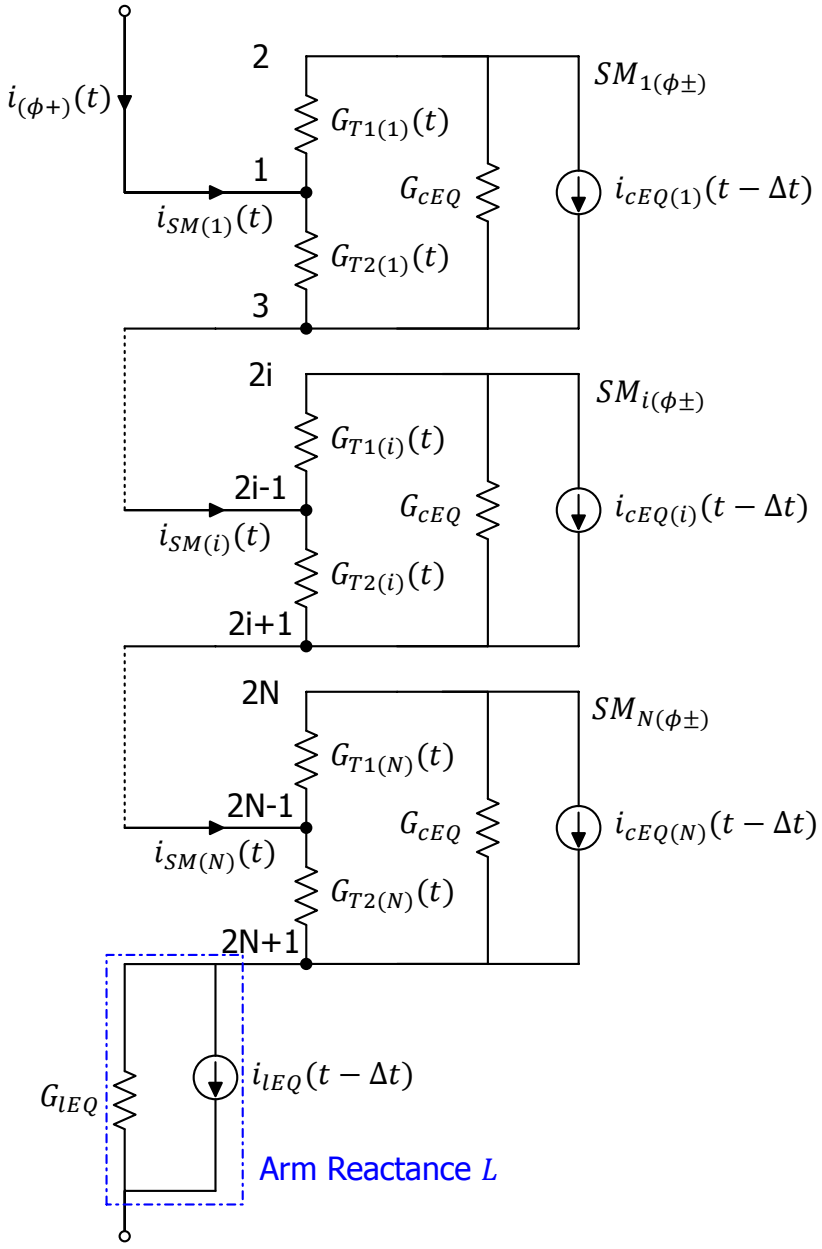


Figure 8.16: Equivalent Representation for an arm

The figure illustrates that an arm has $2N+2$ nodes. Using nodal analysis, EMT solver constructs system matrix for the system. Therefore, for the single arm system equation is given as:

$$A(t)X(t) = B(t) \tag{8.41}$$

where,

$$X(t) = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ \vdots \\ v_{2i-1} \\ v_{2i} \\ v_{2i+1} \\ \vdots \\ v_{2N-1} \\ v_{2N} \\ v_{2N+1} \\ v_{2N+2} \end{bmatrix} \text{ \& } B(t) = \begin{bmatrix} i_{(\phi+)} \\ -i_{cEQ(1)} \\ i_{cEQ(1)} \\ -i_{cEQ(2)} \\ \vdots \\ i_{cEQ(i-1)} \\ -i_{cEQ(i)} \\ i_{cEQ(i)} \\ \vdots \\ i_{cEQ(N-1)} \\ -i_{cEQ(N)} \\ i_{cEQ(N)} - i_{lEQ} \\ i_{lEQ} - i_{\phi+} \end{bmatrix} \tag{8.42}$$

$$A(t) = \begin{bmatrix} a_{11} & a_{12} & a_{13} & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 \\ a_{21} & a_{22} & a_{23} & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \\ 0 & 0 & a_{43} & a_{44} & a_{45} & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \\ 0 & 0 & a_{53} & a_{54} & \ddots & & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & & \ddots & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \\ \vdots & \vdots & \cdots & \cdots & a_{(2i-1)(2i-3)} & a_{(2i-1)(2i-2)} & a_{(2i-1)(2i-1)} & a_{(2i-1)(2i)} & a_{(2i-1)(2i+1)} & \vdots & \vdots & \\ \vdots & \vdots & \cdots & \cdots & 0 & 0 & a_{2i(2i-1)} & a_{2i(2i)} & a_{2i(2i+1)} & \vdots & \vdots & \vdots \\ \vdots & \vdots & \cdots & \cdots & 0 & 0 & a_{(2i+1)(2i-1)} & a_{(2i+1)(2i)} & \ddots & & \vdots & \\ \vdots & \vdots & \cdots & \cdots & \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \vdots & \vdots & \cdots & \cdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & \cdots & \cdots & \cdots & \cdots & a_{(2N-1)(2N-3)} & a_{(2N-1)(2N-2)} & a_{(2N-1)(2N-1)} & a_{(2N-1)(2N)} & a_{(2N-1)(2N+1)} & 0 \\ 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & 0 & a_{(2N)(2N-1)} & a_{(2N)(2N)} & a_{(2N)(2N+1)} & 0 \\ 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & 0 & a_{(2N+1)(2N-1)} & a_{(2N+1)(2N)} & a_{(2N+1)(2N+1)} & a_{(2N+1)(2N+2)} \\ 0 & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & 0 & 0 & 0 & a_{(2N+2)(2N+1)} & a_{(2N+2)(2N+2)} \end{bmatrix} \tag{8.43}$$

where $A(t)$ symmetric and indices a_{kj} for lower triangle ($k \geq j$) are given as

$$a_{kj} = \begin{cases} G_{T1(i)} + G_{cEQ(i)} & \text{where, } k = j = 2i \\ G_{T2(i-1)} + G_{T1(i+1)} + G_{T2(i+1)} + G_{cEQ(i-1)} & \text{where, } k = j = 2i-1 \\ -G_{T1(i)} & \text{where, } k = 2i \text{ \& } j = 2i-1 \\ -G_{cEQ(i)} & \text{where, } k = 2i+1 \text{ \& } j = 2i \\ -G_{T2(i)} & \text{where, } k = 2i+1 \text{ \& } j = 2i-1 \\ 0 & \text{for all other indices} \end{cases}$$

where, $\{i \in \mathbb{Z} \wedge i \geq 1 \wedge i \leq N\}$ & $k \geq j$

$$\text{Except, } \begin{cases} a_{11} & = G_{T1(1)} + G_{T2(1)} \\ a_{(2N+1)(2N+1)} & = G_{T2(N)} + G_{cEQ(N)} + G_{lEQ} \\ a_{(2N+1)(2N+2)} & = -G_{lEQ} \\ a_{(2N+2)(2N+2)} & = G_{lEQ} \end{cases}$$

With the construction of this matrix, the solver determines historical currents and solves for the solution step by step. The sparsity (i.e. number of zero elements) of system matrix A from eq. (8.43) is also visible as most of the element in the matrix are zero. Sparsity is given by:

$$s = \left(1 - \frac{8N + 4}{(2N + 2)^2}\right) 100 \tag{8.44}$$

With $N = 100$, 98% of entries in matrix A are zero. By use of LU decomposition and proper ordering of system matrix, the sparsity of matrix is exploited by the solver.

Conclusion Detailed ideal model preserves the circuit configuration of the MMC and simultaneously solves the entire system using nodal analysis. The only difference between this model and detailed model is the representation of semiconductor devices. In this modeling scheme, an individual arm is mathematically represented by a nodal admittance matrix of dimension $2N + 2\ by\ 2N + 2$.

This model finds application in various system and network level studies such as:

- Simulation of external and internal faults.
- Design and validation of arm and module modulation schemes.
- Design and validation of controls.
- Validation of simplified models.

However, despite simpler representation for semiconductor devices, frequent switching implies repetitive re-triangulation and interpolations of the entire system. This tends to make this model computationally expensive and presents a need for computationally efficient models.

T-IV Isolated sub-module model

Isolated sub-module model (ISM), as proposed by Xu et al.([25]) is identical to the *T-III detailed Ideal model* but based on the concept of "nested fast and simultaneous solution method" models each sub-module as a separate subsystem with its individual system matrix.

All submodules in an arm experience the same current, while arm currents and the state of switches determine the internal dynamics of the submodules [25]. Whereas, the operation of an arm corresponds to a variable voltage source. Based on these principles, this modeling scheme represents individual SMs as an isolated system, and models interconnection with arm via dependent current and voltage sources. A dependent current source in each sub-module mimics its interconnection with arm and all SMs in an arm are replaced by a dependent voltage source, corresponding to the cumulative voltage across all sub-modules, i.e. eq. (8.45). Figure 8.17 further elaborates on this modeling scheme.

$$v_{arm_{(\phi\pm)}}(t) = \sum_{i=1}^{N} v_{sm_{i(\phi\pm)}}(t) \tag{8.45}$$

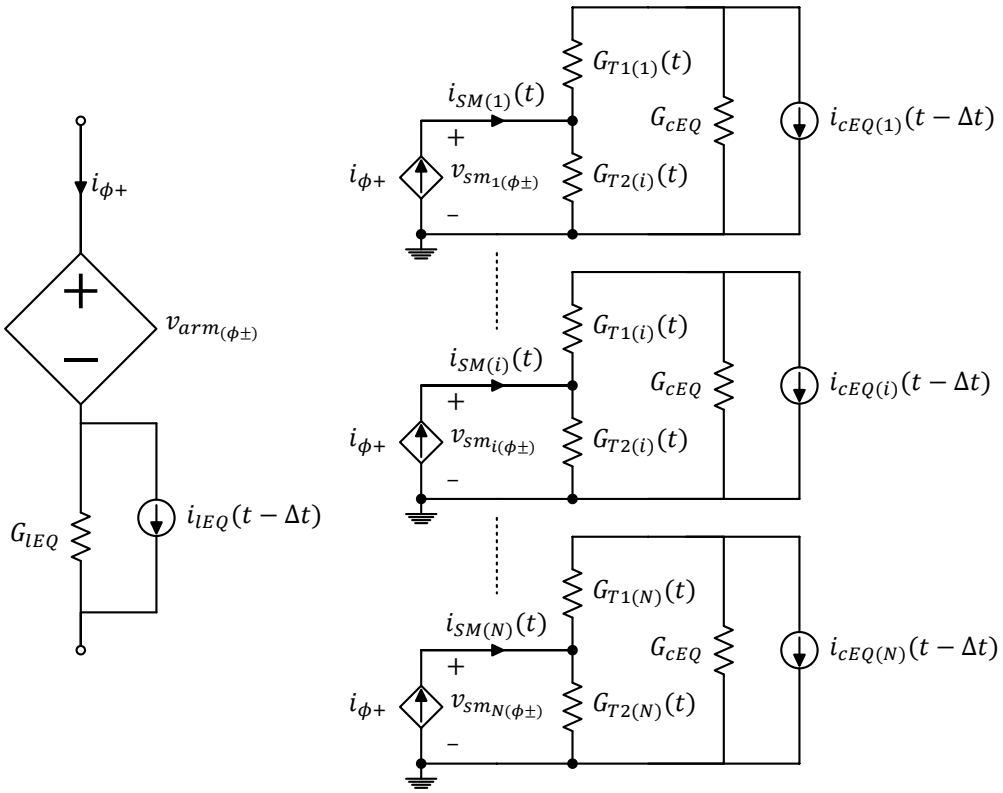


Figure 8.17: ISM - Equivalent Representation for an arm

With this representation, the solver instead of constructing a single large system matrix (eq. (8.41)) constructs N+1 matrices for N submodules and the converter overall. Thereby re-triangulation and interpolation are only applied to respective subsystem's matrix in case of a switching event. This isolated representation for individual sub-module offers computational advantages of solving numerous small matrices over one large matrix as discussed earlier. On the downside, this coupling with dependent sources leads to one-time step delay between the sub-module subsystem and the arm equivalent subsystem. However, continuous nature of current in MMC and a very small step in the account of high effective switching frequency makes the effect of this artificial delay negligible.

Conclusion The isolated submodule model utilizes dependent current and voltage sources to mimic the coupling of converter arm and an individual sub-module. In this modeling scheme, an individual arm is mathematically represented by $N+1$ nodal admittance matrices of dimension $2\ by\ 2$ each.

Separate system matrix for each sub-module provides higher computationally efficient. This representation leads to an artificial delay between a change in arm current and its effect in sub-modules and similarly a change in submodule voltage and its impact in the converter arm. Nevertheless, continuous nature of arm currents and a small simulation time step makes this effect negligible.

This model provide all details for converter and similar to detailed ideal model finds application in various system and network level studies such as:

- Simulation of external and internal faults.
- Design and validation of arm and module modulation schemes.
- Design and validation of controls.
- Validation of simplified models.

T-V Equivalent ideal model

This model as proposed by Gnanarathna et al. ([15]) is similar to T-III,IV regarding the modeling of components. However, this modeling technique takes T-IV's abstraction of sub-modules as an individual subsystem to the next level, and based on "nested fast and simultaneous solution method" employs Thevenin/Norton equivalence to all sub-modules in an arm and models them as a single subsystem.

In this modeling method, for the *inserted* and *bypassed* state, the valve (IGBT and its anti-parallel diode) as a single bi-value resistor. Furthermore, in this representation the gate signals exclusively determine the operation of the valve; unlike the multi-value representation in eq. (8.39) where the state of the valve is also dependent on the associated voltages and currents.

$$R_{eq} = \begin{cases} R_{ON} & \text{if IGBT is ON} \\ R_{OFF} & \text{if IGBT is OFF} \end{cases} \tag{8.46}$$

With this simplified representation of a valve and using submodules EMT equivalent representation fig. 8.15, Thevenin's equivalent of a submodule is derived as eq. (8.47) which is illustrated in fig. 8.18.

$$v_{SM}(t) = R_{SM_{eq}} i_{SM}(t) + v_{SM_{eq}}(t - \Delta t) \tag{8.47}$$

$$\begin{cases} R_{SM_{eq}} & = \dfrac{R_{T_2}(t)(R_{T_1}(t) + R_{cEQ})}{R_{T_2}(t) + R_{T_1}(t) + R_{cEQ}} \\ v_{SM_{eq}}(t - \Delta t) & = \dfrac{R_{T_2}(t) v_{C_{eq}}(t - \Delta t)}{R_{T_2}(t) + R_{T_1}(t) + R_{cEQ}} \end{cases}$$

- $R_{SM_{eq}}$ – Thevenin impedance is dependent on the state of valves and equivalent impedance of capacitor.
- $v_{SM_{eq}}$ – Thevenin voltage depends on the state of valves, equivalent impedance of capacitor and history currents in the sub-module.

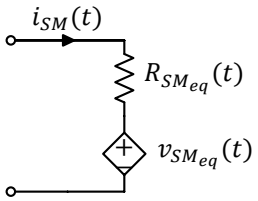


Figure 8.18: Sub-module's Thevenin equivalent representation

This equivalence for a sub-module can be extended to all sub-modules in an arm. "Daisy chaining" [15] of N sub-modules with their Thevenin representation gives equivalent circuit for the arm as illustrated in fig. 8.19.

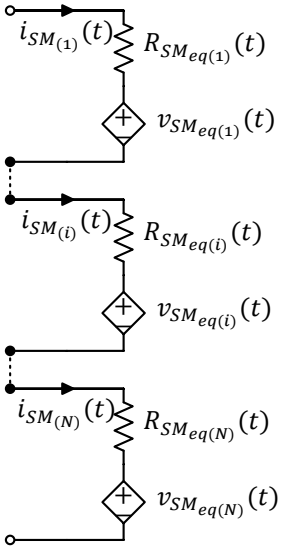


Figure 8.19: Cascaded Chain of N sub-modules

This yields a unified Thevenin's equivalent model of all SM's in an arm as:

$$v_{MV}(t) = \sum_{i=1}^{N} v_{SM_i}(t) = \sum_{i=1}^{N} [i_{SM_i} R_{SM_{eq_i}} + V_{SM_{eq_i}}] \tag{8.48}$$

Series connection of sub-modules imply equal current i.e. $i_{SM_i} = i_{MV}\ \forall i$

$$v_{MV}(t) = i_{MV} R_{MV_{eq}} + v_{MV_{eq}} \tag{8.49}$$
$$\begin{cases} R_{MV_{eq}} & = \sum_{i=1}^{N} R_{SM_{eq_i}} \\ v_{MV_{eq}} & = \sum_{i=1}^{N} v_{SM_{eq_i}} \end{cases}$$

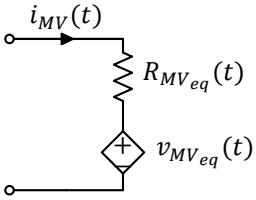


Figure 8.20: Arm's Thevenin equivalent representation

Equation (8.49) reduces all N sub-modules in an arm to a two node circuit as illustrated in fig. 8.20.

The model derived so far determines the state of valves based only gate signals alone; therefore, it only represents *inserted* and *bypassed* states of an SM and doesn't model its *blocked* state. The Blocked state of MMC finds application during dc side faults, and its modeling is essential for HVDC studies.

In *blocked* state both IGBTs are switched off and freewheeling diodes allow the flow of current as illustrated in fig. 8.21. Therefore in this state current flow is dictated by freewheeling diodes and additional consideration of voltages and currents diodes are required to determine the operation state of a valve ('ON', 'OFF'). As discussed earlier in this state SM capacitor is charged in case of positive current with diode $D1$ forward biased, bypassed for negative current with diode $D2$ forward biased or else SM blocks flow of the arm current.

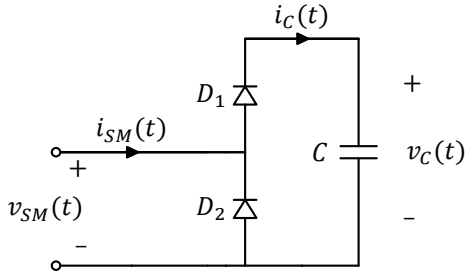


Figure 8.21: Blocked state representation of a SM

Based on these principles, existing literature proposes two different techniques for incorporation of the blocked state in this Equivalent ideal model.

- Algorithmic Method:
  In this method as proposed in article ([16, 18]), solver based on last time step values of voltage and current reproduces the natural commutation in diodes using an algorithm approach as detailed below: To avoid numerical oscillation during

Blocked state algorithm

if SM_i *blocked* **then**
  if $i_{(\phi\pm)}(t) > 0$ and $v_{SM_i}(t - \Delta T) > v_{C_i}(t)$ **then**
    SM_i *Inserted* i.e. set $R_{T_{1(i)}}(t) = R_{ON}$ and $R_{T_{2(i)}}(t) = R_{OFF}$
  else if $i_{(\phi\pm)}(t) < 0$ and $v_{SM}(t - \Delta T) < 0$ **then**
    SM_i *Bypassed* i.e. set $R_{T_{1(i)}}(t) = R_{OFF}$ and $R_{T_{2(i)}}(t) = R_{ON}$
  else
    $R_{T_{1(i)}}(t) = R_{OFF}$ and $R_{T_{2(i)}}(t) = R_{OFF}$
  end if
end if

  the commutation diode article ([18]) utilizes an iterative approach to determine the conduction states correctly.

- Addition of IGBT and diode:
  In this method as proposed in [19], additional external IGBT and diodes are incorporated with the arm's Thevenin equivalent representation as illustrated in fig. 8.22 to model the blocked state of operation.

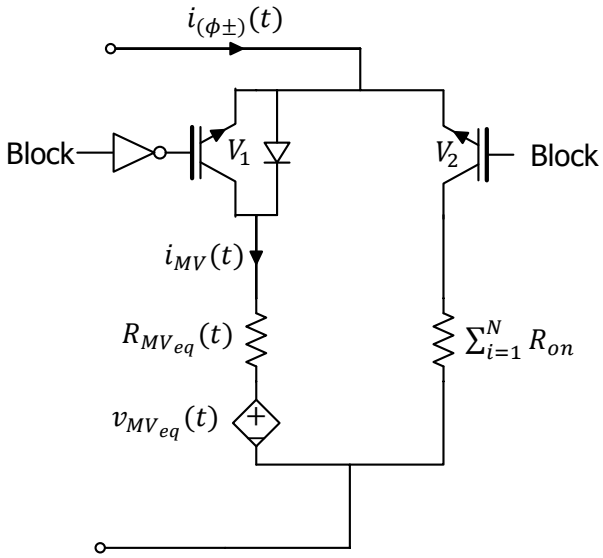


Figure 8.22: TEM with blocked state modeling

These additional IGBTs and diodes mimic the operation of SMs as an uncontrolled rectifier during *blocked* state and is explained as follows:

- Under the nominal operation, IGBT V_1 is kept ON and V_2 is kept off i.e. Thevenin's equivalent model of the arm is connected directly to the converter system.
- In the case of a *blocked* state, IGBT V_1 is turned OFF and V_2 is turned ON. In this mode of operation, states of valves inside the Thevenin's equivalent model are determined by the polarity of arm current. With positive arm current all SMs are inserted and with negative all are bypassed.
  In the case of positive arm current and forward biased diode V_1 all SMs are simultaneously charged; negative arm current with the forward biased V_2 bypasses entire arm via resistance $\sum_{i=1}^{N} R_{on}$ and lastly reverse biased V_1, and V_2 mimic the "Opened" state of SM.

This representation is simple and doesn't require additional storage and is used for the Thevenin equivalent model in this study.

Conclusion TEM drastically reduces the number of nodes in the system. Calculation within an arm no longer utilize computationally expensive matrix operation but instead are modeled by N equations, determined solely by gate signals and last

time step information (eq. (8.49)). In this modeling scheme, an individual arm is mathematically represented by a set of N algebraic equation that update capacitor voltages and a nodal admittance matrices of dimension $3\ by\ 3$ each. References [16–24] validate and present enhanced versions of this model. This representation offers high computational efficiency and moreover is suitable for parallel processing as detailed in articles ([21, 22]). With parallel computation dedicated processors for individual Arms simultaneously determine arm Thevenin equivalents based on gate signals and historical information which are utilized by processor modeling the converter and rest of the system.

In short, TEM drastically improves computational performance while maintaining accuracy. Unlike DIM and ISM, this representation does not utilize interpolation for exact tracking of switching instances and results from this model tend to have less accuracy as compared to DIM. Nevertheless, the small time step of simulation implies that the effect is negligible for most of the system dynamics.

This model provides all details for the converter and can be utilized for most studies related to external and internal parameters of MMC.

- Simulation of external faults.
- Design and validation of arm and module modulation schemes.
- Design and validation of controls.
- Validation of simplified models.

On the downside, this model does not allow end user direct access to individual MMC components and sub-modules and can't be directly utilized for with studies involving modification and access to individual SMs e.g. internal fault in an SM.

8.7.2. T-VI Switching Function Models

In Boolean algebra, switching functions refer to a function that takes value 0 and 1. Applied to power electronic these functions denote ON(1) and OFF(0) state of a switch and are formally defined as:

> "The switching function is a statement of the time instances that both the input and output of a switch or a switch configuration are the same; the input is reflected to the output. The switching function relates the input to the output in a similar way that the transfer function relates input to output in control systems [167]. "

This modeling technique aims to derive analytical relations that accurately represent voltages and currents associated with a switched system into a single unified expression [167]. For simulation purposes based on these relations, switches are replaced by controlled voltage and current sources. In this modeling technique, the operation of an individual semiconductor device is represented by ideal representation using binary number i.e. 1 – ON and 0 – OFF.

Adam et al. [31] present this modeling technique for MMCs where the nominal operation of individual sub-module is expressed in terms of its switching function. In the proposed model, the nominal operation of SM i.e. *Inserted* and *bypassed* states, where valves behave as bi-directional switches, are modeled by switching function $\eta_{SM_i(\phi\pm)}$, similar to reference [31]. Moreover *blocked* state, where diodes dictate whether the SM is *Inserted* ($D1$ forward biased), *bypassed* ($D2$ forward biased) or *opened* ($D1, D2$ reverse biased), is modeled using an additional switching function $\beta_{SM_i(\phi\pm)}$. Based on these functions, voltage source, $v_{SM_i(\phi\pm)}$, and series switch, $SW_{i(\phi\pm)}$, reproduce SM operation. These functions are defined as follows:

- $\eta_{SM_i(\phi\pm)}$ equals 1 when SM_i is *inserted* or *blocked* with either diode forward biased, and is otherwise 0.
- $\beta_{SM_i(\phi\pm)}$ equals 1 when sub-module is inserted or bypassed or diode $(D1)$ is forward biased, otherwise it is 0.
- $SW_{SM_i(\phi\pm)}$ is normally closed unless $D1, D2$ are reverse-biased with SM blocked i.e.

$$SW_{SM_i(\phi\pm)} = \eta_{SM_i(\phi\pm)} \vee \beta_{SM_i(\phi\pm)} \tag{8.50}$$

- Voltage source, $v_{SM_i(\phi\pm)}$ equals $v_{c_i(\phi\pm)}$ when capacitor is inserted and else is 0 i.e.

$$v_{SM_i(\phi\pm)} = (\eta_{SM_i(\phi\pm)} \wedge \beta_{SM_i(\phi\pm)}) v_{c_i(\phi\pm)} \tag{8.51}$$

Table 8.1 further elaborates on these functions. Moreover, an algorithmic approach as illustrated fig. 8.23 is utilized to determine the state of valves when SMs are first blocked. This ensures that when MMC is first blocked all SMs are either all inserted/bypassed/opened based on the current direction. This is justified by inductive

Table 8.1: Truth table for Switching functions

$\eta_{SM_i(\phi\pm)}$	$\beta_{SM_i(\phi\pm)}$	$SW_{i(\phi\pm)}$	State	T1	T2	$v_{SM_i(\phi\pm)}$	$i_{(\phi\pm)}$	Capacitor
1 1	1 1	1 1	Inserted	ON	OFF	$v_{c_i(\phi\pm)}$	> 0 < 0	Charging - via Diode D1 Discharging - via IGBT T1
0 0	1 1	1 1	Bypassed	OFF	ON	0	> 0 < 0	None - bypassed via IGBT T2 None - bypassed via Diode D2
1 1 0	1 0 0	1 1 0	Blocked	OFF	OFF	$v_{c_i(\phi\pm)}$ 0 –	$i_{(\phi\pm)} > 0$ & $v_{SM}(t-\Delta t) \geq v_c(t-\Delta t)$ $i_{(\phi\pm)} \leq 0$ & $v_{SM}(t-\Delta t) \leq 0$ *Else*	Charging - via Diode D1 None - bypassed via Diode D2 None and $i_{(\phi\pm)} = 0$

nature of currents that forcefully forward bias diodes $D1$ or $D2$ when MMC first goes into blocking state. This state for all SMs is retained until arm current drops to zero and table 8.1 dictates the subsequent states of SMs.

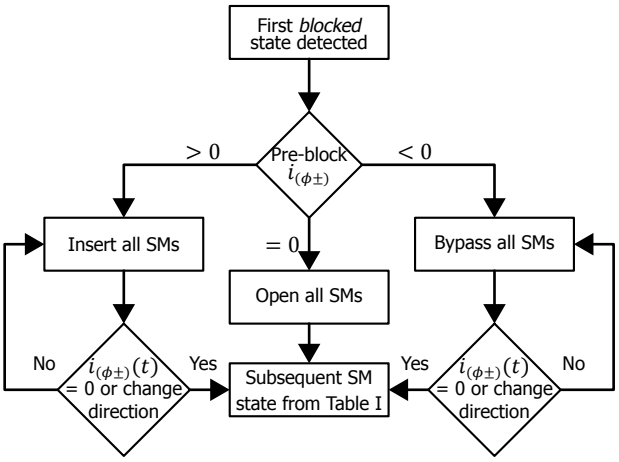


Figure 8.23: SM state after first block

Based on these switching functions, the model of an half-bridge sub-module is defined by eqs. (8.52) to (8.54) equivalently represented as in fig. 8.24.

$$v_{SM_i(\phi\pm)}(t) = \left(\eta_{SM_i(\phi\pm)} \wedge \beta_{SM_i(\phi\pm)}\right) v_{c_i(\phi\pm)}(t) \tag{8.52}$$

$$i_{c_i(\phi\pm)}(t) = \left(\eta_{SM_i(\phi\pm)} \wedge \beta_{SM_i(\phi\pm)}\right) i_{(\phi\pm)}(t) \tag{8.53}$$

$$v_{c_i(\phi\pm)}(t) = \frac{1}{C}\int_0^t i_{c_i(\phi\pm)}(t)dt \tag{8.54}$$

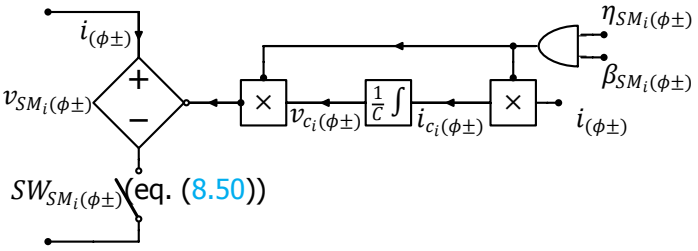


Figure 8.24: Sub-module's switching function representation

Cascaded/series configuration of all sub-modules in an arm implies that an arm operation is defined by eqs. (8.55) and (8.56) and equivalently represented as in fig. 8.25.

$$v_{(\phi\pm)} = \sum_{i=1}^{N} v_{SM_i(\phi\pm)} \tag{8.55}$$

$$SW_{(\phi\pm)} = \prod_{i=1}^{N} \beta_{SM_i(\phi\pm)} \vee \eta_{SM_i(\phi\pm)} \tag{8.56}$$

Unlike SFM presented in literature this model incorporates *blocked state* operation of sub-modules in the function itself.

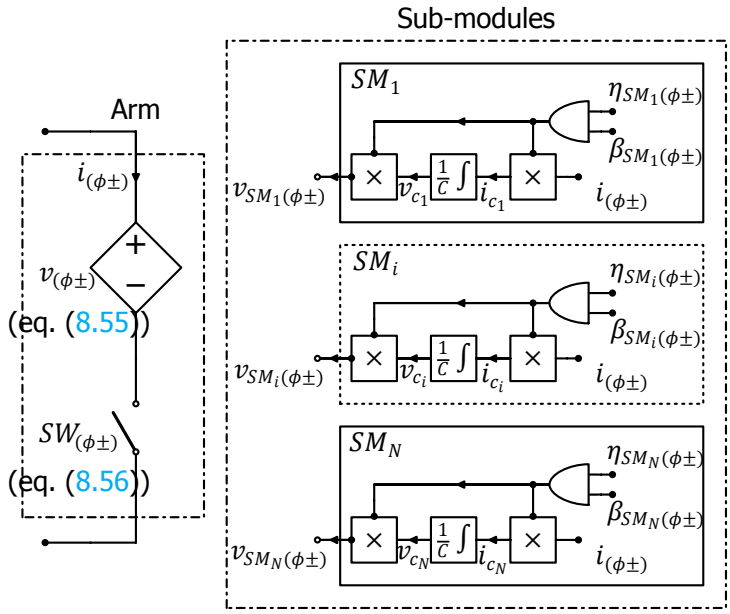


Figure 8.25: Arm's switching function representation

Conclusion In short, switching function model takes the idealized representation of semiconductor devices as a bi-value resistor to the next level and models them with Boolean functions.

Compared to circuit-based models this modeling scheme does not simulate individual semiconductors; instead, model the effect of individual switchings through boolean variables $\eta_{SM_i(\phi\pm)}$. Similar to TEM, this approach significantly reduces the number of nodes in the system and replaces matrix operations and interpolation

associated with modeling of switches with simple integration and algebraic operations [31]. Moreover, this model retains individual sub-modules representation thus model retains all currents and voltage in the system.

Compared to TEM, use of Boolean function instead of switched resistors makes numerical computation more efficient and avoids ill-conditioned mathematical operations i.e. due to division by very small or large values. In conclusion, SFM offers a more computationally efficient and numerically stable model for the MMC.

This model provides all details for the converter and can be utilized for most studies related to external and internal parameters of MMC.

- Simulation of external faults.
- Design and validation of arm and module modulation schemes.
- Design and validation of controls.
- Validation of simplified models.

However, this model does not allow end user direct access to individual sub-modules and can't be directly utilized for with studies involving modification and access to individual SMs e.g. fault in an SM.

8.7.3. T-VII Average value model

Despite the reduced number of nodes in the system with T-V *Equivalent ideal model* and T-VI *switching function model*, individual representation for SM's still implies that the models are computationally intensive for network level studies. Therefore, to mitigate the computational burden of modeling individual sub-modules, further simplification in modeling technique is required, and average value models are introduced.

Average value modeling further simplifies converter representation by ignoring the switching effects in individual submodule and similar to *SFM* models the AC and DC dynamics of the converter as controlled current and voltage sources [152].

The assumption of identical construction of SMs and instantaneous voltage balance control implies that the average duty cycle ($\eta_{SM_i(\phi\pm)}$) for all SMs in an arm is more or less equal. In the blocked state, all SMs in an arm are simultaneously blocked. This implies that the average operation for all SMs in an arm is identical during fault and nominal operating conditions. Based on this, the proposed AVM models an arm by a single equivalent submodule.

To model this, the average equivalent of switching functions of the SFM are utilized. Average duty cycle, *insertion index* [40, 95] defines the average instantaneous value of $\eta_{SM_i(\phi\pm)}$ i.e. the ratio of SMs "inserted or blocked".

$$n_{(\phi\pm)}(t) = \frac{1}{N}\sum_{i=1}^{N} \eta_{SM_i(\phi\pm)}[t] \tag{8.57}$$

Since all SMs are simultaneously blocked in an arm, a single blocked parameter $B_{(\phi\pm)}[t]$ is introduced for AVM i.e.

$$\beta_{SM_i(\phi\pm)}[t] = B_{(\phi\pm)}[t] \quad \forall i \tag{8.58}$$

Based on these parameters an average arm operation is defined by eqs. (8.59) to (8.61) and can be equivalently represented as in fig. 8.26.

$$v_{(\phi\pm)} = (n_{(\phi\pm)}B_{(\phi\pm)}[t])\overline{v^{\Sigma}_{c_{\phi\pm}}} \tag{8.59}$$

$$\overline{i^{\Sigma}_{C(\phi\pm)}} = (n_{(\phi\pm)}B_{(\phi\pm)}[t])i_{(\phi\pm)}(t) \tag{8.60}$$

$$\overline{v^{\Sigma}_{c_{\phi\pm}}} = \frac{N}{C}\int \overline{i^{\Sigma}_{C(\phi\pm)}}dt \tag{8.61}$$

$$SW_{(\phi\pm)} = B_{(\phi\pm)} \vee n_{(\phi\pm)} \tag{8.62}$$

Where, $v_{(\phi\pm)}, \overline{v^{\Sigma}_{c_{\phi\pm}}}, \overline{i^{\Sigma}_{C(\phi\pm)}}$ are the arm voltage, and the voltage and current for equivalent SM's capacitor.

With unified representation for all sub-modules in the arm, this model does not utilize voltage balancing control. Nevertheless, the model incorporates the effect

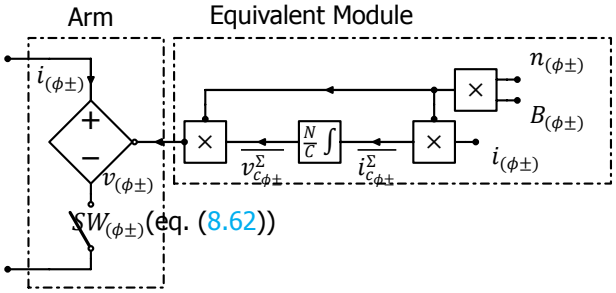


Figure 8.26: Arm's average value representation

of switching by utilizing discrete values for the insertion index, which improves accuracy [33, 162]. However, if module level modulation is not incorporated this formulation yields a *continuous* model.

Conclusion In short, average value model assuming perfect voltage balancing, utilize a single equivalent module that models the total stored energy in N sub-modules. This offers superior computational speed at the expense of accuracy. Despite this, AVM provides suitable representation for terminal characteristic of MMC and can be utilized for:

- Simulation of external faults.
- Design and validation of arm modulation schemes.
- Design and validation of controls.

On the downside, this model does not provide information about internal parameters of converter associated with individual sub-modules.

Since this model does not take individual sub-module into consideration and does not utilize voltage balancing control. Therefore, AVM cannot be utilized for studies involving individual SM such as design and validation of voltage balancing control, failure of a sub-module etc.

8.8. Time step for simulation

For EMT type solvers, ideally simulation time step should be as small as possible for precise calculations using the trapezoidal rule of integration. However, smaller time step implies higher computational load. This presents a need for optimized time step selection that ensures fast simulations without losing on accuracy. In general, maximum expected frequency of a system is the determining factor for stepsize its simulation. For accurate results, Nyquist frequency of EMT type solvers should be at least five times that of the maximum frequency of the system [168] i.e.

$$f_{Nyq} = \frac{1}{2\Delta t} \geq 5 * f_{max} \implies \Delta t \leq \frac{\tau_{min}}{10}$$

$$\text{where, } \begin{cases} f_{max} & = \text{Maximum frequency in the system} \\ \tau_{min} & = \text{Corresponding minimum time constant} \\ f_{Nyq} & = \text{Nyquist frequency of solver} \\ \Delta t & = \text{Corresponding step size} \end{cases}$$

However, the maximum frequency associated with the system is usually unknown. As discussed earlier, for HVDC studies at system and network level switching operation is modeled as an instantaneous transition. Therefore with such simulation maximum frequency associated with the system is taken on the same scale as that of switching events. Switching events are dictated by control and are dependent on the modulation technique and the number of sub-modules.

For nearest level control, where a staircase modulation approximates the reference sinusoidal wave, smallest instants between two switching events can be calculated as follows [114]:

Assuming reference signal given by:

$$v_{ref}(t) = \frac{1}{2}\hat{m}_\phi v_{dc} \cos(\omega t) \tag{8.63}$$

Based on this, minimum time interval for reference signal to change by one level can be approximated as:

$$T_{min} \frac{d}{dt} \underset{max}{v_{ref}}(t) = \frac{1}{N} v_{dc} \implies T_{min} = \frac{2}{N} \frac{1}{\hat{m}_\phi \omega} \tag{8.64}$$

For EMT models with NLC to accurately capture system dynamics within switching evens the time step of simulation should be at least five times less than T_{min} i.e.

$$\Delta t \leq \frac{2}{5N} \frac{1}{\omega} \tag{8.65}$$

For a $N = 14$ this yields $\Delta t \leq 90\mu s$.

On the other hand, for detailed models where transients within the switching process are to be accurately modeled the time step should be far smaller than the time scale of switching events (in order of nano-seconds).

8.9. Conclusion

In this chapter, various equivalent models for MMC were derived. All of the models inherently reproduce all operating modes of converter i.e. *inserted, bypassed* and *blocked*. Tables 8.2 and 8.3 summarize these models:

Table 8.2: EMT Models for MMC: Summary

Model Type	Semiconductor Representation	Solution Method	Dynamics Modeling	Targeted Applications
T-I,II DM	Full Physics or non-linear diodes	Nodal analysis using matrix operations	Transients within switching event	Component level studies and switching losses
T-III DIM	Bi-value resistors	Nodal analysis using matrix operations	Transients with switching as instantaneous event	System and network level studies
T-IV ISM	Bi-value resistors	Nodal analysis using matrix operations with artificial delay	Transients with switching as instantaneous event	System and network level studies
T-V EIM	Bi-value resistors	Algebraic equations for entire all SMs without interpolations	Transients with switching as instantaneous event	System and network level studies
T-VI SFM	Switching functions (0&1)	Algebraic equations for entire all SMs without interpolations	Transients with switching as instantaneous event	System and network level studies
T-VII AVM	Switches not individually modeled	Algebraic equations for entire as an equivalent module	Transients with switching events averages	Network level studies

Table 8.3: EMT Models for MMC: Requirements

Model Type	Time-step Parameters	Over-all Accuracy	Computational Efficiency
T-I,II DM	nanoseconds	★★★★★	★★★★★
T-III DIM	microseconds	★★★★★	★★★★★
T-IV ISM	microseconds	★★★★★	★★★★★
T-V EIM	microseconds	★★★★★	★★★★★
T-VI SFM	microseconds	★★★★★	★★★★★
T-VII AVM	micro to milliseconds	★★★★★	★★★★★

T-I – T-II are highly complex and due to the computational burden are not suitable for analyses of complete MMC and connected systems. T-III – T-VII are of interest in this study and are analyzed in detail using PSCAD/EMTDC simulations in the following chapter.

9

Simulation

This chapter presents and compares PSCAD/EMTDC simulation results for different arm and module level modulation schemes as discussed in chapter 6 and equivalent models for MMCs as proposed in chapter 8.

9.1. Arm & Module Level Modulations

In this section, arm and module level modulation techniques for MMC as examined in sections 6.1 and 6.2 are investigated via PSCAD/EMTDC simulation.

The objective here is to compare these modulation techniques based on their impact on harmonics in circulating current, ripple in submodule's capacitor voltage, total harmonic distortion in line-line ac voltage and average switching frequency in the system under stationary conditions.

These parameters are evaluated via:

- Relative magnitude of non-dc component of circulating current.
  Calculated from FFT of circulating current as:

$$\sum_{non-dc} i_{circ} = \frac{1}{i_{circ(h=0)_\phi}} \sum_{k=1}^{50} i_{circ(h=k)_\phi} \tag{9.1}$$

  where h is the order of harmonic.

- Total harmonic distortion in line-line ac voltage:

Calculated from FFT of line-line ac voltage as:

$$THD = \frac{1}{v_{L-L(h=1)_\phi}} \sqrt{\sum_{k=2}^{50} v^2_{L-L(h=k)_\phi}} \tag{9.2}$$

where h is the order of harmonic.

- Voltage ripple in sub-module's capacitor:
  Calculated in terms of range (maximum and minimum values), mean μ and standard deviation σ of cumulative capacitor voltage for an arm.
- Switching frequency:
  Total switching events in positive and negative arms per cycle.

For this comparison an islanded converter system as illustrated in fig. 9.1 is utilized. The system considers an ideal dc link and an MMC connected to an AC load. The dc-side is modeled with two ideal dc sources grounded in a center. For the MMC a detailed ideal model is utilized while ac load is models via constant loads.

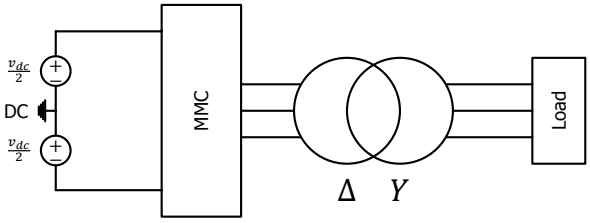


Figure 9.1: PSCAD Model Schematic

The simulation mimics a $20KV$ HVDC link and a fourteen sub-modules per arm MMC rated at $15MVA$ together with a constant three-phase ac load of $12 + 9j\,MVA$. For the MMC, to ensure a ripple (ϵ) of less than 5% in submodule's capacitor voltage, the required total stored energy per MVA, E_{MMC} for the given load was estimated to be $51 \approx 60KJ/MVA$ from eq. (4.15). This yields a value $10.5mF$ of capacitance per module eq. (4.14). Using eq. (4.17) the desired value of arm inductance $L > 2.8mH$; therefore $L = 3mH$ was selected. Assuming an overall loss of 1.5% in the MMC, arm resistance is calculated as 0.1Ω (assuming circulating current to be purely direct). For the converter transformer, a $1:1\ \Delta - Y$ transformer with an inductance of 3% is selected. These parameters for the system are summarized in table 9.1.

Table 9.1: MMC_{14} – Parameters

MMC :	$N = 14$ $L_{arm} = 3mH\,(11.68\%)$	$C = 10.5\ mF$ $R_{arm} = 0.1\Omega$
AC Load:	$12 + 9j\,MVA$	
DC Link: Transformer:	$v_{dc} = 20kV$ $\Delta - Y$ (1:1)	$S_{rated} = 15MVA$ $L_{tf} = 3\%$

9.1.1. Comparison of Arm Level Modulations

The objective here is to investigate different arm level modulation methods as presented in section 6.1. The control scheme utilized here is summarized in Table 9.2.

Table 9.2: Case I: Details for system

System	fig. 9.1–MMC_{14} - Islanded
MMC Model	Detailed ideal model (section 8.7.1)
Module-Modulation	Nearest level control
Voltage balancing	*Rank method* in interrupt mode(section 5.2.1)
Simulation Time	$2s$
Simulation time step	$10\mu s$

Case I : Direct Modulation

Here direct modulation as detailed in section 6.1.1 is utilized for arm level modulation. The simulation results below present internal and terminal dynamics of converter under stationary conditions.

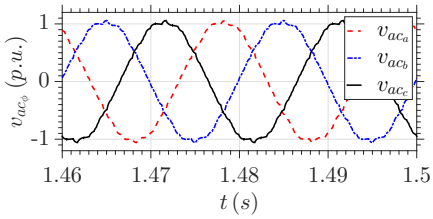


Figure 9.2: Three Phase AC voltage at PCC

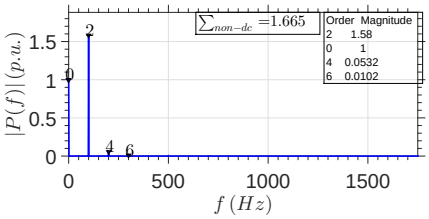


Figure 9.5: Spectrum of Circulating Current

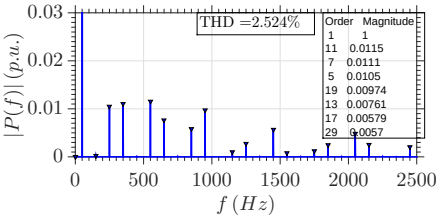


Figure 9.3: Harmonic distortion in line-line ac voltage v_{ab}

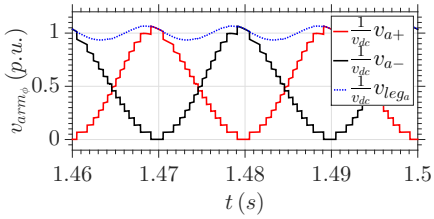


Figure 9.6: Arm voltages and cumulative inserted voltage in a leg

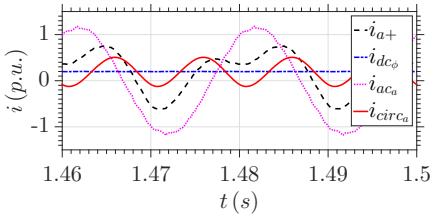


Figure 9.4: Currents in MMC

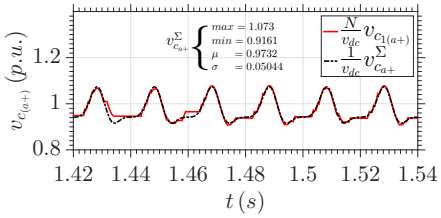


Figure 9.7: Capacitor Voltage

Table 9.3: Case I: Switching Details

Average Switching in Positive Arm Phase A = 364.16
Average Switching in Negative Arm Phase A = 364.08
Average switching frequency for an individual IGBT = $13Hz$

Case II : Uncompensated Modulation

Here uncompensated Modulation as detailed in section 6.1.2 is utilized using circulating current suppression controller for arm level modulation. The simulation results below present internal and terminal dynamics of converter under stationary conditions.

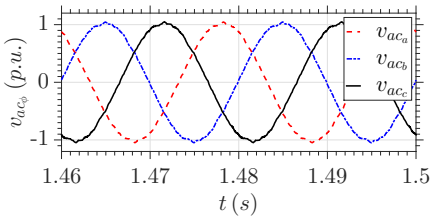


Figure 9.8: Three Phase AC voltage at PCC

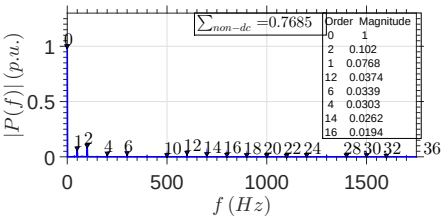


Figure 9.10: Spectrum of Circulating Current

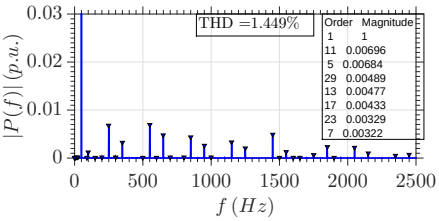


Figure 9.9: Harmonic distortion in line-line ac voltage v_{ab}

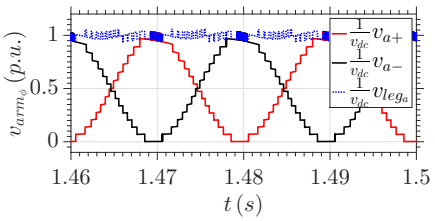


Figure 9.11: Arm voltages and cumulative inserted voltage in a leg

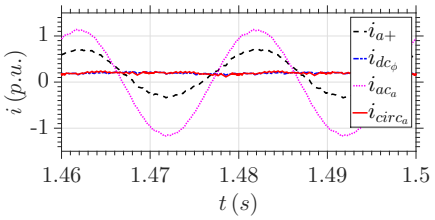


Figure 9.12: Currents in MMC

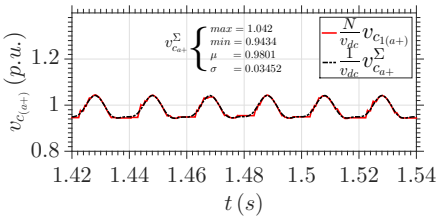


Figure 9.13: Capacitor Voltage

Table 9.4: Case II: Switching Details

Average Switching in Positive Arm Phase A = 396.32
Average Switching in Negative Arm Phase A = 471.08
Average switching frequency for an individual IGBT = 15.5Hz

Case III : Compensated Modulation with estimated cumulative capacitor voltage

Here compensated Modulation as detailed in section 6.1.3 is utilized using estimated cumulative capacitor voltage for arm level modulation. The simulation results below present internal and terminal dynamics of converter under stationary conditions.

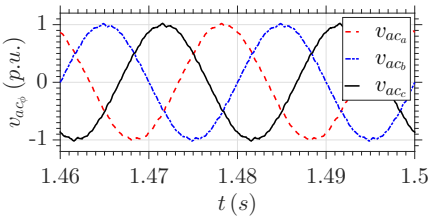


Figure 9.14: Three Phase AC voltage at PCC

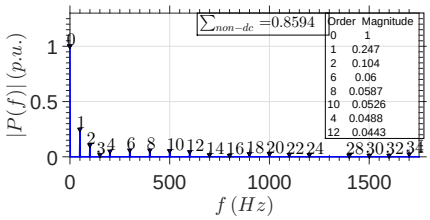


Figure 9.16: Spectrum of Circulating Current

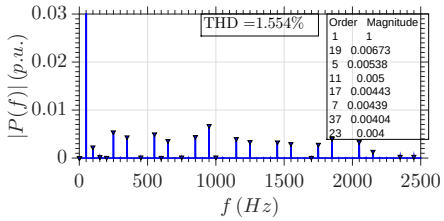


Figure 9.15: Harmonic distortion in line-line ac voltage v_{ab}

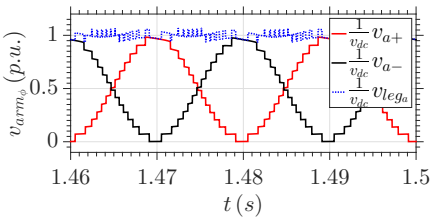


Figure 9.17: Arm voltages and cumulative inserted voltage in a leg

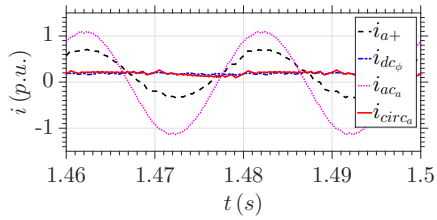


Figure 9.18: Currents in MMC

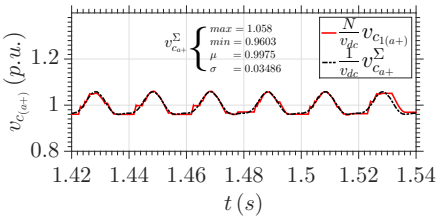


Figure 9.19: Capacitor Voltage

Table 9.5: Case III: Switching Details

Average Switching in Positive Arm Phase A = $364.16 = 2N(N-1)$
Average Switching in Negative Arm Phase A = 364.08
Average switching frequency for an individual IGBT = $13Hz$

Conclusion

The simulation results presented show superior characteristics of uncompensated and compensated modulations in comparison to direct modulation. Table 9.6 summarizes these findings.

Table 9.6: Arm Level Modulation: Findings

Modulation	*Non-dc component in* i_{circ_a}	*THD* $V_{L-L_{ac}}$	Cumulative capacitor voltage $v^{\Sigma}_{c_{a+}}$ *Max*	*Min*	μ	σ	*Switching frequency (Hz)*
Direct	1.665	2.524 %	1.073	0.9161	0.9732	0.05044	13
Uncompensated	0.7685	1.449 %	1.042	0.9434	0.9801	0.03452	15.5
Compensated	0.8594	1.554 %	1.058	0.9603	0.9975	0.03486	13

Uncompensated modulation, with CCSC, corrects for voltage imbalance in a phase leg that leads to significant reduction in the dominant second order harmonic in circulating current. This results in improved control of capacitor voltages and consequently reduces the total harmonic content of circulating current. On the downside, this method increases the number of switching events in a cycle. Nevertheless, as compared to direct modulation two folds decrease in harmonic content outweighs the 20% increase in switching frequency. Hence, this arm level modulation method offers reduced ratings of components, reduced losses, improved voltage balancing, and lower harmonic distortion in ac voltage.

Compensated modulation corrects for both the circulating current and varying cumulative capacitor voltage in an arm. This results in improved control of capacitor voltages and consequently reduces the total harmonic content of circulating current. This method does not affect the number of switching events in a cycle and simultaneously achieves reduced ratings of components, reduced losses, improved voltage balancing and lower harmonic distortion in ac voltage than direct modulation.

Table 9.7: Arm Level Modulation: Conclusion

Modulation	*Circulating Current*	*THD* $V_{L-L_{ac}}$	*Voltage Balancing*	*Switching frequency*
Direct	★★★★★	★★★★★	★★★★★	★★★★★
Uncompensated	★★★★★	★★★★★	★★★★★	★★★★★
Compensated	★★★★★	★★★★★	★★★★★	★★★★★

Table 9.7 summarizes the impact of these modulation techniques. Based on these findings, uncompensated modulation with lowest harmonic content in circulating current is chosen as the preferred choice of arm level modulations in this study.

9.1.2. Comparison of Module Level Modulations

The objective of this section is to investigate different module level modulation methods as presented in section 6.2. The control scheme utilized is summarized in Table 9.8. For a consistent comparison, carrier frequency (where applicable) is selected such that the average switching frequency of IGBTs is of the same order among all modulations.

Table 9.8: Case I: Details for system

System	fig. 9.1 – MMC_{14} - Islanded
MMC Model	Detailed ideal model (section 8.7.1)
Arm-Modulation	Direct Modulation (section 6.1.1)
Voltage balancing	*Rank method* in interrupt mode(section 5.2.1)
Simulation time step	$10\mu s$
Simulation time	$2s$

As discussed in section 6.2, each module level based on the operation of the positive and negative arm is split into $N+1$ and $2N+1$ level modulation. However, only $N+1$ modulation methods are analyzed here, where positive and negative arms a phase leg operate in a complementary fashion.

Case IV : Phase disposed PWM

Here level-shifted phase disposed pulse width modulation, as discussed in section 6.2.3, is utilized for the module-level modulation of the converter. This modulation scheme utilizes N carrier waves to determine the number of sub-modules to be inserted in an individual positive arm of a phase leg ($N_{ins.\phi+}$). While the number of modules to be inserted in the complementary arm are determined as:

$$N_{ins.\phi-} = N - N_{ins.\phi+} \tag{9.3}$$

The simulation results below present internal and terminal dynamics of converter under steady state with $m_f = 33$.

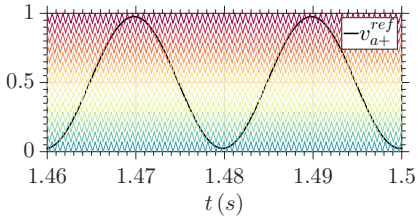


Figure 9.20: PD-PWM Carrier waves

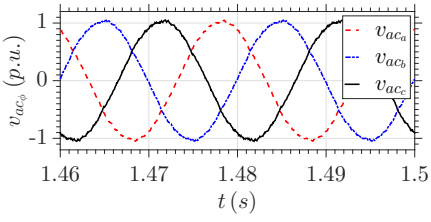


Figure 9.21: Three Phase AC voltage at PCC

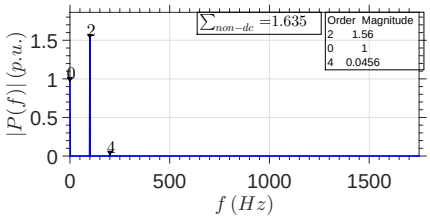


Figure 9.22: Spectrum of Circulating Current

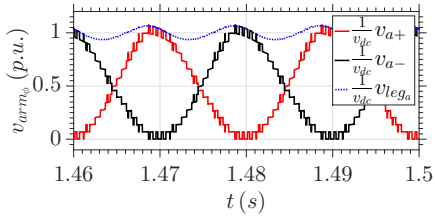


Figure 9.23: Arm voltages and cumulative inserted voltage in a leg

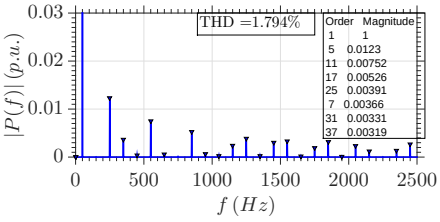


Figure 9.24: Harmonic distortion in line-line ac voltage v_{ab}

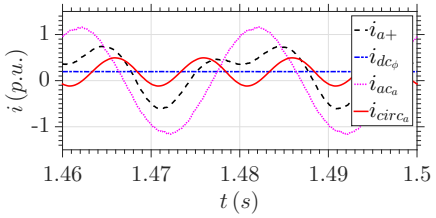


Figure 9.25: Currents in MMC

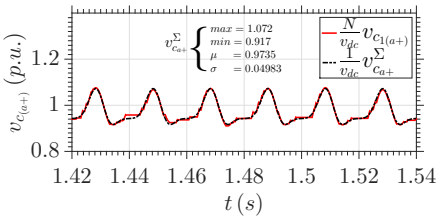


Figure 9.26: Capacitor Voltage

Table 9.9: Case IV: Switching Details

Avg. Switching in Positive Arm Phase A = 516
Avg. Switching in Negative Arm Phase A = 516
Avg. switching freq. for an individual IGBT = 18.43Hz

Case V : Alternative phase opposition disposition PWM

Here level-shifted alternative phase opposition disposition PWM, as discussed in section 6.2.3, is utilized for the module-level modulation of the converter. This modulation scheme utilizes N carrier waves to determine the number of sub-modules to be inserted in an individual positive arm of a phase leg ($N_{ins.\phi+}$). While the number of modules to be inserted in the complementary arm are determined as:

$$N_{ins.\phi-} = N - N_{ins.\phi+} \tag{9.4}$$

The simulation results below present internal and terminal dynamics of converter under steady state with $m_f = 33$.

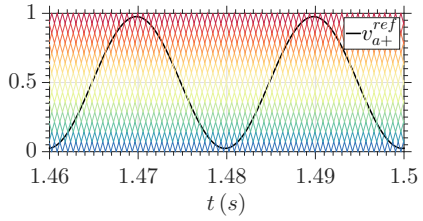


Figure 9.27: APOD-PWM Carrier waves

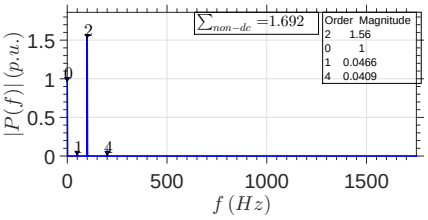


Figure 9.29: Spectrum of Circulating Current

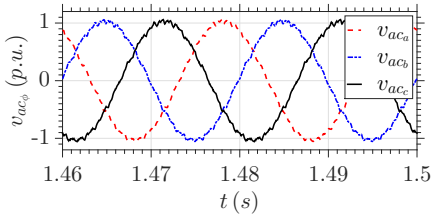


Figure 9.28: Three Phase AC voltage at PCC

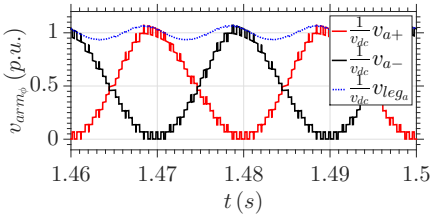


Figure 9.30: Arm voltages and cumulative inserted voltage in a leg

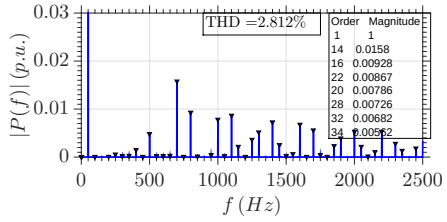


Figure 9.31: Harmonic distortion in line-line ac voltage v_{ab}

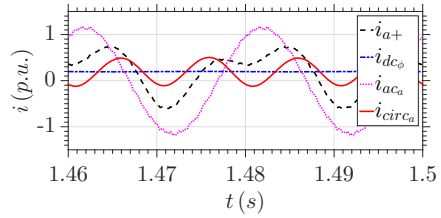


Figure 9.32: Currents in MMC

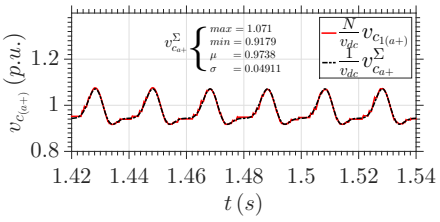


Figure 9.33: Capacitor Voltage

Table 9.10: Case V: Switching Details

Avg. Switching in Positive Arm Phase A = 572
Avg. Switching in Negative Arm Phase A = 588.16
Avg. switching freq. for an individual IGBT = $20.72Hz$

Case VI : Phase-shifted carrier PWM

Here phase-shifted PWM, as discussed in section 6.2.3, is utilized for the module-level modulation of the converter. This modulation scheme utilizes N carrier waves to determine the number of sub-modules to be inserted in an individual positive arm of a phase leg ($N_{ins.\phi+}$). While the number of modules to be inserted in the complementary arm are determined as:

$$N_{ins.\phi-} = N - N_{ins.\phi+} \tag{9.5}$$

The simulation results below present internal and terminal dynamics of converter under steady state with $m_f = 3$.

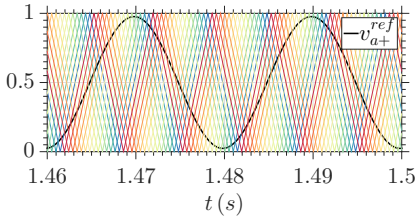


Figure 9.34: PS-PWM Carrier waves

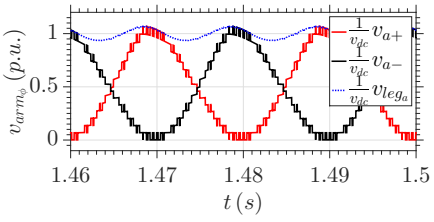


Figure 9.36: Arm voltages and cumulative inserted voltage in a leg

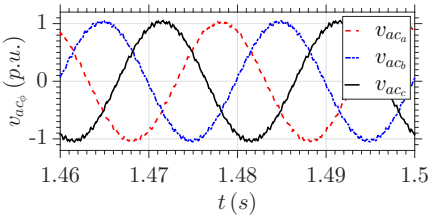


Figure 9.35: Three Phase AC voltage at PCC

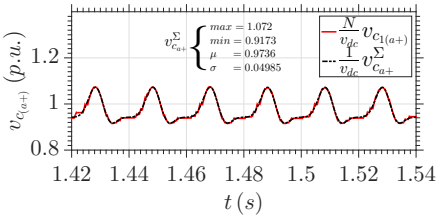


Figure 9.37: Capacitor Voltage

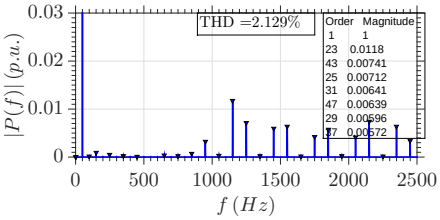


Figure 9.38: Harmonic distortion in line-line ac voltage v_{ab}

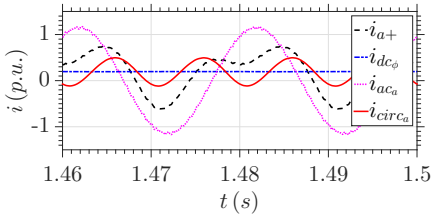


Figure 9.39: Currents in MMC

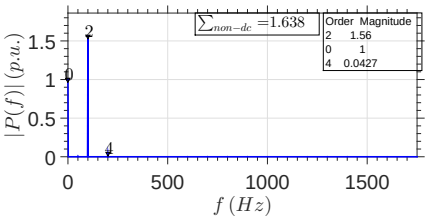


Figure 9.40: Spectrum of Circulating Current

Table 9.11: Case VI: Switching Details

Avg. Switching in Positive Arm Phase A = 598.48
Avg. Switching in Negative Arm Phase A = 598
Avg. switching freq. for an individual IGBT = $21.37Hz$

Conclusion

The simulation results presented show the impact of various module level modulation techniques on harmonic distortion in ac voltage, circulating currents and switching frequency. These findings are summarized in table 9.12.

Table 9.12: Module Level Modulation: Findings

Modulation	f_c *(Hz)*	*Non-dc component in* i_{circ_a}	*THD* $V_{L-L_{ac}}$	Cumulative capacitor voltage $v^{\Sigma}_{c_{a+}}$ *Max*	*Min*	μ	σ	*Switching freq.(Hz)*
NLC	–	1.665	2.524 %	1.073	0.9161	0.9732	0.05044	13
PD-PWM	1650	1.635	1.794 %	1.072	0.9170	0.9735	0.04983	18.43
APOD-PWM	1650	1.692	2.812 %	1.071	0.9179	0.9738	0.04911	20.72
PS-PWM	150	1.638	2.129 %	1.072	0.9173	0.9736	0.04985	21.37

For all of the techniques capacitor voltage and harmonic content of circulating current in more or less similar. PD-PWM yields lowest THD for line-line voltage whereas NLC offers the lowest switching frequency. Table 9.13 summarizes the impact of these modulation techniques. Based on these findings, NLC with its lowest switching frequency, relatively low impact on circulating current with a substantially low harmonic distortion in ac voltage and least computational complexity NLC is selected as the modulation of choice in this study.

Table 9.13: Module Level Modulation: Conclusion

Modulation	*Circulating Current*	*THD* $V_{L-L_{ac}}$	*Voltage Balancing*	*Switching frequency*
NLC	★★☆☆☆	★★★★★	★★★★★	★★★★★
PD-PWM	★★☆☆☆	★★★★★	★★★★★	★★★★★
APOD-PWM	★★☆☆☆	★★☆☆☆	★★★★★	★★☆☆☆
PS-PWM	★★☆☆☆	★★☆☆☆	★★★★★	★★☆☆☆

9.2. Comparison of EMT Models

This section presents a detailed simulation comparison of different EMT Models for the MMC as presented in chapter 8. The comparison is essential for categorization of models regarding relative accuracy and computational speed. Therefore, this section compares the efficient equivalent models against the detailed model of converter under stationary and transient conditions. The simulations for models are subjected to various set-points of real/reactive power and fault conditions. Figure 9.41 illustrates the timeline of the simulation.

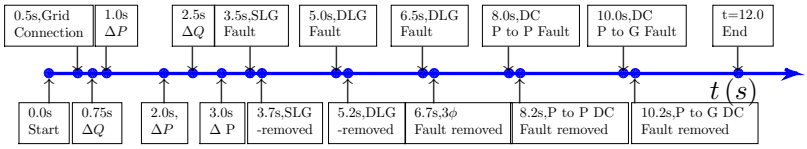


Figure 9.41: Time-line of events in simulation

For this evaluation, a strong grid-connected converter system as shown in fig. 9.42 is considered. In this system, the ac-grid is modeled with ideal voltage source behind reactance ($SCR = 50$) and the dc side is modeled via two ideal dc-sources grounded in the center.

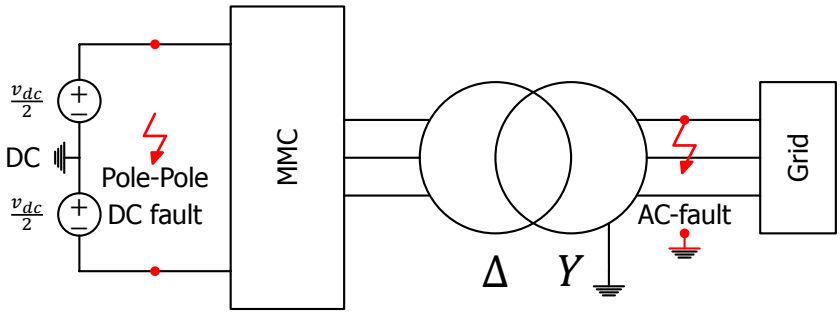


Figure 9.42: PSCAD Model Schematic

The parameters of the system are detailed in table 9.14.

Table 9.14: MMC_{14} – Parameters

MMC :	$N = 14$ $L_{arm} = 3mH\ (11.68\%)$	$C = 10.5\ mF$ $R_{arm} = 0.1\Omega$
AC Grid:	$v_{ac} = 11kV$	$X_{grid} = 2.0\%$
DC Link: Transformer:	$v_{dc} = 20kV$ $\Delta - Y\ (1{:}1)$	$S_{rated} = 15MVA$ $L_{tf} = 3\%$

9.2.1. Model Accuracy

To investigate the accuracy of the proposed models dynamics of the system before, during and after various transient conditions are compared against a detailed model of the converter.

Furthermore, the precision of the models is quantified against the detailed model using *normalized mean absolute error* (ϵ).

$$\epsilon = \frac{\sum^{\mathrm{N}} |X_{Model}(t) - X_{DIM}(t)|}{\mathrm{N}(X_{DIM}^{max} - X_{DIM}^{min})} \tag{9.6}$$

where
- $X_{Model}(t)$ — Dynamics of model under consideration
- $X_{DIM}(t)$ — Dynamics of detailed ideal model
- X_{DIM}^{max} — Maximum value of parameter for DIM
- X_{DIM}^{min} — Minimum value of parameter for DIM
- N — Set of datapoints

The simulations in this section are presented in three parts as follows:

1. Power reversal Operation of MMC $(t = 1.995 - t = 2.15s)$
   This simulation presents dynamics of converter undergoing a step change in set point of P, power exchange with ac grid, from $0.75\ p.u.$ to $-1.0\ p.u.$ at $t = 2.0s$.
2. Single-line to ground fault $(t = 3.4 - t = 3.8s)$
   This simulation presents dynamics of converter under ac-fault conditions, a $200ms$ single phase to ground fault at phase *a* of converter transformer through a small resistance at $t = 3.5s$ is simulated. The converter is kept connected to the fault without any modification in its control.
3. Pole to pole DC fault $(t = 7.9 - t = 8.6s)$
   This simulation presents dynamics of converter under dc-fault conditions, a $200ms$ pole to pole dc fault at $t = 8.0s$. In this case, the sub-modules are blocked as soon as dc voltage drop below 80% of its nominal value and un-blocked $300ms$ after fault removal.

Additional simulation results for case of system under going double-line to ground fault and pole to ground DC fault are presented in appendix (section C.1.1).

Power reversal simulation - External Dynamics

The simulations results present the state operation of MMC during power reversal under balanced conditions.

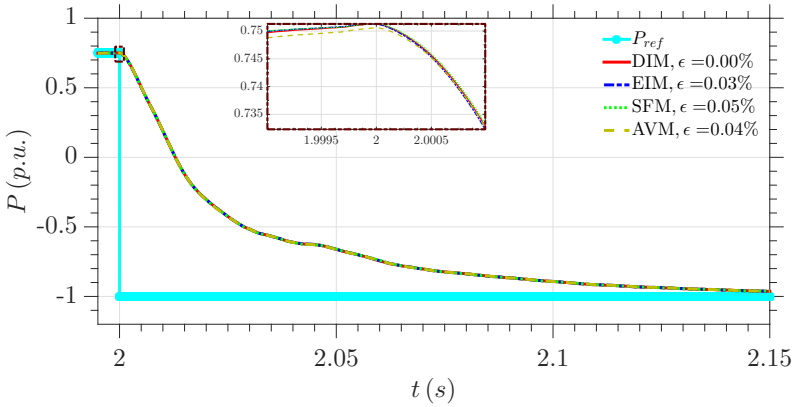


Figure 9.43: Real Power at MMC ac-side

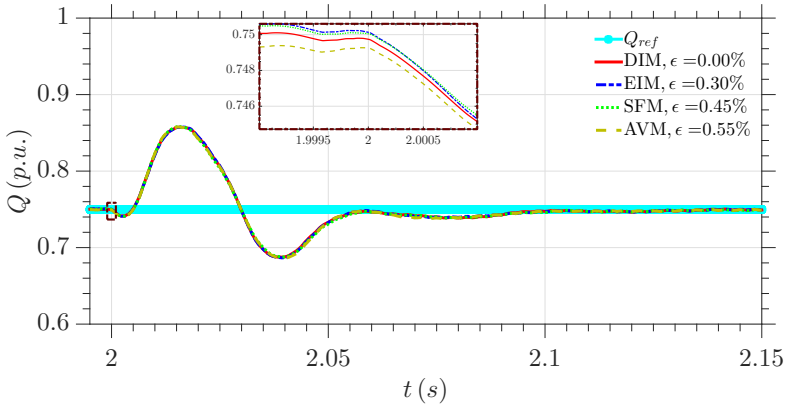


Figure 9.44: Reactive Power at MMC ac-side

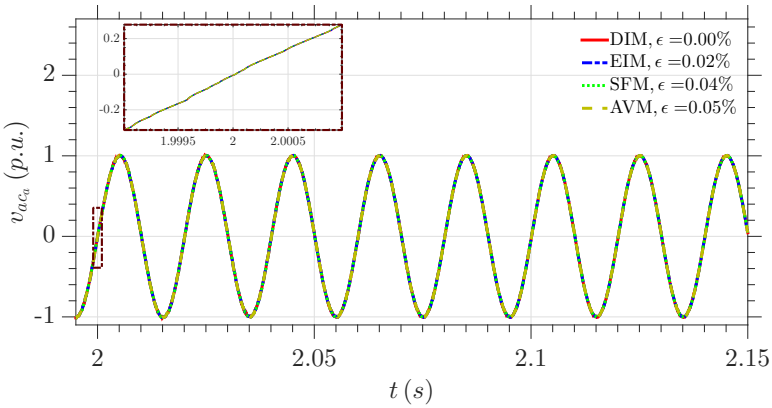


Figure 9.45: Phase a ac voltages at MMC terminals

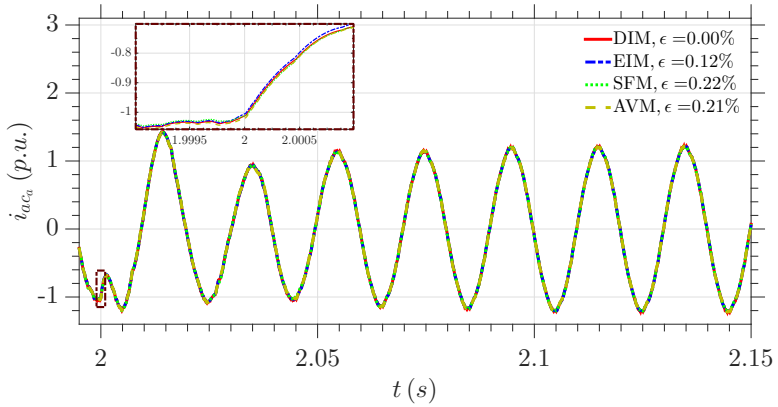


Figure 9.46: Phase a ac currents

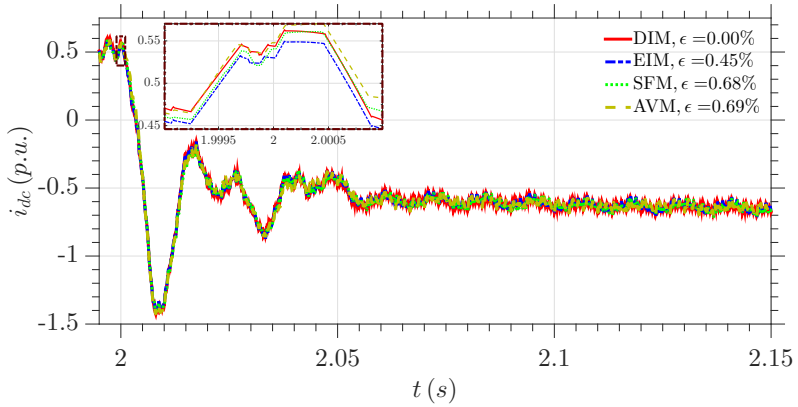


Figure 9.47: Current from dc side

Figures 9.43 to 9.47 present the terminal dynamics of converter under power reversal. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal:

- Near identical results for the detailed ideal model (DIM) and equivalent ideal model (EIM) with *normalized mean absolute error* of less than 0.5%. The minuscule differences in DIM and EIM are due to the absence of interpolations in EIM's calculation of arm equivalents and the rest of converter.
- Switching function model reproduces dynamics with high accuracy with *normalized mean absolute error* of less than 0.7%. Similar to EIM, absence of interpolations in the calculation of arm equivalent and binary representation for switches yields a slightly higher deviation from DIM.
- Average value model, despite its simplified representation, produces results with high accuracy with *normalized mean absolute error* of less than 0.7%.

Power reversal simulation - Internal Dynamics

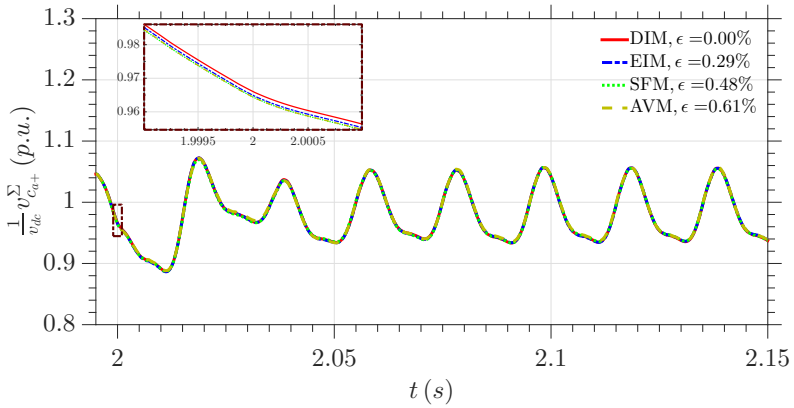


Figure 9.48: Cumulative capacitor voltage positive arm phase-a

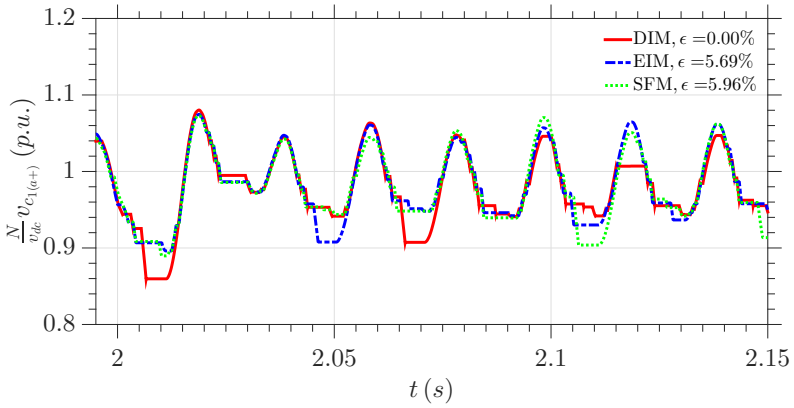


Figure 9.49: First Capacitor Voltage positive arm phase-a

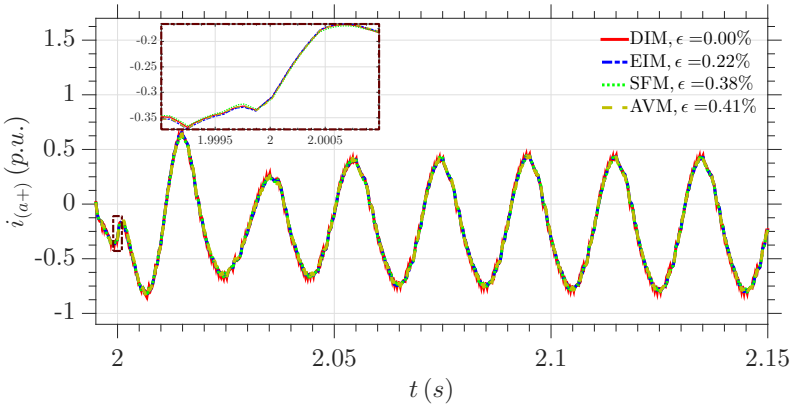


Figure 9.50: Positive arm Current phase-a

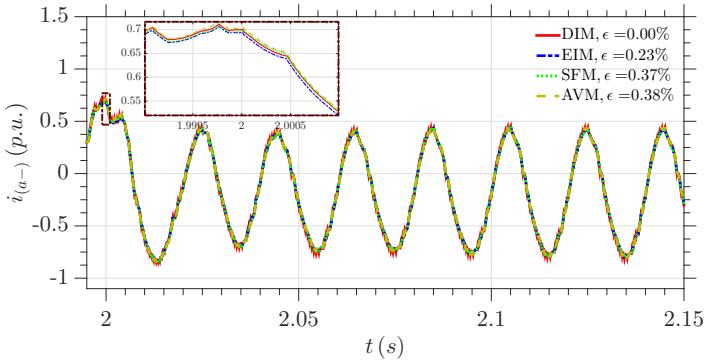


Figure 9.51: Negative arm Current phase-a

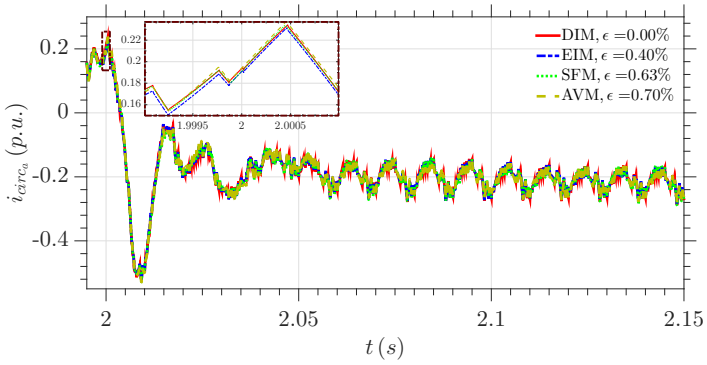


Figure 9.52: Circulating current phase-a

Figures 9.48 to 9.52 present internal dynamics of converter under power reversal.

- Simulation results reveal near identical results for the internal currents of MMC for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $0.4, 0.7$ & 0.8% respectively.
- Similarly, cumulative capacitor voltage in an arm is modeled with reasonable accuracy for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $0.3, 0.5$ & 0.6% respectively.
- However, as seen from fig. 9.49 for individual capacitor voltages, SFM and EIM tend to deviate significantly from DIM with *normalized mean absolute error* of around than 5.7 & 6% respectively. The reason for this deviation is attributed to the accumulation of slight difference in the solution of EIM and SFM due to an absence of interpolation in the calculation of arm equivalents. For most dynamics, this delay results in a minuscule difference in solution. However, for capacitor voltage balancing based on voltage sorting algorithm, these small differences modify SM rank, and subsequent operations lead to a significant difference in the individual SM capacitor voltages.
- Moreover, average value model does not model individual submodules. Therefore, individual capacitor voltages are not available from this model.

Single phase to ground fault - External Dynamics

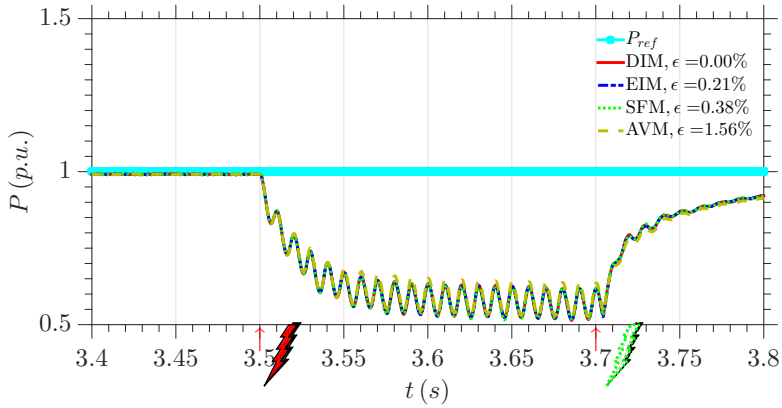


Figure 9.53: Real Power at MMC ac-side

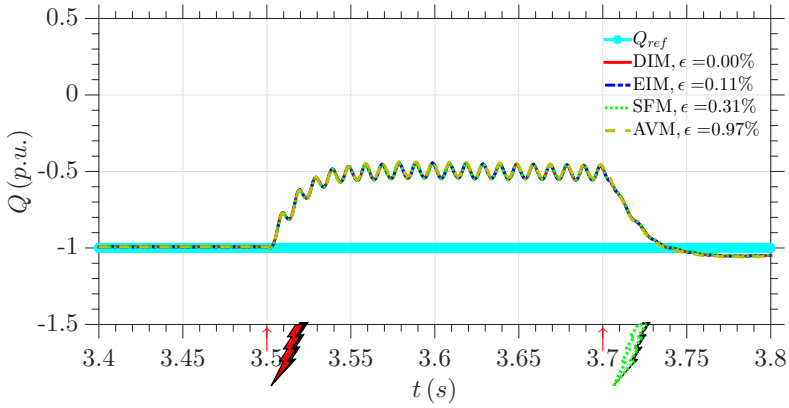


Figure 9.54: Reactive Power at MMC ac-side

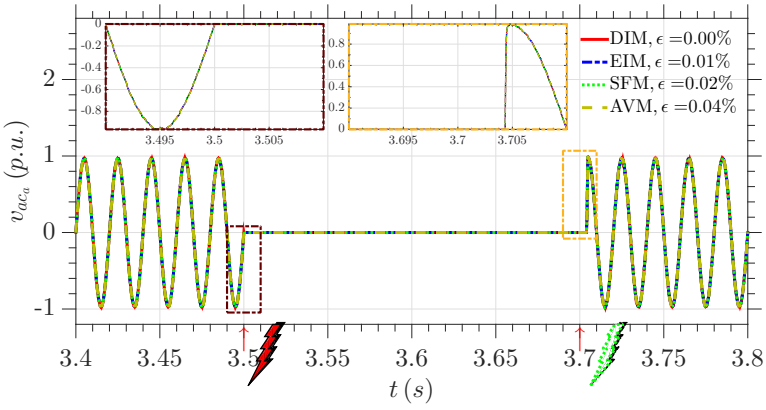


Figure 9.55: Phase a ac voltages at MMC terminals

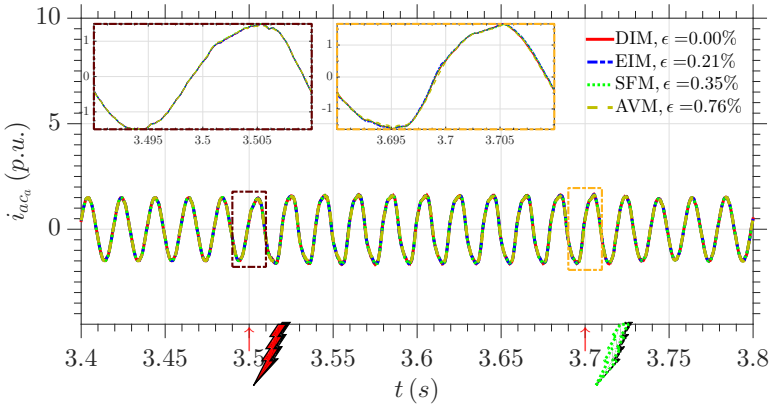


Figure 9.56: Phase a ac currents

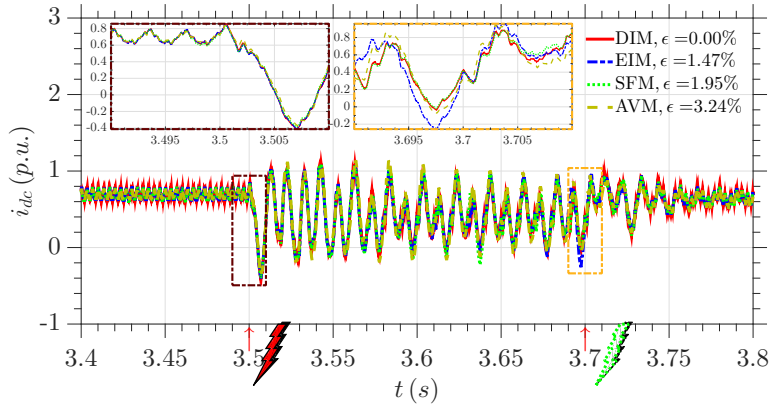


Figure 9.57: Current from dc side

Figures 9.53 to 9.57 present the terminal dynamics of converter under the single line to ground fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal:

- Near identical results for the detailed ideal model (DIM) and equivalent ideal model (EIM) with *normalized mean absolute error* of less than 1.5%. The minuscule differences in DIM and EIM are due to the absence of interpolations in EIM's calculation of arm equivalents and the rest of converter.
- Switching function model reproduces dynamics with high accuracy with *normalized mean absolute error* of less than 2.0%. Similar to EIM, absence of interpolations in the calculation of arm equivalent and binary representation for switches yields a slightly higher deviation from DIM.
- Average value model, despite its simplified representation, yield simulation results with high accuracy with *normalized mean absolute error* of less than 3.5%.

Single phase to ground fault - Internal Dynamics

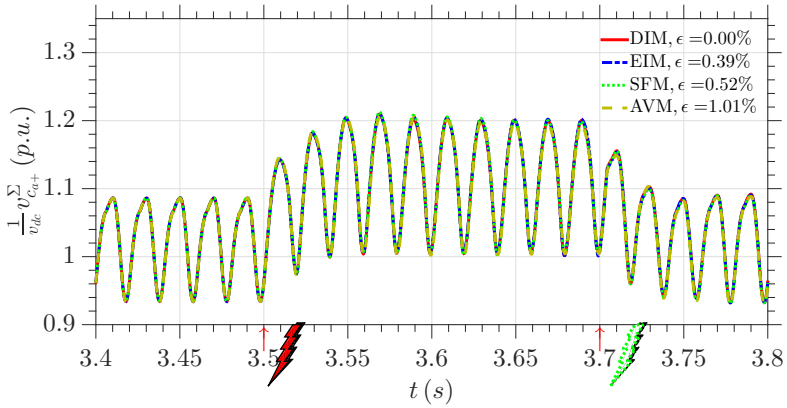


Figure 9.58: Cumulative capacitor voltage positive arm phase-a

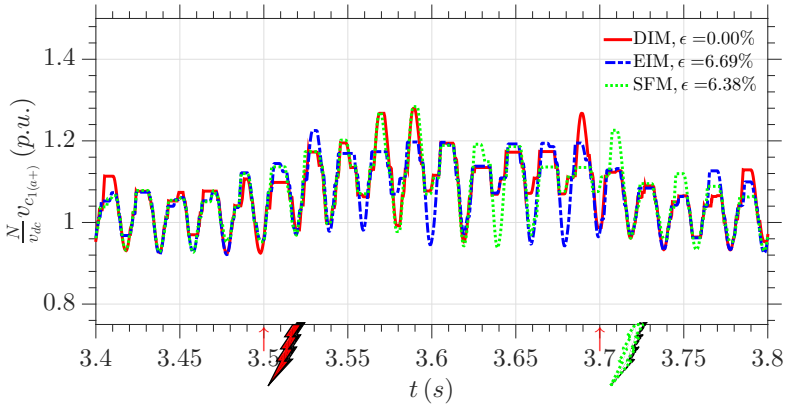


Figure 9.59: First Capacitor Voltage positive arm phase-a

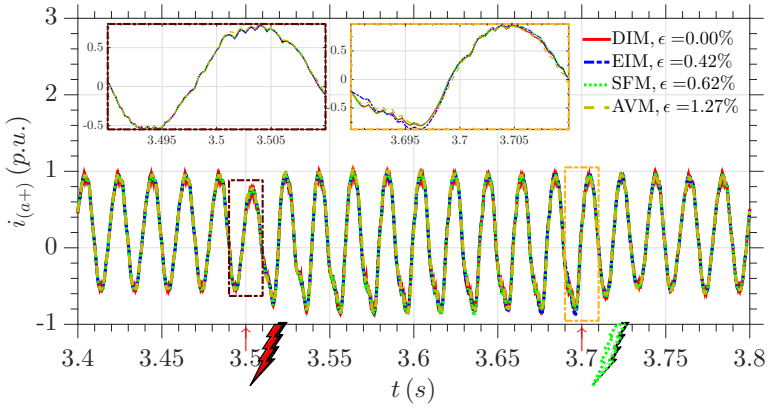


Figure 9.60: Positive arm Current phase-a

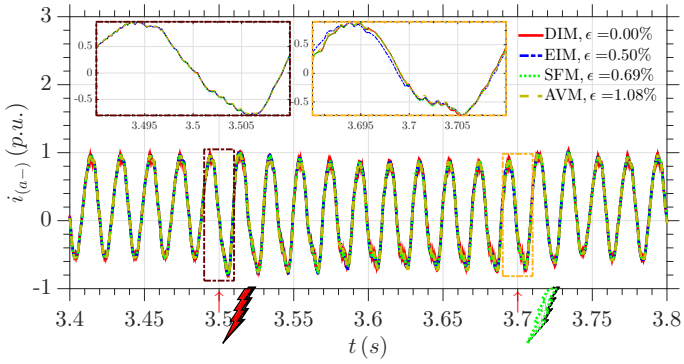


Figure 9.61: Negative arm Current phase-a

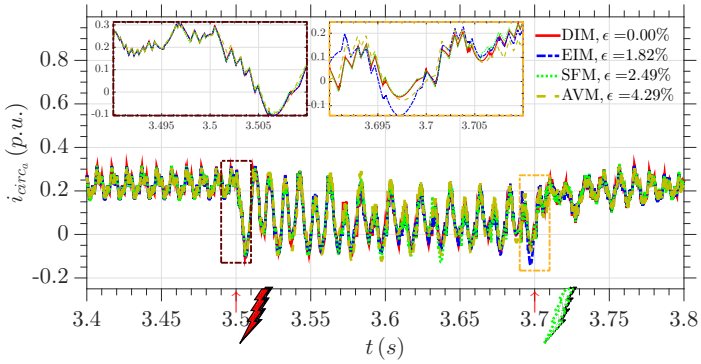


Figure 9.62: Circulating current phase-a

Figures 9.58 to 9.62 present internal dynamics of converter under the SLG fault.

- Simulation results reveal near identical results for internal currents of MMC for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $1.8, 2.5$ & 4.3% respectively.
- Similarly, cumulative capacitor voltage in an arm is modeled with reasonable accuracy for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $0.4, 0.5$ & 1.0% respectively.
- However, as seen from fig. 9.59 for individual capacitor voltages, SFM and EIM tend to deviate significantly from DIM with *normalized mean absolute error* of around than 6.7 & 6.4% respectively. The reason for this deviation is attributed to an accumulation of slight differences in the solution of EIM and SFM due to the absence of interpolations in a calculation of arm equivalent and rest of the converter. For most dynamics, this delay results in a minuscule difference in solution. However, for capacitor voltage balancing based on voltage sorting algorithm, these small differences modify SM rank and subsequent operation which leads to a significant difference in capacitor voltages.
- Average value model does not model individual submodules. Therefore, individual capacitor voltages are not available from this model.

Pole to Pole DC fault - External Dynamics

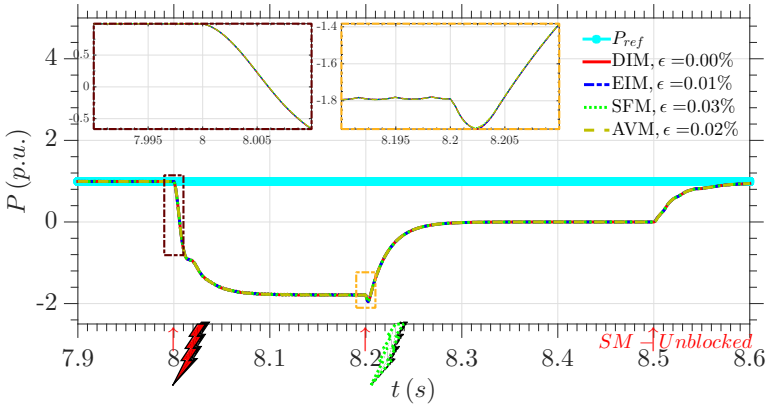


Figure 9.63: Real Power at MMC ac-side

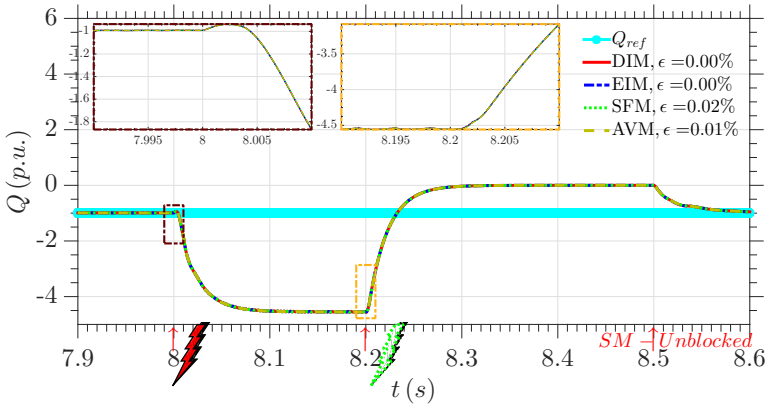


Figure 9.64: Reactive Power at MMC ac-side

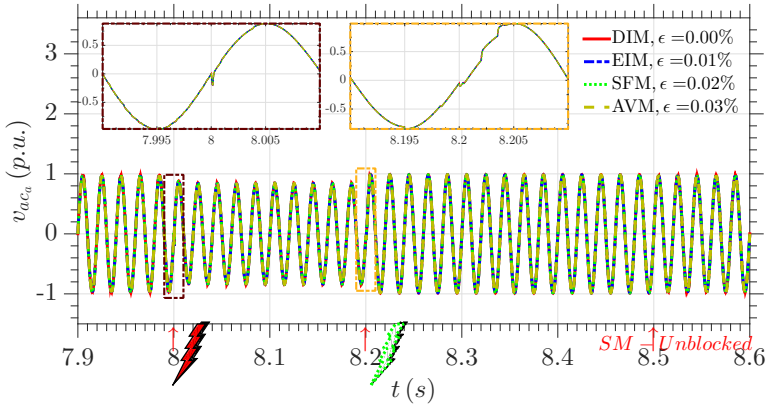


Figure 9.65: Phase a ac voltages at MMC terminals

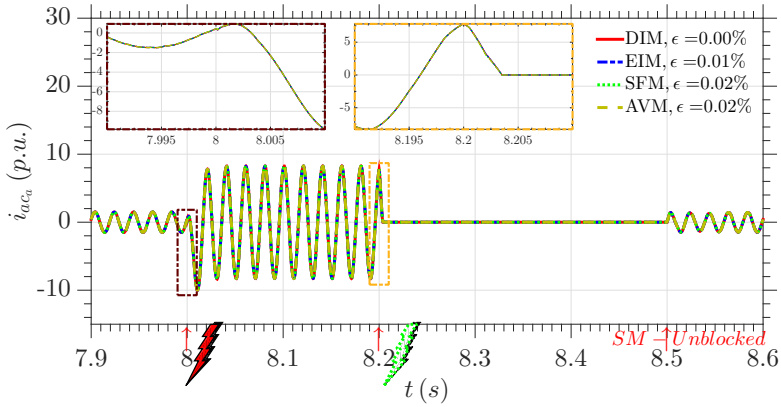


Figure 9.66: Phase a ac currents

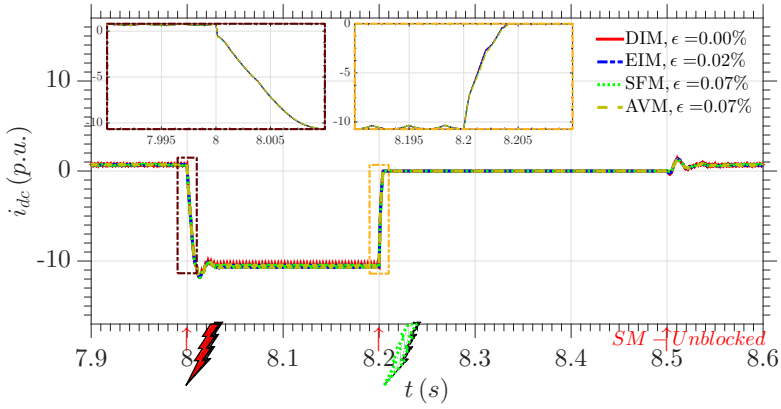


Figure 9.67: Current from dc side

Figures 9.63 to 9.67 present the terminal dynamics of the converter under pole to pole dc fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal:

- Near identical results for the detailed ideal model (DIM) and equivalent ideal model (EIM) with *normalized mean absolute error* of less than 0.01%. The minuscule differences in DIM and EIM are due to the absence of interpolations in EIM's calculation of arm equivalents and the rest of converter. Switching function model reproduces dynamics with high accuracy with *normalized mean absolute error* of less than 0.07%. Similar to EIM, absence of interpolations in the calculation of arm equivalent and binary representation for switches yields a slightly higher deviation from DIM.
- Average value model, despite its simplified representation, yield simulation results with high accuracy with *normalized mean absolute error* of less than 0.07%.

Pole to Pole DC fault - Internal Dynamics

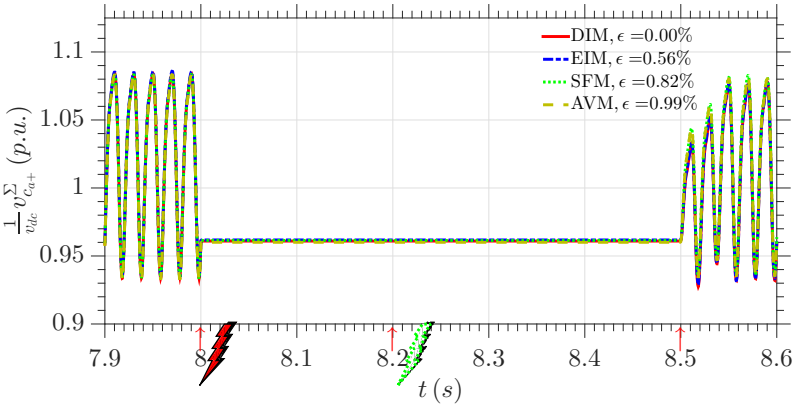


Figure 9.68: Cumulative capacitor voltage positive arm phase-a

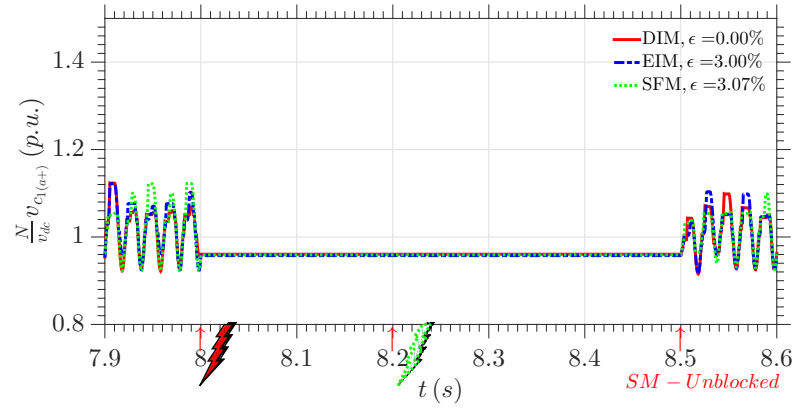


Figure 9.69: First Capacitor Voltage positive arm phase-a

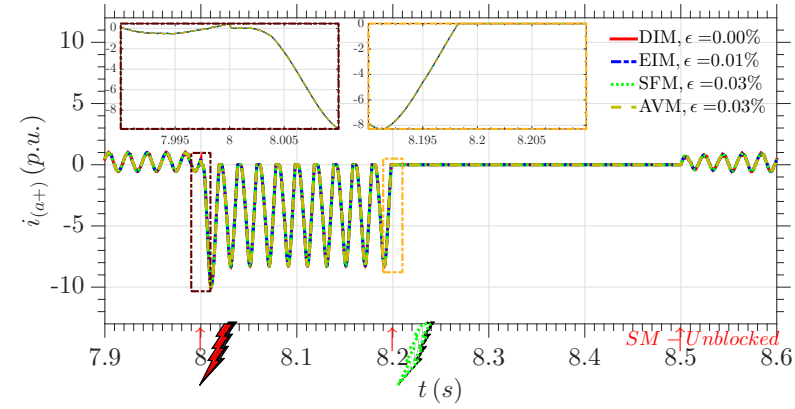


Figure 9.70: Positive arm Current phase-a

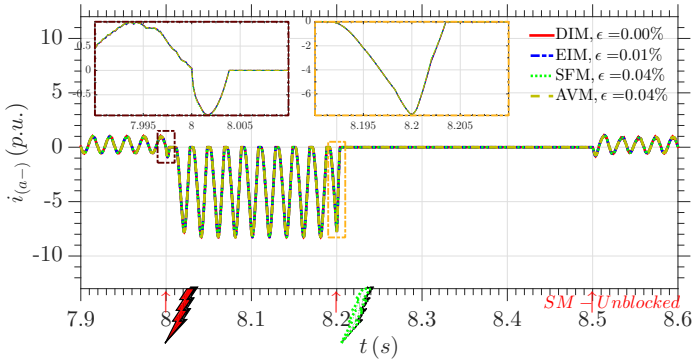


Figure 9.71: Negative arm Current phase-a

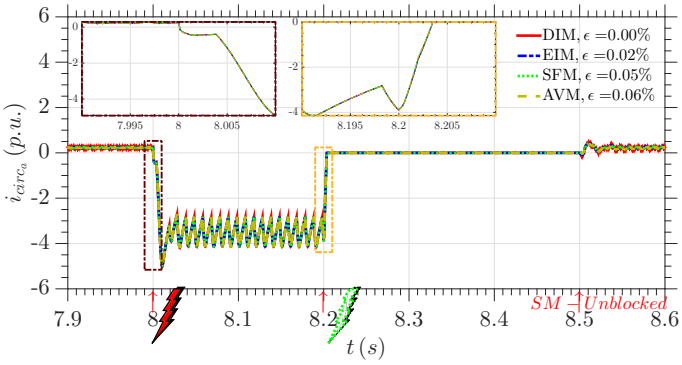


Figure 9.72: Circulating current phase-a

Figures 9.68 to 9.72 present the internal dynamics of converter under PPDC fault.

- Simulation results reveal near identical results for internal currents of MMC for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $0.02, 0.05$ & 0.06% respectively.
- Similarly, cumulative capacitor voltage in an arm is modeled with reasonable accuracy for SFM, EIM, and AVM against DIM of the converter with *normalized mean absolute error* of less than $0.6, 0.8$ & 1.0% respectively.
- However, as seen from fig. 9.69 for individual capacitor voltages, SFM and EIM tend to deviate significantly from DIM with *normalized mean absolute error* of around than 3 & 3.1% respectively. The reason for this deviation is attributed to the accumulation of slight difference in the solution of EIM and SFM due to the absence of interpolations in the calculation of arm equivalent and rest of the converter. For most dynamics, this delay results in a minuscule difference in solution. However for capacitor voltage balancing based on voltage sorting algorithm, these small differences modify SM rank and subsequent operation which leads to a significant difference in capacitor voltages.
- Since the average value model does not model individual sub-modules, individual capacitor voltages are not available from this model.

9.2.2. Model Acceleration

To observe the computational efficiency of the proposed models, the $12s$ simulation of the system (table 9.14 and fig. 9.42), undergoing various set-points changes of real/reactive power and faults, was conducted with the number of SM between 2 to 200. The simulation time step was selected as of $10\mu s$ and 48 core Microsoft Windows Server 2012 running PSCAD version 4.6 using GFortan $4.2.1$ was utilized. Figure 9.73 illustrates the execution time for the T-III DIM, T-IV TEM, T-V SFM and T-VI AVM.

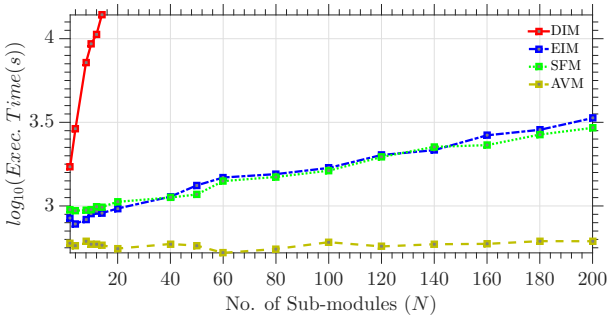


Figure 9.73: Computational burden of MMC models

Figure 9.73 show a superior computational efficiency of the proposed models against a detailed model of the converter. TEM and SFM with similar representation offers a similar computational load which offers 20 times higher computational speed than a detailed model for $N = 14$. Whereas, AVM has a constant computational load corresponding to a $N = 1$ SFM irrespective of the number of submodules.

9.2.3. Conclusion

The conclusion drawn from these simulation are summarized in tables 9.15 and 9.16.

Table 9.15: EMT Simulation accuracy

Model Type	External Parameters	Internal Parameters	Over-all Accuracy	Computational Efficiency
DIM	✓	✓	★★★★★	★★★★★
EIM	✓	✓	★★★★★	★★★★★
SFM	✓	✓	★★★★★	★★★★★
AVM	✓	✗	★★★★★	★★★★★

Table 9.16: EMT Model Use

Type	Models
DIM	External & Internal dynamics for stationary state or internal & external faults. Model all levels of control.
EIM	External & Internal dynamics for stationary state or external faults. Model all levels of control. Can't model internal faults.
SFM	External & Internal dynamics for stationary state or external faults. Model all levels of control. Can't model internal faults.
AVM	External & few Internal dynamics for stationary state or external fault. AVM don't provide information for individual sub-module.

9.3. Application of Models

9.3.1. HVDC transmission system

This section presents a simulation comparison of simplified EMT Models as presented in section 8.5 in a symmetric monopole HVDC transmission as illustrated in fig. 9.74. The parameters of the system are detailed in table 9.17. DC cables are modeled using PSCAD's frequency dependent (phase) model. Table 9.18 and fig. 9.75 summarizes the parameters and dimensions of the cable [19].

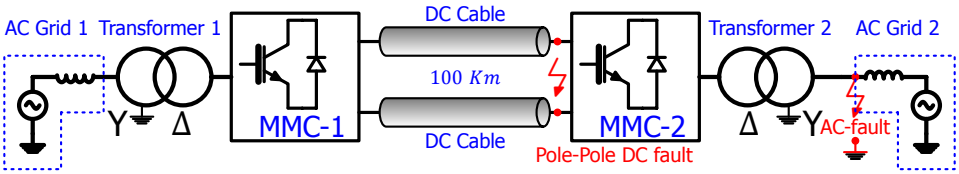


Figure 9.74: Symmetric monopole HVDC transmission - schematic

Table 9.17: System Parameters

MMC-1,2:	$N = 140$ $L_{arm} = 11.68\%$	$C = 10.5\ mF$ $R_{arm} = 0.1\Omega$
AC Grid 1,2:	$v_{ac} = 110kV$	$X_{grid} = 2.0\%$
DC Link:	$v_{dc} = 200kV$	$S_{rated} = 150MVA$
Transformer 1,2:	$\Delta - Y$ (1:1)	$L_{tf} = 3\%$

Table 9.18: DC Cable parameters

Core Conductor	$\rho = 1.84e{-}8\ \Omega m$	$\mu_r = 1$
Insulator 1	$\epsilon_r = 2.3$	$\mu_r = 1$
Sheath	$\rho = 2.14e{-}7\ \Omega m$	$\mu_r = 1$
Insulator 2	$\epsilon_r = 2.3$	$\mu_r = 1$
Armour	$\rho = 1.38e{-}7\ \Omega m$	$\mu_r = 10$
Insulator 3	$\epsilon_r = 2.3$	$\mu_r = 1$

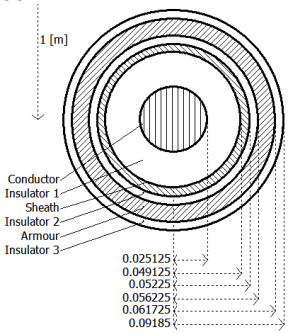


Figure 9.75: HVDC cable cross-section

The simulation in this section are presented in three parts as follows:

1. Power reversal Operation of MMC -2 $(t = 1.995 - t = 2.15s)$
   This simulation presents dynamics of system with MMC -2 undergoing a step change in set point of P, power exchange with ac grid, from $0.75\ p.u.$ to $-1.0\ p.u.$ at $t = 2.0s$.

2. Single-line to ground fault $(t = 3.4 - t = 3.8s)$
   This simulation presents dynamics of system with MMC -2 under ac-fault conditions, a $200ms$ single phase to ground fault at phase *a* of converter transformer through a small resistance at $t = 3.5s$.

3. Pole to pole DC fault $(t = 7.9 - t = 8.6s)$
   This simulation presents dynamics of of system with MMC -2 under dc-fault conditions, a $200ms$ pole to pole dc fault at $t = 8.0s$. In this case both MMC-1 and MMC-2 are blocked with a delay of $1ms$ step and ac breakers are opened with a delay of 2 cycles. After fault removal both ac breakers are closed and MMC-1 unblocked with a delay of $100ms$ while MMC-2 is unblocked after an additional delay of $200ms$.

Power reversal simulation - External Dynamics

The simulations results present the state operation of MMC-2 undergoing power reversal under balanced conditions.

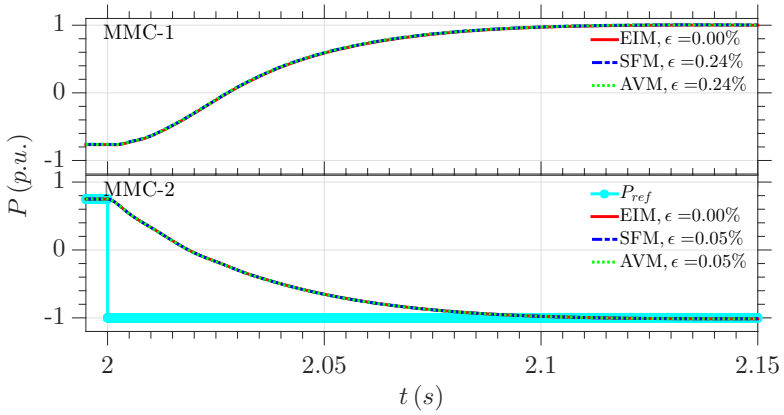


Figure 9.76: Real Power at MMC ac-side

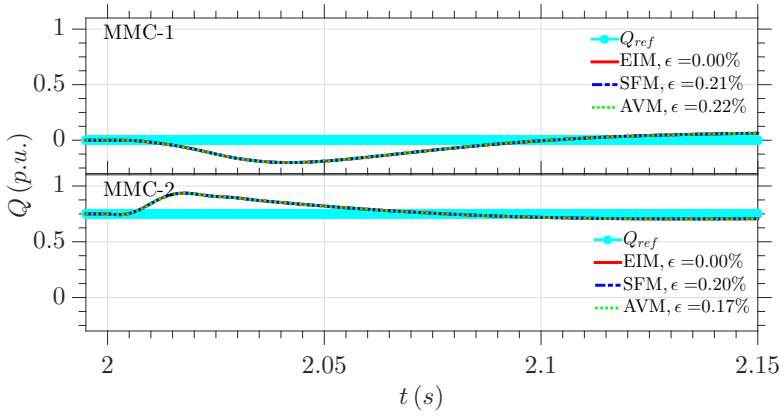


Figure 9.77: Reactive Power at MMC ac-side

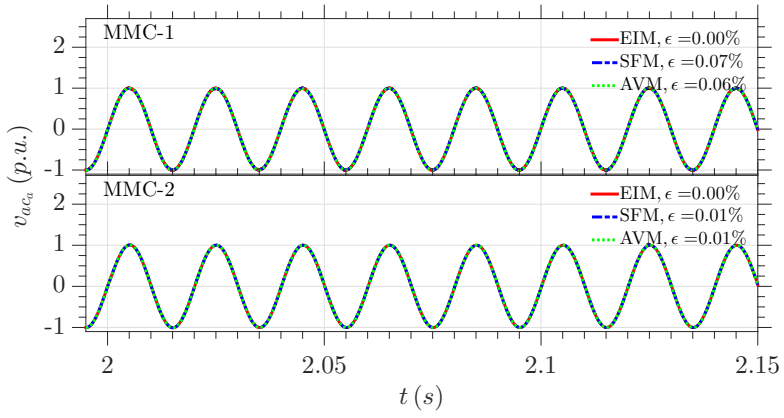


Figure 9.78: Phase a ac voltages at MMC terminals

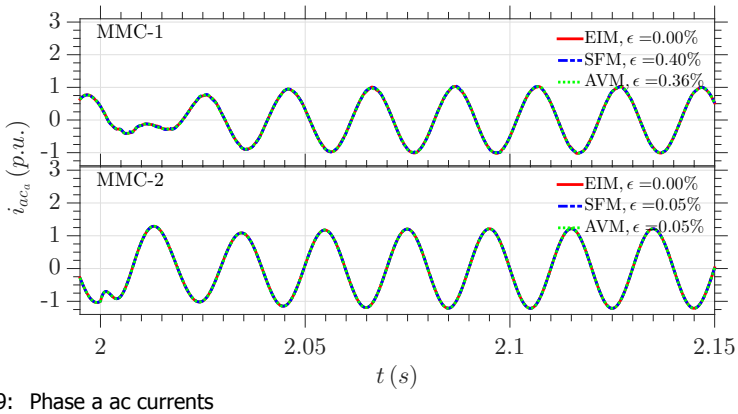


Figure 9.79: Phase a ac currents

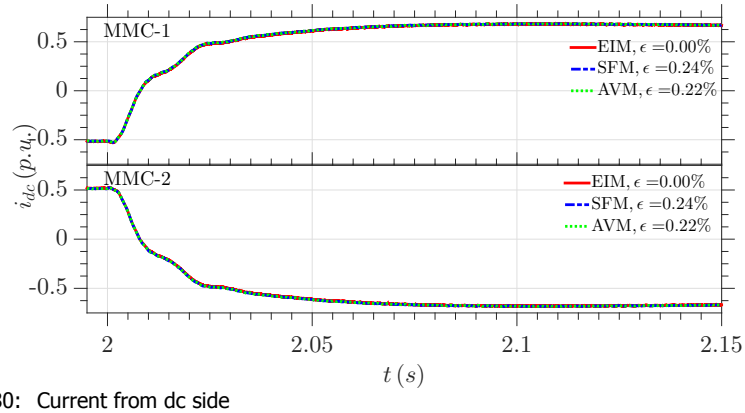


Figure 9.80: Current from dc side

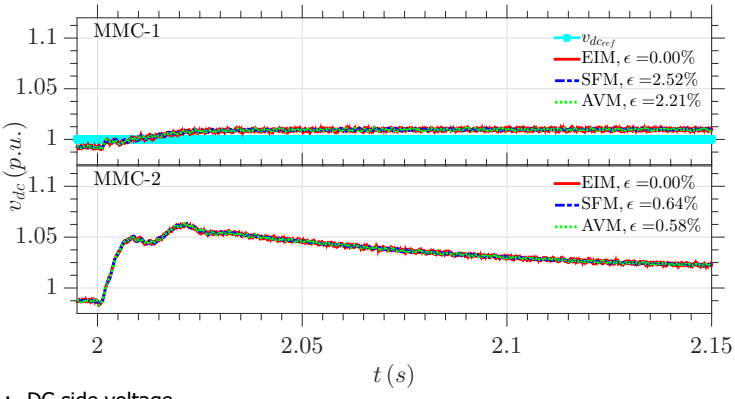


Figure 9.81: DC side voltage

Figures 9.76 to 9.81 present the terminal dynamics of the converter under power reversal. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

Power reversal simulation - Internal Dynamics

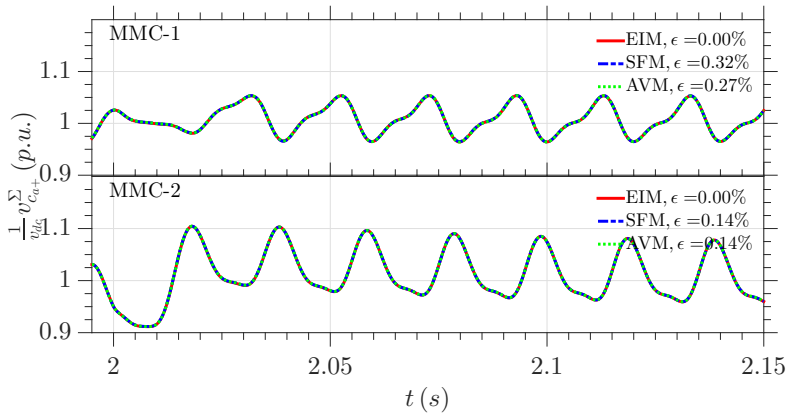


Figure 9.82: Cumulative capacitor voltage positive arm phase-a

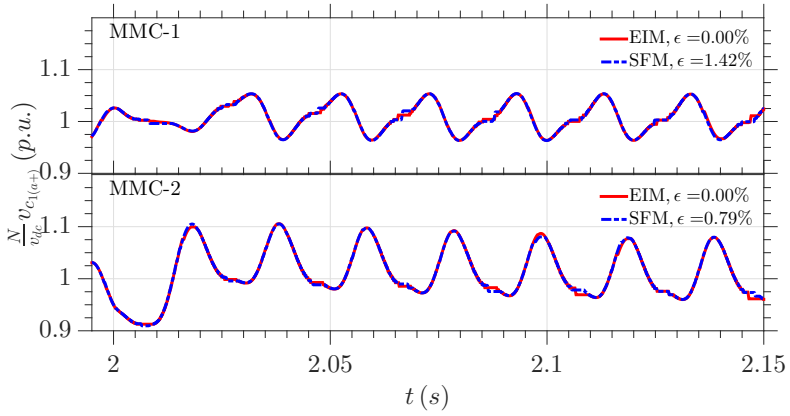


Figure 9.83: First Capacitor Voltage positive arm phase-a

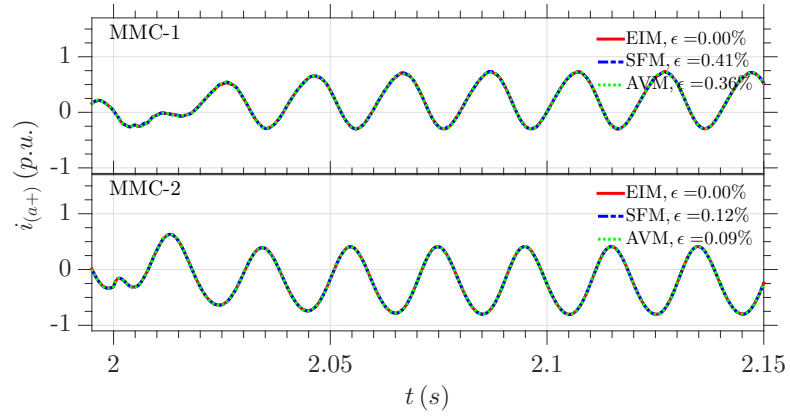


Figure 9.84: Positive arm Current phase-a

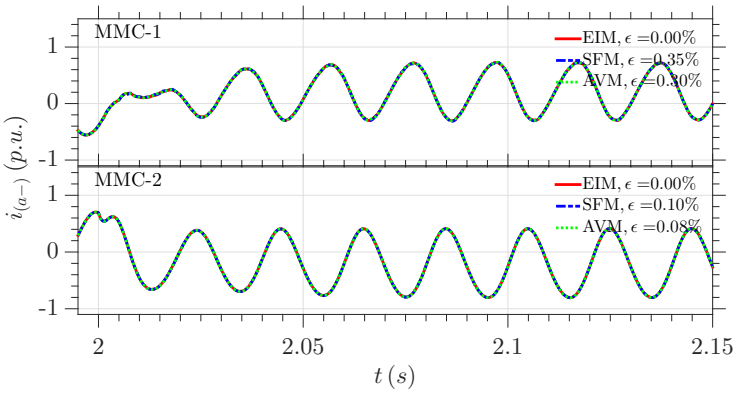


Figure 9.85: Negative arm Current phase-a

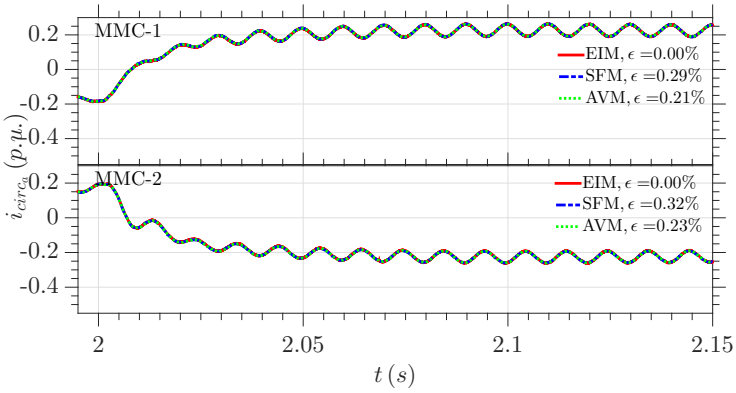


Figure 9.86: Circulating current phase-a

Figures 9.82 to 9.86 present the internal dynamics of the converter under power reversal. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

Single phase to ground fault - External Dynamics

The simulation results present the state operation of MMC-2 under the single line to ground fault.

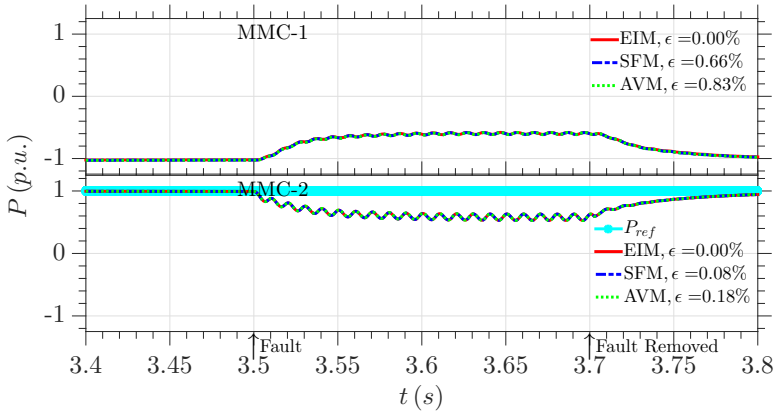


Figure 9.87: Real Power at MMC ac-side

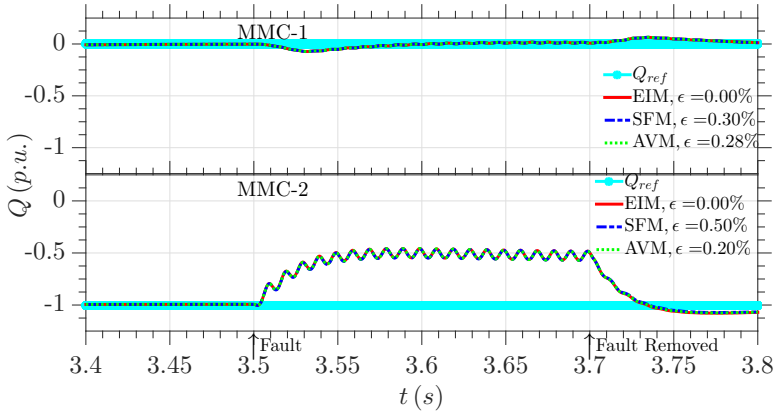


Figure 9.88: Reactive Power at MMC ac-side

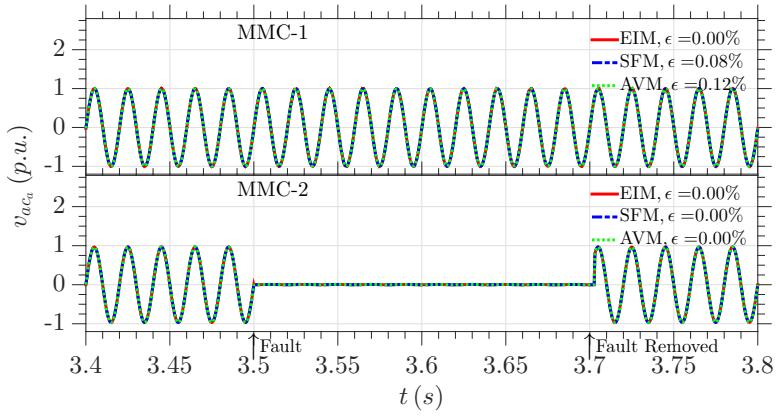


Figure 9.89: Phase a ac voltages at MMC terminals

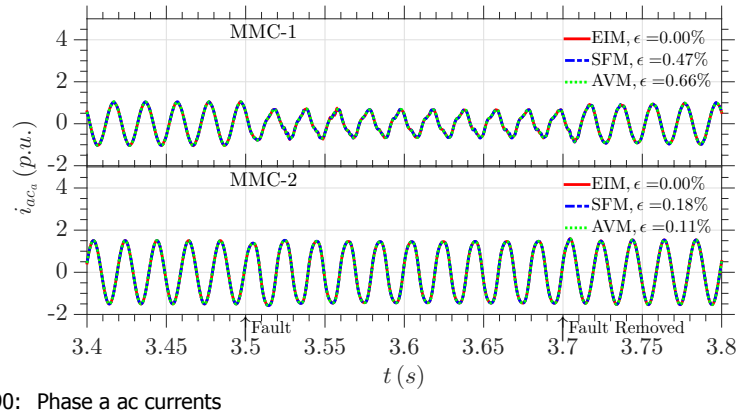


Figure 9.90: Phase a ac currents

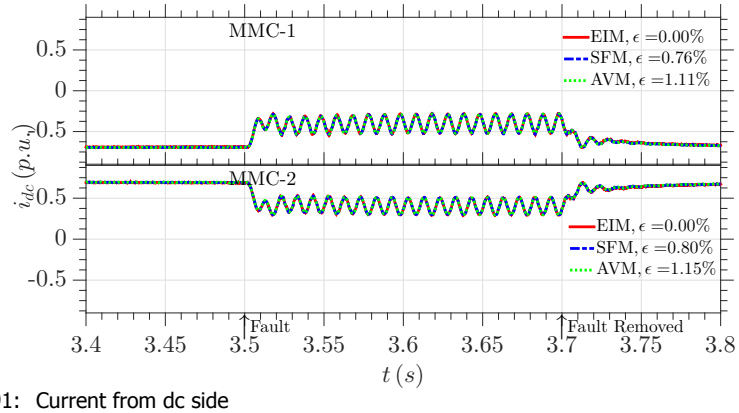


Figure 9.91: Current from dc side

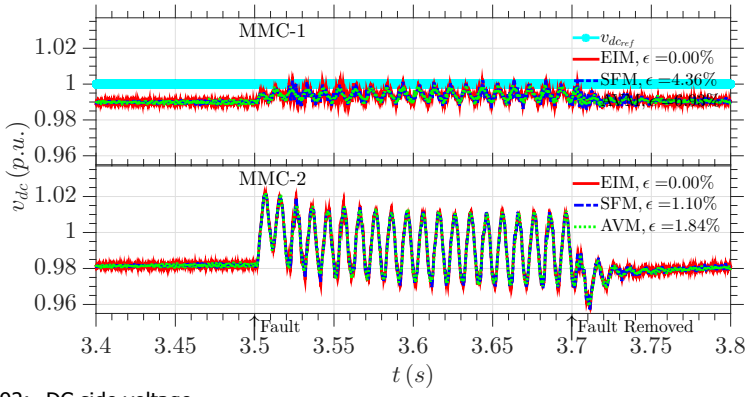


Figure 9.92: DC side voltage

Figures 9.87 to 9.92 present the terminal dynamics of the converter under single line to ground fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

Single phase to ground fault - Internal Dynamics

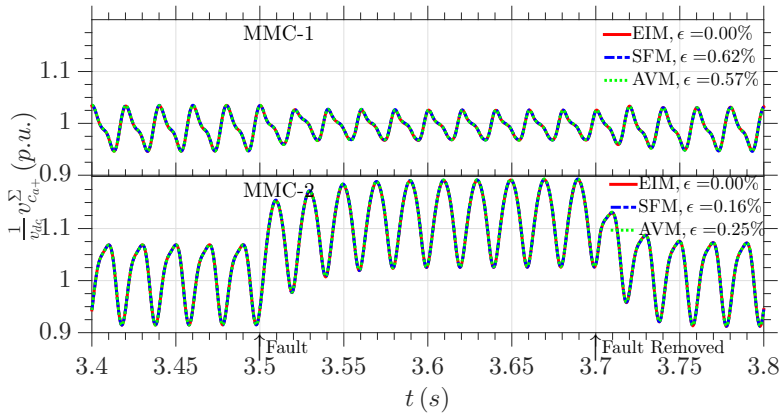


Figure 9.93: Cumulative capacitor voltage positive arm phase-a

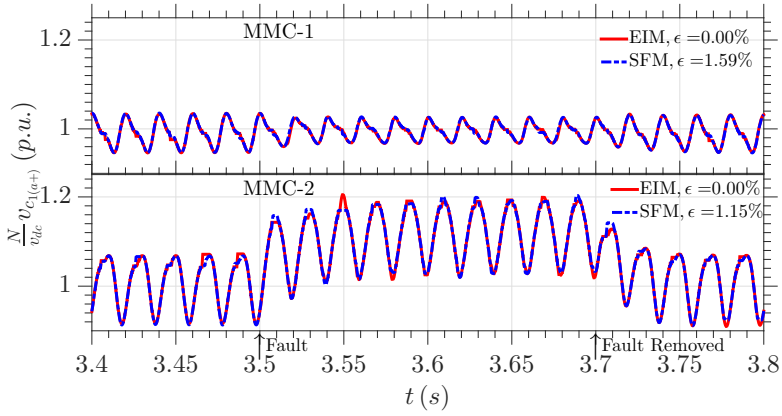


Figure 9.94: First Capacitor Voltage positive arm phase-a

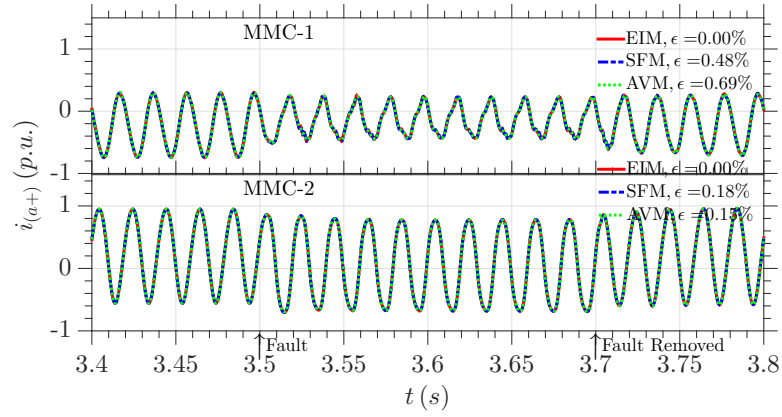


Figure 9.95: Positive arm Current phase-a

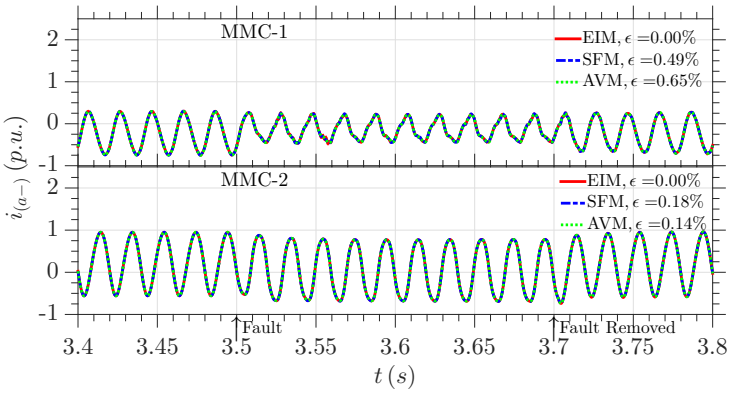


Figure 9.96: Negative arm Current phase-a

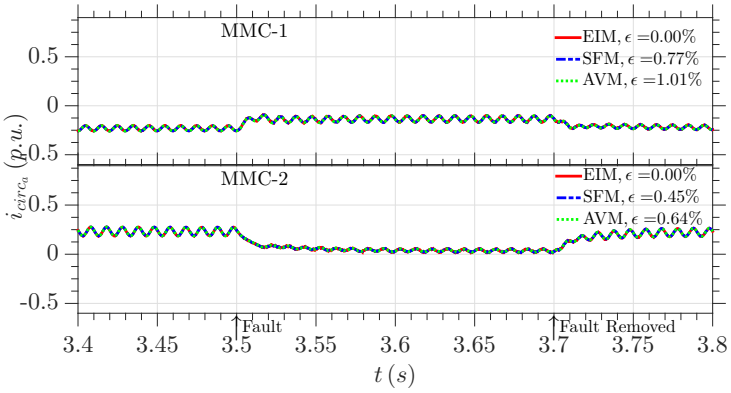


Figure 9.97: Circulating current phase-a

Figures 9.93 to 9.97 present the internal dynamics of the converter under single line to ground fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

Pole to Pole DC fault - External Dynamics

The simulation results present the state operation of MMC-2 under the pole to pole dc fault.

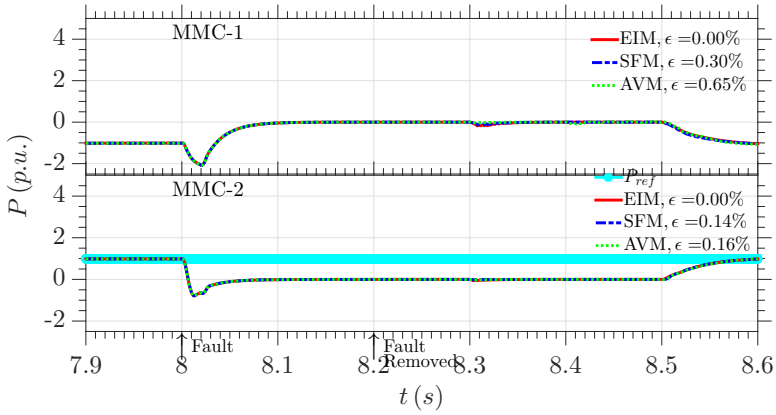


Figure 9.98: Real Power at MMC ac-side

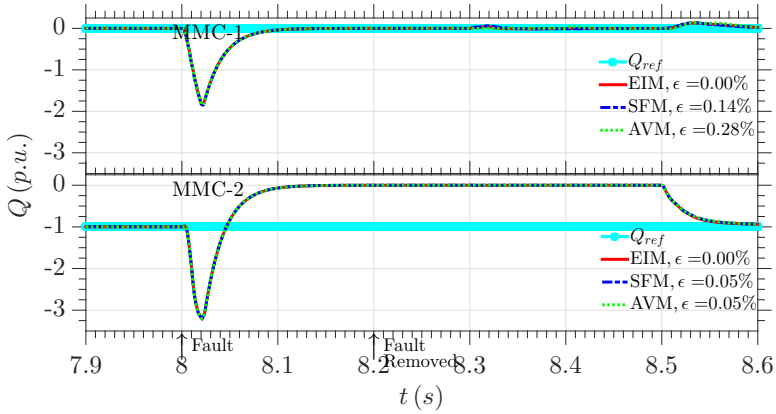


Figure 9.99: Reactive Power at MMC ac-side

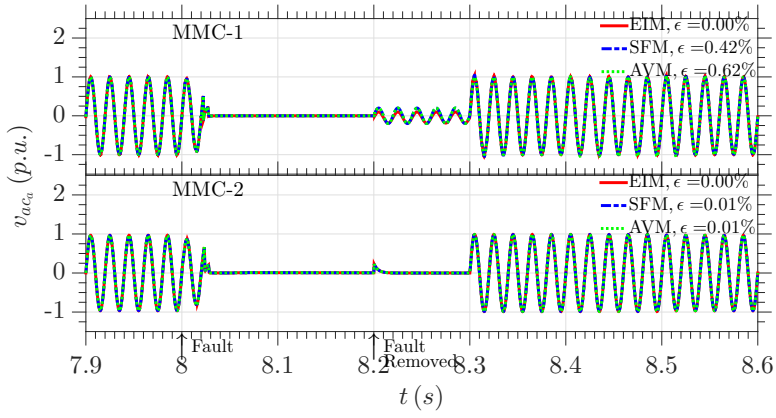


Figure 9.100: Phase a ac voltages at MMC terminals

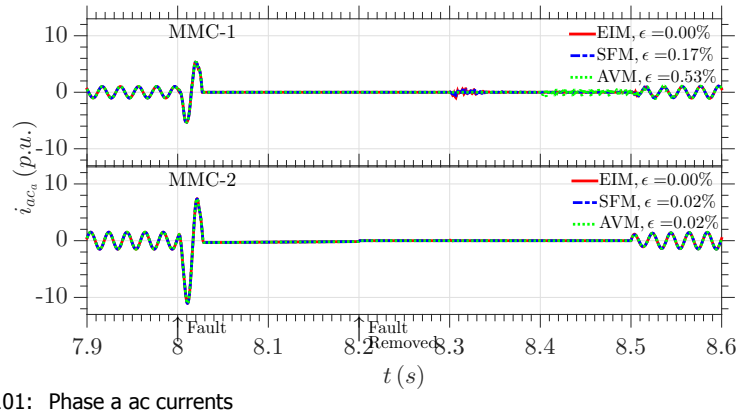


Figure 9.101: Phase a ac currents

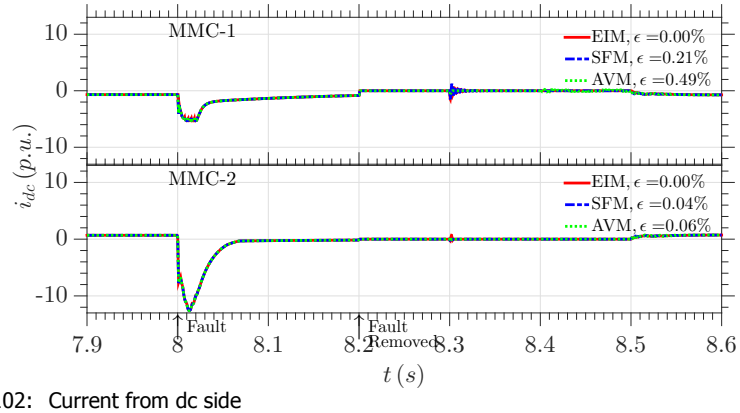


Figure 9.102: Current from dc side

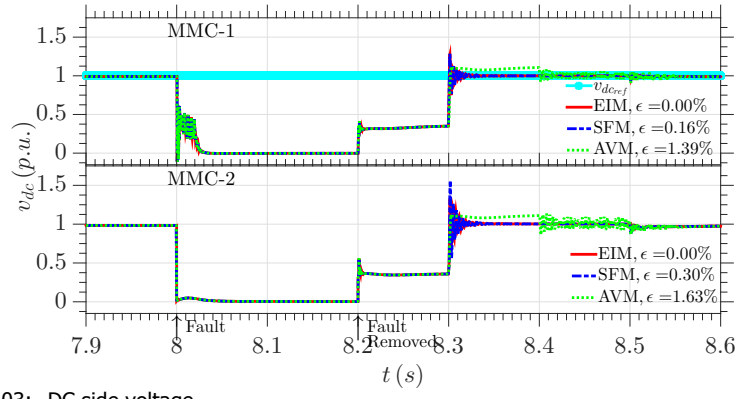


Figure 9.103: DC side voltage

Figures 9.98 to 9.103 present the terminal dynamics of the converter dynamics of converter under the pole to pole dc fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

Pole to Pole DC fault - Internal Dynamics

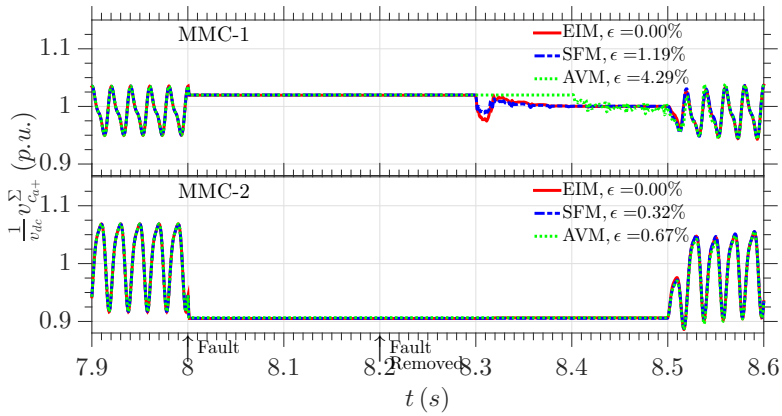


Figure 9.104: Cumulative capacitor voltage positive arm phase-a

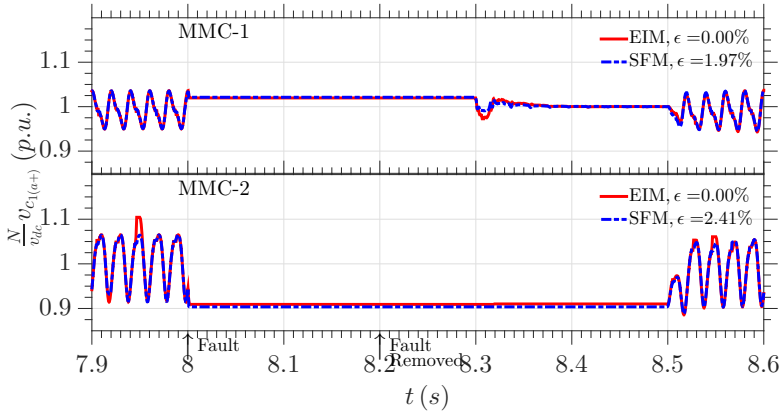


Figure 9.105: First Capacitor Voltage positive arm phase-a

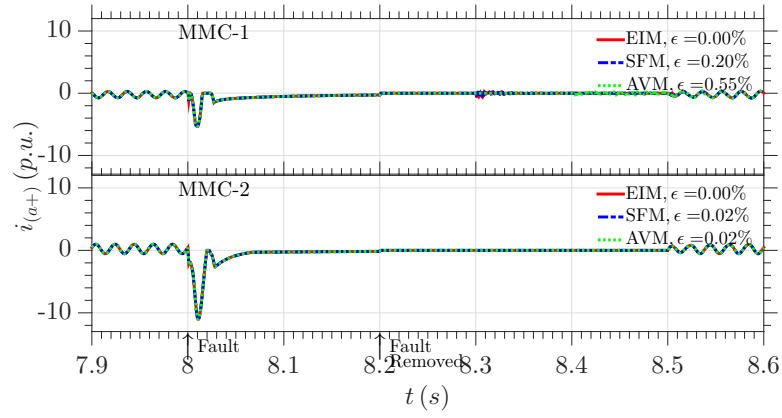


Figure 9.106: Positive arm Current phase-a

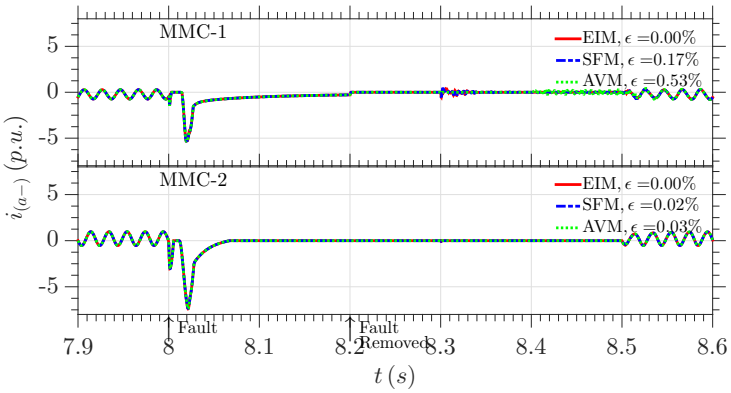


Figure 9.107: Negative arm Current phase-a

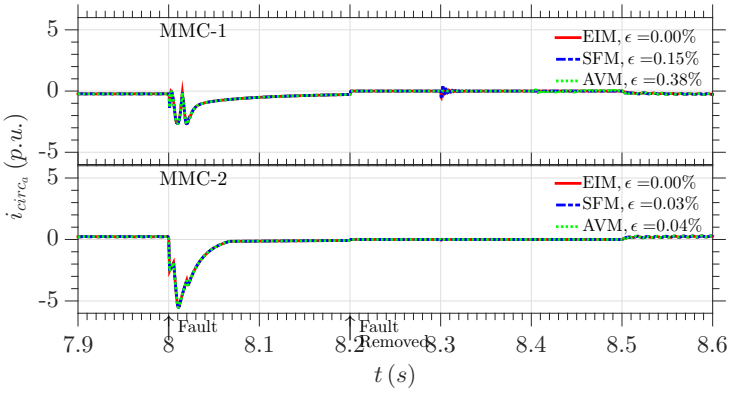


Figure 9.108: Circulating current phase-a

Figures 9.104 to 9.108 present the internal dynamics of the converter under the pole to pole dc fault. Comparison of terminal parameters i.e. voltage, current on ac-side and dc-current for all models reveal the accuracy of AVM and SFM against EIM.

9

Computational load

The relative computational load of the equivalent models is summarized in table 9.19.

Table 9.19: Relative Computational Load

	EIM	SFM	AVM
Relative Computational Load	4.0	3.0	1.0

10

Discussion and Conclusion

Modular multilevel converters, with its numerous advantages over conventional converter technologies, is gradually becoming the preferred choice for HVDC power transmission, multi-terminal HVDC systems and renewable energy applications such as offshore wind farms. However, modeling of MMCs with explicit representation of each semiconductor device, using classical simulation techniques, presents enormous computational burden. This makes the simulation of MMCs, especially within a large power system, unrealizable. Therefore, this thesis focuses on the computationally efficient equivalent models for EMT simulation of MMCs.

The thesis starts with the development of a continuous mathematical model of the converter. Even though the continuous model only captures *inserted* and *bypassed* states of the converter, it serves to analyze the operation of individual sub-modules, arms, and converter as a whole. Based on the continuous model a linear time invariant model for the converter was derived. Using the LTI model a DQ domain controller, for the independent control of real power/ dc voltage and reactive power/ ac voltage of the grid-connected converter, was developed and tuned.

Analysis of instantaneous energy in phase leg based on the continuous mathematical model revealed the presence of harmonics in circulating current between phase legs. Subsequently, using this continuous model a circulating current suppression controlled to suppress the dominant second order harmonic was developed. In addition to this based on results from the continuous model, modulation schemes for control of arm and individual sub-modules were evaluated in the thesis. In short, the continuous model provides a suitable mathematical formulation for the design of control and modulation scheme of the converter.

The specific objective of the thesis was the development of MMC models for EMT studies. These models are expected to reproduce internal and external dynamic of MMC under stationary and transient conditions. Therefore, building on the existing literature, the thesis proposed various equivalent models of MMC that inherently

capture all operating states of the converter and allow for the natural development of internal and external dynamics of the converter. The models investigated here are broadly categorized as follows:

- Models based on classical EMT representation:
  In this modeling scheme, each semiconductor device is explicitly modeled, and solver utilizes nodal admittance method to resolve the system. Based on the representation of semiconductor devices, from full-physics representation to a bi-value resistor, these models are subdivided into three types, referred as T-I – T-III in the thesis. The modeling scheme solves entire system simultaneous and offers the highest accuracy but has the highest computational load.

  For simulation purposes, a detailed model for MMC for up to 14 sub-modules per arm with bi-value resistor representation for semiconductor devices was developed in PSCAD/EMTDC, which serves as the benchmark for the simplified equivalent models.

- Equivalent models with individual sub-module representation:
  This modeling method individually considers all sub-modules and models them in a computationally efficient representation that captures dynamics of all sub-modules. These models are sub-categorized as:

  – T-IV Isolated sub-module model
    Here sub-modules are modeled as isolated sub-system where a dependent current source mimics the arm currents and arms are modeled with a dependent voltage source corresponding to the cumulative voltage across all sub-modules. In this modeling approach, all of the semiconductor device in sub-modules are explicitly modeled, and solver utilizes nodal admittance method to resolve the each sub-module independently, achieving superior computation speed by solving numerous small matrices instead of a single large matrix. However, this modeling approach results in an artificial delay in the system i.e. a change in SM is incorporated in arm with a delay of one-time step and vice-versa.

    Due to the limitation of the number of nodes in the PSCAD/EMTDC's educational version this modeling scheme is not simulated.

  – T-V Equivalent ideal model
    This model utilizes a Thevenin's equivalent representation for all sub-modules in an arm and achieves superior computational scheme by utilizing linear algebraic operations for modeling of individual sub-modules instead of matrix operations in nodal admittance method. This representation does not utilize interpolation algorithms to track switching instants during nominal operation of SM. Blocked state in this model is modeled through additional IGBTs and diode.

  – T-VI Switching function model
    This model is similar to T-V EIM but here switching operation is modeled with boolean functions instead of switched resistor. Furthermore, unlike existing switching function and average models in the literature, which utilize fictitious diodes and switches to mimic *blocked* state of operation, the proposed mod-

els reproduce entire operation of the converter using logical functions alone, while preserving precise representation and computational efficiency. Moreover, an algorithmic method, rather than an iterative approach, to determine the operation of SMs after the first instance of blocked state was presented.

- Equivalent model with unified representation for all sub-modules:
  This model referred as T-VII assumes identical design of all sub-module and ideal voltage balancing control. Based on this, represents all sub-modules in an arm by a single equivalent sub-module. This offers superior computational speed at the expense of loss of dynamics for individual sub-modules.

These equivalent models were simulated under various transient conditions using PSCAD/EMTDC. The simulations demonstrate the ability of proposed models to capture internal and external dynamics of the converter under stationary and transient conditions with high accuracy and computational efficiency. Furthermore, the ability of equivalent models to simulate large systems was verified through an HVDC transmission link.

Based on the design of models and simulation results the applications for the equivalent models are summarized in table 10.1. The proposed equivalent models with individual sub-module representation can replace detailed model for system-level studies. While, the average value model with an equivalent module representation, scalable to any number of sub-modules without any impact on computational speed, offers a relatively accurate representation for studies focused on terminal characteristics of the converter.

Table 10.1: Simulation Application

Model	Type	Application
Detailed	T-I–T-II	Component level studies e.g. switching losses, component optimization, EMC validation. And simplified model validation. Simulate internal and external faults.
Detailed Ideal	T-III	System level studies e.g. control & protection system design, harmonics studies. And simplified model validation. Simulate internal and external faults.
Isolated SM	T-IV	System level studies e.g. control & protection system design, harmonics studies. Simulate internal and external faults.
Equivalent ideal	T-V	System level studies e.g. control & protection system design, harmonics studies. Simulate external faults only.
Switching function	T-VI	System level studies e.g. control & protection system design, harmonics studies. Simulate external faults only.
Average value	T-VII	Network level studies e.g. load flow analyses, design of protection relays and stability studies. Simulate external faults only.

Model Accuracy ↑

Computational Speed ↓

10.1. Future work

This thesis only presents equivalent models for half bridge sub-modules and validates them against a detailed model of the converter.

Suggested future works in this area are:

- Implementation of laboratory setup of MMC and benchmarking of proposed models against experimental results under stationary and transient conditions.
- Extension of the modeling techniques presented here to the full bridge and other hybrid module multilevel converters.

Appendices

A

Harmonics in circulating current

Internal dynamics of converter as derived by the continuous model (eqs. (3.56) and (3.57)) are determined by the choice of insertion index ($n_{\phi\pm}$). This chapter is dedicated to the analysis of internal dynamics of the converter with direct modulation (section 6.1.1). Capacitor voltage, voltage imbalance in phase leg and circulating current are investigated in detail in following sections. Most of the derivation presented here follows from the approach presented in [104].

In addition to the assumptions presented earlier section 3.3.1, the following analyses assume equal voltage across all capacitors in an arm. Instantaneous nature of voltage balancing control, that ensures voltage across all capacitors is within a defined limit justifies this assumption. Incorporation of this assumption in eq. (3.12) yields arm voltages as:

$$v_{(\phi\pm)}(t) = n_{\phi+} N v_{c(\phi\pm)} \tag{A.1}$$

A.1. Capacitor Voltage

Using eqs. (3.10), (3.50), (3.51), (6.3) and (6.4) voltage across a sub-module's capacitor of a phase leg is given by:

$$\begin{aligned} v_{c(\phi\pm)} &= \frac{1}{C}\int n_{\phi+} i_{(\phi\pm)} dt \\ &= \frac{1}{2C}\int (1 \mp \hat{m}_\phi \cos(\omega t + \Phi_\phi + \alpha)) \\ &\quad \left[\frac{1}{3} i_{dc}\left(1 \pm \hat{k}_\phi \cos(\omega t + \Phi_\phi - \theta)\right) + \sum_{n=1}^{\infty} \hat{i}_{\phi,n} \cos(n\omega t + \Phi_{\phi,n})\right] dt \end{aligned} \tag{A.2}$$

(A.3)

$$
\begin{aligned}
&= \frac{i_{dc}}{6\omega C}\left(\pm\hat{k}_{\phi}\sin(\omega t+\Phi_{\phi}-\theta)\mp\hat{m}_{\phi}\sin(\omega t+\Phi_{\phi}+\alpha)\right)\\
&-\frac{i_{dc}\hat{m}_{\phi}\hat{k}_{\phi}}{24\omega C}\sin(2\omega t+2\Phi_{\phi}+\alpha-\theta)\\
&+\frac{1}{2C}\sum_{n=1}^{\infty}\frac{\hat{i}_{\phi,n}}{n\omega}\sin(n\omega t+\Phi_{\phi,n})\\
&\mp\frac{\hat{m}_{\phi}}{4C}\sum_{n=1}^{\infty}\frac{\hat{i}_{\phi,n}}{(n+1)\omega}\sin((n+1)\omega t+\Phi_{\phi,n}+\Phi_{\phi}+\alpha)\\
&\mp\frac{\hat{m}_{\phi}}{4C}\sum_{n=2}^{\infty}\frac{\hat{i}_{\phi,n}}{(n-1)\omega}\sin((n-1)\omega t+\Phi_{\phi,n}-\Phi_{\phi}-\alpha)\\
&\mp\frac{\hat{m}_{\phi}}{4C}\hat{i}_{\phi,1}t\cos(\Phi_{\phi,n}-\alpha)+k_{c_{\pm\phi}}
\end{aligned}
\tag{A.4}
$$

where $k_{c_{\pm\phi}}$ denotes the initial charge on capacitor.
Average value of capacitor voltage for one switching period from eq. (A.4) is given as:

$$
\begin{aligned}
\overline{v_{c(\phi\pm)}} &= \frac{1}{T}\int_{0}^{T} v_{c(\phi\pm)}dt\\
&= \mp\frac{\hat{m}_{\phi}}{2}\hat{i}_{\phi,1}\cos(\Phi_{\phi,n}-\alpha)
\end{aligned}
\tag{A.5}
$$

From eqs. (A.4) and (A.5) it can be seen that:

- In the integral terms, the dc component in the circulating current and dc the component yielded from the product of modulation index and differential current/AC current add to zero. Hence the ac output current counterbalances the charging/discharging effect of the dc component of circulating current on submodule's capacitors [104].

- The average value over one period should be zero; $\overline{v_{c(\phi\pm)}}$ indicates the average change in the value of capacitance over one time period. For the system under stationary conditions this should equate to zero, hence from eq. (A.5) either the fundamental component in circulating current is zero or is orthogonal to reference signal i.e. phase difference of $\pm 90\,\mathrm{deg}$.

- The voltage across a capacitor is a sum of initial capacitor voltage and a ripple due to arm currents.

A.2. Harmonic in circulating current

Harmonics in circulating current stem from voltage imbalance in dc side voltage and voltage inserted in a leg as seen in eq. (3.23). Therefore to accurately determine the harmonics components, voltage imbalance in a phase leg is determined.

Using eqs. (A.1), (A.4) and (3.23) voltage inserted in a phase leg is given as:

$$
\begin{aligned}
&v_{leg_\phi} = v_{(\phi+)} + v_{(\phi-)} = N(n_{\phi+}v_{c(\phi+)} + n_{\phi-}v_{c(\phi-)}) \\
&= \frac{N}{2}[v_{c(\phi+)} + v_{c(\phi-)} + \hat{m}_\phi(v_{c(\phi-)} - v_{c(\phi+)})\cos(\omega t + \Phi_\phi + \alpha))] \\
&= \frac{N}{2C}\Big[k + \frac{\hat{m}_\phi \hat{k}_\phi}{6\omega} i_{dc}\sin(\theta+\alpha) - \frac{\hat{m}_\phi \hat{k}_\phi}{4\omega} i_{dc}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta) \\
&+ \frac{\hat{m}_\phi^2}{6\omega} i_{dc}\sin(2\omega t + 2\Phi_\phi + 2\alpha) + \sum_{n=1}^{\infty} \frac{\hat{i}_{\phi,n}}{n\omega}\sin(n\omega t + \Phi_{\phi,n}) \\
&+ \frac{\hat{m}_\phi^2}{4}\sum_{n=1}^{\infty}\frac{\hat{i}_{\phi,n}}{(n+1)\omega}\big(\sin((n+2)\omega t + \Phi_{\phi,n} + 2\Phi_\phi + 2\alpha) + \sin(n\omega t + \Phi_{\phi,n})\big) \\
&+ \frac{\hat{m}_\phi^2}{4}\sum_{n=2}^{\infty}\frac{\hat{i}_{\phi,n}}{(n-1)\omega}\big(\sin(n\omega t + \Phi_{\phi,n}) + \sin((n-2)\omega t + \Phi_{\phi,n} - 2\Phi_\phi - 2\alpha)\big)\Big]
\end{aligned}
\tag{A.6}
$$

Further simplification of eq. (A.6) & ordering with frequency content yields:

$$
\begin{aligned}
v_{leg_\phi} = \frac{N}{2C}\Big[&k + \frac{\hat{m}_\phi \hat{k}_\phi}{6\omega} i_{dc}\sin(\theta+\alpha) + \frac{\hat{m}_\phi^2}{4}\frac{\hat{i}_{\phi,2}}{\omega}\sin(\Phi_{\phi,2} - 2\Phi_\phi - 2\alpha) \\
&\frac{8+\hat{m}_\phi^2}{8\omega}\hat{i}_{\phi,1}\sin(\omega t + \Phi_{\phi,1}) + \frac{\hat{m}_\phi^2}{8\omega}\hat{i}_{\phi,3}\sin(\omega t + \Phi_{\phi,3} - 2\Phi_\phi - 2\alpha) \\
&\frac{2\hat{m}_\phi^2+3}{6\omega}\hat{i}_{\phi,2}\sin(2\omega t + \Phi_{\phi,2}) + \frac{\hat{m}_\phi^2}{12\omega}\hat{i}_{\phi,4}\sin(2\omega t + \Phi_{\phi,4} - 2\Phi_\phi - 2\alpha) \\
&- \frac{\hat{m}_\phi \hat{k}_\phi}{4\omega} i_{dc}\sin(2\omega t + 2\Phi_\phi + \alpha - \theta) + \frac{\hat{m}_\phi^2}{6\omega} i_{dc}\sin(2\omega t + 2\Phi_\phi + 2\alpha) \\
&+ \sum_{n=3}^{\infty}\frac{2(n^2-1)+n^2\hat{m}_\phi^2}{2n\omega(n^2-1)}\hat{i}_{\phi,n}\sin(n\omega t + \Phi_{\phi,n}) \\
&+ \frac{\hat{m}_\phi^2}{4}\sum_{n=3}^{\infty}\frac{\hat{i}_{\phi,n-2}}{(n-1)\omega}\sin(n\omega t + \Phi_{\phi,n-2} + 2\Phi_\phi + 2\alpha) \\
&+ \frac{\hat{m}_\phi^2}{4}\sum_{n=3}^{\infty}\frac{\hat{i}_{\phi,n+2}}{(n+1)\omega}\sin(n\omega t + \Phi_{\phi,n+2} - 2\Phi_\phi - 2\alpha)\Big]
\end{aligned}
\tag{A.7}
$$

Expressing eq. (A.7) in complex form yields:

$$
\begin{aligned}
v_{leg_\phi} &= \Re e \sum_{n=0}^{\infty} \hat{v}_{leg_{\phi,n}} e^{j\Phi_{vn}} e^{j(n\omega t)} \\
&= \frac{N}{2C} \Re e\Big[k - j\frac{\hat{m}_\phi \hat{k}_\phi}{6\omega} i_{dc} e^{j(\theta+\alpha)} - j\frac{\hat{m}_\phi^2}{4}\frac{\hat{i}_{\phi,2}}{\omega} e^{j(\Phi_{\phi,2}-2\Phi_\phi-2\alpha)} \\
&- j\Big(\frac{8+\hat{m}_\phi^2}{8\omega}\hat{i}_{\phi,1} e^{j(\Phi_{\phi,1})} + \frac{\hat{m}_\phi^2}{8\omega}\hat{i}_{\phi,3} e^{j(\Phi_{\phi,3}-2\Phi_\phi-2\alpha)}\Big) e^{j\omega t} \\
&- j\Big(\frac{2\hat{m}_\phi^2+3}{6\omega}\hat{i}_{\phi,2} e^{j(\Phi_{\phi,2})} + \frac{\hat{m}_\phi^2}{12\omega}\hat{i}_{\phi,4} e^{j(\Phi_{\phi,4}-2\Phi_\phi-2\alpha)} \\
&- \frac{\hat{m}_\phi \hat{k}_\phi}{4\omega} i_{dc} e^{j(2\Phi_\phi+\alpha-\theta)} + \frac{\hat{m}_\phi^2}{6\omega} i_{dc} e^{j(2\Phi_\phi+2\alpha)}\Big) e^{j2\omega t} \\
&- j\sum_{n=3}^{\infty}\Big(\frac{2(n^2-1)+n^2\hat{m}_\phi^2}{2n\omega(n^2-1)}\hat{i}_{\phi,n} e^{j(\Phi_{\phi,n})} \\
&+ \frac{\hat{m}_\phi^2}{4}\frac{\hat{i}_{\phi,n-2}}{(n-1)\omega} e^{j(\Phi_{\phi,n-2}+2\Phi_\phi+2\alpha)} + \frac{\hat{m}_\phi^2}{4}\frac{\hat{i}_{\phi,n+2}}{(n+1)\omega} e^{j(\Phi_{\phi,n+2}-2\Phi_\phi-2\alpha)}\Big) e^{nj\omega t}\Big]
\end{aligned}
\tag{A.8}
$$

From eq. (A.8) following can be concluded about n^{th} harmonic in leg voltage (v_{leg_ϕ}):

- Odd and even harmonics in common mode arm voltage are decoupled.
- $\hat{v}_{leg_{\phi,n}}$ is dependent only on $n-2, n\,\&\,n+2$ harmonics in the circulating current.

Therefore, system of eq. (A.8) can be represented as [104]:
For even harmonics -

$$
\begin{bmatrix}
b_2 & c_2 & 0 & 0 & 0 & 0 & 0 & \cdots \\
a_4 & b_4 & c_4 & 0 & 0 & 0 & 0 & \cdots \\
0 & a_6 & b_6 & c_6 & 0 & 0 & 0 & \cdots \\
\vdots & & \ddots & \ddots & \ddots & & \cdots & \cdots \\
\vdots & \vdots & & a_{2i} & b_{2i} & c_{2i} & \vdots & \cdots \\
\vdots & \vdots & & \vdots & & & \vdots & \cdots
\end{bmatrix}
\begin{bmatrix}
\hat{i}_{\phi,2} e^{j\Phi_2} \\ \hat{i}_{\phi,4} e^{j\Phi_4} \\ \hat{i}_{\phi,6} e^{j\Phi_6} \\ \vdots \\ \hat{i}_{\phi,2i} e^{j\Phi_{2i}} \\ \vdots
\end{bmatrix}
=
\begin{bmatrix}
\frac{2C}{N}\hat{v}_{leg_{\phi,2}} e^{j\Phi_{v2}} + k_1 \\
\frac{2C}{N}\hat{v}_{leg_{\phi,4}} e^{j\Phi_{v4}} \\
\frac{2C}{N}\hat{v}_{leg_{\phi,6}} e^{j\Phi_{v5}} \\
\vdots \\
\frac{2C}{N}\hat{v}_{leg_{\phi,2i}} e^{j\Phi_{v2i}} \\
\vdots
\end{bmatrix}
\tag{A.9}
$$

For odd harmonics -

$$
\begin{bmatrix}
b_1 & c_1 & 0 & 0 & 0 & 0 & 0 & \cdots \\
a_3 & b_3 & c_3 & 0 & 0 & 0 & 0 & \cdots \\
0 & a_5 & b_5 & c_5 & 0 & 0 & 0 & \cdots \\
\vdots & & \ddots & \ddots & \ddots & & \cdots & \cdots \\
\vdots & \vdots & & a_{2i-1} & b_{2i-1} & c_{2i-1} & \vdots & \cdots \\
\vdots & \vdots & & \vdots & & & \vdots & \cdots
\end{bmatrix}
\begin{bmatrix}
\hat{i}_{\phi,1} e^{j\Phi_1} \\ \hat{i}_{\phi,3} e^{j\Phi_3} \\ \hat{i}_{\phi,5} e^{j\Phi_5} \\ \vdots \\ \hat{i}_{\phi,2i-1} e^{j\Phi_{2i-1}} \\ \vdots
\end{bmatrix}
=
\begin{bmatrix}
\frac{2C}{N}\hat{v}_{leg_{\phi,1}} e^{j\Phi_{v1}} \\
\frac{2C}{N}\hat{v}_{leg_{\phi,3}} e^{j\Phi_{v3}} \\
\frac{2C}{N}\hat{v}_{leg_{\phi,5}} e^{j\Phi_{v5}} \\
\vdots \\
\frac{2C}{N}\hat{v}_{leg_{\phi,2i-1}} e^{j\Phi_{v(2i-1)}} \\
\vdots
\end{bmatrix}
\tag{A.10}
$$

i in subscript of matrix elements denotes the row number.

$$a_n = -j\frac{m^2}{4\omega(n-1)}e^{j(2\Phi_\phi+2\alpha)}$$

$$b_{n\ \ n\geq 2} = \frac{2(n^2-1)+n^2\hat{m}_\phi^2}{2n\omega(n^2-1)}$$

$$b_1 = -j[\frac{8+m^2}{8\omega}]$$

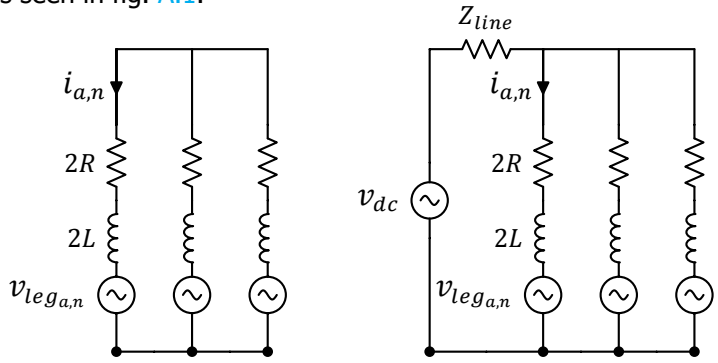
$$c_n = -j\frac{m^2}{4\omega(n+1)}e^{-j(2\Phi_\phi+2\alpha)}$$

$$k_1 = j\Big(-\frac{\hat{m}_\phi\hat{k}_\phi}{4\omega}i_{dc}e^{j(2\Phi_\phi+\alpha-\theta)} + \frac{\hat{m}_\phi^2}{6\omega}i_{dc}e^{j(2\Phi_\phi+2\alpha)}\Big)$$

The solution to system of equations represented by eqs. (A.9) and (A.10) gives the detail of harmonic content in circulating current. This solution is dependent on circuit parameters e.g. dc-link filter, harmonics in dc current, number of phases etc [104]. With a three phase coupled to ac grip via Δ-Y transformer the current on dc side equals sum of arm currents and is considered purely direct. Furthermore, harmonics in circulating current can be divided as:

1. Positive sequence harmonics ($4^{th}, 7^{th}, 10^{th}, .., 3i+1^{th}$...)
2. Negative sequence harmonics ($2^{nd}, 5^{th}, 8^{th}, ..., 3i-1^{th}$...)
3. Zero sequence harmonics ($3^{rd}, 6^{th}, 9^{th}, .., 3i^{th}$...)

With the assumption of purely direct current on the dc side, it is inferred that for the positive and negative sequence circulating current harmonics the dc side appears as an open circuit while for zero sequence it is connected. Based on this inference, the converter system for the harmonic components of circulating current can be depicted as seen in fig. A.1.



(a) Positive and negative sequence harmonics

(b) Zero sequence harmonics

Figure A.1: Circuit for circulating current

Therefore positive and negative sequence harmonic voltages can be expressed as:

$$\begin{aligned} \hat{v}_{leg_{\phi,n}} e^{j\Phi_{vn}} e^{jn\omega t} &= -2L\frac{d}{dt}(\hat{i}_n e^{j\Phi_n} e^{jn\omega t}) - 2R\hat{i}_n e^{j\Phi_n} e^{jn\omega t} \\ \implies \hat{v}_{leg_{\phi,n}} e^{j\Phi_{vn}} &= -2(R + jn\omega L)\hat{i}_n e^{j\Phi_n} \end{aligned} \tag{A.11}$$

Whereas for zero sequence harmonic voltages are expressed as:

$$\hat{v}_{leg_{\phi,n}} e^{j\Phi_{vn}} = -[2(R + jn\omega L) + 3Z_{line}]\hat{i}_n e^{j\Phi_n} + v_{dc} \tag{A.12}$$

Incorporating eqs. (A.11) and (A.12) in eqs. (A.9) and (A.10):

For even harmonics -

$$\begin{bmatrix} q_2 & c_2 & 0 & 0 & 0 & 0 & 0 & \cdots \\ a_4 & q_4 & c_4 & 0 & 0 & 0 & 0 & \cdots \\ 0 & a_6 & q_6 & c_6 & 0 & 0 & 0 & \cdots \\ \vdots & & \ddots & \ddots & \ddots & & \cdots & \cdots \\ \vdots & \vdots & & a_{2i} & q_{2i} & c_{2i} & \vdots & \cdots \\ \vdots & \vdots & & \vdots & & & \vdots & \cdots \end{bmatrix} \begin{bmatrix} \hat{i}_{\phi,2} e^{j\Phi_2} \\ \hat{i}_{\phi,4} e^{j\Phi_4} \\ \hat{i}_{\phi,6} e^{j\Phi_6} \\ \vdots \\ \hat{i}_{\phi,2i} e^{j\Phi_{2i}} \\ \vdots \end{bmatrix} = \begin{bmatrix} k1 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \vdots \end{bmatrix} \tag{A.13}$$

For odd harmonics -

$$\begin{bmatrix} q_1 & c_1 & 0 & 0 & 0 & 0 & 0 & \cdots \\ a_3 & q_3 & c_3 & 0 & 0 & 0 & 0 & \cdots \\ 0 & a_5 & q_5 & c_5 & 0 & 0 & 0 & \cdots \\ \vdots & & \ddots & \ddots & \ddots & & \cdots & \cdots \\ \vdots & \vdots & & a_{2i-1} & q_{2i-1} & c_{2i-1} & \vdots & \cdots \\ \vdots & \vdots & & \vdots & & & \vdots & \cdots \end{bmatrix} \begin{bmatrix} \hat{i}_{\phi,1} e^{j\Phi_1} \\ \hat{i}_{\phi,3} e^{j\Phi_3} \\ \hat{i}_{\phi,5} e^{j\Phi_5} \\ \vdots \\ \hat{i}_{\phi,2i-1} e^{j\Phi_{2i-1}} \\ \vdots \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \vdots \end{bmatrix} \tag{A.14}$$

$$q_n = \begin{cases} a_n + \frac{4C}{N}(R + jn\omega L) & \text{if } n \text{ is not a multiple of 3} \\ a_n + \frac{2C}{N}[2(R + jn\omega L) + 3Z_{line} - v_{dc}] & \text{if } n \text{ is a multiple of 3} \end{cases} \tag{A.15}$$

a_n is purely imaginary therefore from eq. (A.15) q_n which includes a real number is non-zero for all n. This implies that, since in eq. (A.14) as right hand side is completely zero and all diagonal elements are non-zero, all odd-harmonics in circulating current equate to zero.

As a result from eqs. (A.13) and (A.14) magnitude of n^{th} harmonics is given as:

$$\hat{i}_{\phi,n} e^{j\Phi_n} = \begin{cases} 0 & \text{for } n = 2i + 1 \mid i \in \mathbb{Z} \\ \frac{k1 - c_2 \hat{i}_4 e^{j\Phi_4}}{q_2} & \text{for } n = 2 \\ -\frac{a_n \hat{i}_{n-2} e^{j\Phi_{n-2}} + c_n \hat{i}_{n+2} e^{j\Phi_{n+2}}}{q_n} & \text{for } n = 2i \mid i \in \mathbb{Z} \wedge i \geq 2 \end{cases} \tag{A.16}$$

From eq. (A.16) it is concluded:

- Harmonics in circulating currents are of even order only.

- Amplitude of harmonic component in circulating current is dependent on circuit parameter and yields a resonant behavior whose peak correspond to the minimum value of q_n.

  This corresponds to $\Im m(q_n) = 0$ which yields resonant frequency of system as:

$$\omega_{res}^2 = \frac{N}{LC}\frac{2(n^2-1)+\hat{m}^2n^2}{4n^2(n^2-1)} \tag{A.17}$$

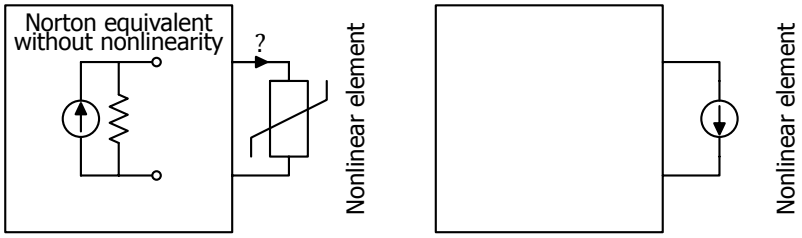
- a_n, c_n decrease with increasing n therefore peak amplitude for resonant frequency (eq. (A.17)) is highest for second harmonic i.e. second harmonic is the most dominant.

B

EMT Solution Method

B.1. Compensation Method

For modeling of nonlinear and time-varying circuit elements circuit elements e.g. arresters, EMT solvers employ the compensation method [9, 154]. In this approach, Norton equivalent of the system without the nonlinear elements is utilized to determine the current through the nonlinear elements either analytically using it's piece-wise wise representation or iteratively through numerical methods e.g. Newton-Raphson. Subsequently, the entire system is resolved with nonlinear element modeled as a current source.



(a) Calculate current into non-linearity (b) Model as current source

Figure B.1: Compensation Method

C

Additional Simulation Results

C.1. Comparison of EMT Models

C.1.1. Model Accuracy

Double phase to ground fault Operation

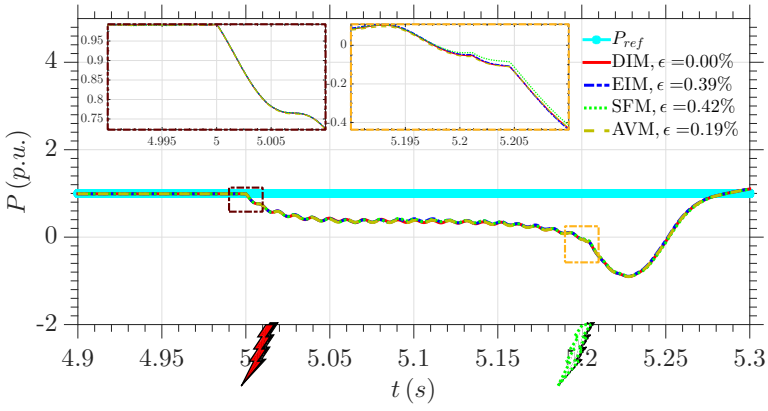


Figure C.1: Real Power at MMC ac-side

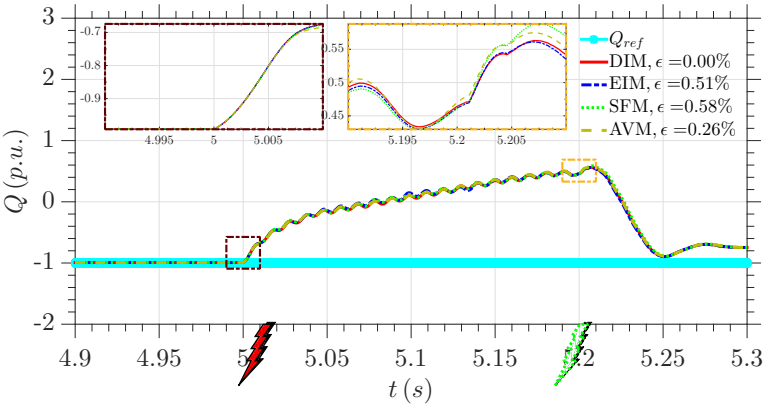


Figure C.2: Reactive Power at MMC ac-side

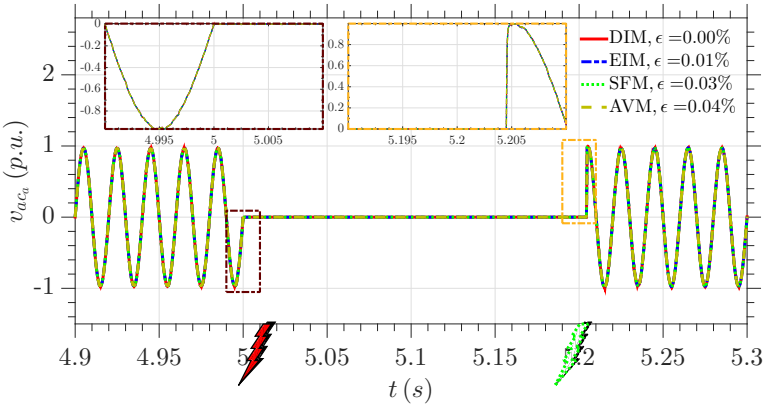


Figure C.3: Phase a ac voltages at MMC terminals

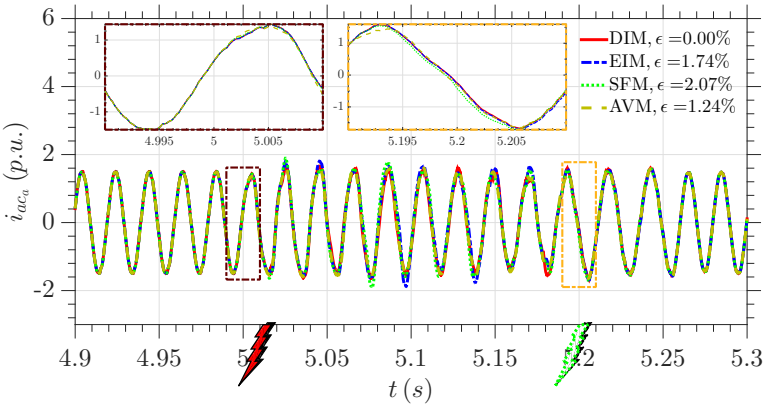


Figure C.4: Phase a ac currents

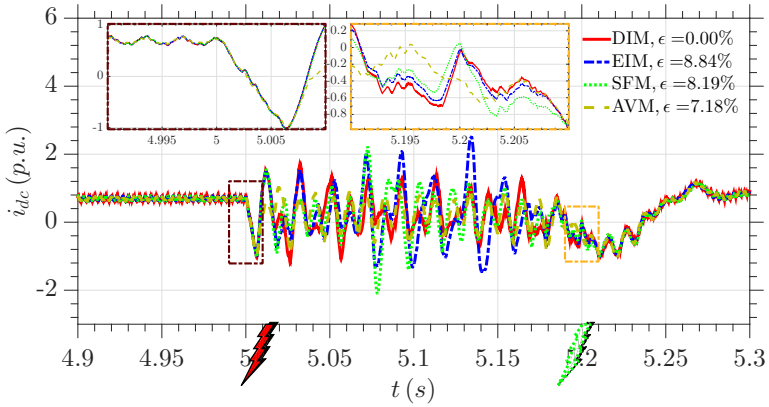


Figure C.5: Current from dc side

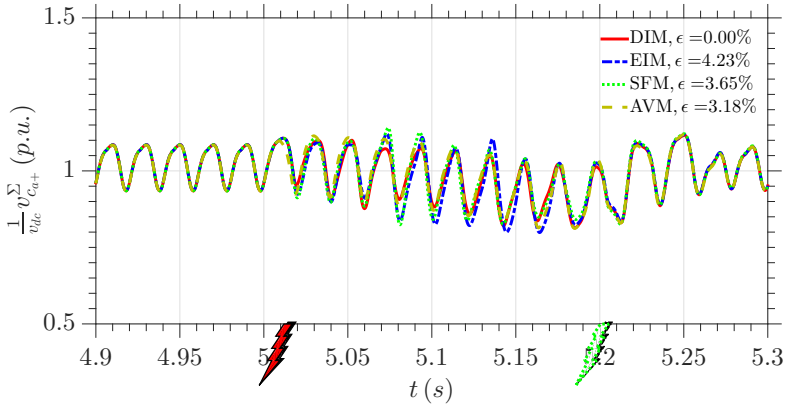


Figure C.6: Cumulative capacitor voltage positive arm phase-a

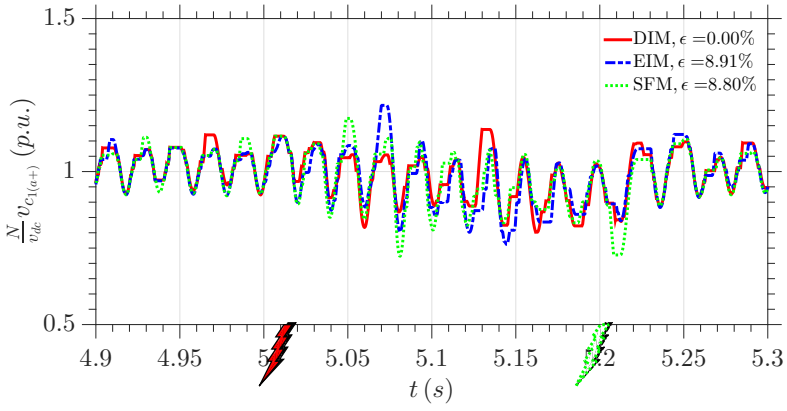


Figure C.7: First Capacitor Voltage positive arm phase-a

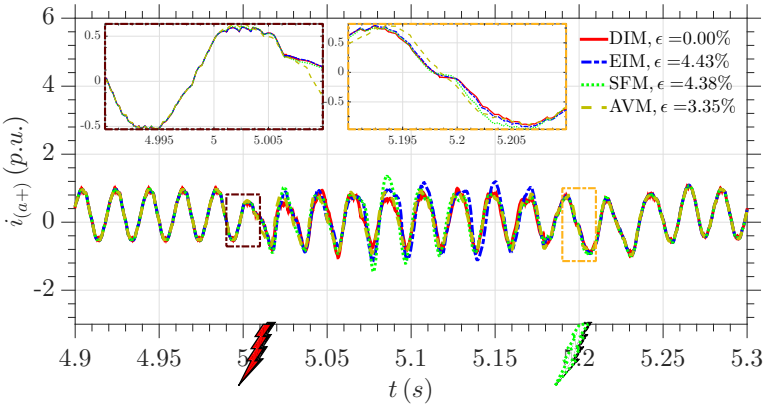


Figure C.8: Positive arm Current phase-a

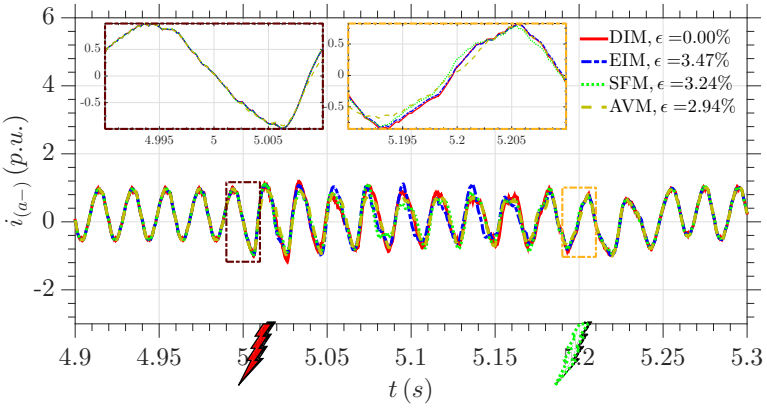


Figure C.9: Negative arm Current phase-a

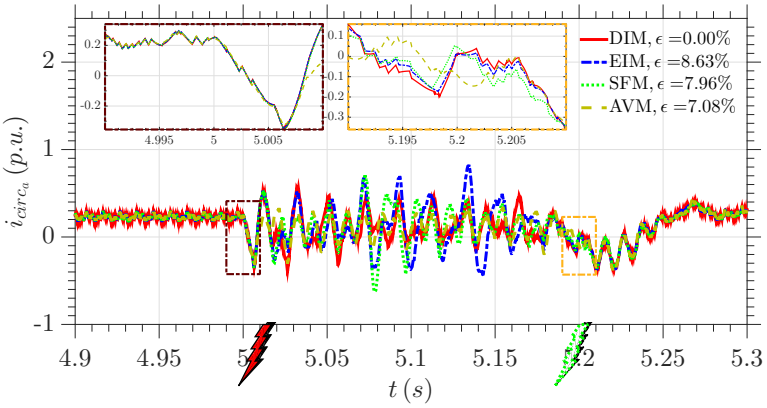


Figure C.10: Circulating current phase-a

Pole to Ground DC fault Operation

The simulations results present the state operation of MMC during power reversal under balanced conditions.

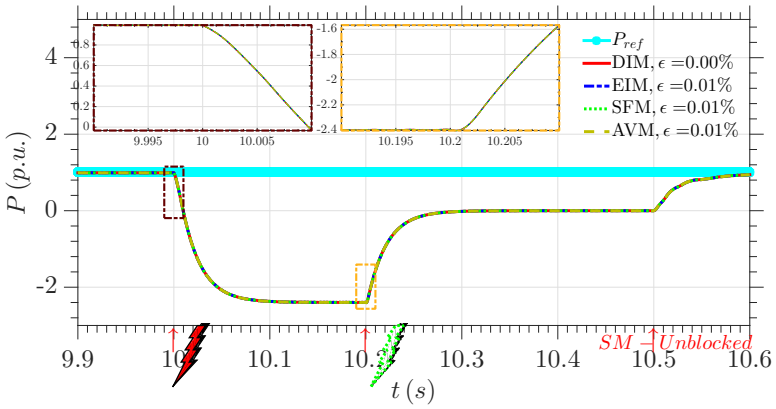


Figure C.11: Real Power at MMC ac-side

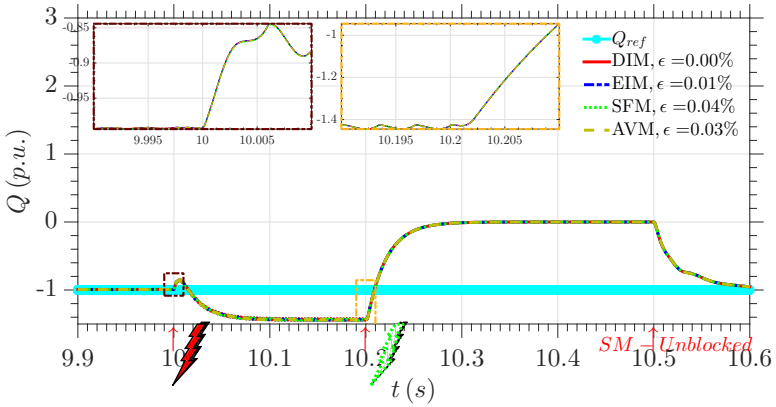


Figure C.12: Reactive Power at MMC ac-side

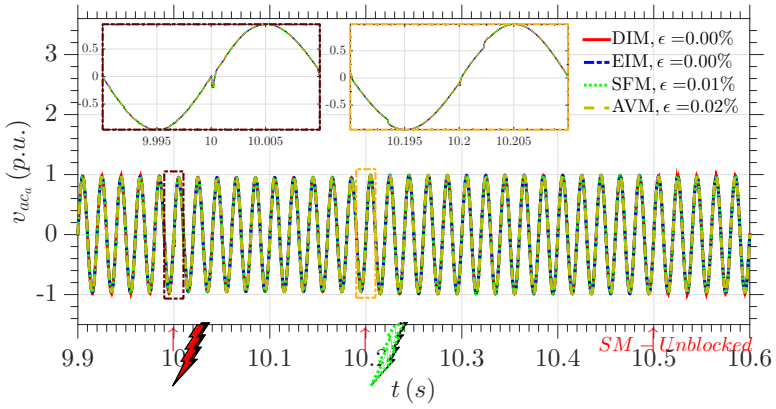


Figure C.13: Phase a ac voltages at MMC terminals

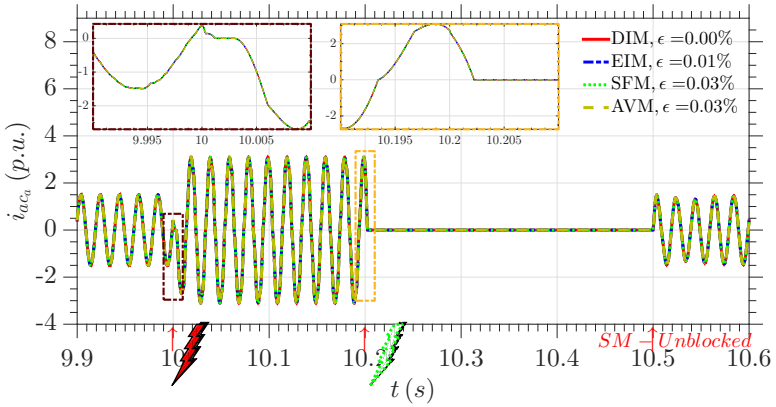


Figure C.14: Phase a ac currents

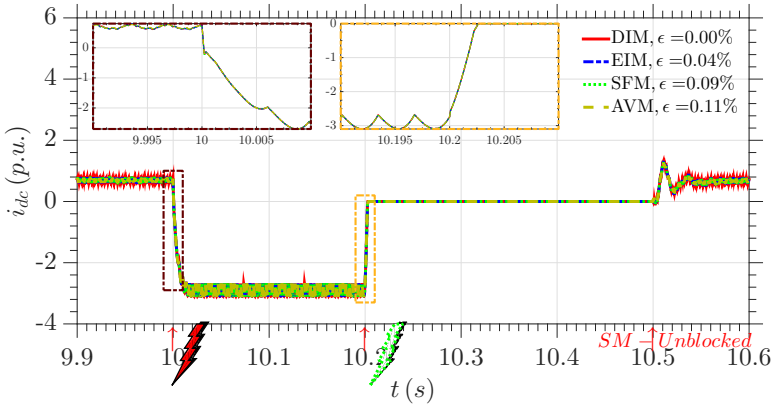


Figure C.15: Current from dc side

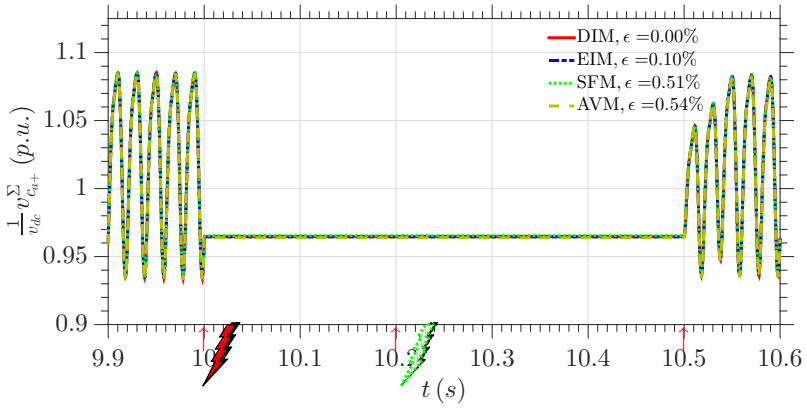


Figure C.16: Cumulative capacitor voltage positive arm phase-a

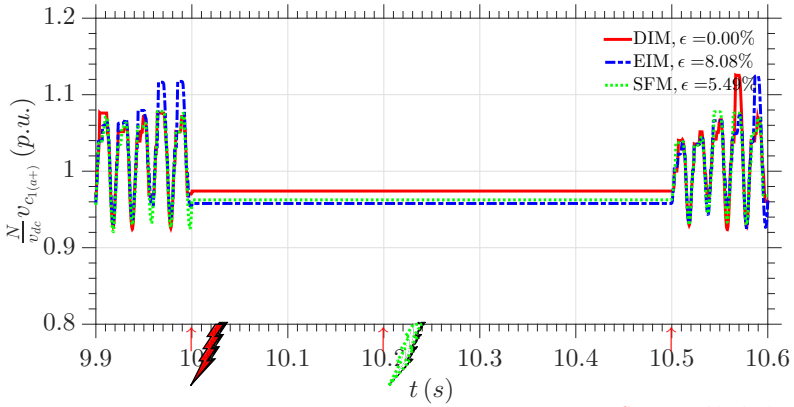


Figure C.17: First Capacitor Voltage positive arm phase-a

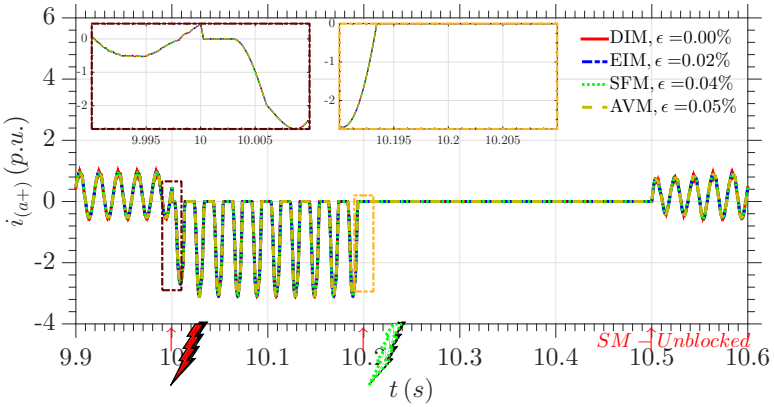


Figure C.18: Positive arm Current phase-a

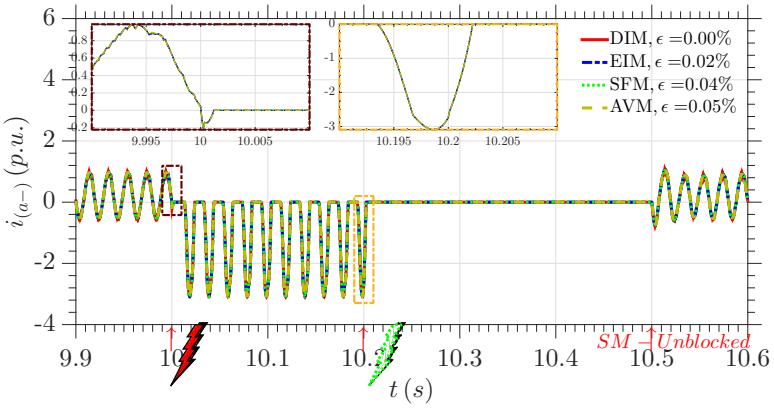


Figure C.19: Negative arm Current phase-a

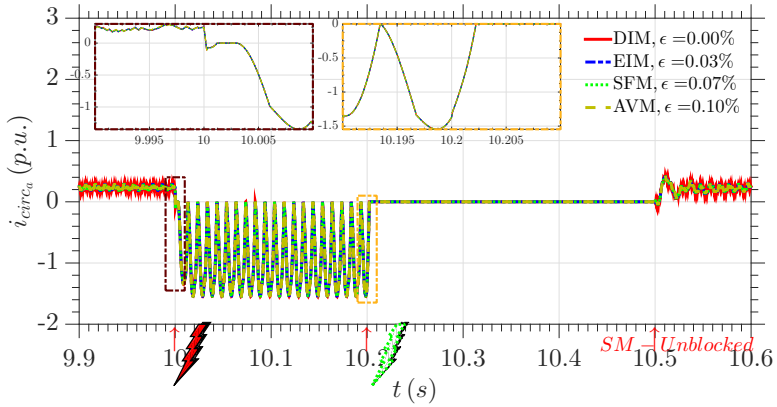


Figure C.20: Circulating current phase-a

D

Model Source Codes

D.1. Equivalent ideal Model

Listing D.1: Source Code Equivalent ideal model

```
/************* Function ****************/
#include "math.h"
#include "stdio.h"
/*************(Fortran convention) ****************/
typedef double real;
typedef long int integer;
typedef long int logical;

void thevmodel_(int* Uigbt, int* Ligbt, real* Iarm, int* Dim
    , real* Capa,real* RP, real* RTON, real* RTOFF, real*
    VsmLast, real* VcLast, real* IarmLast, real* DELT,logical
    * TIMEZERO, real* TIME, real* Vc, real* Ic, real* Veq,
    real* Req, int* SW, int* LastState)
 {
  int i;
  real R1;
  real R2;
  real Rc;
  real Icc;
  real Vcc;
  real Rsmeq;
  real Vsmeq;
  real sumVeq;
  real sumReq;
  real IarmRounded;
```

```
22    real IarmExpolated;
23    real IarmExpRounded;
24    int  BlkCount;
25  /*************(Intialize) ****************/
26    Rc         = (1e6)*0.5*(*DELT)/(*Capa);
27    sumVeq     = 0.0;
28    sumReq     = 0.0;
29       if(*TIMEZERO  == 1)
30       {
31          *IarmLast  = 0.0;
32          *LastState = 0;
33       }
34    *SW = 0;
35    BlkCount = 0;
36    IarmExpolated  = *Iarm + (*Iarm - *IarmLast);
37    IarmRounded    = roundf(*Iarm*1000000)/1000000;         //
        Round to nearest 1mA
38  /*************             ****************/
39       for(i=0;i<(*Dim);i++)
40          {
41           BlkCount = BlkCount  +1;
42  // Intialize History values
43           if(*TIMEZERO  == 1)
44           {
45                   *(VcLast+i)  = 0.0;
46                   *(VsmLast+i) = 0.0;
47           }
48  // Sub-module Inserted
49           if (*(Uigbt+i) == 1 && *(Ligbt+i) == 0)
50           {
51                       R1  = *RTON;
52                       R2  = *RTOFF;
53           }
54  // Sub-module Bypassed
55           if (*(Uigbt+i) == 0 && *(Ligbt+i) ==  1)
56           {
57                        R1  = *RTOFF;
58                        R2  = *RTON;
59           }
60  //Sub-module Blocked
61           if (*(Uigbt+i) == 0 && *(Ligbt+i) ==  0)
62               {   BlkCount = BlkCount  - 1 ;
63                   if (IarmExpolated >= 0 || IarmRounded >= 0
                        ) //if (IarmRounded >= 0 ||
                        IarmExpolated >= 0)
```

```
64                      {
65                              R1   =   *RTON;
66                              R2   =   *RTOFF;
67                      }
68                     else
69                      {
70                              R1   =   *RTOFF;
71                              R2   =   *RTON;
72                      }
73                              }
74  // Current in Capacitor
75          Icc    = (*(Iarm)*R2-*(VcLast+i))/(R1+R2+Rc); //(*(
                Iarm)*R2)/(R1+R2+Rc); //
76 // Capacitor Voltage
77          Vcc    = Rc*Icc + *(VcLast+i);
78 // Thevenin Impedance
79          Rsmeq = R2*(1.0 - R2/(R1+R2+Rc));
80 // Sub-module's Thevenin Voltage
81          Vsmeq = (*(Iarm))*Rsmeq + R2/(R1+R2+Rc)*(*(VcLast+i
                ));
82 // Update Capacitor History
83           *(VcLast+i) = Rc*Icc + Vcc;
84 // Update SM-History
85          *(VsmLast+i) = Vsmeq;
86 // Voltage and Current for individual capacitor]
87          *(Ic +i)   = Icc;
88          *(Vc +i)   = Vcc;
89 // Cumulative for an ARM
90          sumVeq     = sumVeq + Vsmeq;
91          sumReq     = sumReq + Rsmeq;
92          }
93          *Veq       = sumVeq;
94          *Req       = sumReq - *RTON;//Extra Diode/Switch in
                arm.
95          *IarmLast = *(Iarm);
96         if (BlkCount==0)
97         {
98          *SW        = 1; //ALL SMs Blocked//IarmExpolated;
99         }
100 }
```

D.2. Switching Function Model

Listing D.2: Source Code Switching function model

```
1  /************* Function ****************/
2  #include "math.h"
3  #include "stdio.h"
4  /*************(Fortran convention) ****************/
5  typedef double real;
6  typedef long int integer;
7  typedef long int logical;
8
9  void sfmmodel_(int* Uigbt, int* Ligbt, real* Iarm, int* Dim,
       real* Capa, real* VsmLast, real* VcLast, real* IarmLast,
      real* IcLast, real* DELT,logical* TIMEZERO, real* TIME,
      real* Vc, real* Ic, real* Vsm,int* flag, int* SW, real*
      temp,int* Eta, int* Beta)
10  {
11   int i;
12   //real Eta [*Dim];
13   //real Beta[*Dim];
14   real Icc;
15   real Vcc;
16   real Vsmi;
17   real IarmRounded;
18   real IarmExpolated;
19   int  BlkCount;
20 /*************(Intialize) ****************/
21      if(*TIMEZERO  == 1)
22      {
23         *IarmLast  = 0.0;
24      }
25      *SW = 0;
26      BlkCount = 0;
27      IarmRounded    = roundf(*Iarm*1000000)/1000000;
                                  //Round to nearest 1mA
28      IarmExpolated  =  (*Iarm + (*Iarm - *IarmLast)); //
           Round to nearest 1mA
29 /*************            ****************/
30      for(i=0;i<(*Dim);i++)
31         {
32 // Intialize History values
33          if(*TIMEZERO  == 1)
34          {
35                  *(VcLast+i)  = 0.0;
36                  *(VsmLast+i) = 0.0;
```

```
37                  *(IcLast+i)  = 0.0;
38                  *(flag+i) = 0;
39          }
40
41  // flag for inductive nature of current
42          if ((*(Uigbt+i) + *(Ligbt+i)) >  0)
43              {
44                 *(flag+i) = 0;//Reset flag
45                          }
46          else if (*Iarm >0 && IarmExpolated<=0)
47              {
48  //If current goes from positive to negative
49                 *(flag+i) = 1;
50                          }
51                  else if (*Iarm< 0 && IarmExpolated>0)
52              {
53  //If current goes from negative to positive
54                 *(flag+i) = 1;
55                          }
56
57
58  //Sub-module Un-blocked
59          *(Eta+i)    = *(Uigbt+i);
60          *(Beta+i)    = 1;
61  //Sub-module First Block
62          if (*(Uigbt+i) == 0 && *(Ligbt+i) ==  0 && *(flag+i
                )==0)
63              {
64                  if(*Iarm >= 0) //INSERT All
65                   {
66                      *(Eta+i)     = 1;
67                      *(Beta+i)    = 1;
68                   }
69                  else          //Bypass All
70                   {
71                      *(Eta+i)    = 1;
72                      *(Beta+i)   = 0;
73                   }
74                          }
75  //Sub-module NOT First Block
76          if (*(Uigbt+i) == 0 && *(Ligbt+i) ==  0 && *(flag+i
                )>0)
77              {
78                                  *(Eta+i)     = 0;
79                      *(Beta+i)    = 0;
```

```
80                          BlkCount    = BlkCount +1;
81                      if((*Iarm > 0) && *(VsmLast+i)>=*(VcLast+i)
                           )  //INSERT All
82                       {
83                          *(Eta+i)     = 1;
84                          *(Beta+i)    = 1;
85                           BlkCount    = BlkCount -1;
86                       }
87                      else if(*Iarm <0 && *(VsmLast+i)<=0 )
88                       {
89                          *(Eta+i)    = 1;
90                          *(Beta+i)   = 0;
91                           BlkCount   = BlkCount -1;
92                       }
93                             }
94  //Capacitor Current
95                      *(Ic+i)     = (*Iarm)*(*(Eta+i))*(*(Beta+i)
                           );
96  //Capacitor Voltage
97                      *(Vc+i)     = ((*(Ic+i) + *(IcLast+i))
                           *0.5*(*DELT)*(1e6)/(*Capa) + *(VcLast+i)
                           );
98  //SM Voltage
99                      *(Vsm+i)    = (*(Vc+i))*(*(Eta+i))*(*(Beta+
                           i));
100 //Update History
101                     *(IcLast+i) = *(Ic+i);
102                     *(VcLast+i) = *(Vc+i);
103                     *(VsmLast+i)= *(Vsm+i);
104         }
105         *IarmLast   = (*Iarm);
106         *temp       = IarmExpolated;
107         if(BlkCount>=1)
108         { *SW = 1;
109                 }
110 }
```

D.3. Average Value Model

Listing D.3: Source Code Average value model

```
/************* Function ****************/
#include "math.h"
#include "stdio.h"
/*************(Fortran convention) ****************/
typedef double real;
typedef long int integer;
typedef long int logical;

void avmmodel_(real* InsIndex, int* Block, real* Iarm, real*
    Capa, real* VsmLast, real* VcLast, real* IarmLast,real*
   IcLast, real* DELT,logical* TIMEZERO, real* TIME, real*
   Vc, real* Ic, real* Vsm,int* flag, int* SW, real* n, int*
    B, real* Temp)
 {
  int i;
  real Icc;
  real IarmRounded;
  real IarmExpolated;
  int  BlkCount;

/*************(Intialize) ****************/
// Intialize History values
     if(*TIMEZERO  == 1)
         {
                 *(VcLast)  = 0.0;
                 *(VsmLast) = 0.0;
                 *(IcLast)  = 0.0;
                 *(flag)    = 0;
             *IarmLast  = 0.0;
          }
     *SW = 0;
     BlkCount = 0;
     IarmRounded   = roundf(*Iarm*1000000)/1000000; //Round
        to nearest 1mA
     IarmExpolated =  (*Iarm + (*Iarm - *IarmLast));

// flag for inductive nature of current
     if (*(Block) ==  0)
             {
                *(flag) = 0;  //Reset flag
                          }
     else if (*Iarm >0 && IarmExpolated<=0)
```

```
38              {
39 //If current goes from positive to negative
40                  *(flag) = 1;
41                           }
42          else if (*Iarm< 0 && IarmExpolated>0)
43              {
44 //If current goes from negative to positive
45                  *(flag) = 1;
46                           }
47
48
49 //Sub-module Un-blocked
50          *n    = *(InsIndex);
51          *B    = 1;
52 //Sub-module First Block
53          if (*(Block) ==  1 && *(flag)==0 )
54              {
55                  if(*Iarm >= 0) //INSERT All
56                   {
57                      *(n) = 1;
58                      *(B) = 1;
59                   }
60                  else          //Bypass All
61                   {
62                      *(n) = 1;
63                      *(B) = 0;
64                   }
65                      }
66 //Sub-module NOT First Block
67          if (*(Block) ==  1 && *(flag) > 0)
68              {
69                                  *(n) = 0;
70                      *(B) = 0;
71                       BlkCount = BlkCount +1;
72                  if((*Iarm > 0) && *(VsmLast)>=*(VcLast))
                       //INSERT All
73                   {
74                      *(n) = 1;
75                      *(B) = 1;
76                       BlkCount = BlkCount -1;
77                   }
78                  else if(*Iarm <0 && *(VsmLast)<=0 )
79                   {
80                      *(n) = 1;
81                      *(B) = 0;
```

```
82                          BlkCount = BlkCount -1;
83                      }
84                    }
85 //Capacitor Current
86                  *(Ic)      = (*Iarm)*(*n)*(*B);
87 //Capacitor Voltage
88                  *(Vc)      = ((*Ic + *IcLast)*0.5*(*DELT)*(1
                       e6)/(*Capa) + *(VcLast));
89 //SM Voltage
90                  *(Vsm)     = (*Vc)*(*n)*(*B);
91 //Update History
92                  *(IcLast) = *(Ic);
93                  *(VcLast) = *(Vc);
94                  *(VsmLast)= *(Vsm);
95
96          *IarmLast    =  *Iarm ;
97          *Temp        = IarmExpolated;
98          if(BlkCount>=1)
99          { *SW = 1;
100                 }
101 }
```

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[5] A. Lesnicar and R. Marquardt. An innovative modular multilevel converter topology suitable for a wide power range. In *Power Tech Conference Proceedings, 2003 IEEE Bologna*, volume 3, pages 6 pp. Vol.3–, June 2003. doi: 10.1109/PTC.2003.1304403.

[6] R. Marquardt and A. Lesnicar. New Concept for High Voltage - Modular Multilevel Converter. *PESC 2004 Conference in Aachen*, 2004.

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