Ultra Linear Low-loss Varactors & Circuits for Adaptive RF Systems

Cong Huang

Ultra Linear Low-loss Varactors & Circuits for Adaptive RF Systems

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. ir. K. C. A. M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen

op maandag 8 maart 2010 om 12:30 uur

door

Cong HUANG

elektrotechnisch ingenieur
Master of Science van Fudan University, Shanghai, China
geboren te Shanghai, China

Dit proefschrift is goedgekeurd door de promotor:
Prof. Dr.-Ing. J. N. Burghartz

Copromotor:
Dr. ing. L. C. N. de Vreede

Samenstelling promotiecommissie:

Rector Magnificus, voorzitter
Prof. Dr.-Ing. J. N. Burghartz, Technische Universiteit Delft, promotor
Dr. ing. L. C. N. de Vreede, Technische Universiteit Delft, copromotor
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Dr. ir. H. C. de Graaff, adviseur

Reservelid:
Prof. dr. ir. P. M. Sarro, Technische Universiteit Delft

The work described in this thesis was supported by NXP, The Netherlands, Skyworks' Solutions, Newbury Park, USA, and the Delft University of Technology.

Cong Huang,
Ultra Linear Low-loss Varactors & Circuits for Adaptive RF Systems,
Ph.D. Thesis Delft University of Technology,
with summary in Dutch.

ISBN: 978-90-8559-922-7

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Printed by Optima Grafische Communicatie, Rotterdam, The Netherlands.

To My Family

Contents

Chapter 1

Introduction

1.1 From Beacon Tower to Mobile Phone

Since the advent of human beings, the desire to communicate faster and farther has never ceased. In the ancient time, “town criers” [1] held an annual contest to discover who can shout a comprehensible message over the greatest distance. Up to date, the world record for this early human voice based message system is less than 100 meters [2]. The history of communication is mankind’s search for ways to improve upon shouting. Over years, the techniques of communication have evolved from beacon and postage to modern telegraph, telephone, internet, mobile cellular phone and personal communication systems, each of them associated with a massive network such as the Great Wall of China, and the famous network of Roman roads.

A brief comparison between the Chinese Great Wall beacon tower system and the modern cellular phone system (Table I) reveals that significant technical improvements have been achieved in terms of distance, data volume, speed, cost, power consumption and reliability by replacing the beacon tower with a modern base station (see Fig. 1.1, [3], [4]). All of this owes to Maxwell’s theoretical prediction of the existence of electromagnetic (EM) waves in the 1860s and subsequent experiments by Hertz, Marconi and many others. Since then, the nature of communication has undergone a substantial change and new wireless communication methods and services have been enthusiastically adopted by people all around the world.

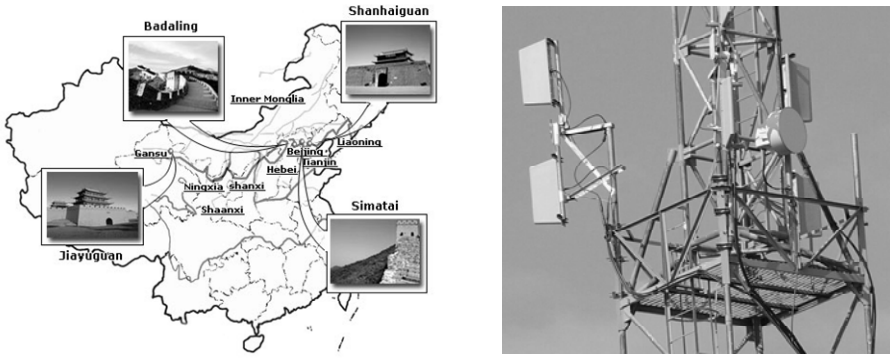
Today, the mobile radio communication industry has grown by orders of magnitude, fueled by digital and RF circuit fabrication improvements, high-level monolithic integration of active and passive components, and other miniaturization technologies, which make portable radio equipment smaller, cheaper and more reliable [5]. In the light of “faster and farther”, mankind’s insatiable desire upon communication, the global mobile system has evolved from the first analogue

generation (1G), mainly intended for voice communication, to the third generation (3G) in the past thirty years. As visualized in Fig. 1.2, the number of subscribers has grown at a phenomenal rate and the global mobile penetration is over 50 percent of total human population at the end of 2008, covering the entire world [6]. The data rate of 3G mobile systems has reached 2.4 Mbps and it is this feature that makes it possible to combine voice, multimedia applications and mobility in a never experienced manner.

Next-generation systems such as fourth generation (4G) and Worldwide Interoperability for Microwave Access (WiMax) promise to add additional capability. The 4G mobile communication services are expected to provide broadband, large capacity, high speed data transmission, providing users with high quality color video images, 3D graphic animation games, and audio services in 5.1 channels.

Table I. Comparison between the Beacon Tower System and Modern Mobile System

	Chinese Great Wall Beacon Tower System	Modern Mobile System
Space Coverage	point to point over 6700 km	entire world
Cost	The construction of the Great Wall had never ceased for nearly all the Chinese feudal dynasties.	The total cost is shared by over 3 billion subscribers and is therefore quite affordable.
Date Rate	~ 1 bit / day	CDMA2000: 2.4 Mbps
Power Consumption	For one bit binary signal, hundreds of beacon towers need to be ignited.	Handset during talk: ~ 1 Watt
Reliability & Privacy of Data	As an alarm signal, the intruders are free to watch and to interfere.	Reliable coded information



(a) (b)

Fig. 1.1. (a) Being the oldest and most effective original telegram, beacon towers are the most important component of the defensive project on the Great Wall. They are built continually to pass military messages. In ancient times, if intruders approached, soldiers on the wall would create smoke in the daytime and light a fire at night to warn their troops. (figure from [3]) (b) Modern Code Division Multiple Access (CDMA) base station (figure from [4]).

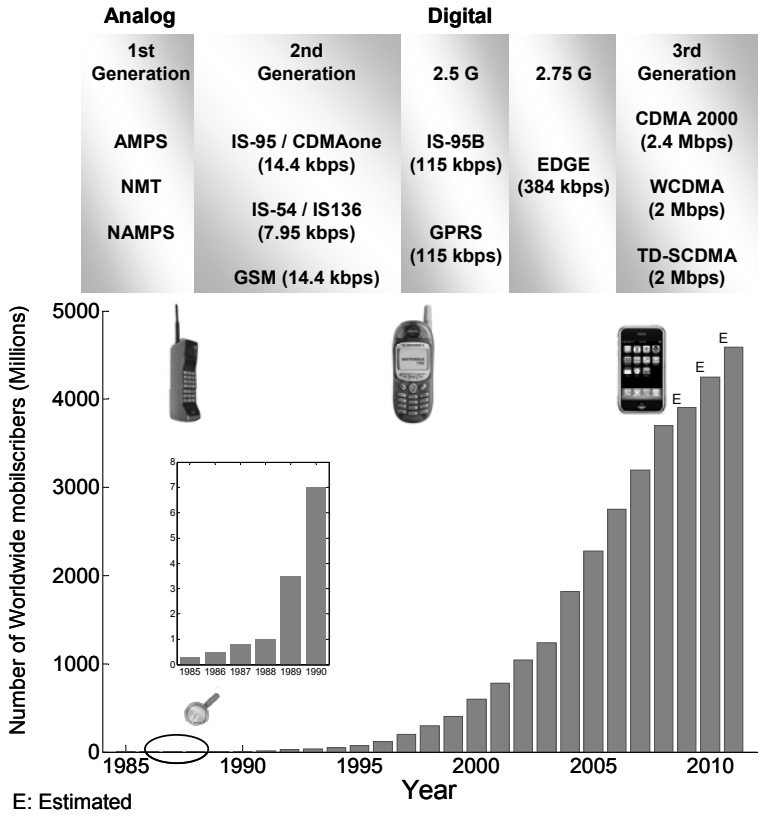


Fig. 1.2. Growth of worldwide mobile subscribers and evolution of cellular networks over years [5], [6].

1.2 The Need for Linear RF Tunable Components

Accompanied by the evolution of wireless communication are the various technical difficulties. First, the use of increased data rates requires the use of complex modulated signals, making the energy consumption of the transmitting stage a concern. Since limited progress is made in battery technology, significant achievements have to, and will be made, in the mobile phone to reduce the power consumption. One of the key ideas is to reduce the power waste of the transmitter related to the environmental changes (e.g. location of the handset with respect to the basestation, disturbance of the antenna, etc.). Second, with the extensive use of cellular phones globally and the migration toward advanced systems, it is desired to build a mobile radio that is flexible enough to handle various communication standards. This leads to research on the multi-mode multi-band RF frontend, in which the main RF parameters, such as operation frequency and bandwidth, can be adaptively adjusted. Last but not the least,

besides the improvement of performance, the cost should be affordable for more subscribers, which in turn motivates the evolution of the wireless communication. To address the issue of cost, on one hand, the cost of a mobile unit can be reduced through high-level integration and hardware reusability. On the other hand, the shared cost of the network can be reduced through the enhancement of system capacity. Note that the former solution relates again with the multi-standard RF reconfiguration and the latter one turns to RF adaptive control of the transmitted power, e.g. as in use for Code Division Multiple Access (CDMA) systems.

In this section, we address how linear RF tunable components, like variable reactors (varactors) and switches, can enable RF reconfigurability for future telecommunication systems. Several case studies are given: (i) linear tunable components based networks can be used to correct the mismatched impedance of the antenna, which helps to maintain the link quality and reduce the power consumption; (ii) they can adaptively control the transmitting power in CDMA systems to increase the total system capacity; (iii) they facilitate to miniaturize and implement multi-band multi-mode radio systems, something that is beneficial for the data rate and system's space coverage; (iv) linear tunable circuits bring even some new functionalities that can serve upcoming modern communication systems. The challenges on tunable components for these applications are brought out, which suggests an urgent need for high-performance tunable components (this is apparent through the survey of currently existing tunable components in Chapter 2).

1.2.1 Adaptive Impedance Control

In modern telecommunication systems, the link quality of cellular phones normally suffers from antenna impedance mismatch caused by the narrow bandwidth of miniaturized high-Q antennas and by detuning of the antenna resonance frequency [7] due to fluctuating body-effects and changes in phone form-factor. For conventional handset transmitter implementations, the effective antenna impedance is supposed to have a nominal value of 50 Ω when the antenna is in the free-space operation without any objects around. However, when the handset is operated close to a metal object or in close proximity to the human body, the effective antenna impedance will vary over a wide impedance range [7]-[13]. When the input impedance varies, there is a mismatch between the power module and the antenna, with two major effects. First, the power module will not perform at its optimum efficiency under the variations of the loading conditions, and, second, the radiated power decreases due to the reflected power. This will result in an increase in energy consumption (i.e., decreased battery endurance) or transmission quality deterioration, increased distortion. In the worst case, the high standing wave amplitude or possible oscillation caused by the mismatch in the circuit

may damage the power amplifier. In view of this, it is desirable to use an impedance-dependent adaptive matching network to maintain the link quality.

1.2.2 Adaptive Power Control

In modern telecommunication systems, power control of RF transmitters is usually required to maximize the system capacity. In order to minimize the interference, the mobile units need to transmit power at variable levels so that the signal strength is similar for all users. This is especially true in the case of CDMA and WCDMA protocols, where the power control is implemented in both base station and handset transmitters [14]-[17]. Power control in the base-station transmitter mitigates the "corner" problem, in which mobile units near the edges of a cell require more power due to transmission losses and adjacent cell interference. On the mobile unit side, to allow for the required variation of RF signal envelopes with modulation schemes, such as quadrature phase-shift keying (QPSK) or multicarrier signaling, power amplifiers have to operate with large peak-to-average power outputs, usually 5 dB or more as shown in Fig. 1.3. Note that such modulation characteristics caused variations are normally on a time scale of microseconds corresponding to the inverse of the modulation bandwidth, and we refer to them as fast variations.

Variations in output power also occur over a slower time scale (ms scale) for CDMA transmission (as well as for all most other cellular protocols) in order to accommodate variable distance between mobile and base, as well as multipath and shadow fading, i.e., slow variations. The transmitted power usage probability density for CDMA applications [15], [17] for rural and urban areas is shown in Fig. 1.4 indicating that the power amplifier operates mostly at 15-20-dB backoff from the peak power, e.g. 27 dBm for this case.

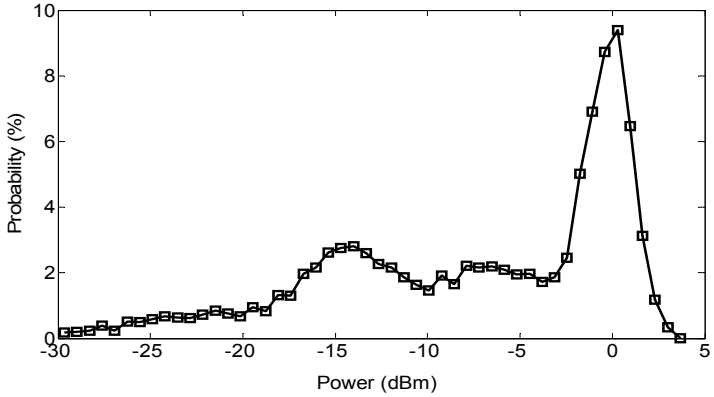


Fig. 1.3. Power output probability distribution for CDMA 2000 forward link under fast variations (peak power = 4 dBm, average power = -3 dBm and chip rate = 1.2288 Mbps).

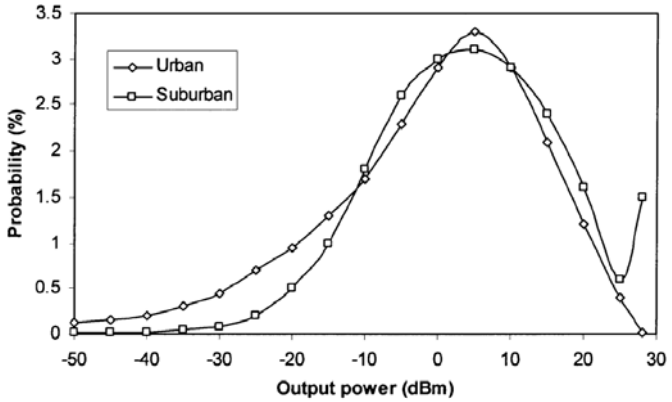


Fig. 1.4. The transmitted power usage probability density for CDMA applications for rural and urban areas under slow variations (data from [14], [17]).

Consequently, the power amplifier operates mostly within regions of low efficiency due to the requirement of power control. Since the power amplifier uses a large portion of the battery power in handsets, it is desirable for power amplifiers in these applications to have higher efficiencies at power-back-off conditions to extend battery life [15]. Techniques that address the efficiency in the back-off mode are dynamic biasing or regulation of the supply voltage of the output stage. Dynamic biasing provides only modest improvements in efficiency. Supply voltage regulation requires an efficient DC-to-DC conversion, increasing system cost and complexity. An alternative for efficiency improvement is load-line adjustment as a function of output power using an adaptive or reconfigurable output matching network. Note that the network in this operation needs to handle fast signal variations, requiring a short response time, and for this reason it is called dynamic adaptive matching network.

1.2.3 Adaptive Multi-band Multi-mode Radio Systems

Wireless communication bands and services are proliferating. Cellular technology standards such as global system for mobile communications (GSM), code division multiple access (CDMA), enhanced data rates for GSM evolution (EDGE), and wideband CDMA (WCDMA) are being developed for long-range voice, data and video transfer. In addition to these public mobile services, many private systems such as IEEE 802.11 WLAN and Bluetooth are also becoming very popular. All these services have different carrier frequencies, channel bandwidths, and modulation schemes. These differences have motivated the industry to look for multi-band multi-mode systems to enable ubiquitous connectivity [18].

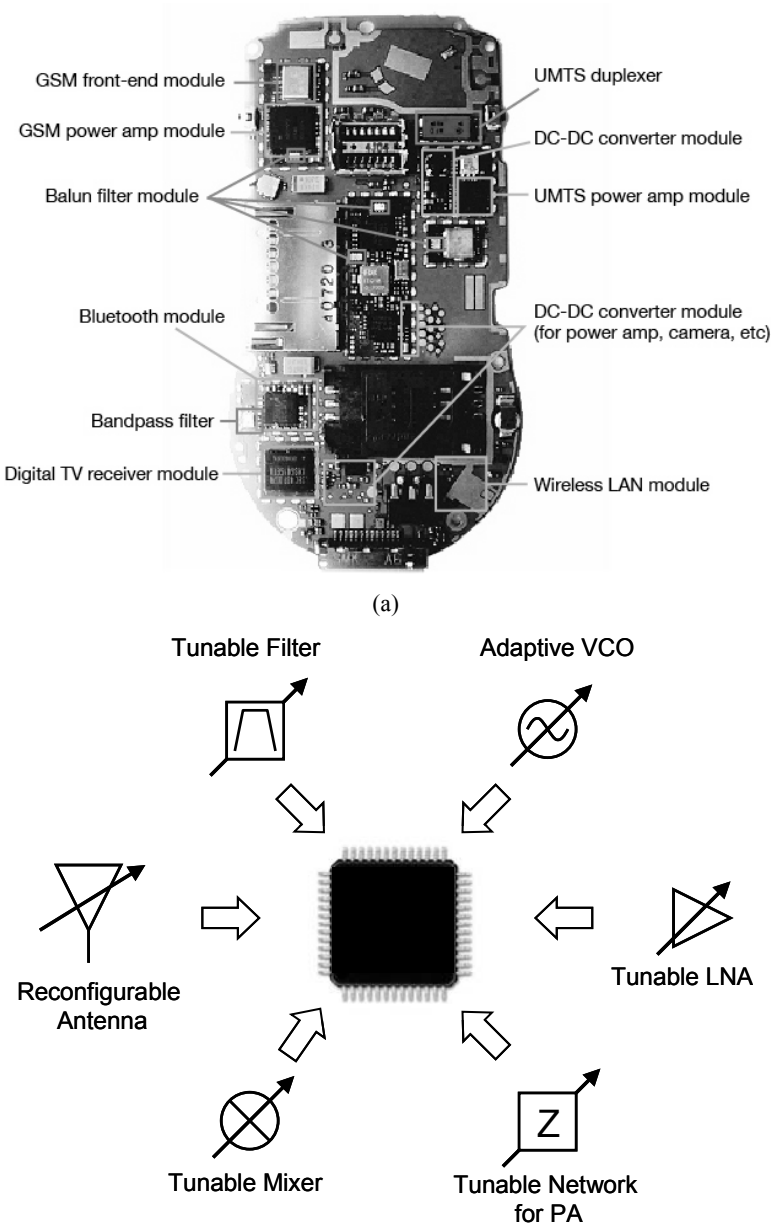


Fig. 1.5. (a) The board for Nokia 6630 mobile phone supporting GSM and UMTS, from Nokia Corp.. In this board, distributed front-end and power amplifier modules are utilized to meet multi-band multi-mode operation (data from [19]). (b) Proposed fully integrated adaptive multi-band multi-mode radio system. With the aid of the high-performance tunable components, multi-standard transceivers can share most circuit functions in an adaptive manner.

In order to fulfill the multi-band multi-mode demands of today's cellular market, current handset implementations are based on distributed modules [see Fig. 1.5(a)], associated with switches, to meet the specific requirements of each communication standard. However, the required extra RF hardware to implement such type of multi-standard radio increases the total chip area and current consumption, therefore neither optimal in cost nor in power. Next-generation wireless systems aiming for size and cost reduction will utilize one or two fully adaptive modules [see Fig. 1.5(b)] to replace the current parallel path concept. Transceivers in such situations can share circuit functions between different standards in an adaptive manner and therefore have the advantages of low power consumption, efficient chip area usage, long talk time, and, most importantly, low cost [20]. In this new architecture, linear tunable components facilitate to implement most of the circuit functions, like adaptive low noise amplifier (LNA), adaptive voltage-controlled oscillator (VCO) [21], [22], tunable high-Q bandpass filters [23], adaptive power amplifiers (PAs). Note that with the trend of multi-band multi-mode integration, above-mentioned power-control and impedance-control matching networks need to be adapted to synchronously meet different communication standard requirements.

It is important to notice that practical design considerations place severe challenges on the tunable elements, the most critical component in the above-mentioned matching networks. First, their tuning range needs to be high enough to implement matching over a wide range at different bands. Second, they should be extremely low loss accompanied with a high breakdown voltage from the power handling and consumption point of view. Last but not the least, the matching networks are mostly placed behind the power amplifier, operating at high power levels, thus the linearity of the tunable components used in these networks is one of most critical issues under consideration, especially in the mobile communication systems with densely populated frequency spectrum.

1.2.4 Amplitude and Phase Modulators

In addition to the applications in power amplifiers and tunable filters, linear tunable components are the most critical elements for passive amplitude modulators and phase shifters, which can act as enablers for the implementation of various radar and communication systems that make use of smart antennas.

In view of this, compact high performance phase shifters are and will be vital components in the realization of modern phase diversity systems. In these systems, the phase of each individual antenna element is controlled to steer the radiation pattern of the antenna without any mechanical movement. As a result of this functionality, a

lower power is required in transmit mode, while signal degradation due to fading in receive mode is significantly reduced [24].

Besides the applications on smart antennas, amplitude and phase modulators provide potential for polar modulators. In contrast to the traditional I/Q modulator, polar modulation techniques can provide magnitude and phase adjustment in a very direct way. Consequently, it can offer a single architecture for various RF transmit systems, which presents opportunities for future communication systems.

Although attractive, the requirements on the amplitude and phase modulators are high: they should be low-loss, compact, require no additional power, and should be highly linear to avoid signal distortion, which directly translate to the challenges on the capacitance density, quality factor and linearity of the tunable components [24].

1.3 Outline

The outline of the thesis is shown schematically in Fig. 1.6. Chapter 2 presents an overview of the state-of-the-art tunable components such as thin-film Barium Strontium Titanate (BST) varactors, Microelectromechanical systems (MEMS) based switches and varactors, and currently available semiconductor switches and varactors. Their advantages and drawbacks are discussed. Chapter 3 deals with the theory of two novel extremely linear varactor diode configurations with complementary linearity properties in a single varactor diode technology, which aims to overcome the limitations of existing tunable components. Both varactor configurations use anti-series varactor diode configurations, where the diodes share the same exponential $C(V_R)$ depletion capacitance relation. However, the proposed structures differ in their harmonic terminations and varactor area ratios, resulting in a fundamentally different linearity behavior versus tone spacing. In Chapter 4, all types of the diode based varactor configurations, aiming for the cancellation of third order intermodulation distortion, are summarized and their performance are compared as guideline for choosing the semiconductor-based varactor configurations. Chapter 5 focuses on the implementation issues of the proposed varactor configurations, together with measurements to support the theory. As two application examples of the novel varactors, the adaptive matching networks for mobile handsets are demonstrated in Chapter 6 and phase shifter and amplitude modulator are created in Chapter 7. Finally, Chapter 8 gives the main conclusions and recommendation for future works.

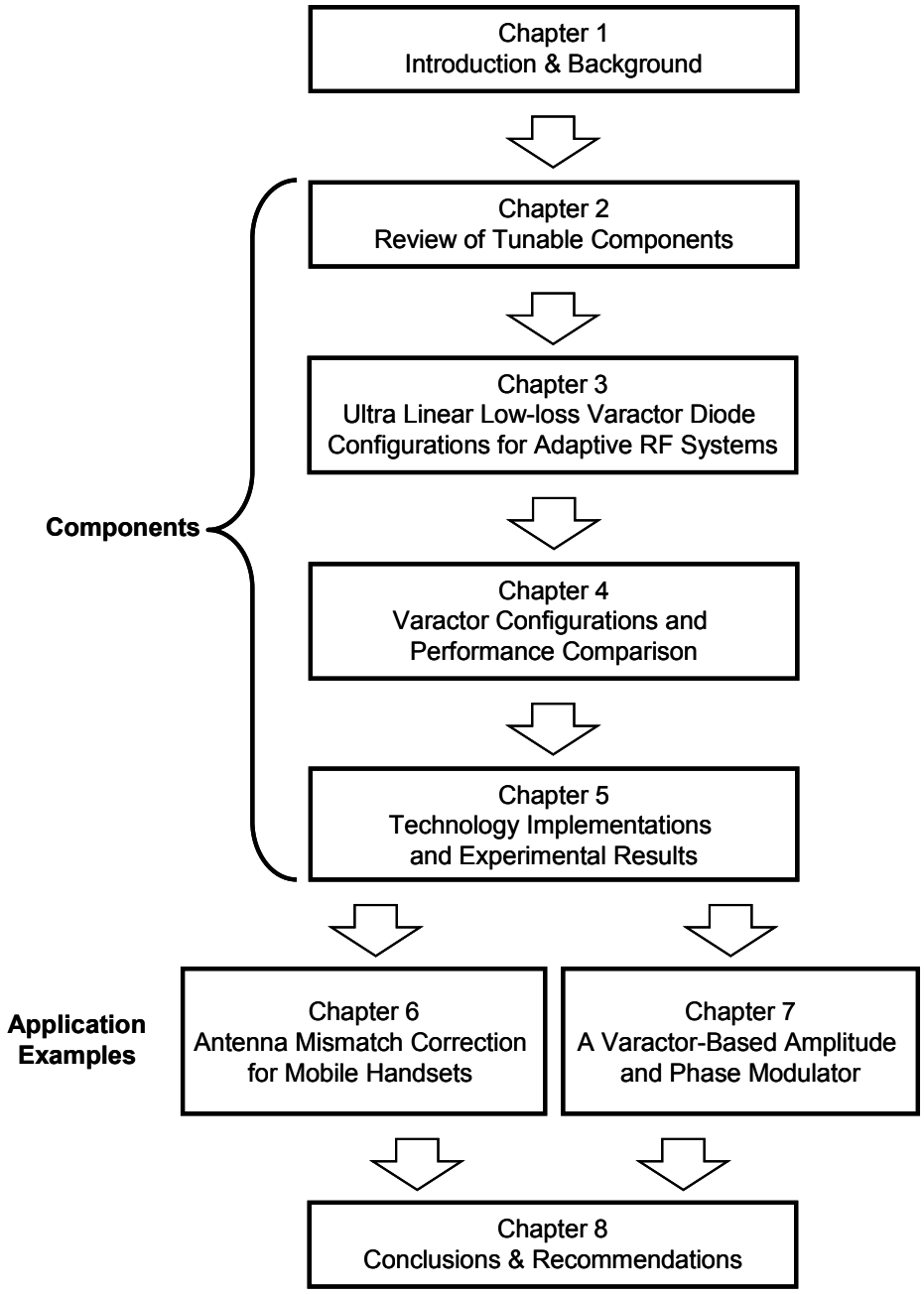


Fig. 1.6. Outline of the thesis

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Chapter 2

Review of Tunable Components

2.1 Introduction

Next-generation wireless systems, such as multi-mode transceivers and "cognitive radios" require circuit techniques that facilitate RF adaptivity. Some examples of adaptive circuits include tunable filters [1], [2] and tunable matching networks for low-noise and power amplifiers [3], [4]. An ideal tuning element for these applications will exhibit extremely low loss, low dc power consumption, high linearity, ruggedness to high voltage and high current, wide tuning range, high reliability, very low cost, low area usage, and will be continuously tunable with a high tuning speed. In this chapter, state-of-the-art tunable components such as thin-film Barium Strontium Titanate (BST) varactors, Microelectromechanical systems (MEMS) based switches and varactors, and conventional semiconductor capacitive switches and varactors are reviewed and compared.

2.2 Currently Available Tunable Elements

2.2.1 Thin-Film Barium Strontium Titanate (BST) Varactors

High-permittivity thin-film dielectrics that exhibit strong field dependence in the dielectric constant can be exploited for voltage-variable capacitors in RF circuits. Thin-film barium strontium titanate (BST) is an example of materials that have been investigated by many research groups [5]-[7]. This research is motivated by the following properties that make it attractive for high-frequency applications:

- High field dependent permittivity variation: as much as 4:1 variation in permittivity.
- High dielectric constant: typically in the range of 200-300.
- "Fast" polarization response: allows for rapid tuning and frequency conversion devices.
- High breakdown electric field: typically > 2×10^6 V/cm, allows for large bipolar voltage swings and hence good power-handling.
- Wide variety of substrate materials available for thin-film deposition.

BST thin-film based varactors [5]-[7] offer advantages in terms of integratability, capacitance density, high speed and they usually exhibit moderate tuning ratio over a relatively low control voltage, which is of the order of 10-20 V, in contrast to 50-100 V [8]-[11] for the microelectromechanical systems (MEMS) varactors or switches. Unlike varactor diodes, BST varactors do not have a forward conduction region and hence can support a relatively large AC voltage swing at low bias voltages, making them useful for moderate-power-level RF applications. However, due to the inherent nonlinear nature of the ferroelectric materials, linearity has been both a concern and challenge in the applications of BST varactors, especially in the spectrally-packed communication systems. In addition, the reproducibility of BST varactors is currently still an issue and hampers their massive manufacture.

2.2.2 MEMS Based Switches and Varactors

Microelectromechanical systems are well suited to implement variable capacitors, inductors, switches and reconfigurable circuits. There are two generic types of MEMS tunable elements: switches and varactors, which have demonstrated impressive performance in terms of low losses, linearity and power handling capability, and for this reason, they are intensively investigated for applications in radar and communication systems.

MEMS switches are composed of a thin metal membrane (or beam), which can be moved to RF line using an electrostatic force due to a voltage between the bridge and bottom electrode, as illustrated in Fig. 2.1. MEMS based switches [10], [11] can provide very low losses while consuming little dc power (microjoule during the switching process). When switching in fixed capacitors, very large capacitance ratios, very low loss and very high linearity can be accomplished. In addition, they can be fabricated on almost any substrate and can also be used to implement tunable circuits by routing the signal through a different path or by providing a stepped control of capacitance. An array with N MEMS switches, for example, will provide 2^N different

combinations of capacitance values, forming a switchable capacitor bank.

However, MEMS switches have several intrinsic disadvantages which restrict their applications in communication systems. First, they are not continuously tunable. For applications where fine tuning is required, a switchable capacitor bank composed of a large number of switching elements is needed, each of them requiring a control voltage. Consequently, the physical metal connections to these switching elements will in practice degrade the overall quality factor of the whole switchable capacitor bank. Second, they have slow switching speeds (1-100 μs) and therefore don't allow fast modulation of the capacitance value. In the meanwhile, their pull-in voltage must be chosen sufficiently large in order to avoid self-actuation due to RF signal and the pull-out voltage must be sufficiently large to avoid non-release under hot-switching conditions [12], which result in a high control voltage (50-100 V). In general, MEMS switches are sensitive to reliability issues, although it has exhibited significant improvement recently.

The MEMS varactor is more or less advanced capacitive membrane switch where analogue control voltage is used to allow continuous tuning. In practice, its structures are very similar to MEMS switches except for the implemented solution to resolve the collapse (snap-down) problem which normally limits the tuning range. The MEMS varactor [8]-[11] is considered to be less sensitive to reliability issues compared to MEMS switches, it provides a very high Q for moderate capacitance values. Nevertheless, its continuous tunable implementations can suffer from intermodulation distortion, since the position of the membrane can move with changes in the modulation envelope of the applied RF voltage [11], [13]. It requires non-standard processing and expensive packaging costs, and its switching speed is still poor compared to the BST and semiconductor-based solutions. Moreover, its relatively small continuous tuning range and high control voltage constrain its RF performance. Also, its relatively small capacitance density makes it difficult to implement large valued capacitors and for this reason its application is mostly found above 5 GHz.

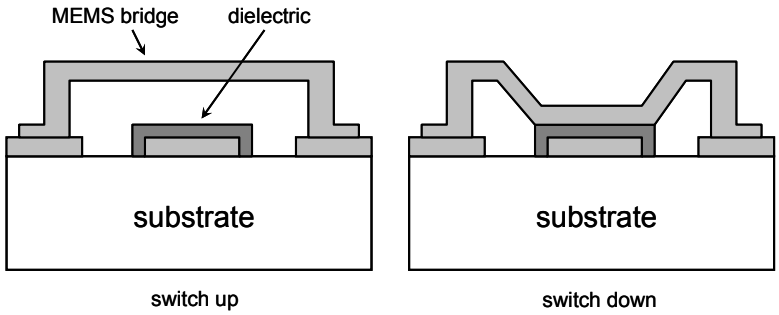

Fig. 2.1. Cross section of an electrostatically actuated capacitive membrane MEMS switch. (a) The switch is off. (b) The switch is on. The switch alternates between a high and low capacitance.

2.2.3 Conventional Semiconductor Based Varactors

Semiconductor varactors, like p-n diode, Schottky diode and MOS varactors, are basically voltage-controlled capacitances, making good use of the voltage dependence of the depletion thickness of the space charge region. Due to relatively high dielectric constants of semiconductor materials, their capacitance densities are normally at least 10 times larger than the MEMS counterparts. In addition, the semiconductor solutions show advantages in terms of integration, reliability, high tuning speed (1-100 ns), low-control voltage and ruggedness. However, their inherently nonlinear behavior does not comply with modern communication systems with densely populated frequency spectrum, and their related quality factors are usually limited at the microwave frequencies of interest for most demanding applications.

2.2.4 Semiconductor Based Switches

When the diodes or transistors are switched between the forward and reverse bias condition, they alternate between a resistor (R_{on}) in the ON state and a capacitor (C_{off}) in the OFF state. In order to obtain a capacitive tuning, a bigger constant capacitor ($C_{on} > C_{off}$) is normally connected in series to form a capacitive switch as shown in Fig. 2.2.

(a) in the OFF state (b) in the ON state

Fig. 2.2. Equivalent circuits of a capacitive switch in the OFF and ON state.

When the diode is under zero or reverse bias (transistor can be also regarded as switching element), it exhibits a low capacitance close to C_{off} as shown in Fig. 2.2(a) resulting in high impedance at RF frequency. Under a forward bias condition, the switched capacitor will behave as a small RF resistance (R_{on}) in series with C_{on} instead [see Fig. 2.2 (b)]. In this case, a smaller R_{on} is favored to achieve a better quality factor, however by lowering R_{on} through up-scaling the switching element typically the capacitance under off-state (C_{off}) will increase, which in turn limits the resulting switchable capacitance ratio (T_{tune}). In view of this, care is normally taken to improve the R_{on}-C_{off} product by making use of special process technologies, like silicon-on-sapphire (SOS) CMOS [14] and pseudomorphic high electron mobility transistor (pHEMT) [15].

The state-of-the-art R_{on}-C_{off} products of semiconductor capacitive switches are listed in Table II and they are translated to Q-T_{tune} product using [16]

$$Q \times (T_{tune} - 1) = \frac{1}{\omega R_{on} C_{off}} \tag{2.1}$$

where ω is the angular RF frequency;

$$Q = 1/(\omega R_{on} C_{on}) \tag{2.2}$$

is the quality factor of the capacitive switch in the ON state, and

$$T_{tune} = C_{on} / \left(\frac{C_{on} C_{off}}{C_{on} + C_{off}} \right) = 1 + \frac{C_{on}}{C_{off}} \tag{2.3}$$

is the capacitance ratio between ON and OFF states.

Table II. Survey of state-of-the-art R_{on}-C_{off} products from different process Technology and corresponding Q-T_{tune} products at 2 GHz and 5 GHz

Process Technology	$R_{on} \times C_{off}$ (fs)	$Q \times (T_{tune} - 1)$ at 2 GHz	$Q \times (T_{tune} - 1)$ at 5 GHz
0.15 μm pHEMT	435 [15]	183	73
0.5 μm pHEMT	360 [15]	221	88
0.5 μm 10 nm T_{ox} SOS	756 [14]	105	42
0.25 μm 5 nm T_{ox} SOS	448 [14]	178	71

Table II implies that the room for compromise between the quality factor and tuning range are very limited especially when the RF operation frequency is high, which can be regarded as the bottleneck for semiconductor switches. For this reason, their applications are mostly found below 2 GHz.

2.2.5 Modern Semiconductor Based Varactors

In order to overcome above-mentioned drawbacks and to create low-loss, easy to integrate, highly reliable and ultra-linear continuous tunable capacitors, varactor diode-based circuit topologies - along with a high performance silicon-on-glass varactor diode process technology - have been presented [17], [18]. These varactor configurations, proposed and initiated by K. Buisman et al., can act as variable capacitors with ideally zero, or extremely low distortion [17]-[23]. A brief description of these two previous low-distortion varactor configurations is given below.

- The distortion-free varactor stack (DFVS) [19]-[23]: is based on an anti-series connection of two identical uniformly doped varactors (capacitance power law

- coefficient $n = 0.5$), which use an infinitely high impedance as center-tap connection. Under these conditions, all distortion components at the RF terminals are perfectly cancelled, yielding a distortion-free operation.
- The high tuning range varactor stack (HTRVS) [17]: is a combined anti-series/anti-parallel topology of four hyperabrupt varactor diodes [24] (capacitance power law coefficient $n > 0.5$), which uses two infinitely high center-tap impedances. At the RF terminals, the resulting even and third-order distortion products are cancelled through a proper selection of the varactor area ratio.

For the implementation of these two varactor configurations, methods are applied to reduce or eliminate the losses from the connecting metals, contact resistance, buried layer and substrate. Consequently, the fabricated distortion-free varactor stack has the lowest quality factor of 180 at zero bias voltage and a tuning range of 4:1 at 2 GHz [17], a value corresponding to a $Q\times(T_{tune}-1)$ product of 540 even for a silicon implementation. Note that further improvement is possible through the use of high-mobility intrinsic material and the theoretically achievable Q-T_{tune} product can be predicted by [25]

$$Q(worst)\times\left[(T_{tune}^2-1)(T_{tune}-1)\right]=\frac{\mu_n E^2_{breakdown}}{2\omega V_j} \tag{2.4}$$

where μ_n is the electron mobility, $E_{breakdown}$ is the maximum electric field at breakdown and V_j is the built-in potential.

Table III. Calculated Q-T_{tune} products of the uniformly doped diodes for a given tuning range (T_{tune}) at different RF frequencies

[$\mu_n = 6000\ \ cm^{-2}/(V\cdot s)$, $E_{breakdown} = 6\times10^5\ \ V/cm$ and $V_j = 0.7\ \ V$]

Tuning Range (T_{tune})	$Q\times(T_{tune}-1)$ at 2 GHz	$Q\times(T_{tune}-1)$ at 5 GHz	$Q\times(T_{tune}-1)$ at 100 GHz
3	15360	6144	307
6	3510	1404	70
9	1674	670	34
12	858	343	17

As a comparison with the semiconductor based switches, Table III lists the calculated Q-T_{tune} products of the uniformly doped diodes in a GaAs implementation. It is seen that the new semiconductor varactors are much better at 2 GHz band and readily operated up until 100 GHz.

Although very good results have been achieved with the configurations above, their practical implementations still have linearity constraints for complex modulated

signals, or other signals with narrow tone spacing. This is caused by the severe requirements for the center-tap impedance, which should approximate infinity when the tone-spacing approaches zero. Due to the requirement of these very high center-tap impedances, rapid modulation of the capacitance value of the distortion-free varactor stack and high tuning range varactor stack becomes problematic. Also, parasitic leakage currents of the diodes can cause voltage drops over this center-tap impedance, yielding an undesired shift of the intended capacitance value.

2.3 Discussion on Current Varactor Topologies

In general, the performance of varactors, like tuning range, control voltage, quality factor, linearity etc, are traditionally trade-off against each other, by choosing either the technology or the element parameters.

Table IV. Varactor Performance Comparison

	Conventional Semiconductor	DFVS/ HTRVS	BST	Continuously Tunable MEMS
Tuning Range	High	High	Moderate	Low
Loss (Q)	Moderate (Q < 60 typ.)	High (Q < 200)	Moderate (Q < 60 typ.)	Very High (Q < 200)
Capacitance Density	Moderate	Moderate	Very High	Low
Control Voltage	< 10 V	typically < 10V	10-20 V	50-100 V
Tuning Speed	Fast	Slow	Fast	Slow
Voltage Handling	Poor	Moderate	Moderate	Excellent
Linearity (IM_3)	Poor	Excellent at large Δf	Poor	Excellent at large Δf
Reliability	Excellent	Excellent	Good	Poor

As compared in Table IV, no solution surpasses the others in all aspects. Currently, MEMS varactors play an important role in the high-frequency (above 5 GHz) regions, while the BST and conventional semiconductor varactors are widely used for low-power applications. The distortion-free varactor stack and high tuning range varactor

stack are newly-invented components and they have shown many promising applications over the DC to 2 GHz frequency range and would appear to have a bright future for high-frequency applications as well. Although very good results have been achieved, they have limitations when rapid modulation of their values is desired while their linearity performance at narrow tone spacings is also of importance. Solutions to these limitations will be addressed in the next chapters.

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Chapter 3

Ultra Linear Low-loss Varactor Diode Configurations for Adaptive RF Systems

3.1 Introduction

In this chapter, we focus on the implementation of two highly linear varactor diode configurations with complementary linearity properties in terms of tone spacing in a single varactor diode technology, which aims to overcome the limitations of existing tunable elements specified in Chapter 2. Both varactor configurations use an anti-series varactor diode topology, where the diodes share the same exponential $C(V_R)$ depletion capacitance relation. However, the proposed structures differ in their harmonic terminations and varactor area ratios, resulting in a fundamentally different linearity behavior versus tone spacing. The first structure has the highest linearity for narrowband modulated signals and is named the narrow tone-spacing varactor stack. This new configuration exhibits improved linearity for narrowband signals, little sensitivity to leakage currents, higher capacitance control range and lower control voltages. The second varactor configuration exhibits the highest linearity for modulated signals with wide tone spacing, and is hereafter named the wide tone-spacing varactor stack. This structure is a direct derivation of the earlier proposed high tuning range varactor stack [1] and for this reason it preserves all the merits of that component.

In receiver applications the input signal is typically small in amplitude (< -30 dBm) relaxing the in-band linearity requirement. Therefore, for the receiver, the most troublesome distortion comes from strong out-of-band interferers whose undesired mixing products can fall in-band and pollute the reception of the desired signal. Note that in practical situations these interfering or jammer signals are typically separated

from the desired signal by more than 100 kHz. As a result the linearity for signals with larger tone spacing is most important. Considering the above, the wide tone-spacing varactor stack is a very attractive candidate for adaptive receivers. On the other hand, the linearity properties of the narrow tone-spacing varactor stack are best suited for the transmitting path. Here, complex modulated signals with a high output power need to be handled without introducing channel-to-channel interference or increasing the error vector magnitude due to intermodulation distortion.

This chapter is organized as follows. The theory of operation for the narrow tone-spacing varactor stack is given in Section 3.1. The requirements for the doping profile and its optimization for the tuning range, breakdown voltage and quality factor are discussed in Section 3.2. The influence of fifth-order intermodulation distortion on the linearity is considered in Section 3.3. The practical implementation issues related to process deviation are discussed in Section 3.4. In Section 3.5, we focus on the analysis of the wide tone-spacing varactor stack, yielding its required varactor area ratio for IM_3 cancellation. The remaining IM_5 distortion for the wide tone-spacing varactor stack has been quantified by a compact expression, while the influence of the center-tap impedances on the linearity as a function of tone spacing has been analyzed. We conclude this chapter in Section 3.6 with a comparison of the two varactor linearization techniques.

3.2 Theory of Operation

The novel high-linearity narrow tone-spacing varactor stack configuration is based on a Volterra analysis of the circuit shown in Fig. 3.1. As a measure of the varactor linearity we consider the IM_3 current flowing through the varactor diodes at frequency $(2f_1\text{-}f_2)$.

The low-frequency impedance of the center-tap is set to zero $[Z_c(f_2\text{-}f_1) = 0]$ while this center-tap impedance is set to infinity at the higher harmonics. Using general Volterra series techniques [2], the resulting IM_3 at narrow tone spacing $[(f_2\text{-}f_1)/f_1 \approx 0]$ for this specific varactor configuration can be achieved, namely:

$$IM_3\Big|_{Z_c(s=0)=0} = \left| \frac{(3c_0c_2 - 2c_1^2)\hat{A}^2}{2c_0^2\left(s_{RF}c_0Z_s(-s_{RF})-2\right)\left(s_{RF}c_0Z_s(s_{RF})+2\right)^2} \right| \tag{3.1}$$

where

$$c_0 = C(V_R), \tag{3.2}$$

$$c_1 = \frac{1}{2}\frac{dC(V_R)}{dV_R}, \tag{3.3}$$

$$c_2 = \frac{1}{6}\frac{d^2C(V_R)}{d^2V_R} \tag{3.4}$$

are the capacitance Taylor coefficients of each varactor diode with V_R being the reverse applied voltage with a positive value , $Z_s(s)$ is the source impedance, s_{RF} is the complex RF center frequency ($j\omega_{RF}$) of the two-tone signal and $\hat{A}$ represents the voltage amplitude of the source signal.

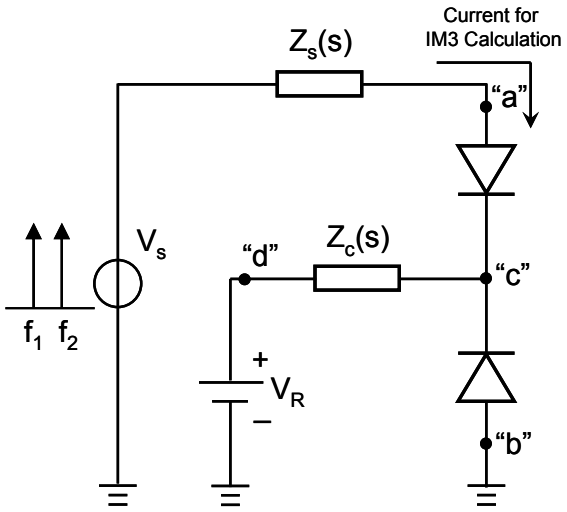


Fig. 3.1. Schematic for the Volterra analysis of the anti-series varactor diode circuit.

By setting (3.1) to zero we can enforce IM_3 cancellation and we find an exponential $C(V_R)$ relation for the varactors, i.e.,

$$C(V_R) = a_1 \exp(-a_2 V_R)\,. \tag{3.5}$$

In this relation, a_1 and a_2 indicate the integration constants, which add some flexibility to the solution. Note that any choice of a_1 and a_2 with positive values will satisfy (3.1) yielding perfect cancellation of the IM_3 distortion component. For this low distortion to be achieved in practice, there must be a *low impedance* path (relative to the AC impedance of the varactor capacitance itself) between the center node *c* and two RF terminals (*a* and *b*) of the varactor stack at low frequency (f_2-f_1). At the same time,

there must be a *high impedance* path for the high frequency components (fundamental and higher harmonics) of the impedance between the center node *c* and two RF terminals (*a* and *b)* of the varactor stack. When these conditions are met, a very high linearity tunable capacitance is achieved between the RF terminals of the varactor stack.

Note that the condition for IM_3 cancellation [numerator of (3.1) equal to zero] only demands a functional relation between the Taylor coefficients, which is fully satisfied by using varactors with an exponential $C(V_R)$ relation. Consequently, the achieved IM_3 cancellation does not depend on the value of the reverse bias voltage, nor the surrounding circuitry [Note, for example, that Z_s does not appear in the numerator of (3.1)]. Therefore, this low-distortion tunable capacitive element can be applied in any circuit topology (including series configuration), provided that the designer takes the proper measures to guarantee the low-impedance paths for the baseband components between the center node *c* and the RF terminals (*a* and *b*), while loading of the center node for higher frequencies should be avoided. The resulting component will also exhibit excellent in-band linearity for the typical wireless complex modulated signals. Linearity restrictions with respect to the bandwidth of these signals (e.g. $B >> 10$ *MHz*), only arise when the baseband short circuit between center node and RF terminals fails to provide a sufficiently low impedance.

3.3 Doping Profile and Performance Compromise

3.3.1 Doping Profile

Based on a Volterra series analysis and the solution of (3.1), the desired capacitance-voltage relation for ideal IM_3 cancellation was determined in (3.5). The next step is to determine the required doping profile. For this purpose we assume a one-sided junction (e.g. a Schottky diode) and solve for the doping profile using [3]

$$N(x) = \frac{C(V_R)^3}{e\varepsilon_s}\left(\frac{dC(V_R)}{dV_R}\right)^{-1} \tag{3.6}$$

where

$$x = \frac{\varepsilon_s}{C(V_R)} \ . \tag{3.7}$$

Making use of these relations, it can be shown that the required doping profile for an exponential capacitance voltage relation is

$$N(x) = N_d x^{-2} \tag{3.8}$$

in which N_d is a doping concentration constant to be defined and x is the distance from the metallurgical junction. It should be noted that this result is singular for $x = 0$, and measures to avoid this singularity must be taken. In order to explain how the doping profile should be defined, we consider Fig. 3.2.

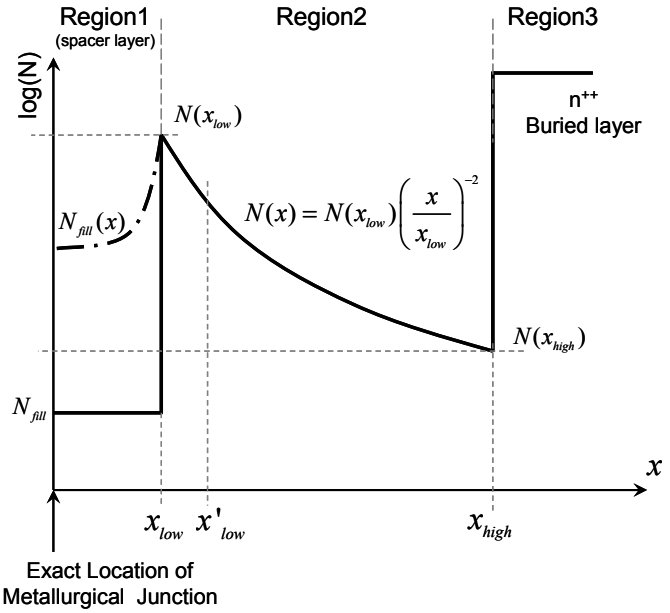


Fig. 3.2. Required varactor doping profile of the narrow tone-spacing varactor stack, to achieve the exponential $C(V_R)$ relation. The black dashed line shows the restriction on the doping level of the "spacer" layer due to the sheet resistance (see Appendix *A*). The solid line represents the ideal doping profile (see Appendix *B*).

In this figure, the ideal doping profile is indicated by the solid line. Since we cannot provide an infinitely high or extremely low doping concentration, this limits the validity of the $N_d x^{-2}$ relationship between x_{low} and x_{high}. Therefore, we define the useful capacitance tuning range (T_{tune}), since the capacitance is inversely proportional to the distance x, i.e.,

$$T_{tune} = \frac{C_{\max}}{C_{\min}} = x_{high} / x_{low} \tag{3.9}$$

To maintain the "exponential" $C(V_R)$ relation, a spacer layer (Region 1 in Fig. 3.2) is

required in order to satisfy the $N_d x^{-2}$ doping versus depth relation with respect to the metallurgical junction position (e.g. a doubling in distance to the metallurgical junction should result in one-fourth the doping concentration). To avoid reduced breakdown voltage, quality factor and capacitance tuning range (T_{tune}), the normally-depleted spacer layer should not significantly increase the electric field. To achieve this, the doping concentration of this spacer layer must be kept low with respect to $N(x_{low})$. In Appendix *A* this is analyzed, resulting in a lower bound on the effective sheet resistance of this spacer layer.

Here we assume for reasons of simplicity that the low doped spacer layer consumes the total built-in voltage of the junction, while the applied voltage is used to deplete the $N_a x^{-2}$ region. As a result, the exponential $C(V_R)$ relation of the fabricated diode (see Appendix *B*) is given by

$$C(V_R) = \frac{A\varepsilon_s}{x_{low}} \exp\left(-\frac{\varepsilon_s}{eN(x_{low}){x_{low}}^2} V_R \right) \tag{3.10}$$

where *A* is the area of the capacitor and the constant ($A\varepsilon_s / x_{low}$) represents the zero bias capacitance value.

Although, in principle we can always choose an appropriate doping concentration of the spacer layer to make (3.10) valid, some practical implementations might use an even lower doping of the spacer layer. In this situation, the depletion distance (x'_{low}) at zero applied voltage can be larger than x_{low} , as shown in Fig. 3.2, and consequently the $C(V_R)$ relation has to be modified to (Appendix *B*):

$$C(V_R) = \frac{A\varepsilon_s}{x'_{low}} \exp\left(-\frac{\varepsilon_s}{eN(x_{low}){x_{low}}^2} V_R \right). \tag{3.11}$$

The formulation above indicates that the zero-bias capacitor value is now $A\varepsilon_s / x'_{low}$, which will reduce the capacitance tuning range by a factor of x'_{low} / x_{low} for the same maximum depletion depth (x_{high}). Note that although the tuning range is reduced, the exponential $C(V_R)$ relation remains, and the IM_3 distortion cancellation condition is still valid. In addition, due to the same doping profile in the $N_a x^{-2}$ region, the exponent coefficient a_2 in (3.5) is unchanged. Later, we investigate the doping profile constraints for practical varactor implementations, which exhibit deviations from the ideal profile.

3.3.2 Varactor Diode Performance Tradeoffs

Based on the equations above, we can optimize the tuning range and quality factor of the varactor for a maximum reverse applied voltage (V_{R_max}). The maximum operation voltage (V_{R_max}), the series resistance R and the quality factor at zero applied voltage ($Q\big|_{V_R=0}$) of the varactor are given by:

$$V_{R\_\max} = \frac{eN(x_{low})x_{low}^{\ 2}}{\varepsilon_s}\left(\ln\frac{x_{high}}{x_{low}}\right) \tag{3.12}$$

$$R\big|_{V_R=0} = \int_{x_{low}}^{x_{high}} \rho(x)\frac{dx}{A} = \frac{1}{Ae\mu_n N(x_{low})x_{low}^{\ 2}}\left(\frac{x_{high}^{\ 3}}{3} - \frac{x_{low}^{\ 3}}{3}\right) \tag{3.13}$$

$$Q\big|_{V_R=0} = \frac{\left|\frac{1}{j\omega C}\right|}{R\big|_{V_R=0}} = \frac{3e\mu_n N(x_{low})}{\omega\varepsilon_s\left[\left(\frac{x_{high}}{x_{low}}\right)^3 - 1\right]} \tag{3.14}$$

where μ_n is the electron mobility.

Since the increase of the electric field due to the lightly doped spacer layer can be neglected, we can use the electric field at the boundary of lightly doped region (Region 1 in Fig. 3.2) and the $N_d x^{-2}$ region (Region 2 in Fig. 3.2) to estimate the peak electric field when the capacitor is just fully depleted ($V_R = V_{R\_max}$), which is given by

$$E_{full\_depletion} = \frac{eN(x_{low})x_{low}^{\ 2}}{\varepsilon_s}\left(\frac{1}{x_{low}} - \frac{1}{x_{high}}\right) \le E_{breakdown} \approx 6\times10^5 \quad \text{V/cm} . \tag{3.15}$$

Based on (3.9) and (3.12)-(3.15), the quality factor at zero bias can be rewritten as

$$Q\big|_{V_R=0} = \frac{3\mu_n \ln(T_{tune})}{\omega V_{R\_\max}(T_{tune}^3 - 1)}\left(\frac{T_{tune}E_{full\_depletion}}{T_{tune} - 1}\right)^2 . \tag{3.16}$$

Since the quality factor at zero bias is proportional to the square of $E_{full\_depletion}$ for a given tuning range and maximum reverse applied voltage, the quality factor can be optimized by dimensioning the varactor such that $E_{full\_depletion} = E_{breakdown}$, which is, for

silicon, approximately 6×10^5 V/cm [3]. Consequently, the maximum reverse applied voltage to deplete the varactor should be chosen close to the breakdown voltage of the varactor. Using this approach, the maximum achievable quality factors at zero bias (Q_{opt}) for different V_{R_max} and tuning ranges C_{max}/C_{min}) are listed in Table V for a silicon implementation.

Table V. Optimized calculated quality factor at 2 GHz for given tuning range (T_{tune}) and V_{R_max} ($\mu_n = 1000$ cm^2/V·s)

Tuning Range (T_{tune})	V_{R_max} = 5 V	V_{R_max} = 10 V	V_{R_max} = 20 V	V_{R_max} = 40 V
3	Q_{opt} = 1634	Q_{opt} = 817	Q_{opt} = 408	Q_{opt} = 205
	a_2 = 0.22 V^{-1}	a_2 = 0.11 V^{-1}	a_2 = 0.055 V^{-1}	a_2 = 0.028 V^{-1}
6	Q_{opt} = 206	Q_{opt} = 103	Q_{opt} = 52	Q_{opt} = 26
	a_2 = 0.36 V^{-1}	a_2 = 0.18 V^{-1}	a_2 = 0.09 V^{-1}	a_2 = 0.045 V^{-1}
9	Q_{opt} = 66	Q_{opt} = 33	Q_{opt} = 16	Q_{opt} = 8
	a_2 = 0.44 V^{-1}	a_2 = 0.22 V^{-1}	a_2 = 0.11 V^{-1}	a_2 = 0.055 V^{-1}
12	Q_{opt} = 30	Q_{opt} = 15	Q_{opt} = 7	Q_{opt} = 4
	a_2 = 0.50 V^{-1}	a_2 = 0.25 V^{-1}	a_2 = 0.12 V^{-1}	a_2 = 0.062 V^{-1}
15	Q_{opt} = 16	Q_{opt} = 8	Q_{opt} = 4	Q_{opt} = 2
	a_2 = 0.54 V^{-1}	a_2 = 0.27 V^{-1}	a_2 = 0.14 V^{-1}	a_2 = 0.070 V^{-1}

As indicated by (3.16), for a given fixed tuning range (T_{tune}), the optimized quality factor (Q_{opt}) is inversely proportional to the maximum operation voltage (V_{R_max}). The quality factor can be further improved through the use of wide bandgap materials, since these materials allow higher electric fields at the device junction and typically provide higher mobilities, enabling even higher quality factor values. For example, in GaAs an enhancement factor of 6 is feasible since $\mu_n = 6000$ cm^2/(V·s) and $E_{breakdown} = 6\times10^5$ V/cm , and in SiC even a factor of 25 is possible with $\mu_n = 900$ cm^2/(V·s) and $E_{breakdown} = 3\times10^6$ V/cm .

3.4 The Influence of IM_5 on the Linearity

3.4.1 Fifth-order Volterra Series Analysis

Although the exponential $C(V_R)$ relation is very effective in cancelling the third-order intermodulation (IM_3), and all even distortion products are canceled by the symmetric anti-series varactor configuration, fifth-order intermodulation (IM_5) is still present. In the following analysis of the fifth-order distortion, we use the same termination conditions at the center tap as for the IM_3 cancellation, i.e. $Z_c(f_2-f_1) = 0$, while $Z_c(f)$ is infinity for all other frequency components. Next, we substitute the $C(V_R)$ relation from (3.5) into the IM_5 formulation. To simplify the analysis, we assume $\Delta f \to 0$ and $Z_s(s) \to 0$, yielding the IM_5 products that appear at the IM_3 frequencies, $2f_1-f_2$ and $2f_2-f_1$, namely:

$$IM_5 \approx \frac{5}{768}\left(a_2 \hat{A}\right)^4 \tag{3.17}$$

where $a_2 = -\varepsilon_s / \left(eN(x_{low})x_{low}^{\ 2}\right)$ is the exponential coefficient of $C(V_R)$ relation (3.5) and $\hat{A}$ is the amplitude of the two-tone test signal at the fundamental frequencies. In order to be consistent with our further discussions, we replace $\hat{A}$ by V_{RF_peak}, which represents the peak amplitude of the two-tone input voltage signal. Hence, (3.17) becomes

$$IM_5 \approx \frac{5}{768} a_2^{\ 4} \left(\frac{V_{RF\_peak}}{2}\right)^4 . \tag{3.18}$$

Based on (3.18), the fifth-order input intercept point (IIP_5) can be expressed as

$$IIP_5 \approx 4 \cdot \left(\frac{48}{5}\right)^{1/4} \frac{1}{a_2} = \frac{7.04}{a_2} . \tag{3.19}$$

Note that the IIP_5 is independent of the applied control voltage at the center pin and only depends on the grading coefficient a_2, which can be chosen freely to adjust the tuning range. Practical values of a_2 are in the range of $0.028\,V^{-1}$ to $0.54\,V^{-1}$ (see Table V), yielding IIP_5 values of 12 V to 256 V. Since the IM_5 drops at the rate of 80 dB per decade, outstanding linearity can be achieved for even modest IIP_5 values.

3.4.2 Tradeoff between Linearity, Quality factor, V_{R_max} and Effective Tuning Range

The discussion in Section 3.2 did not account for the signal swing when calculating tuning range limits. In practical situations, the RF voltage swing will reduce the effective tuning range. For these reasons, it is useful to repeat the capacitance tuning range analysis for large-signal operation by including breakdown, forward biasing and linearity constraints.

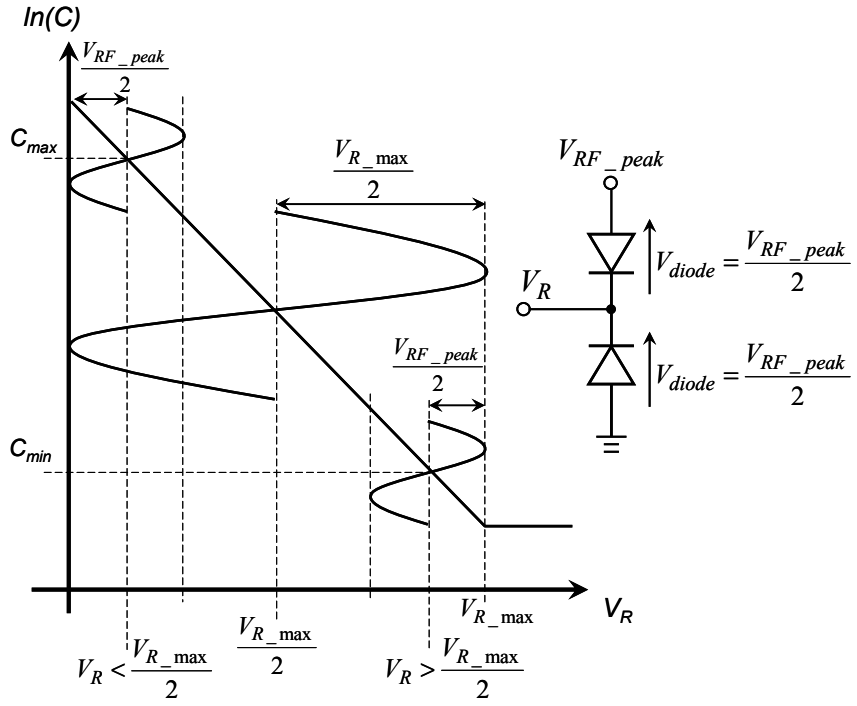


Fig. 3.3. Definition of effective tuning range. Note that by plotting *ln(C)* versus V_R, our desired exponential $C(V_R)$ relation appears as a straight line. This property will be used later to evaluate practical implementation of the varactor devices.

In order to maintain acceptable linearity, both varactor diodes in the stack must remain reverse-biased during large-signal operation and consequently the useful range of capacitance variation will be reduced by the magnitude of the applied RF signal (Fig. 3.3). For this reason, the tuning range of Section 3.2 is replaced by the effective tuning range, which is a function of V_{R_max} and V_{RF_peak}. Since the magnitude of the RF input signal is V_{RF_peak} and the RF impedance between node *c* and *d* in Fig. 3.1 is high, the RF voltage across each individual diode is roughly half of V_{RF_peak}. Hence, the DC bias

voltage at the center tap must be higher than $V_{RF\_peak}/2$ to avoid forward biasing and it must be lower than V_{R_max}-$V_{RF\_peak}/2$ to avoid breakdown.

As illustrated in Fig. 3.3, when the diode is biased at $V_{RF\_peak}/2$, the corresponding capacitor value is C_{max}, when the diode is biased at V_{R_max}-$V_{RF\_peak}/2$, the corresponding capacitor value is C_{min}. Therefore, the effective tuning range (T_{tune_eff}) can be written as

$$\begin{aligned} T_{tune\_eff} &= \exp\left[a_2 \left(V_{R\_\max} - V_{RF\_peak} \right) \right] \\ &= T_{tune} \exp\left(-a_2 V_{RF\_peak} \right) \end{aligned} \tag{3.20}$$

where T_{tune} is the original tuning range defined in (3.9). From (3.20), the $C(V_R)$ exponential a_2 can be expressed as a function of V_{R_max}, V_{RF_peak} and T_{tune_eff},

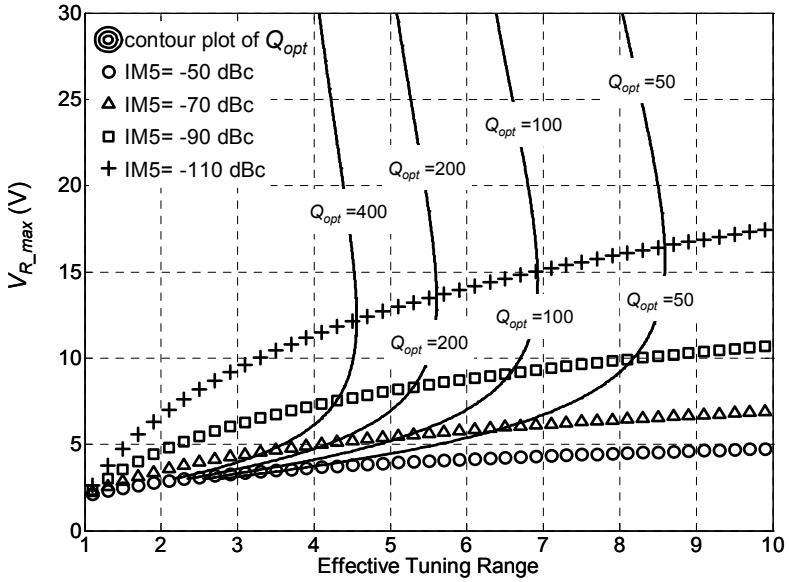
$$a_2 = \frac{\ln(T_{tune\_eff})}{V_{R\_\max} - V_{RF\_peak}}. \tag{3.21}$$

Substituting the formulation above into (3.20), the IM_5 can be written as

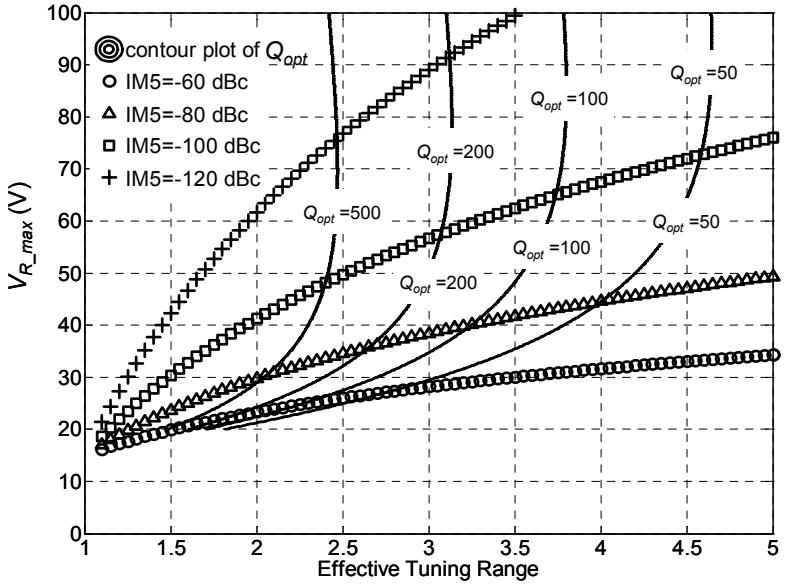
$$IM_5 = 4 \cdot 20 \log\left[\frac{\ln(T_{tune\_eff})}{7.04(V_{R\_\max} - V_{RF\_peak})} V_{RF\_peak} \right] \text{ (dBc).} \tag{3.22}$$

Based on (3.14), (3.15), (3.16) and (3.20), the optimized quality factor at zero bias (Q_{opt}) of the varactor can be rewritten as a function of V_{R_max}, V_{RF_peak} and T_{tune_eff}. Therefore, we can plot the effective tuning range, quality factor and V_{R_max} for different V_{RF_peak} values as shown in Fig. 3.4. In order to give an indication of the achievable performance, the calculation of Fig. 3.4 is based on the mobility of GaAs ($\mu_n = 6000$ cm^2/V$\cdot$s). For the silicon implementation, since the critical field at breakdown ($E_{breakdown}$) is within 10% of that of GaAs [3], one can approximate the quality factor by simply dividing the quality factor of GaAs by a factor of 5-6.

Fig. 3.4 shows the trade-off between quality factor and peak RF voltage. For example, if V_{RF_peak} is small (e.g. 2 V) we can achieve a quality factor of 400 for a device with a breakdown voltage of 12 V, an IM_5 limited linearity of -110 dBc and effective capacitance tuning range of 4:1 [Fig. 3.4 (a)]. In the case of a larger RF signal amplitude (e.g. 15 V), high tuning range, linearity and high breakdown voltage can still be achieved at the cost of higher control voltages and a lower quality factor [Fig. 3.4 (b)].



(a) $V_{RF\_peak} = 2$ V



(b) $V_{RF\_peak} = 15$ V

Fig. 3.4. Tradeoff of breakdown voltage, linearity, quality factor (solid lines) and effective tuning range (GaAs material with $\mu_n = 6000\ \text{cm}^2/\text{V}\cdot\text{s}$) for an RF signal with 2 V (a) and 15 V (b) amplitude. Note that V_{R_max} must be larger than V_{RF_peak} to avoid clipping and forward bias.

3.4.3 Influence of Center-Tap Impedance on Linearity

The narrow tone-spacing varactor stack proposed here requires zero center-tap impedance for the baseband frequencies and infinitely high impedance for all the higher harmonic frequencies. Note that this center-tap impedance requirement is relative to the impedance offered by the varactor capacitance itself at these frequencies. In practical implementations, this can be a single resistor or an inductor, since the capacitive reactance of the varactor stack itself exhibits relatively high impedance at low tone spacing. Fig. 3.5 shows the simulated two-tone linearity of the narrow tone-spacing varactor stack with resistive and inductive center-tap impedance respectively, as measured by the dBc ratio of the fundamental and distortion current (at $2f_1$-f_2) as a function of the tone spacing of the RF input signal (Δf).

From Fig. 3.5, we observe that the narrow tone-spacing varactor stack behaves linear at narrow tone spacing as expected and less linear for large tone spacing. Note that the tone spacing range of the resistive center tapped narrow tone-spacing varactor stack can be extended with a smaller resistance value, but this would reduce the quality factor. Detailed analysis indicates that the product of the 6 dB corner frequency (Δf_{corner}), which is defined as the tone spacing frequency (f_1-f_2) from which the linearity of the narrow tone-spacing varactor stack expressed in dBc degrades by 6 dB, and the quality factor at zero bias (only considering the influence of the resistive center-tap impedance) is a constant value for silicon of

$$\Delta f_{corner} \cdot Q = \frac{5a_2^2 V_{R\_\max}^2 f_{RF} \exp(a_2 V_{\max}/2)}{\sqrt{36864 - 25a_2^4 V_{R\_\max}^4}} \tag{3.23}$$

In this example, this product equals to 4.1×10^8 Hz. If a 1.2 kΩ center-tap resistor is applied, a 6 dB corner frequency (Δf_{corner}) around 1.5 MHz and a quality factor of 300 at zero bias can be achieved. It is important to note that for very low values of the center-tap resistor, the quality factor of the varactor stack will be reduced. For this reason, an inductive center-tapped narrow tone-spacing varactor stack can provide better performance, since it facilitates a linear operation for larger tone spacing (above 10 MHz) without lowering the quality factor. However, for varactor stacks with a low capacitance value, a large inductor value is required to achieve the sufficiently high impedance at the fundamental RF frequency. A more advanced center-tap impedance network can increase the linear bandwidth of the proposed narrow tone-spacing varactor stack to much larger values, as long as it provides a low impedance for the baseband and a high impedance for all higher harmonics.

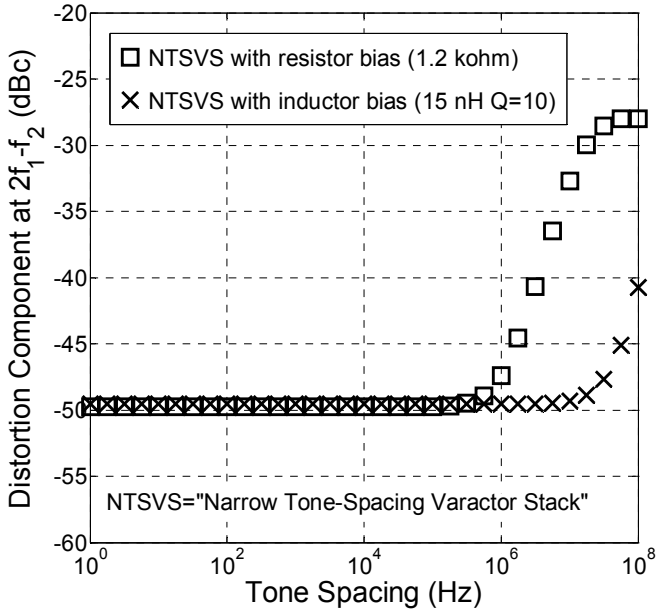


Fig. 3.5. Simulated capacitive current distortion component at $2f_1$-f_2 versus the tone spacing of the input RF voltage signal (a_1 = 0.358 V^{-1} , V_{R_max} = 5 V, V_R = 2.5 V, V_{RF_peak} = 5 V, f_{RF_center} = 2 GHz and $C_{zero\ bias}$ = 5 pF) for the narrow tone-spacing varactor stack circuits.

3.5 The Influence of Process Variation on Linearity

3.5.1 Process Tolerance

Besides the required harmonic terminations, the main issue for the linearity of the proposed narrow tone-spacing varactor stack is the exponential $C(V_R)$ relation, which requires a $N_d x^{-2}$ doping profile as shown in Fig. 3.2. However, in practice, the actual doping profile will deviate somewhat from the desired profile due to process variations.

In Section 3.1 we found that, as long as the $C(V_R)$ relation can be described by (3.5), the IM_3 distortion will be cancelled. Referring to the derivation of the $C(V_R)$ relation in Appendix *B*, there are two deviations of the profile that will cause a violation of the exponential $C(V_R)$ relation:

1) The doping concentration is not proportional to $1/x^2$.

2) The thickness of the spacer layer is not equal to x_{low}, resulting in an offset of the origin of the $N_d x^{-2}$ region.

Note that a doubling of the distance with the junction should result in one-fourth the doping concentration. If the origin of the $N_d x^{-2}$ region changes, this condition is violated.

For the first case, we can assign an arbitrary power (m) for the exponent of the doping concentration, and consequently the $C(V_R)$ relation (see Appendix C) can be written in an explicit form:

$$C(V_R) = A\frac{\varepsilon_s}{x_0(V_R)} = \frac{A\varepsilon_s}{\left[\frac{\varepsilon_s(m+2)V_R x_{low}^m}{eN(x_{low})} + x_{low}^{m+2}\right]^{\frac{1}{m+2}}}. \tag{3.24}$$

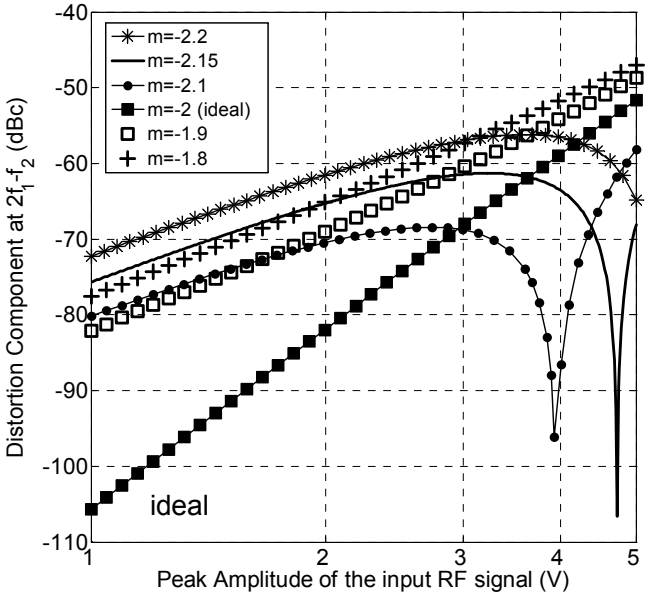
For the second case, we can assume the origin of the distance (x) is offset by a factor of Δx and consequently the $C(V_R)$ relation (see Appendix D) can only be written in an implicit form:

$$V_R = \frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left[\ln\left(\frac{\frac{A\varepsilon_s}{C} - \Delta x}{x_{low}}\right) + \frac{\Delta x}{x_{low}} - \frac{\Delta x}{\frac{A\varepsilon_s}{C} - \Delta x}\right]. \tag{3.25}$$

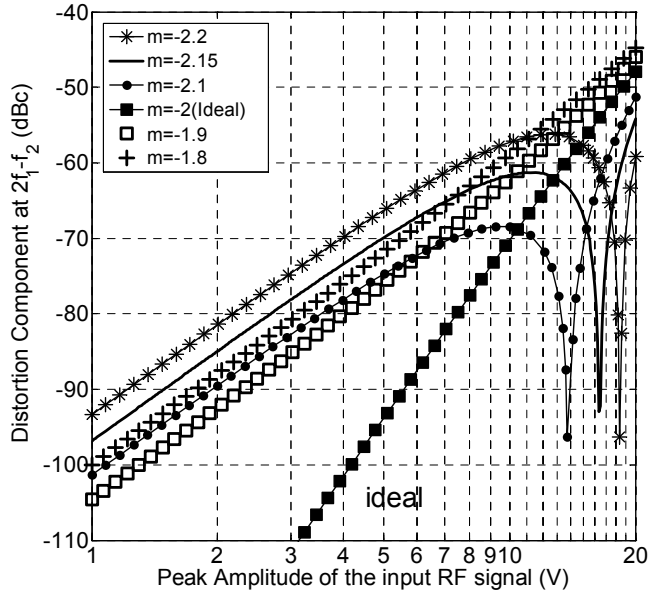
3.5.2 The Influence on Linearity due to Process Deviation of the Power Law Exponent (m)

Using (3.24), we can analyze the influence of a deviation of the power coefficient from the ideal m = -2 case using the Advanced Design System (ADS) Harmonic Balance simulator [4]. Fig. 3.6 show the simulated nonlinear capacitive current at $2f_1$-f_2, which is composed of IM_3 and IM_5 contributions, relative to the fundamental as a function of the RF signal amplitude (V_{RF_peak}), with Fig. 3.6(a) for low-voltage (V_{R_max} = 5 V) and Fig. 3.6(b) for high-voltage (V_{R_max} = 20 V) applications. Note that the simulator does not separate the IM_3 and IM_5 contributions, but they can be distinguished by their slopes.

In Fig. 3.6, the slope of the line for m = -2 is -80 dB/decade as predicted by (3.18). One may find the IIP_5 by extrapolating the line with m = -2 to 0 dBc in Fig. 3.6, which yields IIP_5 values of 21 V and 74 V respectively - consistent with (3.19). The slope of the lines with m = -1.8 and m = -1.9 is roughly -40 dB/decade when V_{RF_peak} is small, which indicates that the third-order distortion component is the dominant factor for nonlinearity at this drive level; with the increase of V_{RF_peak}, the slope becomes larger and finally the slope is similar to that of the line with m = -2.



(a) V_{R_max} = 5 V, T_{tune} = 6, V_R = 2.5 V and IIP_{5_ideal} = 21 V



(b) V_{R_max} = 20 V, T_{tune} = 6, V_R = 10 V and IIP_{5_ideal} = 74 V

Fig. 3.6. Simulated current distortion component at $2f_1$-f_2 in dBc versus the magnitude of the input RF signal when m is not equal to -2 using the simulation setup of Fig. 3.1. Note that since this is a voltage driven situation, the results are insensitive to the actual varactor capacitance (f_{RF_center}=2 GHz).

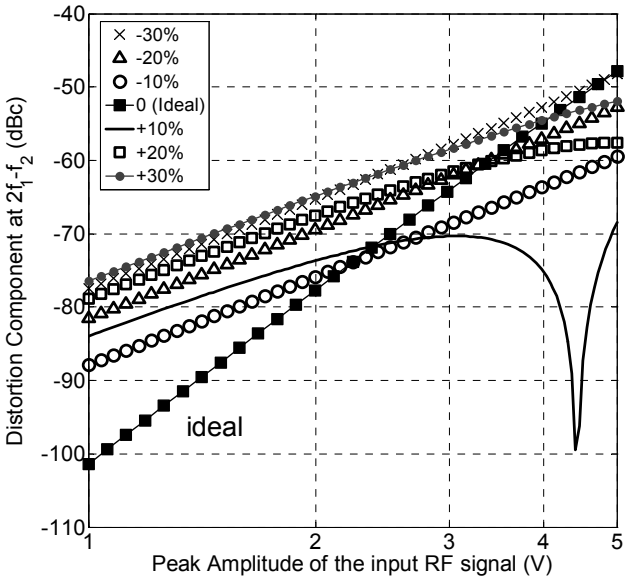
Note that the lines with m = -2.1, -2.15 and -2.2 are clearly different from the others. The reason for this is that when V_{RF_peak} is small, third-order distortion constrains the linearity; when V_{RF_peak} increases, the fifth-order term becomes important and cancellation effects occur at a certain power level, since the fifth-order distortion term has an opposite sign to the third-order term. Consequently, when V_{RF_peak} continues to increase, the fifth-order terms dominate and the nonlinearity has a similar slope as the line for the m = -2 case. The third-order and fifth-order distortion cancellation phenomenon does not occur with m = -1.9 and -1.8, because the third-order and the fifth-order distortion terms have the same sign for these two cases.

To define the fabrication window of the varactor, one may specify a linearity requirement as -60 dBc (sufficient for most applications) and check the acceptable range of m and V_{RF_peak} from Fig. 3.6. The maximum V_{RF_peak} which still results in a distortion component smaller than -60 dBc, becomes larger and larger when m approaches -2.15, due to the third-order and the fifth-order distortion cancellation which occurs when $m < -2$. On the other hand, the existence of the third-order distortion term with the same sign as the fifth-order distortion term will degrade the linearity for $m > -2$. Note that, since the distortion component exceeds the -60 dBc limit for $m < -2.15$ (Fig. 3.6), the acceptable range of V_{RF_peak} values for this linearity constraint will drop drastically for smaller m values.

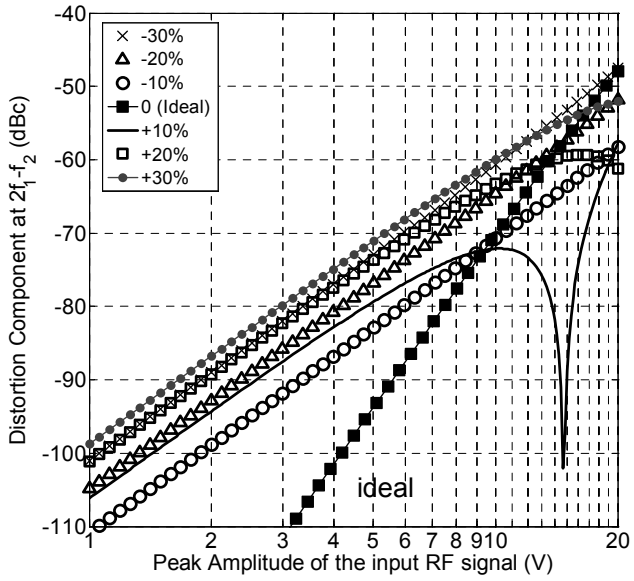
Consequently, when using a varactor with m in the range of -1.85 and -2.15, a very high linearity can be achieved. The most remarkable conclusion is found for values of m close to -2.15. For this value of m, two-tone signals will not generate any significant distortion (i.e., distortion is less than -60 dBc) as long as their peak amplitude does not exceed the maximum control voltage (device breakdown) or drive one of the diodes into forward conduction.

3.5.3 Effect of Spacer Layer Thickness (x_{low}) Variation on Linearity

Using (3.25), we can analyze the influence of variations in the spacer layer thickness on linearity using the ADS Harmonic Balance simulator. The simulated nonlinear capacitive current at $2f_1$-f_2 for the low-voltage (V_{R_max} = 5 V) and high-voltage (V_{R_max} = 20 V) applications are shown in Fig. 3.7 (a) and (b) respectively. It demonstrates that when the spacer layer thickness is larger than x_{low} ($\Delta x > 0$), the third-order and fifth-order distortion cancel for higher input voltages; when the spacer layer thickness is smaller than x_{low} ($\Delta x < 0$), no cancellation occurs and the third-order distortion dominates the nonlinearity.



(a) V_{R_max} = 5 V, T_{tune} = 6, V_R = 2.5 V and IIP_{5_ideal} = 21 V



(b) V_{R_max} = 20 V, T_{tune} = 6, V_R = 10 V and IIP_{5_ideal} = 74 V

Fig. 3.7. Simulated current distortion component at $2f_1$-f_2 versus magnitude of the input RF signal when the spacer layer thickness is not equal to x_{low}. Note that since this is a voltage driven situation, the results are insensitive to the actual varactor capacitance (f_{RF_center} = 2 GHz).

We may again specify a linearity requirement of -60 dBc and check the acceptable range of Δx and V_{RF_peak}. We find that when the spacer layer thickness deviation is in the range of ±20% we meet the linearity requirement. When $\Delta x > 0$ the acceptable range of V_{RF_peak} is increased and for values of $\Delta x < 0$ it is decreased.

In conclusion, the proposed varactor concept, in terms of linearity, has a very reasonable fabrication window to allow a reliable production of this new device type.

3.6 Wide Tone-Spacing Varactor Stack

Up till now, we have discussed the narrow tone-spacing varactor stack which offers the highest linearity for inband signals. Next, we will evaluate the wide tone-spacing varactor stack configuration that also makes use of the same exponential $C(V_R)$ relationship but provides highest linearity for out of band signals, e.g. signals with high tone spacing.

3.6.1 Third-Order and Even-Order Distortion Cancellation

The high-linearity wide tone-spacing varactor stack configuration with four diodes in the anti-series / anti-parallel connection is a special case of the high tuning range varactor stack proposed in [1] and is shown in Fig. 3.8. We consider the third-order intermodulation (IM_3) current through the source impedance at frequency ($2f_1$-f_2), which we will determine using Volterra analysis [2].

The center-tap impedance is set to infinity for all frequency components present in the circuit [$Z_c(s) \equiv \infty$] and the ratio of the diode areas (D_1/D_2) is set to X. For simplicity, we assume the frequencies of the two-tone voltage source are identical ($f_1 \approx f_2 \approx f_{RF}$). The resulting expression for the IM_3 is

$$IM_3\Big|_{Z_c(s)\equiv\infty} = \left| -\frac{3(c_0c_2X^2 - 2c_1^2X - c_0c_2X + c_0c_2)(X+1)\hat{A}^2}{4c_0^2(2Xs_{RF}c_0Z_s(-s_{RF}) - X - 1)(2Xs_{RF}c_0Z_s(s_{RF}) + X + 1)^2} \right| \tag{3.26}$$

where $c_0 = C(V_R)$, $c_1 = \frac{1}{2}\frac{dC(V_R)}{dV_R}$, $c_2 = \frac{1}{6}\frac{d^2C(V_R)}{d^2V_R}$ are the capacitance Taylor coefficients of each varactor diode with V_R being the reverse applied voltage with a positive value; $Z_s(s)$ is the source impedance; s_{RF} is the complex RF center frequency ($j\omega_{RF}$) of the two-tone signal and $\hat{A}$ represents the voltage amplitude of the source

signal. Since we aim for integration in the same technology as the narrow tone-spacing varactor stack, the proposed configuration will share the doping profile with the related $C(V_R)$ relation as expressed in (3.5), i.e., $c_0 = a_1 \exp(-a_2 V_R)$, where a_1 and a_2 are the doping profile dependent coefficients. By substituting (3.5) into (3.26), (3.26) can be simplified as,

$$IM_3\Big|_{Z_c(s)\equiv\infty} = \left| -\frac{(X^2-4X+1)(X+1)a_2^2 \hat{A}^2}{8(2Xs_{RF}c_0Z_s(-s_{RF})-X-1)(2Xs_{RF}c_0Z_s(s_{RF})+X+1)^2} \right| \qquad (3.27)$$

which yields the required diode area ratio for IM_3 cancellation namely: $X = 2 \pm \sqrt{3}$. Note that this cancellation condition is independent of the source impedance $Z_s(s)$ and the particular values of a_1 and a_2.

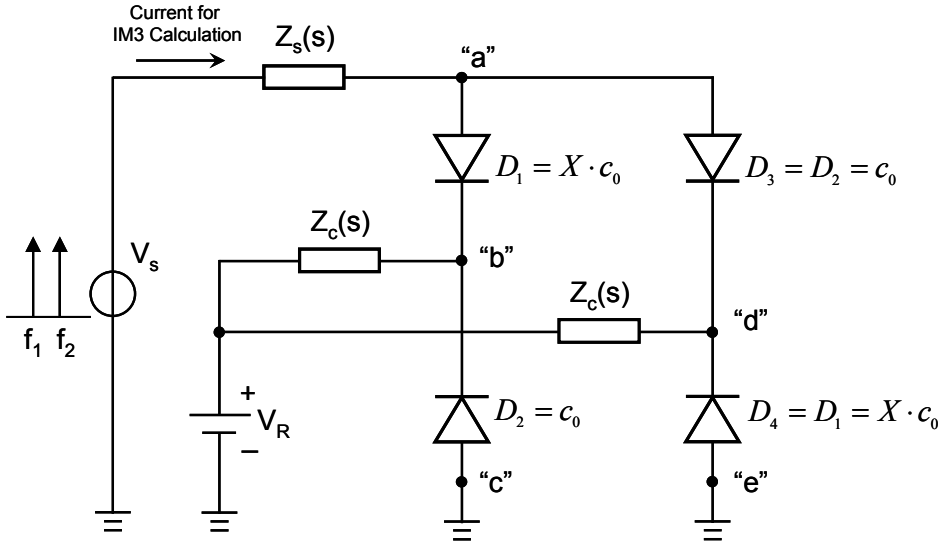


Fig. 3.8. Schematic of the anti-parallel/anti-series connection of the diodes with exponential $C(V_R)$ relation.

The anti-parallel/anti-series topology enforces opposite phases of the even-order nonlinear current sources, so no even-order components leave the varactor structure. To illustrate this point, consider the second-order Volterra series of the schematic shown in Fig. 3.9.

The second-order Volterra kernel for the voltage at input node *a* is

$$H_{2_a}(s_1,s_2)=\frac{\left[X(I_{NL2_{D2}}-I_{NL2_{D3}})-(I_{NL2_{D1}}-I_{NL2_{D4}})\right]Z_s(s_1+s_2)}{2(s_1+s_2)Xc_0Z_s(s_1+s_2)+X+1}=0 \qquad (3.28)$$

where

$$I_{NL2_{D2}}=I_{NL2_{D3}}=\frac{(s_1+s_2)X^2c_1}{\left[2s_1Xc_0Z_s(s_1)+X+1\right]\left[2s_2Xc_0Z_s(s_2)+X+1\right]} \qquad (3.29a)$$

and

$$I_{NL2_{D1}}=I_{NL2_{D4}}=\frac{(s_1+s_2)Xc_1}{\left[2s_1Xc_0Z_s(s_1)+X+1\right]\left[2s_2Xc_0Z_s(s_2)+X+1\right]} \qquad (3.29b)$$

are the second-order nonlinear current sources. From (3.28), it is clear that as long as the mismatch of D_1-D_4 and D_2-D_3 is small, $H_{2_a}(s_1,s_2)$ will be close to zero, and no second-order distortion current flows into the source impedance. Therefore, no second-order voltage components will develop across the varactor structure and *secondary mixing* (which can lead to third-order intermodulation) is avoided; this yields an IM_3 cancellation condition independent of source impedance. A more elaborate analysis shows that *all* even-order distortion components vanish, resulting in a tunable capacitor with no residual distortion with an order lower than five.

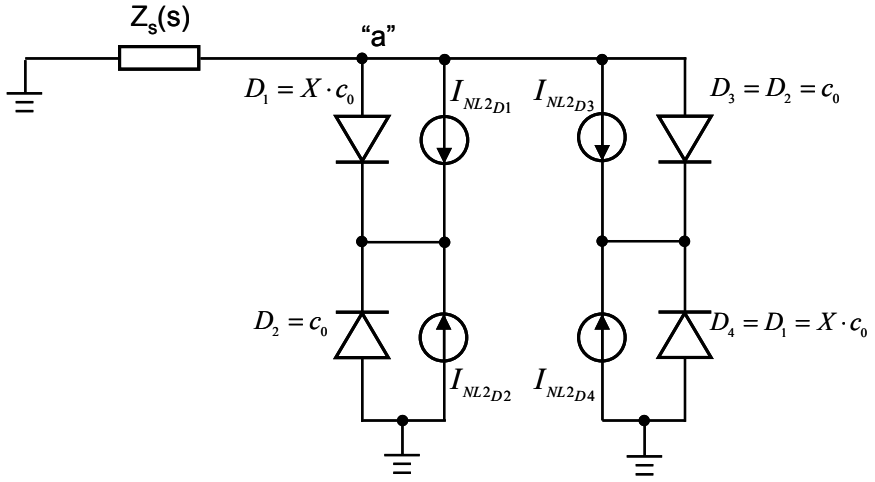


Fig. 3.9. Circuit for the computation of second-order kernels of the circuit of Fig. 3.8.

3.6.2 Influence of Fifth-Order Distortion on Linearity

Although this approach is very effective in cancelling the third-order (IM_3) and all even-order intermodulation, fifth-order intermodulation (IM_5) is still present. When solving for the fifth-order Volterra series, we assume $Z_c(s) \equiv \infty$ for the center-tap connections and $X = 2 \pm \sqrt{3}$. Next, we substitute the $C(V_R)$ relation (3.5) into the IM_5 formulation. To simplify the analysis, we assume $f_1 \approx f_2 \approx f_{RF}$ and $Z_s(s) \to 0$, providing us the IM_5 products that appear at $2f_1$-f_2 and $2f_2$-f_1, namely:

$$IM_5 \approx \frac{5}{288}\left(a_2 \hat{A}\right)^4 \tag{3.30}$$

where a_2 is the exponential coefficient of the $C(V_R)$ relation (3.5) and $\hat{A}$ is the voltage amplitude of the two-tone test signal at the fundamental frequencies. This situation represents the worst-case condition, since for $Z_s(s) \to 0$, all fifth-order current will flow through the source impedance, which approximates a short-circuit condition.
Based on (3.30), the fifth-order input intercept point (IIP_5) can be expressed as

$$IIP_5 \approx \frac{2.75}{a_2} \text{ (V)}. \tag{3.31}$$

The resulting linearity is independent of the reverse bias voltage. In order to be consistent with further discussions, we replace $\hat{A}$ with V_{RF_peak}, which is the peak amplitude of the two-tone input voltage signal. Hence, (3.31) can be rewritten as

$$IM_5 \approx \frac{5}{288} a_2^4 \left(\frac{V_{RF\_peak}}{2}\right)^4. \tag{3.32}$$

In practical cases, the value of a_2 varies from 0.028 V^{-1} to 0.54 V^{-1} as shown in Table V, yielding IIP_5 values of 5.1 V to 98.4 V. Note that since the IM_5 drops at the rate of 80 dB per decade, outstanding linearity can be achieved for even modest IIP_5 values.

3.6.3 Influence of Center-Tap Impedance on Linearity

In the previous section, it was assumed that the center-tap impedance (Z_c) is infinite for all frequency components, so it has no influence on the RF operation. In practical situations, this requires that the center-tap impedances should be much higher than the AC impedances of the varactors themselves. This requirement is difficult to fulfill for the baseband frequency component of a two-tone signal (f_2-f_1) when the tone

spacing approaches zero. For the resulting baseband frequency, the capacitive reactance of the varactors increases without bound as the tone spacing approaches zero. Consequently, there is a lower frequency limit of tone spacing where the third-order distortion cancellation is violated; hence this configuration is called the wide tone-spacing varactor stack.

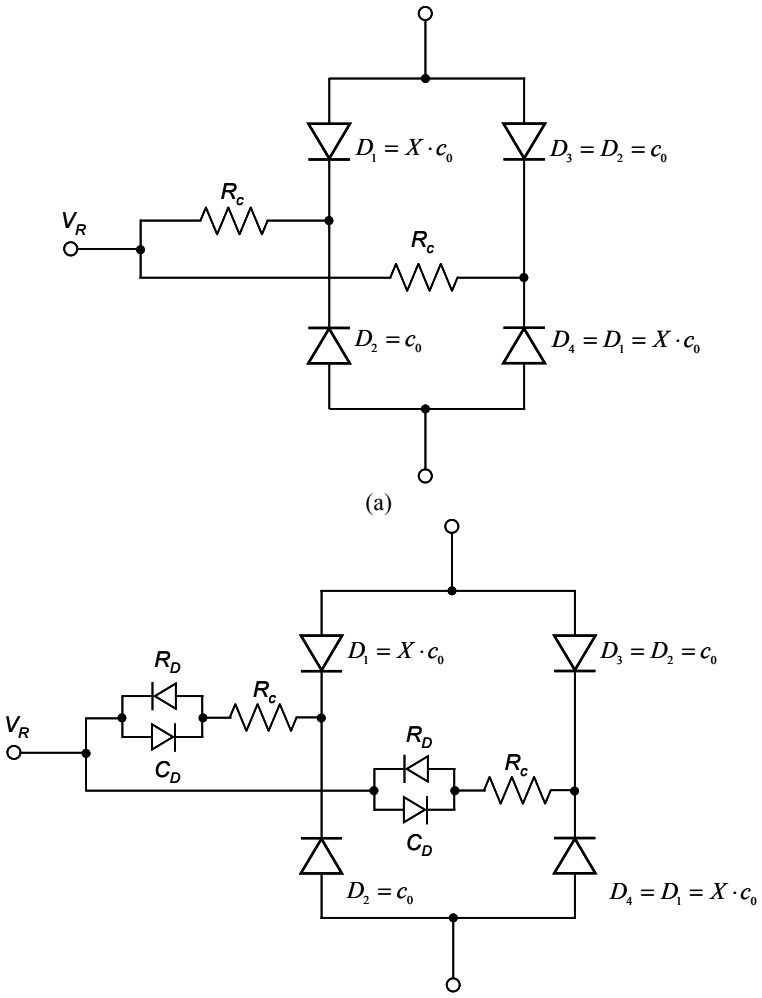


Fig. 3.10. (a) Wide tone-spacing varactor stack configuration with resistor bias. (b) Wide tone-spacing varactor stack configuration with resistor and anti-parallel diode bias for linearity improvement at low-tone spacing.

In practical implementations of the wide tone-spacing varactor stack, similar to what has been done for the uniformly doped distortion-free varactor stack

configuration in [1] and [5], an integrated resistor [see Fig. 3.10 (a)] can be used for the dc biasing networks of the center-tap. For a wide tone-spacing varactor stack configuration as depicted in Fig. 3.8, using resistive center-tap connections, the simulated distortion components at $2f_1$-f_2 as function of tone spacing (f_2-f_1) are depicted in Fig. 3.11, which confirms the conclusion above. When the tone spacing is relatively small, the third-order distortion is no longer canceled, and the IM_3 distortion has a value of

$$IM_3\Big|_{\Delta f\to 0, Z_c\neq\infty} \approx \frac{1}{24}a_2^2\left(\frac{V_{RF\_peak}}{2}\right)^2. \tag{3.33}$$

With the increase of tone spacing, the impedance of the varactor drops and at a certain frequency (above 4 MHz) it becomes much smaller than the center-tap impedance, yielding the improved linearity as predicted by (3.32). For the resistive center-tap configuration, the corner frequency (marked in Fig. 3.11), where the linearity starts to approach the fifth-order distortion dominated regime, can be approximated by

$$\Delta f_{corner} = \frac{\left(96+5a_2^2V_{RF\_peak}^2\right)(2-\sqrt{3})}{10(9-5\sqrt{3})\pi R_c c_0 a_2^2 V_{RF\_peak}^2} \tag{3.34}$$

where R_c is the center-tap resistance. As one can observe, the corner frequency is inversely proportional to the product of the center-tap resistance and the varactor capacitance. In order to improve the linearity performance at low-tone spacing, the center-tap configuration [shown in Fig. 3.10(b)] with a series resistor and anti-parallel diode bias was proposed in [1], [5], whose effect can be observed in Fig. 3.11. If the anti-parallel diodes are not forward biased, they provide very high impedance extending the high linearity operation of the wide tone-spacing varactor stack to very low-tone spacing.

Note that for this configuration, the dc leakage current of the reverse-biased diodes will limit the linearity at ultra-low tone spacing, since this yields a drop in their AC impedance (R_D), violating the condition for the center tap. For slightly higher tone spacings the zero-bias capacitance C_D of the anti-parallel diode pair limits the IM_3 to a small constant value, consequently it is best to use small diodes in the center-tap connection. Above the corner frequency (in this case approximately 40 MHz), defined by (3.34), fifth-order distortion constrains the linearity. Note that the corner frequency is ten times larger than the single resistor case [see Fig. 3.10(a)], since R_c (100 kΩ) is ten times smaller, which is consistent with (3.34). Fig. 3.11 shows that the wide tone-spacing varactor stack clearly offers superior linearity over the single diode (with comparable effective capacitance), especially at relatively large tone spacing.

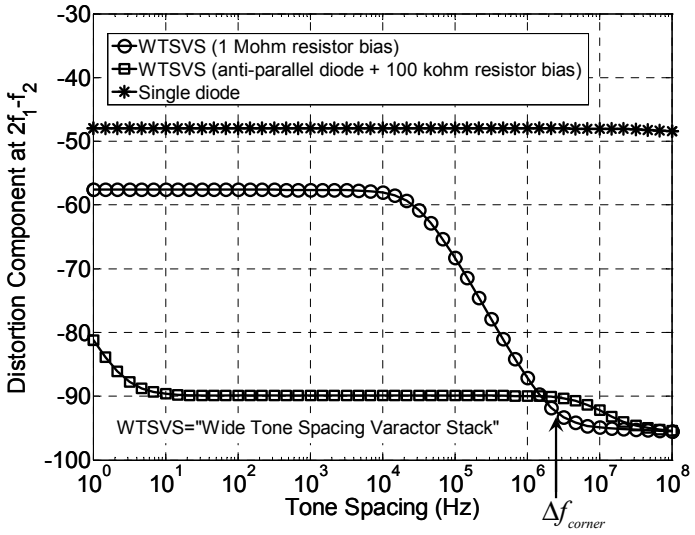


Fig. 3.11. Simulated capacitive current distortion component at $2f_1$-f_2 as a function of input signal tone spacing (V_R = 2.5 V, V_{RF_peak} = 1 V, f_{RF_center} = 2 GHz), for a wide tone-spacing varactor stack with an effective zero bias capacitance of 4.2 pF, (a_2 = 0.358 V^{-1}, $X = 2 - \sqrt{3}$, C_D = 0.1 pF) and single diode with the same zero bias capacitance and a_2.

3.7 Conclusions

Two highly linear varactor configurations have been introduced, which act as enablers for the realization of future adaptive transmitters, receivers and linear capacitive modulators. When considering their linearity versus tone spacing, the wide tone-spacing varactor stack and the narrow tone-spacing varactor stack designs offer complementary linearity behavior. The wide tone-spacing varactor stack provides the best linearity for signals that have a relatively large frequency spacing (several hundred kilohertz). This property makes it most suited for (adaptive) receiver applications where cross modulation of the "weak" desired signals by strong out-of-band interferers should be avoided. In (adaptive) transmitting systems, however, the in-band linearity will be the biggest concern. For these applications the narrow tone-spacing varactor is recommended, since it provides the highest linearity for in-band signals (up to ten's of MHz's). The complimentary linearity behavior of the proposed varactor configurations makes them very suitable to handle the different requirements of adaptive receivers and transmitters in a single varactor technology.

The first proposed structure, i.e., narrow tone-spacing varactor stack, exhibits a high capacitance tuning range, low-control voltages and excellent linearity for in-band

modulated signals in contrast to other known solutions. The proposed solution is based on two identical varactors with an exponential $C(V_R)$ relation in anti-series configuration. For this topology, IM_3 cancellation can be achieved, provided that the proper harmonic terminations are applied to its terminals. When the IM_3 products are successfully cancelled, the remaining distortion is extremely low and dominated by IM_5 products, which decrease in back-off very rapidly due to their fifth-order dependency. The related IIP_5 voltage proves to be independent of the applied control voltage, which guarantees high linearity even at very low control voltages.

The implementation tradeoffs to achieve a good compromise between, quality factor, (effective) tuning-range, breakdown voltage, linearity and RF signal handling have been given. The feasibility of practical implementations has been demonstrated by evaluating the influence of process spread on the linearity. This study indicates a very workable process window for the realization of the required doping profile.

With the information provided, the proposed narrow tone-spacing varactor stack can easily be optimized for the implementation of tunable filters, capacitive switches, adaptive matching networks, phase shifters, antenna mismatch correction or capacitive modulators. The unique feature of this novel varactor topology, compared to the distortion-free varactor stack and MEMS varactors, is its high modulation frequency for operation and high linearity for signals with low tone spacing, making it suitable for the next generation of adaptive handsets featuring multi-band / multi-mode operation.

The second proposed varactor configuration, i.e., wide tone-spacing varactor stack, exhibits the highest linearity for modulated signals with wide tone spacing, and it is a direct derivation of the earlier proposed high tuning range varactor stack. For this reason, it preserves all the merits of the high tuning range varactor stack and provides complementary linearity behavior to the narrow tone-spacing varactor stack. In addition, the fact that it shares the same diode $C(V_R)$ depletion capacitance relation with the narrow tone-spacing varactor stack makes it possible to integrate both varactor configurations in a single technology.

Their integration capabilities, compact size, high reliability, low-cost implementation, high speed, high quality factor, and free choice of tuning and control voltage range make them very interesting components for the implementation of ultra-linear high-performance adaptive RF systems.

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Chapter 4

Comparison of the Varactor Configurations

In Chapter 2, tunable RF components have been reviewed for their performance. In view of this discussion, the previously proposed distortion-free varactor stack and high tuning range varactor stack have been extensively discussed for their benefits and shortcomings. In order to overcome their main drawbacks, the narrow tone-spacing varactor stack and wide tone-spacing varactor stack have been introduced in Chapter 3. Although these four semiconductor-based varactor configurations make use of IM_3 cancellation for improved linearity and share some common properties, they do differ in their implementation, linearity versus modulation bandwidth, area, power handling, tuning range etc. Therefore, as guideline for selecting the most proper semiconductor-based varactor configurations for a given application, we give an overview of the diode based varactor configurations and their properties in this chapter. First, all varactor stack types, aiming for the IM_3 cancellation, are compared in general with single diodes. In Section 4.2, a design example of linear modulator is chosen for comparing its capability to modulate signals. In Section 4.3, the multi-stack topology is used to further improve the linearity and power handling while its linearity enhancement over single varactor stack is compared. In Section 4.4, the system-level response of the different varactor configurations are compared under different bandwidth or data-rate conditions. Finally, we conclude this chapter in Section 4.5.

4.1 Varactor Configurations and their Performance in General

All known types of the varactor stack [1]-[6], providing a tunable capacitance between their RF terminals without introducing nonlinear signal distortion, are compared in Table VIa and VIb in terms of the $C(V_R)$ relation, doping profile,

harmonic conditions, topology, area ratio for IM_3 cancellation, total area for the unit capacitance (relative to single diode), power handling capability and linearity.

Table VIa. Performance comparison of distortion-freevaractor stack [1], [4], high tuning range varactor stack [4] and the single diode with hyper-abrupt doping profile

	single diode [classic $C(V_R)$]	distortion-free varactor stack	high tuning range varactor stack
$C(V_R)$ relation	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-n}$ ($V_R > 0$, $V_j > 0$)	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-0.5}$	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-n}$ ($n > 0.5$)
Doping profile	$N_d x^{\left(\frac{1}{n}-2\right)}$	N_d constant	$N_d x^{\left(\frac{1}{n}-2\right)}$ ($n > 0.5$) hyper-abrupt
Topology	**single** no center-tap impedance	**anti-series** infinite center-tap impedance for all frequencies	**anti-series/ anti-parallel** infinite center-tap impedance for all frequencies
Area ratio for IM_3 cancellation	no cancellation	1:1	$X=\frac{4n+1+\sqrt{12n^2-3}}{2(n+1)}$
Total area for unit capacitance	A	$4A$	$\frac{(1+X)^2}{X}A$
Maximum V_{RF_peak}	$\frac{1}{2}V_{\max}$	$V_{\max}$	$\frac{1}{2}\left(1+\frac{1}{X}\right)V_{\max}$
IP_2	at f_1+f_2 $\frac{V_R+V_j}{n}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_3 at $2f_1-f_2$	$\frac{2\sqrt{2}(V_R+V_j)}{\sqrt{n(n+1)}}$	for big Δf ∞	for big Δf ∞
IP_4	at f_1+f_2 $\frac{\sqrt[3]{4}(V_R+V_j)}{\sqrt[3]{n(n+1)(n+2)}}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_5 at $2f_1-f_2$	$\frac{2\sqrt{6}(V_R+V_j)}{\sqrt[4]{15n(n+1)(n+2)(n+3)}}$	for large Δf ∞	for large Δf $2.72(V_R+V_j)$ ($n=1, X=2$)

Table VIb. Performance Comparison of narrow tone-spacing varactor stack [5], wide tone-spacing varactor stack [6] and the single diode with $N_d x^{-2}$ doping profile

	single diode [exponential $C(V_R)$]	narrow tone-spacing varactor stack	wide tone-spacing varactor stack
$C(V_R)$ relation	$C_{j0}\exp(-a_2 V_R)$	$C_{j0}\exp(-a_2 V_R)$	$C_{j0}\exp(-a_2 V_R)$
Doping profile	$N_d x^{-2}$	$N_d x^{-2}$	$N_d x^{-2}$
Topology	**single** no center-tap impedance	**anti-series** $Z_c(s)$: short for baseband open for all other frequencies	**anti-series/ anti-parallel** infinite center-tap impedance for all frequencies
Area ratio for IM_3 cancellation	no cancellation	1:1	$X = 2 \pm \sqrt{3}$
Total area for unit capacitance	A	$4A$	$6A$
Maximum V_{RF_peak}	$\frac{1}{2}V_{\max}$	$V_{\max}$	$\frac{1}{2}\left(1+\frac{1}{2+\sqrt{3}}\right)V_{\max}$
IP_2	at f_1+f_2 $\frac{1}{a_2}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_3 at $2f_1-f_2$	$\frac{2\sqrt{2}}{a_2}$	for small Δf ∞	for large Δf ∞
IP_4	at f_1+f_2 $\frac{\sqrt[3]{4}}{a_2}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_5 at $2f_1-f_2$	$\frac{2\sqrt{6}}{\sqrt[4]{15}a_2}$	for small Δf $\frac{3.52}{a_2}$	for large Δf $\frac{2.75}{a_2}$

Note that the IP_2, IP_3, IP_4 and IP_5 are expressed in voltage amplitude of each testing tone at f_1 and f_2 instead of V_{RF_peak} and the total area for unit capacitance is relative to the single diode assuming the area required for unit capacitance for the single diode is A.

When comparing the linearity performance of the different varactor stacks with the single diode, it indicates that all of the varactor stacks, with suitable harmonic terminations, outperform the single diode since the distortion components with the order less than five are all cancelled and the residual fifth-order distortion at $2f_1$-f_2 is extremely low. For the varactor stacks, the anti-series configurations [see Fig. 4.1 (b) and (c)] are generally used and the applied RF voltage will be distributed on two series diodes, hence the maximum allowable V_{RF_peak}, which is constrained by the forward bias and breakdown condition, will be correspondingly increased, yielding better power handling capability and linearity. The only cost of the anti-series connection topology is the extra chip area required to implement the same capacitance value, but this drawback is dramatically compensated by the much higher capacitance density compared to that of the MEMS counterpart.

The varactor configurations that feature infinity high center-tap impedance(s) can be linked to each other by considering their required area ratio for IM_3 cancellation. E.g. for the high tuning range varactor stack [1], [4], with its related doping profile, $N_d x^{\left(\frac{1}{n}-2\right)}$, the proper area ratio for IM_3 cancellation is

$$X = \frac{4n+1+\sqrt{12n^2-3}}{2(n+1)} \quad . \tag{4.1}$$

When the capacitance power law coefficient n = 0.5, the resulting X will be unity and therefore the two anti-series branches will be identical, which means that, in practice, the high tuning range varactor stack can be reduced to the distortion-free varactor stack configuration [1] [Fig. 4.1(c) simplified to Fig. 4.1(b)]. On the other hand, when $n = \infty$, the corresponding doping profile and area ratio for IM_3 cancellation will be $N_d x^{-2}$ and $X = 2+\sqrt{3}$, which is identical to the configuration of wide tone-spacing varactor stack [6] (see Table VIb). From this perspective, both the distortion-free varactor stack and wide tone-spacing varactor stack can be regarded as special cases of the high tuning range varactor stack, which implies that these two topologies preserve all the merits of the high tuning range varactor stack. Closer inspection however, shows that the distortion-free varactor stack has the unique property that it is basically free of all distortion in the high tone-spacing regime. In comparison, the high tuning range varactor stack and the wide tone-spacing varactor stack are limited by IM_5 products for their linearity.

When considering the integration compatibility aspects, it proves that the wide tone-spacing varactor stack can be easily integrated with the narrow tone-spacing varactor stack. This facilitates to address the different linearity requirement of transmit and receive chains in one single technology [6]. In view of this, note that, according to Table VIa and VIb, only the narrow tone-spacing varactor stack [5] provides high-

linearity performance in the low-tone spacing regime, which is one of the most essential linearity requirements for adaptive transmitters. Moreover, the fact that use can be made of a base-band "short" at the center-tap connection for the narrow tone-spacing varactor stack facilitates rapid modulation of the tunable capacitance, something that is beneficial for future RF applications like dynamic load-line power amplifiers or modulators. When considering the tuning range, the uniform doping of distortion-free varactor stack has a relatively fixed relationship between the tuning range and control voltage, which is not present for the other configurations due to the free-to-choose grading coefficient (a_2 or n). This flexibility in grading facilitates the adjustment of tuning range and control voltage range for a given application.

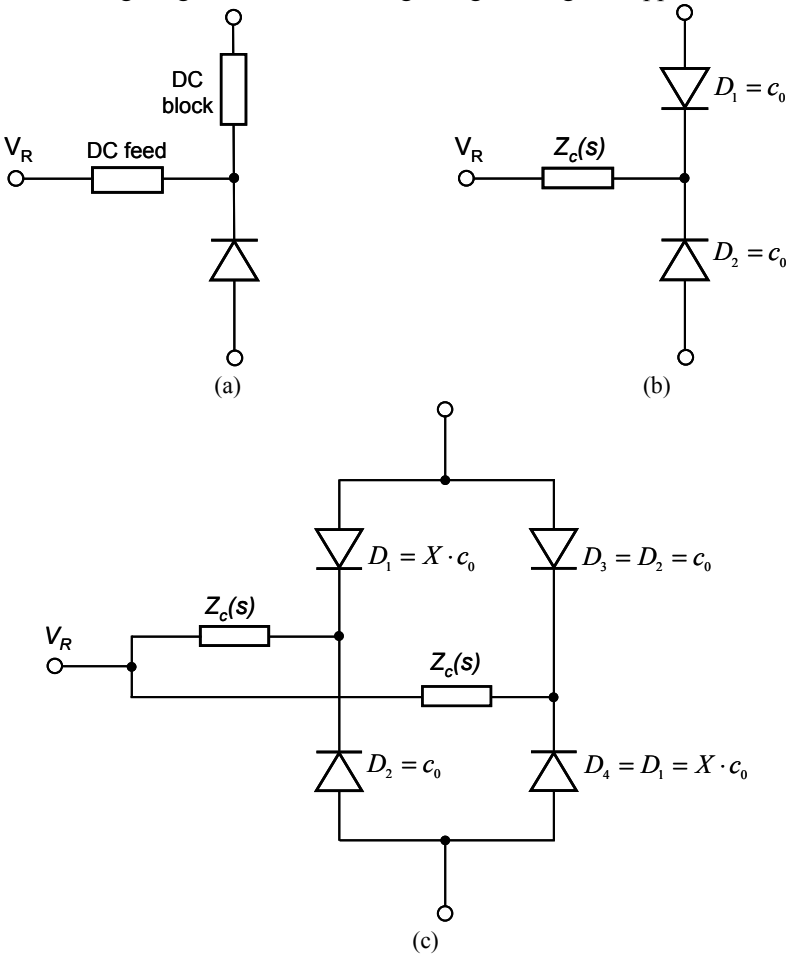


Fig. 4.1. (a) Single diode configuration. (b) Anti-series configuration for distortion-free varactor stack and narrow tone-spacing varactor stack. (c) Anti-series/anti-parallel configuration for high tuning range varactor stack and wide tone-spacing varactor stack.

4.2 Varactor as Linear Modulator

When considering varactors in an anti-series diode configuration as a three-terminal capacitive mixing device, where the applied RF signal is modulated by the baseband center-tap voltage, the effective capacitance between the RF terminals *a* and *b* is modulated by the baseband voltage of node *c* (Fig. 4.2). In order to create a useful linear mixing function, two basic conditions should be fulfilled, namely:

1) the capacitive current flowing through the effective capacitance of the varactor stack should be linearly related to the applied RF voltage. In most practical (telecommunication) applications, this requires a zero value for the third-order distortion with respect to the applied RF signal. Consequently, no third-order intermodulation distortion products should arise in the resulting current.

2) the effective capacitance must be modulated such that the transfer function is linear. As a consequence, the input should be pre-distorted for the non-linear $C(V_c)$ relation of the total capacitance with respect to the center tap voltage, as well as for how a capacitance change relates to the transfer function of the total circuit.

When utilizing the varactor stack configuration with high center-tap impedance at all frequencies, i.e., distortion-free varactor stack, high tuning range varactor stack and wide tone-spacing varactor stack, for capacitance modulation, we face the following conflict: the high impedance requirement for the center-tap connection requires the baseband center-tap voltage to "float" [$Z_c(s) = \infty$]. Imposing a control voltage to modulate the effective capacitance value will violate this high impedance condition and directly yield intermodulation distortion of the applied signal at the RF terminals. This phenomenon can also be observed from the following simulation experiment.

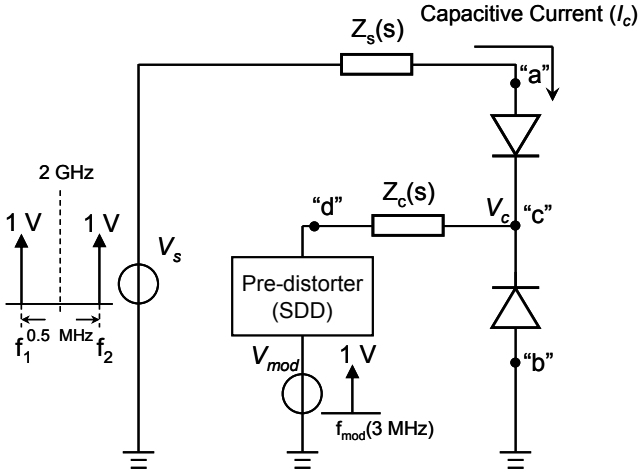
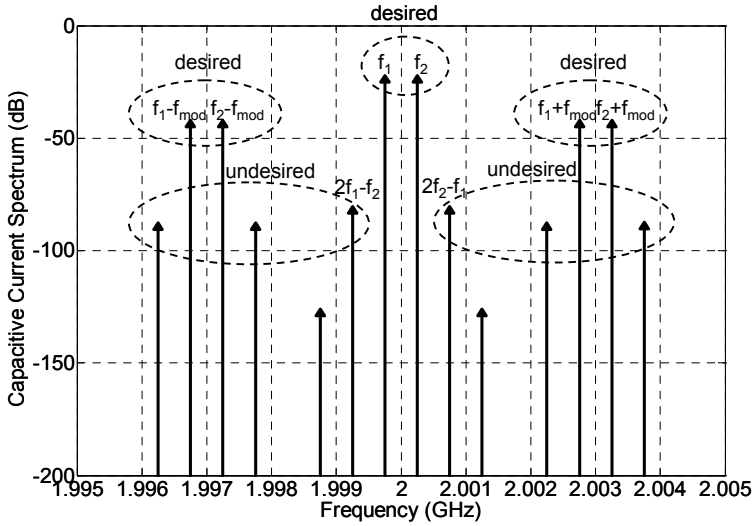
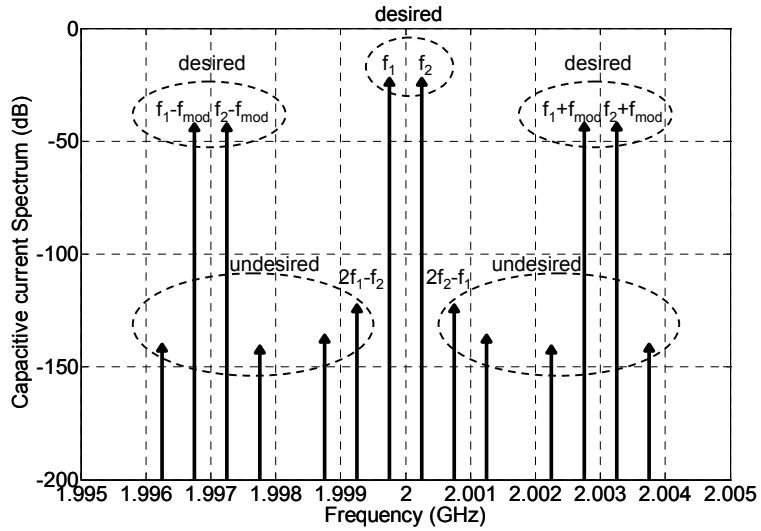


Fig. 4.2. Illustration of linear modulation using capacitive mixing with the narrow tone-spacing varactor stack and distortion-free varactor stack.



(a) distortion-free varactor stack



(b) narrow tone-spacing varactor stack

Fig. 4.3. Simulated spectrum of the capacitive current of the distortion-free varactor stack (a) and narrow tone-spacing varactor stack (b) when performing a 3 MHz capacitance modulation on a 0.5 MHz spacing two-tone signal using Fig. 4.2. Note that the distortion of the modulated signal is -50 dBc in the distortion-free varactor stack case and -100 dBc in the narrow tone-spacing varactor stack case (c_{ab} = 5 pF for both cases).

Consider the simple setup of Fig. 4.2 where a two-tone RF voltage source is connected to a capacitance modulated varactor stack. The center node of the varactor stack is modulated by an independent voltage source (V_{mod}). Depending on the $C(V_R)$ relation, we pre-distort this modulating voltage such that a linear variation of the capacitance is achieved. For simplicity, we only consider the anti-series configurations, i.e., distortion-free varactor stack and narrow tone-spacing varactor stack. In Agilent's ADS we have implemented this pre-distortion function using a Symbolic Defined Device (SDD). Note that in this simple example the pre-distorting function is basically the inverse C-V_R relation of the varactor technology used. Consequently, when using the distortion-free varactor stack (uniform doping), the required pre-distortion function can be written as

$$V_c = \frac{C_{j0}^2 V_j}{V_{\mathrm{mod}}^2} - V_j \tag{4.2}$$

with C_{j0} being the capacitance at zero bias, V_j the build-in voltage and V_{mod} the modulation voltage (see Fig. 4.2); while in the case of the narrow-tone spacing varactor stack, the pre-distortion function is

$$V_c = \frac{\ln(V_{\mathrm{mod}})}{a_2}\,. \tag{4.3}$$

As result of this pre-distortion, we obtain a linear variation of capacitance with the modulating baseband signal. Due to this linear variation, the resulting mixing current flowing through the varactor stack should be perfectly linear, provided that the varactor stack itself does not generate any intermodulation distortion due to the applied RF voltage. In our modulation experiments, we apply the pre-distorted voltage to the center-tap node through a high-value inductor, which behaves as short-circuit for the baseband frequencies and as an open-circuit for fundamental and higher harmonics.

The resulting simulated spectrum of the capacitive current flowing through the distortion-free varactor stack is given in Fig. 4.3(a). IM_3 distortion is observed around the carrier and modulation sideband frequencies. One can argue that this result is expected, since the baseband loading condition for the center tap was violated. Increasing this baseband impedance to the desired level will lower the IM_3 distortion for two-tone signals with relatively large tone spacing; however at the same time it will effectively eliminate the intended capacitance modulation. In theory, one can circumvent this problem by performing the capacitance modulation by charge injection using a very high impedance charge pump. However, this will create many implementation difficulties and drift problems.

In contrast to the distortion-free varactor stack, the proposed narrow-tone spacing varactor stack requires a baseband short-circuit to guarantee its low distortion operation. Consequently, we have to provide a low impedance path at baseband frequencies

between the center tap and the RF terminals and high impedances for the fundamental and higher harmonics. The resulting simulated spectrum of the capacitive current is given in Fig. 4.3(b). The simulated distortion of the capacitive current is significantly improved compared to the results for the distortion-free varactor stack. It should be noted that the minimum intermodulation levels achieved in this experiment now depend on how well one can meet the center-tap impedance conditions.

4.3 Multi-stacked Varactors for Improved Power Handling and Linearity

As mentioned in the foregoing chapter, the third-order intermodulation (IM_3) can be cancelled through proper harmonic loading of the terminals. In this section, multi-stack topology is used to further improve the linearity and power handling capability for different types of varactor stack and the effectiveness will be compared.

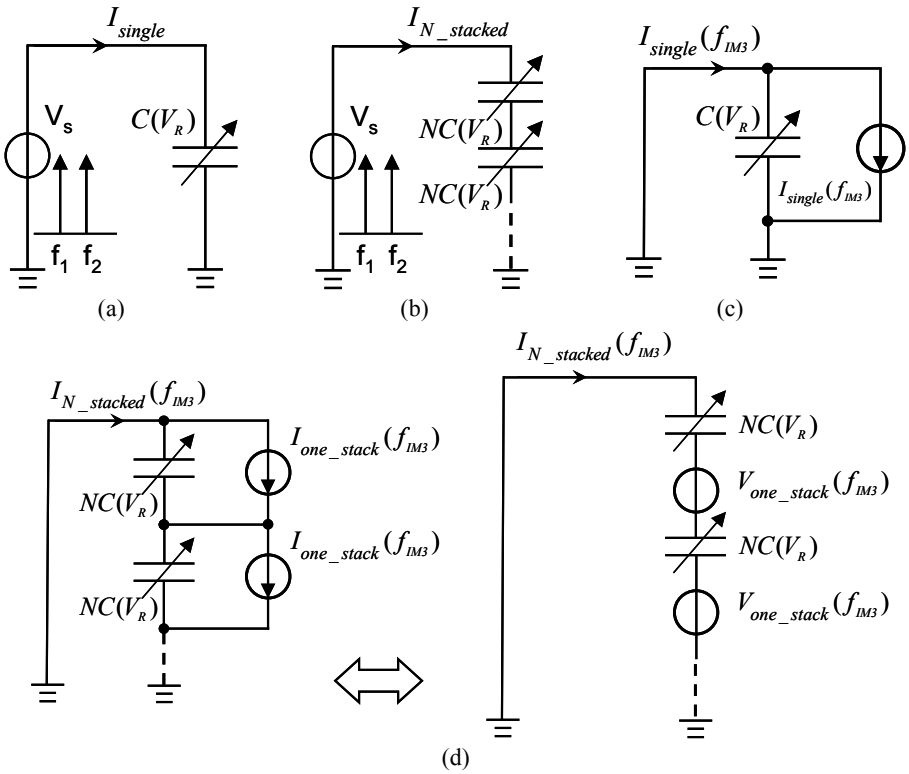


Fig. 4.4. (a) Schematic for a single-varactor stack; (b) schematic for the *N*-varactor stacks; (c) schematic to calculate third-order or fifth-order response for the single varactor stack; (d) schematic to calculate third-order or fifth-order response for the *N*-varactor stacks.

When connecting N varactor stacks in series, the applied RF voltage will be divided over the N stacks. Since the (remaining) nonlinearities of these varactor stacks are excited with a voltage that is N times lower, their resulting nonlinear currents will be reduced. One of the key advantages of the IM_5 dominated varactor stacks, over (typically) IM_3 dominated counterparts is, besides their already much higher initial linearity, the further increased linearity improvement when using these multiple stacks. To support understanding at this point, we consider the external terminal current of the (stacked) varactor in Fig. 4.4.

We use I_{single} to represent a single varactor stack and $I_{N\_stacked}$ for N varactor stacks in series [Fig. 4.4 (a) and (b)]. When keeping the total capacitance the same, the capacitance of multiple stacked varactors must be N times larger than the original single varactor stack. Logically, the *fundamental* currents will be identical when applying the same RF voltage i.e.,

$$I_{single}(f_{fund}) = I_{N\_stacked}(f_{fund}). \tag{4.4}$$

The equivalent circuits for the single stack and $N\times$ varactor stacks to calculate the nonlinear third-order intermodulation (IM_3) components are shown in Fig. 4.4(c) and (d) respectively. To calculate the IM_3 current for the $N\times$varactor stack, the individual nonlinear current sources can be converted to their Thevenin representation as illustrated in Fig. 4.4(d). The related IM_3 voltage across one of the $N\times$ varactor stacks is

$$V_{one\_stack}(f_{IM3}) = \frac{I_{one\_stack}(f_{IM3})}{j\omega NC(V_R)}. \tag{4.5}$$

So the equivalent non-linear current for the total stack can be found by a Norton transformation:

$$I_{N\_stacked\_IM3}(f_{IM3}) = \frac{N \cdot V_{one\_stack}(f_{IM3})}{\frac{1}{j\omega C(V_R)}} = I_{one\_stack}(f_{IM3}). \tag{4.6}$$

Therefore, the resulting IM_3 current for the N-stack configuration is equal to the IM_3 current of one varactor stack in this multi-stack configuration. Consequently, for an IM_3 dominated $N\times$varactor stack, the IM_3 current is proportional to: $(V_{RF}/N)^3$, since stacking reduces this RF voltage by a factor of N, the resulting third-order nonlinear current sources are

$$I_{N\_stacked\_IM3}(f_{IM3}) = I_{one\_stack\_IM3}(f_{IM3}) = N \cdot I_{single\_IM3}(f_{IM3})\left(\frac{1}{N}\right)^3. \tag{4.7}$$

where the first "N" is a result of the larger area compared to a single varactor stack and the "$(1/N)^3$" is a result of the RF voltage splitting. Consequently, multiple-stacking results in a reduction of the distortion current by a factor of N^2, i.e., 40log(N) dB.

By contrast, for an IM_5 dominated device, like the narrow-tone spacing varactor stack used here, the nonlinear IM_5 currents that appear at IM_3 frequencies ($2f_1$-f_2 and $2f_2$-f_1) are proportional to the 5th power of the RF voltage over the elements in the stack, consequently,

$$I_{N\_stacked\_IM5}(f_{IM3}) = I_{one\_stack\_IM5}(f_{IM3}) = N \cdot I_{single\_IM5}(f_{IM3})\left(\frac{1}{N}\right)^5. \quad (4.8)$$

So for a IM_5 dominated device using N-stacks results in a reduction of the non-linear current by a factor of N^4, i.e., 80log(N) dB, which is twice the linearity improvement found for an IM_3 dominated device.

From the above it can be concluded that it is very important to maintain the IM_3 cancellation in a multi-stack topology, especially for those IM_5 dominated devices like the narrow tone-spacing varactor, wide tone-spacing varactor stack and high tuning range varactor stack. One can achieve this by providing the proper harmonic terminations at nodes a, b and d as shown in Fig. 4.5. This is verified in Fig. 4.6 (a) and (b), using ADS's Harmonic Balance simulator, by plotting the capacitive current of the external terminals of the narrow tone-spacing varactor stack at f_1 and $2f_1$-f_2 with correct and incorrect harmonic terminations respectively. Note that for an objective comparison, the number of stacked diodes is kept the same for both cases. It can be observed that the IM_5 dominated nonlinear current is much smaller to start with, while the linearity improvement found for increasing N, is double of that in the IM_3 dominated cases.

In order to compare the linearity improvement by using the multi-stack topology for different types of varactor stack, the double-stack topology is used for testing.

First, the tuning range and maximum operation voltage of the varactor stacks should be normalized. Here we use for comparison a varactor stack with an effective zero bias capacitance of 10 pF, a breakdown voltage (V_{R_max}) of 8 V and a tuning range (T_{tune}) of 3. Consequently, the corresponding exponential coefficient (a_2) for our narrow tone-spacing varactor stack and wide tone-spacing varactor stack should be equal to 0.137 V^{-1} [see (3.5) in the preceding chapter]. Here, the wide tone-spacing varactor stack is used as the representative of the high tuning range varactor stack. Fig. 4.7 shows the simulated two-tone linearity comparison for different types of varactor stack with single and double stack, as measured by the dBc ratio of the fundamental and distortion current (at $2f_1$-f_2) as a function of the tone spacing of the RF input signal (Δf). It can be observed that a linearity improvement of 24 dB is achieved at the IM_3 cancelled / IM_5 dominated region for the narrow tone-spacing varactor stack and wide

tone-spacing varactor stack; while at the IM_3 dominated region, i.e., low tone-spacing region (below 10 kHz in Fig. 4.7) for the wide tone-spacing varactor stack and distortion-free varactor stack, only 12 dB linearity improvement is obtained. Note that the distortion-free varactor stack is principally free of distortion at the high tone-spacing region and therefore there is no need to improve its already superior linearity at the distortion-cancelled region. However, stacking technology does help to improve its linearity at low tone-spacing region. This effect will be the similar for other IM_3 dominated varactor devices, such as BST varactors, and for this reason, it can be concluded that the multi-stack topology works most efficiently for the IM_5 dominated varactor stacks, i.e., narrow tone-spacing varactor stack, wide tone-spacing varactor stack and high tuning range varactor stack.

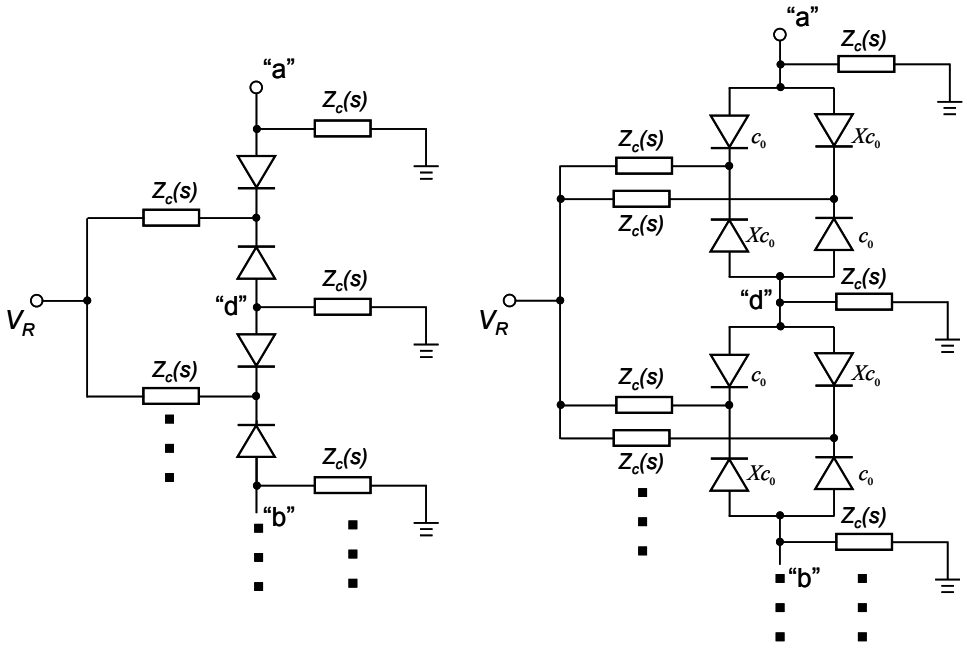


Fig. 4.5. (a) Multi-stack topology for anti-series configurations, i.e., narrow tone-spacing varactor stack and distortion-free varactor stack; (b) Multi-stack topology for anti-series/anti-parallel configurations, i.e., high tuning range varactor stack and wide tone-spacing varactor stack.

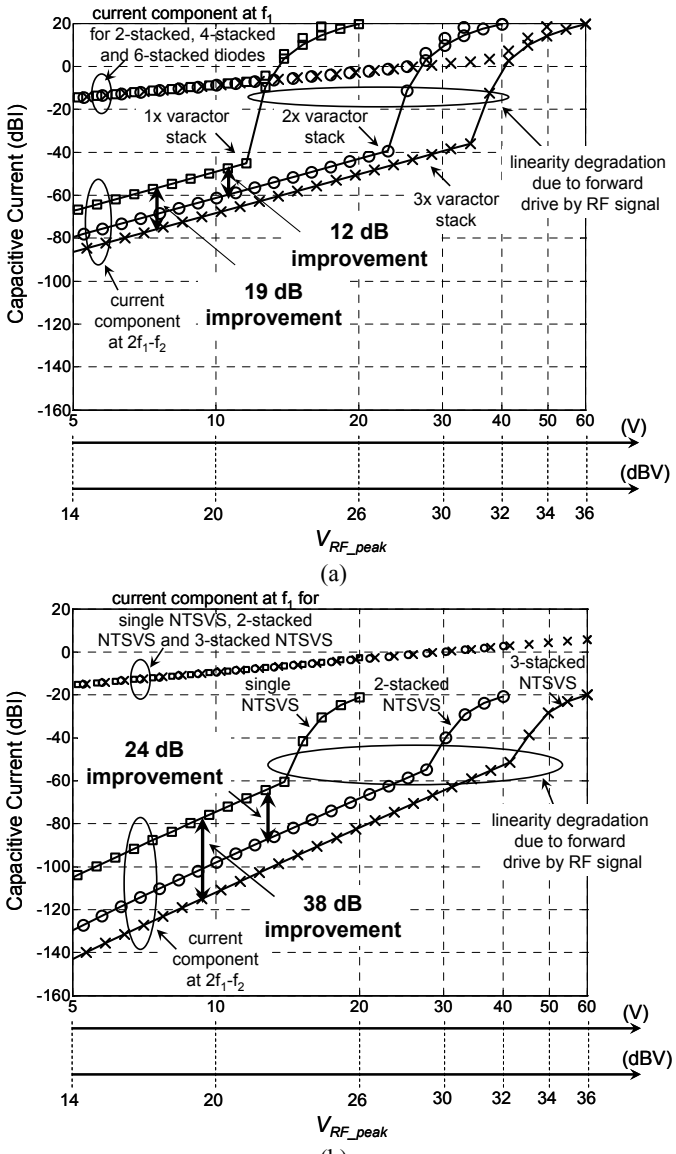


Fig. 4.6. Simulated capacitive linear and nonlinear terminal current versus peak voltage of a two-tone RF signal: (a) $\underline{IM_3}$ dominated case for N-varactor stacks using varactors with an exponential $C(V_R)$ relation but with incorrect harmonic terminations; (b) $\underline{IM_5}$ dominated case for the same varactors in a N-stacked narrow tone-spacing varactor stack configuration. The diode parameters are: a_1 = 20 pF for a single varactor stack and narrow tone-spacing varactor stack, 40 pF for a double varactor stack and double narrow tone-spacing varactor stack configuration, 60 pF for a triple varactor stack and triple narrow tone-spacing varactor stack configuration, for all diodes a_2 = 0.11 V^{-1} while the applied reverse bias (V_R) is 5 V in all situations.

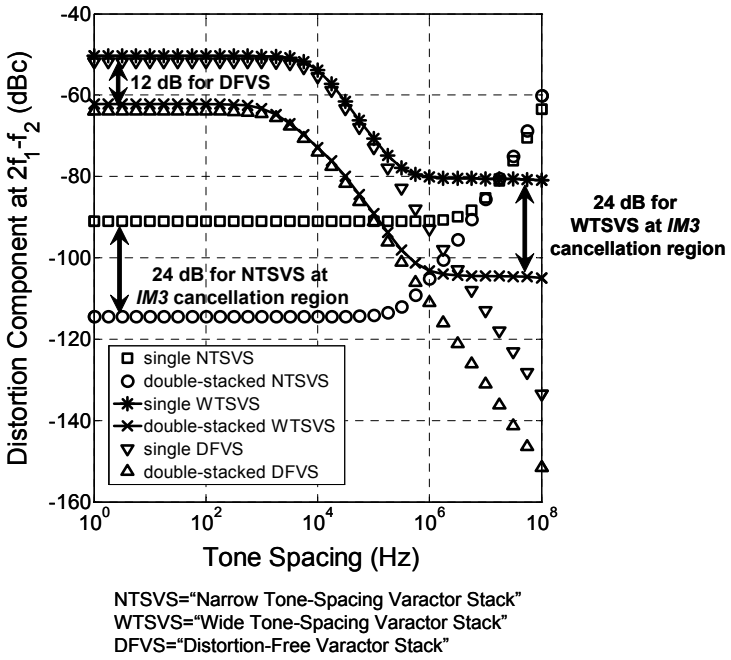


Fig. 4.7. Simulated capacitive current distortion component at $2f_1$-f_2 versus the tone spacing of the input RF voltage signal (a_1 = 0.137 V^{-1} , V_R = 4 V, V_{RF_peak} = 4 V, f_{RF_center} = 2 GHz, $C_{zero\ bias}$ = 10 pF) for single narrow tone-spacing varactor stack, double-stacked narrow tone-spacing varactor stack, single wide tone-spacing varactor stack, double-stacked wide tone-spacing varactor stack, single distortion-free varactor stack and double-stacked distortion-free varactor stack circuits.

4.4 System-level Linearity Comparison

Up till now, the linearity of the varactors is evaluated at the circuit level by monitoring the intermodulation product of a two-tone signal (i.e., IM_3 or IM_5) while varying its tone spacing. When considering the performance of a communication system with a given channel bandwidth, intermodulation distortion will give rise to in-band and out-of-band interference. Out-of-band interference will disturb the information detection of the adjacent-channel user, while the in-band intermodulation products that fall within the assigned transmit bandwidth will pollute the transmitted information by changing its original constellation points, causing difficulties in signal detection. To study these effects, industry use the adjacent channel power ratio (*ACPR*) to evaluate the out-of-band interferes, and the error vector magnitude (*EVM*) as a figure

of merit describing how the transmitted information becomes distorted.

In this section, we investigate the system-level response of the proposed varactor configurations under different bandwidth or data-rate conditions, making use of a varactor-based phase shifter as shown in Fig. 4.8. This true-time-delay type 180° phase shifter is composed of eight cascaded $\prod$ low-pass sections, of which the lossless series inductances (L_{series}) are fixed as 0.36 nH while the shunt capacitances (C_{shunt}) can be tuned from 7.35 pF to 13.60 pF. The simulated s_{11} and s_{21} are given in Fig. 4.9, showing a good matching at the input while providing a phase variation of 180°.

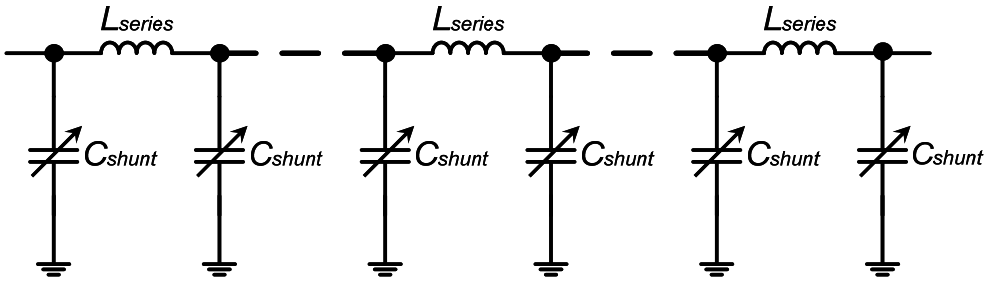
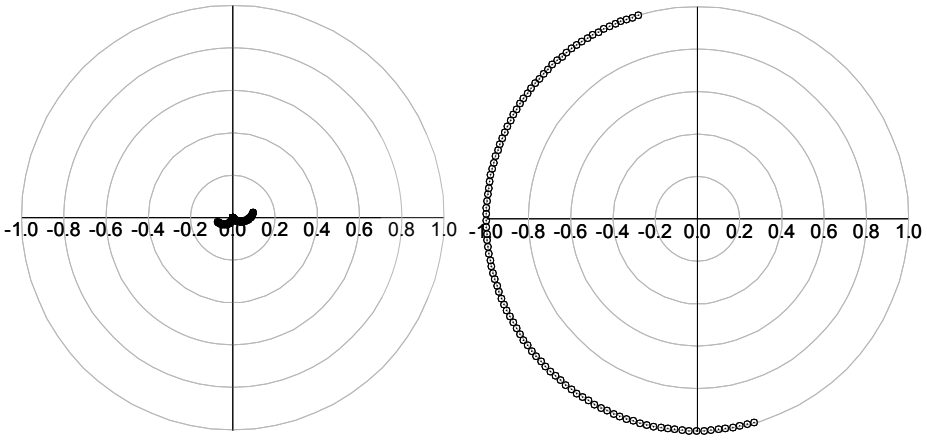


Fig. 4.8. Schematic of the true-time-delay phase shifter to be used for system-level linearity comparison for different varactor configurations. [To achieve a phase shift of 180°, eight $\prod$ low-pass sections are cascaded. The lossless series inductances (L_{series}) are fixed as 0.36 nH, while the shunt capacitances (C_{shunt}) are tuned from 7.35 pF to 13.60 pF. The characteristic impedance is 5 Ω.]



(a) (b)

Fig. 4.9. (a) The simulated s_{11} of the designed phase shifter with polar plot. (b) Polar plot of the simulated s_{21}. [The lossless series inductances (L_{series}) in Fig. 4.8 are fixed as 0.36 nH, while the shunt capacitances (C_{shunt}) are tuned from 7.35 pF to 13.60 pF. The characteristic impedance is 5 Ω and the RF frequency is 2 GHz.].

In practice, the tunable shunt capacitors (C_{shunt}) can be implemented by different varactor configurations to be compared, i.e., (i) single varactor stack with an exponential C-V_R relation but with incorrect harmonic terminations, (ii) narrow tone-spacing varactor stack with 5 nH center-tap inductance, (iii) distortion-free varactor stack with 100 kΩ center-tap resistance, (iv) distortion-free varactor stack with 1 MΩ center-tap resistance. In order to handle a power level of 2 W for the whole phase variation range while avoiding very high voltage swings over the varactor diodes, the characteristic impedance of the phase shifter is set as 5 Ω. Consequently, for the implementation using distortion-free varactor stack, the control voltage needs to be tuned from 4 V to 12 V to obtain an effective tuning range of 1.85 and a power level of 2 W. Accordingly, the grading coefficient (a_2) of those varactor diodes with an exponential C-V_R relation is normalized as 0.0528 V^{-1} to maintain the same effective tuning range over the same voltage range.

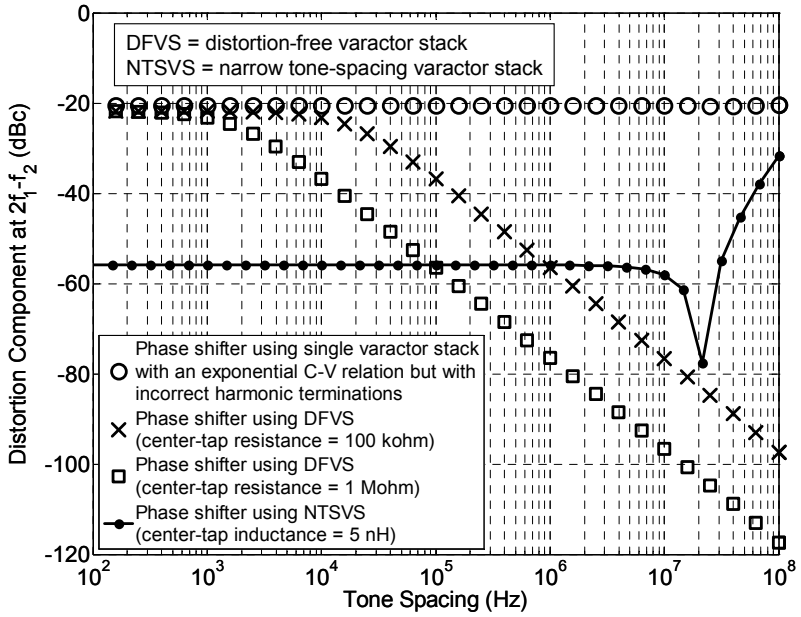


Fig. 4.10. Simulated distortion components for the 180° phase shifter at $2f_1$-f_2 in dBc with respect to the fundamental power (40 dBm each tone) as a function of the tone spacing of the RF input signal. The tunable capacitances (C_{shunt}) are implemented using different varactor configurations, i.e., (i) single varactor stack with an exponential C-V_R relation but with incorrect harmonic terminations, (ii) narrow tone-spacing varactor stack with 5 nH center-tap inductance, (iii) distortion-free varactor stack with 100 kΩ center-tap resistance, (iv) distortion-free varactor stack with 1 MΩ center-tap resistance. The diode parameters are: a_1 = 33.90 pF and a_2 = 0.0528 V^{-1} for the single varactor stack; a_1 = 34.45 pF and a_2 = 0.0528 V^{-1} for the narrow tone-spacing varactor stack; C_{j0} = 78.2 pF and V_j = 0.7 V for the distortion-free varactor stack. The RF frequency is 2 GHz, while the applied reverse bias (V_R) is 10 V in all situations.

To study the linearity of the phase shifter, of which the tunable capacitances (C_{shunt}) are implemented using the different varactor configurations, the circuit is first simulated using a two-tone signal (40 dBm each tone) while varying the tone spacing (Fig. 4.10). It can be observed that the phase shifter making use of distortion-free varactor stack starts to offer better linearity than the single varactor stack (with incorrect harmonic terminations) above 1 kHz for the center-tap resistance of 1 MΩ and above 10 kHz for the center-tap resistance of 100 kΩ, while the phase shifter implemented with the narrow tone-spacing varactor stack provides superior linearity up to 30 MHz.

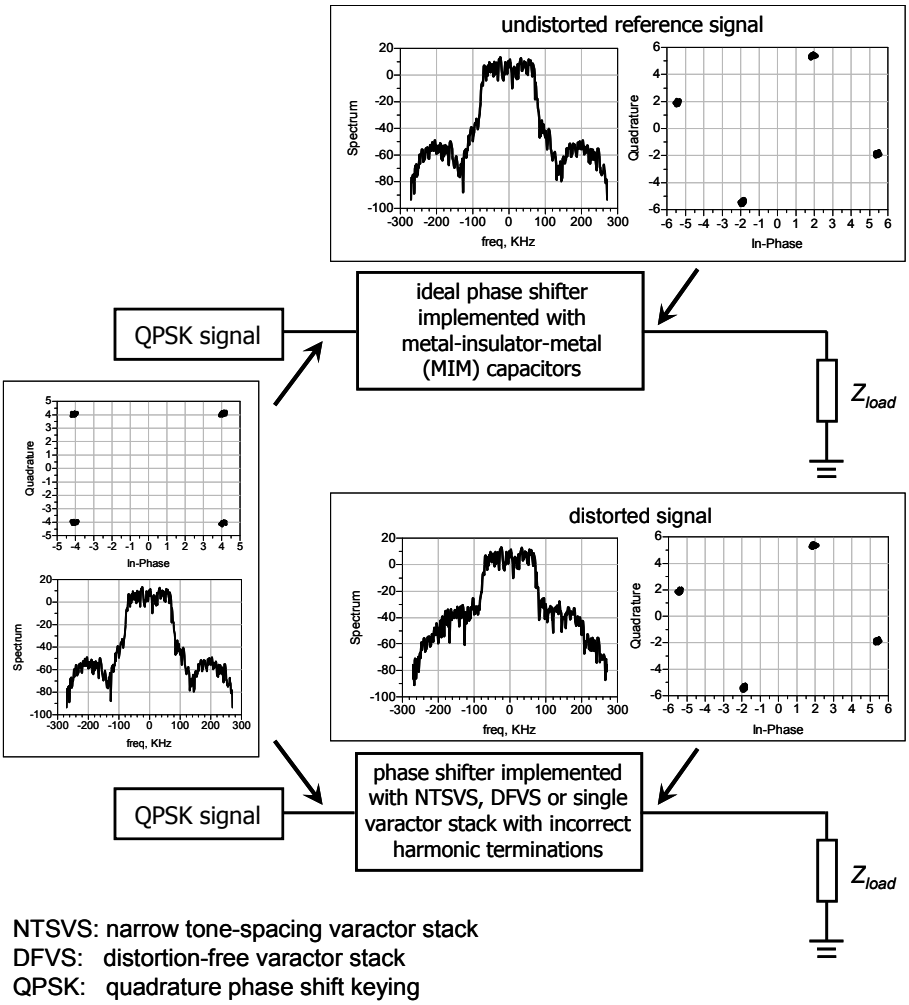


Fig. 4.11. Schematic for system-level linearity comparison of the phase shifter.

Table VII. Parameters used in Fig. 4.11 for the system-level linearity comparison

	bandwidth	symbol rate of the QPSK signal	integration region for *ACPR* calculation (offset frequency is used here)	
			lower sideband	upper sideband
high data-rate application	5 MHz	3.6864 MHz	-6.8432 MHz ~ -1.8432 MHz	1.8432 MHz ~ 6.8432 MHz
moderate data-rate application	200 kHz	135.5 kHz	-300 kHz ~ -100 kHz	100 kHz ~ 300 kHz

For the system-level linearity comparison, we consider the schematic as shown in Fig. 4.11. A relatively pure quadrature phase-shift keying (QPSK) signal with a mean power of 35 dBm and the peak-to-average ratio of 4.35 dB is used as the signal source (see the input signal in Fig. 4.11), of which the bandwidth and data rate can be adjusted for different applications. Here, as listed in Table VII, we study two cases: the moderate data-rate application with the symbol rate of 135.5 kHz and the high data-rate application with symbol rate of 3.6864 MHz. Since *EVM* is a figure of merit describing how the constellation points are shifted from their original places during transmission, it is important to note that the "ideal" phase shifter structure itself, as well as the nonlinearities of the varactors used in such a phase shifter, can change the positions of the constellation points of the transmit signal. Fortunately, a true-time delay phase shifter only rotates constellation points without distorting the signal. In Fig. 4.11, a reference phase shifter path, of which the shunt capacitance (C_{shunt} in Fig. 4.8) is implemented with perfectly linear metal-insulator-metal (MIM) capacitors, is used to normalize the rotation of the constellation points. By doing so, when comparing the degradation of the *EVM* of the phase shifters, this degradation can be totally assigned by the distortion contributions of the varactors. In the meanwhile, the *ACPR* of the distorted signal and the undistorted reference signal can be tested and compared.

The simulated *EVM* and *ACPR* for the moderate and high data-rate applications are listed in Table VIIIa and VIIIb respectively. It can be observed that the *EVM* and *ACPR* of the single varactor stack with incorrect harmonic terminations are worst for both application cases, which reflects the fact that a nonlinearity as strong as -20 dBc remains for the whole range of the tone spacings up to 100 MHz as shown in Fig. 4.10. On the other hand, the simulated *EVM* and *ACPR* of the narrow tone-spacing varactor

stack are extremely small for both application cases, which means the narrow tone-spacing varactor stack raises neither in-band distortion nor out-of-band interference, and these results agree very well with the two-tone simulation results in Fig. 4.10. Note that the narrow tone-spacing varactor stack provides a superior linearity up to 30 MHz. For the distortion-free varactor stack, as shown in Fig. 4.10, it starts to offer better linearity above 1 kHz for the center-tap resistance of 1 MΩ and above 10 kHz for the center-tap resistance of 100 kΩ. Since the bandwidths under consideration are both at least 10 times larger than the tone spacing where the distortion-free varactor stack behaves nonlinear, the linearity performance evaluated by *ACPR* survives for both application cases. However, the *EVM* results reveal that the distortion-free varactor stack topology raises in-band distortion for the moderate data-rate application and this can be explained by its linearity limitations at low tone spacing as earlier indicated in Fig. 4.10. In summary, it can be concluded that the narrow tone-spacing varactor stack is suitable for both moderate and high data-rate applications, while the distortion-free varactor stack may raise some in-band distortion when the bandwidth under consideration is relatively small.

Table VIIIa. Simulated *ACPR* and *EVM* using the schematic of Fig. 4.11 and the parameters of Table VII for the high data-rate application (symbol rate=3.6864 MHz)

	ACPR (dBc)		*EVM* relative to the undistorted reference (%)
	lower sideband	upper sideband	
undistorted reference (MIM capacitor)	-63.44	-63.54	0
narrow tone-spacing varactor stack with 5 nH center-tap inductance	-63.42	-63.50	0.008
single varactor stack with incorrect harmonic terminations (exponential C-V_R)	-46.18	-45.08	0.256
distortion-free varactor stack with100 kΩ center-tap resistance	-63.43	-63.52	0.054
distortion-free varactor stack with 1 MΩ center-tap resistance	-63.44	-63.54	0.013

Table VIIIb. Simulated *ACPR* and *EVM* using the schematic of Fig. 4.11 and the parameters of Table VII for the moderate data-rate application (symbol rate=135.5 kHz)

	ACPR (dBc)		*EVM* relative to the undistorted reference (%)
	lower sideband	upper sideband	
undistorted reference (MIM capacitor)	-58.46	-58.90	0
narrow tone-spacing varactor stack with 5 nH center-tap inductance	-58.36	-58.93	0.002
single varactor stack with incorrect harmonic terminations (exponential C-V_R)	-43.84	-43.99	0.253
distortion-free varactor stack with100 kΩ center-tap resistance	-58.03	-56.25	0.439
distortion-free varactor stack with 1 MΩ center-tap resistance	-58.67	-59.01	0.113

The diode parameters are: a_1 = 33.90 pF and a_2 = 0.0528 V^{-1} for the single varactor stack; a_1 = 34.45 pF and a_2 = 0.0528 V^{-1} for the narrow tone-spacing varactor stack; C_{j0} = 78.2 pF and V_j = 0.7 V for the distortion-free varactor stack. The RF frequency is 2 GHz, while the applied reverse bias (V_R) is 10 V in all situations.

4.5 Conclusions

In this chapter, all types of varactor stacks, aiming for the IM_3 cancellation, are compared. When considering power handling capability and linearity, the anti-series topologies, i.e., distortion-free varactor stack and narrow tone-spacing varactor stack, provide better performance than the anti-series/anti-parallel topologies due to the equal splitting of RF signal. The unique feature of narrow tone-spacing varactor stack, compared to other infinite impedance center-tapped varactor stacks and MEMS varactors, is its high modulation frequency for operation and high linearity for signals

with low tone spacing, making it suitable for the many dynamic modulation applications. The wide tone-spacing varactor stack, which can be implemented in the same process as the narrow tone-spacing varactor stack, offers complementary linearity behavior in terms of tone spacing and it can be regarded as a bonus, provided that the use of the narrow tone-spacing varactor stack is compulsory. In addition, their exponential $C(V_R)$ relationship generally yields larger tuning range compared to the uniformly doped varactors, i.e., distortion-free varactor stack. Based on these facts, the combination of narrow tone-spacing varactor stack and wide tone-spacing varctor stack will be the best solutions for adaptive RF systems. The multi-stack topology is used to further improve the IM_5 dominated linearity and power handling capability. From the comparison, it is concluded that the multi-stack topology works most efficiently for the IM_5 dominated varactor stacks and the resulting linearity improvement is generally double of that found in IM_3 dominated devices. The system-level responses of the different varactor configurations are investigated under different bandwidth or data-rate conditions. It reveals that the narrow tone-spacing varactor stack is suitable for both moderate and high data-rate applications, while varactor configurations with linearity limitations at low tone spacings, like the distortion-free varactor stack, may raise some in-band distortion when the bandwidth under consideration is relatively small.

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Chapter 5

Technology Implementations and Experimental Results

In the previous chapters, the theory of the low-loss, high-linearity varactor stack has been extensively analyzed. In this chapter, we first focus on the implementation issues in Section 5.1. The silicon-on-glass (SOG) varactor process, which was first demonstrated by K. Buisman in cooperation with Prof. L. K. Nanver and many other DIMES colleagues, and a new Skywork's GaAs technology for ultra-low distortion varactors have been developed and utilized for the implementation of the newly proposed varactor topologies in Chapter 3 (i.e., narrow tone-spacing varactor stack and wide tone-spacing varactor stack).

For our experiments, trial runs were defined to achieve the exponential $C(V_R)$ relation using the proposed varactor profile in Chapter 3. Based on the various applications, three types of varactor diodes have been selected for implementation, namely:

- SOG low-voltage varactor devices (V_{R_max} = 5 V, T_{tune} = 6) to serve applications that do not allow or require the use of high control voltages, like tunable filters [1], [2] and phase shifter [3], [4];
- SOG high-voltage varactor devices (V_{R_max} = 20 V, T_{tune} = 6) for high-power applications, like dynamic load-line power amplifiers;
- GaAs large-tuning-range varactor devices (V_{R_max} = 12 V, T_{tune} = 9) for applications that need extremely high tuning ability, like antenna mismatch correction networks.

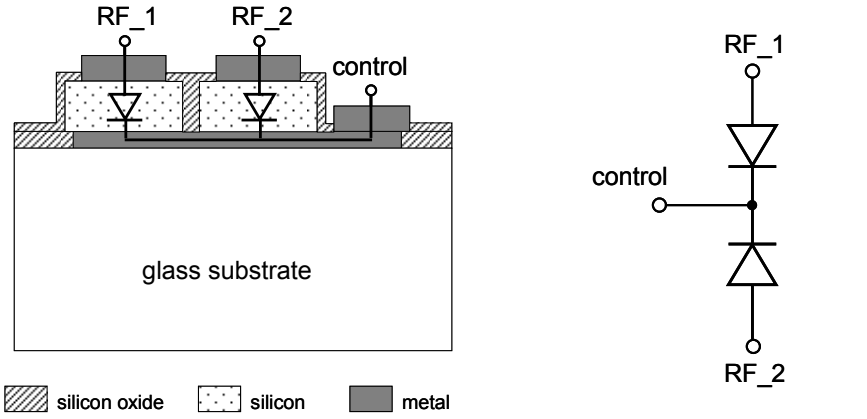
In Sections 5.2-5.4, the measurement results of these structures are given, which provide the experimental evidence for the predicted IM_3 cancellation, as well as, for the complementarty linearity behavior of narrow tone-spacing varactor stack and wide

tone-spacing varactor stack. The multi-stack topology is used to further reduce the IM_5 dominated nonlinearity of the narrow tone-spacing varactor stack, yielding a record high linearity for continuously tunable capacitances. Finally, we conclude this chapter in Section 5.5.

5.1 Technology Implementations

5.1.1 Silicon-on-Glass Technology

The most straightforward implementation of the varactor stack is in the dedicated silicon-on-glass technology [5], [6] as shown in Fig. 5.1 developed at the Delft University of Technology. This wafer-transfer technology eliminates substrate losses and facilitates patterning of both frontside and backside of the wafer. Using this feature, the intrinsic varactor can be directly contacted by thick metal interconnects on both sides as shown in Fig. 5.1. This eliminates the use of finger structures typically used in conventional varactor implementations to lower the influence of the buried layer series resistance. The remaining losses of the metal interconnects can be significantly reduced through the use of plated copper, facilitating very high quality factors.



(a) Cross section (b) Equivalent schematic

Fig. 5.1. Cross section (a) and equivalent schematic (b) of a varactor stack implemented in silicon-on-glass technology with metal interconnects on both sides.

A simplified varactor process flow [5] is shown schematically in Fig. 5.2. The starting material is a 4" silicon-on-insulator (SOI) wafer on which the specific varactor profile has been grown epitaxially. The total epi thickness depends on the required doping profile as defined in Chapter 3. The wafer is covered with 1 µm plasma-

enhanced chemical vapor deposition (PECVD) oxide to enable the gluing of the wafer to a glass wafer. Substrate transfer techniques [7] are then used to replace the bulk silicon substrate with glass. To preserve integrity of the adhesive, all subsequent thermal processing temperatures must not exceed 300 °C . On the back-side of the wafer, the diode contacts were implanted with 5 keV As^+ and excimer laser annealed, resulting in very low-ohmic contacts to the Al/Si metallization. Electroplating of 4 µm copper on the Al/Si surface was performed to reduce the metal resistance.

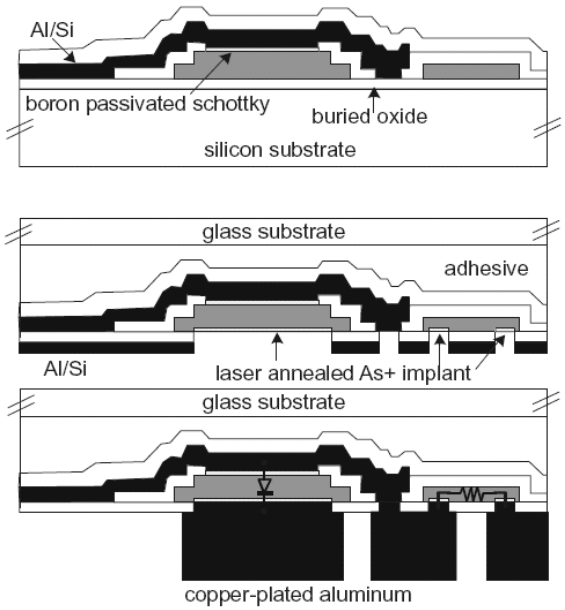


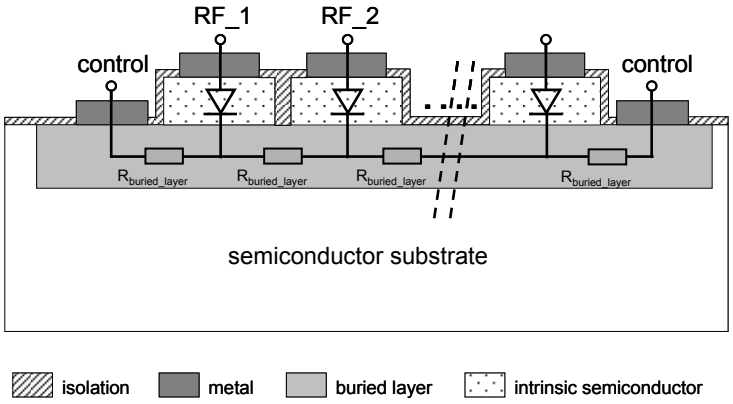
Fig. 5.2. Schematic of the process flow for the integration of silicon-on-glass varactor diodes (From [5]).

5.1.2 Finger based Implementation of the Varactor Stack

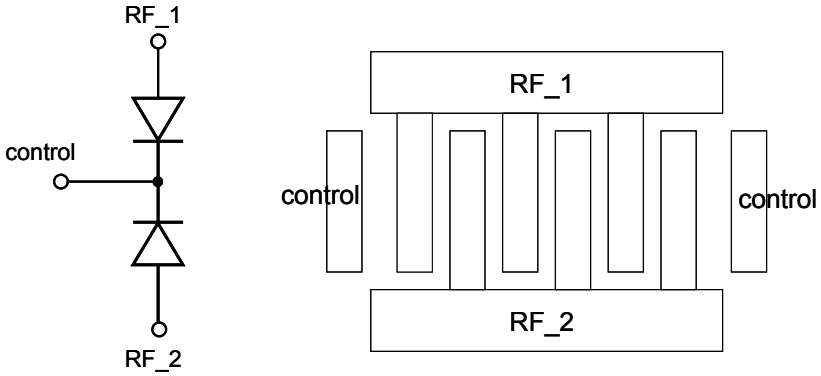
When integrating the varactor stack in conventional process technology, like silicon, GaAs or other wide bandgap materials, a buried layer under the intrinsic area is inevitable for interconnection as illustrated in Fig. 5.3.

In an integrated process technology to optimize the quality factor of a varactor diode with a large capacitance value, typically a finger structure is applied to reduce the influence of the sheet resistance of the buried layer (see Fig. 5.3). This approach is needed since the sheet resistance of the buried layer in an integrated process technology can't be easily reduced to any extent without rising problems of isolating devices from each other. When implementing a varactor stack for RF applications using the finger approach, this method works reasonably well for capacitors with a

moderate capacitance value (e.g. below 10 pF). Since the conditions for the center tap impedance are less strict than those for the RF path, the connection scheme for this terminal is more relaxed and can be limited to one or two contacts for the total structure (see Fig. 5.3).



(a) Cross section



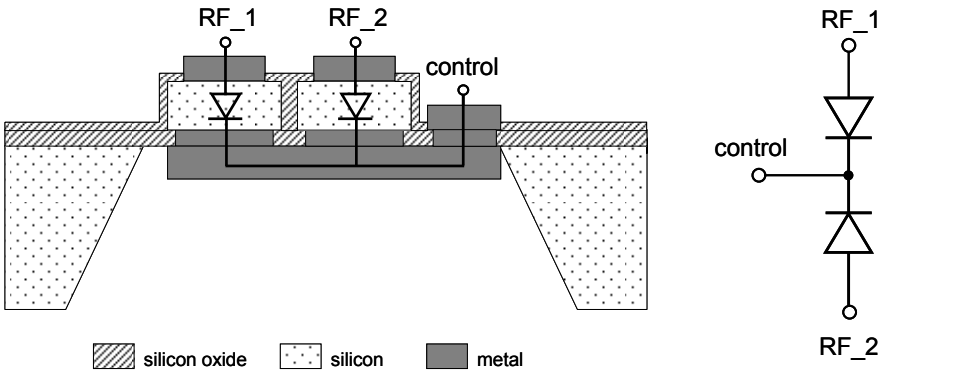
(b) Equivalent schematic (c) Top view

Fig. 5.3. Cross section (a), equivalent schematic (b) and top view (c) of the finger based implementation of varactor stack.

The use of finger structures increases the required area to implement the varactor device since the fingers need to be isolated from each other with a minimum distance of the fingers. Another issue is that the use of finger structures yields increased series resistance of the connecting top metal layer. A third issue is that due to side wall and other parasitic capacitances it is more difficult to accurately achieve the desired exponential $C(V_R)$ relation for these devices. To address these problems related to the 2-D integration, care needs to be taken during layout to reduce the top metal loss while keeping the total structure compact. Moreover, technologies, like trench isolation, can be utilized to reduce the parasitic capacitance and resistance.

5.1.3 Micromachined Back-side Contacted Varactor Stack

A way to drastically reduce the effective sheet resistance of the buried layer in an integrated process technology which requires isolation between individual components is the use of a backside metal contact in combination with micromachining as illustrated Fig. 5. 4. In this figure the backside of the wafer is etched away until the buried layer is reached. This etching can be controlled using an etch-stop layer, e.g. buried oxide in the case by using a silicon-on-isolator wafer or by similar techniques in III-V materials. By making contact holes in the etch-stop layer and directly contacting the buried layer or the lightly doped n region with a thick metal, the effective resistances between the diodes in the RF path can be significantly reduced. Consequently, the sheet resistance of the buried layer is less an issue, since the metal takes care for the conduction of the RF signal. As a result, no finger structures are required anymore on the front side resulting in an effective reduction of the required wafer area and an improved quality factor. Note that in this approach the backside metal does not require high-quality contacts with the front side of the wafer. The only connection to the front side of the wafer is for the implementation of the center-tap terminal. But since this terminal only needs to provide a connection for the DC and baseband signals the impedance requirements of this connection are quite relaxed. In Fig. 5.4, a drawing with the principle of this implementation is given. Note that finger structures at the top side are no longer needed due to the reduced resistance of the backside metal connection. The structure can be further improved /customized by taking measures to improve the mechanical stability, e.g. by gluing or growing mechanical support layers. The implementation of this latest structure is still in process at the time of writing this thesis.



(a) Cross section (b) Equivalent Schematic

Fig. 5.4. Cross section (a) and equivalent schematic (b) of a varactor stack with micromachined backside metal contact.

5.2 Experimental Results of the Silicon-on-Glass (SOG) Low-voltage Varactor Devices

For our experiments, a trial run was first performed using silicon-on-glass technology to implement low-voltage varactor devices to serve applications that do not allow or require the use of high control voltages, like tunable filters [1], [2], phase shifters [3], [4] etc.

5.2.1 Measurement of the C-V_R Dependence and Doping Profile for the SOG Low-voltage Varactor Diode

The varactor parameters (intended and realized) are listed in Table IX. The intended varactor parameters are based on MEDICI simulations [8], which indicated a zero bias depletion depth (x'_{low}) of 50 nm and a tuning range (T_{tune}) of 5. The measured $C(V_R)$ behavior and related electron concentration are given in Fig. 5.5 and Fig. 5.6 respectively. Although not perfect, the measured $C(V_R)$ behavior is very close to the intended one over the voltage range 0.5-3.5 V. The deviation at very low voltages is due to out-diffusion of electrons from the highly doped $N_d x^{-2}$ region into the lightly doped spacer layer. This yields a minor deviation for small reverse bias voltages (Fig. 5.5). In future implementations this deviation can be compensated by slightly increasing the doping concentration close to x_{low}. The measured electron concentration, which is a good indication of the realized doping profile, starts to deviate from the $N_d x^{-2}$ relation at 175 nm due to an imperfect transition to the backside contact of the varactor. This deviation (Fig. 5.6) limits the quality factor of the realized varactors. The extracted parameters from the $C(V_R)$ measurements are given in Table IX.

Table IX. Main parameters of the processed varactor stack extracted from the measurement results, compared with the designed values

Parameters	x'_{low} (nm)	x_{high} (nm)	a_2 (V^{-1})	V_{R_max} (V)	$V_{breakdown}$ (V)	T_{tune} @$V_{R\,Max}$
Designed	50	250	0.358	5	5	5
Measured	50	175	0.358	3.5	> 5	3.5

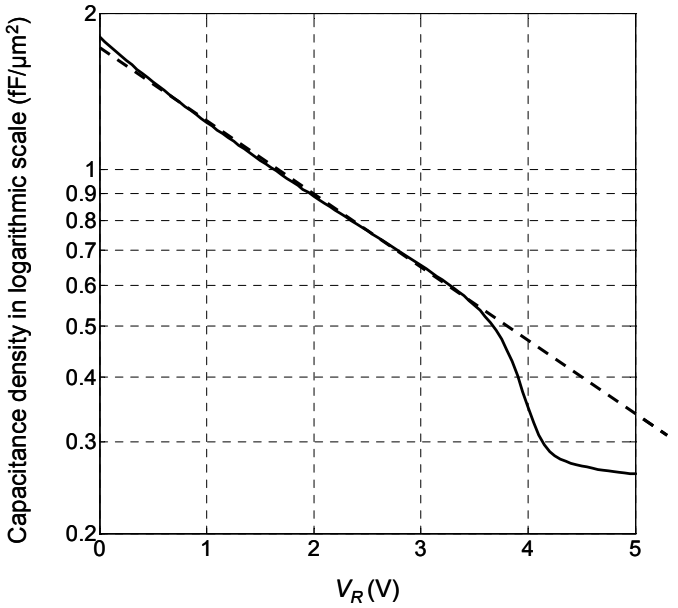


Fig. 5.5. Measured C-V_R dependency (the dashed line indicates the ideal exponential relationship).

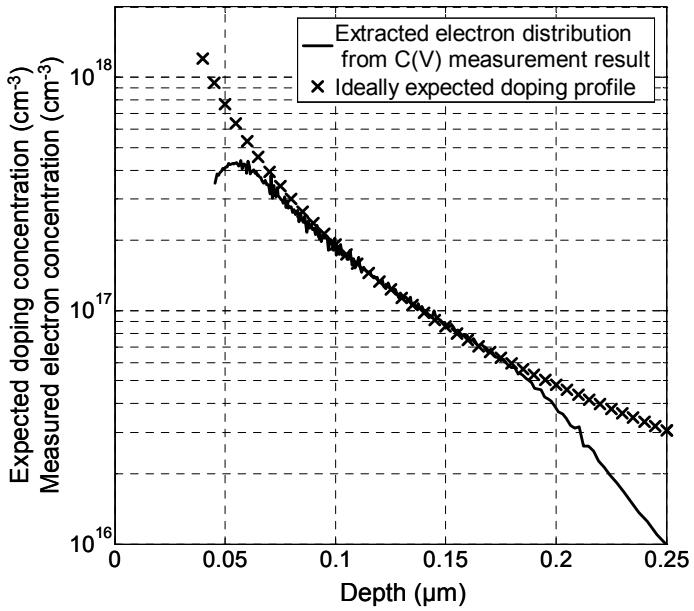


Fig. 5.6. Extracted electron distribution from $C(V_R)$ measurement compared with the ideal doping profile.

5.2.2 Linearity Measurements of the SOG Low-voltage Devices

To verify the linearity theory, the proposed narrow tone-spacing varactor stack devices need to be combined with the proper harmonic terminations. For this purpose we have used a shunt varactor stack of 33 pF in a two-port configuration with 10 nH inductive center tap connection. A microphotograph of the layout is given in Fig. 5.7.

Linearity testing of the structure of Fig. 5.7 was performed using a two-tone signal (f_{center} = 2.14 GHz) with varying tone spacing. For the calibrated power measurements, we have used the system of [9]. Fig. 5.8 plots the measured and simulated distortion component at $2f_1$-f_2 as a function of output power for different values of tone spacing. The measurement results confirm that successful third-order distortion cancellation occurs for low-tone spacing (see the results for 10 kHz, 100 kHz and 1 MHz) resulting in a slope of 4:1 versus output power for the distortion component at $2f_1$-f_2 (in dBc). The slope of 4:1 indicates that the remaining source of nonlinearity is the much smaller fifth-order distortion component (IM_5). For large tone spacing (> 10 MHz), the third-order distortion cancellation condition is violated by the increased center-tap impedance of the inductor for the baseband frequency $(f_2$-$f_1)$. Consequently, a slope of 2:1 versus output power for the now IM_3-dominated distortion at $2f_1$-f_2 (in dBc) is observed as expected.

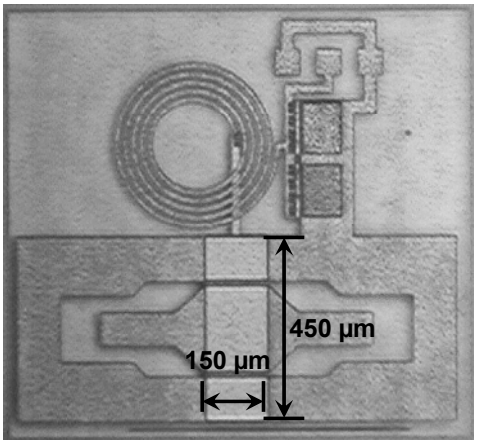


Fig. 5.7. Microphotograph of the 33 pF varactor stack used in the $C(V_R)$ and linearity measurements with 10 nH center-tap inductor.

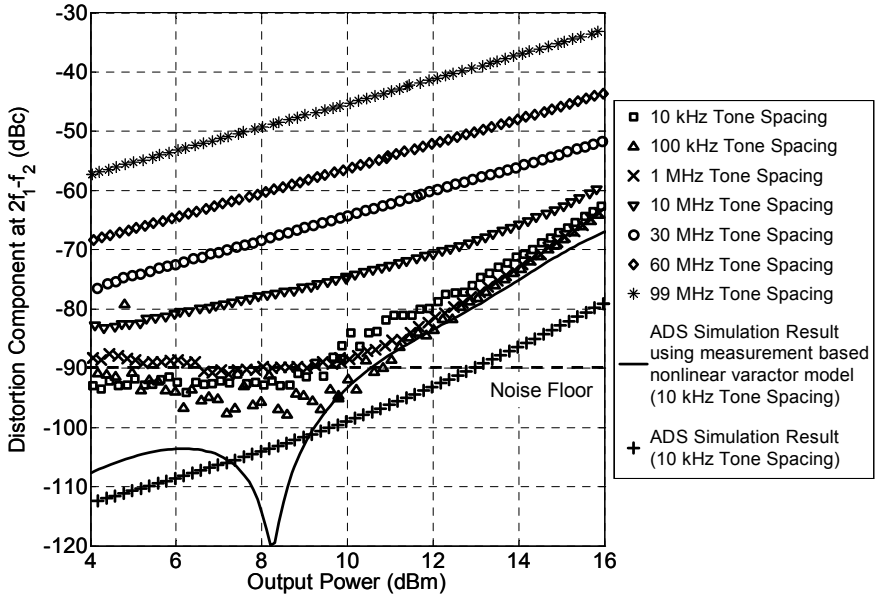


Fig. 5.8. Measured and simulated distortion components at $2f_1$-f_2 versus output power [capacitance of varactor stack = 33 pF, center tap inductance = 10 nH (simulated self resonation frequency > 8 GHz), $a_2 = 0.358\ V^{-1}$, $f_{center} = 2.14$ GHz and $V_R = 2$ V].

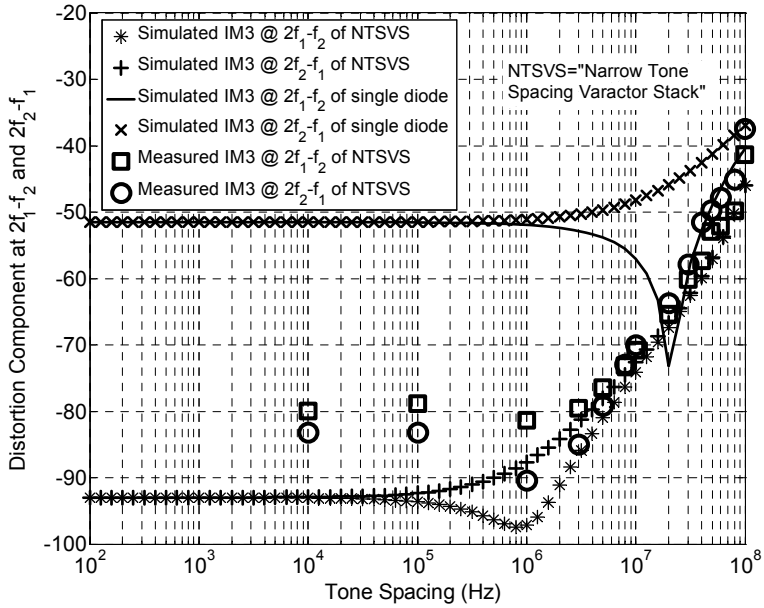


Fig. 5.9. Measured and simulated distortion components at $2f_1$-f_2 and $2f_2$-f_1 as function of tone spacing at a power level of 12 dBm (capacitance of varactor stack = 33 pF, center tap inductance = 10 nH, $a_2 = 0.358\ V^{-1}$, $f_{center} = 2.14$ GHz and $V_R = 2$ V).

When comparing our measured linearity with the harmonic balance simulation results based on ideal varactor devices with a perfect exponential $C(V_R)$ relation, we find - in spite of the already overwhelming linearity improvement - that there is a 10 dB discrepancy. To investigate if this deviation can be related to imperfections of the realized $C(V_R)$ behavior, a nonlinear varactor model based on a 15th-order polynomial fit of the measured $C(V_R)$ data was developed within ADS. As Fig. 5.8 shows, the modeled $C(V_R)$ behavior of the fabricated diodes explains the measured increase in distortion. Consequently even better linearity is feasible by further optimization of the $N_d x^{-2}$ profile. Finally, Fig. 5.9 plots the measured and simulated distortion component at $2f_1$-f_2 and $2f_2$-f_1 as function of tone spacing at a power level of 12 dBm, a value that corresponds with peak voltage amplitude of 2.5 V over the varactor stack. The narrow tone-spacing varactor stack clearly offers a superior performance over the single diode (with comparable effective capacitance) and the results match the theory quite well.

5.3 Experimental Results of the SOG High-voltage Varactor Devices

In the second testing run, we aimed for varactor devices with a breakdown voltage of 20 V, capacitance tuning range of 6:1, and epi-layer thicknesses of 1.1 µm were realized. For these varactors MEDICI [8] simulations predicted a quality factor of 50 at zero bias (worst case).

5.3.1 Measurement of the C-V_R and Q-V_R Dependence for the SOG High-voltage Varactor Diode

According to the previous discussion, from the technology perspective, the implementation of the $N_d x^{-2}$ doping profile, and the resulting exponential $C(V_R)$ relationship, is critical for achieving optimum performance. To verify the $C(V_R)$ relation, we measured the capacitance density of a single diode as function of bias voltage. The varactor diode has a zero bias capacitance of 1 pF.

The $C(V_R)$ and $Q(V_R)$ behavior is shown in Fig. 5.10. The $C(V_R)$ behavior exhibits a straight line in the logarithmic plot as a function of reverse voltage, indicating a near-ideal exponential $C(V_R)$ relationship. The measured quality factor is 43 at zero bias. However, at 11.5 V, the Q has already increased to 192, indicating the advantage of copper plating. Above 11.5 V the varactor suffers from a steep increase in leakage current due to imperfections in the epilayer; this restricts its useable voltage range and consequently also the upper limit for Q.

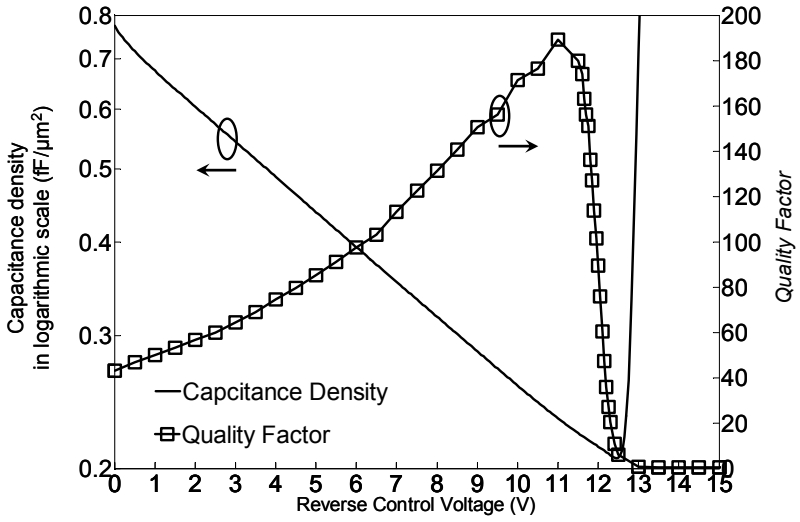


Fig. 5.10. Measured C-V_R and *Quality Factor*-V_R dependence as function of reverse control voltage (V_R) at 1.95 GHz.

5.3.2 Linearity Measurements of the Narrow Tone-spacing Varctor Stack using SOG High-voltage Varactor Diodes

As done above for the low-voltage varactors, a two-port configuration of a shunt 10 pF narrow tone-spacing varactor stack with 20 nH terminations is used (Fig. 5.11). This configuration is measured using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing. Fig. 5.12 plots the measured distortion component at $2f_1$-f_2 as a function of output power for different values of tone spacing. It can be observed that the linearity improves with decreasing tone spacing. Note that the linearity at low-tone spacing is comparable to that of the measurement setup as shown for the tone spacing below 30 MHz in Fig. 5.12. Since at these linearity levels it becomes difficult to separate the non-linearities resulting from the varactors from that of the measurement setup, a conservative boundary of trust is marked as "measurement limitation" in Fig. 5.12. Consequently, conservatively speaking, an OIP_3 > 57 dBm is achieved up to 30 MHz tone spacing.

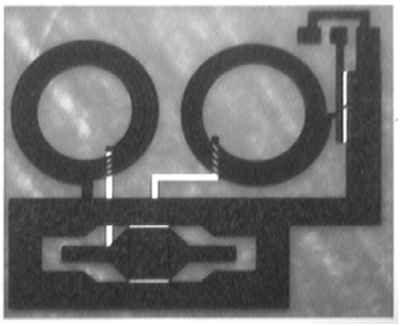


Fig. 5.11. Microphotograph of the 10 pF SOG narrow tone-spacing varactor stack used in the linearity measurements (inductance at terminations = 20 nH with the self resonation frequency above 6 GHz).

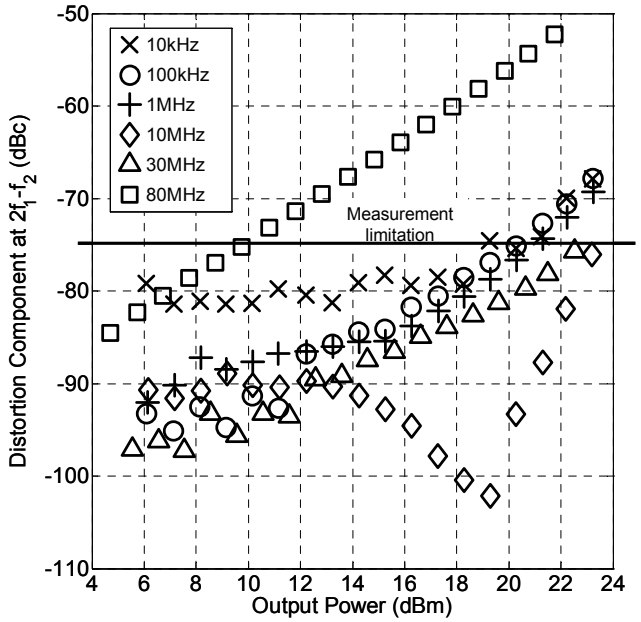


Fig. 5.12. Measured distortion components at $2f_1$-f_2 versus output power for the SOG narrow tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, inductance at terminations = 20 nH, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V).

In order to confirm that the narrow tone-spacing varactor stack can provide superior linearity for any surrounding circuit condition, the source-pull setup of Fig. 5.13 is used. In these experiments the two-tone source voltage (V_s) is adjusted with the tunable source impedance, such that for all loading conditions the voltage amplitude over the varactor ($V_{varactor}$) stack is kept close to 4 V for each tone yielding an envelope

peak voltage of 8 V. Since the varactor stack is reverse biased at 5 V and the RF voltage will split over the varactor diodes, the diodes are operated close to their maximum voltage swing but will remain reverse biased at all times.

The frequency components of the resulting source current are used to monitor the linearity of the varactor. Due to the fact that the inductors satisfy the low-impedance requirements for the baseband signals, source independent IM_3 cancellation takes place. The remaining IM_5 components in the external current at $2f_1$-f_2 in dBc, relative to the fundamental, has been simulated as function of the source impedance and plotted as contours of constant distortion for different values of tone spacing (Fig. 5.14). From these results we conclude that the narrow tone-spacing varactor stack element in this experiment provides an $IM_5 <$ -60 dBc for any source impedance up to 10 MHz bandwidth. At higher tone spacing (40 MHz and 52 MHz) the linearity degrades as expected. Since the linearity of the varactor outperforms that of the measurement setup in most of the conditions, only several points can be accurately measured for a tone spacing of 40 MHz and 52 MHz. These measured results are also indicated in Fig. 5.14(c) and (d) and confirm the trend of the simulated linearity. Note that a slightly inductive source yields the "worst" linearity, since, in combination with the capacitive varactor stack, it provides a close to perfect AC short causing all available non-linear current to flow through the source.

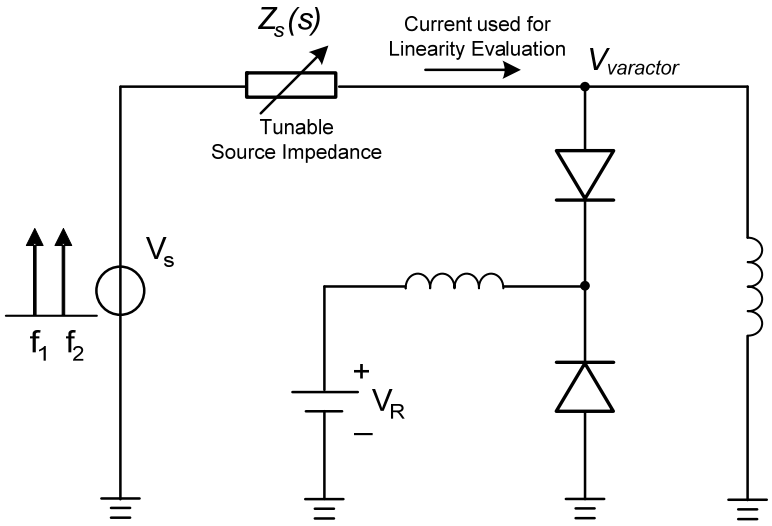
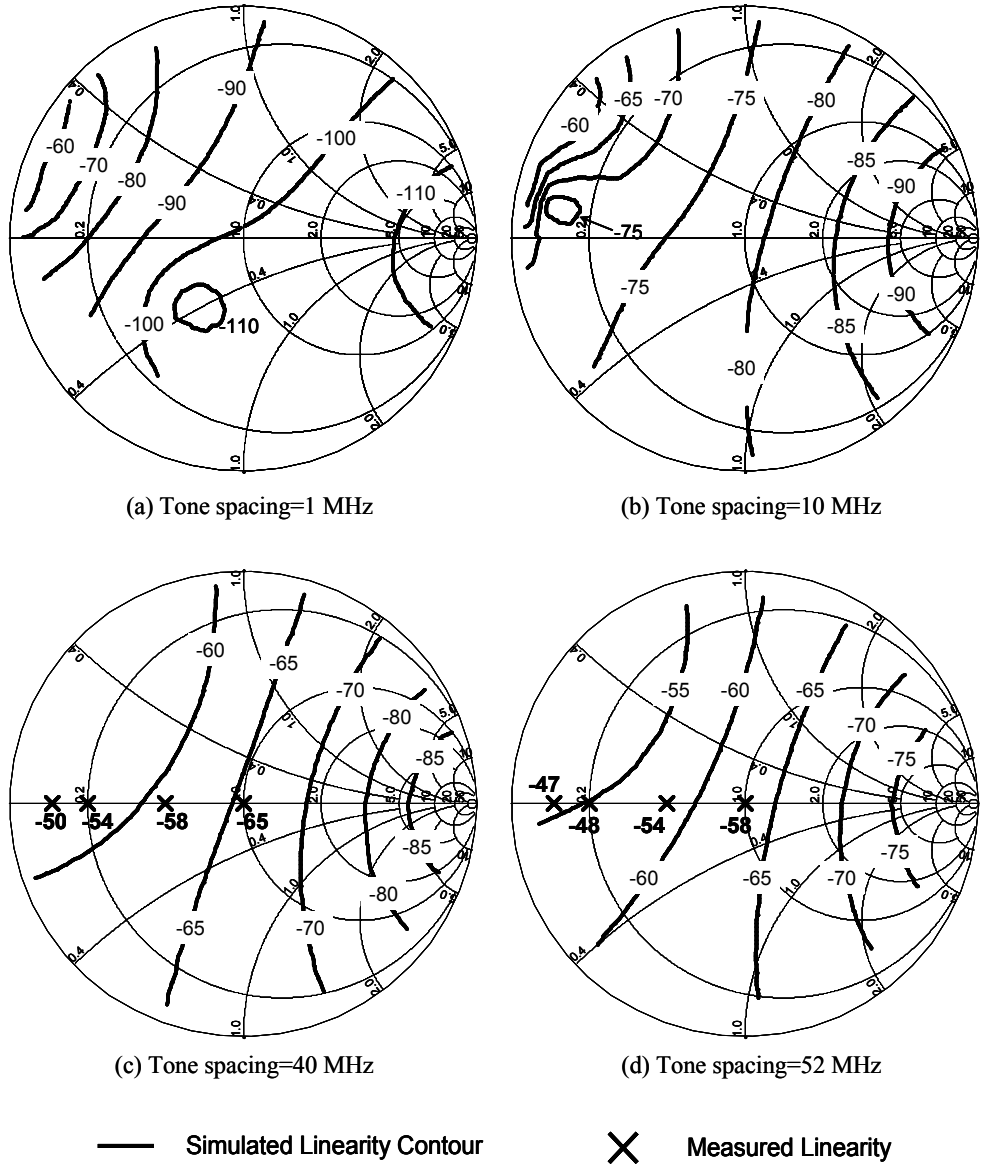


Fig. 5.13. Source-pull setup used to evaluate the linearity of SOG narrow tone-spacing varactor stack for different impedances of the surrounding circuitry (effective zero bias capacitance = 10 pF, inductance at terminations = 20 nH, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V).



(a) Tone spacing=1 MHz

(b) Tone spacing=10 MHz

(c) Tone spacing=40 MHz

(d) Tone spacing=52 MHz

Fig. 5.14. Simulated linearity contours and measured linearity points as function of the source impedances of the remaining IM_5 components in the source current at $2f_1$-f_2 in dBc for different values of tone spacing. The envelope peak voltage over the varactor stack is kept constant at 8 V (effective zero bias capacitance = 10 pF, inductance at terminations = 20 nH, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V).

5.3.3 Linearity Measurements of the Wide Tone-spacing Varctor Stack using SOG High-voltage Varactor Diodes

To verify the linearity of the wide tone-spacing varactor stack, we have measured the shunt wide tone-spacing varactor stack with an effective zero bias capacitance of 10 pF in a two-port configuration using a 500 kΩ resistive center-tap connection (see Fig. 5.15).

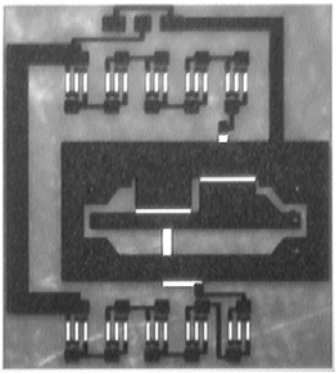


Fig. 5.15. Microphotograph of the 10 pF SOG wide tone-spacing varactor stack used in the linearity measurements with 500 kΩ center-tap resistor.

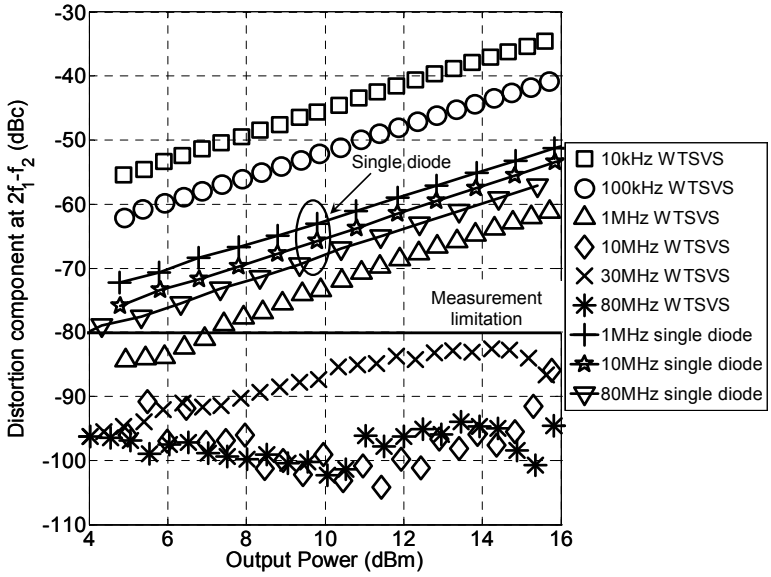


Fig. 5.16. Measured distortion components at $2f_1$-f_2 versus output power for the SOG single diode and the SOG wide tone-spacing varactor stack with the center-tap resistance of 500 kΩ (for both cases: the effective zero bias capacitance = 10 pF, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V).

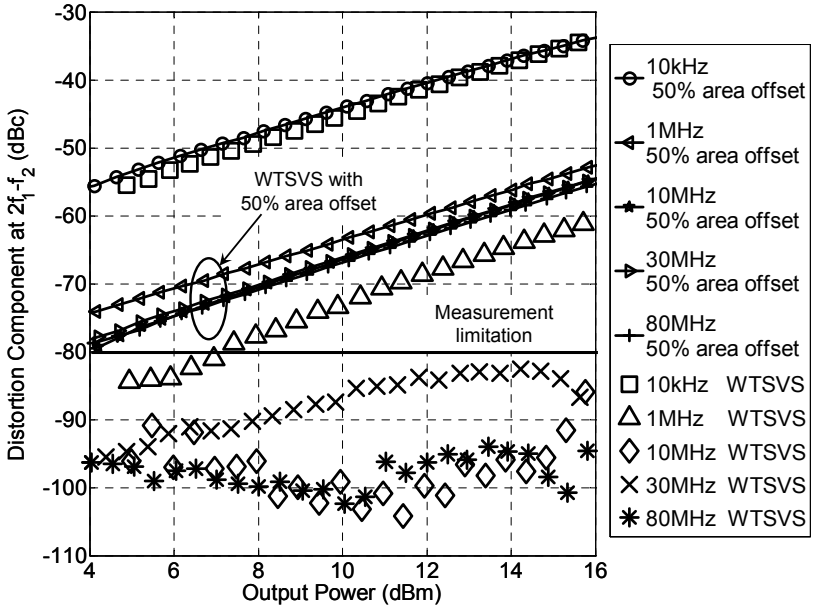


Fig. 5.17. Measured distortion components at $2f_1$-f_2 versus output power for the SOG wide tone-spacing varactor stack with proper area ratio (X = 3.7) and wide tone-spacing varactor stack with 50% area ratio offset (X = 1.9) (for both cases: the effective zero bias capacitance = 10 pF, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V).

The linearity testing is performed using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing [9]. Fig. 5.15 plots the measured distortion components at $2f_1$-f_2 as a function of output power for different values of tone spacing. It can be observed that the linearity improves with the increase of tone spacing and a superior linearity over that of the single diode is obtained for a tone spacing higher than 10 MHz. Note that the linearity at high tone spacing is comparable to that of the measurement setup as shown for the tone spacing of 10 MHz, 30 MHz and 80 MHz in Fig. 5.16. Since at these linearity levels it becomes difficult to separate the non-linearities resulting from the varactors from that of the measurement setup, a conservative boundary of trust is marked as "measurement limitation" in Fig. 5.16 and the following figures. Consequently, conservatively speaking, the OIP_3 will be larger than 56 dBm for a tone spacing larger than 10 MHz. Note that we use here OIP_3 rather than IIP_3, since a significant part of the input power will be reflected by the varactor shunt impedance. Therefore, the output power level is a better measure of the actual RF voltage over the varactors. It is this voltage that determines the resulting IM_3 / IM_5 levels.

Normally, it is handy to consider the $2f_1$-f_2 or $2f_2$-f_1 components as function of power (in dBc) to verify if the third-order distortion is truly cancelled and only IM_5

distortion remains. Note that for this condition, a 4:1 slope should be found. However, in our experiments the distortion level is so low that this phenomenon is difficult to verify experimentally. Fortunately, we also implemented varactor stacks with an area ratio of 1.9 instead of 3.7, which we have tested for their linearity as reference. These devices have a 50% area ratio offset with respect to the ideal ratio needed for IM_3 cancellation. By comparing the linearity of the ideal wide tone-spacing varactor stack with these structures, the IM_3 cancellation was verified. As shown in Fig. 5.17, the correctly dimensioned wide tone-spacing varactor stack clearly offers superior performance over the wide tone-spacing varactor stack with 50% area ratio offset, especially for the tone spacing larger than 10 MHz.

5.3.4 Overview of the Narrow Tone-Spacing Varactor Stack and the Wide Tone-Spacing Varactor Stack

In order to complete our overview for the linearity of the narrow tone-spacing varactor stack and wide tone-spacing varactor stack, we plot the measured and simulated distortion component at $2f_1$-f_2 as function of tone spacing at an output power level of 15 dBm (Fig. 5.18).

According to the simulation results, the wide tone-spacing varactor stack starts to offer better linearity than the narrow tone-spacing varactor stack above 5 MHz tone spacing for the center-tap impedances indicated. Note that the implementation of the center-tap impedance determines the linearity bandwidth. E.g. when using a higher impedance for the wide tone-spacing varactor stack center-tap (now 500 kΩ) the high linearity operation can be extended to much lower frequencies. Taking the influence of the leakage current into account, the measurement results of the wide tone-spacing varactor stack match the simulation quite well. It can be observed that for the wide tone-spacing varactor stack structure the presence of the leakage currents will cause a modulation of the center-tap voltage for narrow tone spacing, resulting in linearity degradation. Even if so, the combination of the narrow tone-spacing varactor stack and wide tone-spacing varactor stack provide a superior linearity (below the measurement limitation: -80 dBc) for the whole range of the tone spacing, making them very attractive candidates for many RF applications.

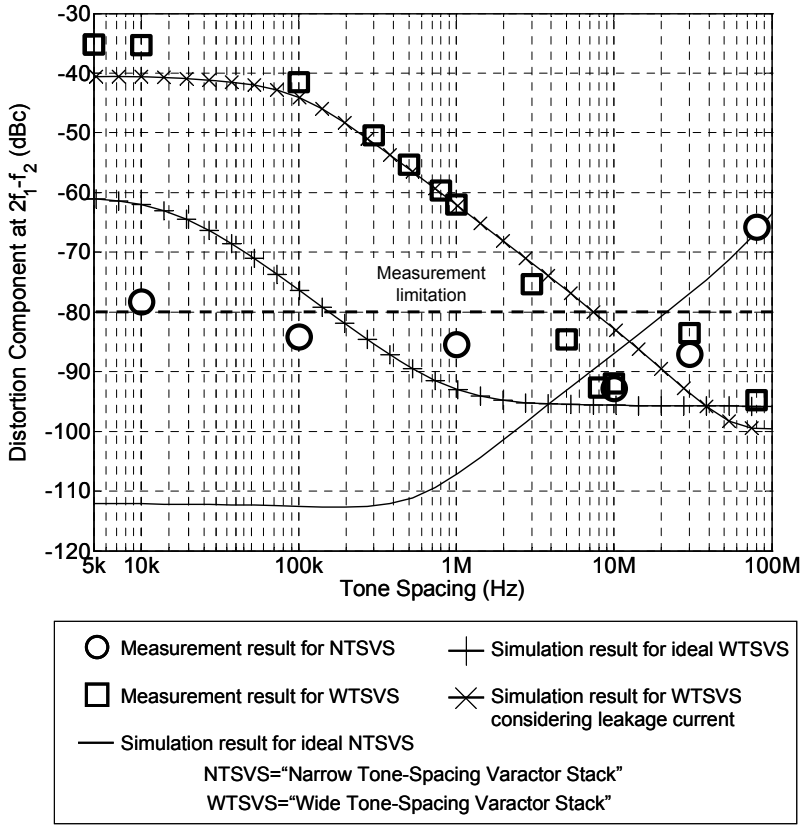


Fig. 5.18. Measured and simulated distortion component at $2f_1$-f_2 as function of tone spacing at a power level of 15 dBm (for both cases: effective zero bias capacitance = 10 pF, f_{center} = 2 GHz, a_2 = 0.0896 V^{-1} and V_R = 5 V). The SOG narrow tone-spacing varactor stack has two inductors of 20 nH at terminations (see Fig. 5.11), while the center-tap resistance of the wide tone-spacing varactor stack is 500 kΩ (see Fig. 5.15).

5.3.5 Measurement of the Multi-stacked Narrow Tone-Spacing Varactor Stack using SOG High-voltage Varactor Diodes

In order to check the effectiveness of the multi-stack topology, a 2.7 pF 3×stacked narrow tone-spacing varactor stack as shown in Fig. 5.19 is implemented using high-voltage varactor devices with DIMES silicon-on-glass technology.

The measured quality factor at 2 GHz is approximately 40 and the capacitance tuning ratio is 3:1 with the maximum control voltage of 10 V (Fig. 5.20). Note that

even better quality factor can be achieved if diode leakage currents are reduced; in that case the quality factor will increase with V_R.

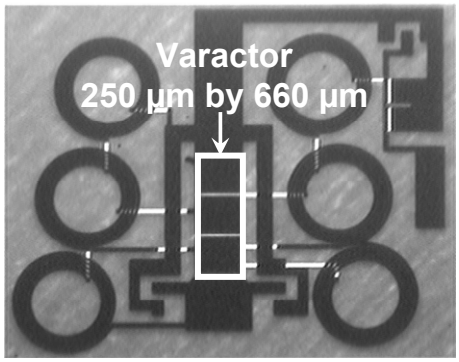


Fig. 5.19. The 2.7 pF 3-stacked SOG narrow tone-spacing varactor stack used for the measurements (six 20 nH inductors are used to implement the harmonic baseband "short" while providing high impedance for the fundamental and harmonics).

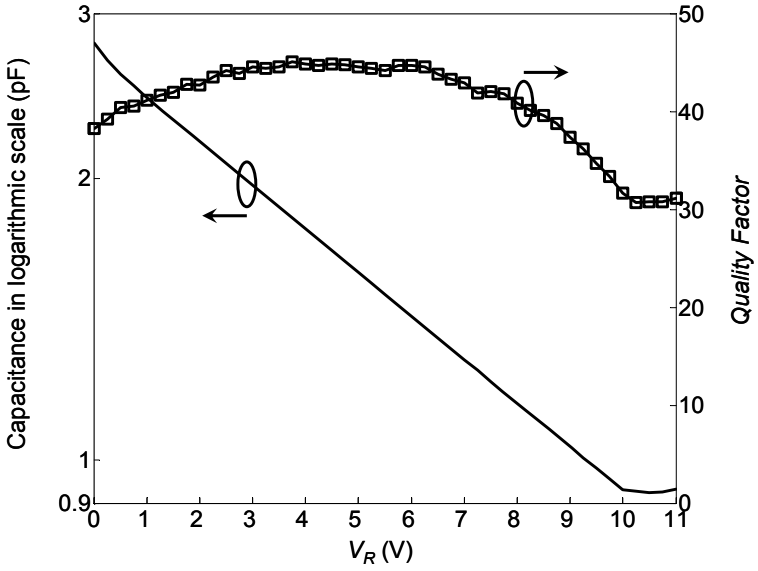


Fig. 5.20. Measured C-V_R and Q-V_R dependence at 2 GHz. Note that the $C(V_R)$ measurements yield a straight line in the logarithmic plot as a function of reverse voltage, indicating a near-ideal exponential $C(V_R)$ relationship.

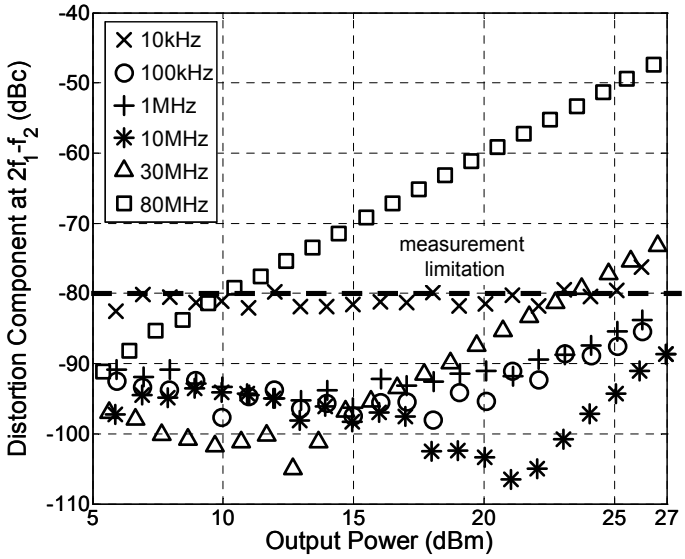


Fig. 5.21. Measured distortion components at $2f_1$-f_2 versus output power at different tone spacings for a two-tone input signal with the f_{center} of 2 GHz (capacitance at zero bias voltage = 2.7 pF, V_R = 5 V).

The linearity testing is performed using a two-tone signal (f_{center} = 2 GHz) as function of power using the setup described in [9]. Fig. 5.21 plots the measured distortion components at $2f_1$-f_2 as a function of output power for different values of tone spacing. Note that the linearity of signals with tone spacing below 30 MHz is comparable to that of the measurement setup and for that reason the conservative boundary of trust is marked as "measurement limitation" in Fig. 5.21. Conservatively speaking the measured OIP_3 is larger than 67 dBm up to 10 MHz bandwidth, which is 22 dB better than the reported 9-stacked BST varactor in [10] and comparable to that of MEMS switched devices. The maximum power, which can be handled by the measurement setup, is 27 dBm, a value corresponds with peak voltage amplitude of 14.2 V. However, in practice, this structure will be capable of handling a maximum power of 33.5 dBm, equivalent to a peak voltage amplitude of 30 V (assuming output impedance = 50 Ω).

5.4 Experimental Results of the GaAs Large-tuning-range Varactor Devices

In the previous testing runs, silicon-on-glass process is utilized for the implementation of the varactor diodes. In the SOG varactor process the varactor diode

is a very straightforward "one-dimensional" structure, for which the advantages of the two-sided contacting are over-evident. Using this feature, many parasitics, like the buried layer series resistance and substrate losses, are significantly reduced. As a result, the series resistance of the intrinsic silicon becomes the bottleneck that limits the quality factor of the varactors, especially for those varactors with large tuning ranges, for which normally thick intrinsic doping profiles are epitaxially developed. Fortunately, the use of the high-mobility semiconductors can be the solution, e.g. the series resistance can be reduced by 5-6 times for a GaAs implemenation. In light of this, GaAs varactor devices, aiming for large tuning ranges, are fabricated in Skyworks' GaAs technology.

5.4.1 Measurement of the C-V_R and Q-V_R Dependence for the GaAs Large-tuning-range Varactor Diode

As done in the previous sections, $C(V_R)$ dependence is first measured to confirm good implementation of exponential $C(V_R)$ relationship, one of the most critical issues for optimum linearity performance. To verify the $C(V_R)$ relation, we measured the 10 pF narrow tone-spacing varactor stack with 10 nH inductive center-tap connection. The resulting $C(V_R)$ and $Q(V_R)$ behaviors are shown in Fig. 5.22.

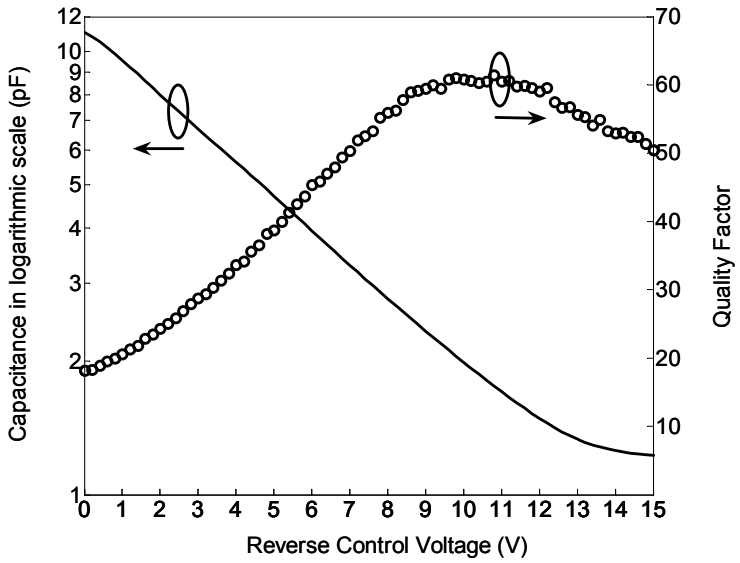


Fig. 5.22. Measured C-V_R and Q-V_R dependence at 2 GHz for 10 pF GaAs narrow tone-spacing varactor stack with 10 nH inductive center-tap connection.

The $C(V_R)$ behavior exhibits a straight line in the logarithmic plot as a function of reverse voltage, indicating a near-ideal exponential $C(V_R)$ relationship. The measured capacitance ranges from 1.23 pF to 11 pF, corresponding with a tuning range as large as 9:1, which is the maximum achieved value among all existing continuously tunable elements. The average quality factor at 2 GHz is 50, accompanied with the breakdown voltage above 28 V. The fact that breakdown voltage (> 28 V) is much higher than the maximum control voltage (V_{R_max} = 15 V for full depletion) indicates that one may further improve the quality factor by increasing the intrinsic doping concentration. In the meanwhile, the use of thick connecting metal and higher doped buried layer can also help to enhance the quality factor.

5.4.2 Linearity Measurements of the GaAs Large-tuning-range Varactors

To confirm that the proposed varactor configurations can also work well for "two-dimensional" diodes, i.e., finger-based structures, four testing structures are fabricated within Skyworks' GaAs technology as listed below:

- LV_A: 10 pF GaAs narrow tone-spacing varactor stack with 10 nH inductive center-tap connection
- LV_B: 10 pF GaAs narrow tone-spacing varactor stack with 2 kΩ or 12 kΩ resistive center-tap connection
- LV_C: 2.5 pF GaAs narrow tone-spacing varactor stack with 10 kΩ or 50 kΩ resistive center-tap connection
- LV_D: 10 pF GaAs wide tone-spacing varactor stack with 200 kΩ resistive center-tap connection

Linearity testing was performed using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing making use of active load-pull system [9].

The measurement results of the inductive center-tapped narrow tone-spacing varactor stack (LV_A) are shown in Fig. 5.23 and 5.24. Fig. 5.23 plots the measured distortion component at $2f_2$-f_1 as a function of output power for different values of tone spacing. The measurement results again confirm that successful third-order distortion cancellation occurs for low-tone spacings through the slope of 4:1 versus output power for the distortion component at $2f_2$-f_1 (in dBc). The resulting OIP_3 are roughly 57 dBm at the out power level of 20 dBm and 53 dBm when the output power equals to 24 dBm. Fig. 5.24 plots the measured and simulated distortion component at $2f_2$-f_1 as function of tone spacing at a power level of 24 dBm, where one may observe that the measurement results match the simulation quite well and the 6 dB corner frequency (Δf_{corner}) is around 10 MHz, a value strongly supporting the theory of Section 3.3.3.

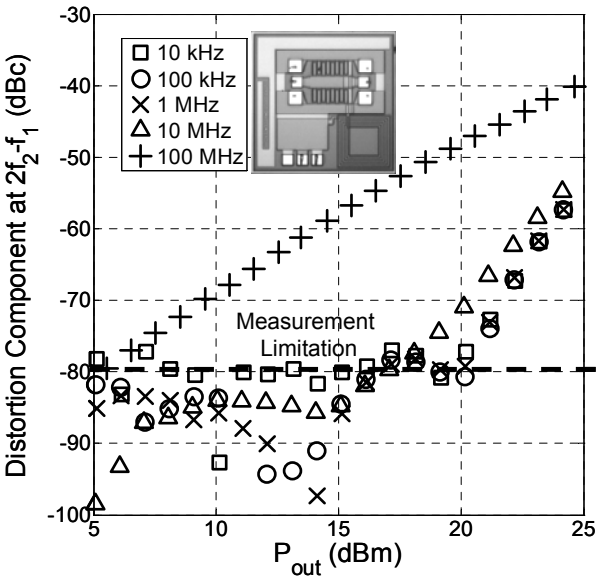


Fig. 5.23. Measured distortion components at $2f_2$-f_1 versus output power for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, inductance at terminations = 10 nH, f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

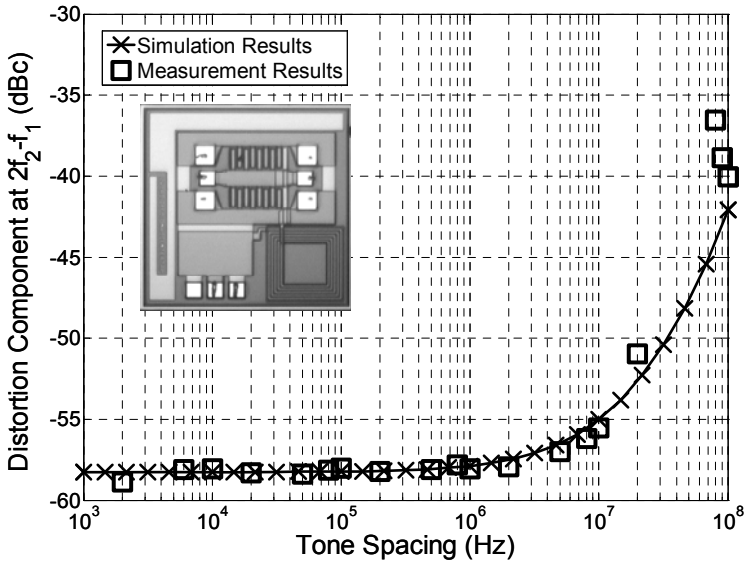


Fig. 5.24. Measured and simulated distortion components at $2f_2$-f_1 as function of tone spacing at a power level of 24 dBm for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, inductance at terminations = 10 nH, f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

The measurement results of the resistive center-tapped GaAs narrow tone-spacing varactor stack (LV_B and LV_C) are shown in Fig. 5.25 – 5.28.

Fig. 5.25 and 5.26 plots the measured distortion component at $2f_2$-f_1 as a function of output power for different values of tone spacing. It proves that resistive center-tap impedances can be also used for IM_3 cancellation regardless of the varactor's capacitance values.

Fig. 5.27 and 5.28 plots the measured and simulated distortion component at $2f_2$-f_1 as function of tone spacing at the output power level of 24 dBm. The resulting OIP_3 are roughly 48 dBm at the out power level of 24 dBm and the 6 dB corner frequency (Δf_{corner}) is around 500 kHz. Note that the device becomes more compact by making use of resistive center-tap impedance. However, in order not to degrade the varactor's quality factor, this resistance needs to be properly chosen according to its capacitance value and for this reason the resulting 6 dB corner frequency is normally limited up to 1 MHz. When the tone spacing is small, the presence of the leakage currents will cause a modulation of the center-tap voltage, resulting in linearity degradation, especially for those big resistance values. Fortunately, the influence of the leakage currents on the linearity can be controlled to a certain degree by utilizing a moderate valued center-tap resistance, e.g. 2 kΩ used in LV_B (effective zero bias capacitance = 10 pF) and 10 kΩ used in LV_C (effective zero bias capacitance = 2.5 pF) as shown in Fig. 5.27 and 5.28.

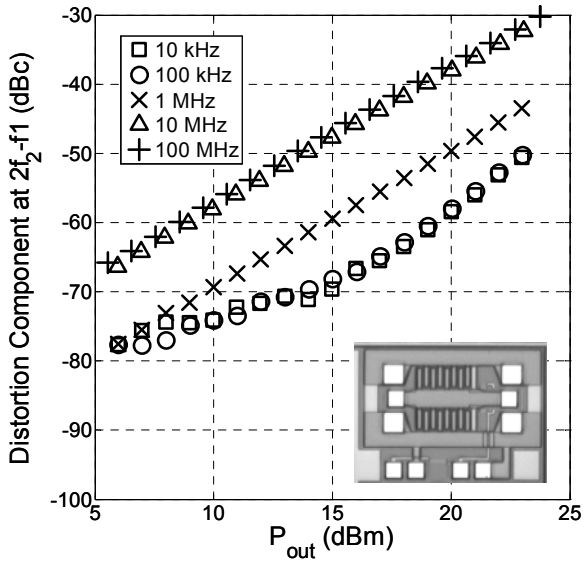


Fig. 5.25. Measured distortion components at $2f_2$-f_1 versus output power for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, resistance at terminations = 2 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

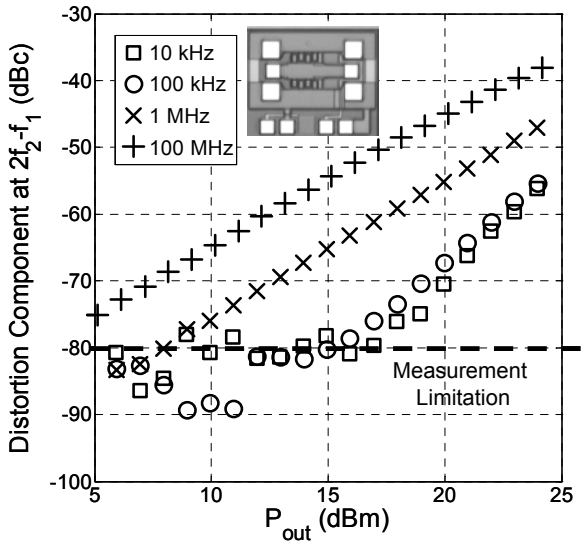


Fig. 5.26. Measured distortion components at $2f_2$-f_1 versus output power for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 2.5 pF, resistance at terminations = 10 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

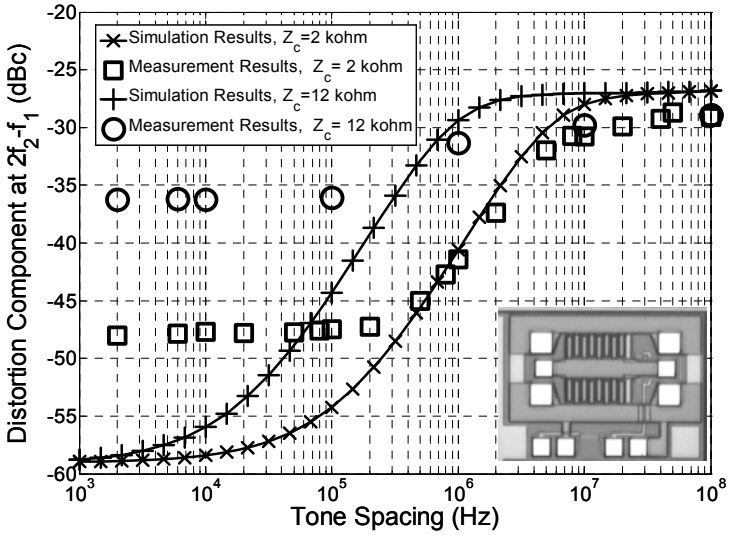


Fig. 5.27. Measured and simulated distortion components at $2f_2$-f_1 as function of tone spacing at a power level of 24 dBm for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, resistance at terminations = 2 kΩ or 12 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

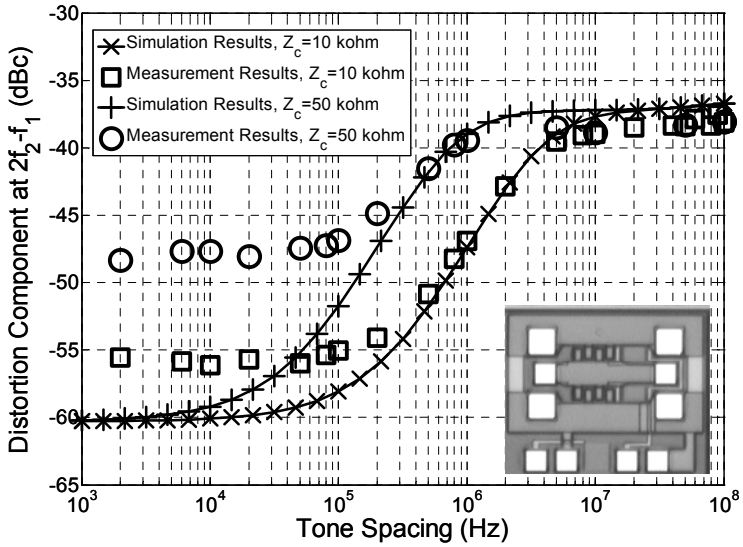


Fig. 5.28. Measured and simulated distortion components at $2f_2$-f_1 as function of tone spacing at a power level of 24 dBm for the GaAs narrow tone-spacing varactor stack (the effective zero bias capacitance = 2.5 pF, resistance at terminations = 10 kΩ or 50 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

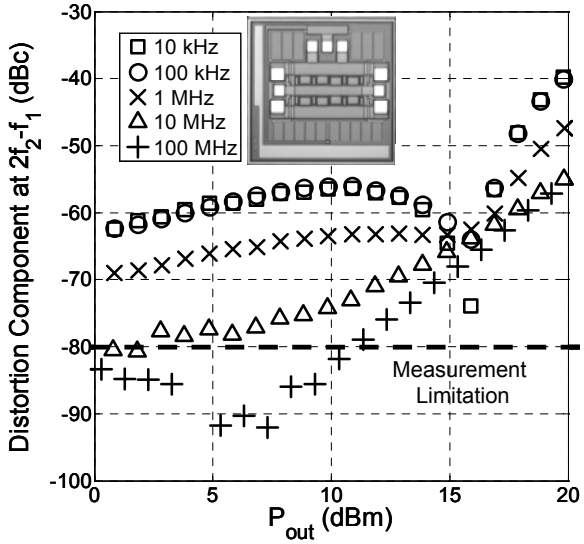


Fig. 5.29. Measured distortion components at $2f_2$-f_1 versus output power for the GaAs wide tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, resistance at terminations = 200 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

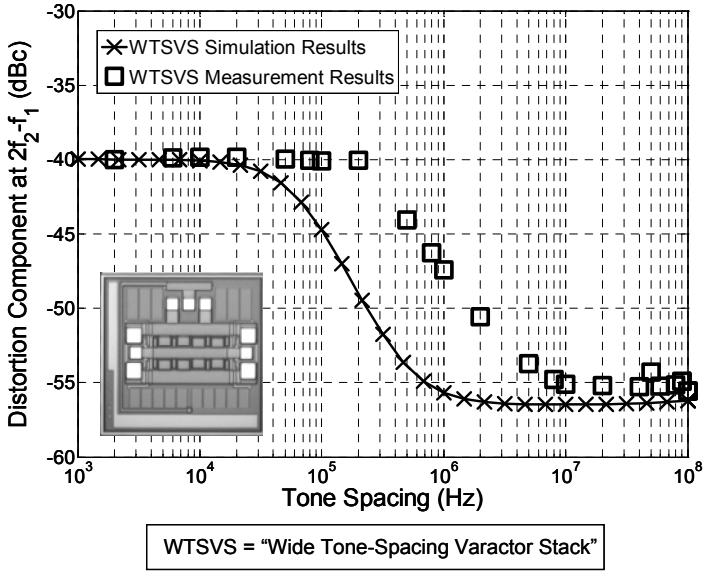


Fig. 5.30. Measured and simulated distortion components at $2f_2$-f_1 as function of tone spacing at a power level of 20 dBm for the GaAs wide tone-spacing varactor stack (the effective zero bias capacitance = 10 pF, resistance at terminations = 200 kΩ , f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

The measurement results of the resistive center-tapped GaAs wide tone-spacing varactor stack (LV_D) are shown in Fig. 5.29 and 5.30. Fig. 5.29 plots the measured distortion components at $2f_2$-f_1 as a function of output power for different values of tone spacing. It can be observed that the linearity improves with the increase of tone spacing and the third-order distortion is truly cancelled for the tone spacing of 10MHz and 100 MHz. Fig. 5.30 plots the measured and simulated distortion component at $2f_2$-f_1 as function of tone spacing at the output power level of 20 dBm. It can be observed that the resulting OIP_3 is roughly 48 dBm at an output power level of 20 dBm for a tone spacing larger than 10 MHz.

For an overview of the linearity of the narrow tone-spacing varactor stack and wide tone-spacing varactor stack with GaAs large-tuning-range varactor diodes, we plot the measured distortion component at $2f_2$-f_1 as function of tone spacing at an output power level of 20 dBm in Fig. 5.31. As one may observe, it proves once again that the wide tone-spacing varactor stack and the narrow tone-spacing varactor stack provide complementary linearity behavior in terms of tone spacing. The combination of the narrow tone-spacing varactor stack and wide tone-spacing varactor stack provide a superior linearity (below -56 dBc and OIP_3 > 48 dBm) for the whole range of the tone spacing. Note that all of these topologies can be implemented on the same wafer by using different planar layout. In view of this, one may freely choose the proper devices according to the availability of chip area and RF application specification.

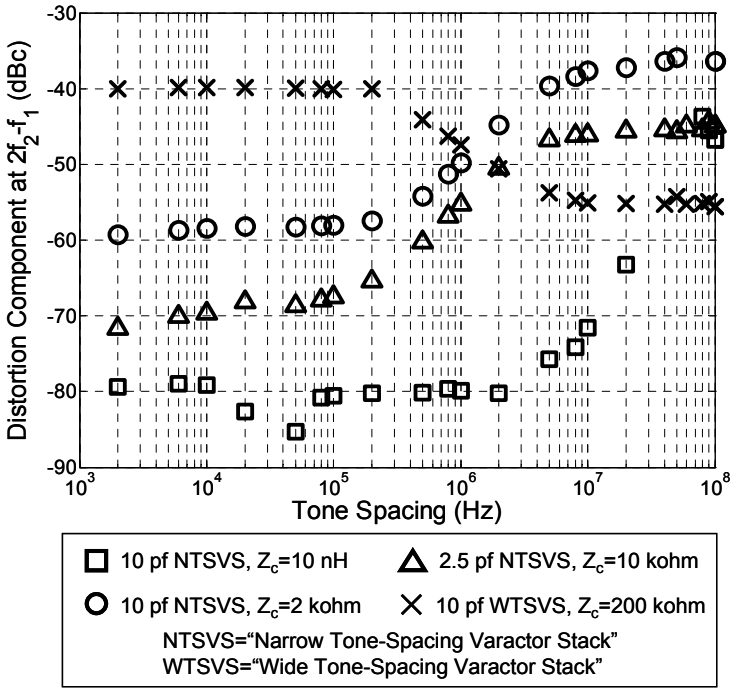


Fig. 5.31. Measured distortion component at $2f_2$-f_1 as function of tone spacing at a power level of 20 dBm (for all cases: f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

5.5 Conclusions

This chapter has discussed the technology implementation issues and offered the experimental verification of the previously proposed varactor configurations.

The narrow tone-spacing varactor stack using the low-voltage varactor diodes has been first implemented with our in-house DIMES silicon-on-glass technology. The measurements provide experimental evidence for the predicted IM_3 cancellation and indicate a superior linearity for modulated signals up to 10 MHz bandwidth.

Two highly linear varactor configurations using high-voltage varactor diodes have been successfully implemented in a single silicon-on-glass process technology. When considering their linearity versus tone spacing, the wide tone-spacing varactor stack and the narrow tone-spacing varactor stack designs offer complementary linearity behavior, with the wide tone-spacing varactor stack performing best with wide tone-spacing and the narrow tone-spacing varactor stack performing best with narrow tone spacing. This makes them very suitable to handle the different requirements of adaptive

receivers and transmitters in a single varactor technology. Due to the almost perfect control of the doping profile and ohmic contacts, a close to ideal exponential $C(V_R)$ relation and quality factor were realized. This accurate $C(V_R)$ behavior yielded a measured linearity performance of $OIP_3 > 56$ dBm for the wide tone-spacing varactor stack and $OIP_3 > 57$ dBm for the narrow tone-spacing varactor stack, which is compatible with the requirements of most demanding wireless applications. Their usability in practical circuit conditions was demonstrated through source-pull simulations and measurements, illustrating that high linearity can be maintained in all cases. The multi-stack topology is used to further improve the IM_5 dominated linearity and power handling of the narrow tone-spacing varactor stack without seriously degrading the quality factor, while capacitance tuning range and control voltage remain unchanged. Due to its IM_5 dominated nonlinearity, the use of the narrow tone-spacing varactor stack multi-stack topology yields a dramatic linearity improvement, which is double of that found in IM_3 dominated devices. The experimental data confirm this, yielding a record high linearity for continuously tunable capacitances regardless of the technology of implementation.

Finally, the proposed varactor topologies are implemented with a pre-industrial GaAs process technology. Once again, it demonstrates the predicted IM_3 cancellation and the complmentarty linearity behavior of narrow tone-spaing varactor stack and wide tone-spacing varactor stack, which confirms that 2-D integration issues can be well addressed. Due to the use of high-mobility GaAs as the intrinsic material, a tuning range as large as 9:1 is achieved, associated with a reasonably high quality factor and linearity, which represents the state-of-the-art tuning range, quality factor and linearity characteristics performance among all existing continuously tunable elements. Although excellent results have been already achieved, these processes can be still further optimized for quality factor and leakage currents, something that will be also beneficial for the linearity.

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Chapter 6

Antenna Mismatch Correction for Mobile Handsets

6.1 Introduction

The antenna input impedance is one of the most variable parameters for mobile handsets, where the environment and the presence of human bodies change its value continuously. For conventional handset transmitter implementations, the effective antenna impedance is supposed to have a nominal value of 50 Ω when the antenna is in the free-space operation without any objects around. However, when the handset is operated close to a metal object or in close proximity to the human body, the effective antenna impedance will vary over a wide impedance range [1]-[5]. When the input impedance varies, there is a mismatch between the power amplifier module and the antenna, with two major effects. First, the power amplifier will not perform at optimal efficiency under load variations, and, second, the radiated power decreases due to the reflected power [6]. This will result in an increase in the energy consumption (i.e., decreased battery endurance) or transmission quality deterioration, increased distortion, and in the worst case, the raised voltage due to the high standing wave amplitude caused by antenna mismatch may damage the power transistors in the output stage.

To overcome these difficulties and to meet the handset specifications, an isolator can be inserted at the output of the amplifier, which provides constant loading for the power amplifier. Also it is common technique to over dimension the transmitting stage and add protection circuitry to the power amplifier [7], [8]. However, it is obvious that these approaches will only limit the impact of antenna impedance variations and do not correct for them, which leads to increased attenuation and thus reduced efficiency. The

resulting output power may significantly lower the signal strength and cause call drops [7]. In view of this, a tunable impedance matching network, which corrects for the varying antenna impedance would be ideal, since it would enable high-efficiency and high output power of the transmitting stage at all times. To address this need, implementations of tunable matching networks have been proposed using silicon-on-sapphire (SOS) [9], RF-MEMS [10]-[12], CMOS [13] or p-i-n [14] switches, thin-film barium strontium titanate (BST) tunable capacitors [15] and varactor diodes [6], [16], [17]. Among them, the SOS and MEMS switch based networks provide better performance than the other solutions in terms of linearity and loss, which are regarded as most essential parameters for such correction networks. However, due to their switched nature, only a limited set of antenna mismatch conditions can be compensated, while in practical situations the antenna impedance can vary over a very wide range [1]-[6]. For example, to perform testing for antenna mismatch, industry uses a voltage standing wave ratio (*VSWR*) of 10:1 to mimic the most severe mismatch conditions, a value that corresponds with reflection coefficient magnitude of 0.818 [$|\Gamma_L| = (VSWR-1)/(VSWR+1)$], where the phase of Γ_L can vary from 0^o to 360^o. Note that this leads to almost full coverage of the Smith-chart, making it difficult to address with a switched approach since a lot of switching stages are required, and this is especially true in multi-band and multi-mode applications. Furthermore, practical experiences suggest that even when the switching can be close to ideal through the use of a large bank, the loss of the interconnection to these switches will be problematic. In view of this, a continuously tunable network based on the narrow tone-spacing varactor stack can provide a better Smith-chart coverage. While reducing the constraints on the metal interconnection, such "whole Smith-chart" corrections would significantly relax the design of the antenna and the rest of the transmitter path, facilitating shorter time to market.

This chapter is organized as follows. In Section 6.2, the antenna mismatch issues are first considered in general. Second, in Section 6.3, the method to evaluate the adaptive matching network is introduced. Two narrow tone-spacing varactor stack-based adaptive networks are designed and their performance are evaluated accordingly in terms of loss, impedance correction capability and linearity. The introduced network configurations can handle the antenna mismatch conditions with a *VSWR* larger than 10, independent of phase for an output power of 1 W, under different RF operation frequencies, which is readily to fulfill strict requirement of the next generation handset, featuring multi-band multi-mode operation. Third, in Section 6.4, it proves that the designed networks are also suitable for load-line adaptation of the power amplifier in the power back-off mode while properly correcting mismatched antenna impedance. Finally, we conclude this chapter in Section 6.6, along with a discussion from the architecture point of view in Section 6.5.

6.2 Antenna Mismatch Issues

6.2.1 Reduction of Efficiency and Output Power

For conventional handset transmitter implementations, the effective antenna impedance is supposed to have a nominal value of 50 Ω when the antenna is in free-space operation. For an ideal operation, as shown in Fig. 6.1 [18], through the impedance converting network, the purely resistive 50-Ω load at the antenna side is converted to R_{opt} at the output of the amplifier, where a shunt-connected parallel resonant circuit at the fundamental frequency is added to ensure a fundamental load resistor ($Z_{load}=R_{opt}$ at f_0) and a conceptual harmonic short ($Z_{load}=0$ at all other frequencies). Assume that the amplifier handles a maximum RF output power (P_{RF_max}) of 1 W and operates in Class-B mode. The corresponding value of the fundamental load resistor for a supply voltage of 3 V is

$$R_{opt} = \frac{V_{cc}^2}{2P_{RF\_\max}} = 4.5 \quad (\Omega). \tag{6.1}$$

Note that, to obtain the highest efficiency (78.5%) for this 1-W, 3-V Class-B amplifier, the maximum collector current (I_{c_max}) needs to be dimensioned accordingly such that

$$I_{c\_\max} = 2 \cdot I_{load}(f_0) = \frac{2V_{cc}}{R_{opt}} = 1.33 \quad (A), \tag{6.2}$$

where $I_{load}(f_0)$ is the fundamental current of the load (see Fig. 6.1).

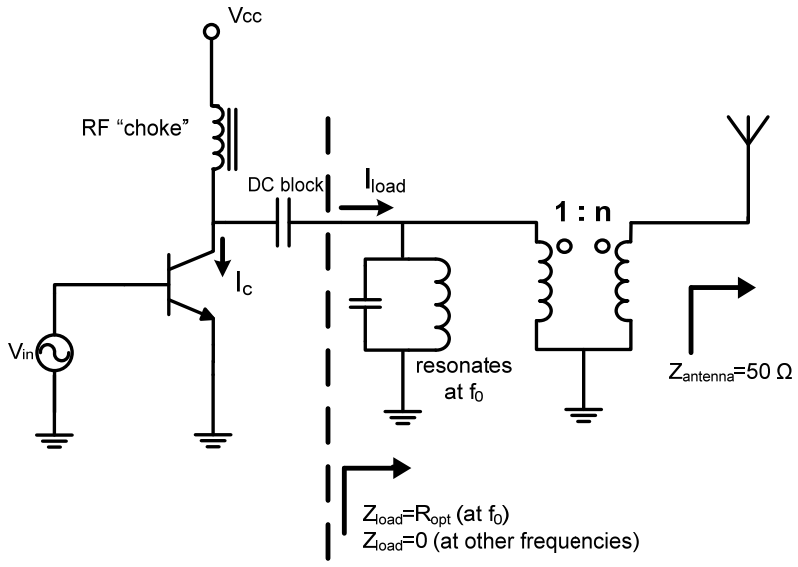
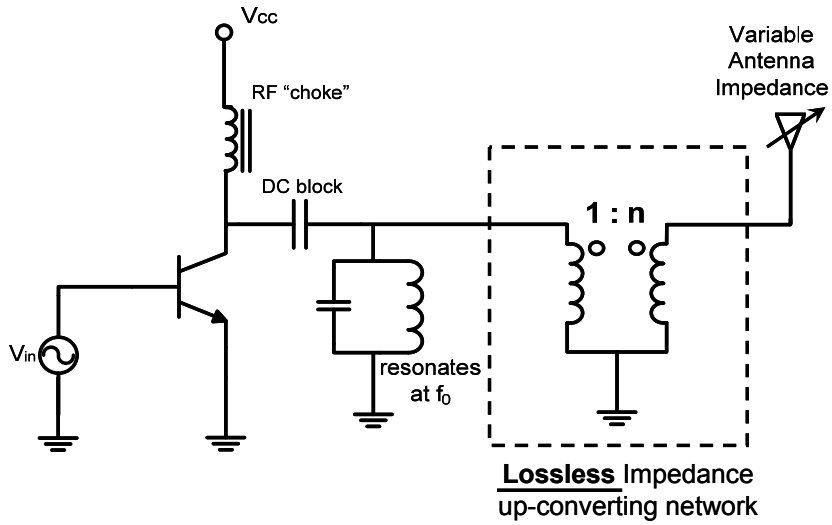


Fig. 6.1. General power amplifier model used for analysis [18].

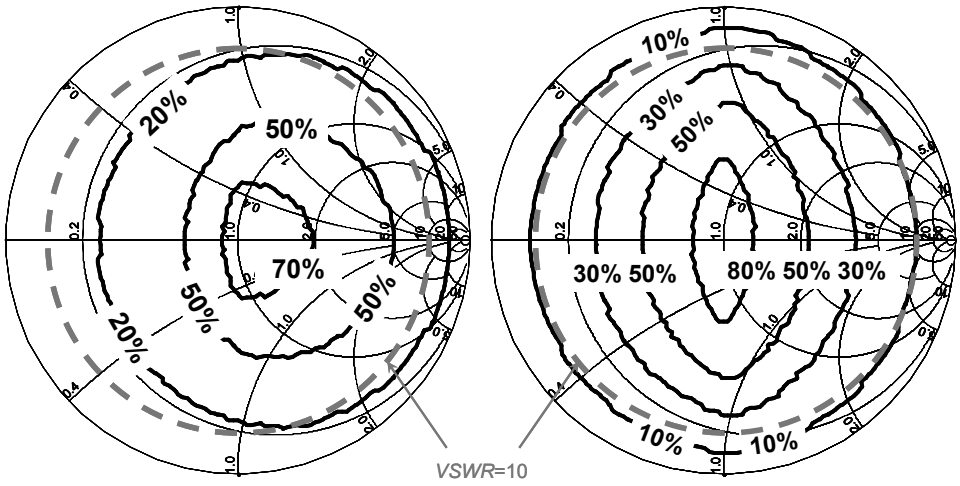
In the real world, antennas rarely present their nominal load to the power amplifier due to the uncontrollable surrounding environments, resulting in a reduced output power and efficiency of the power amplifier when the load differs from its optimal value.

In the case of the lower loading conditions ($|Z_{load}(f_0)| < R_{opt}$), the power device will swing over the full current range up to I_{c_max} which is typically limited by the active device, therefore the fundamental current that flows into the load remains constant in this operation regime. Due to the reduced voltage swing at the load, the output power and efficiency will degrade accordingly. This is normally called as current-limited regime [19]. On the other hand, in the case of higher loading conditions ($|Z_{load}(f_0)| > R_{opt}$), the output power and efficiency are limited by the voltage swing instead, therefore named as voltage-swing-limited regime [19], where the voltage swing on the load keeps at the maximum value, while the current swing decreases due to the higher loading impedance. This phenomenon is illustrated by plotting both the efficiency and output power contours in Smith-chart form with varying antenna impedance. As shown in Fig. 6.2, under severe mismatch conditions, e.g. *VSWR*=10, a value that corresponds with the reflection coefficient magnitude of $|\Gamma_L|$ = (*VSWR*-1)/(*VSWR*+1) = 0.818, the output power is reduced to 10% (10 dB less) of the maximum output power with the efficiency less than 20%.

In practice, the performance of power amplifier becomes even worse with the presence of loss from the impedance up-converting network. When this network is implemented off chip, e.g. making use of printed circuit board (PCB), the loss for an impedance conversion ratio of 11:1 (50 Ω to 4.5 Ω) can be normally controlled within 0.3 dB. However, it will reach 1 dB for on-chip implementations, where the quality factors of inductances are strongly restricted by the thickness of metal and the losses of substrate. With this in mind, we added a 1-dB attenuator in simulation to represent this loss. As plotted in Fig. 6.3, both efficiency and output power will be further reduced by 1 dB compared to the results of Fig. 6.2 when the loss of the up-converting network is taken into account. Since we aim for the on-chip correction for the antenna mismatch in this chapter, the results of Fig. 6.3 can be used as a benchmark, through which the correction capability of the adaptive network can be evaluated.



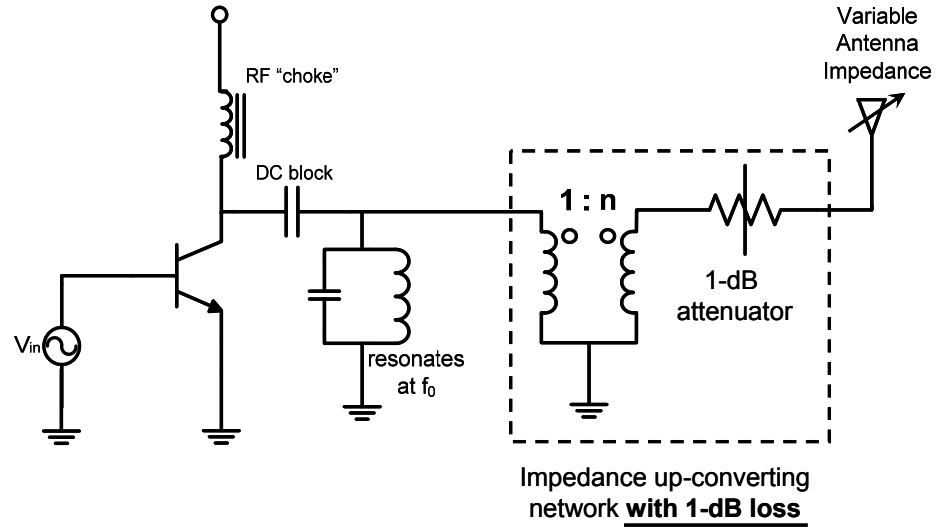
(a) Schematic for simulation



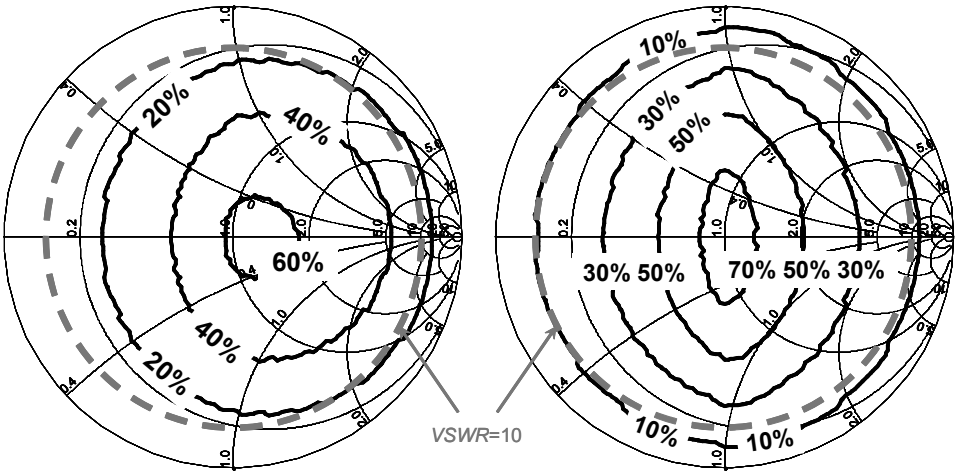
(b) Power efficiency contours

(c) Output power contours (in percentage of maximum output power under optimum load impedance)

Fig. 6.2. Efficiency and output power degradation due to antenna mismatch. (a) Schematic for simulation. Power efficiency (b) and output power (c) contours under mismatch conditions for Class-B operation with an ideal current-limited device (data is normalized to 50 Ω at the antenna side, the operating parameters of the active device are: V_{cc}=3 V, I_{c_max}=1.33 A and P_{RF_max}=1 W). Note that, in this simulation, an ideal lossless transformer with fixed impedance conversion ratio is used to convert the characteristic impedance from 50 Ω at the antenna side to 4.5 Ω at the output of power amplifier.



(a) Schematic for simulation



(b) Power efficiency contours

(c) Output power contours (in percentage of maximum output power under optimum load impedance)

Fig. 6.3. Efficiency and output power degradation due to antenna mismatch. (a) Schematic for simulation. Power efficiency (b) and output power (c) contours under mismatch conditions for Class-B operation with an ideal current-limited device (The parameters of the active device are same as Fig. 6.2). Note that a 1-dB attenuator is used in this simulation to represent the loss of the impedance up-converting network.

6.2.2 Linearity Degradation

The reduced output power and efficiency is accompanied by the linearity degradation of the power amplifier. To investigate this, we consider Fig. 6.4, where the linearization approach described in [20], [21] is followed.

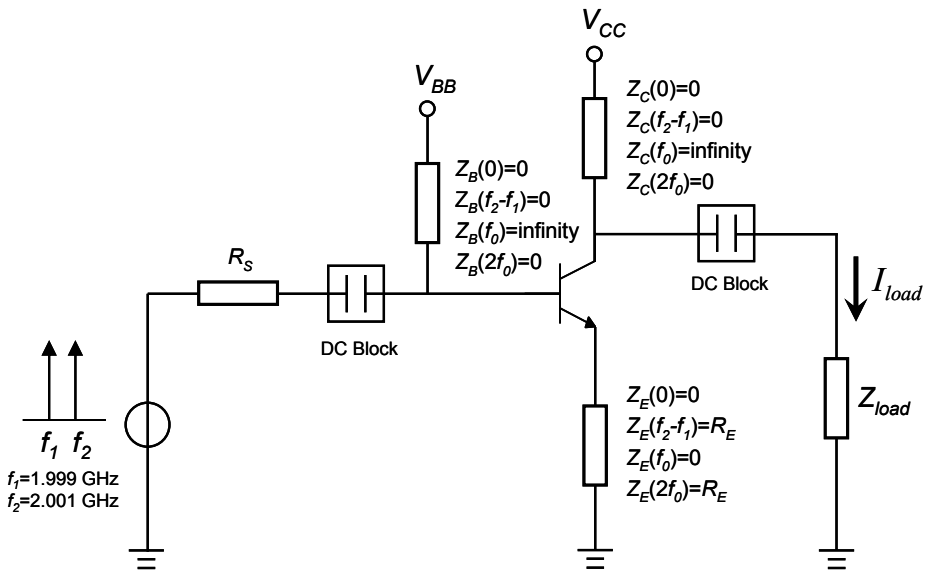


Fig. 6.4. Circuit Schematic of a basic common-emitter configuration with the emitter tuning at the even harmonics.

At the low-power levels the indirect IM_3 mixing term, originating from the secondary mixing between the fundamental and second-order distortion products, can be well controlled by making good use of proper terminations at the even harmonic frequencies as defined in Fig. 6.4. Consequently, this indirect mixing product can be used to cancel out the direct IM_3 mixing product of the bipolar device, yielding a significant improvement on linearity. This is visualized in Fig. 6.5(a) by plotting the output power at f_2 and $2f_2$-f_1 as a function of the input power for a two-tone test. It can be observed that an improvement of > 15 dB in IM_3 is obtained over a wide range of output powers (-20 dBm to 10 dBm) by setting

$$R_E \approx \frac{1}{2g_m} = 3.5 \ \ (\Omega) \quad . \tag{6.3}$$

Although the enhancement in IM_3 is available up to the peak output power as shown in Fig. 6.5(a), this improvement becomes smaller with the increase of power level due to the non-negligible higher-order mixing products, e.g. the fifth-order distortion components (IM_5) that appear at the IM_3 frequecies ($2f_1$-f_2 and $2f_2$-f_1). To solve for this problem, it is possible to force IM_3 and IM_5 to have opposite signs at the high-power region, creating certain sweet spots for cancellation [21]. For convenience, we keep the harmonic terminations of Fig. 6.4 and sweep the emitter resistance (R_E) at even harmonics for optimizing these IM_3 sweet spots. As depicted in Fig. 6.5(a), when setting R_E to 0.5 Ω, IM_3 and IM_5 cancellation occurs very close to the 1 dB compression, which is a beneficial range when aiming for low distortion at high output power levels.

It is important to notice that the IM_3 and IM_5 cancellation solution is strongly power-level dependent, since the IM_3 and IM_5 products follow different power laws as the input voltage. This is fundamentally different from the out-of-band IM_3 cancellation solution at the low-power level, where the transfer function [$H_3(f_2, f_2, -f_1)$] is forced to 0, and therefore it is principally power level independent when only IM_3 (both direct and indirect) are in play. It is this difference that determines their distinguished behaviors under antenna mismatch conditions. As visualized in Fig. 6.5(b), when the output loading impedance increases to 45 Ω due to the antenna mismatch, the out-of-band IM_3 cancellation solution for the low power levels is still valid up to the voltage-clipping point (P_{out}=12 dBm), while the IM_3 and IM_5 cancellation phenomenon doesn't occur at the range close to the clipping point. In other words, the desired linearity improvement at the high-power region is not available under the mismatched conditions. To solve for this, one needs to correct the mismatched impedance back to the optimum value ($Z_{load} = R_{opt} = 4.5 \ \ \Omega$) making use of the adaptive matching network. By doing this, the harmonic terminations of the power amplifier stage are kept unchanged and accordingly the expected linearity enhancement is restored. With this in mind, we will concentrate on the linearity issues of the adaptive matching network in the rest of this chapter, while assuming the optimum linearity performance of the power amplifier.

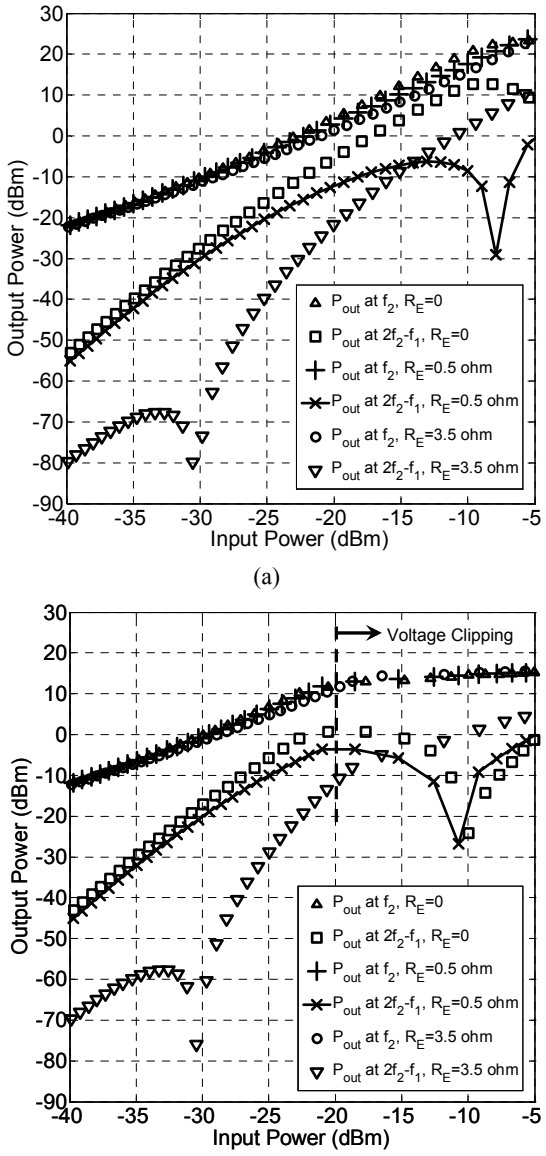


Fig. 6.5. Simulated output power at the fundamental and IM_3 frequencies versus the input power using the circuit schematic of Fig. 6.4. (a) Matched condition ($Z_{load} = R_{opt} = 4.5\ \Omega$). Out-of-band IM_3 cancellation approach is used to improve the linearity at low power level by setting $R_E = 3.5\ \Omega$, while the linearity at high power level is enhanced through the IM_3 and IM_5 cancellation by setting $R_E = 0.5\ \Omega$. (b) Severe mismatched condition ($Z_{load} = R_{opt} = 45\ \Omega$). Note that, for this case, the 1-dB compression point of the output power is around 12 dBm.

6.3 Design of the Adaptive Matching Network

6.3.1 Performance Evaluation of the Adaptive Matching Network

To correct the mismatched impedance to the desired optimum value, an adaptive matching network can be inserted between the output of the power amplifier and the antenna as shown in Fig. 6.6. However, in practice, such a network is generally associated with loss, which in turn will reduce the output power and efficiency. To investigate the impedance correction capability of the network in a systematic way, the S-matrix as depicted in Fig. 6.6 can be utilized. For this purpose we assume 50 ohm port impedance at the antenna side, while a characteristic port impedance at the output stage is used, which is equal to the optimum loading resistance R_{opt}. By now assuming that Γ_{Lstage}=0 (see Fig. 6.6), the antenna mismatch conditions that the network is able to correct can be calculated as

$$\Gamma_{\mathrm{L}} = \frac{S_{11}}{S_{11}S_{22} - S_{12}S_{21}}, \tag{6.4}$$

where Γ_L is the reflection coefficient at the antenna side (see Fig. 6.6). Note that, with this assumption (Γ_{Lstage}=0), the power amplifier will be always loaded by optimum resistance (R_{opt}), and therefore it remains maximum efficiency, optimum output power and linearity. The actual power delivered to the antenna and the total efficiency will be solely dependent on the network losses and the reflection at the antenna side. These two factors can be together evaluated by the operating power gain (G_p), which can be correspondingly written as

$$G_P = \left(\frac{1}{1-\left|\Gamma_{Lstage}\right|^2}\right)\left|S_{21}\right|^2\left(\frac{1-\left|\Gamma_L\right|^2}{\left|1-S_{22}\Gamma_L\right|^2}\right) = \left|S_{21}\right|^2\left(\frac{1-\left|\Gamma_L\right|^2}{\left|1-S_{22}\Gamma_L\right|^2}\right). \tag{6.5}$$

In summary, (6.4) investigates the mismatch conditions that can be corrected to the desired value and (6.5) calculates the corresponding losses, while the linearity can be evaluated with a standard way as the normal networks since the linearity of the power amplifier remains in principle unchanged when the antenna mismatch correction is fully functional.

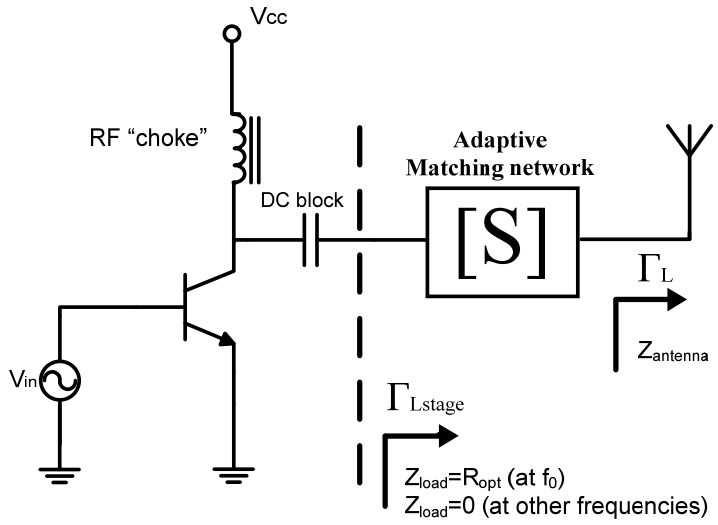


Fig. 6.6. Schematic of Class-B power amplifier with the adaptive network for antenna mismatch correction. The adaptive network is simplified as a two-port black box, whose S parameters are used to evaluate the network's impedance correction capability and the corresponding losses.

6.3.2 LC Resonators based Π-section Network

In order to achieve the desired impedance correction, we choose an LC resonators based Π-section network as shown in Fig. 6.7. This is motivated by the combination of low circuit complexity while providing a large mismatch correction region on the Smith chart. Note that under certain resonance condition, one of shunt LC resonators can be regarded as an open circuit and therefore the Π network can act as an L-network in two directions (see Fig. 6.8), which facilitates the up- and down- conversion [19] of the mismatched impedance and makes it possible to increase the correction capability with a simple Π-section network. The varactors are based on the high-linearity narrow tone-spacing varactor stack, while we aim for a low-loss silicon-on-glass technology implementation. It must be stressed that the narrow tone-spacing varactor stack will behave only linear if the requirement for the center-tap impedance is met. For this reason, center-tap inductors (L_c) are used in combination with a carefully designed layout. Table X summarizes the performance parameters of narrow tone-spacing varactor stack used in the design. Since the adaptive correction network has to handle a reasonably high RF power (1 W has been used in our study), the effective tuning range of the varactors will be lowered due to the constraints of the forward bias and

breakdown of the individual diodes. For this reason, a conservative effective tuning range of 3 is assumed during the design. The loss of the network is mostly limited by the inductors of the LC tanks. To minimize this, the inductors are kept below 2 nH, which enable us to implement them with bond wires, providing higher quality factors. In our simulations, a conservative quality factor of 50 is used for the bond wires, although in practice it can easily exceed 100.

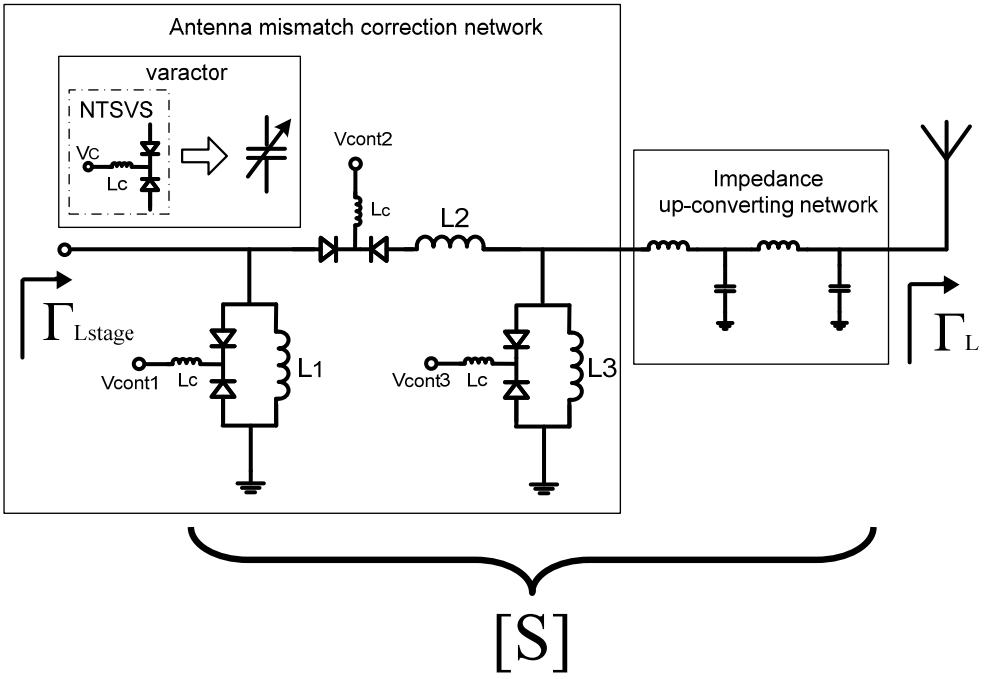


Fig. 6.7. Schematic of LC resonators based Π-section network.

Table X. Parameters of narrow tone-spacing varactor stack used in the LC Resonators based Π-section network

Average intrinsic Q	Maximum control voltage	Tuning range	OIP_3
100	20 V	6	> 60 dBm

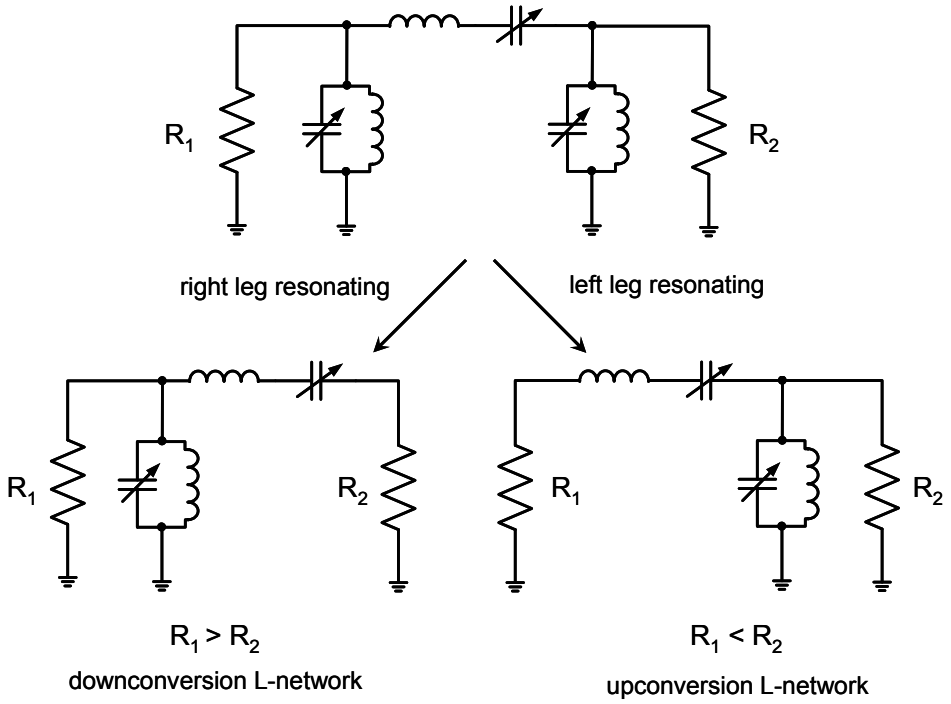


Fig. 6.8. Equivalent circuits when one of the leg in the Π-section resonates out.

Fig. 6.9 shows the ADS simulated constant contours of the operating power gain (G_P) of the network at 1.8 GHz, 2 GHz and 2.2 GHz. It can be observed that the achieved mismatch correction region on the Smith chart is very large while providing a relatively high operation power gain, which illustrates the high correction capability of the designed adaptive matching network. Note that the fixed on-chip matching networks for the impedance conversion, like the transformer in Fig. 6.1 and the second stage in Fig. 6.7, are normally responsible for 1 dB loss. With this taken into account, the added loss arising from the adaptive correction network (the first stage in Fig. 6.7) is less than 3 dB for a *VSWR* as high as 10.

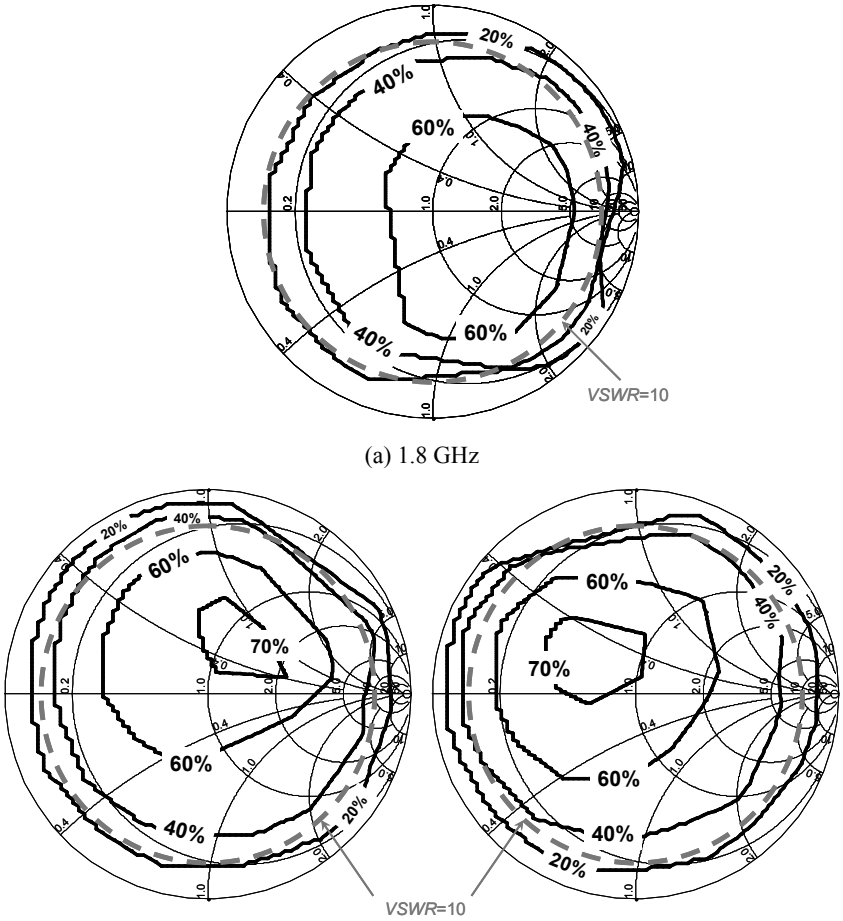
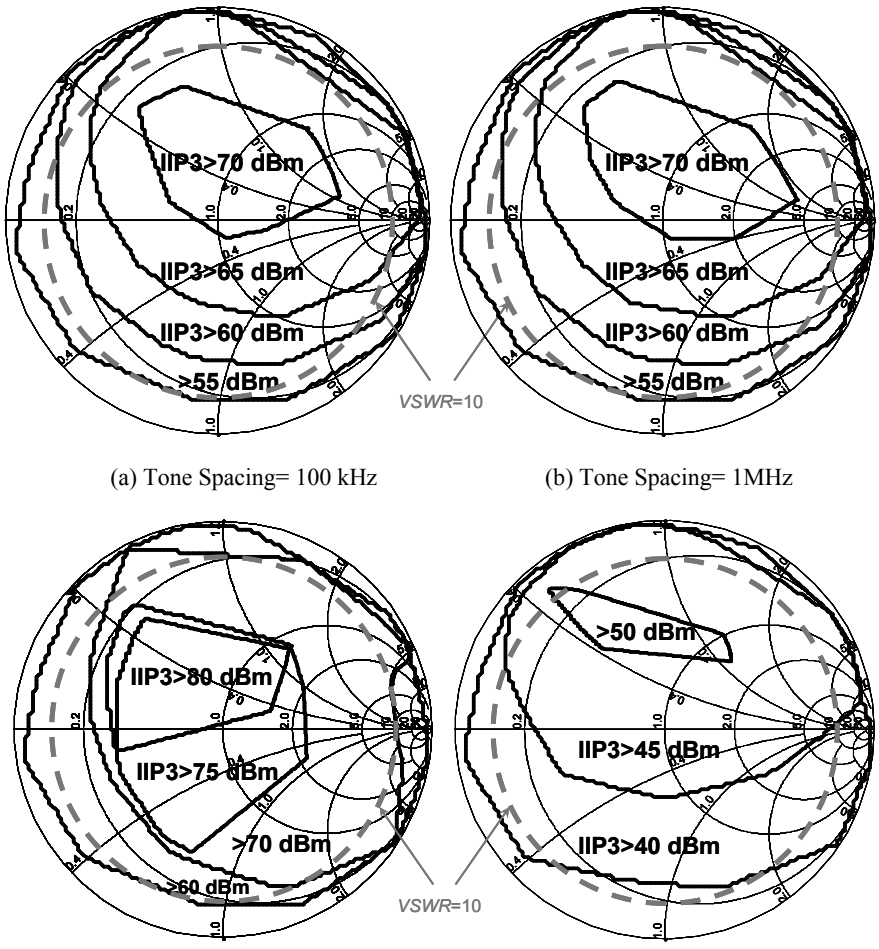


Fig. 6.9. Simulated contours of the constant operating power gain (G_P) of the LC resonators based Π-section network at 1.8GHz, 2 GHz and 2.2 GHz.

The linearity of the network is simulated using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing and mismatch loading condition at the output, while the input power of each tone is kept as 27 dBm. Fig. 6.10 plots constant IIP_3 contours for different tone spacings on the Smith-chart of output loading plane (Γ_L), where the achievable IIP_3 at variant loading conditions are visualized. The simulated IIP_3 for a *VSWR* of 10 is typically better than 60 dBm up to 10 MHz bandwidth, which is negligible compared to the nonlinearity of the power amplifier and sufficient for many communication standards. It should be stressed that a similar linearity performance is

achievable for the center frequency (f_{center}) of 1.8 GHz and 2.2 GHz as well, making this network suitable for multi-mode applications.



(a) Tone Spacing= 100 kHz (b) Tone Spacing= 1MHz

(c) Tone Spacing= 10 MHz (d) Tone Spacing= 100 MHz

Fig. 6.10. Simulated constant IIP_3 contours for different tone spacings on the Smith-chart of output loading plane (Γ_L). The achievable IIP_3 values for different loading conditions are marked on the figure.

The final layout of the LC Resonators based Π-section correction network is shown in Fig. 6.11. It can be found that the first stage is quite compact due to its low characteristic impedance and the impedance up-converting network takes most of the chip area. It is possible to combine these two stages by making use of the transformer for the impedance conversion, which will be introduced in the next section.

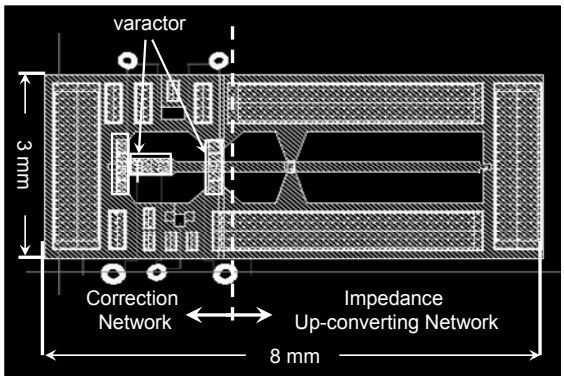


Fig. 6.11. The final layout of the LC resonators based Π-section network.

6.3.3 Capacitive Quad based Network

As done above, we assume a characteristic port impedance of 50 Ω at the antenna side (Z_L in Fig. 6.12) and 4.5 Ω at the output stage of the power amplifier, which is equal to the optimum loading resistance R_{opt}. A transformer, instead of a fixed L-network, is first used to convert the characteristic impedance level to roughly 15 Ω, and the capacitive quad based network will continue to correct the mismatched impedance back to R_{opt} (4.5 Ω) as shown in Fig. 6.12. This solution is easy to implement and compact since it avoids the use of bondwire inductors and bulky L-network. The capacitive quad based network provides much more resonance combinations, which significantly increase the Smith-chart coverage even for a characteristic impedance ratio of about 3 (4.5 Ω at the input and 15 Ω before the transformer). In order to optimize the quality factor of the transformer, the values of L_2 and L_3 are chosen similar, facilitating the improvement of the coupling factor during layout. The final layout is shown in Fig. 6.13 and the resulting chip area is 2.9 mm by 3.4 mm, which is much smaller than the foregoing LC resonators based Π-section network.

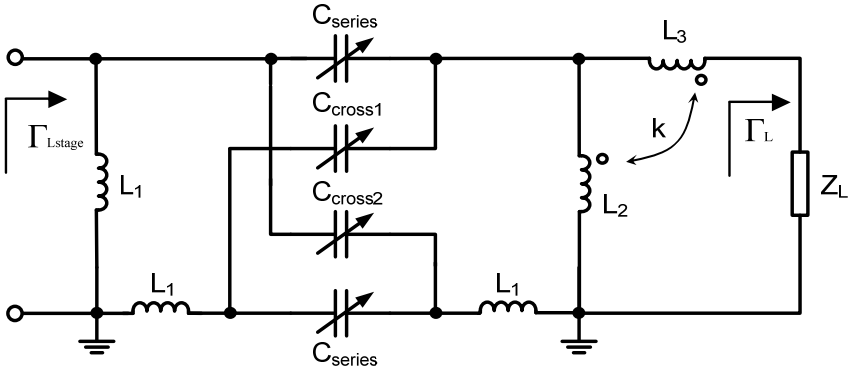


Fig. 6.12. Schematic of capacitive quad based network.

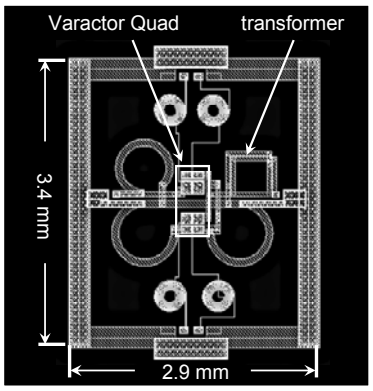
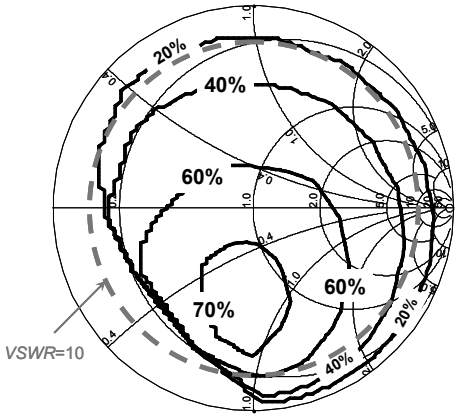
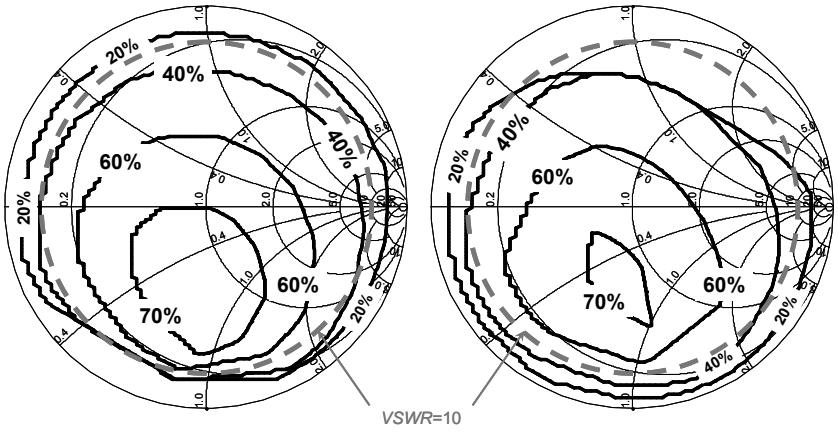


Fig. 6.13. The final layout of capacitive quad based network.



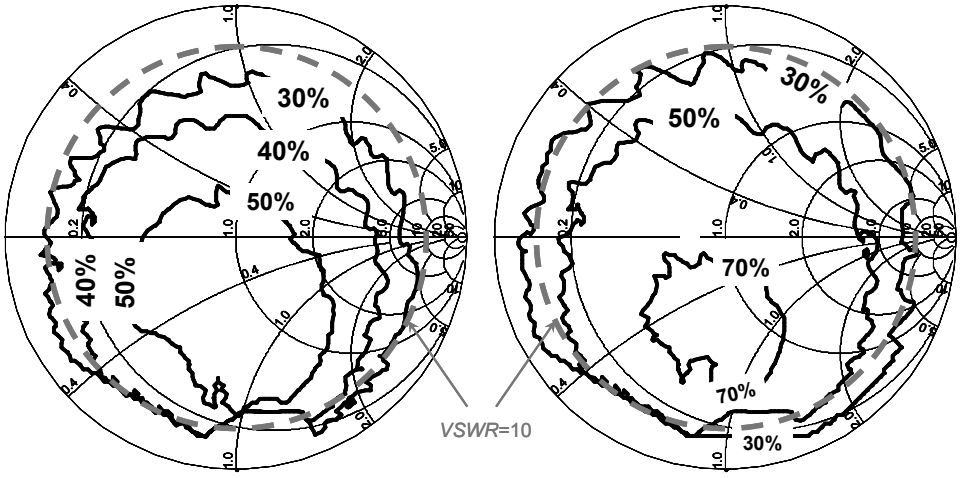
(a) 1.8 GHz



(b) 2 GHz (c) 2.2 GHz

Fig. 6.14. Simulated contours of the constant operating power gain (G_P) of the capacitive quad based network at 1.8GHz, 2 GHz and 2.2 GHz.

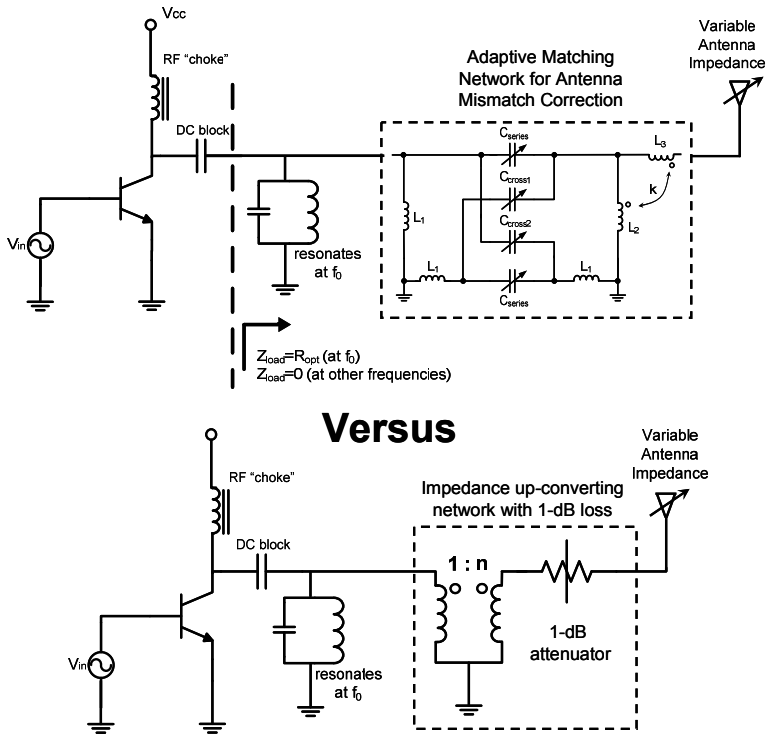
Fig. 6.14 shows the ADS simulated contours of the constant operating power gain (G_P) of the designed network at 1.8 GHz, 2 GHz and 2.2 GHz and a comparable performance is achieved as that of the LC resonators based Π-section network. It needs to be stressed that although the efficiency and output power of the power amplifier stage itself (the first stage of Fig. 6.6) remains fixed to its optimum with the aid of the adaptive network, the added losses of this inserted correction network will reduce the efficiency and the transmitted power as well. To investigate this point, we make use of the designed network in the schematic of Fig. 6.6 and simulate the overall efficiency and the transmitted power at the antenna side. As depicted in Fig. 6.15, the overall efficiency and output power will be > 30% for the most severe mismatch conditions. It is worthwhile to compare the result of Fig. 6.15 (overall efficiency and output power after correction with the loss of adaptive network taken into account) with that of Fig. 6.3 (reduced efficiency and output power due to the antenna mismatch and the loss of the impedance up-converting network) to check the performance improvements achieved through the designed network. As illustrated by the shadowed area in Fig. 6.16, the loss of the inserted network is mostly compensated by the improved efficiency and output power, indicating a very effective correction capability of the designed network.



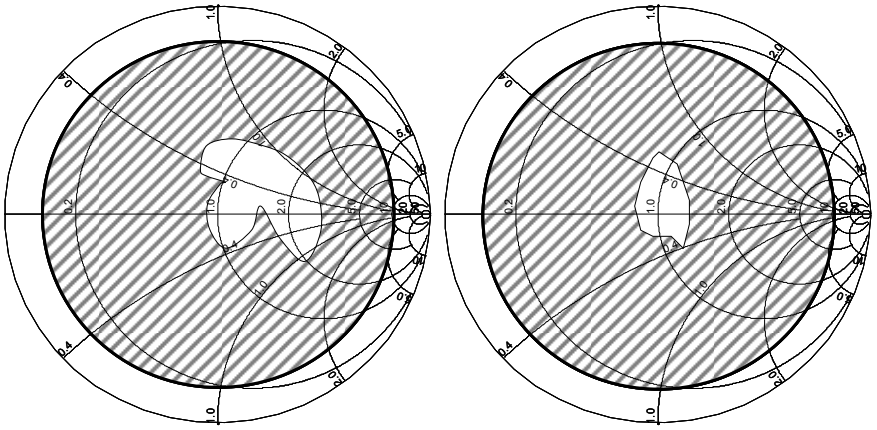
(a) Overall power efficiency contours

(b) Overall transmitted power contours (in percentage of maximum output power under optimum load impedance)

Fig. 6.15. Overall power efficiency (a) and transmitted power (b) contours making use of the designed network in the schematic of Fig. 6.6 (the transistor model is same as Fig. 6.2; the characteristic impedance of 50 Ω at the antenna side is used, V_{cc}=3 V, I_{c_max}=1.33 A and P_{RF_max}=1 W).



(a) Schematics used for comparison



(b) Efficiency comparison (c) Output power comparison

Fig. 6.16. Comparison results between Fig. 6.15 (overall efficiency and output power after correction with the loss of adaptive network taken into account) and Fig. 6.3 (reduced efficiency and output power due to the antenna mismatch and the loss of the impedance up-converting network) to check the performance improvement due to the adaptive correction network. The area, where the efficiency and output power are improved due to the designed network, is shadowed.

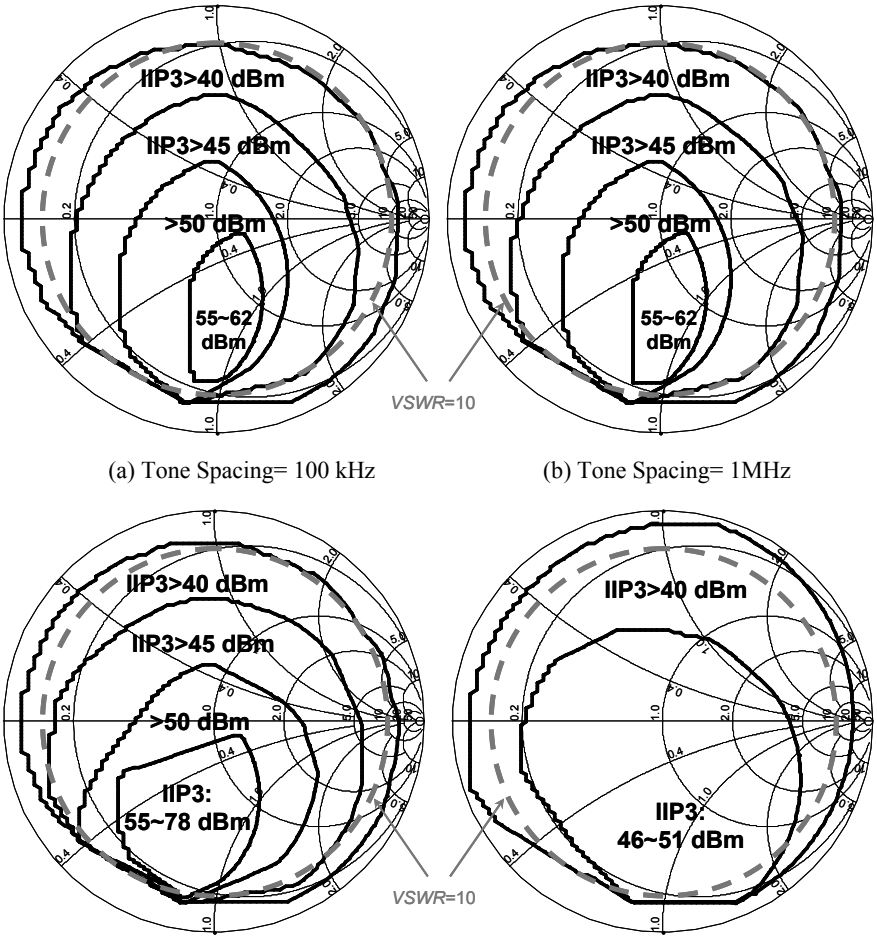


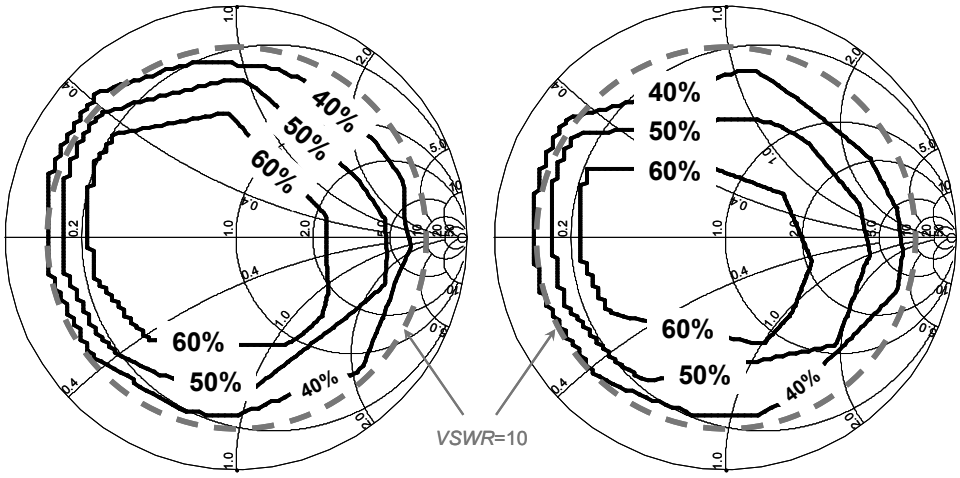
Fig. 6.17. Simulated constant IIP_3 contours for different tone spacings on the Smith-chart of output loading plane (Γ_L). The achievable IIP_3 values for different loading conditions are marked on the figure.

The linearity of the network is simulated using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing and mismatch loading condition at the output, while the input power of each tone is kept as 27 dBm. Fig. 6.17 plots constant IIP_3 contours for different tone spacings on the Smith-chart of output loading plane (Γ_L). The simulated IIP_3 for a *VSWR* of 10 is typically better than 45 dBm up to 100 MHz bandwidth. Although the linearity is worse than the previous version due to more the more complex resonance combinations, it is still negligible compared to the nonlinearity of

the power amplifier. In practice, stacking of the varactors can be used to further improve the linearity. Note that stacking of narrow tone-spacing varactor stacks is very efficient in IM_3-free systems, i.e., $40logN$ improvement in IIP_3 for N-stacked narrow tone-spacing varactor stack, as explained in Chapter 4.

6.4 Load-line Adaptation

In traditional amplifier implementations, the linearity requirement typically results in the use of class-AB operation for the output stage [18], which provides a workable compromise between linearity and efficiency. When considering linearity, the class-AB output stage must be dimensioned in such a way that it can provide its peak output power without saturation. As defined in (6.1), assuming the peak output power (P_{RF_max}) of 1 W and the battery voltage (V_{cc}) of 3 V, the optimum load impedance (R_{opt}) for a class-AB stage at the fundamental frequency is fixed to 4.5 Ω [22].



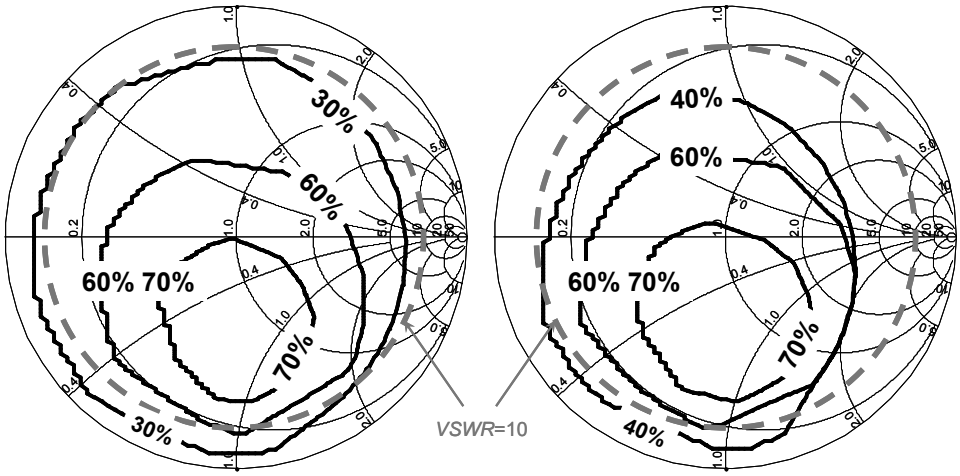
(a) R_{opt}=6.5 Ω, P_{RF_max}=0.7 W (1.5 dB back-off)

(b) R_{opt}=9 Ω, P_{RF_max}=0.5 W (3dB back-off)

Fig. 6.18. Simulated contours of the constant operating power gain (G_P) of the LC resonators based Π-section network 2 GHz for different values of R_{opt} (V_{cc} = 3 V).

Unfortunately, class-AB operation provides its highest efficiency only under maximum drive conditions. When operated at the required back-off level, due to linearity reasons for a given communication standard like (W)CDMA, a rather dramatic loss in efficiency occurs [23]. To address this problem, dynamic load-line

adjustment as a function of output power, using a reconfigurable output matching network is regarded as one of the best solutions in terms of cost and complexity [7], [22]. In view of this, the adaptive networks designed in this chapter are potentially useful for this function as well. For testing this potential, the characteristic port impedance at the output stage of the power amplifier are now set to 6.5 Ω and 9 Ω, which correspond to the optimum load impedance for 1.5 dB and 3 dB back-off conditions respectively. Fig. 6.18 and 6.19 plot the ADS-simulated contours of the constant operating power gain (G_P) of the designed networks at 2 GHz. It shows that the Smith-chart coverage and operating power gain will not degrade for different R_{opt}, indicating that the designed networks can serve not only for antenna mismatch correction but also for the load-line adaptation of the power amplifier in the back-off mode.



(a) R_{opt}=6.5 Ω, P_{RF_max}=0.7 W (1.5 dB back-off)

(b) R_{opt}=9 Ω, P_{RF_max}=0.5 W (3dB back-off)

Fig. 6.19. Simulated contours of the constant operating power gain (G_P) of the capacitive quad based network 2 GHz for different values of R_{opt} (V_{cc} = 3 V).

6.5 Locations to Place the Adaptive Network

It is worthwhile to mention that the adaptive network can be alternatively placed inside the antenna or close to feedpoint as shown in Fig. 6.20.

The first alternative is to place the antenna mismatch correction network inside the antenna [18]. This idea is originally applied to adjust the resonance frequency or bandwidth of the antenna for multi-band applications making use of a single varactor

[24]-[26] or a simple matching network [27]. In light of this, it is also possible to integrate an adaptive antenna mismatch correction network with whole Smith-chart coverage inside the antenna, allowing the band switching as well as the impedance correction in the meanwhile.

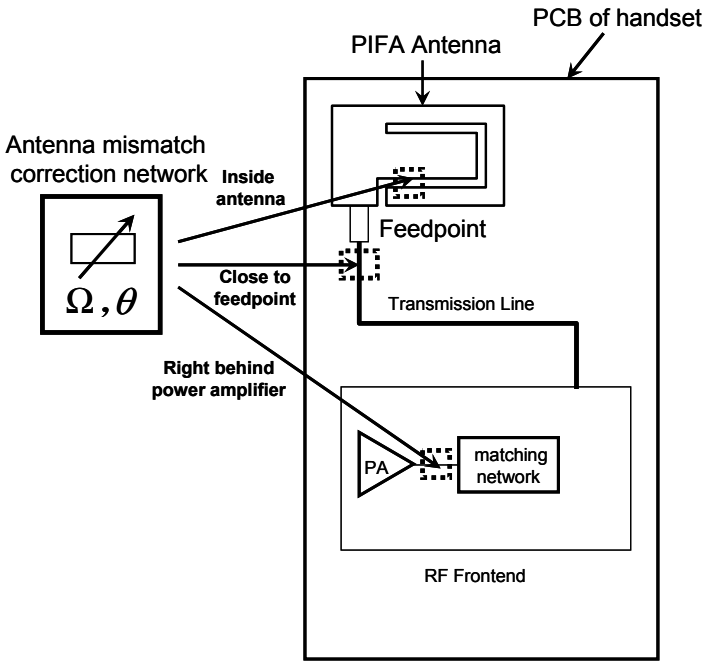


Fig. 6.20. Top view of handset's PCB. Alternative positions to place an antenna mismatch correction network inside the conventional mobile handset.

In practice, cares should be taken to choose a position with low characteristic impedance to place such a network, relaxing the requirement of the tunable component in terms of voltage handling capability. Note that an adaptive network with the whole "Smith-chart" coverage will make the design difficult due to the inevitable series resonance conditions. In addition, with the tremendous demand of antennas with high efficiencies in very small form factors that fit inside ever-shrinking portable wireless devices [14], the size of the adaptive network is strongly restricted. In view of this, varactors with low capacitance density will not qualify since the dimension of the adaptive network becomes essential. Finally, the design of the antenna has to be accompanied with the adaptive network, which suggests an extension of the design period and accordingly the time to market.

When placing a network close to the feedpoint, one may have a separate and independent general module for different kinds of the antenna, making the design of the adaptive network, antenna and RF frontend orthogonal and significantly relaxing the design of the antenna and other RF building blocks. However, the fact that the characteristic impedance is around 50 Ω near the feedpoint will place a challenge on the tunable components' voltage handling capability. For this reason, some of the current implementations making use of MEMS elements are only able to compensate imaginary part of the antenna impedance [11], [12] and those using SOS switches choose a *VSWR* of 7:1 [9]. Although according to [2], the mismatch of antenna impedance mainly locates at the upper part of the Smith-chart and these solutions seem enough, experiments [6] show that even severe events may be met in practice, which is especially true in multi-band and multi-mode applications. In addition, with the trend of integrating the GPS within the cellular phone, the mobile handset is usually placed near the windscreen of the vehicle. In this circumstance, the antenna is used in extreme proximity to the glass, instead of hand, finger or head as modeled in [2], and the resulting antenna characteristics can be differently affected. In view of this, placing an adaptive network with whole Smith-chart coverage at the stage with relatively low characteristic impedance seems to be the automatic choice. With this in mind, we place the adaptive network right behind the power amplifier, where the port characteristic impedance is normally 10 times smaller. This avoids unnecessary high RF voltages over the varactors and allows more series and shunt resonator to be used in the design, yielding to a larger Smith-chart coverage. In the meanwhile, low characteristic impedance suggests smaller inductance and bigger capacitance to be used, which helps to decrease the total dimension of the network.

6.6 Conclusions

The work demonstrated in this chapter is focused on efficiency enhancement of the power amplifier in presence of antenna mismatch. Using a varactor-based approach, high-linearity adaptive matching networks, capable of correcting the antenna mismatch with the *VSWR* of 10 over the whole Smith-chart, are presented. For all these conditions, an optimum loading for a power level between 0.5 W and 1 W is offered to the power amplifier stage along with a relatively high operating power gain. This "whole Smith-chart" solution will ease the design of the RF frontend and antennas yielding a significantly reduction in the time-to-market of mobile phones.

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Chapter 7

A Varactor-Based Amplitude and Phase Modulator

7.1 Introduction

Amplitude modulators and phase shifters are essential building blocks for many measurement and communication / radar systems. Examples include phased-array antennas, active load-pull systems etc. In general, these blocks need to provide good tuning capabilities, while providing very low distortion and acceptable losses. In view of this, the low-distortion varactors, as proposed in the previous chapters, are logic candidates for the tuning elements due to their merits in tuning range, losses and linearity.

In support of this, in Section 7.2 a novel amplitude modulator configuration is proposed that yields no significant AM-PM distortion, a very important feature when controlling the envelope power of complex modulated signals. The proposed circuit enables a transfer function (s_{21}), which can be continuously tuned along the imaginary axis between $-j$ and j, while providing purely ohmic loading impedance to the driving stage.

In Section 7.3, a transmission line based true-time-delay 180° phase shifter is designed, which can facilitate phase diversity systems.

When combining the upper amplitude and phase modulator in a single circuit, full amplitude and phase control is achieved with superior linearity ($IIP_3 \sim 50$ dBm). The proposed techniques can be utilized to introduce a new class of low-distortion, low-loss RF circuits that can serve various applications. To demonstrate the above, in Section 7.4 a polar modulator is introduced, based on these principles, which can considerably simplify the traditional transmitter architecture, while still being able to generate any

desired complex modulated signal. By controlling the transfer function of the polar modulator in a careful time-variant way, we can obtain the constellation diagram of choice, according to the requirements of the communication standard under consideration. In Section 7.5, experimental results are provided to support the theory. Finally, we conclude this chapter in Section 7.6.

7.2 Differential Varactor Amplitude Modulator (DVAM)

The differential varactor-based amplitude modulator is based on the combination of direct and cross wise connected capacitive coupling of the input and output as shown in Fig. 7.1. The principle of this configuration is based on the fact that the displacements currents through the directly connected capacitors are in opposite phase with those of the cross coupled capacitor pair. When the circuit is driven differentially and all the capacitive elements have the same value, the capacitive currents will cancel, yielding a perfect isolation between input and output. By varying the value of the cross wise connected capacitors in respect to the direct connected capacitors, the displacement currents will not cancel and energy will be transferred from the differential input to output port and visa versa. By combining this capacitive quad with two shunt inductors and properly dimensioning the element values, some special properties can be achieved for this circuit configuration, which makes it attractive as amplitude modulator in RF applications.

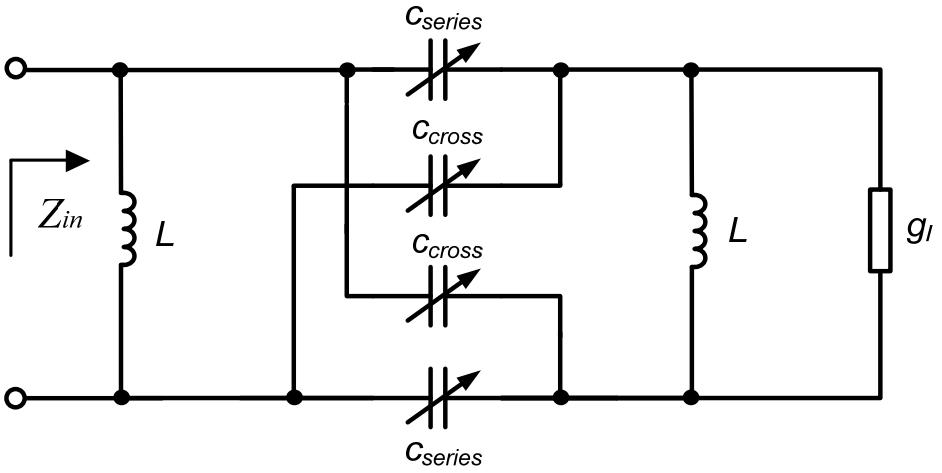


Fig. 7.1. Schematic of the capacitive amplitude modulator.

The unique behavior of this circuit can be best studied by enforcing the input impedance to be resistive. The input impedance of this configuration is given by:

$$Z_{in} = \frac{(s^2 Lc_{series} + s^2 Lc_{cross} + 2g_l sL + 2)sL}{(2s^4 L^2 c_{series} c_{cross} + s^3 L^2 c_{series} g_l + 2s^2 Lc_{series} + s^3 L^2 c_{cross} g_l + 2s^2 Lc_{cross} + 2g_l sL + 2)} \tag{7.1}$$

Enforcing the imaginary part of Z_{in} to be zero yields the following relation for the series and cross connected capacitors

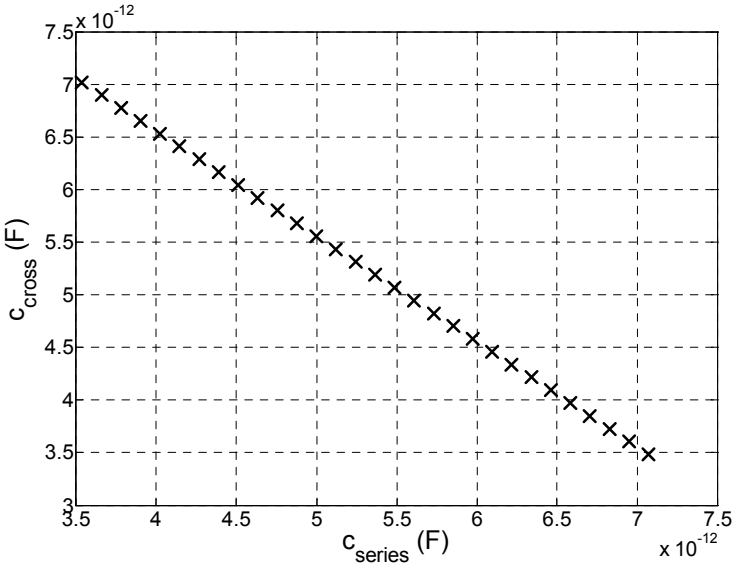
$$c_{cross} = \frac{-\omega^2 Lc_{series} + 2}{\omega^2 L} \quad \text{or} \quad c_{cross} = \frac{\omega^2 Lc_{series} - 1 - g_l{}^2 \omega^2 L^2}{\omega^2 L(\omega^2 Lc_{series} - 1)} \tag{7.2}$$

in which; c_{series} is the series connected capacitance, c_{cross} is cross connected capacitance; g_l is the single-end loaded conductance and L is the shunt connected inductance.

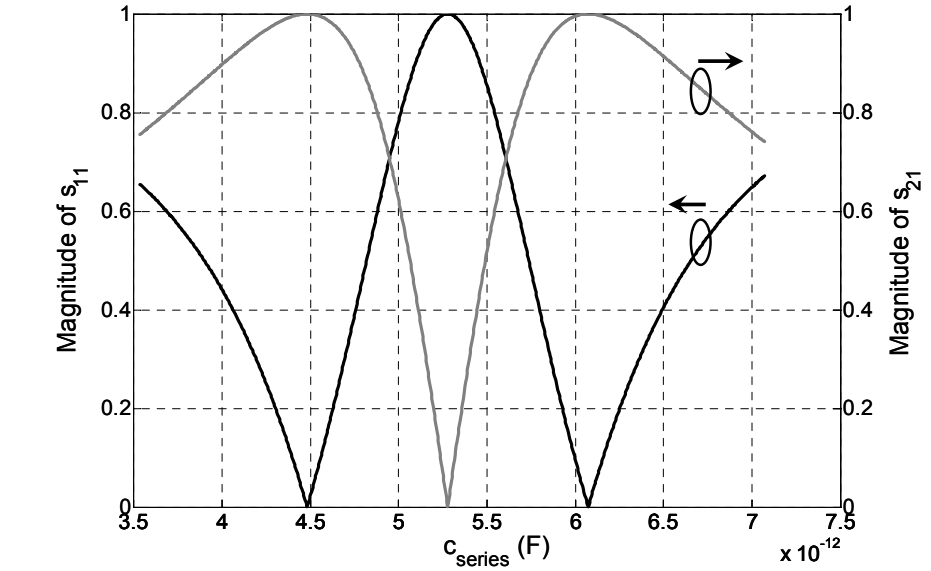
By varying the values of the c_{series} versus c_{cross} while satisfying (7.2), the following properties can be achieved:

- The transfer (s_{21}) can be continuously varied between *-j* and *+j*.
- The input impedance is always resistive.

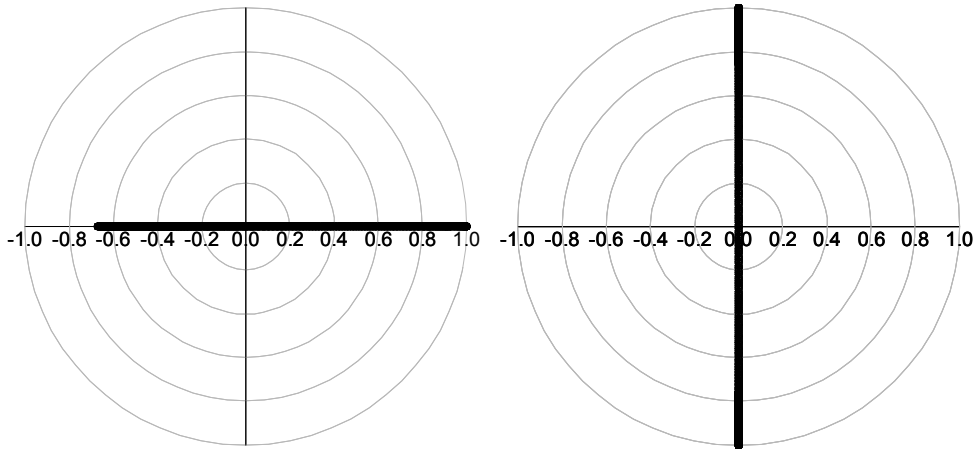
This behavior is visualized in Fig. 7.2 using a small-signal *S*-parameter analysis based on the schematic of Fig. 7.1.



(a)



(b)



(c) s_{11} (d) s_{21}

Fig. 7.2. Simulated *S*-parameter of the circuit of Fig. 7.1. (a) capacitance relationship between c_{series} and c_{cross} to obtain the results of Fig. 7.2 (c) and (d). (b) s_{11} & s_{21} in magnitude versus the capacitance variation of c_{series}. (c) Polar plot of the simulated s_{11}. (d) Polar plot of the simulated s_{21}. [f_{RF} = 2 GHz, L_{shunt} = 1.2 nH, g_l = 0.01 S and $c_{cross} = (2 - \omega^2 L c_{series}) / \omega^2 L$]

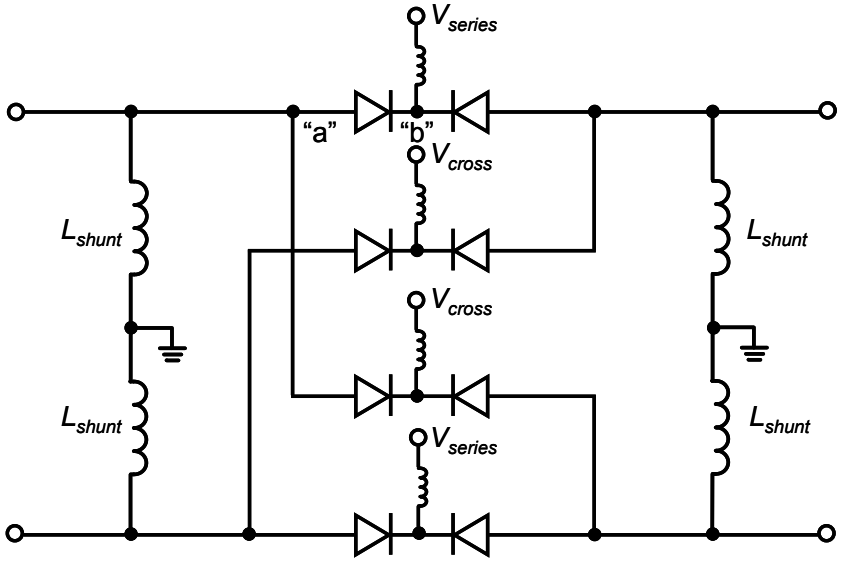


Fig. 7.3. Schematic of the differential varactor amplitude modulator using narrow tone-spacing varactor stack.

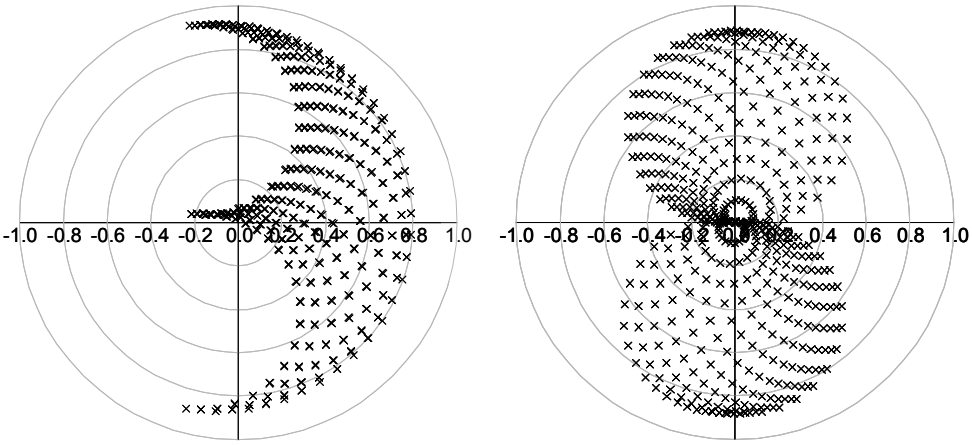
When considering the results of Fig. 7.2, one can observe that this circuit will not introduce any AM to PM distortion, since s_{21} is always on the imaginary axis. The phase reversal indicates the potential operation as multiplier. The fact that the circuit is lossless results in a reflection of all energy ($s_{11} = s_{22} = 1$) when no power is transferred ($s_{21} = s_{12} = 0$) from input to output ($c_{series} = c_{cross}$), and visa versa when all of the power transferred ($s_{21} = s_{12} = \pm j$), yielding an infinitely high impedance at the ports. Note that an inverse behavior ($s_{11} = s_{22} = -1$) is also possible if one uses series inductors rather than shunt inductors yielding short circuit conditions at the ports. The fact that the input impedance varies with the power transfer makes the network interesting for dynamic load-line applications. In the meanwhile, its unique transfer property makes it an ideal amplitude modulator for RF applications.

When the narrow tone-spacing varactor stack is utilized for the tunable capacitive element, care has to be taken to meet proper impedance requirement for IM_3 cancellation. As shown in Fig. 7.3, the center-tap inductor and additional ground in the middle of the shunt inductor are used for this purpose. Note that the shunt inductor is reused to provide a low-impedance path between the varactor diode (e.g. node *a* and *b* in Fig. 7.3) without any influence on the RF performance due to the differential topology. Two control voltages (i.e., V_{series} and V_{cross}) are used for tuning and the

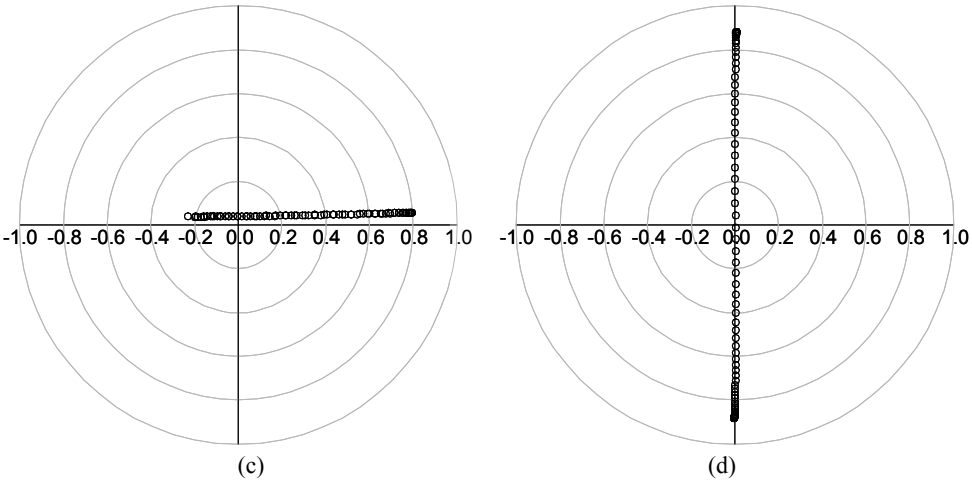
simulated s_{11} and s_{21} are plotted in Fig. 7.4 (a) and (b) when these two control voltages are tuned separately. Compared to Fig. 7.2 (d), larger constellation diagram coverage can be achieved [see Fig. 7.4 (b)], while the resulting input impedance (Z_{in}) will not be purely resistive as shown in Fig. 7.4 (a). Note that this will be problematic only for the applications that require resistive input impedance, e.g. dynamic load-line adaptation for the power amplifier. To serve these applications, (7.2) needs to be satisfied and accordingly the following function should be remained between two control voltages

$$V_{cross} = -\frac{1}{a_2}\ln\left(\frac{2-\omega^2 L_{shunt} c_{series0}\exp(-a_2 V_{series})}{c_{cross0}\omega^2 L_{shunt}}\right) \tag{7.3}$$

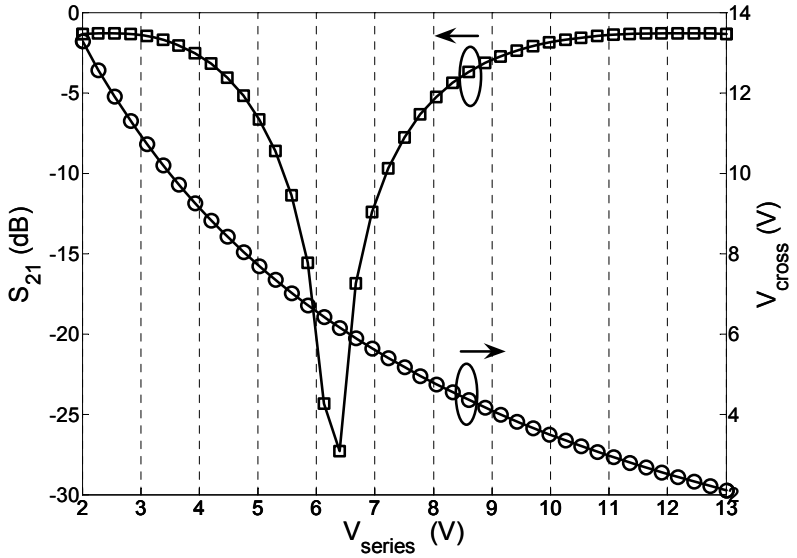
where a_2 is the doping profile dependent coefficient determining how rapidly the capacitance changes with the control voltage; $c_{series0}$ and c_{cross0} are the capacitances at zero bias of the varator diodes. Fig. 7.4 (c) and (d) show the resulting s_{11} and s_{21} with (7.3) followed, while Fig. 7.4 (e) plots s_{21} (in dB) and V_{cross} as function of V_{series}. It can be observed that s_{21} equals to 0 when $V_{cross} = V_{series} = 6.3$ V and reaches its maximum (-1 dB) when one of the control voltage is at its maximum value, while the other is at its minimum value. Note that this condition yields the biggest difference in effective capacitance between c_{series} and c_{cross}. This phenomenon agrees with our foregoing discussion. Note that the losses of the varactors and inductances are included in this simulation and for this reason the s_{11} slightly deviates from the real axis, while the s_{21} is accompanied with 1-dB loss. Fortunately, all of this is within an acceptable range and depending on the application, these losses can be easily compensated with some extra amplification as for example is the case in active load-pull measurement setups.



(a) (b)



(c) (d)



(e)

Fig. 7.4. (a) Polar plot of the simulated s_{11} when V_{cross} and V_{series} are separately tuned. (b) Polar plot of the simulated s_{21} when V_{cross} and V_{series} are separately tuned. (c) Polar plot of the simulated s_{11} when the variation of V_{cross} and V_{series} follows (7.3). (d) Polar plot of the simulated s_{21} when the variation of V_{cross} and V_{series} follows (7.3). (e) s_{21} in dB when the variation of V_{cross} and V_{series} follows (7.3). (f_{RF} = 2 GHz, L_{shunt} = 1.427 nH, $c_{series0} = c_{cross0}$ = 7.8 pF, a_2 = 0.0896 V^{-1}, the varactor's quality factor at zero bias = 50 and the losses of the inductance are counted by ADS momentum simulation).

The linearity of the network is simulated using a two-tone signal (f_{center} = 2 GHz) with varying tone spacings, while the input power of each tone is kept at 20 dBm. Fig. 7.5 plots the simulated IIP_3 as function of tone spacing and it can be observed that a superior linearity as high as 50 dBm is available up to 100 MHz. In addition to the optimized linearity of the narrow tone-spacing varactor stack, the capacitive quad topology itself also helps to improve linearity and power handling, since in the worst condition when the power is fully transferred ($s_{21} = j$), the maximum voltage swing over one of the stacks is only $1/\sqrt{2}$ times of the input voltage due to the 90° phase shift of the input-to-output signal.

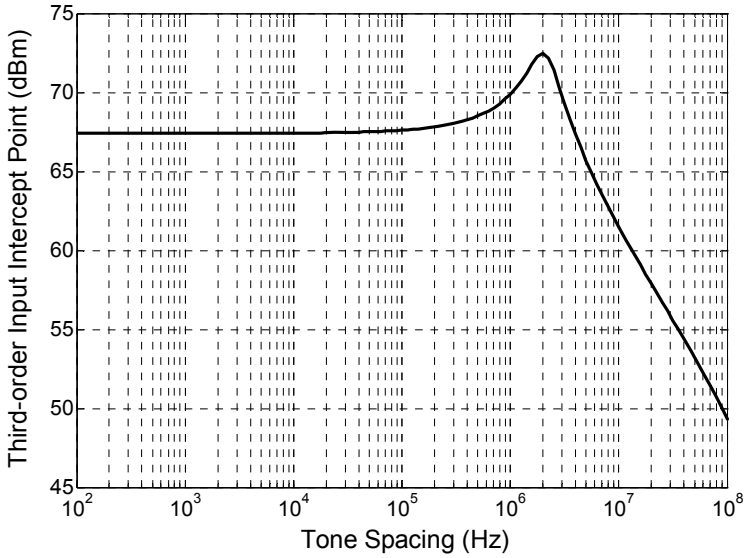


Fig. 7.5. Simulated third-order input intercept point at $2f_1$-f_2 (f_{center} = 2 GHz) as function of tone spacing when the input power equals to 20 dBm. (The transfer s_{21} is at its maximum by setting V_{series} = 2 V and V_{cross} = 13 V).

7.3 Phase Shifter with Narrow Tone-spacing Varactor Stack

For the implementation of the true-time-delay type phase shifters [1], a distributed LC ladder network is used as shown in Fig. 7.6.

In [2], the characteristics of single segment of such a network have been investigated. The transmission term s_{21} of the scattering matrix can be written as

$$s_{21} = \frac{2}{2(1 - Y_C X_L) + j(X_L + 2Y_C - Y_C^2 X_L)} \tag{7.4}$$

$$\angle s_{21} = \tan^{-1}\left[\frac{Y_C^2 X_L - 2Y_C - X_L}{2(1 - Y_C X_L)}\right] \tag{7.5}$$

with

$$X_L = \frac{\omega L}{Z_0} \tag{7.6}$$

and

$$Y_C = \omega C Z_0 \tag{7.7}$$

as normalized impedance and susceptance of the inductance and capacitance respectively. For $s_{21} = 1$ and $s_{11} = 0$, assuming lossless components, the relationship below needs to be satisfied:

$$X_L = \frac{2Y_C}{1 + Y_C^2}\,. \tag{7.8}$$

In practice, Y_C can be varied through the use of varactors or switches, whereas the impedance X_L is normally fixed and therefore can't be tuned accordingly. It suggests that the perfect matching condition, i.e., (7.8), is only available for a single combination of X_L and Y_C, while, with the variation of the capacitance, the insertion loss will be always accompanied with the desired phase shift even if the tunable elements are lossless. As a good compromise between high transmission phase-control range and low insertion loss, we define that Y_C varies symmetrically around Y_{C0}, where perfect matching ($s_{21} = 1$ and $s_{11} = 0$) occurs, by

$$Y_{C\max} = Y_{C0}\sqrt{T_{tune\_eff}} \tag{7.9}$$

and

$$Y_{C\min} = \frac{Y_{C0}}{\sqrt{T_{tune\_eff}}}\,, \tag{7.10}$$

with T_{tune_eff} being the effective tuning range of the varactors. The resulting phase-control range and maximum insertion-loss variation can be written as

$$\Delta\angle s_{21} = \left|\tan^{-1}\left[\frac{Y_{C0}^2 T_{tune\_eff} X_L - 2Y_{C0}\sqrt{T_{tune\_eff}} - X_L}{2\left(1 - Y_{C0}\sqrt{T_{tune\_eff}}\,X_L\right)}\right] - \tan^{-1}\left[\frac{\frac{Y_{C0}^2 X_L}{T_{tune\_eff}} - \frac{2Y_{C0}}{\sqrt{T_{tune\_eff}}} - X_L}{2\left(1 - \frac{Y_{C0} X_L}{\sqrt{T_{tune\_eff}}}\right)}\right]\right| \tag{7.11}$$

$$\Delta\left|s_{21}\right| = \frac{2}{\sqrt{4\left(1 - Y_{C0}\sqrt{T_{tune\_eff}}\,X_L\right)^2 + \left(X_L + 2Y_{C0}\sqrt{T_{tune\_eff}} - Y_{C0}^2 T_{tune\_eff} X_L\right)^2}} \tag{7.12}$$

When several $\prod$ low-pass sections are connected together to form multi-segmented phase shifter, the resulting s_{21} can be calculated by recursively doubling the number of lossless reciprocal segments (e.g. 1, 2, 4, 8, 16…) using

$$s_{21,c} = \frac{s_{21,o}^2}{1 - s_{11,o}^2} \tag{7.13}$$

where the subscripts "c" and "o" represent the resulting cascaded and original structure respectively.

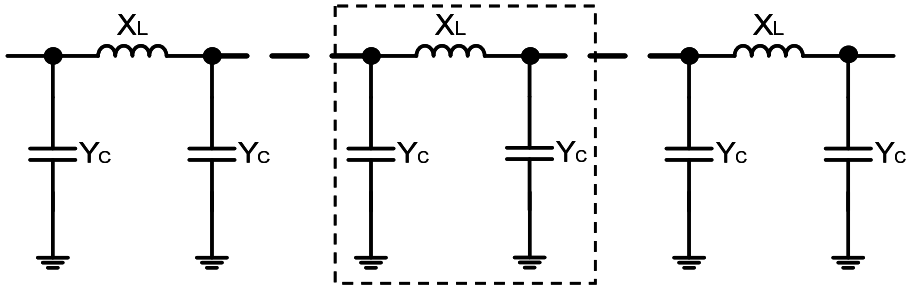


Fig. 7.6. Lumped circuit model of a true-time-delay phase shifter.

For the differential excitation, one can symmetrically copy the single-ended structure without changing the capacitance and inductance as shown in Fig. 7.7 and the resulting phase variation will be identical. Note that in the differential topology, the center-tap terminal of the narrow tone-spacing varactor stack is virtually grounded at the RF operation frequency, which facilitates the center-tap impedance requirement. In the other word, one may simply use a small resistor (e.g. 200 Ω in our design) at the center-tap node without reducing the quality-factor of varactor, which helps to increase the IM_3 cancellation region in terms of tone spacing without using the bulky inductor. In the practical layout, one may use the advantage of the coupling between inductors to reduce the losses and the total chip area.

In [2] and [3], (7.12) and (7.13) are analyzed in details. It concludes that larger tuning range and capacitance value lead to a higher phase shift for a single $\prod$ section, whereas it is accompanied with increased insertion loss. Moreover, with the increase of capacitance value, the inductance needs to increase accordingly in order to keep the matching condition for given characteristic impedance, which again results in a higher loss due to the bulky on-chip inductors. In view of this, five spiral structures as shown in Fig. 7.8 are used in our design, with a good compromise between the number of required sections and the phase shift of each section. Taking advantage of the coupling between the coils, the total chip area and loss are reduced through the use of spiral structures.

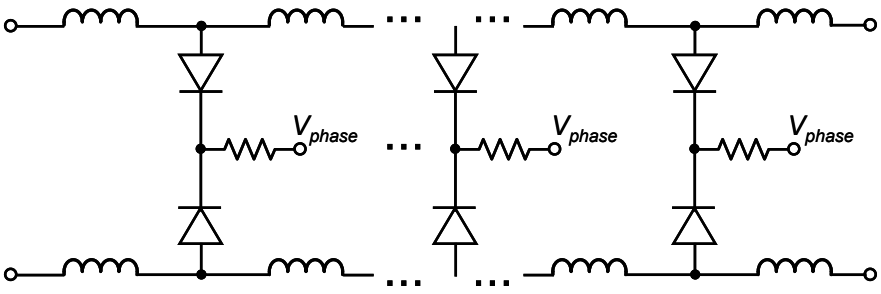
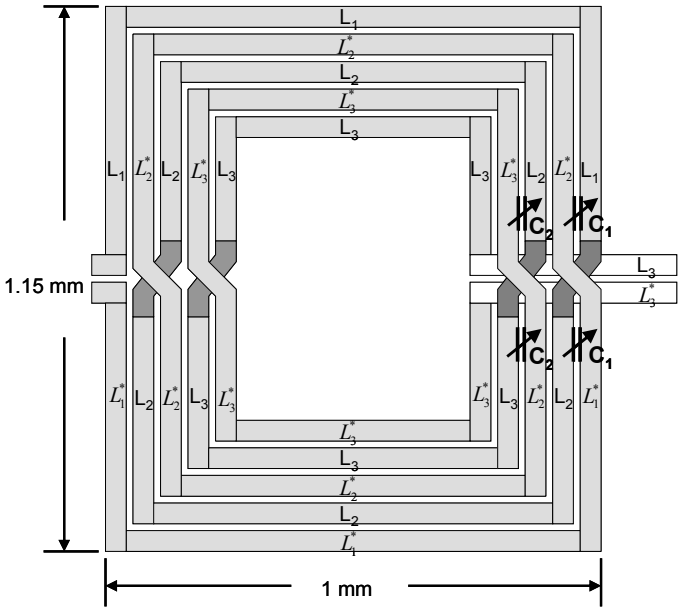
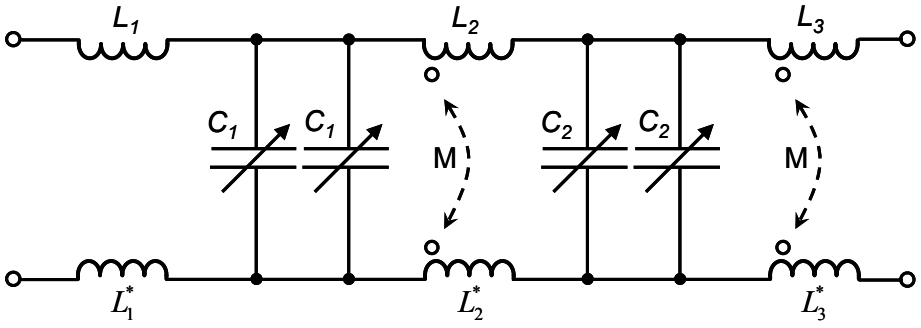


Fig. 7.7. Differential phase shifter structure using the narrow tone-spacing varactor stack.

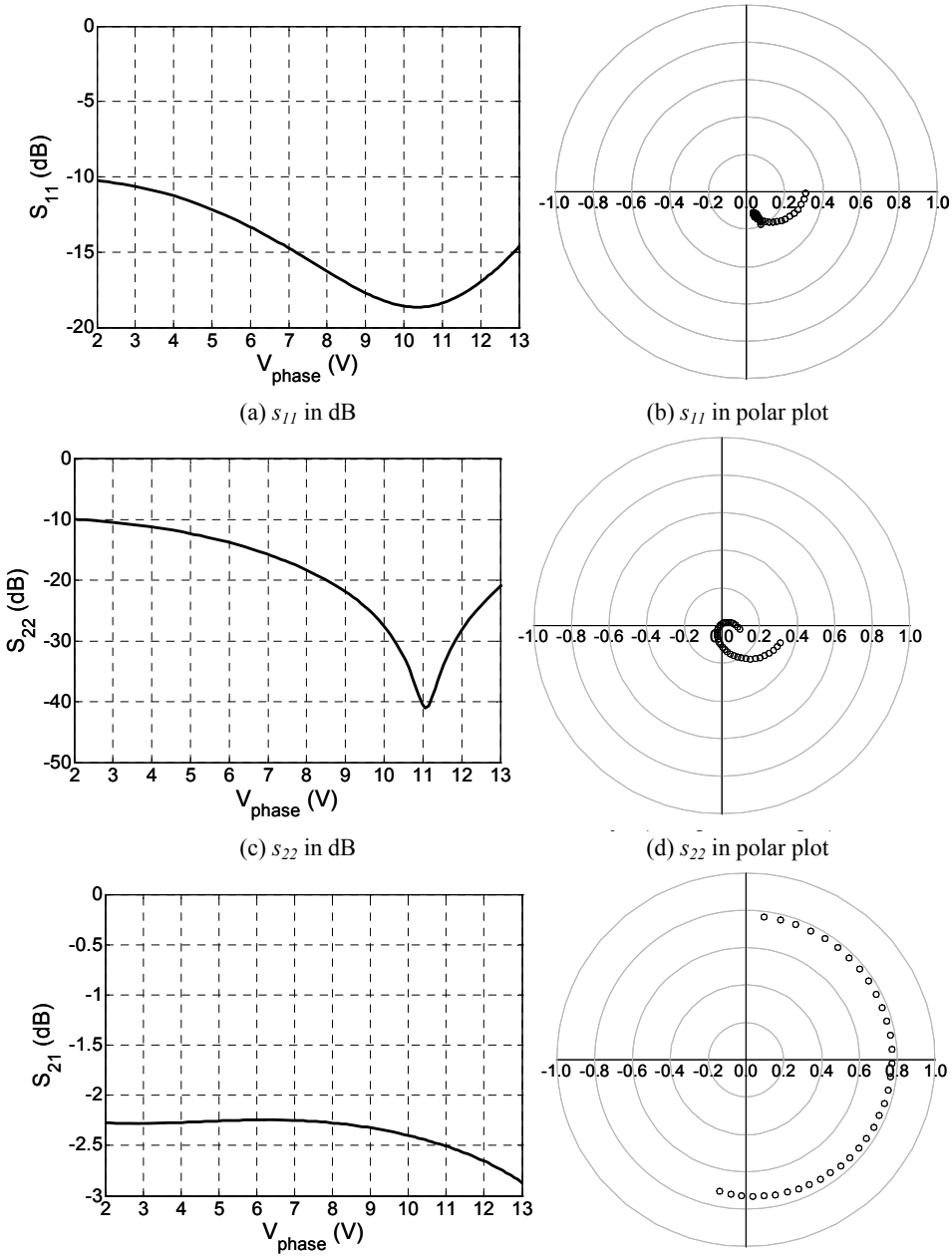


(a)



(b)

Fig. 7.8. (a) Layout of the single spiral structure for the transmission line based on a true-time-delay phase shifter. (b) Schematic of the single spiral structure.



(a) s_{11} in dB (b) s_{11} in polar plot

(c) s_{22} in dB (d) s_{22} in polar plot

(e) s_{21} in dB (f) s_{21} in polar plot

Fig. 7.9. (a) Simulated s_{11} in dB versus V_{phase}. (b) Polar plot of the simulated s_{11}. (c) Simulated s_{22} in dB versus V_{phase}. (d) Polar plot of the simulated s_{22}. (e) Simulated s_{21} in dB versus V_{phase}. (f) Polar plot of the simulated s_{21}. (f_{RF} = 2 GHz, a_2 = 0.0896 V^{-1} assuming a varactor's quality factor = 50)

The simulated *S* parameters for the 180° phase shifter is given in Fig. 7.9, showing a good matching at the input and output while providing a user controlled phase variation of 185° with a reasonable insertion loss. Note that the differential characteristic impedance of this phase shifter is 100 Ω, which saves the additional networks for impedance conversion. For this reason, big on-chip inductors are inevitable in the design and the resulting insertion loss is relatively large compared to those with lower characteristic impedances [3].

The linearity of the network is simulated using a two-tone signal (f_{center} = 2 GHz) with varying tone spacing, while the input power of each tone is kept as 20 dBm. Fig. 7.10 plots the simulated IIP_3 as function of tone spacing and suggests a superior linearity as high as 50 dBm available up to 10 MHz.

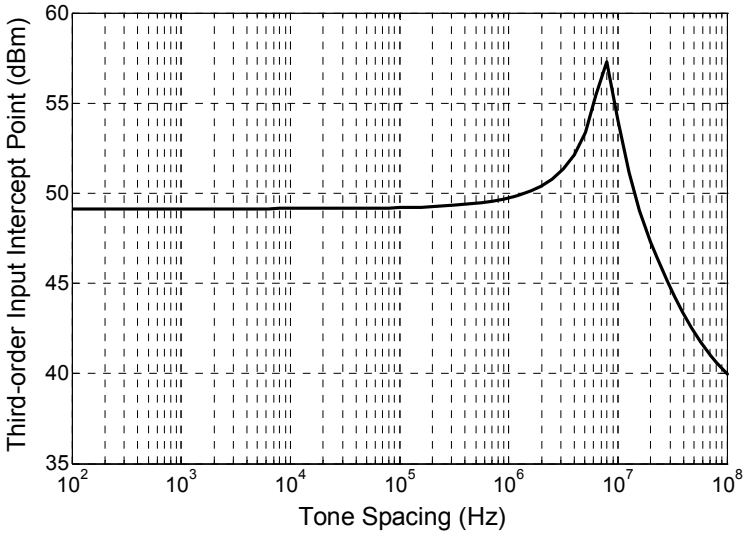


Fig. 7.10. Simulated third-order input intercept point at $2f_1$-f_2 (f_{center} = 2 GHz) as function of tone spacing with the input power of each tone set equal to 20 dBm. (V_{phase} = 8 V).

7.4 Novel Implementation of Polar Modulator

With the structures designed above, amplitude and phase control of an RF signal is facilitated in an arbitrary way with a very low distortion. As previously discussed, such functionality can be very useful in improving the performance of RF systems, like phased-array antennas and active load-pull systems, and in the meanwhile it facilitates

many new RF applications. As a demonstration, here we use a varactor-based polar modulator as potential replacement of the traditional transmitter architecture.

When combining the previous differential varactor-based amplitude modulator with the varactor-based phase shifter, we are able to create a polar modulator as shown in Fig. 7.11.

In such a concept, the amplitude and phase shift of the input signal can be controlled by the voltages of the varactor elements, yielding a very direct modulation control. Note that such a configuration can considerably simplify the traditional transmitter architecture (see Fig. 7.12), while still being capable of generating the desired complex modulated signals as are in use in wireless systems. The proposed modulator based transmitter architecture is given in Fig. 7.13. As can be noted from this figure, the control voltages of the varactors in the modulator are delivered by digital-to-analog converters, which operate at base-band frequencies. This concept eliminates the need of many RF function blocks (e.g. compare to Fig. 7.12).

By controlling the transfer function of the polar modulator in a time-variant way, we can obtain the constellation diagram of the desired modulation. By accurately controlling the transitions between the constellation points in the proper fashion, the resulting frequency spectrum at the output of the polar modulator can be adjusted in order to meet the communication standard requirements. In the meanwhile, the resulting transmitter structure is capable of serving many different modulation formats, [e.g. quadrature phase-shift keying (QPSK), binary phase-shift keying (BPSK), frequency-shift keying (FSK) etc] by just varying the digital input of the A/D converter. Consequently, the complex modulation schemes can be generated without the need of linear RF circuit blocks like the mixers and intermediate filters in the traditional transmitter implementation as shown in Fig. 7.12, which will result in a reduction of the total power. Note that the power amplifier itself can be placed in front of or behind the polar modulator (see Fig. 7.13). When placed in front, a dynamic load-line power amplifier is created, since its loading impedance will be adjusted in relation to the output power required. This mode of operation facilitates high efficiency also in power back-off operation.

However, this approach drastically increases the power / voltage level to be handled by the polar modulator, which in practice is limited by the voltage handling capability of the varactors used in the network. Also the losses of the polar modulator will have now a significant impact on the efficiency of the total transmitter.

When placing the polar modulator in front of the power amplifier, the voltage handling capability can be relaxed, however this configuration will no longer result in an efficiency improvement of the transmitter for complex modulated communication signals.

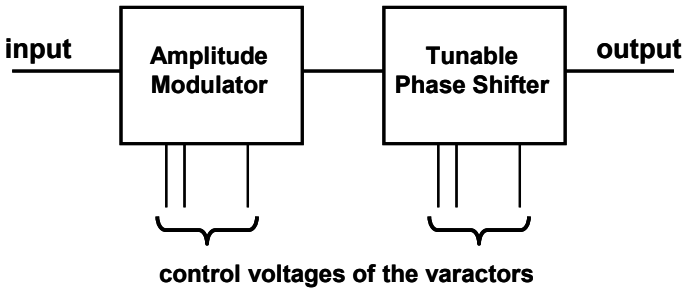


Fig. 7.11. Polar modulator based on a combination of a varactor-based amplitude and phase modulator.

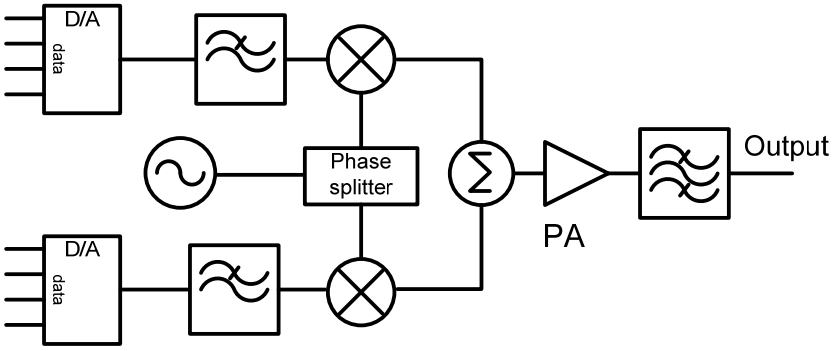


Fig. 7.12. Traditional transmitter architecture [4].

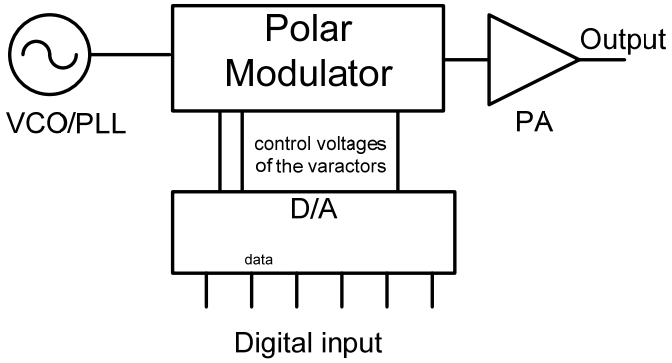


Fig. 7.13. Proposed transmitter architecture using a varactor-based polar modulator.

Since the varactors are tunable, multiple frequency bands can be addressed by just offsetting the varactor values in the network in a proper way. The phase shifter, when based on an all-pass network, or artificial transmission line topology, using multiple LC sections, has a wideband nature by itself, yielding an almost frequency independent

reconfigurable network. Note that such a network can have considerable advantages when aiming for multi-mode / multi-band transceivers since no intermediate filters or other (reconfigurable) RF functions are required. The proposed setup can also be useful for low-power, high-frequency transmitter implementations, since less power-hungry RF circuit blocks are required.

As an example, a potential implementation of such a polar modulator is achieved when we combine the designed structures as done in Fig. 7.14. Note that in these solutions it is essential that the tunable capacitive element allows fast tuning and does not cause any intermodulation distortion. For this reason, the narrow tone-spacing varactor stack seems to be the best choice, since it allows fast modulation due to the use of a base-band "short" for its center-tap control terminal, while its IM_3 distortion is canceled by combining this base band short with the proper doping profile. By changing the control voltages of the narrow tone-spacing varactor stacks, any phase shift or amplitude can be achieved, as shown in Fig. 7.15. It must be mentioned that many network topologies are possible for the amplitude and the phase modulator [1]-[3], [5], [6] that result in similar properties as shown here, however the properties of the amplitude modulator (ohmic input, no significant AM-PM distortion) can be considered to be quite unique.

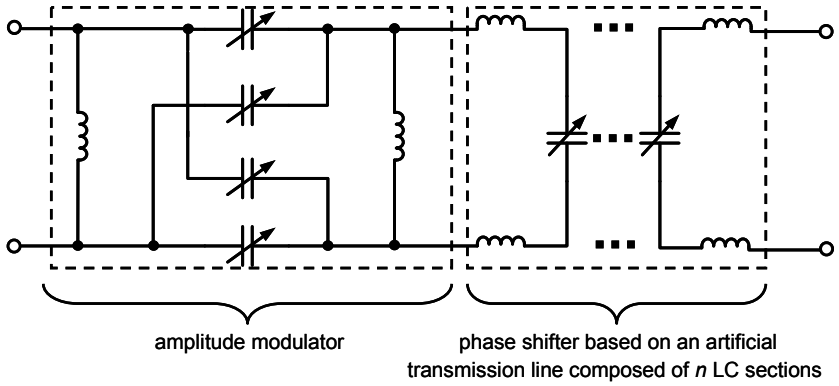
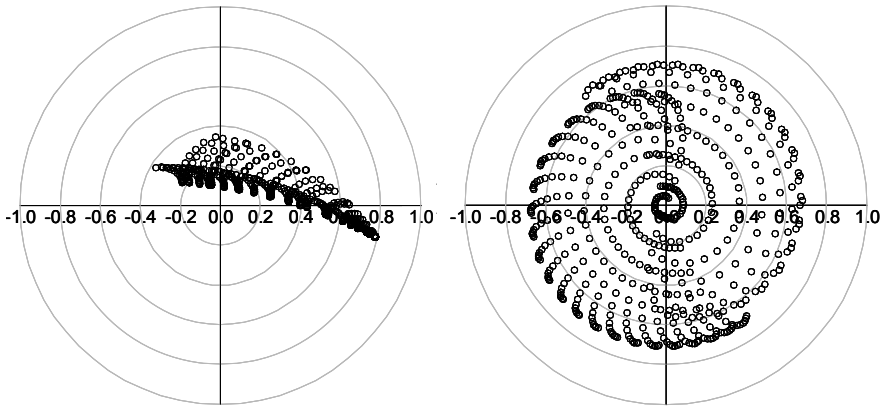


Fig. 7.14. Direct polar modulator composed of an amplitude modulator and phase shifter based on an artificial transmission line using varactors as the tunable capacitive elements.

The simulated s_{11} and s_{21} of this polar modulator, composed of the amplitude and 180° phase shifter as discussed above, are given in Fig. 7.15, which shows full coverage of the constellation diagram, with an insertion loss of around 4 dB. This loss can be easily compensated in a system as shown in Fig 7.13 by using an amplifier with a slightly higher gain. Note that such an approach can save many active RF building blocks and therefore the related system power budget can be relatively relaxed.



(a) s_{11} (b) s_{21}

Fig. 7.15. (a) Polar plot of the simulated s_{11}. (b) Polar plot of the simulated s_{21}. [f_{RF} = 2 GHz, a_2 = 0.0896 V^{-1}, the varactor's quality factor = 50, the copper thickness of the inductances=5.4 μm, the variation of V_{cross} and V_{series} follows (7.3) with the tuning between 2 V and 13 V].

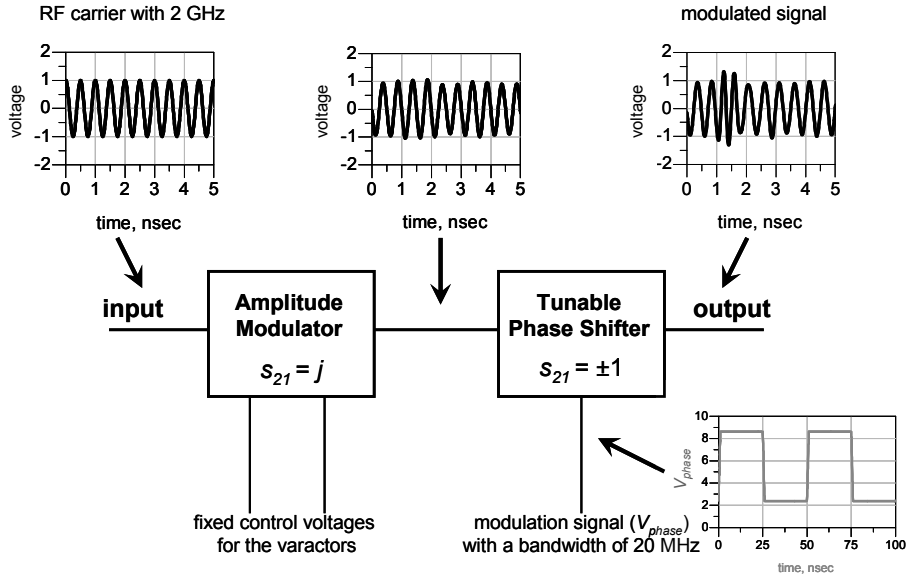


Fig. 7.16. BPSK signal generated by the polar modulator. The RF frequency is 2 GHz and modulation signal is a periodical pulse wave with a bandwidth of 20 MHz, the amplitude modulator is kept to a constant transfer function in this experiment.

In order to investigate the tuning speed of the polar modulator, a binary phase shift keying (BPSK) signal is generated with this polar modulator by fixing the transfer function $s_{21}=j$ for the first stage (amplitude modulator) and switching the s_{21} of the second stage (phase shifter) between -1 and 1 through the use of a periodical pulse

wave for the control voltage of the phase shifter (V_{phase}) as shown in Fig. 7.16. Eventually, the overall transfer function s_{21} of the polar modulator will be varied between $+j$ and $-j$, yielding the desired BPSK signal. The phase of the output modulated signal is extracted and plotted in Fig. 7.17. It shows that the rise time is around 2.5 ns and the fall time is around 3.5 ns, indicating that the polar modulator is capable of handling rapid modulation.

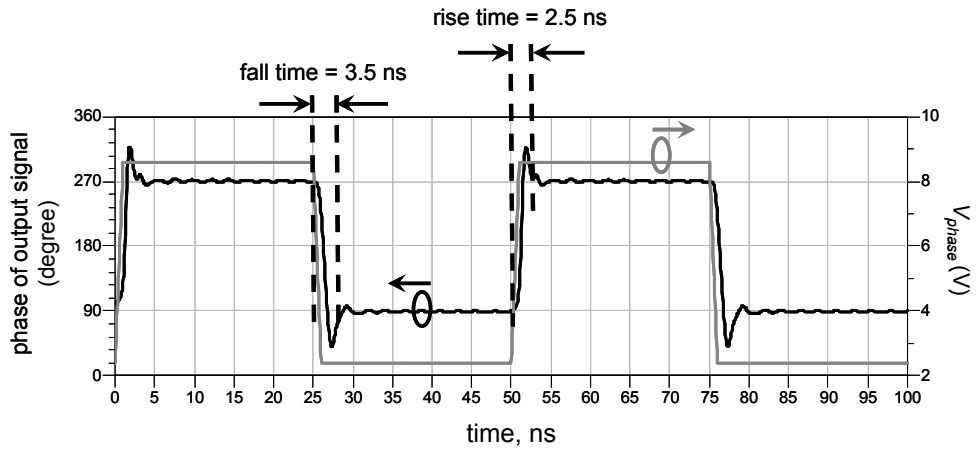


Fig. 7.17. The phase of the output BPSK signal and control voltage of phase shifter (V_{phase}) used as the modulation signal. The rise time refers to the time required for the phase to change from a low value to 90% of the step height exclusive of overshoot or undershoot, while the fall time refers to the time required to decrease from a high value to 10% of the step height exclusive of overshoot or undershoot. The bandwidth of the modulation signal is 20 MHz.

7.5 Experimental Results

To verify the concept, a polar modulator with three base-band control voltages (i.e., $V_{seriess}$, V_{cross} and V_{phase}) is implemented within the DIMES in-house silicon-on-glass technology. The resulting structure is shown in Fig. 7.18. In this test run, we have made use of high-voltage varactors diodes with the tuning range of 3.5 and maximum control voltage of 12 V. The measured s_{21} of the amplitude modulator and 180° phase shifter are plotted in Fig. 7.19 and 7.20, showing a good agreement with the simulation results in Fig. 7.4 and 7.9, except for a shift in operation frequency, which is due to the smaller breakdown voltage of the actual implemented varactor diodes (the designed value was 20 V instead of 12 V). Note that in this case the tuning is restricted to the use of relatively large capacitance values, since the desired small capacitances as used in the simulation can not be reached in the measurement due to the lower breakdown

voltage of the varactors realized. To solve this, methods, like the doping profile modification and extra ion-implantation at the edge of the active area, can be applied to improve the breakdown performance, and alternatively the area of varactors can be adjusted for frequency correction. The overall performance of the polar modulator is evaluated by cascading the measurement data of the two stages within ADS. The resulting overall s_{11} and s_{21} are shown in Fig. 7.21 with a complete coverage of constellation diagram and an insertion loss of 4 dB. The almost purely ohmic input impedance can be beneficial in terms of efficiency, when driven directly by an active device.

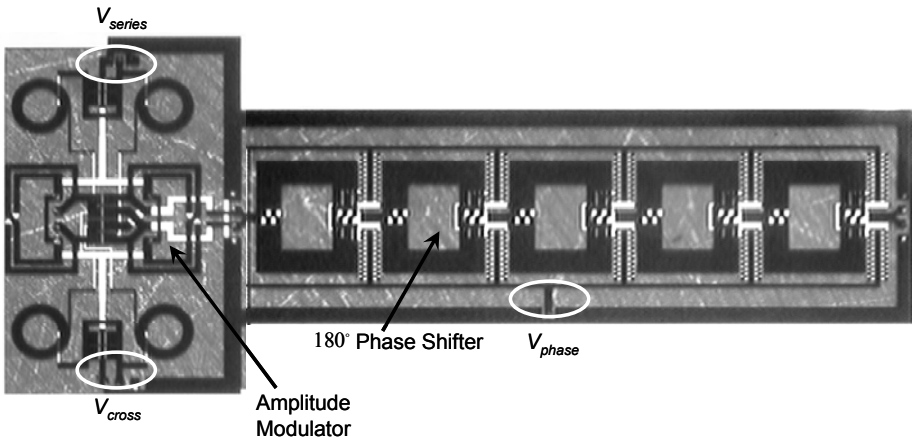
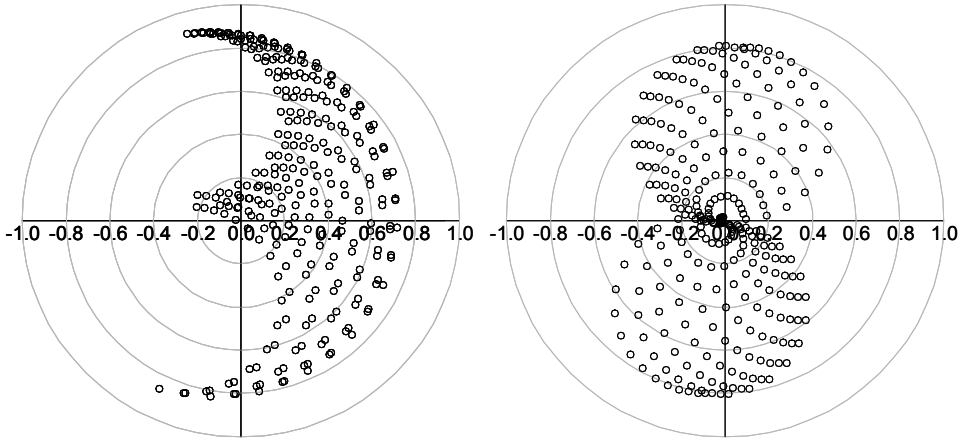
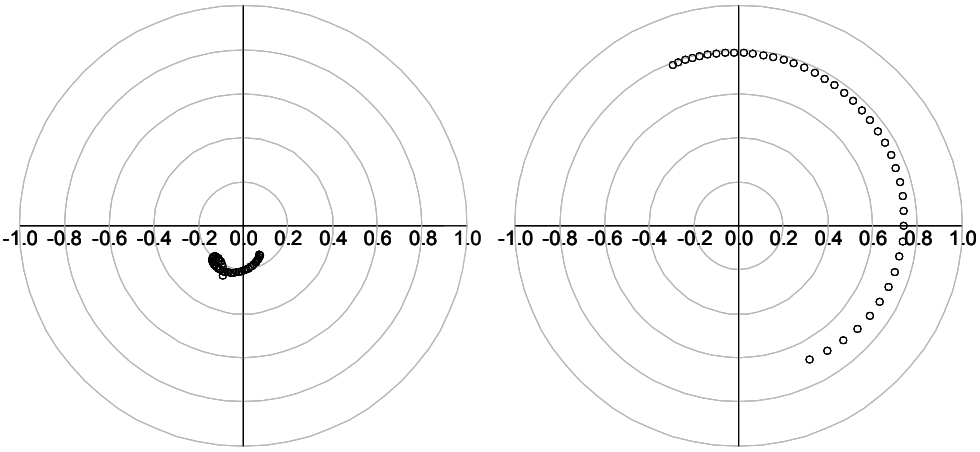


Fig. 7.18. The implemented polar modulator using the DIMES in-house silicon-on-glass technology. (Three base-band control voltages are used for tuning or modulation)



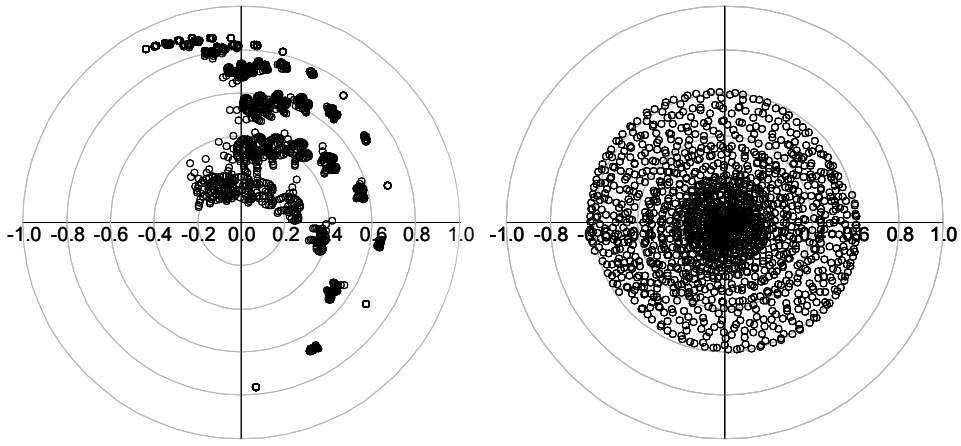
(a) s_{11} (b) s_{21}

Fig. 7.19. (a) Polar plot of the measured s_{11} of the amplitude modulator. (b) Polar plot of the measured s_{21} of the amplitude modulator. (f_{RF} = 1.4 GHz; V_{cross} and V_{series} are controlled separately between 0 V and 8 V)



(a) s_{11} (b) s_{21}

Fig. 7.20 (a) Polar plot of the measured s_{11} of the 180° phase shifter. (b) Polar plot of the measured s_{21} of the 180° phase shifter. (f_{RF} = 1.2 GHz; V_{phase} is tuned from 0.6 V to 8.6 V)



(a) (b)

Fig. 7.21. (a) Polar plot of the resulting s_{11} of the polar modulator by cascading the amplitude modulator and 180° phase shifter using ADS Data Access Component (DAC). (b) Polar plot of the resulting s_{21}. (f_{RF} = 1.3 GHz, V_{cross} and V_{series} are separately controlled between 0 V and 8 V, while V_{phase} is tuned from 0.6 V to 8.6 V).

7.6 Conclusions

In this chapter, the previously proposed narrow tone-spacing varactor stack is applied for the implementation of amplitude and phase modulators, which can be in use in phase diversity systems. The designed structures allow rapid amplitude and phase modulation with a very low distortion. These components can not only improve the performance of existing RF systems, like phased-array antennas and active load-pull system, but also facilitate other new circuit implementations or RF applications. As a demonstration, a novel polar modulator is proposed that can considerably simplify the structure of the traditional transmitter architecture, while being capable of generating the complex signals, which are typically in use in wireless communication systems. Using this modulator and controlling the transitions between the constellation points in the proper fashion, the resulting frequency spectrum at the output of the polar modulator can be adjusted to meet the requirements of the communication standard under consideration. Consequently, the proposed transmitter structure is capable of serving many different modulation formats [e.g. quadrature phase-shift keying (QPSK), binary phase-shift keying (BPSK), frequency-shift keying (FSK) etc] by just varying the digital input of the D/A converter. Other important features of this modulator are its capability to provide only purely ohmic loading conditions in power back-off operation, and the ability to avoid AM-PM distortion. To verify the proposed concept, a polar modulator is implemented within the DIMES in-house silicon-on-glass technology. The related measurements demonstrate the desired coverage of constellation diagram with a reasonably low insertion loss. This realized module can be easily further optimized for various RF applications.

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Chapter 8

Conclusions and Outlook

In this thesis, we presented different varactor diode-based circuit topologies that facilitate RF adaptivity. These proposed varactor configurations can act as variable capacitors with high tuning range, low loss, ultra-low distortion, and continuously tunable with a high tuning speed. The experimental results of the fabricated devices represent the current state-of-the-art in tuning range, linearity and quality factor among all existing continuously tunable elements. Making use of these components, we dealt with various RF reconfiguration issues, like power and impedance control in the mobile systems and multiple-standard modulators for transceivers and phase diversity systems. In this chapter, the most important results are summarized, ranging from the device components to their related RF applications, followed by a set of recommendations for future study.

8.1 Conclusions

8.1.1 Summary of Varactor Device

- **Tuning Range**

The narrow tone-spacing and wide tone-spacing varactor stacks proposed in the Chapter 3 require a free-to-choose exponential C-V_R relationship for IM_3 cancellation, which facilitates the adjustment of tuning range and control voltage range for various RF applications. Using the ability to adjust the C-V_R relationship through the doping profile, different varactor diodes with desired capacitance tuning range and related control voltage have been implemented. In the silicon-on-glass technology, “low-

voltage" devices with T_{tune}=3.5 & V_{R_max}=3.5 V and "high-voltage" devices with T_{tune}=3.5 & V_{R_max}=12 V have been fabricated, while an even more aggressive version with T_{tune}=9 & V_{R_max}=12 V is produced in the Skyworks' GaAs technology, which represents state-of-the-art tuning range and linearity characteristics performance among all existing continuously tunable elements. (Chapter 5)

- **Quality Factor**

For the junction based varactor as proposed in this thesis, the main losses come from the intrinsic semiconductor, metal interconnection, ohmic contact, low-resistivity buried layer and substrate.

To address these issues, a dedicated high-performance silicon-on-glass varactor process technology is first applied, where the varactor diode is a very straightforward "one-dimensional" structure with two-sided contacting. Using this feature, the intrinsic varactor can be directly contacted by thick metal interconnects on both sides, which eliminates the need for finger structures as typically used in conventional varactor implementations to lower the influence of the buried layer series resistance. The remaining losses of the metal interconnects can be significantly reduced through the use of plated copper, facilitating very high quality factors. Substrate losses are eliminated by the perfect isolating properties of the glass carrier, while due to low dielectric constant of glass, the influence of parasitic shunt capacitances are reduced as well. On the back-side of the wafer, the diode contacts were implanted with As^+ and laser annealed to yield very low-ohmic contacts. In order to reduce the loss of the intrinsic semiconductor, the doping profile is dimensioned for quality factor optimization and, from the material aspect, the Skyworks' high-mobility GaAs technology is used to implement the varactor diodes with extremely large tuning range and moderate control voltage, something that is not easy to fabricate in silicon, and at this stage, conventional finger structures are utilized for testing. For a brief review, all efforts used to enhance the quality factor of the varactor diode in this thesis are listed below:

	Q-limitation		*Q*-enhancements
❖	Substrate loss	→	Replace the silicon substrate with Glass
❖	Use of buried layer	→	Backside contacting
❖	Ohmic contact	→	As^+ implantation and laser annealing
❖	Metal interconnection	→	Copper plating
❖	Intrinsic semiconductor	→	Doping profile optimization and use of GaAs

Consequently, the measured quality factor at 2 GHz of the SOG varactor diode with $N_d x^{-2}$ doping profile is from ~50 to 200 over a capacitance tuning range of 3.5 with the maximum control voltage of 12 V, while the GaAs varactor diode obtained a measured quality factor from ~20 to 60 over a capacitance tuning range of 9 with the maximum control voltage of 12 V. Note that both of them represent the state-of-the-art achievable quality factor among all existing continuously tunable elements (Chapters 3 & 5). It is expected that adding a backside contact in the GaAs process technology can bring the quality factor beyond what is needed for mobile communications.

- **Linearity**

Linearity is the most important issue to be addressed in this thesis. Compared with the existing linear varactor configurations, namely the distortion-free varactor stack and high tuning range varactor stack, the narrow tone-spacing varactor stack, proposed in this thesis, provides high-linearity performance uniquely in the low-tone spacing regime, which is one of the most essential linearity requirements for adaptive transmitters. In addition, the second proposed varactor configuration, i.e., wide tone-spacing varactor stack, exhibits the highest linearity for modulated signals with wide tone spacing and provides complementary linearity behavior along with the narrow tone-spacing varactor stack and is in this sense equivalent to the high tuning range varactor stack. From the integration compatibility perspective, it proves that the wide tone-spacing varactor stack can be easily integrated with the narrow tone-spacing varactor stack, which facilitates to address the different linearity requirement of transmit and receive chains in one single technology. (Chapters 3 & 4)

The multi-stack topology is used to further improve the IM_5 dominated linearity and power handling capability. Due to its IM_5 dominated nonlinearity, the use of the narrow / wide tone-spacing varactor stack multi-stack topology yields a dramatic linearity improvement, which is double of that found in IM_3 dominated devices. (Chapter 5)

The main achievements in the linearity aspect are listed as follows:

- Measured OIP_3:
  - "Low-voltage" SOG device (T_{tune}=3.5 & V_{R_max}=3.5 V)
    - Narrow tone-spacing varactor stack:
      OIP_3 = 46 dBm up to 10-MHz tone spacing when P_{out}=16 dBm
  - "High-voltage" SOG device (T_{tune}=3.5 & V_{R_max}=12 V)
    - Narrow tone-spacing varactor stack:
      OIP_3 > 57 dBm up to 30-MHz tone spacing when P_{out}=24 dBm

- 3-stacked narrow tone-spacing varactor stack:
  OIP_3 > 67 dBm up to 10-MHz tone spacing when P_{out}=27 dBm
  Record high linearity for continuously tunable elements
- Wide tone-spacing varactor stack:
  OIP_3 >56 dBm for tone spacing > 10 MHz when P_{out}=16 dBm

➢ GaAs device (T_{tune}=9 & V_{R_max}=12 V)

- Narrow tone-spacing varactor stack:
  OIP_3 = 53 dBm up to 10-MHz tone spacing when P_{out}=24 dBm
- Wide tone-spacing varactor stack:
  OIP_3 = 48 dBm for tone spacing > 10 MHz when P_{out}=20 dBm

❖ IM_3 cancellation has been demonstrated in all implementations.

❖ It has been demonstrated that the narrow tone-spacing varactor stack and wide tone-spacing varator stack provide complementary linearity in terms of tone spacing and can be integrated on the same wafer.

❖ Their usability in practical circuit conditions has been demonstrated through source-pull simulations and measurements, illustrating that high linearity can be maintained in all cases.

❖ The system-level responses of the proposed varactor configurations are investigated under different bandwidth or data-rate conditions. It reveals that the narrow tone-spacing varactor stack is suitable for both moderate and high data-rate applications.

- **Tuning Speed**

Among all of the existing linear configurations, aiming for providing a tunable capacitance between their RF terminals without introducing nonlinear signal distortion, the narrow tone-spacing varactor stack is the only one making use of base-band "short" at the center-tap connection, which facilitates rapid modulation of the tunable capacitance, something that is beneficial for future RF applications like dynamic load-line power amplifiers or modulators. It has been demonstrated that narrow tone-spacing varactor is capable of handling rapid modulation while maintaining high-linearity performance. (Chapter 7)

8.1.2 Tunable Networks in the Mobile Systems

The adaptive matching networks demonstrated in this thesis are aimed to address the power and impedance control issues in the mobile systems. Making use of a varactor-based approach, the resulting networks are capable of dynamically correcting

the antenna mismatch with the *VSWR* of 10 over the whole Smith-chart. For all these conditions, an optimum loading for a power level between 0.5 W and 1 W is offered to the power amplifier stage along with a relatively high operating power gain. The proposed "whole Smith-chart" solution will ease the design of the RF frontend and antennas, yielding a significantly reduction in the time-to-market of mobile phones. When control over the antenna is available, antenna mismatch correction and frequency can also be directly embedded in the antenna design. In theory, this should give less losses than the "whole Smith-chart" solution, since high-*Q* conditions will be circumvented. (Chapter 6)

8.1.3 Multiple-standard Modulators for Transceivers and Phase Diversity Systems

The amplitude and phase modulator implemented in this thesis, making good use of the proposed varactor configurations, allows rapid amplitude and phase modulation in an arbitrary way with a very low distortion. It not only helps to improve the performance of the existing RF systems, like phased-array antennas and active load-pull system, but also facilitates many new RF applications. As a demonstration of new applications, the novel direct modulator proposed in this thesis facilitates the implementation of different modulation formats with a single circuit. This configuration can considerably simplify the traditional architecture of a transmitter, while still capable of generating the desired complex modulated signals, which are typically in use in wireless communication. By accurately controlling the transitions between the constellation points in the proper fashion, the resulting frequency spectrum at the output of the polar modulator can be adjusted to meet the communication standard requirements under consideration. Conquently, the resulting transmitter structure is capable of serving many different modulation formats, depending on the desired communication standard [e.g. quadrature phase-shift keying (QPSK), binary phase-shift keying (BPSK), frequency-shift keying (FSK) etc] by just varying the digital input of the A/D converter. To verify this concept, the direct modulator is implemented with the in-house silicon-on-glass technology. The related measurement results demonstrate the desired whole coverage of constellation diagram with a reasonable insertion loss. This implemented module can be easily optimized for various RF applications since it offers polar signal conditioning modulation with a very high linearity. (Chapter 7)

8.2 Recommendations for Future Work

8.2.1 Varactor Device

In this thesis, various methods are applied to enhance the quality factor of the varactor devices within two separate technologies, i.e., silicon on glass and GaAs. Consequently, the intrinsic silicon became the bottleneck for the SOG devices, while the rest of losses, like buried layer and thin metallization, constrained the quality factor of the GaAs devices. In the future, the intrinsic quality factor of the varactor device can be further improved by using wide bandgap materials, as indicated in Table XI for a SiC implementation.

In addition, one may combine all above-mentioned methods in one single technology, where the high-mobility or wide-bandgap material, like GaAs and SiC, can be utilized for the intrinsic part of the varactor and thick metal contacts can be placed on both sides, similar as the silicon-on-glass technology. By doing so, a resulting varactor device with the tuning range of 9, the breakdown voltage of 40 V and the worst quality factor at zero bias of 180 will not be a dream.

Table XI. Optimized intrinsic quality factor at 2 GHz for a SiC implementation
($\mu_n = 900\ \mathrm{cm^2/V \cdot s}$, $E_{breakdown} = 3\times10^6\ \mathrm{V/cm}$)

Tuning Range (T_{tune})	V_{R_max}=5 V	V_{R_max}=20 V	V_{R_max}=40 V
3	Q_{opt}=36765	Q_{opt}=9180	Q_{opt}=4613
6	Q_{opt}=4635	Q_{opt}=1170	Q_{opt}=585
9	Q_{opt}=1485	Q_{opt}=360	Q_{opt}=180

8.2.2 Varactor Applications

- **Above 2 GHz Bands**

In this thesis, junction varactor-based circuits have shown outstanding performance over the DC to 2 GHz frequency range, especially for wireless communication applications. The reason for such a choice is mainly due to the need of relatively large valued varactors at these bands, where the advantage of the 10+ times higher

capacitance density is over-evident compared to MEMS counterparts. However, the application of the proposed junction based varactors is readily extended till 100 GHz. In light of this, all the subsystems as demonstrated in this thesis can be scaled or redesigned for those bands. Note that the advantage of the large capacitance density will still remain in these designs and for this reason even compact size or better performance can be predicted especially for those varactor prevailed circuits, like phase shifters, tunable filters and tunable networks.

- **System Level Integration**

The proposed high-performance varactor devices may also allow the development of small-form-factor systems based on tunable filters, tunable networks and tunable antennas for multiband radios by replacing the parallel path concept as discussed in Chapter 1. In light of this, more work is required for the system level integration.

Appendix A

Calculation of Electric Field Due to the Doping of the Spacer Layer

Here we derive the restrictions on the doping level of the spacer layer in order not to seriously degrade the tuning range, breakdown voltage and quality factor.

Assume that the spacer layer (Region1 in Fig. A.1) is arbitrarily doped and the doping concentration is defined as $N_{fill}(x)\cdots(0 < x < x_{low})$.

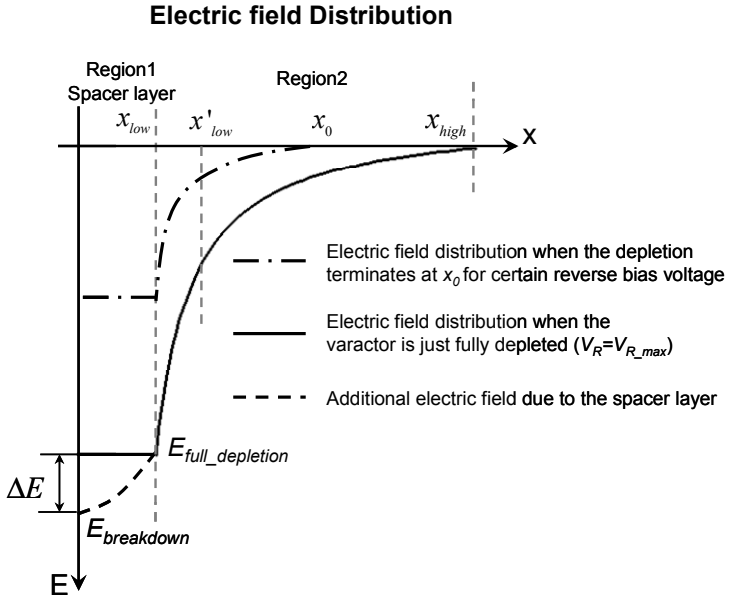

Fig. A.1. Typical electric field distribution of the graded varactor, the solid line represents the situation that the spacer layer (up to x_{low} is not doped). The dashed line represents the situation when doping in the spacer layer is present (increasing the electric field).

The additional electric field, due to the spacer layer, as shown in Fig. A.1 can be expressed as

$$\Delta E = \frac{e}{\varepsilon_s}\int_0^{x_{low}} N_{fill}(x)dx\,. \tag{A.1}$$

The sheet resistance of the spacer layer can be written as

$$R_{sheet\_spacer\_layer} = \frac{1}{e\mu_n \int_0^{x_{low}} N_{fill}(x)dx} = \frac{1}{\mu_n \varepsilon_s \Delta E}\,. \tag{A.2}$$

Consequently, if we assume that the increase in electric field must be limited to: $\Delta E = E_{breakdown}/10 = 6\times10^4$ V/cm, we can derive that - for silicon- the sheet resistance of the spacer layer equals 12 kΩ/ □. As a result, practical implementations of the quality factor optimized varactor diode will exhibit a sheet resistance for the spacer layer higher than this value.

Appendix B:

Derivation of the Doping Profile for the Exponential $C(V_R)$ Relation

In order to develop the analytical relationship between the doping profile as shown in Fig. 3.2 and the $C(V_R)$ relation, we assume:

1) The n-type region has an abrupt boundary between low doped spacer region and $N_d x^{-2}$ region.

2) The donor doping concentration is the same as the electron concentration in the n-type region.

3) Due to the high doping level at the start of $N_d x^{-2}$ region, the low-doped spacer region consumes the total built-in voltage, while the applied voltage completely depletes the $N_d x^{-2}$ region.

The doping concentration of the varactor is defined as follows:

$$N(x) = \begin{cases} N_1(x) = N_{fill} \cdots\cdots\cdots\cdots\cdots\cdots (0 < x < x_{low}) \\ \\ N_2(x) = N(x_{low})\left(\dfrac{x}{x_{low}}\right)^{-2} \ldots (x_{low} \le x \le x_{high}) \end{cases} . \tag{B.1}$$

The electric field is determined from Poisson's equation which, for a one-dimensional analysis, is

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx} \tag{B.2}$$

where $\phi(x)$ is the electric potential, $E(x)$ is the electric field, $\rho(x)$ is the volume charge density, and ε_s is the permittivity of the semiconductor. The electric field (Fig. A.1) in the n-region is found by integrating (B.2).

$$E_2(x) = -\frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left(\frac{1}{x} - \frac{1}{x_0}\right) \cdots\cdots (x_{low} \le x \le x_0) \tag{B.3}$$

$$E_1(x) = \frac{eN_{fill}}{\varepsilon_s}\left(x - x_{low}\right) - \frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left(\frac{1}{x_{low}} - \frac{1}{x_0}\right) \cdots\cdots (0 \le x \le x_{low}) . \tag{B.4}$$

Due to the Schottky contact, the potential at $x = 0$ can be defined as zero. Based on (B.3) and (B.4), the potential at x_0 can be determined,

$$\phi(x_0) = \frac{eN_{fill}}{2\varepsilon_s}x_{low}^2 + \frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\ln\frac{x_0}{x_{low}} = V_{bi} + V_R \ . \tag{B.5}$$

The first item in (B.5) is the built-in voltage, and then we have

$$C(V_R) = \frac{A\varepsilon_s}{x_0} = \frac{A\varepsilon_s}{x_{low}}\exp\left(-\frac{\varepsilon_s}{eN(x_{low})x_{low}^2}V_R\right) \tag{B.6}$$

where the constant ($A\varepsilon_s / x_{low}$) is the capacitance of the original depletion region.

The derivation of the $C(V_R)$ relation above assumes that the low-doped spacer region consumes the total built-in voltage, while the applied voltage completely depletes the $N_d x^{-2}$ region. However, even if the beginning of the $N_d x^{-2}$ region is highly doped (normally from 2×10^{17} cm^{-3} to 2×10^{18} cm^{-3}), it still consumes part of the built-in voltage. Now, we consider the more general situation, where the depletion width at zero applied voltage is x'_{low}, which is larger than x_{low}.

In this situation, (B.5) is still valid since there is no change of the doping profile. The difference is that the built-in voltage no longer equals the first term of (B.5). Instead, it should be written as

$$\phi(x'_{low}) = \frac{eN_{fill}}{2\varepsilon_s}x_{low}^2 + \frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\ln\frac{x'_{low}}{x_{low}} = V_{bi} . \tag{B.7}$$

As done previously, we substitute (B.7) into (B.5), we have

$$\frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left(\ln x_0 - \ln x'_{low}\right) = V_R . \tag{B.8}$$

Similarly, the C-V_R relation can be written as

$$C(V_R) = \frac{A\varepsilon_s}{x'_{low}}\exp\left(-\frac{\varepsilon_s}{eN(x_{low})x_{low}^2}V_R\right) \tag{B.9}$$

where the constant ($A\varepsilon_s / x'_{low}$) is the zero-bias capacitance value.

Appendix C:

Derivation of $C(V_R)$ Relation in the Case of Variation from the Ideal Power Law Exponent

Here, we keep the three assumptions mentioned above in the beginning of Appendix *B*. But, due to process variations, the doping concentration of the varactor is modified as

$$N(x)=\begin{cases} N_1(x)=N_{fill}\cdots\cdots\cdots\cdots\cdots\cdots(0<x<x_{low}) \\ \\ N_2(x)=N(x_{low})\left(\dfrac{x}{x_{low}}\right)^m\cdots\cdots\cdots(x_{low}\le x\le x_{high}) \end{cases} . \qquad \text{(C.1)}$$

Note that only the exponent of the doping profile is changed from its ideal value.

Making use of the Poisson equation, the electric field in the n-type region can then be written as

$$E_2(x)=\frac{eN(x_{low})x_{low}^{\ -m}}{\varepsilon_s(m+1)}\left(x^{m+1}-x_0^{\ m+1}\right)\cdots(x_{low}\le x\le x_0) \qquad \text{(C.2)}$$

$$E_1(x)=\frac{eN_{fill}}{\varepsilon_s}\left(x-x_{low}\right)+\frac{eN(x_{low})x_{low}^{-m}}{\varepsilon_s(m+1)}\left(x_{low}^{m+1}-x_0^{\ m+1}\right)\cdots(0\le x\le x_{low}) \ . \qquad \text{(C.3)}$$

Still defining the potential at $x = 0$ as zero, based on (C.2) and (C.3), the potential at x_0 is given by

$$\phi(x_0) = \frac{eN_{fill}}{2\varepsilon_s} x_{low}^2 + \frac{eN(x_{low})x_{low}^{-m}}{\varepsilon_s(m+2)} \left(x_0^{m+2} - x_{low}^{m+2} \right) = V_{bi} + V_R \,. \tag{C.4}$$

As was done earlier, the first item in (C.4) cancels with the built-in voltage V_{bi}. Consequently, the $C(V_R)$ relation can be written as

$$C(V_R) = A\frac{\varepsilon_s}{x_0(V_R)} = \frac{A\varepsilon_s}{\left[\frac{\varepsilon_s(m+2)V_R x_{low}^m}{eN(x_{low})} + x_{low}^{m+2} \right]^{\frac{1}{m+2}}} \,. \tag{C.5}$$

Note that the result above is only valid when m is not equal to -2.

Appendix D:

Derivation of $C(V_R)$ Relation for Variation of Doping Density at the Origin

Here, we maintain the three assumptions mentioned in the beginning of Appendix *B*, but the doping concentration of the varactor is modified as

$$N(x)=\begin{cases} N_1(x)=N_{fill}\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(0<x<x_{low}+\Delta x) \\ \\ N_2(x)=N(x_{low})\left(\dfrac{x-\Delta x}{x_{low}}\right)^{-2}\cdots(x_{low}+\Delta x\le x\le x_{high}+\Delta x) \end{cases}. \tag{D.1}$$

Making use of the Poisson equation, the electric field in the n-type region can be written as

$$E_2(x)=-\frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left(\frac{1}{x-\Delta x}-\frac{1}{x_0-\Delta x}\right)\cdots\cdots(x_{low}+\Delta x\le x\le x_0) \tag{D.2}$$

$$E_1(x)=\frac{eN_{fill}}{\varepsilon_s}\left(x-x_{low}-\Delta x\right)-\frac{eN(x_{low})x_{low}{}^2}{\varepsilon_s}\left(\frac{1}{x_{low}}-\frac{1}{x_0-\Delta x}\right)\cdots(0\le x\le x_{low}+\Delta x)\,. \tag{D.3}$$

Defining the potential at $x = 0$ as zero and cancelling the built-in voltage, based on (D.2) and (D.3), the $x_0(V_R)$ relation can be written as

$$V_R=\frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left(\ln\frac{x_0-\Delta x}{x_{low}}+\frac{\Delta x}{x_{low}}-\frac{\Delta x}{x_0-\Delta x}\right). \tag{D.4}$$

Consequently, the $C(V_R)$ relation is given by

$$V_R = \frac{eN(x_{low})x_{low}^2}{\varepsilon_s}\left[\ln\left(\frac{\frac{A\varepsilon_s}{C}-\Delta x}{x_{low}}\right)+\frac{\Delta x}{x_{low}}-\frac{\Delta x}{\frac{A\varepsilon_s}{C}-\Delta x}\right]. \tag{D.5}$$

Note that the $C(V_R)$ relation can only be written in an implicit form.

Appendix E:

Calculation of 6 dB Corner Frequency for the Resistive Center-tapped Narrow Tone-Spacing Varactor Stack

For the narrow tone-spacing varactor stack, at the IM_3-cancelled region, the remaining IM_5 can be expressed in dBc as

$$IM_5 = 20\log\left[\frac{5}{768}a_2^4\left(\frac{V_{RF\_peak}}{2}\right)^4\right] \tag{E.1}$$

where a_2 is the exponential coefficient of $C(V_R)$ relation and V_{RF_peak} represents the peak amplitude of the two-tone input voltage signal. Note that IM_5 is independent of the tone spacing (Δf) and bias voltage.

With the increase of the tone spacing (Δf), the impedance of varactor stack decreases dramatically and at certain point the IM_3 cancellation condition [$Z_c(f_2\text{-}f_1) << Z_{varactor}(f_2\text{-}f_1)$] will be violated, resulting in an IM_3-dominated nonlinearity. Based on Volterra series, the IM_3 can be expressed in function of the center-tap resistance and tone spacing Δf as

$$IM_3(R_C,\Delta s) = 20\log\left|\frac{a_2^2 C_{j0}\exp(-a_2 V_{R\_\max}/2)R_C\Delta s}{16C_{j0}\exp(-a_2 V_{R\_\max}/2)R_C\Delta s - 8}\left(\frac{V_{RF\_peak}}{2}\right)^2\right| \tag{E.2}$$

where C_{j0} is the capacitance at zero bias of the single varactor diode, R_C is the center-tap resistance and Δs equals to $i2\pi\Delta f$.

Based on Eq. (E.1) and (E.2), the 6 dB corner frequency of the varactor stack can be defined as the frequency from which the linearity of the varactor stack degrades by 6 dB. Since the nonlinearity of the varactor stack is the sum of IM_3 and IM_5 and the IM_5 distortion dominates the nonlinearity when the tone spacing is small, the 6 dB bandwidth could be estimated by the frequency at which IM_3 equals to IM_5:

$$\Delta f_{corner} = \frac{5a_2^2 V_{RF\_peak}^2}{4\pi R_C C_{j0} \exp(-a_2 V_{R\_\max}/2)\sqrt{36864 - 25a_2^4 V_{RF\_peak}^4}}. \quad \text{(E.3)}$$

Note that (E.3) takes the worst condition ($|IM_3| = |IM_5|$) into account and strictly speaking the 6 dB corner frequency should be defined as the frequency where $|IM_3 + IM_5| = 2|IM_5|$, normally resulting in a larger 6 dB bandwidth.

(E.3) hints that Δf_{corner} can be increased without bound by reducing the center-tap resistor R_C since it is inversely proportional to R_C. However, this will degrade the Q of the varactor stack. To support understanding at this point, we operate the impedance transformation at RF frequency as shown in Fig. E. 1. The resulting Q at zero bias due to the center-tap resistance can be written as

$$Q = \left| \frac{4R_C}{\frac{1}{j\omega_{RF} C_{j0}/2}} \right| = 2\omega_{RF} C_{j0} R_C \quad \text{(E.4)}$$

where C_{j0} is the capacitance at zero bias of the single varactor diode.

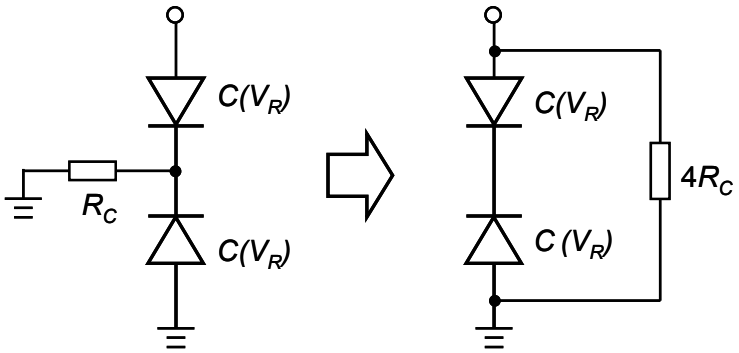

Fig. E. 1. The impedance transformation of the resistive center-tapped narrow tone-spacing varactor stack. Note that this transformation is only valid under the high Q condition, i.e., R >> $\left| \frac{1}{j\omega_{RF} C(V_R)} \right|$.

Based on (E.3) and (E.4), it can be concluded that the product of the 6 dB corner frequency (Δf_{corner}) and Q at zero bias (only considering the influence of the resistive center-tap impedance) is a constant value:

$$\Delta f_{corner} \cdot Q = \frac{5a_2^2 V_{R\_\max}^2 f_{RF} \exp(a_2 V_{R\_\max}/2)}{\sqrt{36864 - 25a_2^4 V_{R\_\max}^4}}. \quad \text{(E.5)}$$

Summary

Title: Ultra Linear Low-loss Varactors & Circuits for Adaptive RF Systems
By: Cong Huang

With the evolution of wireless communication, varactors can play an important role in enabling adaptive transceivers as well as phase-diversity systems. This thesis presents various varactor diode-based circuit topologies that facilitate RF adaptivity. The proposed varactor configurations can act as variable capacitors with high tuning range, low losses and ultra-low distortion, while being continuously tunable and facilitating fast modulation. Making use of these special components, we dealt with various RF applications that can benefit from their unique features, like power and impedance control in the mobile systems and multiple-standard modulators for transceivers and phase diversity systems.

Chapter 1 provides an overview of challenges associated with the evolution of wireless communication. Through several case studies, it has been addressed how linear variable reactors (varactors) can enable RF reconfigurability for future telecommunication systems. The challenges on varactors for these applications are brought out, which suggests an urgent need for high-performance varactors. This chapter ends with a descriptive and flow-graph-like outline of the thesis.

Chapter 2 presents an overview of the state-of-the-art tunable elements such as BST varactors, MEMS based switches and varactors, and currently available semiconductor switches and varactors. Their advantages and drawbacks are extensively discussed. These surveys clarify the motivation and goal of this thesis, and can at the same time be used as a reference to place this research with respect to the existing literature.

To overcome the limitations of currently available tunable elements, **Chapter 3** deals with the theory of two novel extremely linear varactor diode configurations with complementary linearity properties in a single varactor diode technology. Both varactor configurations use anti-series varactor diode configurations, where the diodes share the same exponential $C(V_R)$ depletion capacitance relation. However, the proposed structures differ in their harmonic terminations and varactor area ratios, resulting in a fundamentally different linearity behavior versus tone spacing. It is this feature that

makes it possible to address different requirements of transmit and receive chains in one single technology.

In **Chapter 4**, all varactor configurations, aiming for the cancellation of third-order intermodulation distortion, are summarized and their performance are compared. It is shown that the unique feature of the narrow tone-spacing varactor stack, compared to other "infinite" impedance center-tapped varactor stacks and MEMS varactors, is its high modulation frequency for operation and high linearity for signals with low tone spacing, making it perfectly suitable for many dynamic RF modulation applications. The wide tone-spacing varactor stack, which can be implemented in the same process technology as the narrow tone-spacing varactor stack, offers a complementary linearity behavior in terms of tone spacing and it can be regarded as a bonus, provided that the use of the narrow tone-spacing varactor stack is compulsory. In addition, their exponential $C(V_R)$ relationship generally yields larger tuning range compared to the uniformly doped varactors, i.e., the distortion-free varactor stack. When the multi-stack topology is used to further improve the IM_5 dominated linearity and power handling capability, it turns out that this stacking yields a linearity improvement that is the double of what is generally found for IM_3 dominated devices. The system-level responses of the different varactor configurations are investigated under different bandwidth or data-rate conditions. It reveals that the narrow tone-spacing varactor stack is suitable for both moderate and high data-rate applications, while varactor configurations with linearity limitations at low tone spacings, like the distortion-free varactor stack, may raise some in-band distortion when the bandwidth under consideration is relatively small.

Chapter 5 discusses the technology implementation issues and provides the experimental verification of the proposed varactor configurations. The measurement results provide the experimental evidence for the predicted IM_3 cancellation, as well as, for the complementary linearity behavior of the narrow tone-spacing varactor stack and wide tone-spacing varactor stack. Their usability in practical circuit conditions was demonstrated through source-pull simulations and measurements, illustrating that high linearity can be maintained in all cases. The multi-stack topology is used to further reduce the IM_5 dominated nonlinearity of the narrow tone-spacing varactor stack, yielding a record high linearity for continuously tunable capacitances. Using the ability to adjust the C-V_R relationship through the doping profile, the desired capacitance control range and related control voltage are achieved for various practical applications. In particular, the measured data of Skyworks' pre-production GaAs varactors represent the current state-of-the-art in tuning range, linearity and quality factor among all existing continuously tunable elements.

As two application examples of the novel varactors, the adaptive matching networks for mobile handsets are demonstrated in **Chapter 6**, while a phase shifter and amplitude modulator are given in **Chapter 7**.

The demonstrated adaptive matching networks in Chapter 6 are focused on the efficiency enhancement of the power amplifier in the presence of antenna mismatch. Making use of a varactor-based approach, the resulting networks are capable of dynamically correcting the antenna mismatch with the *VSWR* of 10 over the whole Smith-chart. For all these conditions, an optimum loading for a power level between 0.5 W and 1 W is offered to the power amplifier stage along with a relatively high operating power gain. The proposed "whole Smith-chart" solution will ease the design of the RF frontend and antennas, yielding a significant reduction in the time-to-market of mobile phones.

As another application example, given in Chapter 7, ultra linear low-loss varactors are applied for the implementation of amplitude and phase modulators, which can be used in phase diversity systems. The designed structures allow rapid amplitude and phase modulation with a very low distortion. These components can not only improve the performance of existing RF systems, like phased-array antennas and active load-pull system, but also facilitate other new circuit implementations or RF applications. As a demonstration, a novel polar modulator is proposed that can considerably simplify the structure of the traditional transmitter architecture, while being capable of generating the complex signals, which are typically in use in wireless communication systems.

Chapter 8 presents the conclusions and recommendations of this research. The most important conclusion is that the linearization techniques proposed in this thesis has enabled the implementation of ultra linear low-loss varactors. Making use of these varactors, various adaptive circuits can be designed for adaptive RF systems.

Samenvatting

Titel: Ultra Linear Low-loss Varactors & Circuits for Adaptive RF Systems
Door: Cong Huang

Met de evolutie van draadloze communicatie kunnen varactors een belangrijke rol spelen in de implementatie van adaptieve zenders / ontvangers alsmede faseverscheidenheidssystemen. Dit proefschrift beschrijft verschillende varactordiode schakelingen die verstembare RF schakelingen mogelijk maken. Deze componenten, die werken als regelbare condensators, bieden RF verstembaarheid met lage verliezen en lage vervorming. De ontwikkelde varactordiode schakelingen zijn traploos verstembaar en kunnen indien gewenst snel van capaciteitswaarde veranderen. In dit proefschrift zijn verschillende RF toepassingen onderzocht welke kunnen profiteren van de unieke eigenschappen van deze nieuwe varactorschakelingen. Voorbeelden zijn vermogens- en impedantie controlerende netwerken in mobiele communicatiesystemen alsmede signaalmodulatoren die geschikt zijn voor breed inzetbare zendontvangers en faseverscheidenheidssystemen.

Hoofdstuk 1 geeft een overzicht van de uitdagingen en de evolutie van draadloze communicatiesystemen. Door middel van een aantal voorbeelden wordt duidelijk gemaakt hoe vervormingsvrije regelbare capaciteiten (varactors) RF verstembaarheid voor toekomstige telecommunicatiesystemen mogelijk maken. De uitdagingen voor de varactors in deze toekomstige RF toepassingen worden inzichtelijk gemaakt, wat de noodzaak voor kwalitatief zeer goede varactors benadrukt. Dit hoofdstuk wordt besloten met een illustratie die de inhoud van dit proefschrift schematisch weergeeft.

Hoofdstuk 2 geeft een overzicht van de op dit moment bekende “passieve” regelbare componenten zoals; BST varactors, MEMS schakelaars en MEMS varactors alsmede conventionele halfgeleider schakelaars en varactors. Hun voordelen en nadelen worden uitgebreid besproken. Dit overzicht verheldert de motivatie en doel van dit proefschrift en kan als referentie gebruikt worden om dit onderzoek een plaats te geven binnen de bestaande literatuur.

Om de beperkingen van de op dit moment bekende verstembare RF componenten weg te nemen geeft **Hoofdstuk 3** de theorie van twee varactordiode configuraties, die complementaire lineariteits eigenschappen bezitten. Beide varactor configuraties gebruiken een anti-serie varactordiode topologie, waarin de dioden dezelfde

exponentiële $C(V_R)$ capaciteit – spannings relatie delen. Hierdoor kunnen zij binnen dezelfde technologie worden gerealiseerd. Echter door de verschillen in hun structuur (harmonische afsluitingen en oppervlakte verhoudingen van de varactordioden) vertonen zij een verschillend lineariteitsgedrag t.o.v. communicatie signalen met een specifieke spectrale inhoud. Het is dit kenmerk dat het mogelijk maakt om de verschillende eisen van zend- en ontvangstsystemen te adresseren binnen een enkele technologie.

In **Hoofdstuk 4** worden alle varactordiode configuraties die streven naar het onderdrukken van derde-orde intermodulatievervorming beknopt samengevat en hun prestaties vergeleken. De NTSVS topologie biedt de hoogste lineariteit voor gemoduleerde signalen met een beperkte bandbreedte. Zijn unieke eigenschap is de snelheid waarmee zijn capaciteitwaarde kan worden veranderd. Dit in contrast met andere reeds bestaande varactorstructuren die gebruik maken van hoogohmige middenaansluitingen of MEMS varactors. Door deze eigenschap is deze topologie geschikt om signalen te moduleren. Dit feit en zijn hoge lineariteit voor gemoduleerde signalen met een beperkte bandbreedte maakt deze configuratie de perfecte kandidaat voor veel verstembare RF toepassingen. De varactortopologie (WTSVS) biedt een complementair lineariteitsgedrag en is het meest geschikt voor zeer breedbandige signalen, ook deze configuratie kan in dezelfde procestechnologie als de NTSVS varactortopologie worden geimplementeerd. Beide varactor configuraties maken gebruik van een exponentiële $C(V_R)$ relatie wat een groter capaciteits regelbereik geeft dan wat kan worden bereikt met uniform gedoteerde varactors.

Wanneer het meervoudig stapelen van deze nieuwe varactor topologieen wordt gebruikt om de IM_5 gedomineerde lineariteit verder te verbeteren, dan blijkt deze verbetering het dubbele te zijn van dat wat er normaal gevonden wordt voor IM_3 gedomineerde systemen. De systeemeigenschappen van de verschillende varactor configuraties zijn onderzocht voor verschillende signaalbandbreedtes en gegevenssnelheden. Hieruit blijkt dat de NTSVS geschikt is voor zowel gemiddelde als hoge gegevenssnelheden, terwijl de WTSVS en DFVS door hun lineariteits beperking voor smalbandige signalen, in-band vervorming kunnen geven waneer de signaalbandbreedte klein is.

Hoofdstuk 5 behandelt de technologische implementatie en geeft de experimentele verificatie van de nieuwe varactor configuraties. De meetresultaten geven het experimentele bewijs voor de beoogde IM_3 eliminatie alsmede het complementaire lineariteitsgedrag van de NTSVS en de WTSVS. De praktische bruikbaarheid van deze twee schakelingen wordt door load-pull simulaties en metingen gedemonstreerd en bevestigd dat hun goede lineariteit in alle situaties kan worden gehandhaafd. Verder is de meervoudige gestapelde NTSVS structuur gebruikt om de IM_5 gedomineerde lineariteit verder te verminderen, een aanpak die een lineariteitsrecord opleverde voor traploos verstembare capacitive elementen. Door middel van het dopingsprofiel kan de

$C(V_R)$ relatie van deze varactorelementen worden beinvloed, hiermee kan het capaciteitsbereik en de controlespanning optimaal gekozen worden voor diverse toepassingen. Uit metingen blijkt dat de pre-productie GaAs varactors van Skyworks, gebaseerd op de principes geintroduceerd in dit proefschrift, het beste regelbereik, lineariteit en lage verliezen bieden van alle bekende traploos regelbare varactoren.

In **Hoofdstuk 6** worden als toepassingsvoorbeelden voor deze nieuwe varactors, dynamische impedantieaanpasnetwerken voor mobiele telefoons gedemonstreerd, terwijl een fasedraaier en een amplitude modulator in **Hoofdstuk 7** worden gegeven.

De impedantie aanpasnetwerken in Hoofdstuk 6 zijn gericht op het efficienter maken van de eindversterker als de antenne impedantie varieert door omgevingsinvloeden. Door hier gebruik te maken van varactordioden, zijn deze impedantie aanpasnetwerken in staat om de varierende antenne impedantie te corrigeren binnen een VSWR = 10 waarde over de “Smith-Chart”. Voor dit gehele bereik kan de eindversterker een vermogen tussen de 0.5 W en 1 W aan de antenne leveren terwijl zijn versterking voldoende hoog blijft. De voorgestelde "hele Smith-Chart" oplossing vereenvoudigt het ontwerp van het RF frontend en de antenne, terwijl een beduidend kortere ontwikkeltijd van mobiele telefoons wordt bereikt.

Als aanvullende voorbeelden worden in Hoofdstuk 7, de lineaire varactors met hun lage verliezen voor amplitude- en fasemodulators toegepast, welke in faseverscheidenheidssystemen kunnen worden gebruikt. De ontwikkelde schakelingen staan snelle amplitude en fasecorrecties met een heel lage vervorming toe. Deze modulatoren kunnen niet alleen de prestatie verbeteren van bestaande RF systemen, zoals “phased-array” antennes en actieve “load-pull” systemen, maar maken ook de weg vrij voor totaal nieuwe schakelingen of RF toepassingen. Als onderbouwing wordt een nieuwe polaire modulator gepresenteerd die complex gemoduleerde signalen kan genereren, terwijl de structuur van traditionele communicatiesystemen sterk vereenvoudigd kan worden.

Hoofdstuk 8 geeft de conclusies en aanbevelingen van dit onderzoek met als belangrijkste conclusie dat de linearisatie technieken van dit proefschrift, de realisatie heeft mogelijk gemaakt van zeer lineaire varactors met lage verliezen. Door gebruik te maken van deze nieuwe varactor topologieen kunnen adaptieve schakelingen voor afstembare RF systemen worden ontwikkeld.

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Co-authorship:

L. K. Nanver, H. Schellevis, T. L. M. Scholtes, L. La Spina, G. Lorito, F. Sarubbi, V. Gonda, M. Popadic, K. Buisman, L. C. N. de Vreede, C. Huang, S. Milosavljevic, E. J. G. Goudena, "Improved RF Devices for Future Adaptive Wireless Systems Using Two-sided Contacting and AlN Cooling", *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, Sep. 2009.

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Acknowledgements

The work described in this thesis would not have been possible without the contributions of many people and I have to say that it is a result of great team work. Here, I shall attempt to express my gratitude towards them.

First and foremost, I would like to sincerely thank my supervisor and co-promotor Dr. Leo C. N. de Vreede for his guidance, encouragement, a lot of great and funny ideas, assistance in writing numerous papers and reports and being the witness of my marriage. With his enthusiasm, inspiration and great efforts, I've finished this biggest and best work ever in my life.

I am very thankful to my promotor Prof. Joachim N. Burghartz for convincing me to join his group and later granting me a Ph.D. position, and for his guidance and support through this research.

A special thanks goes to Prof. Lis L. K. Nanver and her group, for supporting the fabrication of the devices proposed in this thesis, without their great work, the results in this thesis would have not been possible.

For many profitable discussions and insightful suggestions, for correcting my journal manuscripts, and for having accepted to be part of my promotion committee, I thank Prof. Lawrence E. Larson from University of California at San Diego, USA.

I thank members of my doctoral committee: Prof. dr. ir. Frank E. van Vliet, Prof. dr. Lawrence E. Larson, Dr. ir. Henk de Graaff, Prof. dr. John R. Long, Prof. dr. ir. Lis L. K. Nanver, Dr. ing. Leo C. N. de Vreede and Prof. dr. ing Joachim N. Burghartz for taking time out of their busy schedules to review this thesis, and providing insightful suggestions and commentary on the manuscript.

I am grateful to Prof. C. I. M. Beenakker and Dr. C. J. M. Verhoeven for offering me the opportunity to start my study in TU Delft.

The DIMES technical staffs have been of great help during these years; for this reason I would like to thank them all. A special thanks goes to my colleagues: Mr. "Everything": Koen Buisman (the Dutchman who is almost involved in all projects), Mr. "Loadpull": Mauro Marchetti, Mr. "Measurement": Dr. Marco Spirito (a funny friend who always has jokes), Francesso Sarubbi and Miloš Popadić (who worked together to give me varactors with the right profiles), Jun Tian (a friend that made me

drunk during my marriage banquet), Yue Ma, Dr. Lei Gu, Dr. Behzad Rejaei, Jawad Qureshi, Atef Akhnoukh, Macro Pelk, Edmund Neo, Dr. Mark van der Heijden, Saoer M. Sinaga, Dr. Hsien-Chang Wu, Sebastian Sosin, Dr. Yan Zhuang and Dr. Pedram Khalili Amiri for sharing knowledge and many useful suggestions. To my office roommate: Yan Han and José Gabriel Macías Montero, I would like to say "thank you", for being good friends and people who I could always count on.

I would like acknowledge the following people of the DIMES IC-Processing lab: Tom Scholtes, Hugo Schellevis, Bert Goudena, Silvana Milosavljević, Wiebe de Boer and W. Wien as well as Dr. Lei Gu for their contributions to the fabrication of the varactor samples.

The work contained in this thesis was supported by NXP, The Netherlands, and Skyworks' Solutions, Newbury Park, CA. I would like to thank Rik Jos, Freek van Straten, Pieter Lok, Anton de Graauw, Bart Smolders, Reinout Woltjer of NXP, The Netherlands, for actively supporting this work. For the people I worked with in Skyworks' Solutions, I would like to thank Peter Zampardi, Mike Sun, Jianli Fu, Shao and Rui for all the support and advice.

During the past six years while I was in the Netherlands, in countless ways I was supported by friends from my homeland. For this reason, a special thanks goes to all of them: Han Yan, Mingzi Zhang, Lei Gu, Qi Jia, Kerong Luo, Yiyin Wang, Xi Tan, Tao Chen, Jun Xu, Jun Tian, Bing Zhang, Yue Ma, Yi Zhao, Wanghua Wu, Yi Zhu, Junlin Yan, Lujun Zhang, Cui Zhou, Peng Zhao, Yanfei Mao, Yetao Zhu, Yi Zhu, Wenjing Lu, Rong Wu, Jia Wei, Yujian Huang, Chao Yue, Zhan Zhang, Yiwei Gong, Boxun Zhang, Zhiming Yang, Yuguang Yang and many others from Fudan University.

I also owe a big acknowledgement to my former supervisors in Fudan University: Prof. Tingao Tang and Prof. Yinyin Lin, for valuable education and guidance.

Last but not the least, a special thanks is due to my family. For their trust in my ability and being a great source of motivation, I am extremely grateful to my parents and grandparents. I would like to thank my beloved wife, Luyi Gong, and my fabulous daughter, Yiyi Huang, for their constant love and support. With you, my life has become beautiful.

About the Author

Cong Huang was born in Shanghai, China, in 1980. He received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2002, the M.Sc. degree (*cum laude*) in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2005, the M.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2005. His master's research concerned low phase-noise voltage-controlled oscillators and piezoelectric-material-based cantilevers for MEMS applications.

From 2005 to 2009, he has worked towards his Ph.D. degree at the Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology, where he is involved with high-performance varactors for RF adaptivity and the development of RF integrated circuits (RFICs) for next-generation wireless systems. During this period, he also served as an assistant lecturer of three M.Sc. courses: "Semiconductor Component and Technology", "Passive Microwave Components", and "Microwave Circuit Design".

Besides his wide interest in scientific research and education, he is with a dream of "travelling around the world".