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DOI
10.1109/JSEN.2021.3104715

Publication date
2022

Document Version
Final published version

Published in
IEEE Sensors Journal

Citation (APA)
French, P. J., Krijnen, G. JM., Vollebregt, S., & Mastrangeli, M. (2022). Technology Development for MEMS: A Tutorial. *IEEE Sensors Journal*, *22*(11), 10106-10125. https://doi.org/10.1109/JSEN.2021.3104715

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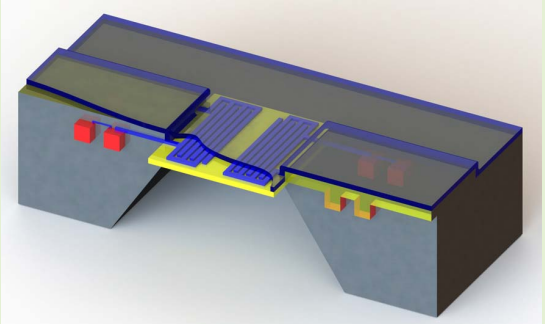
Technology Development for MEMS: A Tutorial

Paddy J. French, *Fellow, IEEE*, Gijs J. M. Krijnen, *Senior Member, IEEE*, Sten Vollebregt, *Senior Member, IEEE*, and Massimo Mastrangeli, *Member, IEEE*

***Abstract*—Silicon sensors date back to before 1960 with early Hall and piezoresistive devices. These used simple processing that was part of the early integrated circuit (IC) industry. As the IC industry developed, silicon sensors could benefit from the technological advances. As silicon sensors advanced, there came the need for new technologies specifically for microsystems. This led to a range of 3-D structures using micromachining and enabled the development of both sensors and actuators. The integration of sensors with electronics on a single chip also presented new challenges to ensure that both sensor and electronics would function correctly at the end of the processing. In recent years many new technologies and new materials were introduced to enhance the functionality of microsystems. Some sensors are still based on silicon, but others introduce new materials such as carbon nanotubes and graphene. Technologies that have been used in other applications for many years are now integral part of the microsystem technology portfolio. These include screen printing and inkjet printing. Moving more into the third dimension, 3-D printing presents many new opportunities to fabricate novel structures on a silicon substrate. This tutorial focuses on the additional technologies which have been developed to supplement standard IC processes to create MEMS structures.**



***Index Terms*—3-D printing, flexible devices, inkjet printing, micromachining, MEMS, microsystems, polymers, screen printing.**

I. Introduction

THIS paper looks into the development of technologies for microsystems, from the early devices using standard integrated circuit (IC) processing to the development of new processes suitable for new materials. After the first transistor and understanding of the pn-junction, development in silicon technology and devices advanced rapidly [1], [2]. The first idea of an integrated circuit was shown in a German patent in 1949 [3], although the first working ICs are attributed to Jack Kilby and Robert Noyce [4].

Early sensing devices included piezoresistive and Hall sensors, which were fabricated in standard processing. In the 1950s Smith and Adams showed the piezoresistive effect in silicon and germanium [5], [6]. The potential for silicon as a Hall device was first shown around the same period [7], [8]. These devices were purely planar devices. To move towards 3-D devices, there was the need to etch silicon much deeper than before. A number of papers showed how to achieve this [9]–[11]. In particular, bulk silicon micromachining by anisotropic etching provided a method to accurately determine the lateral dimensions. Interest in etching of silicon grew as the excellent material properties of silicon were reported [12]. Although surface micromachining is often seen as a younger technology, the first surface micromachined device was shown in 1967 [13].

An early example of piezoresistors fabricated on membranes was reported in 1962 [14]. An early micromachined pressure sensor was etched, not using anisotropic etching, but using spark erosion followed by electrochemical etching [15]. Soon, wet anisotropic etching using potassium hydroxide (KOH) became the dominant technique. Other etchants include hydrazine and ethylenediamine pyrocatechol (EDP), although both of these have issues with toxicity and were therefore not widely used in laboratories. KOH has issues with cleanroom contamination, which the use of tetramethylammonium hydroxide (TMAH) avoids [16]. These etching solutions yield well defined structures but are limited in the shapes which can be made. This was addressed with the expansion of plasma etching [17]. Initially this was intended for etching thin films or shallow structures into the substrate

Manuscript received June 29, 2021; accepted July 27, 2021. Date of publication August 13, 2021; date of current version May 31, 2022. The associate editor coordinating the review of this article and approving it for publication was Dr. Marios Sophocleous. *(Corresponding author: Paddy J. French.)*

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Digital Object Identifier 10.1109/JSEN.2021.3104715

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(*i.e.*, a few microns below the surface). This changed with the development of deep reactive ion etching (DRIE). The Bosch process [18] allowed deep etching of structures with high aspect ratio. Due to the cycling of passivation and etching steps, the Bosch process produced ripples on the sidewalls. An alternative is the cryogenic etching process, which uses continuous passivation and thus yields smooth sidewalls [19]. However, the cryogenic process is extremely sensitive to etching parameters and can depend on crystal orientation. With these considerations, the Bosch process has become the dominant process for DRIE. The processes described above are all silicon based. With the development of microsystems came interest in new materials. Some were introduced for achieving additional functionality or protection layers. Others became in use for their ability to work in harsh environments. In particular, silicon carbide (SiC) is known as a material able to work at high temperatures and is chemically extremely robust. The development of chemical vapor deposition (CVD) techniques made SiC an attractive material in combination with silicon. SiC MEMS devices could be made on top of silicon with excellent mechanical properties [20]. Carbon nanotubes (CNTs) and graphene have also shown excellent properties for a range of sensors [21], [22].

In recent years new, and sometimes old, technologies have been introduced into microsystem fabrication. Processes such as screen printing which can be traced back to the Song Dynasty (960-1279 AD) have been adapted, and the same basic idea is used for modern microsystems [23]. Inkjet printing dates back to the 1950s, and the ability to deposit small dots of a material has led to a wide range of possibilities for microsystems [24]. A new development in printing is the development of 3-D printing [25], [26].

The final part of microsystem processing is the packaging. Although this is one of the last steps, it needs to be considered at an early stage. The challenge with packaging is that there is no simple solution for all sensors, especially given the fact that some sensors need to have an open interface to the environment.

II. Silicon Process Technologies

The IC industry has made massive advances from a feature size of 10μm in 1971 to the few nm range in 2020. The complexity of the IC increased dramatically. When the number of devices approached 1 million, we referred to very large-scale integration (VLSI) and eventually to ultra-large-scale integration (ULSI). Using a combination of standard processes, the complete IC can be fabricated [27]–[30]. The processing is performed in a cleanroom. A cleanroom is given a class (e.g. 10) which relates to the maximum number of allowed particles of 0.5 μm diameter, or larger, per cubic foot. The class required depends on the types of devices being made and the minimum feature size.

A. Basic Processing Steps

When fabricating devices, whether they be simple structures or complex ICs, a number of basic processing steps are needed, which are used and repeated many times. Wafers must be cleaned after every step, to remove any residues (i.e., organic and inorganic particles, solvents) from the previous step and prevent contamination in the next equipment. A standard cleaning process such as RCA alternates surface oxidation, oxide stripping, rinsing and drying steps.

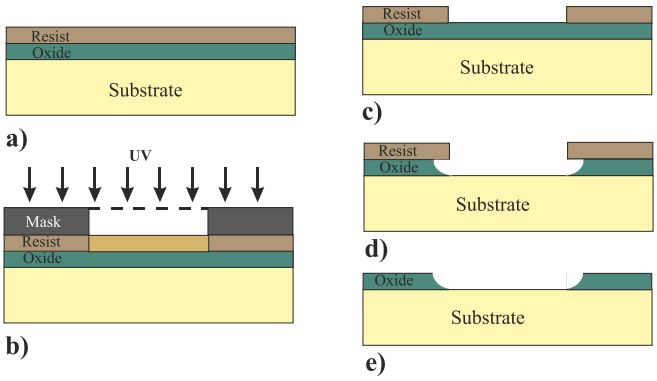

Fig. 1. Basic patterning process.

The basic process steps are:

- Patterning
  - photolithography (contact aligner, stepper),
  - direct write
- Oxidation
  - Dry, wet
- Doping
  - Ion implantation, diffusion
- Annealing, drive-in
- Etching
  - Wet, dry
- Deposition
  - chemical (CVD), physical (PVD: sputtering, evaporation)
- Packaging
  - Wafer-to-wafer, wafer-level, wire bonding, System-in-a-package, System-on-a-chip

Patterning. Patterning is a basic processing step in the cleanroom, predominantly conducted by photolithography. Processing would stop quickly if the wafer patterning is not functioning. The basic process is shown in Fig. 1. Resist is a UV-sensitive polymer material. Positive resist is softened with exposure and negative resist is hardened with exposure to UV light. In the example in Fig. 1 positive resist is spun onto the wafer and a mask is brought onto the wafer (a) to expose only selected areas of the resist to UV light (b). The resist is then chemically developed and baked to leave a pattern on the wafer (c). The wafer is then processed (d), and finally the resist is removed. Step (b) is an example of contact mode photolithography by means of a mask contact aligner. In this case the pattern on the mask covers the whole wafer at once. A stepper conversely projects the UV light through the mask onto the wafer, and using an optical system reduces the dimensions of the pattern compared to those of the mask exposing one chip at a time and covering the whole wafer in repeated exposure steps. Thanks to its optics, the stepper achieves higher patterning resolution than a contact aligner. It was once thought that optical lithography would cease as

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device dimensions decreased. However, by moving further into the UV wavelength and using advanced techniques including multiple exposures and phase masks, optical lithography can still be used for the smallest devices made. Direct write involves writing the pattern directly on the resist with, for example, an electron or laser beam. This allows for extremely high resolution, although the process is rather slow.

Oxidation – Silicon oxidizes very easily. At room temperature, it will form a native oxide of a few nm. To obtain thicker oxides, the wafers are placed in an oxygen rich environment at elevated temperatures (usually 900 °C – 1200 °C). This can be done in a dry atmosphere (dry oxidation), which gives a dense high-quality uniform oxide, or with added moisture (wet oxidation) which allows much thicker oxides. The thickness of the oxide can be estimated using the Deal-Grove model [31].

Doping – Doping uses arsenic, phosphorus or antimony for n-type material or boron for p-type material. The doped areas are defined by lithography as described above. One approach is to use diffusion. In this case the wafer is in an environment containing the desired dopant. The dopant can be from a solid, liquid or gas source. The desired dopant will diffuse into the silicon if the temperature is sufficiently high. The second technique is ion-implantation. In this case the ions are accelerated towards the wafer at high speed and are buried into the substrate. This method gives accurate shallow junctions.

Anneal/drive-in – The ion implantation, described above, causes considerable damage to the crystal structure. A thermal anneal (around 800 °C-1000 °C) repairs this damage and also allows the doping atoms to become part of the crystal structure and therefore be activated. Activation means that the doping atom takes its place in the crystal lattice thus making an electron or hole available for conduction. This process will not change the junction depth. To achieve a deeper junction, a drive-in is used. With temperatures of 1050 °C to 1200 °C the dopant will diffuse deeper (and also laterally) into the silicon.

Etching. Etching can be wet or dry. Wet etching can be used for most materials. Many are isotropic but some are anisotropic (see below). Most etching is performed at room temperature or slightly elevated temperatures. There are many etchants, and for each one needs to consider the etch-rate for the target material and also the etch-rate of any other material being used as a mask. Examples of etchant for some common materials for wet and dry etching are given in Table I.

The dry etching process is described below.

Deposition – There is a wide range of options for film deposition. Most metals are formed using sputtering or evaporation, although screen printing can also be used for high conductive metal alloys. Silicon-based materials are usually deposited using chemical vapor deposition (CVD). These come in three categories; Low pressure (LPCVD), atmospheric pressure (APCVD) and plasma enhanced (PECVD). These all use the breaking down of gasses at a set temperature to deposit the layers on the substrate. LPCVD is widely used for this purpose. Examples of gasses and temperatures are given in Table II.

If lower temperatures are required, PECVD is used. The plasma lowers the temperatures at which the gasses break down, and thus temperatures compatible with e.g. aluminum can be used. However, the layers are usually of lower quality compared to LPCVD layers. Another example of CVD is epitaxial growth. It uses the same basic process shown above, but is used for growing single-crystal layers (whereas the layers in Table II are polycrystalline or amorphous). This is widely used for silicon epitaxial layers where uniform doped layers can be deposited on the substrate. Epitaxial layers can also be formed using molecular beam epitaxy (MBE). This technique is widely used for compound semiconductors. Other epitaxial systems include liquid phase epitaxy and solid phase epitaxy.

Packaging – Packaging is an essential part of the whole IC and MEMS fabrication process and often forgotten till it is too late. For standard ICs there are standard solutions, but for sensors special solutions are often needed. For delicate surface micromachined structures it can be necessary to perform wafer-level packaging. This can be used to encapsulate the mechanical devices on the wafer before dicing and packaging. Once encapsulated, the mechanical structures can survive the normal wafer dicing process. One technique often used is to leave the sacrificial etching (see section on surface micromachining section) until after the encapsulation. In some cases, stacked wafers are required. This requires silicon-to-silicon or silicon-to-glass bonding, although other combinations are also used. There are a number of options, as illustrated in Fig. 2. The choice made depends on the structures to be bonded and

TABLE I
EXAMPLES OF ETCHANTS FOR SOME COMMON MATERIALS

Material	Wet etchant	Dry etchants
Alunimum	80% phosphoric acid (H_3PO_4) + 5% acetic acid+ 5% nitric acid (HNO3) + 10% water (H2O) at 35–45 °C[30]	Cl_2, CCl_4, $SiCl_4$, BCl_3[31]
Silicon	Nitric acid (HNO3) + hydrofluoric acid (HF) [30], Potassium hydroxide (KOH) Ethylenediamine pyrocatechol (EDP), Tetramethylammonium hydroxide (TMAH)	CF_4, SF_6, NF_3 [31], Cl_2, CCl_2F_2[31]
Silicon dioxide	Hydrofluoric acid (HF)[30] Buffered oxide etch [BOE]: ammonium fluoride (NH_4F) and hydrofluoric acid (HF)[30]	CF_4, SF_6, NF_3[32]
Silicon nitride	85% Phosphoric acid (H3PO4) at 180 °C[30] (Requires SiO2 etch mask)	CF_4, SF_6, NF_3,[31] CHF_3
Silicon carbide	Only electrochemical etching in HF	$CF_4/SF_6/O_2$ [20]

TABLE II
EXAMPLES OF LPCVD PROCESSES

Layer	Gasses	Temperature
Polysilicon	SiH_4	550°C - 700°C
Silicon nitride	SiH_2Cl_2 + NH_3 $SiH_4 + NH_3$	750°C - 900°C 700°C-800°C
Silicon dioxide (undoped)	$SiH_4 + O_2$	400°C - 500°C
PSG (phosphorus doped)	$SiH_4 + O_2 + PH_3$	400°C - 500°C
BSG (boron doped)	$SiH_4 + O_2 + BCl_3$	400°C - 500°C
BPSG (phosphorus/boron doped)	$SiH_4 + O_2 + PH_3 + BCl_3$	400°C - 500°C
SiC	$SiH_4 + CH_4$	900°C - 1000°C

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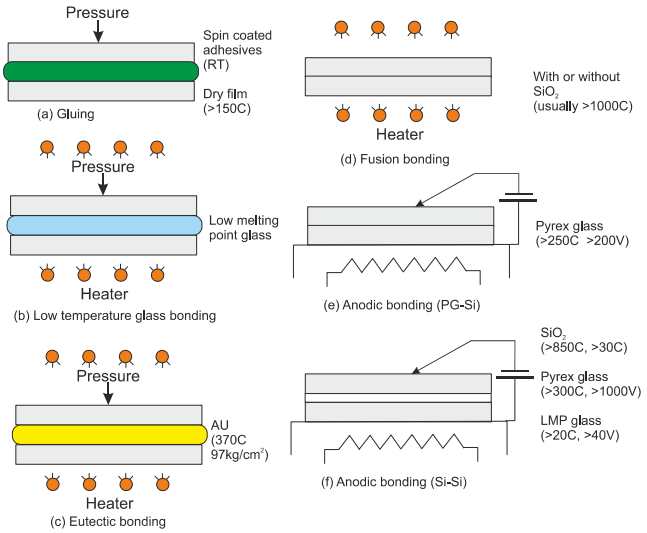

Fig. 2. Wafer-to-wafer bonding options.

also the maximum temperature which can be used. One simple technique is gluing. Even photoresist can be used to bond wafers (Fig. 2a). This can be sufficient for some applications, but for many this is insufficient. The second option is to use low melting temperature glass. This allows the glass layer to soften sufficiently to bond to both wafers (Fig. 2b). The glass frit process has been used in packaging, sealing and bonding. This glass has a low melting temperature, but the glass usually contains lead [32].

An additional option is relatively low temperature eutectic bonding with gold (Fig. 2c). Direct silicon-to-silicon (fusion) bonding (Fig. 2d) is usually performed at high temperature (around 1000 °C). It is, however, possible to bond at much lower temperatures with careful surface treatment [33]. Silicon-to-glass bonding is usually performed with anodic bonding, which uses elevated temperature and high electric field in combination with specific glass types (e). A similar process can also be used for silicon-glass-silicon bonding (f).

B. Bulk Micromachining

There are several isotropic etchants for silicon. One example is HNO_3:HF [34]. Being isotropic made it difficult to accurately define lateral dimensions. Anisotropic etchants such as KOH and TMAH solved this problem when using (100) or (110) wafers. Other etchants include EDP and hydrazine, although these have health and safety issues and are less widely used. These etchants yield the well-known rectangular holes (in (100) wafers) [11], [35], as shown in Fig. 3.

The basic process is relatively simple. The wafer to be etched is immersed in the etch-bath. It should be noted that etching parameters are highly dependent upon concentration and temperature. The important parameters are etch-rate and plane-dependent etch-rate ratio (100:111). In general, the etch process stops on the (111) plane.

The next issue is to impose the thickness of a membrane or spring. This requires an etch-stop. For this, there are four techniques:

- Time-stop

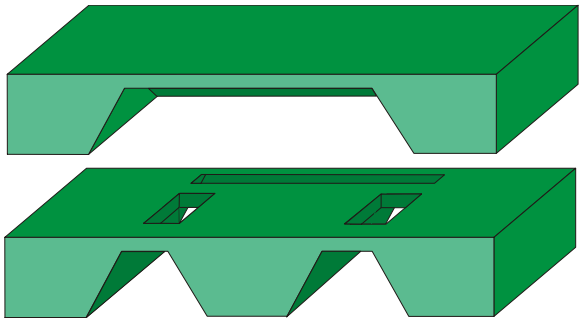

Fig. 3. Two structures fabricated using wet anisotropic etching in (100) wafers.

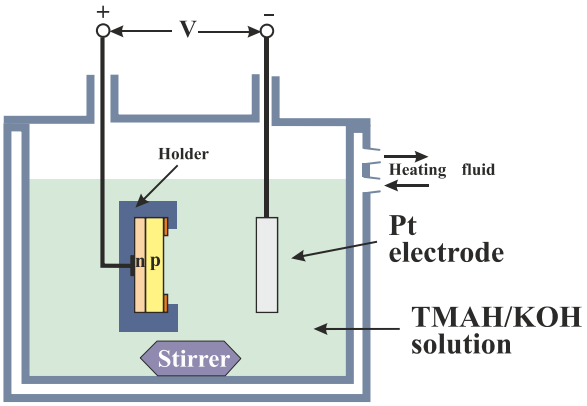

Fig. 4. Etch set-up for electrochemical etch-stop.

- P+ etch-stop
- Electrochemical etch-stop
- Galvanic etch-stop

The time-stop is simple but not accurate. The p+ etch-stop makes use of the fact that the etch-rate falls significantly with high p-doping [36]. This is accurate but can induce intrinsic stress in the structures and it is difficult to fabricate devices in high doped material. The electrochemical etch-stop uses passivation of an n-type layer. The basic etch set-up is shown in Fig. 4. The process etches through the p-type silicon until the n-type layer is reached and then a current flows. If this ensures that the passivation potential is reached, the etching stops [37], [38]. This method is accurate, but does require electrical connection to the n-type region and that the wafer is held in a holder. This makes mass production more complicated.

An etch-stop technique which avoids the need for an external electrical contact is the galvanic etch-stop. Gold in contact with silicon in a solution of KOH or TMAH forms a galvanic cell [39]. An important aspect is to have enough oxygen in the solution as this is a crucial part of the chemical process in creating the galvanic cell. This can be achieved using NaClO, which is a high oxidizing agent [40]. The basic set-up is shown in Fig. 5.

Electrochemical etching of silicon in HF can be isotropic or anisotropic. The set-up is similar to that in Fig. 4. With p-type silicon, the silicon is made porous and the process is isotropic. The resulting structure is like a sponge. The porosity can be in the range of 90%, meaning that only 10% of the silicon is left. The resulting porous layer can be used for sensors [41],

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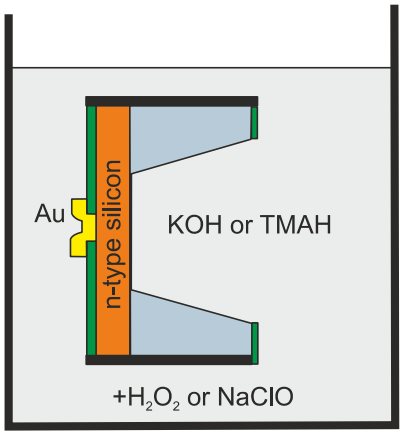

Fig. 5. Galvanic etch-stop.

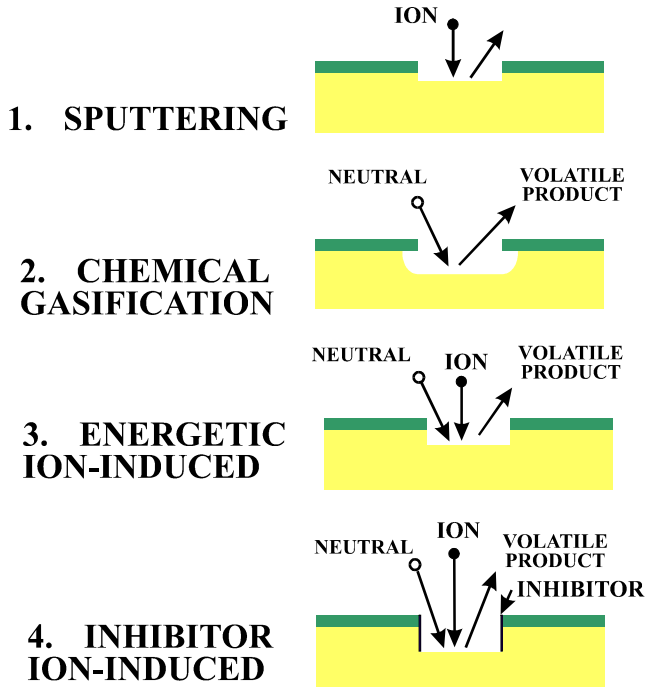

Fig. 6. Four modes for dry etching.

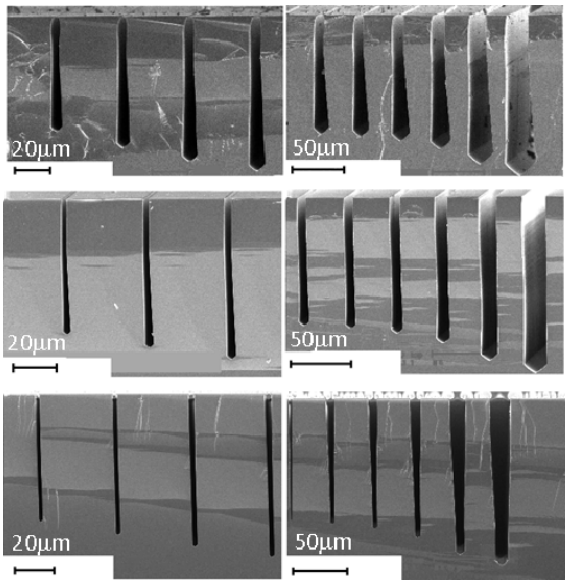

Fig. 7. Issues of tapering and aspect-ratio dependence in deep etching of silicon. (Reproduced with kind permission: Gabriel Craciun, TU Delft.)

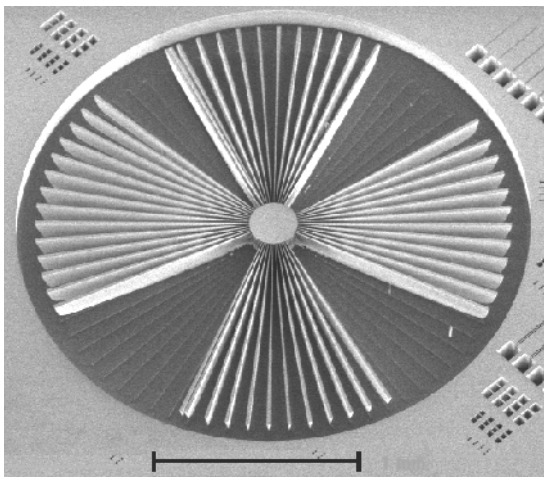

Fig. 8. Wagon wheel structure fabricated using cryogenic etching. (Reproduced with kind permission: Gabriel Craciun, TU Delft.)

or as a sacrificial layer [42]. The structure in n-type materials is quite different. With n-type material high aspect-ratio holes can be achieved by using illumination from the backside [43]. This can be used to make capacitors or for micromachined structures [44]. In micromachining, porous silicon has been used to create an easy-to-etch layer, on which an epi layer can be grown. This has been applied to the manufacture of a pressure sensor [45]. Electrochemical etching is one of the few options for wet etching of SiC [46]. This is usually used to make porous SiC, but an increase in the applied current can achieve electropolishing.

Reactive ion etching (RIE) is a type of dry etching which uses a chemically reactive plasma to etch into the substrate. It is also widely used for etching thin films on the surface. RIE uses different etching modes to achieve different shapes. As shown in Fig. 6, there are four modes. Sputtering gives vertical holes, for shallow etching. Chemical gasification will yield isotropic etching. Energetic ion-induced etching combines these two modes to give a range of profiles. Finally, passivating the sidewalls allows vertical walls during deep etching.

For bulk micromachining there was the need for deep etching and in some cases for etching through the whole wafer. The cryogenic process was first introduced in 1988. The process involves using a cooled chuck (about −110 °C) and oxygen which continually passivates the sidewall. This yields structures with very smooth sidewalls and high aspect ratio, but is sensitive to temperature, crystal orientation and aspect ratio. The etching plasma is SF_6. Fig. 7 shows the issue of verticality of the sidewall. This is related to the level of oxygen and the temperature. Also, in each of the figures the aspect-ratio dependence can be seen. The crystal orientation effect can be seen in Fig. 8. The crystal orientation dependence of the taper has led to some structure being undercut and broken off during cleaning [19]. Another issue with cryogenic etching is the sensitivity to any contamination. Although this process

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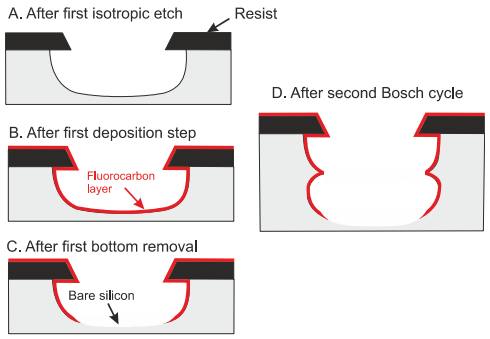

Fig. 9. The alternating steps in the Bosch etch process.

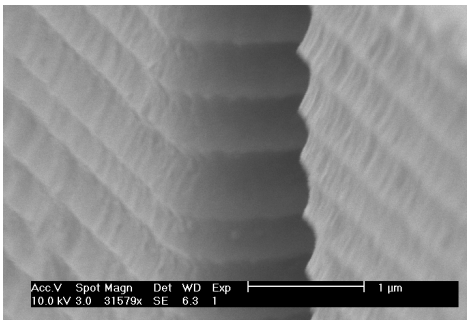

Fig. 10. Rippled sidewalls of a Bosch etched structure.

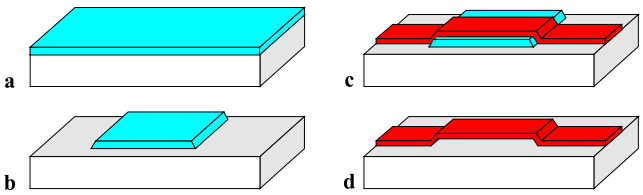

Fig. 11. Basic surface micromachining process.

TABLE III
EXAMPLE OF MATERIAL COMBINATION AND SUITABLE ETCHANTS

Sacrifical layer	Mechanical layer	Sacrificial etchant
Oxide (PSG LTO etc.)	Polysilicon, silicon nitride, silicon carbide	HF
Oxide (PSG LTO etc.)	Aluminium	Pad etch, 73% HF
Polysilicon	Silicon nitride, silicon carbide	KOH
Polymer/Polyimide	PECVD SiC	Acetone/oxygen plasma
Resist	Aluminium	Acetone/oxygen plasma

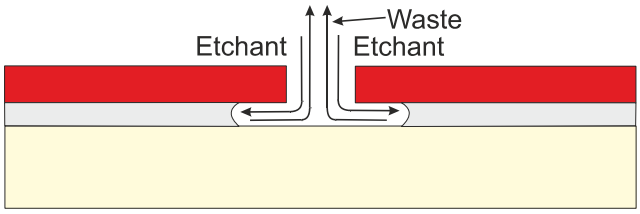

Fig. 12. Etching process with surface micromachining.

has some drawbacks, for a range of structures it can be a valuable processing tool.

The main process for deep reactive ion etching (DRIE), is the Bosch process. This was first filed in 1994 [47] and later improved in 1999 [48]. This process uses three steps, as shown in Fig. 9. First an anisotropic etch is performed (A), followed by coating with a passivation layer of all surfaces (B). Ion bombardment is finally used to clear the passivation at the base of the hole (C); then the cycle is repeated (D). This yields the ripple structure on the sidewalls (Fig. 10). With the development of new plasma etchers, faster switching can reduce the size of the ripples (if needed). The Bosch process does not have the problems with crystal orientation dependence of aspect ratio.

It should be noted that, although many etching machines can support both cryogenic and Bosch etching, problems can arise if both are used in a single machine. The Bosch process deposits the passivation layer on the inside of the chamber. If the cryogenic is then used, without cleaning the chamber, deposits from chamber walls will deposit on the wafer and deteriorate the etching process.

C. Surface Micromachining

Surface micromachining generally uses thin films deposited on the substrate, which are divided into two groups: mechanical (structural) layers and sacrificial layers. The first example of a surface micromachined structure was presented in 1967 [13]. The basic process is shown in Fig. 11.

The sacrificial layer is deposited (a) and patterned (b). This is followed by the deposition and patterning of the mechanical layer (c) which is partly detached from the substrate and released by selectively removing the sacrificial layer (d). It is important that the mechanical layer has good mechanical properties, and that the sacrificial layer can be easily removed without damaging the mechanical layer. The main preferred mechanical properties are:

- Low tensile stress
- Low stress gradient through the thickness of the layer.

Low tensile stress will ensure that a double-clamped beam remains straight and does not buckle. A stress profile in the layer (difference in intrinsic stress between upper and lower surface) will cause single clamped structures to curve up or down after release. There have been examples where a stress profile has been addressed through design [49]. Examples of material combinations are given in Table III. There are many more options beyond these examples.

The development of polysilicon surface micromachining was probably the most important boost to the use of surface micromachining [50]–[54], and this led to the introduction of several other materials. Silicon nitride, deposited by LPCVD, has also been shown to be an excellent material for micromachining [53]. In more recent years there has been increased interest in SiC due to its excellent mechanical properties, high temperature capabilities and chemical inertness [20], [54].

Most silicon-based layers are formed using CVD, metals, by sputtering or evaporation and polymers by spinning. The example given in Fig. 11 is for a single mechanical layer. The basic process is to immerse the wafer into the etchant. In all cases there are limitations as to how far the under-etching can proceed due to the need to remove the waste products from the etching areas. This is illustrated in Fig. 12.

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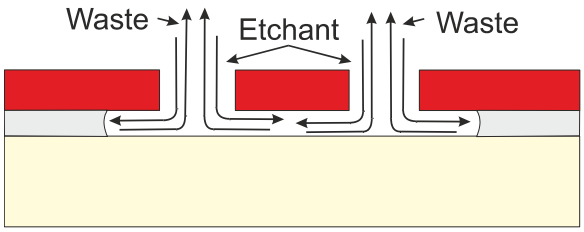

Fig. 13. Under-etching structures using etch holes in the mechanical layer.

Fig. 14. Working gear system made with polysilicon. (Courtesy Sandia National Laboratories, SUMMiT™Technologies, www.sandia.gov/mstc.)

In this process, the etch-rate will slow down and eventually effectively stop. The solution is to include etch holes, as shown in Fig. 13.

Surface micromachining has been expanded into multiple layers, mainly driven by the development of micro-actuators. Sandia, for example, has a 5-polysilicon layer process which enables the fabrication of complex actuators. An example of a micro gear system is given in Fig. 14.

A major issue with surface micromachining is stiction. When devices are released, structures can be sucked down due to surface tension as the liquid dries and stick to the substrate. A final rinse in IPA will reduce the surface tension, which can reduce stiction, but has limited effect. The two main ways to avoid stiction during release are "freeze drying" [55] and super critical drying [56]. Using vapor etching, or plasma release can also greatly reduce stiction problems [57], [58].

Freeze drying uses a final rinse in cyclohexane. The substrate must be rapidly cooled and gradually brought back to room temperature. This uses the fact that cyclohexane does not expand when freezing and also that it sublimates in the warming process. It is important to keep the devices in a nitrogen flow during warming to avoid any moisture from the air entering in the chamber. Super critical drying uses a number of temperature and pressure cycles in a high-pressure CO_2 filled chamber. In the same way as freeze drying this technique ensures that the liquid evaporates without causing stiction.

After release stiction can occur when surfaces come into contact. Surface roughening or bumps in mechanical structures will reduce the surface area of contact and thus reduce the sticking force [59]. Alternatively, an anti-stiction coating can be used [60]. This is applied to the surfaces to ensure a significant reduction in stiction forces. Organic hydrophobic monolayers are deposited on the substrate to reduce surface energy and avoid stiction. High-quality monolayers can be deposited from liquid or vapor phase, the latter option being more widely accepted and convenient for manufacturing.

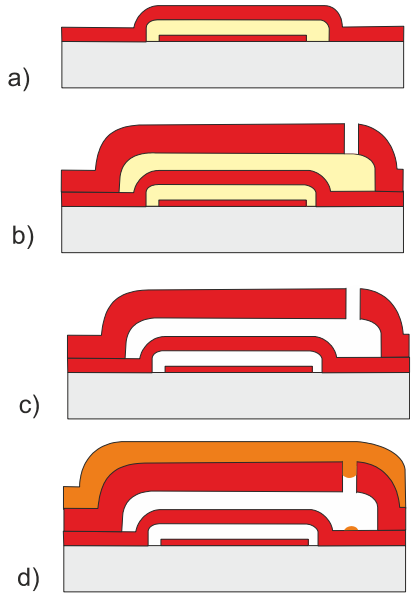

Fig. 15. Wafer-level encapsulation process.

A further important consideration is packaging, as described above. Surface micromachined structures can be delicate, so one option is to encapsulate them, which can be done at wafer scale. This process is shown in Fig. 15. The processing is performed up to the sacrificial etching (a), after which a second sacrificial layer is deposited together with the encapsulation layer (b). Note the access hole in the encapsulation layer. Through the access hole, the sacrificial etching is performed (c). Finally, a second encapsulation layer is deposited, which seals the cavity (d). The pressure in the cavity will be determined by the deposition pressure and temperature of the last layer.

D. Epi Micromachining

Although less widely used than surface micromachining, epitaxial micromachining can make use of the excellent mechanical properties of single crystal silicon while having the lateral dimensions of surface micromachining. Processes include: epi-poly [61], silicon-on-insulator (SOI) [62], merged epitaxial lateral overgrowth (MELO) [63], [64] and sacrificial porous [42], all of which use the upper epitaxial layer as the mechanical element. Epi-poly is similar to polysilicon surface micromachining but deposits the polysilicon in an epitaxial chamber. This enables much thicker layers than practical in LPCVD. A combination of Epi-poly and single crystal silicon can be formed in a single deposition by having areas of the substrate covered with oxide and LPCVD and in other areas bare silicon [65]. The SOI process uses commercially available

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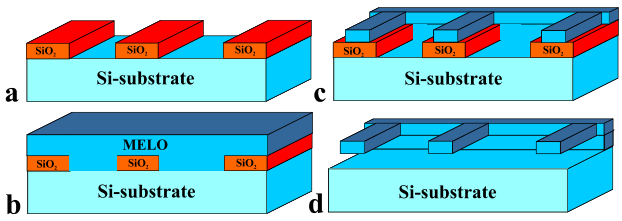

Fig. 16. Basic MELO process (adapted from [64]).

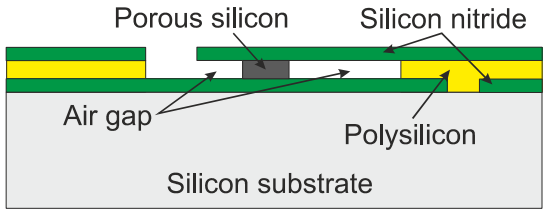

Fig. 17. Porous silicon plug, made in polysilicon (Adapted from [66].)

SOI wafers. The upper layer thickness can be chosen to fit the application. MELO is based on selective epitaxial growth (SEG), whereby silicon only grows where the silicon substrate is not masked by the silicon dioxide. If this process is extended the epi will grow laterally over the oxide. The basic MELO process is shown in Fig. 16. After the oxide is formed and patterned (a), the epi-layer is grown to form a continuous layer over the oxide (b). This is then patterned (c) and the structure is released using standard sacrificial etching (d).

Finally, the sacrificial porous process makes use of the fact that, in dark conditions, p-type material will be made porous, but n-type not. Using this, the p-type substrate can be made porous without affecting the n-type epi-layer. Silicon with high porosity will etch extremely quickly and can be removed easily, leaving free-standing n-type silicon mechanical structures.

Sacrificial porous silicon makes use of selective porous formation of p-type silicon and not etching the n-epitaxial layer. It should avoid illumination, since this can lead to macro-porous formation in the n-type silicon. The porous formation is an electrochemical process. A higher current will result in electropolishing of the silicon, so it is removed directly. A lower current will leave a porous silicon layer, which can be removed later in the process. The resulting structure is shown in Fig. 17 [66]. The porous silicon is made in polysilicon. When a low current is used porous silicon will result. If the current is then increased, electropolishing will result, without affecting the porous silicon plug. A low temperature oxidation of the porous plug will seal the cavity.

Another approach is to make a highly porous layer, or electropolish just under the surface of the silicon. The top layer should be porous enough to allow the HF to access the underlying layer. Once the cavity has been created, an epi-poly layer can be deposited on top [67].

E. Wafer-Scale Transfer and Substrate Etch-Back

Wafer-scale transfer is similar, in many cases, to wafer bonding, but uses a wide range of materials and can also be used for thin-film addition to the substrate. One example is for CMOS, where most of the substrate is removed and contact made from the backside. This basic process is shown

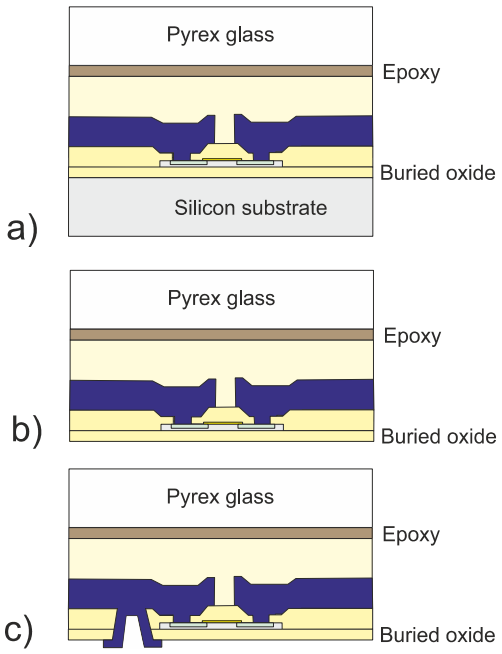

Fig. 18. Wafer transfer for CMOS. Adapted from [68].

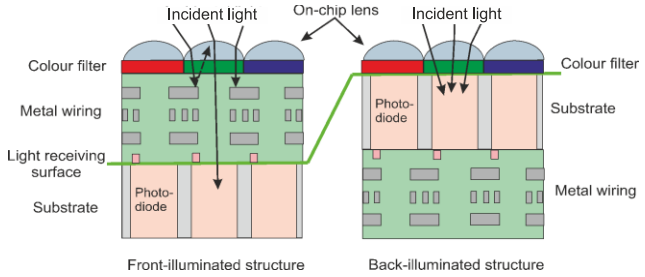

Fig. 19. Back illumination of CMOS image sensors. Based on the SONY report [69].

in Fig. 18. At the end of the CMOS process an epoxy is used to fix the wafer to a Pyrex wafer (a). The silicon substrate can then be removed while mechanical stability is maintained (b). Finally electrical contacts are made to the underside of the CMOS circuit (c) [68].

In some cases, standard IC's are etched back to leave a thin layer of silicon, which can be used to reduce parasitics from the substrate. In CMOS image sensors, this can be used to enable back illumination, as shown in Fig. 19.

Another area of application for wafer-transfer is combining III-V materials with silicon. Thin films can be deposited on a III-V substrate, removed, and transferred to a silicon substrate. Such a process is shown in Fig. 20. Finally, the emergence of 2D materials like graphene, which often require a separate growth template, led to the development of many different transfer techniques [70]–[72]. For this typically a polymer support is used during transfer. An example of such a transfer process for graphene is illustrated in Fig. 21 [72].

III. New/Alternative Materials

The processes described above have been based on silicon. Although silicon is an excellent semiconductor and mechanical material, there are many other material options

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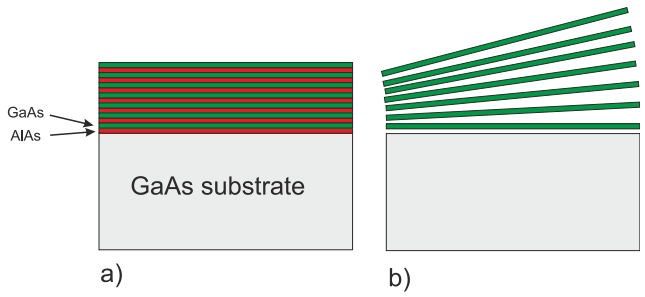

Fig. 20. III-V materials for transfer to a silicon substrate. Adapted from [70].

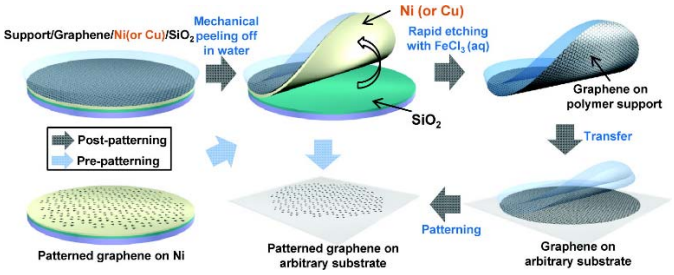

Fig. 21. Schematic illustration for synthesis, etching, and transfer of large-area graphene films. Reproduced with kind permission from [72]. Copyright 2010 American Chemical Society.

available, which alone and/or in combination with silicon allow to address a larger variety of needs and applications for microsystems.

A. Silicon Carbide

Silicon carbide wafers have been on the market for many years. This wide band-gap semiconductor is highly suitable for power devices and high temperature applications. For many MEMS applications, however, the wafers were too expensive. The introduction of CVD processes made SiC much more attractive for MEMS applications [20], [54], [73]. The main deposition methods are LPCVD (deposition 800 °C-1000 °C) and PECVD (deposition <400 °C). Deposition requires a source of Si and C. One combination is SiH_4/CH_4. As with all CVD processes the parameters are extremely important. In addition to temperature and pressure, the ratio of the two gasses controls the chemical composition of the material and also properties such as the mechanical stress.

The excellent mechanical properties (strength, chemical resistance) make SiC an extremely attractive material for MEMS applications and harsh environments. The chemical robustness of SiC also means that it is difficult to etch chemically. Plasma etching is usually used. There is the option of electrochemical etching in HF [74]. This is used to make porous SiC. By increasing the current density, this will lead to electro-polishing.

B. Polymers

Polymers and organics are not new materials in IC technology, and some, such as photoresists, have been used for many years as key enablers of photolithographic patterning. Nevertheless, new applications have been found for polymers and organics as both structural and sacrificial materials in microsystems.

The LIGA *(LIthographie, Galvanoformung, Abformung)* process was developed to make truly tall structures on the substrate. This used a polymer which could be deposited in thick layers and patterned using synchrotron X-rays or UV-light. The full process then used electroplating to form mechanical structures [75]. The problem with this approach was the need for synchrotron radiation, which is expensive and not widely available.

A cheaper alternative to LIGA is SU8, an epoxy-based negative-tone photoresist which can be used to fabricate a range of mechanical structures. SU8 can be patterned using standard lithography and deposited by spin coating, inkjet printing and dry film lamination, the latter convenient for relatively thick layers. The chemical structure of SU8 enables high aspect-ratio structures to be achieved [76], and recent new formulations allow improved adhesion to substrates including silicon. Multiple sequential exposures can be used to generate 3-D structures in SU8. One such example is given in Fig. 22. SU8 has been used as a mechanical material [77], as an optical material [78] and is commonly used in soft lithography processes for the fabrication of master molds for microfluidic, lab-on-chip and organ-on-chip devices.

Polydimethylsiloxane (PDMS) is a silicone-based elastomer dominant among soft mechanical materials used in microfluidics and related devices. This is due to its wide availability, biocompatibility, optical transparency, oxygen permeability, stiffness tuneability, and covalent bonding with silicon dioxide and glass mediated by oxygen plasma treatment. Its ease of use by casting or spinning makes PDMS a common choice for fast prototyping of single-layer devices by soft lithography [80]. Moreover, off-stoichiometric and surface-functionalized formulations of PDMS are available, which overcome some limitations of PDMS for biomedical applications [81]. Use of PDMS for fabrication of more complex (e.g. multi-layer) devices and in combination with other, particularly non-polymeric materials is less straightforward. A case of wide interest is the embedding of metal tracks (*e.g.*, TiN) onto PDMS to be used as *e.g.* microelectrodes. In this regard, polyimide (PI) layers can be interposed, both to improve metal adhesion upon oxygen plasma surface activation on PDMS and as stress buffer to match the higher mechanical stiffness of metals. The latter can avoid deleterious consequences such as wrinkling and warpage [82], [83]. PI can be formulated as adhesive in tape form (commercially known as Kapton), besides as photo-patternable photoresist. PI is also employed as well structural layer in advanced MEMS processes involving suspended, bulk micromachined silicon islands (see also Section IV.D) [84], and in out-of-plane deployment of 3-D structures by thermally-induced self-folding [85].

More generally, polymers can be a good option when developing flexible devices. They can be deposited onto a wafer, after which most (or all) of the substrate is removed. This yields a flexible device with active and passive components. A range of polymers has been applied to mechanical

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structures [86], thereby including medical probes or microneedles [79].

The simplicity and low-cost of polymer processing make it a good candidate for rapid prototyping [87]. For instance, the molding process used in *e.g.* soft lithography for microfluidic devices is such that, once the mold has been made, multiple copies of the same device can be produced cheaply and rapidly. The low-cost aspect is important since many of these devices are disposable [88].

Hydrogels [89] are a family of highly soft and water-rich polymer networks, which offer many possibilities in bio-MEMS and sensing [90], [91]. One application is based on the expansion of a hydrogel in the presence of CO_2, whereby the measurement of the expansion yields a CO_2 sensor [92]. Hydrogels have also been shown to be good materials for glucose sensing [93], [94], and can also be applied to MEMS structures [95].

There is increasing interest in polymer as a material for electronics. Polymers such as *e.g.* polyvinilidene fluoride (PVDF) are exploited for their piezoelectric properties [96], [97]. Polymers can additionally have conductor and semiconductor properties. An example of the former is PEDOT:PSS [98], which is electrically conductive and can be made locally resistive by UV illumination [99] or electrochemical over-oxidation [100]. PEDOT is also an interesting material for in-vivo devices [101]. Concerning semiconducting polymers, they can be used to fabricate diodes [102]. Moreover, interest in cheaper light-emitting diodes (LEDs) motivated a rapid development towards polymer-based LEDs and polymer-based electronics [103]–[105].

Spin coating is the method of choice to deposit thin layers (*i.e.*, up to tens of micron) of photoresists, polymers and resin materials with reproducible thickness on flat substrates. The final thickness mainly depends on spin parameters (duration, speed profile), polymer characteristics (density, viscosity, solvent type and content), and on polymer/substrate affinity (wettability). The latter can be effectively enhanced by means of primers and adhesion promoters. Spin coating suffers from surface contamination with particles, and is not suitable when requiring conformal coating over rugged substrates with relatively high topography (*i.e.,* much higher than the layer thickness). In the latter case spray coating is to be preferred if a dilution of the polymer can be formulated which is suitable for spraying. Dilution with solvent may also imply the need for multiple spray coating steps to obtain relatively thick polymer layers after solvent evaporation, with impact on the throughput of the technique. It should also be noted that spin and spray coating do not make efficient use of the materials to be deposited, since much the material is lost during process.

General requirements for polymer processing entail degassing, wetting, curing and contamination control. Removal of gasses from polymer matrices, before or after their deposition, is conducted in desiccators or vacuum ovens, and is needed to avoid later detrimental nucleation of bubbles. Wetting and adhesion of polymers deposited over substrates, and particularly onto hydrophobic polymer surfaces, can be enhanced by exposure of the latter to mildly oxidizing atmospheres, such as provided by low-power oxygen or UV plasmas. It should be noted that the effect of such surface treatments is only temporary, as most polymers recover their native hydrophobicity in tens of minutes. Conversely and similarly to stiction avoidance in MEMS, polymer adhesion to substrates can be prevented, as required for *e.g.* repeated uses of master molds in soft lithography, by pre-treating the substrates with low-energy chlorinated or fluorinated surface chemistries. These can be provided by thin passivating layers (*e.g.*, Teflon-like fluoropolymer films, as deposited during the Bosch process) or by vapor phase-deposited silane-based self-assembled monolayers (SAMs) [105]. Room or mild temperature (60 °C to 110 °C) curing is typically used to remove residual solvents and complete cross-linking of the polymers. An extended curing time (*e.g.*, overnight or several days) at room temperature leads to the best results in terms of layers stress release and surface smoothness, which can be traded off with fabrication throughput by rising the curing temperature. Finally, while surface cleanliness is mandated to obtain high-quality and reproducible material interfaces, hydrophobic polymers are additionally highly susceptible to absorbance and uncontrolled release of small hydrophobic particles and molecules (*e.g.*, nanoparticles, drugs). This needs to be considered in their application to biomedical devices, both *in vitro* (*e.g*. organ-on-a-chip) or *in vivo* (*e.g.*, implantable and wearable devices). For *in vivo* applications, polymers such as vapor-phase deposited parylene [107] and polyurethanes [108] can be used as coating or encapsulation layers to protect the body from the device.

C. Graphene

Graphene is a single atom layer of sp^2 hybridised carbon with unique electrical, optical, and mechanical properties [109]. Due to its thickness and properties, there has been a large interest in graphene for sensors and membranes [110]–[112]. Beside single-layer graphene, also double-layer graphene and few-layer graphene ($\leq$10 layers) are of interest for MEMS devices.

The first graphene samples were fabricated using mechanical exfoliation (a.k.a. the scotch tape method). While this process results in a high-quality material, it cannot be scaled up to high volume production. Other methods for graphene synthesis, like liquid exfoliation in combination with printing [113], epitaxy on SiC [114], and CVD on metal catalysts [115], provide more scalable fabrication methods. Of these methods, CVD is widely regarded as the most promising in terms of scalability, while maintaining excellent control over the material quality and composition.

The CVD process typically uses a metal foil or thin film as catalyst (e.g. Cu, Ni, Pt, Mo, Ru) in combination with a carbon feedstock (typically CH_4 diluted in Ar and/or H_2) at temperatures around 1000°C. Graphene nucleates by an isothermal process (e.g. Cu) which is often self-limiting and/or by supersaturation of the metal catalyst with carbon followed by precipitation during cooling (e.g. Ni) [116]. After deposition, the graphene usually resides on top of the catalyst film.

Removal of graphene from the catalyst is one of the biggest challenges in integrating graphene in a semiconductor process.

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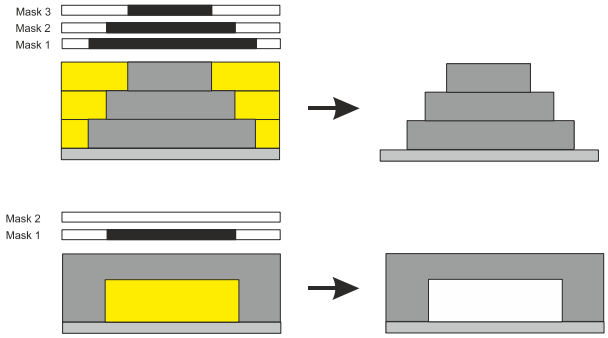

Fig. 22. Schematic of multiple exposure with SU8; (a). In (a) three masks are used with different energies to make the pyramid structure. In (b) the same technique is used to make a bridge structure (Based on [79].)

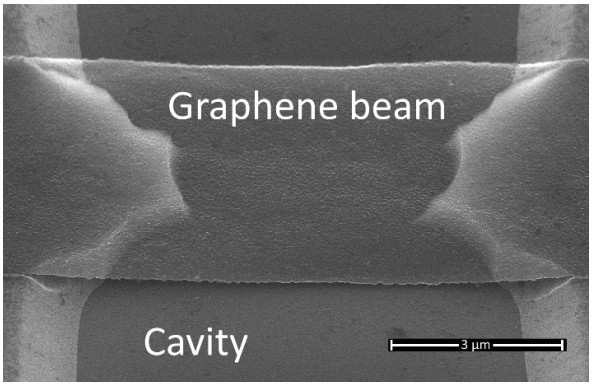

Fig. 23. Suspended graphene beam over a trench etched in SiO_2 [119].

Typically, a transfer technique is used whereby the graphene is coated with a polymer like PMMA, after which the graphene is removed from the catalyst, for instance by wet etching the catalyst, and subsequently transferred in a wet or dry ambient on top of the target wafer [72]. Finally, the polymer is removed using an organic solvent (e.g. acetone), and further post-processing of the graphene is performed. Challenges here are possible polymer contamination, damage to the graphene layer, scaling, and the adhesion of the transferred graphene which sticks to the wafer by van der Waals forces. To circumvent these challenges some groups have explored techniques that circumvent transfer by removing the catalyst thin film from directly underneath the graphene [117], [118]. Graphene is typically patterned by either pre-patterning the catalyst or by using an O_2 plasma after transfer. Using surface and bulk micromachining suspended graphene structures have been realized (Fig. 23) [119], [120].

D. Carbon Nanotubes

Carbon nanotubes (CNT) can be visualised as rolled-up sheets of graphene. Depending on the number of walls, CNT are either single-walled, double-walled or multi-walled. Many of the properties of CNT are like those in graphene, with some exceptions (e.g., optical properties). The chirality of the CNT influences its electrical properties, for instance, certain chiral angles result in semiconducting tubes. At this moment it is, however, not possible to fully control the chiral angle during nucleation although much research has been performed on this [121]. CNT can be, among other applications, used for electrodes [122], sensors [123], NEMS [110], [124] and MEMS [125], [126].

CNTs can be created using arc-discharge and laser ablation, but by far the most popular method is CVD. Here, transition metal catalyst nanoparticles (typically Fe, Co or Ni) are used together with a carbon feedstock (e.g., CH_4, C_2H_4, C_2H_2; diluted by Ar, N_2 and/or H_2) and temperatures between 350-1000 °C, where the material quality depends on temperature [127]. The nanoparticles are formed from dewetting of a nm-thin metal film upon heating or are directly deposited on a substrate. Metal powders can be used in case of bulk production. The CNT nucleate from the nanoparticles, with the nanoparticle either sticking to the base or being lifted by the CNT [128]. Bulk produced CNTs can be formed into a (purified) suspension by using an organic solvent [129] and then coated over a wafer. Dielectrophoresis can be used to control their orientation [130].

By patterning the catalyst film selective growth can be achieved (Fig. 23). On Si wafers it is necessary to deposit a diffusion barrier underneath the catalyst. For this, materials like Al_2O_3, SiO_2, or TiN are used as they have a low surface energy with respect to the catalyst which aids in the formation of nanoparticles by Oswald ripening [131]. When the nanoparticles are close enough the CNT interact and self-align by Van der Waals forces, creating a CNT forest, Fig. 24. Otherwise, the CNT grow in a random direction. It is also possible to force CNT to grow horizontally, for instance by using terraces on the wafer or a horizontal electric field [132]. Nanotubes in a CNT forest interacts weakly and therefore are mechanically soft. By coating the CNT with CVD layers their mechanical robustness can be tuned [133].

E. Biodegradable MEMS

With temporary biomedical implants there can be great advantages if the device/system is resorbed into the body. An implant after an operation can give valuable feedback to the doctors on the success of the operation and the healing process. These devices have a useful lifetime or around 1-2 weeks. It is not desirable to perform a second operation to remove the device, but if the device remains in the body for more than 30 days, the FDA regulations are far stricter. Biodegradable sutures are widely used for internal wounds. In terms of metals, much effort has been directed towards non-corrosive metals. However, materials such as magnesium have been used as biodegradable metals for more than 200 years [134]. Also, a number of iron alloys are now being used in implants, designed to be absorbed by the body [135]. There is an increasing number of biodegradable polymers and polymer composites being used in implants [136]. Furthermore, with the development of organic electronic devices comes the possibility of implantable electronic circuits which will be absorbed by the body once their useful life is finished [137], [138].

IV. Additive and New Processes

Together with new and alternative materials, new techniques have been introduced to further expand the options in microsystem processing.

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A. Integrated MEMS

Once MEMS structures could be made using silicon technology, the interest in combining the two technologies increased, leading to integrated MEMS. There are many options and many limitations. Macro-porous silicon usually requires n-type silicon [44], although it is possible to achieve macro-pores in p-type silicon, but with less control over the structure [139]. Most other bulk micromachining processes are low temperature and can be performed after a standard CMOS/bipolar process [140]. Surface micromachining is more complicated. There are three approaches:

1. Pre-processing
   Additional layers are deposited before standard processing and only the sacrificial etching performed as post-processing.
2. Integrated (co-) processing
   The wafers are removed from the standard line for additional (MEMS) processing and then returned to finish the IC processing
3. Post-processing
   The micromachining process is performed on fully processed ICs.

An example of pre-processing was shown by Sandia labs [141]. A pit is etched into the silicon, after which micromechanical structures are formed. They are not released, but covered with silicon dioxide and the wafer is planarized. This wafer then goes through the standard IC processing, after which the mechanical structures are released. To use this technique, it is essential to ensure that all materials used are compatible with the IC process and will not cause any contamination. Secondly, the process of the mechanical layers has to be developed to ensure that they have good mechanical properties after the high thermal budget of the IC process.

For integrated processing, the stage in the IC process when the micromachining process will be performed has to be chosen. One example is to do this before the aluminum processing. This will allow a maximum temperature of the micromachining of around 850 °C (depending on the IC process) [142], [143]. This does require full access to the IC process, and the materials used need to be suitable to return to the last stages of the IC processing.

Post-processing gives the most flexibility of materials used, since the wafers will not return to the line. However, this comes with the greatest limitation in thermal budget (usually around 400 °C). An alternative approach is to use another metal, rather than aluminum, which can withstand the higher temperatures of the additional processing [59]. There are many examples where this approach has been used. In some cases, the materials used in the IC process are used for the micromachining [144], [145]. In this case, no additional thermal processing is required. However, the materials might not have the desired mechanical properties and processing may have to be adjusted, or the designs are made to work with this issue. Additional layers with process temperatures lower than 400 °C (*e.g.*, polySiGe) have also been used. The TI mirror arrays use aluminum layers for the mirrors [146]. In others additional layers are used to complete the process. PECVD layers can be deposited at temperature below 400 °C. PECVD SiC has been found to have the required mechanical quality and is also chemically robust [147], [148].

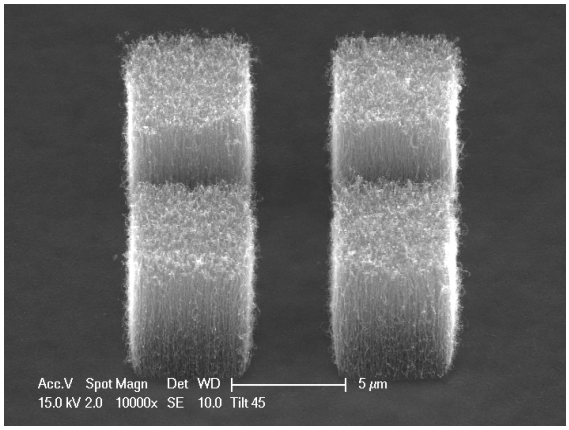

Fig. 24. Bundles of vertically aligned CNT grown by CVD using a pre-patterned catalyst.

B. Screen Printing & Inkjet Printing

Screen printing and inkjet printing are established technologies which are finding increasing use in MEMS technology. Screen printing has long been used for thick-film devices [149]. The basic process is shown in Fig. 25. A wide range of materials are available in the paste form including conductors, resistors, insulators and piezoelectric layers (ceramic and polymer).

The basic idea of inkjet printing (IJP) dates back to 1905, and inkjet printing was a leading technology in color printers for home use. Most printing nozzles use either thermal or piezoelectric microactuators for droplet generation. The high-frequency actuation excites standing waves within the ink column, whose energy overcomes the surface tension of the free ink boundary at the open nozzle end to generate monodisperse droplets. Although the resolution of IJP may not be as high as in modern lithography, it is sufficient for many microsystem applications. IJP lends itself naturally to the fabrication of hemispherical and rounded 3-D geometries for *e.g.* lenses [150] and capsules [151], and to local deposition of small nanoparticle suspension volumes; moreover, drop-on-demand IJP makes very efficient use of ink materials. The nozzle and printing process are illustrated in Fig. 26 [152].

C. 3-D Printing

Adding materials on a substrate or object can have many implementations (such as inkjet printing), however, its most popular form is 3-D printing. In this technology an object designed in a suitable 3-D CAD environment is digitally sliced in many layers. These layers are eventually split up, depending on the nature of the 3-D printer technology, in either voxels (volume elements) or traxels (track elements) [153]. 3-D printers that work based on voxels are, for example, the poly- or multi-jetting printers, where materials are printed using printheads consisting of multiple nozzles ejecting small droplets of structural material or binder material on a powder-bed, or vat-polymerisation printers, which make layers by scanning

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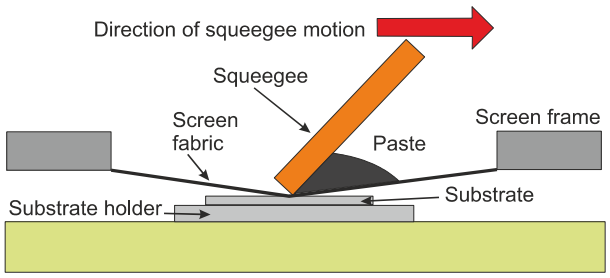

Fig. 25. Basic screen-printing process. Adapted from [149].

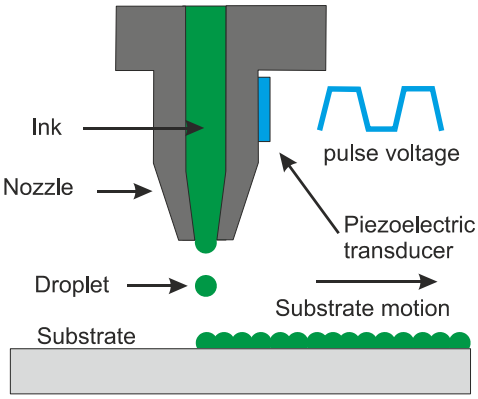

Fig. 26. Basic inkjet nozzle (Adapted from [151].)

laser-beams or by using a Digital Light Processor (DLP) chip to illuminate and (UV) photo-polymerize certain thin layers of resin. Other examples are selective laser sintering and binder-jetting 3-D printers. 3-D printers that work by fusing of traxels are extrusion based such as fused deposition modelling (FDM), also called fused filament fabrication (FFF). In this method a solid filament, often of polymer nature, is fed by means of an extruder into a heated chamber where the filament is molten and pushed out through a nozzle by the pressure generated by the filament feed. The molten filament solidifies when exposed to the lower temperatures outside the heated nozzle and, when under the proper conditions, will bond to underlying and neighboring traxels, eventually forming a solid object.

Important aspects of 3-D printing are the resolution, the maximum build volume and the build speed. High-resolution, (i.e. deep sub-micron), 3-D prints can for example be made by two-photon photo-polymerisation in tailored resins. However, this resolution is only available over a relatively small volume. In general, the ratio of smallest to largest dimensions tops off at a few thousand. For example, latest generation vat photo-polymerisation 3-D printers use 4K DLP devices for illumination which, as there are no shifting mechanisms such as in wafer steppers, limits the ratio of smallest to largest lateral dimension to 4000 or less. For FDM this ratio is roughly 1000 (nozzle hole of about 0.3 – 0.5 mm, working area about 30 – 50 cm). However, often the resolution in the z-direction, this is the direction normal to the layers, can be much smaller, around 25 – 50 μm for FDM. Moreover, the accuracy of the displacements of the print-bed in x and y-directions is generally as small as 10 – 25 μm. Fig. 27 shows a simplified tree of various properties and types of 3-D printing, limited to these that are of interest to electro-mechanical structures.

The most important requirement for 3-D printing of functional structures is the ability to print multiple materials in a single object. Obviously, for sensing and actuation properties the minimum requirements are to have at least one conductive and one dielectric material which do bond well to form mechanically stable devices. Additional materials of interest are those that can enable specific sensing functionality such as piezoresistive (most carbon and silver filler-based), piezoelectric (PVDF), thermo-resistive (virtually all conductive materials) and magnetic materials.

Due to the multi-material requirement FDM is used often for research on 3-D printed functional structures, as it is relatively easy to make specialty filaments and there exist reasonably proper mechanical solutions for multi-nozzle deposition [154]. Suitable combinations of materials are often obtained by doping an existing polymer filament with silver particles or some form of carbon [155], e.g., carbon black (particles of tens to hundreds of nanometer diameter) [156], graphite, graphene, carbon nano tubes. The doping should be sufficiently high that percolation networks can be formed to enable sufficient conductivity, while remaining low enough to not affect the printability substantially [157]. This balance results in resistivities on the order of 10 – 1000 Ωcm, subject to printing, curing and annealing conditions and the direction in the eventual printed part. Examples of such materials are thermoplastic polyurethane (TPU) [158] and polylactic acid (PLA) [159], which can be combined in doped and undoped versions.

In order to increase the conductivity of certain parts in a print, combinations of extrusion based and deposition-based printing are seen; *e.g.* in FDM printers equipped with an additional dispenser of conductive ink (Liquid Deposition Modeling, LDM). Such inks often consist of solutions with Ag or Au particles and curing may be by UV or thermal treatment. The extruders can be for example pneumatic, syringe, or progressive cavity based [154]. For biocompatible devices one may look into PEDOT:PSS. This conductive polymer may be included in the 3D printing process in a variety of ways [191], [192], where a special interesting one in the context of FDM is its use in the form of FDM printable filament [193].

To increase complexity of 3-D printed structures one may add support material to the object which is used only to provide structural stability during the 3-D printing process. The materials of choice are polyvinyl alcohol (PVA) or butenediol vinyl alcohol copolymer (BVOH) which can be relatively easily dissolved in water. This is conceptually comparable to the sacrificial layer etching in surface micromachining.

Combination of 3-D printed parts with electronics is still in its infancy. Generally, 3-D printers are not equipped with registration detection and control, implying that depositing material onto wafers or dies is currently not feasible, at least not in commercial 3-D printers. The other way around, researchers have developed elaborate robotic systems in which 3-D printing is interrupted at set states of fabrication to insert electronic parts in the host structure, together with the

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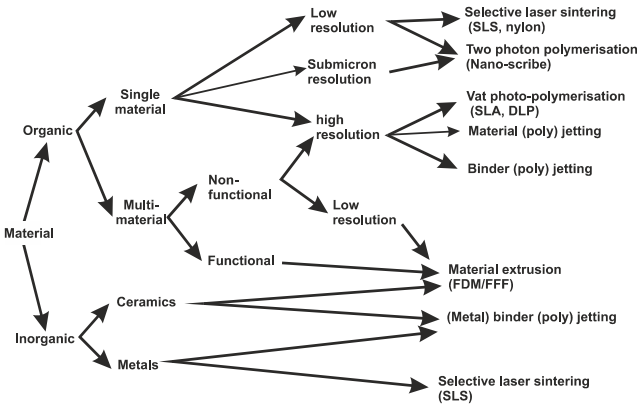

Fig. 27. Simplified tree for 3-D printing methods for electro-mechanical structures.

necessary electrical connections, *e.g.* by rolling in copper strips and soldering them to the chips [26].

Examples of 3-D printed devices are accelerometers [160], [161], optofluidic temperature sensors [162], flexible capacitive sensors [163], resonant circuits where the resonance frequency depends on food freshness [25], electrical structures for micro cube-satellites [164], [165], electrical switches [166] deformation sensing in shoe-soles [167], phononic band-gap structures [168], force-sensors [169], sEMG sensors [170], a complete miniature pump (using assembly of magnets) [171] and flow sensors [172]. Many more examples can be given, however, much of the publications up to date primarily represent research, with few devices found in actual commercial products. Indeed, this is what can be expected from 3-D printed products: they are not easy to make in large numbers and will easily be less cost-effective than parts that can be made in large numbers, such as by wafer-scale micromachining or molding. However, where 3-D printed parts will be most interesting is in small number series and fully customized parts, such as in medical applications and replacements for obsolete parts. In these situations, the relatively low price of single 3-D printed components as the enabling part may be very cost-effective.

D. Flexible Device Fabrication

Flexible devices have found a wide range of applications. Flexible displays require the display and the electronics to be flexible. In the field of medicine, flexible (and sometimes stretchable) devices allow systems to mold to the shape of the body or organ. There are a number of possible fabrication approaches.

1. Depositing flexible materials on the silicon and then removing the silicon at the end of the process.
2. Creating rigid silicon islands connected by flexible hinges.
3. Creating complete devices in flexible materials.

A very simple example of the first option is given in Fig. 28. There are a number of options for the flexible material, which will later form the main substrate. Many of these are polymers, which can be spun onto the wafer. The basic process is as follows: (a) is standard processing after which the flexible

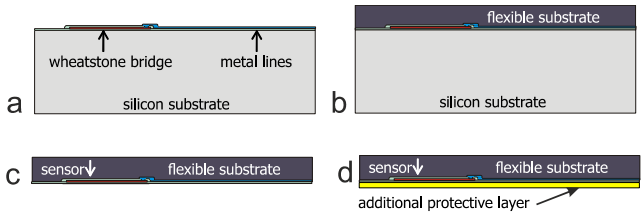

Fig. 28. Simple process for flexible device.

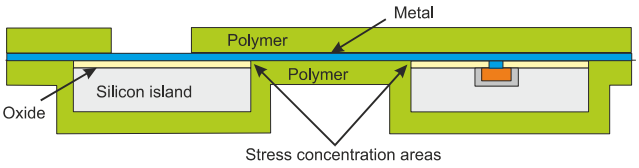

Fig. 29. Cross-section of a flex-stiff structure (Adapted from [174].)

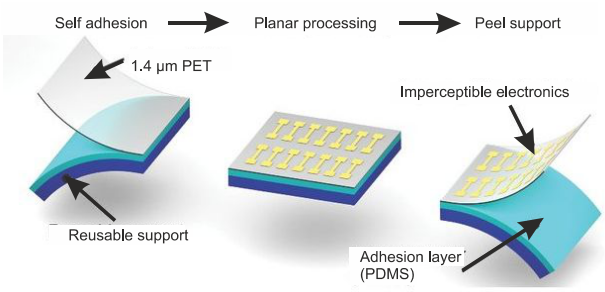

Fig. 30. Fabrication of flexible electrode arrays (Adapted from [175].)

material is deposited (b). The substrate is then removed to leave a flexible device (c), after which an additional protection layer can be added (d) [173].

The second approach is to etch through the silicon locally to create stiff islands. This can be the full thickness of the silicon or thinned areas separated by flexible hinges. A cross-section of such a device is given in Fig. 29 [174]. As with Fig. 28, the first part is standard processing, followed by the deposition of the flexible layer. The difference here is that areas of silicon are left, which remain stiff during operation. It is important to define the silicon islands. For this there are a number of options. If the silicon islands are n-type, the electrochemical etch-stop, described above, could be used. A backside mask could also be used. If the backside mask thickness is correctly calculated, this will be removed during the etching. The etching will continue, maintaining the profile and thus the island structure is formed. If using dry etching the etch could stop on an oxide layer leaving the islands

The third approach is to complete the full process in flexible materials. This may use a support during processing as shown in Fig. 30 [175]. The device in Fig. 31 is fabricated on a PDMS/Polyimide substrate [176].

Many options have been developed to make flexible/organic devices. Processes using organics have been developed for transistors and solar cells. One such process is shown in Fig. 32 [177]. Many of these flexible materials can be formed through spinning, which is a simple process. Polymers can also be formed using screen-printing.

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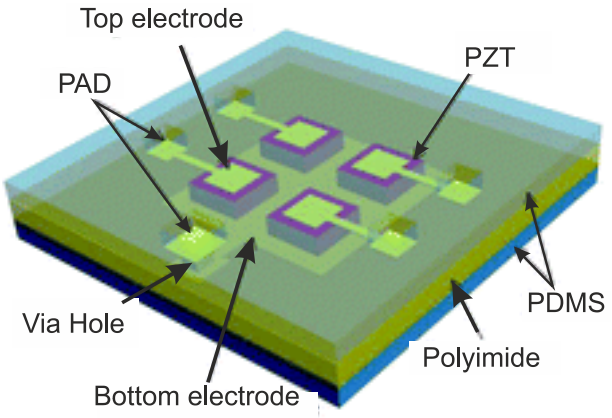

Fig. 31. Flexible device with PDMS/Polyimide substrate. Adapted from [176].

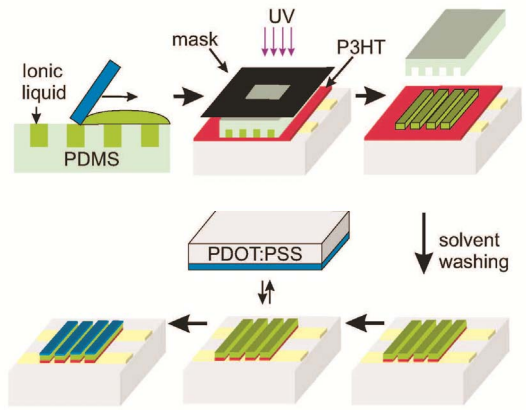

Fig. 32. Process flow using screen printing (Adapted from [177].)

Fig. 33. Interconnect design for flexible/stretchable devices.

In some cases, the substrate needs to be stretchable as well as flexible. This can present several additional challenges. Stretching can create stress concentration around the interface between the stiff sections and the flexible sections. Also, any conductive interconnects need to stretch with the device. There are two options. One is to use a conductor which is stretchable. The other is to design a structure to enable stretching. This type of structure is shown in Fig. 33. Any stress due to stretching will be released in the curves and not result in cracking of the metal lines.

The active components in the device also must be stretchable [178].

An example of a process combining SU8 as flexible material and CNT is given in Fig. 34 [179].

The process starts with a silicon wafer with an omnicoat as sacrificial layer (a). Gold is added (b), followed by the CNT/SU-8 mix (c). A SU-8 layer is spun-on (d) with a second, much thicker, layer (e). Finally, the SU-8 structure is release

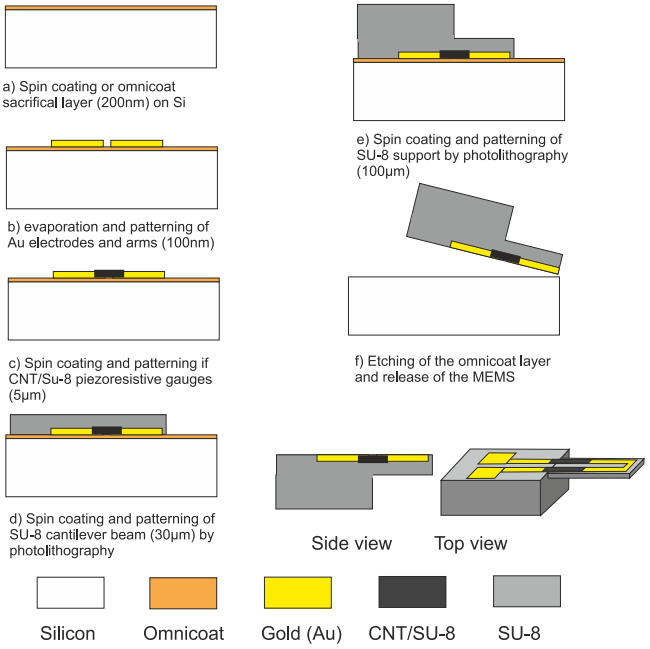

Fig. 34. Fabrication process of a hybrid piezoresistive MEMS stain sensor (Based on [179].)

to yield the final device. The gauge factor of the CNT/SU-8 resistors was found to be 200.

V. Conclusion

Processing for micromachined devices requires adaptations of standard processing techniques, and in some cases totally new techniques. These can be using conventional IC materials, or materials not usually found in the IC processing. Furthermore, many relevant applications often require the design and fabrication of three-dimensional electro-mechanical structures, which is not straightforward to achieve based on an inherently 2-D technology, as dictated by the use of photolithography as patterning method.

The development of bulk and surface micromachining showed how this could be achieved. Recent developments have brought old technologies, such as screen printing, again into use, and added new additive manufacturing technologies such as inkjet and 3-D printing to the toolset. 3-D printing allows to fabricate complex structures by programming a suitable printer to deposit materials in a layer by layer fashion. This enables rapid prototyping at a low cost and low throughput, and opens up interesting possibilities. In medical applications, as an example, 3-D printing of prototypes allows quick iterative adjustments of a design to adapt to the needs of a patient, before eventually scaling up the production of the final device.

Polymers recently found greater use with the development of microfluidics and its specialized derivations, where the cost of production had to be low since many of the devices were disposables. Many of these polymers are also biocompatible, (for many in-vivo applications) yielding advances in medical implants for in-vivo applications and in organs-on-chip for in-vitro applications. Materials such as SiC and graphene are extremely chemically robust, which enables them to be used in

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harsh environments and as sensing materials for gasses which would conversely attack standard IC materials.

In this paper we have provided an introduction and state-of-the-art for all of the above to the reader interested in appreciating the landscape of available solutions for IC and MEMS microfabrication. It is to be expected in turn that ever new drivers and applications will keep the microfabrication toolbox updating and expanding. Interesting directions currently under rapid development, and expected to require significant contribution from and trigger new developments in M/NEMS and related material processing technologies. include advanced human/machine interfaces [180], wearable electronics [181] in the form of health screening appliances and electronics-laden textiles [182], ubiquitous computing powered by distributed networks of sensor nodes, ingestible electronics [183] as complement or alternative to endoscopic screening or surgery, and soft robot(ic)s [184] for access, exploration and mapping of harsh unstructured environments and for safer interaction with humans.

Finally, it is wished that future developments of M/NEMS and of micro/nanoelectronics more generally may also consider environmental friendliness, sustainable sourcing of materials and energy, and circularity in the economics related to the design of devices, choice of materials and their processing, and planning of their full life cycle including recycling. As the diversity and ubiquity of micro/nanosystems and devices is expected to grow further, the conception and implementation of a more sustainable scenario poses interesting constraints and additional challenges for a new generation of technology creators.

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