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A Load Insensitive Doherty Power Amplifier with better than −39 dBc ACLR on 2:1 VSWR Circle using a Constant 50 Ω Trained Pre-distorted Signal

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***Abstract*— This paper presents a low-loss load-insensitive Doherty power amplifier (DPA) technique. The proposed DPA is insensitive to ohmic load variation by adjusting its supply voltages and input drive of the main and peaking stages in a mirrored approach. Moreover, a low-loss tunable matching network (TMN) is employed to cancel out any reactive part of the load. To validate this technique, a printed circuit board (PCB) based demonstrator consisting of the Doherty PA, a six-port reflectometer, and a tunable shunt resonator have been fabricated. When subjected to a 50 Ω load, at the 1 dB compression point, the DPA delivers an output power of 32.3 dBm with a power gain and peak drain efficiency of 14.6 dB and 61 %, respectively. When the DPA is driven with a pre-distorted 64-QAM 4 MHz signal optimized for the 50 Ω loading condition, it delivers 24.4 dBm at 41 % average drain efficiency, with EVM/ACLR −40.9 dB / −46.9 dBc. Subsequently, when subjected to a 2:1 VSWR over a 0°-360° mismatch trajectory, using the unaltered 50 Ω DPD correction, it is capable of delivering an output power of 24.4 ± 0.1 dBm with a 34 − 39 % drain efficiency while maintaining an EVM/ACLR better than −32.3 dB / −39.3 dBc for all load conditions.**

***Keywords*— self-healing transmitter, VSWR, control circuit, Doherty, six-port reflectometers, and tunable matching networks.**

I. Introduction

The ever-growing demand for higher data rates has led to the use of spectrally efficient complex modulated signals, which are characterized by a high peak-to-average power ratio (PAPR). To amplify these signals in an energy-efficient manner, envelope tracking (ET) and Doherty power amplifiers (DPA) are employed. ET-based transmitters utilize fast dynamic supply modulators, which can provide good performance for signals with a limited modulation bandwidth (< 40 MHz). Consequently, DPAs are typically preferred when operating with signals that have both high PAPR, and modulation bandwidth. However, DPAs are very sensitive to load impedance variation [1] and therefore are rarely found in handset or phased array applications. In a handset terminal, the changing antenna environment is the cause of PA load mismatch conditions [2]. While in phased-array systems, the (unwanted) mutual coupling between the antenna elements, in combination with the changing relative phases needed for the beam steering, cause loading variation [3]. A tunable matching network (TMN), in theory, can correct for these varying VSWR conditions [2]. However, correcting for arbitrary complex loads for a given VSWR range causes high insertion loss, defeating the potential benefits [2]. In contrast, this work exploits a combination of supply voltage and input drive adjustments to handle the ohmic load variation [4], [2], along with a low loss TMN/tunable shunt capacitor to compensate for the varying reactive part of the load [2], as such enabling truly load-insensitive DPA operation over a given VSWR area (see Fig. 1). The DC-DC supply modulators are considered not to be within the focus of this research. Since they only need to trace the slow varying VSWR conditions (they do not track the modulation envelope) and can be realized with very high efficiency (e.g., 98.4%) [4]. This work provides the following contributions. Firstly, compared to [4], for the first time on a DPA, 0°-360° VSWR detection and full correction are demonstrated. Secondly, it is theoretically shown the proposed technique applies to both symmetrical and asymmetrical DPAs. Thirdly, DPD correction no longer needs to be adjusted/updated for changing loading conditions in the proposed load-insensitive DPA approach. The latter statement is demonstrated by evaluating the DPA linearity over the full 2:1 VSWR circle while using a fixed DPD correction set pre-trained on a 50 Ω load condition.

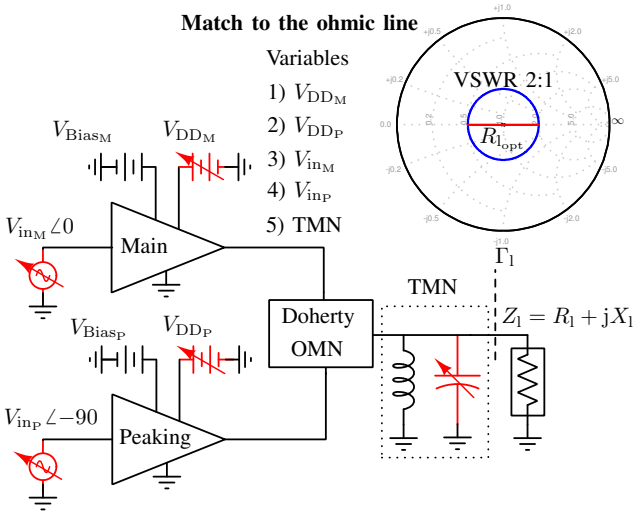

Fig. 1. The proposed low-loss load-insensitive Doherty PA consisting of a tunable input drive, supply voltage and tunable matching network.

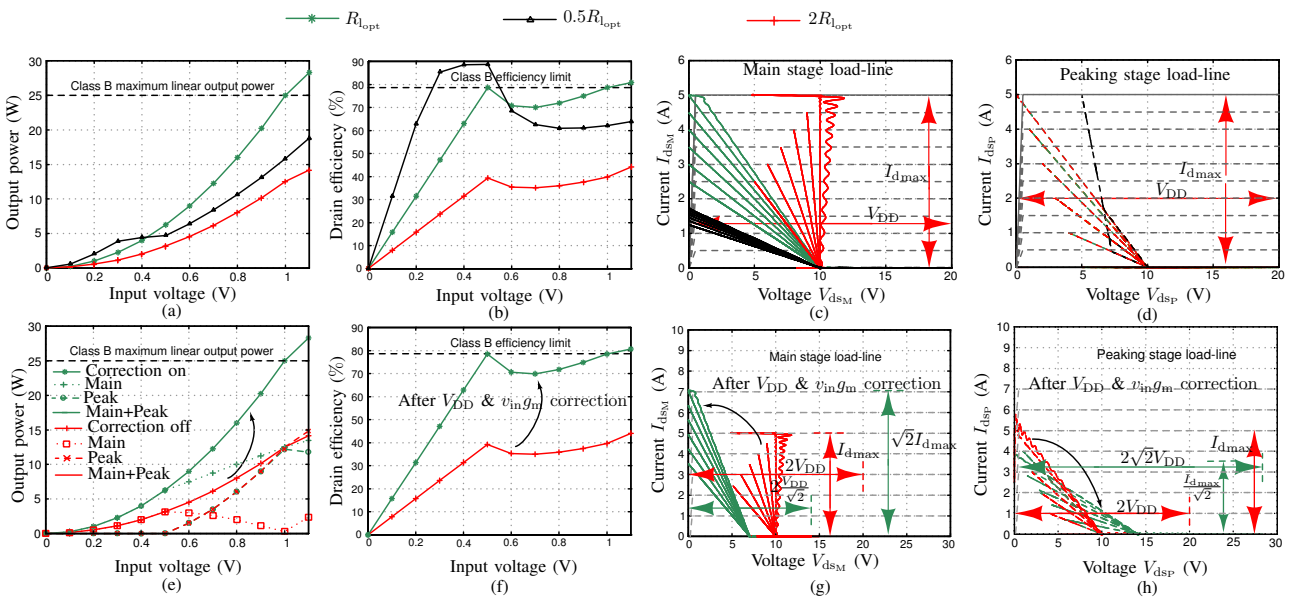

Fig. 2. DPA performance in terms of: (a) output power, (b) drain efficiency, (c) load-line of main output stage, and (d) load-line of peaking output stage, for R_l=$R_{l_{opt}}$(green), R_l=2$R_{l_{opt}}$(red), and R_l=0.5$R_{l_{opt}}$(black). DPA performance in terms of (e) output power, (f) efficiency, (g) main stage load-line, and (h) load-line of peaking output stage, when applying the mismatch condition ($2R_{l_{opt}}$) without (red) and with (green) the proposed correction-technique.

$$\begin{bmatrix} V_M \\ I_M \end{bmatrix} = \begin{bmatrix} \cos(\beta l) & jZ_0\sin(\beta l) \\ \frac{j\sin(\beta l)}{Z_0} & \cos(\beta l) \end{bmatrix} \begin{bmatrix} V_P \\ jI_P + \frac{V_P}{R_l} \end{bmatrix}$$

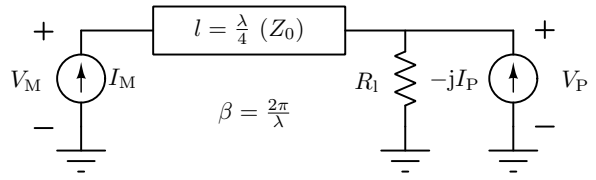

Fig. 3. An ideal Doherty PA.

II. Load-Insensitive DPA Theory

Fig. 3 illustrates an ideal conventional (asymmetrical) two-way DPA using identical supply voltages (V_{DD}) and unequal currents for its main (I_M) and peaking device (I_P). The impedance seen by the main device for a given power back-off point (α) is given by,

$$Z_{M(R_l=R_{l_{opt}})} = \frac{R_{l_{opt}}^2}{\alpha^2 R_l} - \frac{R_{l_{opt}}}{\alpha}\frac{I_P}{I_M} \tag{1}$$

When an ohmic VSWR condition is applied the loading impedance R_l will deviate from its optimum value $R_{l_{opt}}$. For a given VSWR value, the ohmic part of R_l will vary from $R_{l_{opt}}/VSWR$ to $R_{l_{opt}}.VSWR$. From (1), we can conclude that e.g. for a symmetric DPA ($\alpha = 0.5$) and $R_l = 2R_{l_{opt}}$ at $v_{in} = 1$ (full power), the offered impedance to the main device becomes zero, as such entirely obstructing the desired Doherty operation. This highly sensitive feature of a Doherty amplifier for its provided load is also illustrated in Fig. 2, which relates to the symmetrical DPA ($\alpha = 0.5$) case. In these simulations, the even harmonics are shorted by a $\frac{\lambda}{4}$ transmission line, leaving the odd harmonics somewhat uncontrolled. This arrangement represents the actual circuit implementation used in section III. Also note that, when R_l = 0.5R_{opt}, the main voltage clips much earlier than in the nominal case. Consequently, I_M will not keep up with I_P in a practical circuit, causing the peaking device impedance ($Z_P = V_P/I_P$) to move towards the short-circuited condition.

A. Solution

To alleviate the Doherty amplifier for ohmic mismatch due to R_l deviations and restore its basic properties in terms of output power ($P_{out,max}$), and efficiency vs. power back-off, the following expressions are derived.

$$V_{DD_M,R_l} = V_{DD_M,R_{l_{opt}}}\sqrt{\frac{R_{l_{opt}}}{R_l}} \tag{2}$$

$$I_{M_{max},R_l} = I_{M_{max},R_{l_{opt}}}\sqrt{\frac{R_l}{R_{l_{opt}}}} \tag{3}$$

Note that both the V_{DD_M} and $I_{M_{max}}$ have been modified to handle the new R_l and provide the same power for the main device in the power back-off point. Moreover, the new conditions for the supply voltage and required current of the peaking device are derived in the following equations.

$$I_{P_{max},R_l} = I_{P_{max},R_{l_{opt}}}\sqrt{\frac{R_{l_{opt}}}{R_l}} \tag{4}$$

Consequently, we find (5), which completes our solution for load-insensitive operation.

$$V_{DD_P,R_l} = V_{DD_P,R_{l_{opt}}}\sqrt{\frac{R_l}{R_{l_{opt}}}} \tag{5}$$

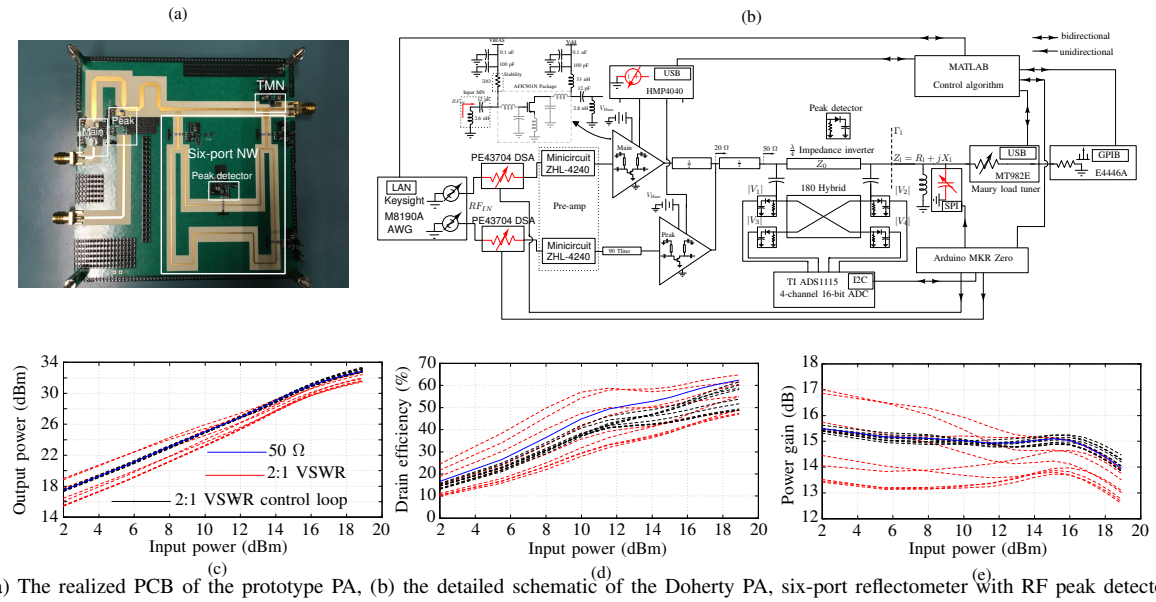

Fig. 4. a) The realized PCB of the prototype PA, (b) the detailed schematic of the Doherty PA, six-port reflectometer with RF peak detectors, and parallel resonator with tunable capacitor. The measurement instruments and the control loop implementation are also shown. DPA performance when the load is matched to the $50\,\Omega$, and on a 2:1 VSWR circle for a phase steps of $45°$ with and without the proposed control loop method. (c), (d), and (e) shows the DPA output power, power gain, and drain efficiency vs. input power.

As an example, simulation results of this recovery procedure when the DPA is subjected to a $2R_{\mathrm{l_{opt}}}$ load impedance, with (green color), and without (red color) adjusting the voltage and drive parameters for the main and peaking device are shown in Fig. 2e, 2f, 2g, and 2h.

III. Design & Measurement

A. Design Details

A load-insensitive Doherty PA prototype ($(R_{\mathrm{l_{opt}}} \approx 15\,\Omega$) capable of delivering $33\,\mathrm{dBm}$ at $900\,\mathrm{MHz}$ is realized, using packaged LDMOS devices (AFIC901N)). In this context, an impedance matching control loop has been designed and implemented on a Rogers RO4350B substrate with $0.508\,\mathrm{mm}$ thickness (see Fig. 4a).

B. Measurement Results

The load-insensitive DPA with its measurement setup is shown in Fig. 4b. The main stage LDMOS device is biased in the desired class-AB mode with $V_{\mathrm{DD_M}}$= $5.0\,\mathrm{V}$ yielding $I_{\mathrm{d_q}}$= $44\,\mathrm{mA}$, respectively. While the peaking stage is biased in class-C mode with $V_{\mathrm{DD_P}} = 5.0\,\mathrm{V}$ yielding $\approx 0\,\mathrm{mA}$. It can be seen that the DPA (blue color) has a power gain of $15.5\,\mathrm{dB}$ (see Fig. 4e) and delivers an output power of 32.3 dBm (see Fig. 4c) at its $1\,\mathrm{dB}$ compression point with a $61\,\%$ (see Fig. 4d) drain efficiency when matched to its nominal $50\,\Omega$ load.

1) Control Loop Method

A MATLAB offline trained look-up table (LUT) based control algorithm was exploited in this work. The LUT takes the voltage ratios $\frac{V_1}{V_2}$ and $\frac{V_3}{V_4}$ as input, and returns the optimum setting for the switchable-capacitor bank, as well as, the input drive levels and supply voltages for the main and peak output stages.

a) Single-tone: The single-tone measured DPA output power, power gain, and drain efficiency performance for the load trajectory on the 2:1 VSWR circle, with and without the actuation method, are shown in Fig. 4c, 4d, and 4e, respectively. The performance of the DPA when matched to a $50\,\Omega$ load is added for comparison.

b) Modulated signal: For a 64-QAM $4\,\mathrm{MHz}$ modulated signal, first a simple static AM-AM/AM-PM based DPD was trained for the DPA when connected to a $50\,\Omega$ load, yielding a set of pre-distorted drive signals for the main and peaking devices, which remain unaltered in the following VSWR measurements. Fig. 5a, 5b, 5c, and 5d show the resulting DPA output power, drain efficiency, EVM in dB, and ACLR at $1\,\mathrm{MHz}$ offset for a 64-QAM $4\,\mathrm{MHz}$ signal using this unaltered ($50\,\Omega$ case) DPD correction.

From the single-tone and modulated signal measurements, we can observe that the VSWR control loop, when activated recovers the DPA performance in terms of output power and gain with a variation of less than $\pm$ $0.1\,\mathrm{dB}$ for a linear output power of $24.4\,\mathrm{dBm}$. Furthermore, it can maintain close to constant efficiency and linearity performance, i.e., EVM/ACLR better than $-32.3\,\mathrm{dB}/-39.3\,\mathrm{dBc}$ across the entire 2:1 VSWR circle. The limited degradation in linearity can be traced back to angles with increased changes in AM-PM distortion (see Fig. 5e). The latter can be explained by considering the impact of the non-linear output capacitance (C_{ds}) of the main and peaking devices. Namely, it acts as a catalyst for the output phase distortion. In a practical DPA the output phase is a function of R_{l}, g_{m}, C_{gs}, and C_{ds} (of which C_{ds} has a dominant role) [5], [6]. Consequently, a change in C_{ds} and R_{l} (due to the changing load impedance) yields a change in the phase distortion.

In Table 1, a comparison with state-of-the-art load-insensitive

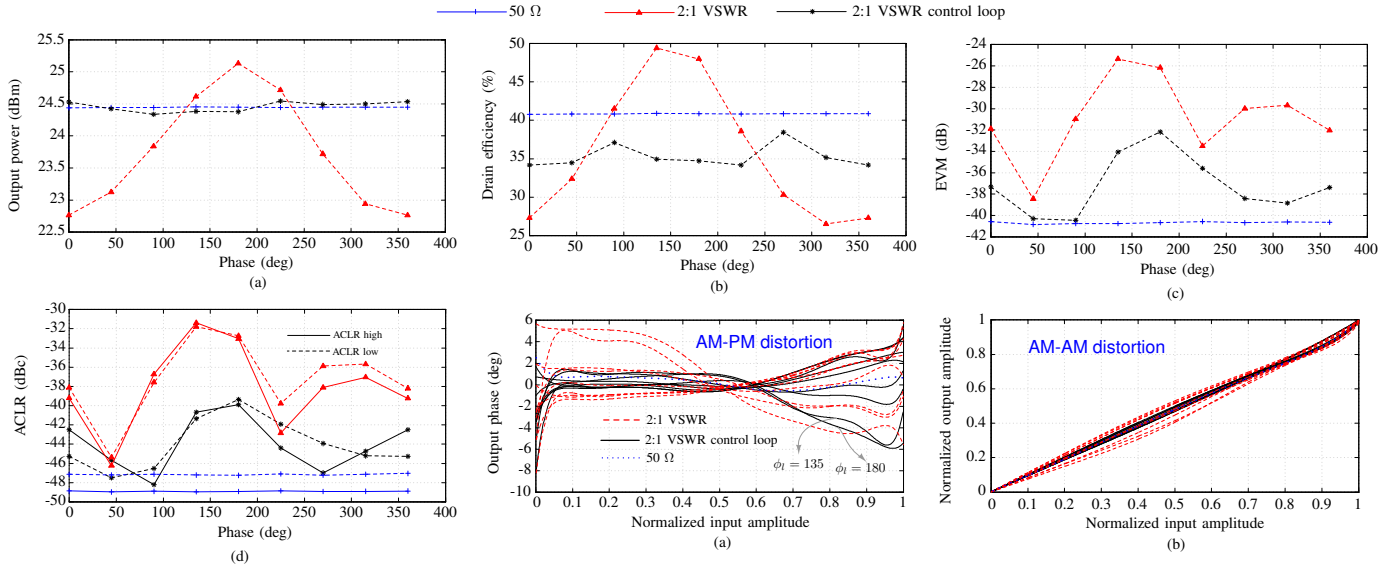

Fig. 5. The DPA performance on $50\,\Omega$ load and 2:1 VSWR circle with and without activation of the VSWR control loop, while, using a $50\,\Omega$ trained pre-distorted 64-QAM $4\,\mathrm{MHz}$ signal with an input power of $9\,\mathrm{dBm}$ (a) output power, (b) drain efficiency, (c) EVM, and (d) ACLR at $1\,\mathrm{MHz}$ offset. Also shown are the DPA (e) AM-PM distortion in degree and (f) AM-AM distortion.

Table 1. COMPARISON WITH THE STATE OF THE ART LOAD INSENSITIVE DPAS

Comparison	**This work**		[7] TMTT-2021		[4] TMTT-2021	
Technique	**Proposed**		QB-DPA ‡		Supply + Input drive-DPA ‡	
Technology	**LDMOS-PCB**		GaN-PCB		GaN-PCB	
Impedance detector	**yes**		no		yes	
Freq GHz	**0.9**		3.5		3.6	
Z_l/VSWR	50 Ω	**2:1**(0°-360°)	50 Ω	2:1(0°-360°)	50 Ω	25 Ω-100 Ω
CW signal	**1-tone CW**		1-tone CW		1-tone CW	
$P_{\mathrm{out}_{1\mathrm{dB}}}$ dBm	**32.3**	**32.3[0.4,-0.2]**	40.7	38.8-40.4	43.5	42.6-43.4
DE/PAE %	**61/60**	**48-59/47-58**	68.4/-	51-59/-	68.0/-	54-64/-
Modulated signal	**64-QAM** 4 MHz		64-QAM 20 MHz		LTE 5 MHz	
DPD	**static**		no		no	
PAPR	7.3		NR		5.5	
P_{out} dBm	**24.4**	**24.4±0.1**	35	33-34.2	NR	NR
DE_{avg}/PAE_{avg} %	**41/40**	**34-39/33-38**	45	32.5-42.5/-	46.4/-	40.2-43/-
$ACLR$ dBc	**-46.9**	< **-39.3**	-41.0	NR	-31.8	<-30.1
EVM dB/%	**-40.9/**	< **-32.3/**	-/1.48	-/1.75-4	NR	NR

‡ results are estimated from plots; NR = Not Reported; † Saturated performance; †† with PA $50\,\Omega$ performance (VSWR 1:1) as the reference, the reflection loss for a 2:1 VSWR will be $0.51\,\mathrm{dB}$;

Doherty PAs is provided. It can be seen that the proposed technique achieves the best performance in terms of constant linear output power with a variation of only $\pm\,0.1\,\mathrm{dB}$, with an average drain efficiency of $\approx 35\,\%$. The linearity performance i.e., EVM/ACLR is better than $-32.3\,\mathrm{dB}/-39.3\,\mathrm{dBc}$ over the entire 2:1 VSWR circle.

IV. CONCLUSION

This paper has demonstrated Doherty PA with built-in self-healing capability for handset or phased array applications. The realized DPA is insensitive to load variation by adjusting its input drive levels and the supply voltages of the main and peaking devices in a mirrored approach, while an adjustable capacitor bank handles the reactive loads. The prototype DPA and LUT-based fully-automated control algorithm was able to recover from the load variations on a 2:1 VSWR circle and could reduce the gain and output power variation to less than $\pm\,0.1\,\mathrm{dB}$ when driven by a complex modulated signal. Furthermore, it was shown that the DPD correction is largely independent of load mismatch over a given VSWR range.

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