A 0.028-mm^2 32-MHz *RC* Frequency Reference With an Inaccuracy of ±900 ppm From −40 °C to 125 °C and ±1600 ppm After Accelerated Aging

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***Abstract*— This article describes the design and implementation of a compact CMOS *RC* frequency reference based on N-type diffusion (N-diff) resistors and metal–insulator–metal (MIM) capacitors. It consists of a frequency-locked loop (FLL) that locks the period of a voltage-controlled oscillator (VCO) to the time it takes a current source to charge a capacitor to a reference voltage. Conventionally, the temperature compensation of such FLLs involves the use of resistors with different temperature dependencies. In this work, however, this is done by using two bipolar junction transistor (BJT)-based current sources with different temperature dependencies to charge a MIM capacitor and generate a reference voltage across an N-diff resistor, respectively. Implemented in a standard 180-nm technology, the resulting frequency reference achieves small size (0.028 mm^2), moderate inaccuracy (±900 ppm) from −40 °C to 125 °C, and low drift (±1600 ppm) after accelerated aging. The versatility of the proposed temperature compensation scheme is validated by replacing the N-diff resistor with a P-poly resistor. However, the latter exhibits greater inaccuracy (+2000/−2500 ppm) and more drift (−2600/−8100 ppm) after accelerated aging.**

***Index Terms*— Accelerated aging, bipolar junction transistor (BJT), CMOS frequency reference, long-term inaccuracy, *RC* frequency reference, temperature compensation.**

I. Introduction

RAPID developments in the performance of integrated frequency references have brought them to the point where they can replace traditional crystal oscillators in wake-up timers [1], [2] and MCU clock generators [3]. Compared to other potential candidates, such as micro-electromechanical systems (MEMSs) oscillators [4], [5], bulk acoustic wave (BAW) resonators [6], [7], *LC* oscillators [8], and thermal-diffusivity frequency [9], [10], *RC*-based frequency references are more compact, occupying less than 0.1 mm^2, and typically dissipating lower power, typically at the microwatt or even the nanowatt level [1], [2], [11], [12]. Recent hybrid frequency references, such as *LC*-compensated ring oscillators [13] and crystal-compensated *RC* oscillators [14], can also achieve low (average) power. By using an *LC* oscillator to periodically calibrate a ring oscillator, sub-100-ppm inaccuracy can be achieved after a single-point calibration [13], with an average power of 0.21 mW. Such designs are well-suited for wireless IoT applications. However, due to their more complex architectures, they occupy significantly more area.

The inaccuracy of *RC*-based frequency references is typically worse than that of MEMS/BAW/*LC* references. This is mainly due to the large and nonlinear temperature coefficients (TCs) of on-chip resistors. To address this, *RC* frequency references typically employ low-TC polysilicon resistors [15], [16], [28], [29], resulting in 100-ppm-level inaccuracy from −40 °C to 85 °C [15], [16] with the help of digitally assisted temperature compensation schemes.

Unfortunately, polysilicon resistors are prone to aging [17], [18], [19], [21]. In [12] and [20], frequency references built around P-poly resistors exhibit output frequency drifts as large as 5000 ppm after accelerated aging. This can be addressed by periodically calibrating them with respect to a more aging-robust reference, as in [13], [14], and [20]. However, this approach increases design complexity and area.

Alternatively, more stable resistors can be used. For example, thin-film, silicided and metal resistors are all significantly more stable than polysilicon resistors [19]. However, thin-film resistors are not available in standard CMOS technologies, while the low sheet resistance of silicide/metal resistors makes them unsuitable for use in compact designs. The latter also have much larger TCs and thus require more complex temperature compensation schemes. Diffusion resistors, which have a larger sheet resistance than metal/silicided resistors and a lower $1/f$ noise than polysilicon resistors, are thus better candidates for use in compact and aging-robust *RC* frequency references.

This work, which is an extended version of [23], presents a CMOS *RC* frequency reference with a 32-MHz output, which is a commonly used microcontroller clock frequency [24], [25]. It is based on N-type diffusion (N-diff) resistors

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and metal–insulator–metal (MIM) capacitors. The 1st- and 2nd-order TCs (TC1 and TC2) of the N-diff resistors are compensated by adjusting the TCs of the currents generated by a bipolar junction transistor (BJT)-based bias circuit, which has proven robustness to aging [26], [27]. In a standard 180-nm CMOS process, the frequency reference occupies only 0.028 mm^2 and achieves ±900-ppm inaccuracy from −40 °C to 125 °C and ±1600-ppm inaccuracy after accelerated aging. This represents the state-of-the-art performance for compact frequency references.

The rest of this article is organized as follows. Section II briefly introduces the architecture of the proposed *RC* frequency reference and its temperature compensation scheme. After presenting circuit implementation details in Section III, measurement results with different kinds of resistors (diffusion/polysilicon) are presented in Section IV, and the performance of the frequency reference is compared to the state of the art. Finally, conclusions are drawn in Section V.

II. Circuit Architecture and BJT-Based Temperature Compensation

A. Architecture Choice

Although the simple architecture of a relaxation oscillator [28], [29] results in compact designs, their inaccuracy is limited by comparator delay. Better accuracy can be achieved by implementing a frequency-locked loop (FLL), in which the comparator is replaced by an integrator that drives a voltage-controlled oscillator (VCO) [30], [31], [32].

Fig. 1(a) shows the simplified circuit diagram of such an FLL [12]. Its front end can be regarded as a Wheatstone bridge (WhB) made from three resistors and a switched-capacitor resistor. The integrated output of the bridge is used to drive a VCO, and the loop is closed by using its (divided) output to drive the switched capacitor C_0 and thus tune its equivalent resistance. At steady state, the integrator's dc gain forces the average output of the WhB to zero, and as a result, the VCO's frequency will be a function of $R_{0/1/2}$ and C_0.

In [12], the TC1 of a P-poly resistor (R_0) is compensated by a trimmed divider (R_1 and R_2) made from P-poly and N-poly resistors. The design achieves an inaccuracy of ±2800 ppm from −45 °C to 125 °C and occupies only 0.01 mm^2 in a standard 180-nm process. However, the use of P-poly resistors leads to a significant error (∼5000 ppm) after accelerated aging [12], [20]. Simply replacing R_0 by a diffusion resistor results in greater inaccuracy (±14 400 ppm) over the same temperature range [12]. This is mainly due to the non-linear nature of the temperature compensation scheme, which results in a significant TC2 after the large TC1 of the diffusion resistor is canceled. Greater accuracy can be achieved by using other kinds of resistors [16] or by applying two-point trim and digitally assisted polynomial correction [15], [34], but this comes at the expense of chip area and calibration effort.

In this work, the temperature dependence of an N-diff resistor is compensated by adjusting the TCs of the currents I_R and I_C injected into the resistive and switched-capacitor branches of the front end, as shown in Fig. 1(b). As in [12], its operation can be divided into three phases. During the discharge phase

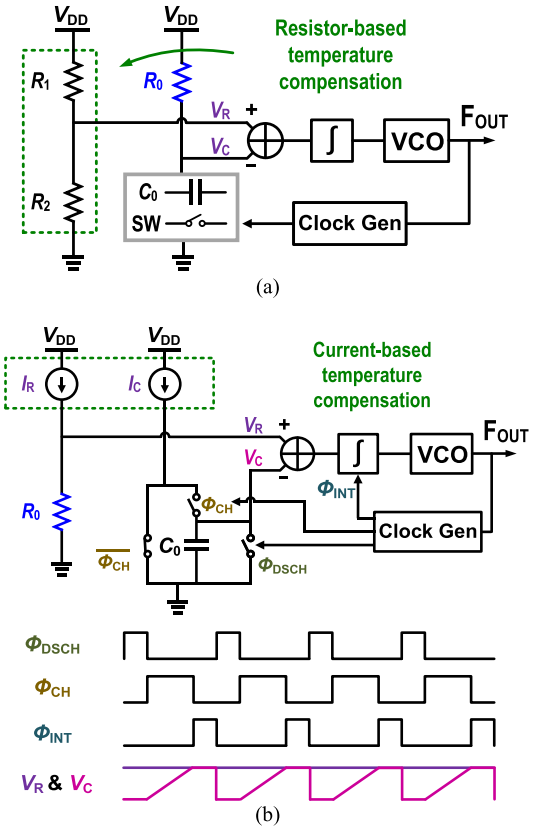


Fig. 1. Compact FLL-based *RC* frequency references with (a) resistor-based temperature compensation 0. (b) Proposed current-based temperature compensation and the corresponding timing design.

Φ_{DSCH}, capacitor C_0 is discharged by shorting it to GND. Then, C_0 is charged by the current I_C during the charging phase Φ_{CH}, at the end of which the voltage V_C is sampled. During the subsequent integration phase Φ_{INT}, the difference between V_R and the sampled V_C is integrated and applied to the VCO. The temperature dependence of R_0 can then be compensated by ensuring that the temperature dependence of the current ratio I_R/I_C is equal to that of $R_0 \cdot C_0$.

B. BJT-Based Temperature Compensation

When biased in its forward active region, a BJT's base–emitter voltage (V_{BE}) has a complementary-to-absolute-temperature (CTAT) characteristic, while the V_{BE} difference (ΔV_{BE}) of a pair of BJTs biased at different current densities has a proportional-to-absolute-temperature (PTAT) characteristic. As shown in Fig. 2, currents with PTAT and CTAT characteristics I_{PTAT} and I_{CTAT}, respectively, can then be generated by using opamps to force ΔV_{BE} and V_{BE} across resistors R_{BP} and R_{BC}, respectively. These currents can then be scaled and combined to generate the currents I_R and I_C, whose temperature dependencies can be adjusted to cancel the temperature dependency of the *RC* time constant. To minimize the effect of their process spread on the resulting temperature dependencies, the same kind of resistor is used to implement R_{BP}, R_{BC}, and R_0.

Denoting K_{RP}, K_{RC}, K_{CP}, and K_{CC} as the scaling factors of the PTAT/CTAT currents used to generate the currents I_R

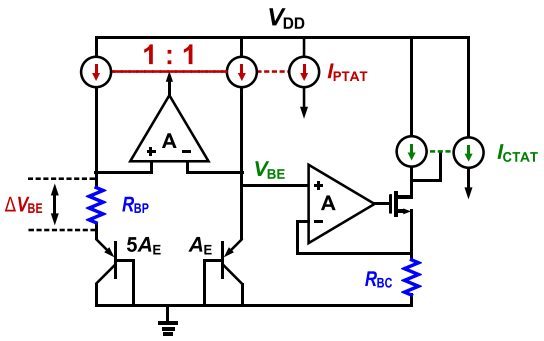


Fig. 2. Generation of I_{PTAT} and I_{CTAT} currents.

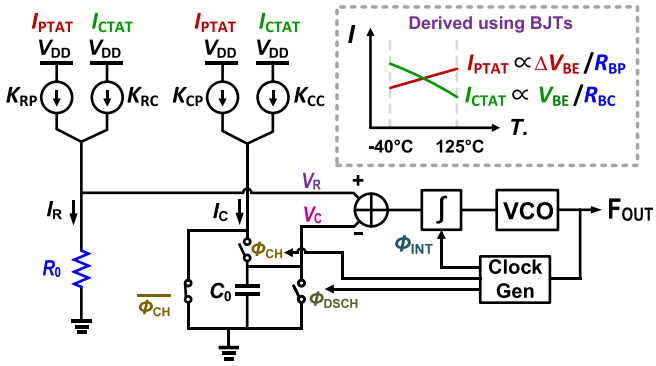


Fig. 3. Proposed BJT-based temperature compensation scheme.

and I_{C}, respectively, and N as the division ratio of the clock generation block, the reference voltage V_R and the voltage on the capacitor V_{C} at the end of a charging cycle can be expressed as follows:

$$V_R = I_R \cdot R_0 = \left(K_{\mathrm{RP}} \cdot \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{BP}}} + K_{\mathrm{RC}} \cdot \frac{V_{\mathrm{BE}}}{R_{\mathrm{BC}}}\right) R_0 \quad (1)$$

$$V_{\mathrm{C}} = \frac{N \cdot I_{\mathrm{C}}}{F_{\mathrm{OUT}} \cdot C_0} = \frac{N\left(K_{\mathrm{CP}} \cdot \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{BP}}} + K_{\mathrm{CC}} \cdot \frac{V_{\mathrm{BE}}}{R_{\mathrm{BC}}}\right)}{F_{\mathrm{OUT}} \cdot C_0} \quad (2)$$

where F_{OUT} is the FLL's output frequency. Since $V_R = V_{\mathrm{C}}$ at steady state, F_{OUT} can be obtained by combining (1) and (2)

$$F_{\mathrm{OUT}} = \frac{N}{R_0 C_0} \cdot \frac{I_{\mathrm{C}}}{I_R} = \frac{N}{R_0 C_0} \cdot \frac{K_{\mathrm{CP}} \cdot \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{BP}}} + K_{\mathrm{CC}} \cdot \frac{V_{\mathrm{BE}}}{R_{\mathrm{BC}}}}{K_{\mathrm{RP}} \cdot \frac{\Delta V_{\mathrm{BE}}}{R_{\mathrm{BP}}} + K_{\mathrm{RC}} \cdot \frac{V_{\mathrm{BE}}}{R_{\mathrm{BC}}}}. \quad (3)$$

To illustrate how both TC1 and TC2 can be canceled, we assume that $K_{\mathrm{CP}} \cdot (\Delta V_{\mathrm{BE}}/R_{\mathrm{BP}}) + K_{\mathrm{CC}} \cdot (V_{\mathrm{BE}}/R_{\mathrm{BC}})$ and $K_{\mathrm{RP}} \cdot (\Delta V_{\mathrm{BE}}/R_{\mathrm{BP}}) + K_{\mathrm{RC}} \cdot (V_{\mathrm{BE}}/R_{\mathrm{BC}})$ can be rewritten as $I_{\mathrm{A}}(1 + \mathrm{TC}_{1A} \cdot \Delta T + \mathrm{TC}_{2A} \cdot \Delta T^2)$ and $I_{\mathrm{B}}(1 + \mathrm{TC}_{1B} \cdot \Delta T + \mathrm{TC}_{2B} \cdot \Delta T^2)$, respectively, where I_{A} and I_{B} are the nominal currents at room temperature (RT), ΔT is the temperature difference with respect to the RT, and TC_{1A}, TC_{2A}, TC_{1B}, and TC_{2B} are the 1st or 2nd-order TCs. Equation (3) can then be rewritten as (4), shown at the bottom of the page, where τ_0 and TC_{1C} and TC_{2C} are the nominal value and TCs of R_0C_0, respectively. By tuning the K ratios in the numerator and denominator, the TC1 of R_0C_0 can be canceled, i.e., by setting $\mathrm{TC}_{1C} = \mathrm{TC}_{1A} - \mathrm{TC}_{1B}$. Furthermore, since the denominator is the product of two terms with (predominantly) 1st-order TCs, it also has an additional tunable 2nd-order TC term, i.e., $\mathrm{TC}_{1C} \cdot \mathrm{TC}_{1B}$. This provides another degree of freedom that enables the simultaneous cancellation of the TC1 and TC2 of R_0C_0. This scheme requires only one kind of resistor, making it robust to resistor spread.

C. Temperature Compensation Range

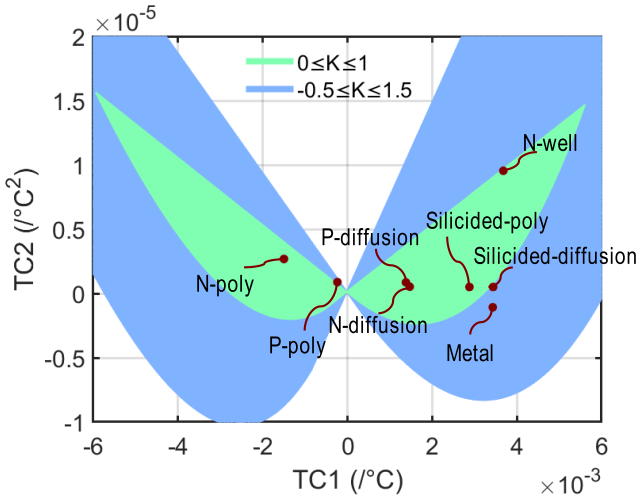
The circuit shown in Fig. 2 can be used to investigate the performance of the proposed temperature compensation method with different kinds of resistors. Since an exact mathematical analysis is intractable and does not provide much insight, numerical simulations were used instead.

In the simulations, Fig. 2 circuit was implemented with six PNPs with 2 × 2 μm emitter areas, an emitter–area ratio of 5, and a reference current $\Delta V_{\mathrm{BE}}/R_{\mathrm{BP}} = V_{\mathrm{BE}}/R_{\mathrm{BC}} = 2$ μA at RT. For simplicity, the temperature dependence of C_0 (TC1 ∼ 3×10^{-5}), which is much smaller than that of the resistors, was neglected during the initial analysis. The effect of the non-zero TC of the biasing resistor on V_{BE} was captured by making a 1st-order Taylor approximation. With a zero TC biasing resistor, the TC1/TC2 of ΔV_{BE} is about 0.156 mV/°C and 0.097 μV/°C^2, while that of V_{BE} is about −1.66 mV/°C and 1.67 μV/°C^2, respectively.

From (3), the optimal scaling factors ($K_{\mathrm{RP/CP/RC/CC}}$) can then be found for different kinds of resistors. Since the temperature characteristics of the numerator and denominator only depend on the K ratios, the search space can be constrained by setting $K_{\mathrm{RC}} = 1 - K_{\mathrm{RP}}$, and $K_{\mathrm{CC}} = 1 - K_{\mathrm{CP}}$. The K factors then represent the proportion of PTAT/CTAT currents flowing in the capacitive/resistive branches at RT, as depicted in Fig. 3.

The correction range of the proposed scheme is shown in Fig. 4(a), together with the TC1 and TC2 for different kinds of resistors. The magnitude of the corresponding PTAT/CTAT components in I_R and I_{C} is summarized in Fig. 4(b). With all-positive K factors ($0 \le K_{\mathrm{RP/CP/RC/CC}} \le 1$), the compensation range is constricted to the light green region in Fig. 4(a). This can be expanded to the light blue region by allowing the use of negative K factors (modeling the sinking, rather than the sourcing, of currents into the capacitive/resistive branches). The proposed scheme can compensate for the TCs of all the available resistors in the targeted 180-nm technology. In general, the TC spread of resistors is much smaller than their nominal resistance spread, so the trimming method can be applied. Although the K factors are limited to −0.5 to 1.5 in Fig. 4(a), a wider range is also possible. An interesting observation is that the scheme cannot be applied to resistors, whose temperature dependency is TC2 dominated.

$$F_{\mathrm{OUT}} = \frac{N \cdot I_{\mathrm{A}}\left(1 + \mathrm{TC}_{1A}\Delta T + \mathrm{TC}_{2A}\Delta T^2\right)}{\tau_0\left(1 + \mathrm{TC}_{1C}\Delta T + \mathrm{TC}_{2C}\Delta T^2\right) \cdot I_{\mathrm{B}}\left(1 + \mathrm{TC}_{1B}\Delta T + \mathrm{TC}_{2B}\Delta T^2\right)} \quad (4)$$



(a)

Resistor type	TC1	TC2	K_{RP}	K_{RC}	K_{CP}	K_{CC}
N-diff	1.47×10^{-3}	8.32×10^{-7}	36%	64%	61%	39%
P-diff	1.43×10^{-3}	7.82×10^{-7}	31%	69%	65%	35%
N-poly	-1.51×10^{-3}	2.68×10^{-6}	80%	20%	58%	42%
P-poly	-2.38×10^{-4}	8.85×10^{-7}	105%	-5%	102%	-2%

(b)

Fig. 4. (a) Optimally compensated TC1 and TC2 of F_{OUT} with the BJT-based compensation scheme and different resistor types in the chosen 180-nm CMOS technology. (b) Simulated K ratios for the different resistor types.

From (3), TC1 = 0 implies that $K_{RP} = K_{CP}$, and so, 2nd-order compensation is not possible without 1st-order compensation.

III. Circuit Implementation

A. RC Front-End and Frequency-Locked Loop

Fig. 5 shows the schematic of the *RC* front-end and the FLL, and the corresponding timing diagram is shown in Fig. 6. As discussed in Section I, R_0 (190 kΩ) is an N-diff resistor to achieve good robustness against aging. It is biased at ∼2 μA, which is much larger than its substrate leakage current (<1nA over PVT). The timing capacitor C_0 is a MIM capacitor (4 pF). A *Gm–C* stage ($gm = 1.5$ μS and $C = 4$ pF) is used to integrate the error voltage $V_C - V_R$. Compared to traditional FLLs, which often employ a large capacitor to smooth out the ripple across a switched-capacitor resistor [37], this sampled scheme saves area at the expense of noise efficiency, since the error voltage is now only integrated during Φ_{INT}, while the integrator's noise is present during all four phases. The loop filter output then drives a VCO, which produces a 32-MHz output frequency.

To mitigate errors due to the delay of the phase generation circuit, the duration of the charging phase Φ_{CH}, which determines the FLL's output frequency, is made 2× longer than Φ_{INT} and Φ_{DSCH}. For the same reason, the phase-generation circuit is driven by $F_{OUT}/8$ (4 MHz). The ratio of 8 is chosen as a tradeoff between system stability and frequency error.

To improve the FLL's long-term stability, the *gm*-stage (telescopic OTA) is chopped at 1 MHz to suppress its $1/f$ noise. To reduce its short-term stability or jitter, which is mainly set by the VCO, three techniques are applied. First, a compact single-ended switched-capacitor notch filter operated at half the chopping frequency is used to suppress the up-modulated offset of the chopped *gm*-stage [36]. Dummy switches are used to cancel the charge injection of its switches. Second, resistor degeneration is used to suppress the flicker noise of the current source that drives the VCO. Last, the VCO employs differential delay elements with cross-coupled auxiliary inverters to achieve fast, balanced, rising/falling edges.

B. BJT Core and Current Generation

Fig. 7 shows the simplified circuit realization of the PTAT/CTAT current generation circuits described in Section II. $9 \cdot R_{BP} = R_{BC}$ (140 kΩ), and the resulting I_{PTAT} and I_{CTAT} after current mirror copying and trimming are 2.5 and 5.2 μA at RT, respectively. A1 and A2 are identical cascaded telescopic OTAs, their dc gain is ∼80 dB, and a single OTA consumes ∼6.3 μA at RT. As discussed in Section II, the K ratios of the currents applied to the *RC* front end were determined by simulation. According to Fig. 4(b), setting $K_{RP} \sim 0.36$ and $K_{CP} \sim 0.61$ effectively cancels the TC1 (∼1500 ppm/°C) and TC2 (∼0.8 ppm/°C²) of the N-diff resistors. Both the OTAs and the current mirrors were chopped to reduce their offset and $1/f$ noise. To increase the output impedance of the current mirrors, all the PMOS current sources were self-cascoded with lower threshold devices (MVt PMOS transistors).

C. Trimming Circuits

Figs. 8 and 9 show the trimming circuits in this work to compensate for process and temperature variations. As in Fig. 8, the nominal frequency spread over process (30%) is compensated by a 4-bit coarse MIM cap array (f_0[11:8]), while the variations within a batch (<2%) are trimmed by an 8-bit fine metal–oxide–metal (MOM) cap array (f_0[7:0]). In the chosen 180-nm technology, both types of capacitors have a low TC and negligible leakage current, while the density of MOM capacitors is 2.4× smaller than that of MIM capacitors. The two arrays are stacked to reduce chip area. To improve the trimming resolution, two bridge capacitors (MIM cap, $C_{BRG} = 1$ pF) are used to scale the effective LSB CDAC (C_{U2}) from 2.9 to 0.7 fF. This also results in a near-linear trimming resolution of 180 ppm [Fig. 8(b)]. The FLL's TC1 is tuned by applying a 5-bit trim (TC1[4:0]) to K_{CP}, i.e., to the PTAT current (I_C) injected into the capacitive branch. As shown in Fig. 9, the combination of a CMOS direction-control MSB switch and PMOS/NMOS LSB switches allows the TC1 to be adjusted in LSB steps of ∼2.1 ppm/°C (∼350 ppm from −40 °C to 125 °C). The TC2 of the FLL is tuned by applying a 3-bit trim to R_{BC} in the I_{CTAT} generation branch (Fig. 7). This ensures that both K_{CC} and K_{RC} are adjusted in the same manner, and so, the nominal TC1 remains almost unchanged.

D. P-Poly Resistor Version

To demonstrate the flexibility of the proposed temperature compensation method, an FLL based on P-poly resistors was

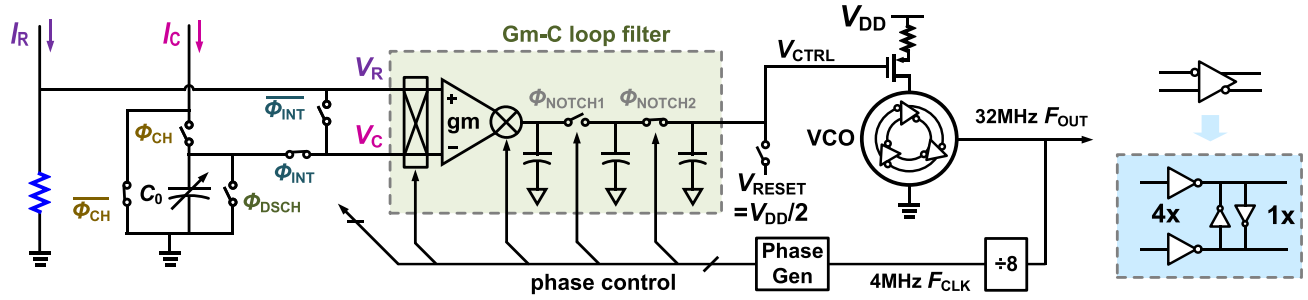


Fig. 5. *RC* front-end and FLL design.

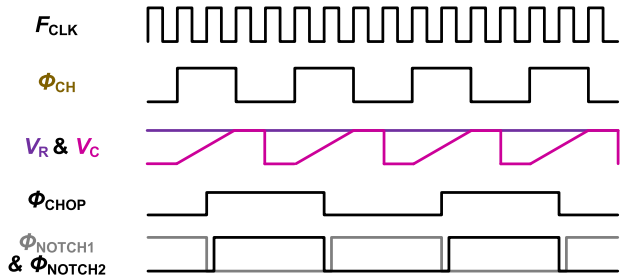


Fig. 6. Timing diagram of the FLL.

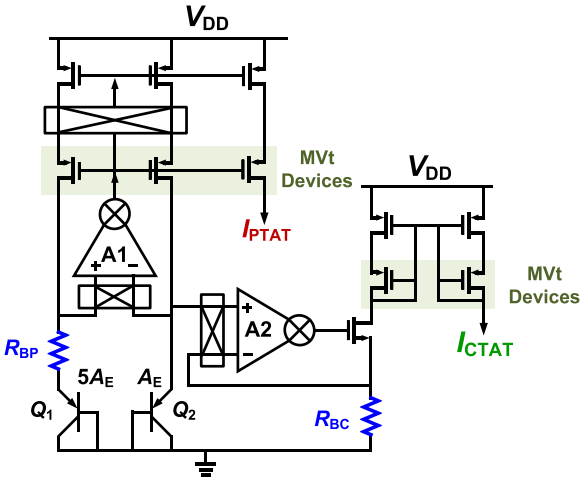


Fig. 7. BJT core and current generation circuits of the N-diff-based FLL.

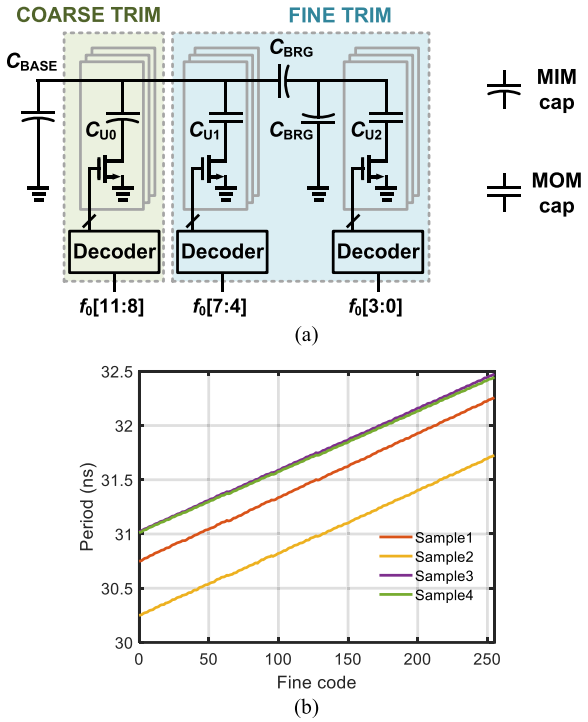


Fig. 8. (a) Nominal frequency (f_0) trimming circuit. (b) Measured output period versus fine tuning code of some samples.

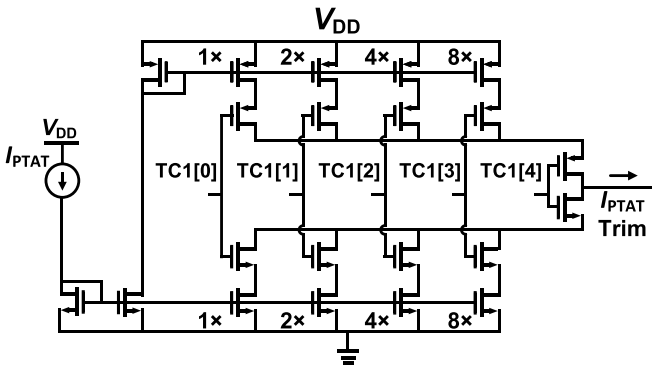


Fig. 9. 1st-order TC (TC1) trimming circuit.

also designed. The TC1 and TC2 of the P-poly resistor are ∼−240 ppm/°C² and ∼0.9 ppm/°C², respectively. According to the simulations in Section II-C, the best compensation is achieved with $K_{RP} \sim 1.05$ and $K_{CP} \sim 1.02$. Since the absolute TCs are significantly smaller than those of the N-diff resistor, the resolution of the TC1/TC2 trims was limited to 4/2 bits.

IV. Measurement Results and Discussion

As shown in Fig. 10, eight FLL-based *RC* frequency references were fabricated on the same die in a standard 180-nm CMOS process. Four employ N-diff resistors, whereas the other four employ P-poly resistors. At RT, the N-diff version occupies 0.028 mm² and draws 73 μA (48-μA analog and 25-μA digital) from a 1.8-V supply. Due to its larger sheet resistance, the P-poly version (0.025 mm²) is slightly smaller, but its current consumption is similar (77 μA).

A. Noise and Start-Up

As shown in Fig. 11, the proposed FLL achieves a thermal-noise-limited closed-loop period jitter of 20.8 ps_{rms} (∼660 ppm); compared with the open-loop jitter of about 18.0 ps_{rms}, the added jitter comes from the noise of the

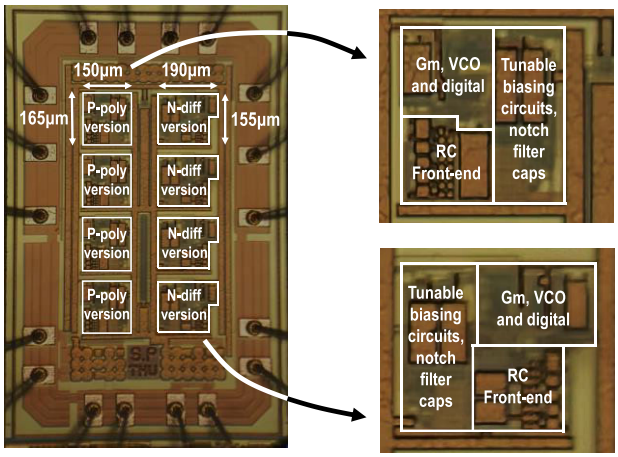


Fig. 10. Chip photograph and zoomed-in view of different FLLs.

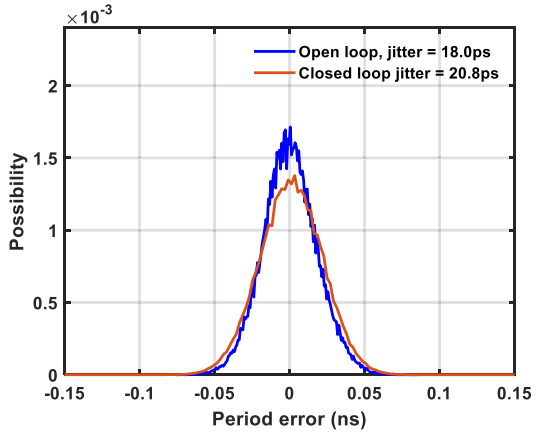


Fig. 11. Open-loop and closed-loop period jitter of the proposed frequency reference.

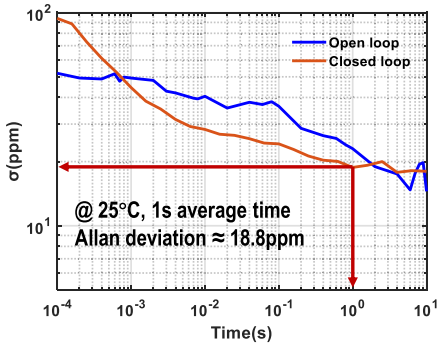


Fig. 12. Allan deviation of the proposed frequency reference.

front-end circuit and the notch filter. As a result, their residual $1/f$ noise of the TC trimming current sources, which are not chopped, will limit the Allan deviation of the proposed FLL. As shown in Fig. 12, it achieves a ∼18.8-ppm Allan deviation floor with a 1-s stride, which is about 8× worse than [12].

As in [12], the dominant pole (∼60 kHz) of the proposed FLL is set by the *Gm–C* filter ($gm \sim 1.5\ \mu$S and $C \sim 4$ pF). Although the notch filter is only updated at 0.5 MHz ($F_{OUT}/64$), good stability is achieved with ∼10× frequency margin. As shown in Fig. 13, due to the notch filter, the output

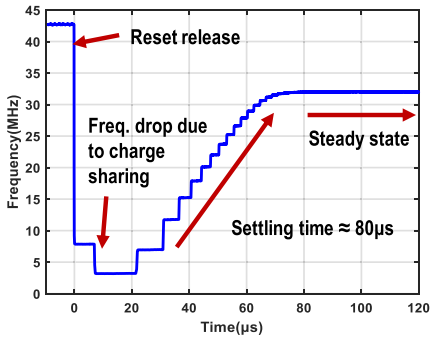


Fig. 13. Start-up behavior of the proposed frequency reference.

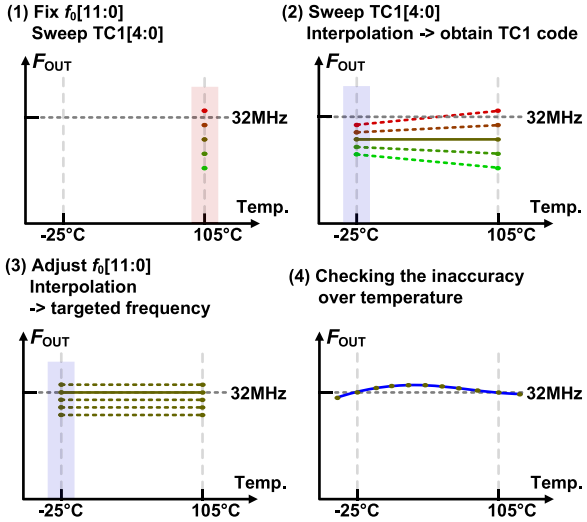


Fig. 14. Two-point calibration steps.

frequency exhibits a stepwise transient after a reset, which settles within about 80 μs.

B. Trimming and Inaccuracy

As shown in Fig. 14, a two-point calibration was used to compensate for the effect of process spread on the FLL's nominal output frequency and TC1/2. After a batch calibration to determine the TC2 code, each FLL is then individually trimmed by sweeping its TC1 code at 105 °C and −25 °C. After choosing the TC1 code that minimizes the output frequency difference between the two temperature conditions, the circuit's nominal frequency is then trimmed at −25 °C. Although the related trimming cost is higher than that of conventional one-point calibrations, the FLL's chip area is kept relatively small, resulting in a low fabrication cost and a restricted overall cost.

Seven DIP 18 wire-bonded ceramic-packaged chips (28 samples of each type) from one wafer were trimmed and characterized in a temperature-controlled oven. With a ∼20 °C temperature step and a temperature settling time of 1 h/step, the complete temperature hysteresis from −40 °C to 125 °C is done within 18 h. As shown in Fig. 15(a), the N-diff-based FLL clearly exhibits stress-induced hysteresis and spread as the oven temperature is cycled between cold

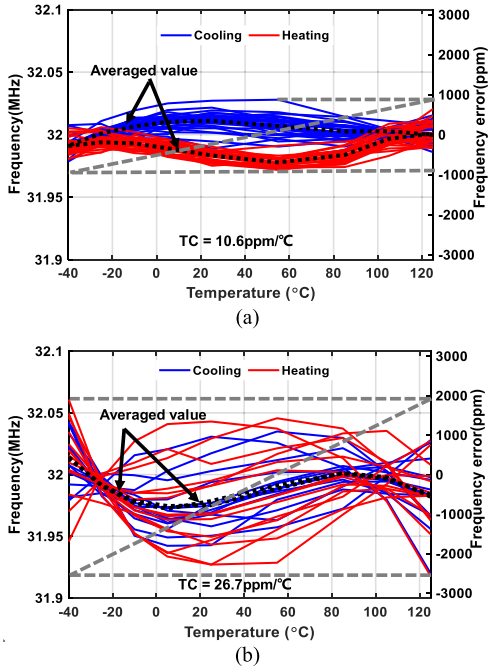


Fig. 15. Temperature characteristics of (a) N-diff and (b) P-poly frequency references. Heating: chip is characterized from hot to cold; cooling: chip is characterized from cold to hot.

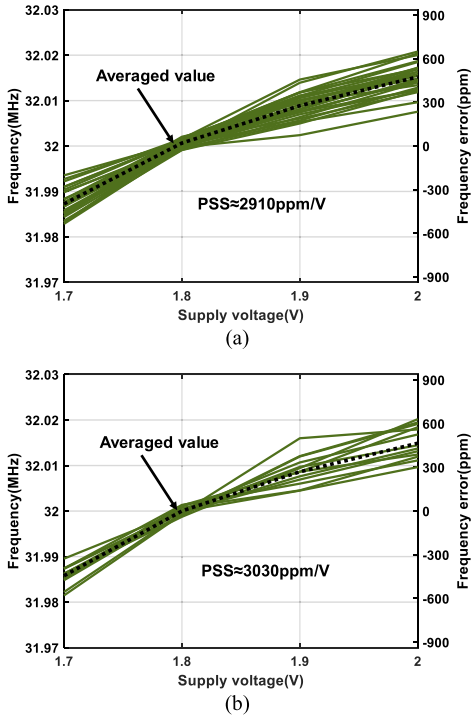


Fig. 16. Temperature characteristics of (a) N-diff and (b) P-poly frequency references.

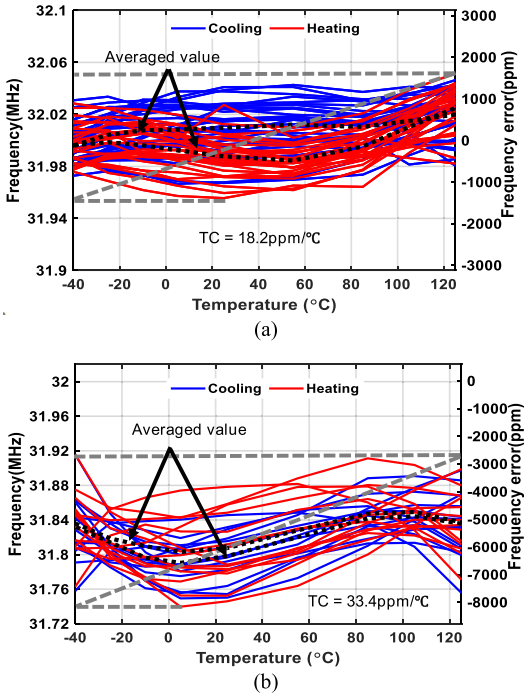


Fig. 17. Aging effect of (a) N-diff and (b) P-poly frequency references.

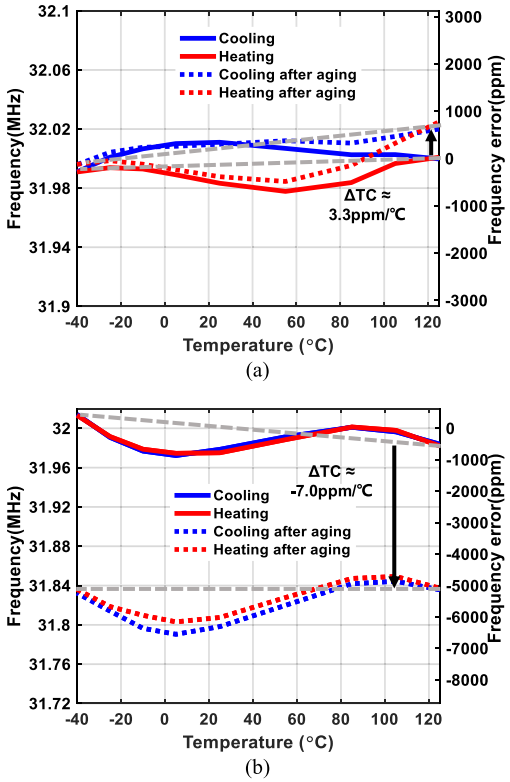


Fig. 18. Averaged value drift of (a) N-diff and (b) P-poly frequency references after accelerated aging (the gray lines connecting data points at the lowest/highest temperatures indicate the changes of TC1).

and hot. Its peak inaccuracy is 900 ppm, which corresponds to a residual TC 10.6 ppm/°C from −40 °C to 125 °C (box method). Due to process spread and the limited TC1 tuning range, only half of the P-poly samples (14 out of 28) could be properly trimmed. Over the same temperature range, these samples achieved a larger peak inaccuracy of 2500 ppm and residual TC [26.7 ppm/°C, Fig. 15(b)]. However, their averaged hysteresis is somewhat less than that of the N-diff samples.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART *RC* FREQUENCY REFERENCES

	JSSC 2022 [15]	JSSC 2023 [16]	ISSCC 2022 [28]	JSSC 2023 [20]	TCAS-I 2016 [29]	ISSCC 2023 [12]	This work	
Technology	180nm	65nm	180nm	65nm	180nm	180nm	180nm	
Main resistor	P-Poly	P-Poly	P-Poly	P/N-Poly	P-Poly	P-Poly	P-Poly	N-Diff
Compensation device	S-Poly	N+ Diff P+ Diff	S-Poly N-well	VIA Res.	N+ Diff	N-Poly	BJT	
Area [mm^2]	0.3	0.19	0.07	0.22	0.012	0.01	0.025	0.028
Total capacitance[pF] (Capacitor types)	>50 (MIM)	>81 (MIM,MOM)	>2 (-)	>23.2 (MIM,MOM)	- (-)	16 (MIM,MOM)	10.7 (MIM,MOM)	
Frequency [Hz]	16M	100M	2.3M	100M	12.77M	10M	32M	
Power [μW]	220	101	7.6	142	56.2	85.1	139	131
Energy [pJ/cycle]	13.8	1.01	3.3	1.42	4.4	8.51	4.3	4.1
Supply range [V]	1.6~2	1.2	1.3~2.0	1.1~1.3	0.6~1.1	1.5~1.8	1.7~2.0	
Supply sensitivity [ppm/V]	1200	83	5100	1400	10000	9000	~3000	
Jitter [ps]	39.9	13.3	9	5.1	78.7	41.4	20.8	
Temp. range [°C]	-45~85	-40~95	-40~125	-40~85	-30~120	-45~125	-40~125	
Temp. coefficient [ppm/°C] [a]	1.3	2.1	7.93	12.16	31 [b]	31.5	26.7	10.6
Max. freq. error [ppm]	±90	±140	+1000/ -2000 [b]	±760	±9000 [b]	±2800	+2000/-2500	±900
Averaged Freq. drift [ppm]	-	-	-	-	-	5000 [d]	200 [d]	5200 [d]
Freq. error after aging [ppm]	-	-	-	±1030 [c]	-	-	-2600/-8100 [d]	+1600/-1400 [d]
Trimming points (Trimming temperature[°C])	2+batch (-35,75)	3 (-35,25,90)	2 (-)	2 (-40,85)	1 (25)	1+batch (25)	2 (-25,105)	
Number of samples	20	20	11	10	4	112	14	28

[a] box method [b] Estimated from the inaccuracy plot [c] 500hours @ 125°C [d] 168hours @ 150°C

TABLE II
COMPARISON WITH OTHER TYPES OF FREQUENCY REFERENCES

	JSSC 2010 [10]	JSSC 2012 [9]	JSSC 2021[8]	JSSC 2023 [13]	This work	
Technology	700nm	160nm	130nm	130nm	180nm	
Structure	Thermal-Diffusivity	Thermal-Diffusivity	LC Colpitts	LC Cross-coupled	RC (P-Poly)	RC (N-Diff)
Compensation method	Digital polynomial	Digital polynomial	Digital polynomial	Digital polynomial	Current defined by BJT	
Area [mm^2]	6.75	0.19	0.26	0.69	0.025	0.028
Frequency [Hz]	1.6M	16M	1380M	70M	32M	
Power [μW]	7800	2100	4250	210	139	131
Energy [pJ/cycle]	4875	131.25	3.07	3.0	4.3	4.1
Supply range [V]	5	1.8	2.5	3.3	1.7~2.0	
Supply sensitivity [ppm/V]	-	-	220	92 [b]	~3000	
Jitter [ps]	312	45	0.5	14.3	20.8	
Temp. range [°C]	-55~125	-55~125	-50~170	-63~165	-40~125	
Temp. coefficient [ppm/°C] [a]	11.2	11.2	1	0.7	26.7	10.6
Max. freq. error [ppm]	±1000	±1000	±120	+74/-93	+2000/-2500	±900
Averaged Freq. drift [ppm]	-	-	-	52 [c]	200 [d]	5200 [d]
Freq. error after aging [ppm]	-	-	-60/170 [c]	±205 [c]	-2600/-8100 [d]	+1600/-1400 [d]
Trimming points (Trimming temperature[°C])	1+Batch (25)	1+Batch (25)	1 (25)	1 (25)	2+Batch (-25, 105)	
Number of samples	16	24	16	18	14	28

[a] box method [b] with an LDO [c] 144hours @ 175°C [d] 168hours @ 150°C

Fig. 16 shows the power supply sensitivities (PSSs) of the FLLs. From 1.7 to 2.0 V, the average PSSs are 2910 and 3030 ppm/V for the N-diff and P-poly FLLs, respectively. This indicates that the current biasing scheme effectively

suppresses the voltage-dependent characteristic of the N-diff resistors.

C. Accelerated Aging Test

For comparison with the results reported in [12], the packaged samples were subjected to one week of accelerated aging at 150 °C. As shown in Fig. 17, this translates into a total long-term inaccuracy of ±1600 ppm for the N-diff version, which is much better than that of the P-Poly version (from −2600 to −8000 ppm). Furthermore, as shown in Fig. 18, the N-diff version exhibits much less average drift (200-ppm nominal frequency and 3.3 ppm/°C TC) than the P-poly version (−5200-ppm nominal frequency and −7 ppm/°C TC). Assuming an activation energy of 0.68 eV [20], the aging conditions used are equivalent to 544 h of aging at 125 °C, which is similar to 500 h at 125 °C used in [20]. No aging experiments were conducted to investigate the effect of different packages. This is an important topic for future research.

D. Comparison to Previous Work

The performance of the proposed *RC* frequency reference is summarized in Table I and compared with the state of the art, while a comparison with other types of frequency references is presented in Table II. Despite being manufactured in a mature 180-nm CMOS process, the N-diff-based FLL occupies the least chip area among *RC*-frequency references with sub-1000-ppm inaccuracy. It also achieves low supply sensitivity and good inaccuracy after accelerated aging, without the use of aging compensation circuitry [20]. However, compared to *LC*-based [13], its aging performance is an order of magnitude worse.

V. Conclusion

This article presents a compact, accurate, and aging-robust CMOS *RC* frequency reference based on N-diff resistors and MIM capacitors. It is based on an FLL, which locks the period of a VCO to the time it takes a current source to charge a MIM capacitor to a reference voltage. Conventionally, such FLLs are temperature compensated by using resistors with different TCs to generate temperature-dependent reference voltages and/or charging currents. In this work, for better stability, this is done with the help of a TC-tunable BJT-based biasing circuit. A prototype *RC* frequency based on N-diff resistors achieves small area (0.028 mm^2), low inaccuracy (±900 ppm) from −40 °C to 125 °C, and the state-of-the-art inaccuracy after accelerated aging (±1600 ppm). The versatility of the proposed TC compensation scheme is demonstrated via simulation and measurements. A version based on P-poly resistors has been implemented. However, it exhibits worse inaccuracy (+2000/−2500 ppm), which gets much worse (−2600/−8100 ppm) after accelerated aging. Overall, this article presents a promising BJT-assisted architecture and design method for the realization of compact and accurate *RC* frequency references in CMOS processes.

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