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A Comparison between ^{90}Sr and ^{60}Co

Menicucci, Alessandra; Malatesta, Fabio; Di Capua, Francesco; Campajola, Luigi; Casolaro, Pierluigi; Furano, Gianluca; Di Mascio, Stefano; Ottavi, Marco

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Simplified procedures for COTS TID testing: a comparison between ^{90}Sr and ^{60}Co

1st Alessandra Menicucci
Department of Space Engineering
TU Delft
Delft, The Netherlands
a.menicucci@tudelft.nl

2stFabio Malatesta
Cobham Gaisler
Göteborg, Sweden
fabio.malatesta@gaisler.com

3stFrancesco Di Capua
Dept. of Physics
University of Naples Federico II and INFN
Naples, Italy
dicapua@na.infn.it

4stLuigi Campajola
Dept. of Physics
University of Naples Federico II and INFN
Naples, Italy
luigi.campajola@na.infn.it

5stPierluigi Casolaro
Dept. of Physics
University of Naples Federico II and INFN
Naples, Italy
pierluigi.casolaro@na.infn.it

6stGianluca Furano
Data Systems and Microelectronics Division
European Space Technology Centre - ESTEC
Noordwijk, The Netherlands
gianluca.furano@esa.int

7stStefano Di Mascio
Department of Space Engineering
TU Delft
Delft, The Netherlands
s.dimascio@tudelft.nl

8stMarco Ottavi
Department of Electronic Engineering
University of Rome Tor Vergata
Rome, Italy
ottavi@ing.uniroma2.it

***Abstract*—The tolerance to the cumulative effects of ionizing radiation is one of the most important parameters to keep into account when selecting an EEE component for space applications. TID sensitivity is normally investigated measuring changes induced by gamma rays from ^{60}Co sources to nominal parameters of a component or to its expected functional behavior. In this work we propose an on-chip ^{90}Sr/^{90}Y electron source as an alternative methodology for TID tests.^{60}Co and ^{90}Sr/^{90}Y TID test setups for a complex SoC are compared in terms of complexity and of experimental results, investigating the use of a ^{90}Sr/^{90}Y as well as the established ^{60}Co. We show that ^{90}Sr allows a simpler test setup, manages to reproduce specific modes of failure obtained with ^{60}Co and causes failures at comparable total doses. This makes ^{90}Sr an interesting alternative to^{60}Co qualification and the use of untested components, to be further investigated especially for complex COTS SoCs.**

***Index Terms*—component, total dose, Cobalt**

I. Introduction

The use of System-on-Chip (SoC) solutions in the design of space-borne data handling systems is an important step towards further miniaturization in space. In cubesats and in many aggressive commercial missions, use of Commercial Off-The-Shelf components is becoming the rule, rather than the exception and many of those are complex SoC, MPSoC (multiprocessor system-on-chip), SiP (System in package) or AMS-SoC (Analog/Mixed Signal SoC) [1]. It is well known that the possible sources of failure of these devices are Single Event Effects (SEE) [2], [3] and Total Ionizing Dose (TID) [4], [5]. In particular the TID characterization of these complex devices presents new challenges that are either not fully addressed by current testing guidelines or may result in cumbersome test configurations. In this activity we aim to study test set-up, procedures and achieve some sample results for TID testing of miniaturized complex devices. This is a starting point to build knowledge and set guidelines to be applicable to all devices for which classical ^{60}Co tests is too cumbersome or expensive to be viable.

During standard tests using high intensity ^{60}Co sources, all sensitive parts except the Device Under Test (DUT) must be shielded. One commonly used method is to deploy heavy lead blocks of sheets to shield the sensitive components in order to avoid the risk to invalidate the test. This is sometime impossible given the fact that ancillary circuits are often on the same test board and, even with bespoke designs, the maximum possible distance is limited. These difficulties in a standard ^{60}Co irradiation room, could be overcome only with the development of complex and expensive test setup. A more confined radiation field could avoid such problems and the need for ad-hoc designed boards, allowing the use of typical SoCs modular evaluation boards which provide cheaper and faster solutions.

Furthermore, physical distance between the DUT and the measurement equipment needed is often on the order of 10 meters or more, depending on the facility. For this reason, testing at realistic clock speeds, comparable with real applications, is very cumbersome if using the traditional approach which relies on the usage of long cables [6]: if fast clocks or analogue signals need to be monitored on the DUT, complex set-up is needed. In this work we used the solution addressed by [7]

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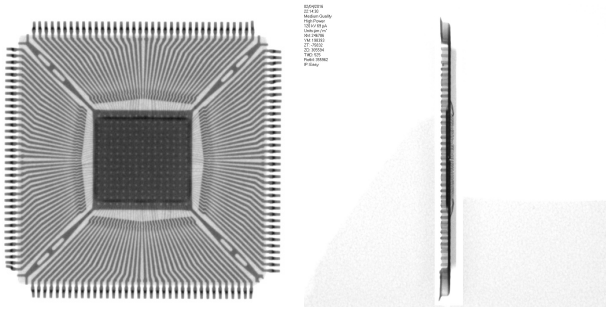

Fig. 1. Chip radiography

which makes use a $^{90}Sr/^{90}Y$ on-chip beta source for TID testing.

II. $^{90}Sr/^{90}Y$ Source and Dosimetry

The β particles are electrons emitted by a β radioactive decay: ^{90}Sr undergoes a decay of 0.546 MeV energy distributed to an electron, an anti-neutrino and to the ^{90}Y isotope, which in turn undergoes a decay with energy 2.28 MeV. Therefore the energy spectrum assumes continuous values that, starting from zero, rapidly fall down to 2.28 MeV end-point.
Electrons having energy greater than 0.4 MeV can penetrate most of plastic encapsulation packages and then produce ionization in the DUT's active area. These electrons can be easily shielded with 1-2 cm of plastic material, for such reason a beta source with an activity high enough to allow Low Dose Rate TID testing (< 1 mGy/s) can be easily managed in laboratory environment with no complex radiation safety procedures.
The dose rate of the ^{90}Sr/^{90}Y source has been measured by mean of calibrated EBT3 Radiochromic films and an ionization chamber by obtaining a complete dose characterization as a function of source distance from DUT [7]. In order to obtain a uniform dose distribution on the DUT we used an Al build-up collimator of annular shape with an internal diameter of 10 mm. The measured dose rate with the build-up collimator at 8 mm source-DUT distance is 538 rad/h in Silicon. The non-uniformity of the field on chip size, measured with EBT3 itself, is less than 5%. To definitively estimate the dose delivered on chip die, an X-ray radiography of the device has been performed to find the exact position of die and the package size (Fig. 1). This is found 0.35 mm down to a Sumitomo EME-G700 type LG mold compound. With a Geant4 simulation we found a dose/rate on the die of 552 rad/h

III. Experimental Setup and Preliminary Results

The board used for the tests is a NXP XPC56XL [8], which supports the SPC56EL70 micro-controller. The board is composed by a Mini-module which plugs into a Motherboard. The Motherboard provides the I/O pins and some devices like an RS232 controller and a potentiometer. The SPC56XL70xx micro-controller is built around a dual-core safety platform with a safety concept targeting ISO26262 ASILD and IEC61508 SIL3 integrity levels.The two cores can be used in two modes of operation:

- Lock Step Mode (LSM): cores execute the same operations on the same data. If outputs differs the system knows something went wrong and can take proper actions.
- Decoupled Parallel Mode (DPM): cores operate as independent cores (1.6x performance over the LSM one).

In these tests the DUT was always running in Lock Step Mode, in which the Redundancy Control and Checker Units (RCCUs), implemented on all outputs of the cores (addresses, data and control signals) check if the two modules in redundancy have the same outputs. Any difference between the outputs of the cores indicates a fault and triggers the according reaction, sending an out-of-lock flag to the Fault Collection and Control Unit (FCCU). The FCCU is a FSM that, once spotted a fault, can lead the device to a "safe state" and eventually reset the micro-controller. Moreover, the FCCU provides 2 external bidirectional signals (FCCU_F interface). Different protocols for the FCCU_F interface are supported. For example,in the Dual Rail protocol, as long as the FCCU is in NORMAL or ALARM state, output will show "no-faulty" signal: output pins FCCU_F[0] (board pin J16) and FCCU_F[1] (board pin J18) will toggle between 01 and 10 with a given frequency. Further information about the board and the micro-controller are available in [9] and [10]. Two test programs have been used:

- **ADC program**: program reading a static value from an ADC channel connected to the potentiometer on the motherboard.
- **"Test as you fly" program**: this program is composed of time slots, each intensively using a resource of the microcontroller. The goal of this software is to emulate typical program flows during missions.

A. $^{90}Sr/^{90}Y$ test

The experimental setup with ^{90}Sr/^{90}Y is simplified in terms of shielding requirement since only the DUT will be irradiated while the rest of the test equipment can stay inside the radiation room without the need to shield it. These tests were carried out in a standard laboratory at the University of Napoli Federico II where the the ^{90}Sr source is located. An Adjustable output stabilized power supply provided power to the board (12 V DC) while monitoring the exact current drain. The clock was provided by a Pulse-Pattern Generator: external clock has been supplied in order to ensure that no oscillator faults would trigger "false" DUT errors. The clock signal provided was a square wave with 50% duty cycle, 40 MHz frequency, 1.3 V peak to peak with a 0.65 V offset. An Oscilloscope was constantly monitoring the FCCU pins on the Mini-module. Moreover, a Multimeter was used to monitor the voltage level of the core's supply pin. During the irradiation, the device was constantly logging its behavior through UART and a laptop in the radiation room received all the logs.

The source mechanism was configured at 8mm above the DUT and it provided a stable dose rate of 538 rad/h. Two

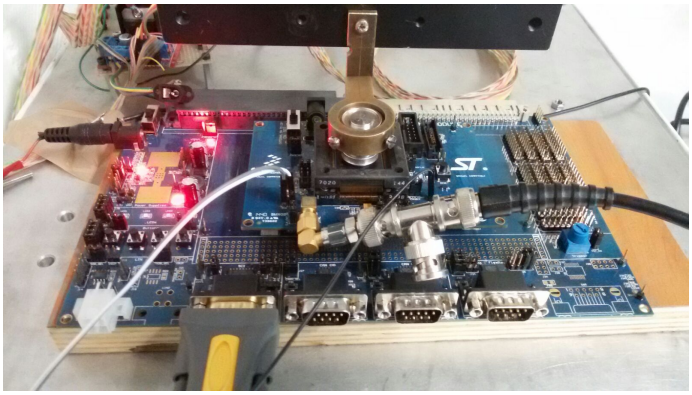

Fig. 2. Test Setup for ^{90}Sr test

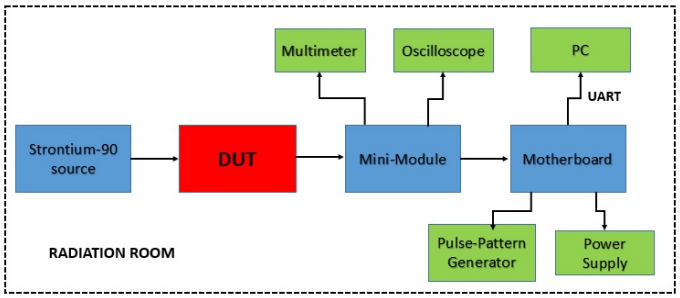

Fig. 3. Diagram of the test setup for ^{90}Sr test

different test procedures have been employed:

Procedure A: this test has been performed in the same conditions as the ^{60}Co test, described in [11]. For this reason the procedure is the same as in [11], and it is reported here:

1) Flash the DUT with the ADC program and read ADC value.
2) Flash the DUT with the "Test as you fly" program and place it for irradiation.
3) Irradiate the device to the dose required, according to the current irradiation step (see Table III-A).
4) Stop the irradiation and execute intermediate operations:
   - Monitor FCCU outputs with the oscilloscope to check correct activity of the device, voltage levels and frequency.
   - Measure current absorption without clock using the power analyzer.
   - Measure V_{core} voltage with a multimeter (DUT unclocked)
   - Reprogram the DUT with the ADC program (using additional motherboard) and measure ADC value.
   - Go to step 2 if other irradiation steps are required (see Table III-A)
5) Test again the DUT after several annealing conditions with the procedure described in step 4

Procedure B: the goal of this procedure is to find out what is the maximum total dose that the DUT can tolerate. Therefore, the DUT has been placed under radiation with no interruption until it showed an unrecoverable failure. During the test time the device was running the "Test-as-you-fly" program, and its behavior was constantly monitored with the laptop. Moreover, the following parameters have been monitored:

- Supply Current absorption
- FCCU outputs: voltage levels and frequency
- V_{core} voltage

For annealing, after irradiation, the device rested at room temperature for 1 day and then for 1 week at 100°C, inside a thermal chamber. Both anneals have been performed in the same electrical bias condition as the irradiations, but without providing the clock signal. During the annealing the board supply current was constantly monitored and electrical measurements have been made following each anneal increment.

*1) **Test results for Procedure A**:* The test results for procedure A are showed in table II. The device failed reprogramming at 25.8 krad(Si). After the annealing procedure the device was unable to recover its functionality and no contact through the JTAG was possible. We can conclude that the DUT reported a permanent failure on the flash controller. In fact, as described in [12], the on-chip charge pump is the first part of the flash memory to fail, although flash memories will continue to work - in read-only mode - at much higher radiation levels. During the 48 hours of irradiation the device experienced a total of 10 automatic resets, probably caused by the FCCU. The results showed a correlation with what happened in the ^{60}Co test, performed in [11]: also with the ^{60}Co the device failed reprogramming at approximately 30 krad(Si). This result shows a remarkable alignment between ^{60}Co and ^{90}Sr tests.

*2) **Test results for Procedure B**:* The device was continuously working under radiation for 247 hours, receiving a total dose of 133 krad(Si). After 247 hours the micro-controller

TABLE I
^{90}Sr TEST: IRRADIATION SCHEDULE FOR PROCEDURE A

Step	Dose Rate [rad/h]	Duration [h]	Total dose [krad(Si)]
1	538	24	12.9
2	538	24	25.8
3	538	24	38.7
4	538	24	51.6

TABLE II
^{90}Sr TEST: RESULTS FOR PROCEDURE A

Step	0 krad(Si)	12.9 krad(Si)	25.8 krad(Si)
Current (clocked) [A]	0.18	0.18	0.18
Current (unclocked) [A]	0.09	0.09	0.09
V_{core} (clocked) [V]	1.268	1.277	1.278
V_{core} (unclocked)[V]	1.250	1.251	1.251
FCCU (J16) [V]	3.68	3.68	3.68
FCCU (J18) [V]	3.52	3.52	3.52
FCCU [KHz]	7.87	7.88	7.88
ADC value	663	66B	-
Reprogramming	yes	yes	no

TABLE III
^{90}Sr TEST: RESULTS FOR PROCEDURE B

Total Dose [krad(Si)]	0	13	39	65	91	117	133
Board supply corrent [mA]	180	179	181	180	180	180	190
V_{core} [V]	1,258	1,259	1,260	1,262	1,264	1,266	1,268
FCCU (J16) [V]	3,5	3,5	3,5	3,5	3,5	3,5	3,7
FCCU (J18) [V]	3,6	3,6	3,6	3,6	3,6	3,6	3,8
FCCU [KHz]	7,81	7,81	7,81	7,82	7,82	7.82	7,82

froze and needed a power supply reset, but the FCCU never showed any fault signal. After the reset the processor got stuck again after a few seconds. Since the device was unable to work continuously for more than 5 seconds, this was considered an unrecoverable fault: irradiation was stopped. After the annealing procedure the device did not recover its functionality: it was still unable to work continuously and, once locked, the FCCU still didn't show any fault signal. None of the tested parameters showed any significant variation, except for the V_{core} voltage, whose behavior is showed in figure 4.The test results for procedure B are showed in table III. During the test the device experienced a total of 51 automatic resets.

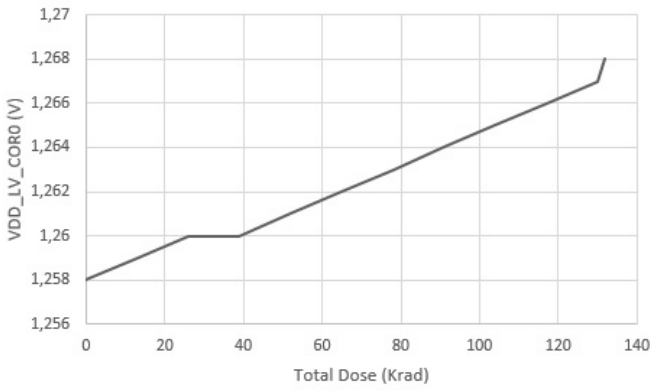

Fig. 4. ^{90}Sr TEST: Behavior of the V_{core} voltage

B. ^{60}Co test

This test has been carried out in the ESA-ESTEC ^{60}Co facility. As stated in [13], in ESTEC the Co-60 source consists of multiple small rods about 50 mm long held around the periphery of a 30mm diameter container. Once the source is raised to the irradiation position, the gamma beam produced by the Co-60 decay exits the irradiator unit through a collimator window into the radiation cell. The facility consists of the radiation cell a and large external control room with cable feed-throughs that enable the remote monitoring and controlling of experiments. For this reason, all the cables used for the measures and for the signaling needed to be long about 6 meters.

The dose rate used for the test has been of 830 rad/h. The test setup contained the following equipment:

- An oscilloscope, to monitor the FCCU pins on the minimodule
- A Pulse-Pattern Generator to provide the clock signal to the device. The clock signal provided was a square wave with 50% duty cycle, 40 MHz frequency, 1.3 V peak to peak with a 0.65 V offset.
- A Current Probe, to monitor the core's DC supply current.
- An Adjustable Output Stabilized Power Supply, to provide power to the board (12 V DC) and monitor the current drain.
- A laptop in the control room to log the program flow signaled from the DUT via UART.

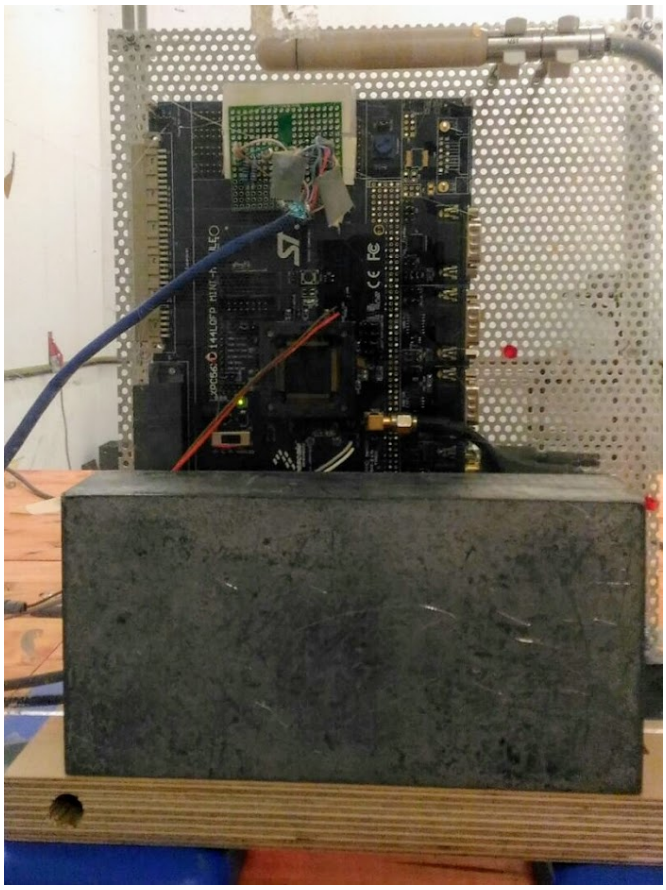

Fig. 5. Test Setup for ^{60}Co test

As shown in figure 6, only the board was stored in the radiation room. Moreover, shielding was necessary to ensure that no peripheral circuitry was interested by the irradiation. To ensure this condition, a lead brick has been arranged in front of all the used ancillary electronics on the board. All the remaining equipment was stored in the control room. As in procedure B of the ^{90}Sr test, the goal of this test is to find out what is the maximum total dose that the DUT can tolerate. Therefore, the DUT has been placed under radiation until it would had showed an unrecoverable failure. During the test

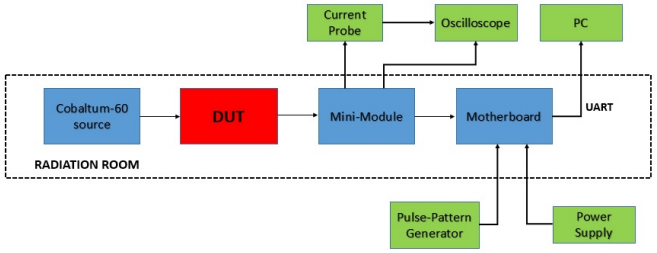

Fig. 6. Diagram of the test setup for ^{60}Co test

time the device was running the "Test-as-you-fly" program, and was constantly signaling its behavior via UART. After the end of the irradiation procedure, the DUT has undergone the annealing procedure described in III-A.

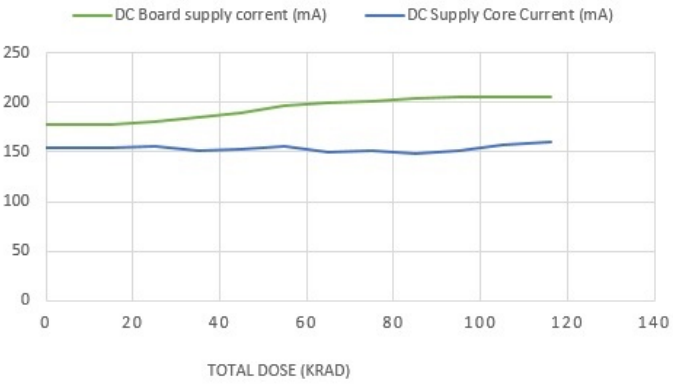

Fig. 7. ^{60}Co TEST: Monitored currents

*1) **Test results**:* when the total dose reached 95 krad(Si) the DC Supply Core Current, while maintaining a stable average value, showed a wave shape very irregular comparing to the one at the test start (see figure 8). After 140 hours of irradiation (with a total dose of 116 krad) the device froze. After some power resets, the device was still unable to work continuously for more than 10 seconds. This was considered an unrecoverable failure and the start of the annealing procedure. Moreover, the FCCU signaling was damaged and the J18 pin experienced a 90% decrease of the peak to peak voltage. During the irradiation time, the DUT experienced a total of 3 automatic resets. The measures are reported here in table IV. After the annealing procedure the FCCU J18 pin recovered its normal behavior and the tested parameters returned to their original values. Nevertheless, the device kept freezing every 10 seconds and the Core Current kept its irregular shape. This results are very similar to those obtained to the procedure B of the ^{90}Sr test. This is a further suggestion about the using of ^{90}Sr as a valid alternative to the ^{60}Co .

IV. Conclusion

This paper showed results from two different test procedures run both under ^{60}Co and ^{90}Sr irradiation. The results show

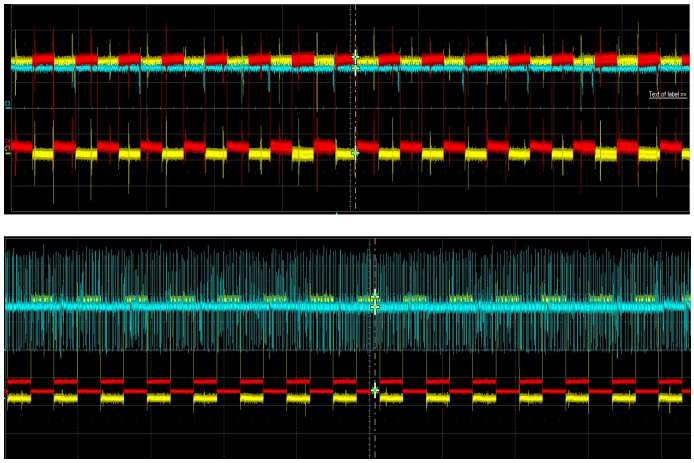

Fig. 8. ^{60}Co TEST: Oscilloscope at test start (top) and at total dose equal to 116 krad(Si) (bottom). In red FCCU J18, in yellow FCCU J16, in cyan Supply Core Current.

Total Dose [krad(Si)]	0	15	45	75	95	105	116
Board supply corrent [mA]	177	177	190	201	205	206	206
Supply Core Current [mA]	154	154	153	151	151	157	160
FCCU (J16) [V]	3,5	3,5	3,5	3,5	3,6	3,6	3,6
FCCU (J18) [V]	3,4	3,4	3,4	3,4	3.5	3.5	0,3
FCCU [KHz]	7,84	7,84	7,84	7,84	7,84	7,84	7,84

TABLE IV
^{60}Co TEST: MONITORED PARAMETERS

remarkable alignment. Procedure A showed that the maximum dose rate before flash reprogramming failure is about 30 krad for ^{60}Co and 25.8 krad(Si) for ^{90}Sr. Procedure B showed that the maximum (lethal) dose rate before the chip stops operating is about 116 krad for ^{60}Co and 133 krad(Si) for ^{90}Sr.

For complex SoCs it is crucial to irradiate the DUT without degrading the performances of the auxiliary circuits, which was much easier to be obtained with a directional source like ^{90}Sr.

In addition, for COTS devices, the radiation qualification is often seriously compromised by the fact that samples with the same component identification may potentially have significantly different radiation hardness characteristics. Testing with ^{90}Sr can then be exploited for the study of lot-to-lot variations.

These results suggest that electron irradiation with ^{90}Sr/^{90}Y source could represent in future a viable, low-cost and suitable solution for screening of components to be used in space applications.

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