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***Abstract*—In the domain of power electronics, especially for applications requiring high power, high temperature, and high frequency, Silicon Carbide Metal Oxide Semiconductor Field-Effect Transistors (SiC MOSFETs) stand out due to their excellent properties such as high thermal conductivity, elevated breakdown electric field, and minimal power loss. These devices are pivotal in the reliability and safety of electric vehicles, where avalanche-induced failures represent a significant risk within automotive uses. This study extensively explores the avalanche ruggedness of both planar and trench SiC MOSFET configurations through a combination of Unclamped Inductive Switching (UIS) testing in single and multiple pulse scenarios, and Technology Computer-Aided Design (TCAD) simulations. Initial UIS experiments revealed the primary failure mechanisms and their origins in SiC MOSFETs. Following empirical analysis, TCAD simulations were employed to develop comprehensive models of these devices, enhancing the understanding of failure dynamics during UIS conditions. The integration of empirical and simulation data supports the creation of advanced strategies to reduce the risk of avalanche failures, thereby enhancing the durability and reliability of Wide Bandgap Semiconductor devices.**

Keywords—SiC MOSFET; UIS; Avalanche failure; Avalanche ruggedness

I. Introduction

Silicon Carbide (SiC), distinguished for its remarkable physical attributes such as an exceptionally high breakdown electric field and superior thermal conductivity, stands as a paramount example of wide bandgap semiconductor devices. These characteristics make SiC devices highly suited for surpassing traditional silicon-based power devices in efficiency and performance. As manufacturing technologies have evolved and costs have diminished, SiC MOSFETs have increasingly been adopted in emerging sectors such as electric vehicles powered by new energy sources, photovoltaic power generation, and advanced power supplies[1]. The dynamic reliability of these SiC MOSFETs under extreme operational stresses, including conditions of high temperature and voltage, has become a critical area of research. This reliability encompasses challenges such as avalanche, short-circuit, and surge reliability. Avalanche reliability, in particular, concerns the device's capability to manage sudden overvoltage incidents that result from the rapid release of stored energy in inductive or reactive components during swift switching events, posing significant challenges for device stability and operational integrity.

In the context of automotive applications, the failure of SiC MOSFETs due to avalanche events is identified as a catastrophic fault arising under conditions such as substantial voltage or current surges, where the device fails to endure significant electrothermal stresses[2]. It is, therefore, essential to conduct evaluations and tests on the avalanche endurance of SiC MOSFETs to verify their dependability and durability in harsh environments. Unclamped Inductive Switching (UIS) tests serve as a method to examine the performance of MOSFETs when subjected to avalanche scenarios, ascertain the highest avalanche energy causing device breakdown, and thereby aid in the development of more dependable power electronics systems. Research by Saito et al[3] involved the enhancement of UIS robustness in SiC MOSFETs through the integration of parallel-connected varistors, aimed at augmenting the cutoff current capabilities of solid-state circuit breakers. Jiao et al[4] undertook experimental evaluations across a temperature spectrum from 25°C to 125°C, alongside TCAD simulations, to explore the avalanche durability and the underlying failure mechanisms in commercial 1200V planar SiC MOSFETs during single-pulse UIS trials. Further, Luo et al[5] executed UIS experiments on planar SiC MOSFETs featuring hexagonal cell topology with varied JFET widths. Ren et al[6] probed into the single-pulse avalanche durability and the failure mechanisms pertinent to SiC MOSFETs under UIS examinations, contrasting these with Si IGBTs, and pointed out the triggering of the parasitic BJT within SiC MOSFET devices as the cause of avalanche failures. Their findings also disclosed that, given the chip area of SiC MOSFETs is approximately one-seventh that of Si IGBTs, their avalanche robustness is merely around 30% in comparison. Nonetheless, the failure dynamics of SiC MOSFETs across different configurations are not uniform, and the investigations into both single-pulse and multi-pulse avalanche failures remain incomplete, indicating the necessity for further studies in this domain.

This study has conducted a comprehensive investigation into the failure dynamics of both planar and trench SiC MOSFETs when subjected to UIS testing in single-pulse and multi-pulse scenarios, integrating both experimental data and simulation analysis.

II. Experimental Setup and Methods

A. Experimental Setup

This research evaluates the avalanche robustness of 1200V commercial planar and trench SiC MOSFETs utilizing both single-pulse and multi-pulse UIS testing methodologies. The UIS experiments employed a T334A system configured with an inductive load for avalanche testing, while static parameter evaluations were executed with a Keysight B1505A device as depicted in Fig. 1. A comparative analysis was performed on the chosen SiC MOSFETs, and the fundamental parameters of these MOSFETs used in the experiments are detailed in Table I.

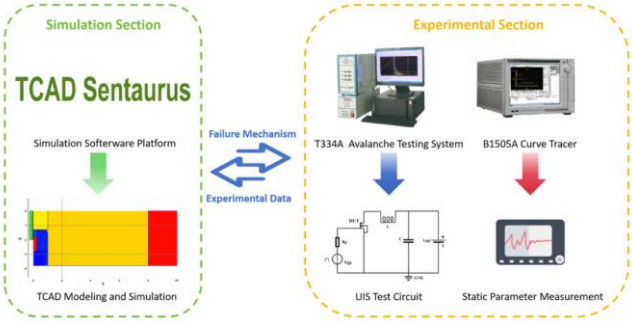

Fig. 1. A schematic view of the experimental equipment

TABLE I. Basic Parameters of SiC MOSFET Devices

Device	Parameters		
	V_{DS}	I_{DS}	R_{dson}
Planar-gate device	1200V	38A (T_C = 25°C, $R_{th\ (j\text{-}c,max)}$)	75mΩ (V_{GS} = 18 V, I_{DS} = 20 A, T_J = 25°C)
Trench-gate device	1200V	31A (T_C = 25°C, $R_{th\ (j\text{-}c,max)}$)	80mΩ (V_{GS} = 18V, I_{DS} = 10A, T_J = 25°C)

B. Experimental methods

Upon the activation of the gate-to-source voltage V_{gs}, the device under test (DUT) becomes operational, allowing the direct current power source V_{dd} to charge the inductor L. The subsequent instantaneous cessation of V_{gs} to zero deactivates the DUT, and the swift alteration in current generates an avalanche voltage V_{ds} across the inductor. This, in turn, leads to avalanche breakdown of the DUT, producing an avalanche current denoted as I_{av}. The duration for which the device sustains this avalanche breakdown is measured as I_{av}. Simultaneously, the current that flows through the device at any point is referred to as I_{ds}. The described phenomena are mathematically articulated through the equations below:

$$V_B = L\frac{di}{dt} + V_{dd} \tag{1}$$

$$t_{av} = \frac{L}{V_B - V_{dd}} I_{av} \tag{2}$$

$$I_{ds} = \frac{V_B - V_{dd}}{L} t \tag{3}$$

By integrating the principles described in equations (2) and (3), the expression for the peak avalanche energy E_{av} that the device absorbs is formulated and demonstrated in equation (4).

$$E_{av} = \int_0^{t_{av}} V_B\, I_{ds}\, dt = \frac{1}{2} L\, I_{av}^2 \frac{V_B}{(V_B - V_{dd})} \tag{4}$$

Following the experimental setup and theoretical framework previously described, both planar and trench variants of SiC MOSFETs underwent testing under both single-pulse and multi-pulse UIS conditions.

III. UIS Test Results

A. Single-pulse UIS Tests

UIS testing was performed on both planar and trench SiC MOSFETs, capturing the voltage and current waveforms of the devices under test in real time. To standardize experimental conditions, the gate bias voltage V_g was consistently set at 15 V, the gate resistor R_g at 75 Ω, the inductance at 5 mH, and the charging voltage V_{dd} at 50 V.

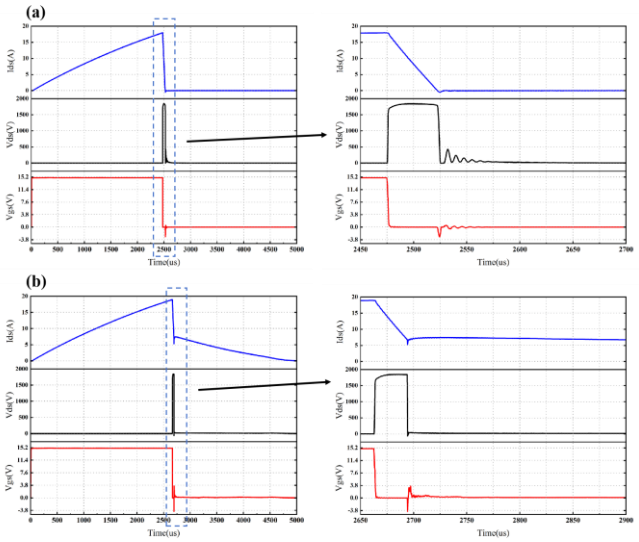

Fig. 2. Waveforms of single-pulse avalanche failure in planar devices. (a) Before failure. (b) After failure.

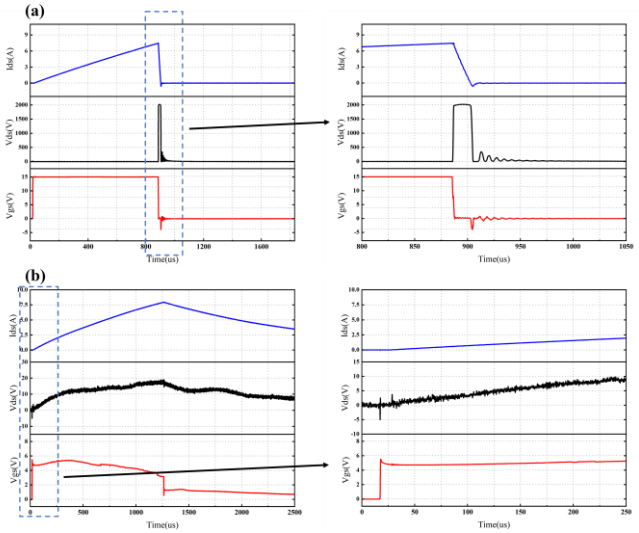

Fig. 3. Waveforms of single-pulse avalanche failure in trench devices. (a) Before failure. (b) After failure.

As depicted in Fig. 2, for the planar SiC MOSFET, at lower drain current Ids levels, the device manages only a reduced avalanche energy as outlined by equation (4). Under these conditions, the device is capable of being switched off

normally, demonstrating that it has not undergone an avalanche failure because I_{ds} retains normal recovery attributes. Conversely, when Ids escalates to Iav, the avalanche energy of the device peaks at its maximum tolerable threshold, E_{av}. A reduction of V_{gs} to zero does not allow Ids to decrease to zero swiftly, resulting in an inability to switch off the device properly, thus signifying an avalanche failure. In Fig. 3, the waveforms of a trench SiC MOSFET are shown before and after encountering a single-pulse avalanche failure. As illustrated in Fig. 3(a), prior to an avalanche failure, the device switches off normally once V_{gs} returns to zero, with Ids declining to zero within 50μs. However, as depicted in Fig. 3(b), post-avalanche failure, V_{gs} fails to achieve the experimentally established 15 V, and the drain-source voltage V_{ds}, which is expected to be zero, displays oscillations. This behavior suggests a loss of gate control over the device's channel, indicating a possible gate breakdown.

Several devices under test (DUTs) underwent single-pulse UIS testing, with the computation of the peak avalanche energy E_{av} for each DUT carried out according to equation (4), as illustrated in Fig. 4. A statistical evaluation highlighted that planar devices typically possess an E_{av} markedly higher than that of trench devices and display enhanced uniformity. This disparity is underscored by the differences in the standard deviations of E_{av} values between the planar and trench types.

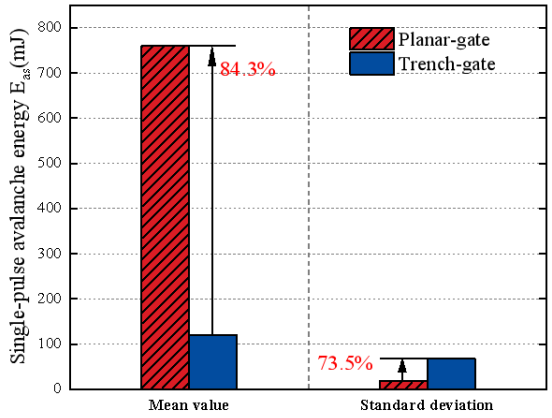

Fig. 4. A schematic view of the experimental equipment

B. *Multi-pulse UIS Tests*

To enhance the simulation of real-world conditions, multiple pulse UIS tests were applied to both planar and trench power devices. In these tests, each pulse aimed to impart an avalanche energy corresponding to 60% of the device's maximum E_{av}, maintaining a constant interval across the series of avalanches. Measurements of the device under test (DUT) static characteristics were systematically performed after intervals of 5000 cycles, and continuous monitoring of operational waveforms was maintained until the point of failure. The outcomes illustrated in Fig. 5 and Fig. 6 revealed consistent threshold voltage (V_{th}) and reverse breakdown voltage (BVDSS) across 80,000 cycles for both device types. Notably, Fig. 6 highlights a progressive increase in the on-resistance (R_{dson}) for planar devices, initially reaching 132 mΩ after 50,000 cycles and subsequently rising more rapidly. By the completion of 80,000 cycles, the R_{dson} value had escalated to 300 mΩ, though the planar devices continued to exhibit clear forward conduction properties. Following another 410 cycles of multi-pulse stress, planar devices ultimately failed, and further data collection ceased. Conversely, trench devices demonstrated resilience, showing no failure under similar conditions.

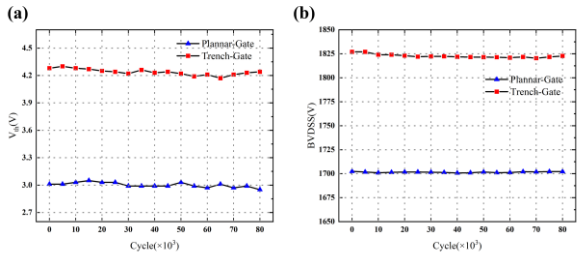

Fig. 5. Parameter degradation of planar devices and trench devices under multi-pulse avalanche. (a) V_{th}. (b) BVDSS.

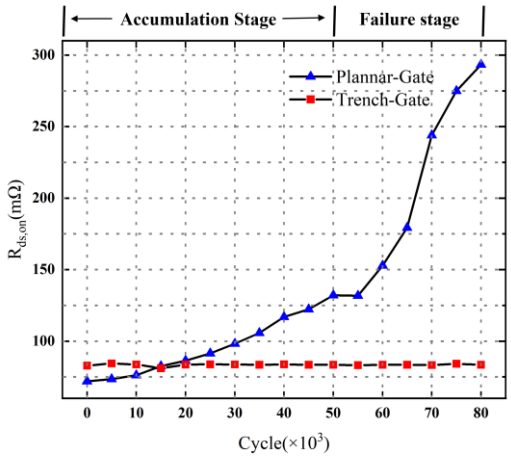

Fig. 6. R_{dson} degradation of planar devices and trench devices under multi-pulse avalanche.

IV. Simulation and Failure Analysis

A. *TCAD Simulation*

To delve deeper into the factors contributing to single-pulse avalanche breakdown in planar and trench SiC MOSFETs, a detailed TCAD simulation was carried out. The configuration of the device is presented in Fig. 7, while the half-cell setup employed for this simulation is illustrated in Fig. 8. The simulation was designed to accurately mirror the operational dynamics of SiC MOSFETs by integrating several models: the Shockley-Read-Hall and Auger recombination processes, mobility and velocity saturation behaviors, self-heating effects, and impact ionization phenomena.

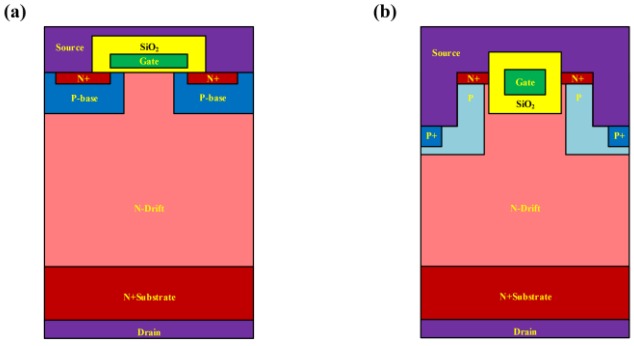

Fig. 7. Schematic of device structures. (a) Planar. (b) Trench.

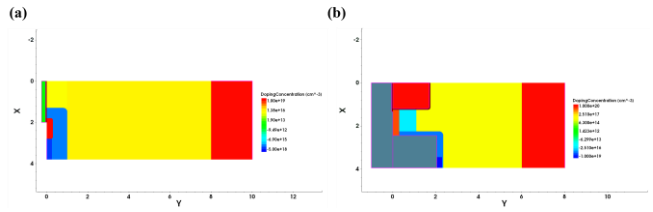

Fig. 8. Schematic of TCAD simulation semi-cellular structure. (a) Plana. (b) Trench.

The settings for the TCAD simulations were meticulously adjusted to emulate the electrical and thermal scenarios faced by the devices during the UIS testing. The figures showing potential distributions post-single-pulse avalanche failures for both planar and trench devices are captured in Fig. 9. As depicted in Fig. 9(b), the trench device, because of its unique embedded gate structure, displays a concentrated potential line formation at the lower corner of the gate oxide. In contrast, the potential across the planar device appears more uniform. Fig. 10 presents simulations of electric field intensity for both device types. Notably, Fig. 10(a) highlights a sharp increase in electric field intensity at the base of the gate oxide in the trench device, which precipitates the gate oxide's degradation. On the other hand, although the planar device also shows a peak in electric field intensity near the junction of the gate oxide layer and the JFET region, this peak is considerably milder compared to that in the trench device and does not suffice to induce gate oxide failure. A significantly elevated electric field intensity was detected at the base of the P-base region in the planar device. Further structural analysis revealed that this anomaly is linked to the activation of the internal parasitic BJT, as illustrated in Fig. 11(a). The intrinsic N-P-N configuration of the planar device tends to initiate a latch-up effect, which, through positive feedback, impedes the device's ability to shut off, thereby intensifying the current flow. This leads to excessive thermal generation or current overload, culminating in the device's failure, as corroborated by Fig. 11.

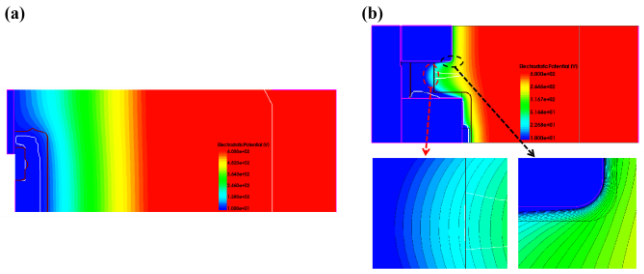

Fig. 9. Potential distribution. (a) Planar. (b) Trench.

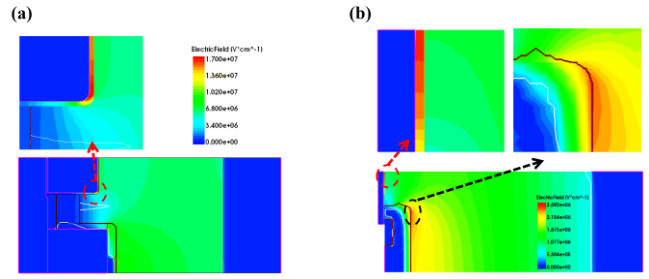

Fig. 10. Electric field intensity distribution. (a) Planar. (b) Trench.

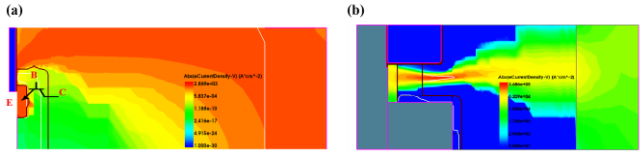

Fig. 11. Electron current density distribution. (a) Planar. (b) Trench.

B. *Failure Analysis*

Following the simulations, rigorous failure analysis confirmed the initial conclusions and validated the hypotheses posited in the testing section. Employing failure analysis techniques including C-mode Scanning Acoustic Microscopy (CSAM), de-encapsulation inspection, Scanning Electron Microscopy (SEM), and Energy Dispersive Spectroscopy (EDS), the causes of failure in the planar devices were examined, as presented in Fig. 12.

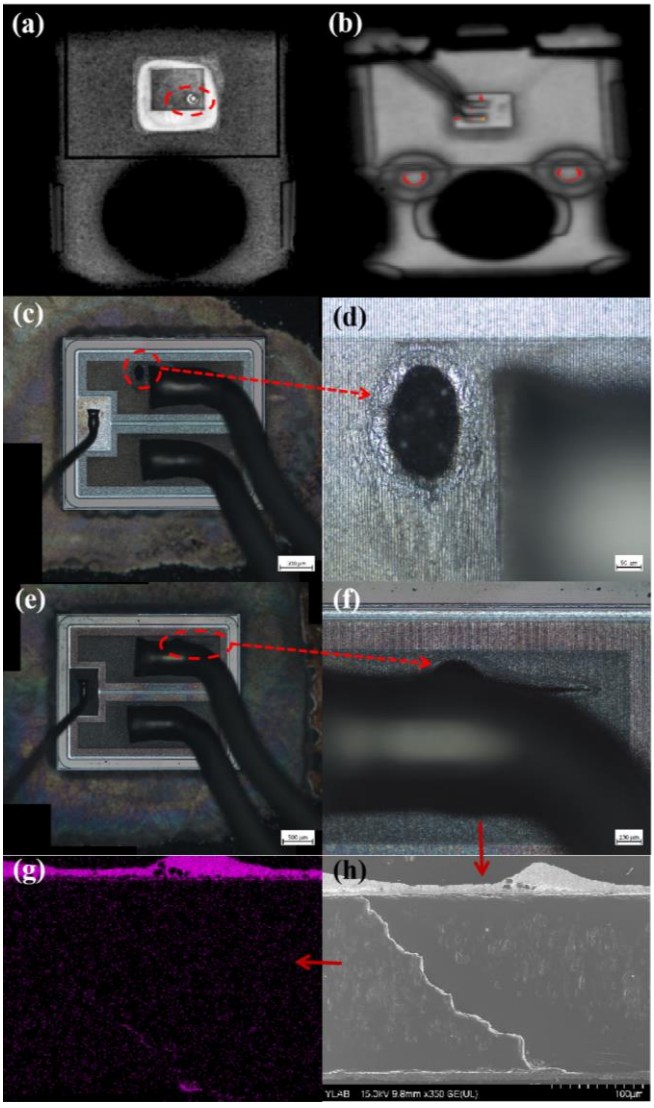

Fig. 12. Failure analysis of failed planar devices. (a-b) CSAM. (c-f) De-encapsulation inspection. (h) SEM. (g) EDS of lead.

Observations revealed that devices subjected to single-pulse avalanche testing showed metal surface melting. This phenomenon, coupled with the simulation insights, implies that conduction through the parasitic BJT prevented device shutoff, leading to latch-up effects and resultant heat

accumulation. The temperatures reached were sufficient to melt aluminum, explaining the observed metal surface degradation. De-encapsulation exposed significant burn damage at the interfaces where the aluminum leads meet the active regions of devices affected by multi-pulse avalanche failure. Detailed SEM and EDS analyses identified severe step-like damage at these junctions and detected the presence of Pb-containing solder on the surface. This analysis, integrated with findings from the UIS testing, indicates that thermal fatigue, caused by alternating thermal stresses at the contact points during numerous pulse cycles, led to noticeable degradation in R_{dson}. An increase in R_{dson} elevates the avalanche current I_{av}, intensifying Joule heating. If this heat cannot be dissipated promptly, it accumulates, causing burn damage at the contact points between the active areas and the leads, ultimately leading to device failure.

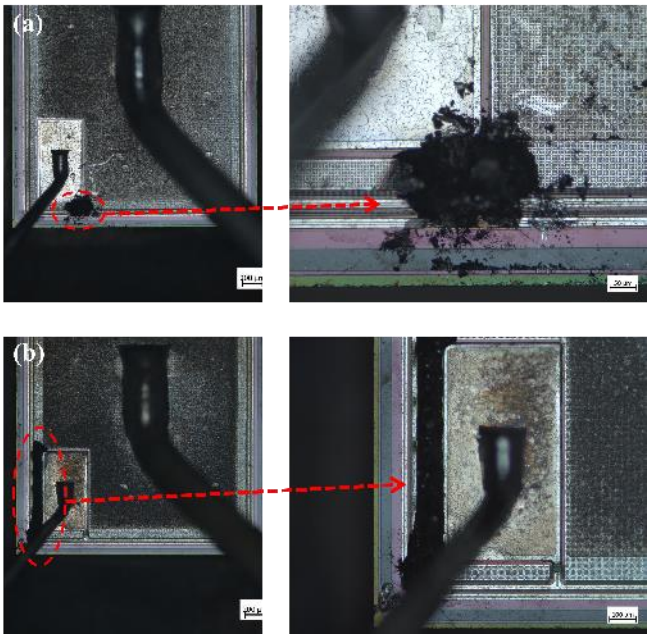

Fig. 13. Gate breakdown phenomenon of failed trench devices.

De-encapsulation studies conducted on the trench devices, as illustrated in Fig. 13, disclosed substantial gate damage in several devices that failed during single-pulse tests. Synthesizing these findings with the results from simulation studies, it appears that the predominant cause of failure in these trench devices during single-pulse avalanches is attributed to the intense electric fields generated at the moment of avalanche, culminating in gate degradation and irreversible harm.

V. Conclusion

This study has thoroughly analyzed the behavior of planar and trench SiC MOSFETs under single-pulse and multi-pulse Unclamped Inductive Switching (UIS). Through a synthesis of experimental data, TCAD simulations, and a variety of failure analysis methods, significant insights have been gained:

1) A fusion of experimental results and simulation data offers a detailed understanding of avalanche failure mechanisms affecting both planar and trench SiC MOSFETs.
2) In planar devices, the activation of parasitic BJT and subsequent latch-up phenomena have been pinpointed as the primary culprits behind single-pulse avalanche failures, leading to surface metal melting within the active areas.
3) Thermal fatigue has been identified as the predominant factor leading to the degradation of R_{dson} and eventual failure in planar gate devices subjected to repeated avalanche stresses.
4) The unique structural attributes of trench SiC MOSFETs result in heightened electric fields during single-pulse avalanches, primarily concentrated at the gate oxide corners, which precipitates irreversible gate breakdown. This structural factor generally yields a lower E_{av} for trench devices in comparison to planar types.

Acknowledgment

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