Implementation of a high-voltage MMC submodule

For a multilevel modular converter

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by

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Abstract

In this master thesis, the design and implementation of a high-voltage switch using series-connected Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is discussed. A high-voltage switch is needed for applications such as high-voltage DC converters. Multilevel modular converters (MMCs) can also aid in the voltage-blocking capabilities of converters. MMCs use multiple submodules to block the full voltage. Every submodule thus only blocks a part of the full voltage. Each submodule needs multiple components that can be expensive, like voltage sensors and gate drive circuitry. By having the submodules block a higher voltage, fewer components are needed. By implementing a higher voltage blocking switch into such a submodule, cost and components can be spared by having a lower total amount of submodules.

Current technologies of high-voltage switches are MOSFETs, insulated gate bipolar transistors, thyristors or electro-mechanical switches. MOSFETs have the advantage of being faster and have lower losses than the other technologies. The downside of using MOSFETs is that the voltage-blocking capability is lower than the other technologies. This could be solved by connecting multiple MOSFETs in series for a higher blocking voltage. To do this, care has to be taken that the MOSFETs turn on- and off at the same time. They also need to share the voltage equally to take full advantage of the blocking voltage of each MOSFET.

A cost-effective way to implement a high-voltage switch using series-connected MOSFETs is to use capacitive coupling. In this method, the gate charge needed to turn the MOSFETs on is stored in capacitors. When the first MOSFET is turned on, the other series-connected MOSFETs will also turn on. This method has the downside that the switch can only be turned on for a limited amount of time (a few microseconds) and that the voltage balancing is dependent on the load, the switching frequency and the parasitics of the circuit. For this reason, a single high-voltage MOSFET was used in this project, even though it can be slower and more lossy than the series-connected switch.

An MMC submodule was made using a full-bridge configuration. Additionally required components such as a gate signal generator, power supply, voltage- and current sensors, and fault protection were also designed, built and tested. In this way, a functioning MMC submodule was created that can be used with a capacitor or an isolated transformer as its source.

Preface

The goal of this master thesis was to provide a prototype and a report after ten months of work. During this time, I massively appreciated all the help from Professor Mohamad Ghafarian Niasar and Sohrab Ghafoor. I would also like to thank Professor Peter Vaessen for his invaluable feedback. A special thanks goes out to my friends Xi Tao, Jolijn, and Namo for studying together with me and motivating me to work harder. Finally, I would like to thank my parents for their support and words of encouragement during the project.

Brecht Hurkmans
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Contents

1 Introduction

The energy supply in the world is moving more towards sustainable energy sources like wind and solar energy [1]. For these applications, power electronic switches are needed. With these switches, the energy produced by these sustainable sources can be converted into a desired form. To connect a solar farm to the grid for example, an inverter is needed to convert its DC output into a 50 Hz AC waveform that can be transported over the grid. This conversion can introduce noise into the grid [2]. This has an influence on the high-voltage cables, that can be degraded by this noise [3]. This influence has to be accounted for. A high-speed high-voltage converter can be made to simulate the effect of power electronic noise on high-voltage cables. This will require a converter that can generate arbitrary wave shapes. This converter will need switches to generate the required wave shape. These switches have a certain breakdown voltage that cannot be exceeded, or they will break down. Higher breakdown voltage switches are often more expensive and slower than lower voltage switches. A more cost-effective solution could be to use multiple lower voltage switches. These can be connected in series to block a higher voltage. However, a problem with this approach is that they have to be switched at the same time. The purpose of this project is to analyze and implement a high-voltage switch, using the series connection of two or more MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). MOSFETs are faster and have a lower on-resistance compared to IGBTs (Isolated Gate Bipolar Transistors), but they generally have a lower breakdown voltage. Four switches can be used in a H-bridge configuration inside a full-bridge Multilevel Modular Converter (MMC) submodule. This MMC submodule will be operated at 4 kV, to be used in a high-voltage MMC that can be used to test high-voltage cables. A schematic overview of this project can be seen in Figure 1.1. The scope of this project is limited to the design, building, and testing of the MMC submodule.

The objective of this master thesis is to compare ways of implementing a high-voltage switch for a fast multilevel modular converter. The next objective is to implement this switch in a full-bridge configuration that can be used in a multilevel modular converter. Then, the surrounding circuitry for the driving, powering and measurement of this full-bridge will be designed and implemented to complete the submodule. For this, a literature review will be conducted. After that, a switch topology will be selected to be implemented in a submodule. This topology will be simulated and after that, a prototype will be made for the switch, the full-bridge and a full submodule. These prototypes will be tested to confirm the working of each of these prototypes, and they will be improved where necessary.

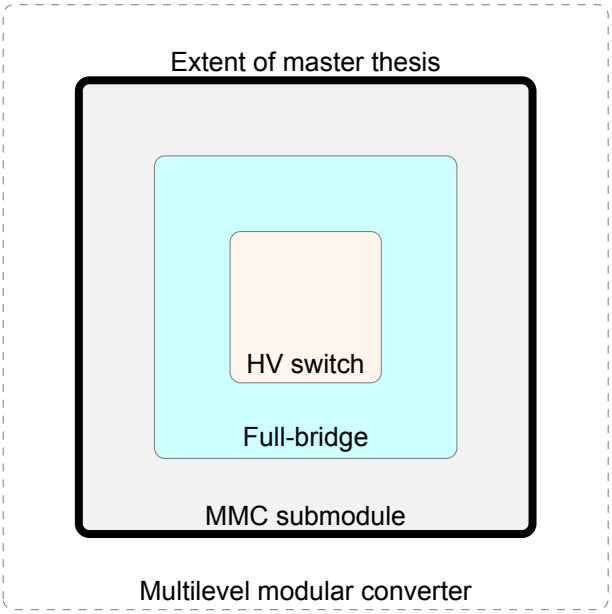

Figure 1.1: Schematic overview of the project

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MOSFETs

Metal oxide semiconductor field effect transistors (MOSFETs) are a type of switch that can be used for switching high-voltages. Other types include thyristors, bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs). These other types of transistors are slower than MOSFETs. Since the switch will be used in an arbitrary waveform generator, switching speed is very important. That is why a MOSFET will be used. There are several types of MOSFETs. Silicon, GaN, SiC and even diamond [4].

2.1. Silicon carbide MOSFETs

Silicon carbide (SiC) MOSFETs are generally faster than silicon MOSFETs. They also have a higher breakdown voltage than MOSFETs and gallium nitride transistors. This makes silicon carbide MOSFETs a good candidate for high-voltage high-speed switching. SiC MOSFETs are currently readily available up to 1.7 kV. This is still not enough of a blocking voltage for some high-voltage applications. Multilevel converters can be used to increase the blocking voltage using more switches. MOSFETs can also be placed in series to increase their blocking voltage. This will be discussed in chapter 3.

2.2. Parasitics

MOSFETs do not function like a perfect switch. The MOSFET has some delay, a finite switching speed, and a maximum power dissipation for example. These characteristics can be modeled using passive components around an idealized version of the MOSFET. The construction of the power MOSFET can be seen in Figure 2.1.

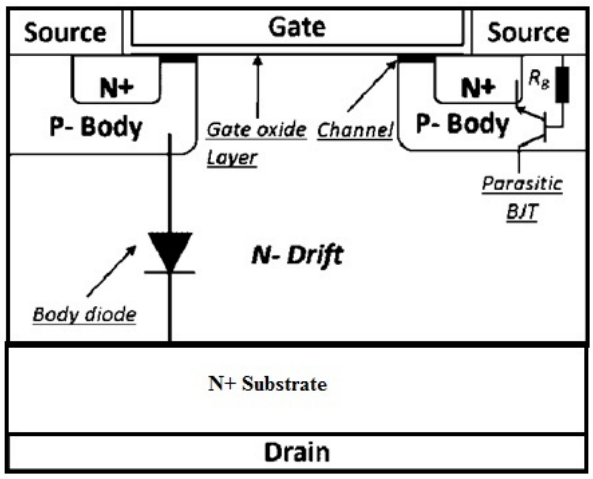


Figure 2.1: Power MOSFET construction [5]

2.2.1. Parasitic BJT
Due to the constuction of the MOSFET, there is a pnp-junction present inside the MOSFET. This pnp-junction acts like a bipolar junction transistor (BJT). If this BJT turns on, the MOSFET will be turned on until the drain to source voltage becomes low enough. This is called latch up. This latch up can be prevented by limiting the rise time of the voltage across the MOSFET. This can be done by using a gate resistor to limit the rise of the gate to source voltage and thus the drain to source voltage.

2.2.2. Body diode
Due to the construction of the MOSFET, there is also a pn-junction present in the MOSFET. This will act like an antiparallel diode to the MOSFET. This diode can be used to provide a path for inductive loads to discharge. In designs, this diode should be taken into account, since a current can flow through the MOSFET if the diode is forwardly biased.

2.2.3. Resistances
The MOSFET also has some resistances. The material it is made of has a finite resistance. The main resistances that should be taken into account are the gate-to-source resistance, the drain-to-source resistance when the MOSFET is turned on, and the drain-to-source resistance when the MOSFET is turned off. These resistances cause a leakage current, which should be taken into account in low-current or balanced situations. The drain-to-source resistance of the MOSFET is mainly caused by the N- doped region in Figure 2.1. This region is also responsible for the voltage isolation of the MOSFET. A thicker N- region will thus cause the MOSFET to have a higher voltage blocking capability, but its on-resistance will also be increased.

2.2.4. Capacitances
Parallel surfaces inside the MOSFET cause parasitic capacitances. According to equation 2.1, this capacitance (C) depends on the area of the surfaces (A), the dielectric constant (ϵ), and the distance (d) between them. The main capacitances that are of importance are the gate-to-source capacitance, the gate-to-drain capacitance, and the drain-to-source capacitance. These capacitances slow down the working of the MOSFET because the voltage over them cannot change instantaneously. The gate-to-source capacitance and the gate-to-drain capacitance will cause a delay between the gate signal being applied and the MOSFET turning on. This is called the input capacitance of the MOSFET, or C_{iss}. The gate-to-drain capacitance and the drain-to-source capacitance will cause the MOSFET to have a rise time when it is turned off. This is called the output capacitance of the MOSFET or C_{oss}.

$$C = \frac{\epsilon A}{d} \tag{2.1}$$

2.3. Power loss
A MOSFET has two types of power losses: conduction loss and switching loss. Conduction losses are caused by the on-resistance of the MOSFET. When the MOSFET is turned on, it has a certain resistance. A current through this resistance will cause the conduction losses. A lower on-resistance will thus help reduce the conduction losses. Switching losses are caused by the current and voltage of the MOSFET overlapping during switching. This is caused by the parasitic output capacitance of the MOSFET charging and discharging.

$$P_{cond} = I_D^2 R_{DS,on} \tag{2.2}$$

$$P_{sw} = \frac{1}{2} C_{OSS} V_{DS,off} f_s w \tag{2.3}$$

2.3.1. Snubbers
Snubbers can be used to shift the switching losses away from a switch. It does so by delaying the rise of the voltage during turn-off or by delaying the rise of the current during turn-on. Reactive components like inductors and capacitors are used for this.

3

Series-connected MOSFETs

There are several ways to implement series-connected MOSFETs. The most important part is the balancing of the voltage over the MOSFETs. Balance has to be achieved in the static case (steady state) and the dynamic state (during switching). An imbalance can be caused by the manufacturing differences between devices, mismatch in the gate signals or differences between the device surroundings (e.g. temperature and parasitic capacitance). For series-connected MOSFETs, it is not possible to connect all the gates to one single gate driver. This is because all the MOSFETs need a certain gate-to-source voltage. The source voltages will be different when they are off, therefore it is not possible to drive them using the same gate driver.

3.1. Parasitics

Parasitic capacitance and parasitic resistance can cause voltage imbalance between series-connected MOSFETs [6]. These parasitics are present because of the construction of the MOSFETs. The insulation has a finite resistance and due to the proximity of the gate, drain, and source, a capacitance is present. This capacitance can be modelled as a capacitance between each of the ports. The parasitic capacitances can be seen in Figure 3.1. Here, C_{gd} is the gate-to-drain capacitance, C_{ds} is the drain-to-source capacitance, and C_{gs} is the gate-to-source capacitance. There will also be parasitic capacitances present from each node to the ground of the system, depending on their proximity.

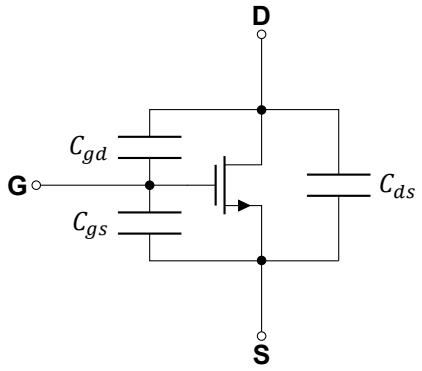


Figure 3.1: MOSFET with parasitic capacitances

3.2. Static balancing

In [6], Lin et al. investigated the static voltage balancing of series-connected MOSFETs. It was found that the parasitic capacitances from the gate can introduce a significant voltage imbalance. It is thus important to take the parasitic capacitance between the gate and heatsink, as well as the capacitance between the gate and the bus into account. The current during the turn-off transition of the MOSFET also plays a part in the imbalance [6].

In the steady state, a voltage divider consisting of resistors can be used. These resistors are placed in parallel with each MOSFET. A high enough current should flow through these resistors so that the parasitic leakage current is insignificant compared to the balancing current. In this way, the voltage will be divided evenly over the MOSFETs. As a rule of thumb, this current could be ten times larger than the leakage current [6]. The value for the balancing resistor can thus be calculated using equation 3.1. In this equation, $R_{balance}$ is the value of the balancing resistor in Ω, $V_{ds,off}$ is the drain to source off-voltage of the MOSFET in volt, and $I_{leakage}$ is the leakage current in ampere. This resistor should also be able to withstand the full off-voltage of the MOSFET and it should be able to dissipate the power.

$$R_{balance} \leq \frac{V_{ds,off}}{I_{leakage}} \cdot \frac{1}{10} \tag{3.1}$$

3.3. Dynamic balancing

The MOSFETs should stay balanced during the dynamic operation. After the turn-on transition, the voltage will be very low since the MOSFETs are turned on. After the turn-off transition however, it is important that the MOSFETs block approximately the same voltage. This turn-off transition is thus the most important part of the dynamic balancing [6]. To balance this transition, the $\frac{dV_{ds}}{dt}$ has to be controlled. This can be done by influencing the gate current, delaying the gate signals for the faster MOSFETs or coupling the gates together using inductors or capacitors.

3.3.1. Active gate driver

The first way is to control the gate current using an active gate driver [7–9]. By controlling the gate current when the MOSFET is turning off, the slope of the drain-to-source voltage can be controlled. With appropriate feedback and control, this can balance the voltage over each MOSFET.

The gate current can be controlled by inserting (or not inserting) a resistor between the gate driver and the gate of the MOSFET [7, 9]. It can also be done by using bipolar junction transistors to source or sink more current from the gate [8]. These methods require feedback to measure the voltage balance and adjust the gate current accordingly. This requires fast electronics and a control scheme.

3.3.2. Delay compensation

The second way is to compensate with delay between the different gate drivers [10]. Not only the inherent delay between gate drivers is compensated, but also the difference in fall time can be compensated using the delay between the gate drivers. In this way, the voltage can be balanced using appropriate feedback and control.

3.3.3. Inductive coupling

The third way is to couple the gates together using coupled inductors [11, 12]. By coupling the gates using inductors, the delay between the gate drivers can be mitigated. If one of them turns on first, this will cause the other gate to also rise. Using the coupling between these inductors and the snubber inductor, there is a sort of feedback implemented, without the use of electronics.

3.3.4. Capacitive coupling

The fourth way is to couple the gates together using capacitors [13–19]. By using a capacitor on the gate of the MOSFET, the charge can be stored to turn the MOSFET on or off. By turning the lowest MOSFET on, the gate capacitors will discharge into the parasitic capacitors, turning the other MOSFETs on.

The capacitive coupling can be implemented by inserting a capacitance between the gates and different points in the circuit. Pang et al. investigated the different placements of the capacitors. It was found that placing a capacitor between the gate and ground yielded the best balance [15].

3.3.5. Comparison

From the different ways of implementing series-connected MOSFETs, the active gate driver and delay compensation seem like the most robust options. Using the feedback, they can adjust to differences in the switching times between the MOSFETs. A downside, however, is that the feedback needs to be

fast and implemented using expensive electronics. This feedback can also make the switching times slower [20].

The inductive coupling has the advantage of not needing electronics for its feedback. It does however require bulky and intricate components for the coupling. This can lead to higher manufacturing costs, as well as variation between the inductive components.

The capacitive coupling seems like the most cost-effective option. It will be further analyzed and implemented into a prototype switch.

3.4. Selected topology

The topology described in [14–16] was used because of its cost-effectiveness. It only requires a single gate driver and a few passive components. This same structure can also be enhanced by adding zener diodes between the gate and source to prevent a gate-to-source overvoltage [13]. It can also be expanded by supplementing extra gate current when the MOSFET is turned on, like in [17–19]. This does require extra active components, which makes the circuit more expensive.

In the steady state, the resistors in parallel with the switches will make sure that the voltage is balanced. The balance resistors should balance out the leakage current of the MOSFETs. This can be accomplished by sizing the resistor according to Equation 3.1.

When the switch get turned on, the gate-to-source voltage of the first switch will rise by the gate driver. This will cause the voltage over M0 to drop when M0 turns on. This will create a potential difference between the gate and source of M1 which cause M1 to turn on. The voltage over M1 will also drop and thus cause a V_{gs} for M2 causing M2 to turn on and so on. This propagates until all the switches are on. The capacitors will then be slowly discharged through the R_{1i} resistors which limits the on-time.

When the switch get turned off, the gate-to-source voltage of the first switch will fall by the gate driver. This discharges C_{gd} and C_{gs} through R_{11} until the threshold voltage is reached. This will cause M0 to turn off. Then the voltage of M0 will rise due to C_{ds} getting charged by the voltage source through R_L and C_1 through R_L and R_{11}. When the threshold voltage of M1 is reached in this way, it will turn off. The M1 MOSFET will turn off, and its C_{ds} gets charged through R_L, along with C_2 through R_L and R_{12}. This will continue on, until all the MOSFETs are off and the capacitances are charged.

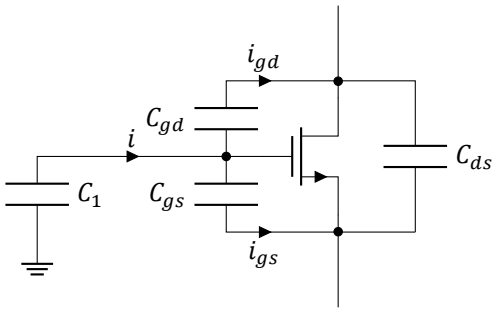


Figure 3.3: MOSFET with parasitics and gate capacitor

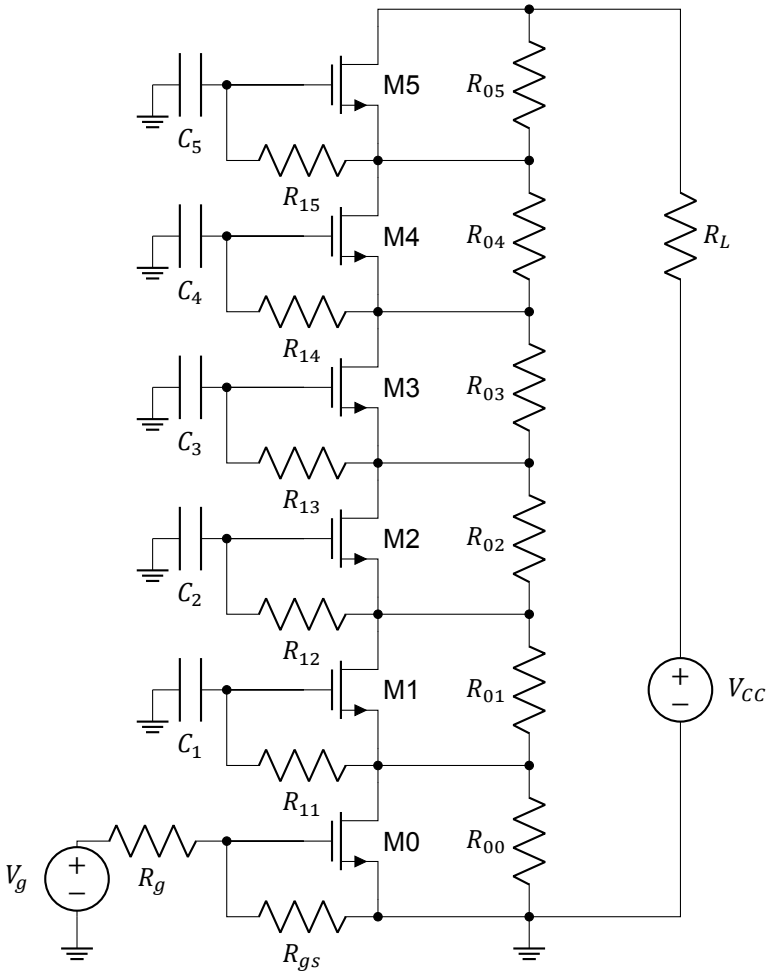


Figure 3.2: Basic capacitive coupling schematic

The time that the switch can stay on is limited by the discharging of the C_{iss} capacitance in parallel with the coupling capacitance. This coupling capacitance C_i will be discharged through R_{1i}. The time that the switch can stay on can be calculated using Equation 3.5. The time constant τ of the RC system can be used to calculate the voltage over time. This can then be used to calculate the maximum on-time. In reality, this time will be shorter, since the MOSFET will start to conduct before the threshold voltage is reached.

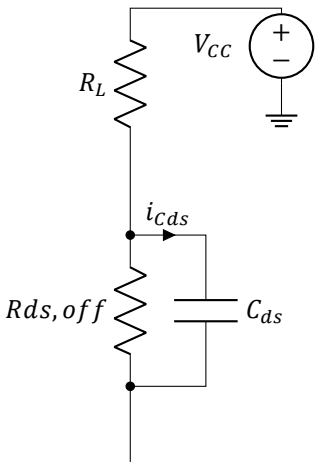


Figure 3.4: Charging and discharging of C_{ds}

$$\tau = R_{11}(C_5 + C_{gs} + C_{gd}) \tag{3.2}$$

$$V = V_{gs,max}(1 - e^{\frac{-t}{\tau}}) \tag{3.3}$$

$$V_{th} = V_{gs,max}(1 - e^{\frac{-t}{\tau}}) \tag{3.4}$$

$$t_{on,max} = -\tau ln(\frac{V_{gs} - V_{th}}{V_{gs}}) \tag{3.5}$$

3.5. Coupling capacitor design

The coupling capacitors need to be sized correctly for the system to function. The coupling capacitor stores and releases the gate charge that is needed to turn the MOSFETs on. The capacitance value needed for these coupling capacitors can be calculated using Equation 3.6 [15]. Q_g is the gate charge, V_C is the change in voltage over the capacitor. The gate charge is then decomposed into the charge in the C_{GS} capacitor and the charge in the C_{GD} capacitor. The coupling capacitance of the i-th MOSFET in series with the directly driven MOSFET can then be calculated using Equation 3.8. This means that the capacitance goes down with more MOSFETs in series. This capacitance can become too low in comparison with the parasitic capacitances to ground that are present in any construction of this circuit [6]. At that point, it is not feasible anymore to add more MOSFETs in series.

$$C = \frac{Q_g}{V_C} = \frac{V_{GS}C_{GS} + V_{DS,off}C_{GD}}{V_C} \tag{3.6}$$

$$V_{Ci} = V_{DS} \cdot i \tag{3.7}$$

$$C_i = \frac{C_1}{i} \tag{3.8}$$

3.6. Snubber capacitor design

The rise of the drain-to-source voltage can be delayed by placing a capacitor in parallel with the MOSFETs. In this way, the dynamic voltage imbalance can be corrected. By adding a zener diode between the source and gate, a higher value of coupling capacitance can be used while limiting the gate-to-source voltage to a maximum value of the zener voltage of the diode. By combining these techniques, it is possible to create a switch that is well balanced for a wider range of voltages [17]. The coupling capacitance can be increased to accommodate for lower voltages, while the higher voltages will not charge the capacitors too much since they are limited to the zener voltage. This also means that the switch can stay on for longer.

These snubbers can be realized by equalizing the output capacitance of the MOSFETs, to make

them charge at the same rate. This is done by adding parallel capacitances proportional to the coupling capacitance. This means that $C_{0i} = i \cdot C_1$. In this way, all the C_{oss} capacitance values are equal.

A schematic of the total circuit can be seen in Figure 3.5.

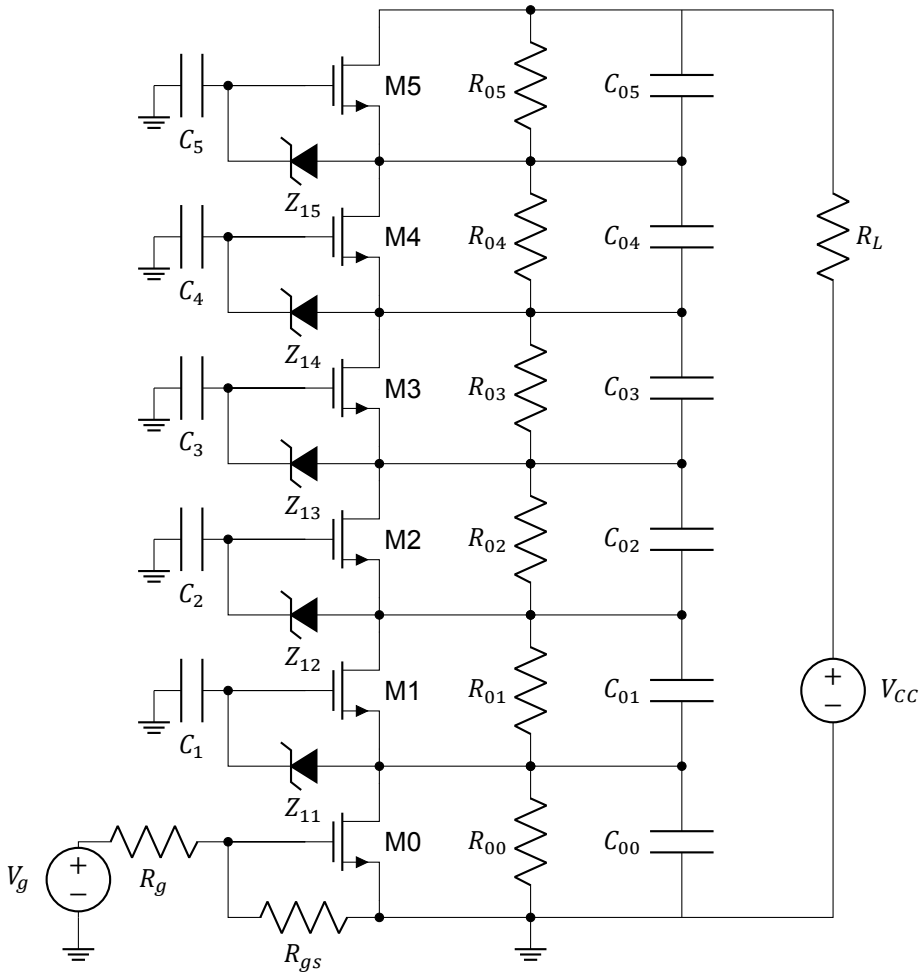


Figure 3.5: Capacitive coupling with zener diodes and snubber capacitors

4

MMC submodule

Power converters exist in several different types. There are two-level power converters, like the half-bridge converters. There are three-level power converters like the full-bridge converters. There are also multilevel converters. These converters are differentiated by the amount of discrete voltage levels that the switches can switch between. Multilevel converters have the advantage that the stress on the semiconductor switches is divided over the multiple levels. In this way, a higher voltage converter can be made using several switches. Since only a division of the high-voltage is switched, the switches do not need to block all the voltage.

There are multiple ways to implement a multilevel converter [21]. Some often used converters are the cascaded H-bridge (CHB) topology, and the multilevel modular converter (MMC). Each level in these topologies consists of switches and a DC source. In the case of the CHB, this DC source is an isolated DC supply and in the case of the MMC this is a capacitor. These DC sources are connected to the output, depending on the voltage that is needed on the output. In this way, an output signal with multiple voltage levels can be generated, depending on the number of modules.

For a modular multilevel converter (MMC), submodules are needed. These submodules consist of a half-bridge or a full-bridge configuration of switches, along with the DC source. These submodules can be seen in Figure 4.1. The half-bridge only needs two switches, while the full-bridge needs four switches. The full-bridge has the advantage of being able to invert the output voltage. The half bridge has the advantage of needing less switches. Using less switches means that the cost and power consumption will be lower.

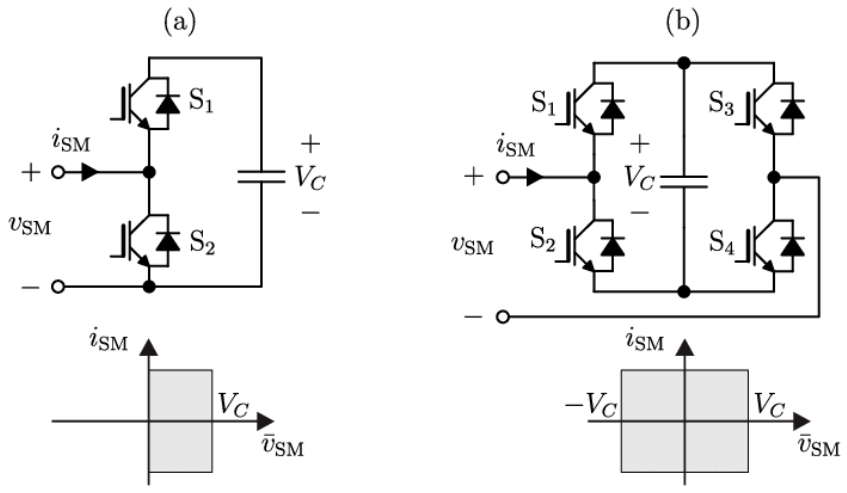


Figure 4.1: MMC submodule in half-bridge (a) and full-bridge (b) configuration [22]

4.1. Multilevel modular converter

A multilevel modular converter (MMC) is a type of AC to DC converter (or DC to AC). It works on the principle of inserting charged capacitors into its arm. By inserting several capacitors, the voltage can go to a very high level. The advantage of this is that the switches only have to be rated for the capacitor voltage, and not the full output voltage. In this way, a high-voltage converter can be created with lower voltage switches. The downside of this is that there are more components needed than with a single switch. Gate driving circuits, as well as monitoring components are needed to control and monitor the submodules. That is why less submodules can be beneficial to reduce the total amount of components. Using a higher voltage switch in a submodule can thus contribute to less components being used and lower the losses for the full system.

4.2. Half-bridge

The half-bridge submodule has three states:

1. Inserted
2. Bypassed
3. Blocked

In the inserted state, the top switch is on so the capacitor is inserted in the circuit. In the bypassed state, the bottom switch is on so the capacitor is not in the circuit. In the blocked state, both switches are off so no current can flow through the submodule. By using these states, the MMC can control the voltage across each arm.

During a DC fault, either the capacitor is inserted or the lower switch is short circuited (depending on the arm current) because of the body diodes. This is a downside of the half-bridge modules. A full-bridge module is more robust to DC faults.

4.3. Full-bridge

The full bridge has the same states as the half bridge. It can also connect the capacitor in the reverse direction, resulting in a reduction of the output voltage. It thus has the following states:

1. Inserted
2. Bypassed
3. Blocked
4. Inverted inserted

In case of a DC fault, the capacitor is always inversely inserted. This is because the body diodes form a full-bridge rectifier. In this way, it will lower the output voltage and block the DC fault from affecting the AC side [23].

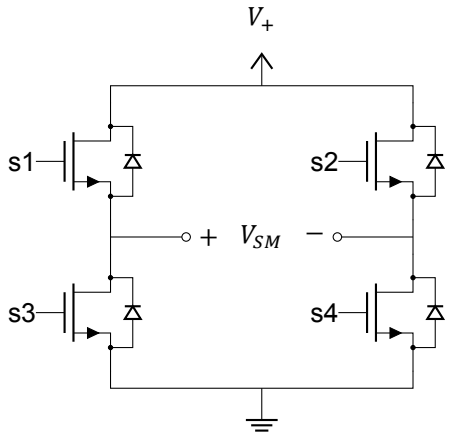


Figure 4.2: Full bridge circuit

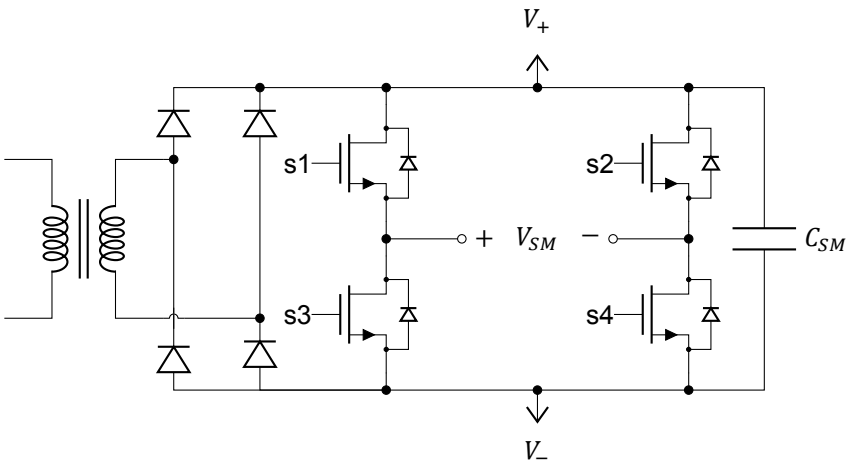


Figure 4.3: Full bridge CHB mode circuit

4.4. Dead time

Two switches in the same leg of a circuit cannot conduct at the same time. If they would, a short circuit is created (shoot-through). The MOSFETs need a finite time to turn off. This is why there should be a dead time (blanking time) between switching one switch off and the other switch on. This dead time should be longer than the fall time of the switch. This means, that there is a period when none of the switches are conducting. During this dead time, the submodule will be in the blocked state.

4.5. Auxillary power supply

An auxillary power supply is needed to power the gate drivers for the submodule. These gate drivers should be isolated and thus require an isolated power supply. An auxillary power supply can also be used to provide the initial charge for the capacitors in the submodule. The capacitor voltages can also be balanced in this way. The auxillary power supply should thus be able to create the full submodule voltage, as well as the lower gate driving voltage for the lower- and upper switches.

For the CHB mode, a lower turn ratio secondary winding can be added to facilitate this auxillary power. The AC voltage from this winding should then be rectified and regulated to power the submodule. For MMC operation, this auxillary power should come from an isolated power supply. This power supply could be powered from the submodule capacitor, or it could come from a primary source, similarly to how the CHB mode is powered.

5

Simulation

A simulation was performed in LTspice to confirm the working of the circuit. The MOSFET spice model was downloaded from the website of the manufacturer [24]. The gate driver was implemented using a voltage source with a pulsed output. Paramatric values were given to the coupling capacitors, gate resistors, balancing resistors, and gate-to-source resistors. This was then simulated for a few cycles to compare the voltage balance of the drain-to-source voltages.

5.1. Series MOSFETs

The voltage balance is dependent on the coupling capacitors, the load current, and the gate voltage of the lower MOSFET. A lower gate resistance on the lower MOSFET makes the lowest MOSFET's voltage rise faster during turn-off. This is because a lower resistance means that the gate capacitance can charge faster because of the higher current. If the gate capacitance charges faster, that means that the gate voltage will charge faster and thus it will turn on the MOSFET faster. This also means that the drain-to-source voltage will rise faster, which will impact the voltage balance.

The results of the simulation can be seen in Figure 5.2 and Figure 5.3. The gate-to-source voltage in Figure 5.2 shows that the MOSFETs get turned on at approximately the same time, with only the lowest MOSFET being driven. There is also some overshoot in the signals. The signal also has a slight slope down while the MOSFET is on, caused by the coupling capacitors discharging through the source resistors. In Figure 5.3 it can be seen that the voltage is balanced in the steady state. During the dynamic transitions, there is some imbalance.

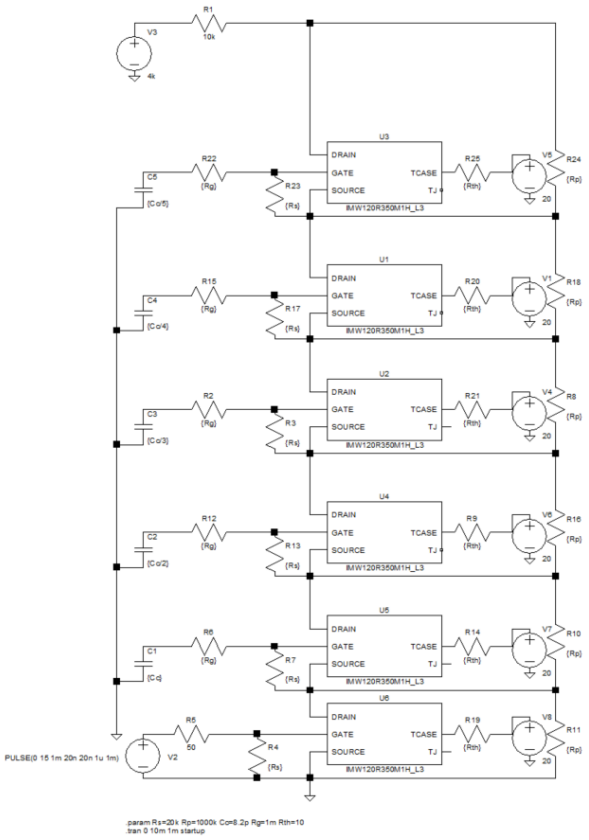


Figure 5.1: LTspice simulation schematic

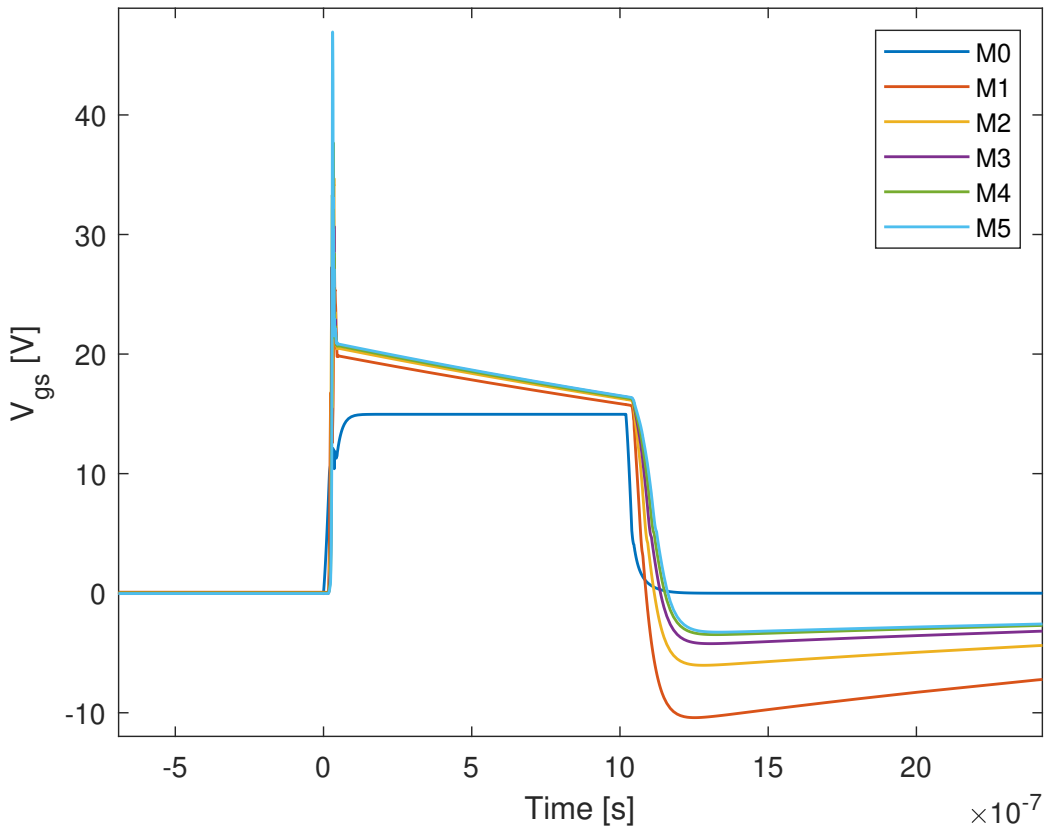


Figure 5.2: Gate-to-source voltages of the MOSFETs, in order of the lowest to the highest MOSFET

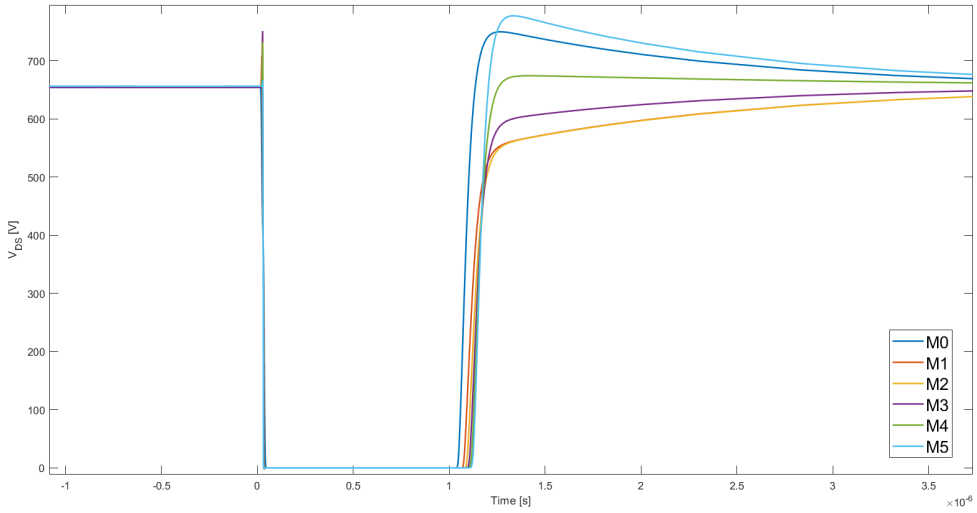


Figure 5.3: Drain-to-source voltages of the MOSFETs, in order of the lowest to the highest MOSFET

5.2. Custom snubbers

With snubber capacitors and zener diodes, the balance and stable voltage range can be improved. With the zener diodes, and custom snubbers, as described in Chapter 3, the following results were obtained. A coupling capacitance of 1 nF was used, along with 15 V zener diodes. In Figure 5.5, it can be seen that the balance is better but the overal switch is slower. This is caused by the fact that the drain-to-source capacitance is effectively increased, which charges slower. With the gate-to-source resistors removed, the gate-to-source voltage can float up a bit. This causes a slight voltage imbalance during the steady state. This can be fixed by reintroducing the gate-to-source resistors, but this will again lower the maximum on-time of the switch. This is caused by the capacitors being able to discharge through this resistor.

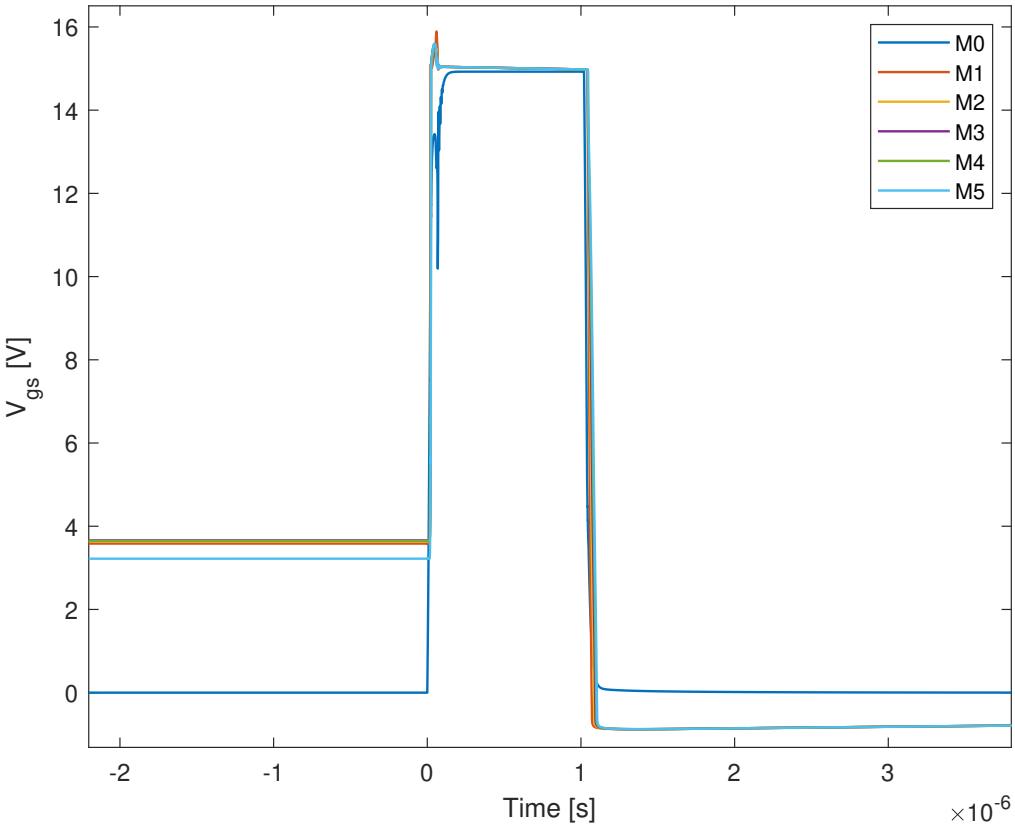


Figure 5.4: Gate-to-source voltages of the MOSFETs with zener diodes and snubbers, in order of the lowest to the highest MOSFET

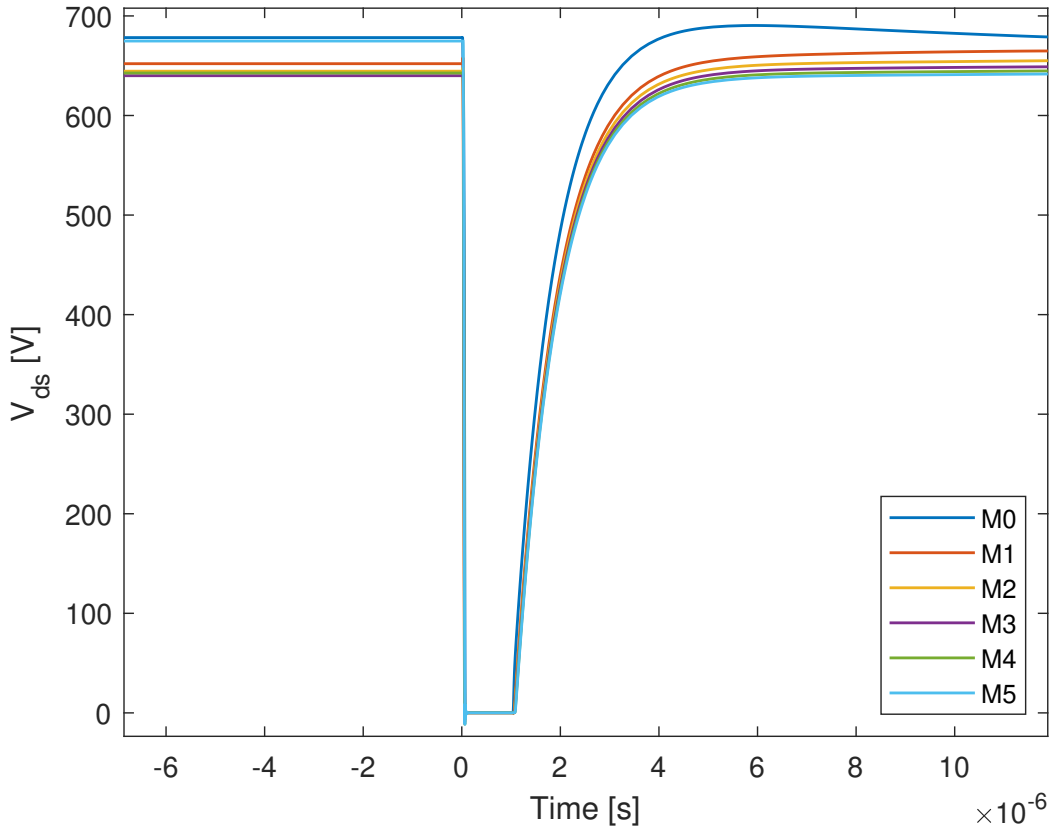


Figure 5.5: Drain-to-source voltages of the MOSFETs with zener diodes and snubbers, in order of the lowest to the highest MOSFET

6

Prototypes

Several prototypes were made to test and develop a high-voltage submodule. Firstly, a prototype was made to test two MOSFETs in series. Secondly, a prototype was made to test six MOSFETs in series. Thirdly, a prototype was made to test a high-voltage full-bridge of 4 kV. And lastly, a prototype high-voltage full-bridge submodule was made that can be used for MMC or CHB operation.

6.1. Two MOSFET switch

For the prototype, the selected capacitive coupling topology was implemented. The MOSFETs were selected based on the maximum blocking voltage, and their input- and output capacitance. The capacitance is important to switch the MOSFETs as fast as possible. The input capacitance determines the turn-off delay, and the output capacitance determines the turn-off fall time. A bigger delay or a mismatch in fall time will result in imbalance between the MOSFETs. The IMW120R350M1H from Infineon was selected [25]. This MOSFET has a breakdown voltage of 1200 V, and low parasitic capacitances compared to similar MOSFETs. This will mean that the operation of the switch will be faster, as the switching times depend on the parasitic capacitances. Since the parasitic capacitance is low, the coupling capacitance can also be kept low, aiding the speed of the switch. This is apparent from Equation 3.6. Two MOSFETs were connected in series on a proto board, along with a UCC37322P gate driver and a coupling capacitor. This prototype can be seen in Figure 6.1. The values of the parasitic capacitances were taken from the datasheet of the IMW120RM1H [25]. Using Equation 6.5, the coupling capacitance was calculated for a 100 V switch. The voltage was kept low to verify the working of the series connected switch without damaging the components. A value of 200 pF was chosen since it was the closest available value.

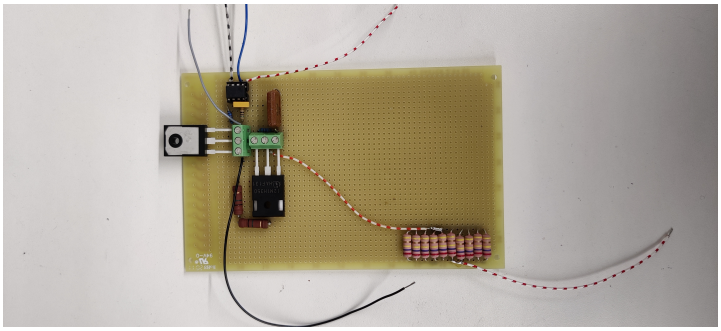


Figure 6.1: Two MOSFET switch prototype

$$C = \frac{Q_g}{\Delta V} = \frac{V_{GS}C_{GS} + V_{DS,off}C_{GD}}{V_C} \tag{6.1}$$

$$C_{GD} = C_{rss} = 1pF \tag{6.2}$$

$$C_{GS} = C_{iss} - C_{GD} = 181pF \tag{6.3}$$

$$C_{DS} = C_{oss} - C_{GD} = 9pF \tag{6.4}$$

$$C_1 = \frac{15 \cdot 181 \cdot 10^{-12} + 100 \cdot 1 \cdot 10^{-12}}{100} = 227pF \tag{6.5}$$

(6.6)

6.2. Six MOSFET switch

The series connected switch using six MOSFETs was designed in a similar way as the two MOSFET switch. The sockets for the MOSFETs were arranged in a way that the drain of one MOSFET was closest to the source of another MOSFET. In this way, they could be connected in series in a compact way. The coupling capacitors were connected to ground, minimizing the total loop inductance. The MOSFETs, coupling capacitors, balancing resistors, gate discharge resistors, and the gate driving circuit were soldered onto a protoboard. The prototype can be seen in Figure 6.2. The chosen capacitors were 8.2 pF 1 kV capacitors. These were selected based on the gate charge of the gate charge of the MOSFETs [25] and Equation 6.7. The closest available capacitance value for a high enough voltage was chosen, which was the 561R10TCCV82 8.2 pF 1 kV capacitor. These capacitors were put in series for C_2 to C_5. i capacitors were put in series for capacitor C_i. In this way, the desired coupling capacitance was reached for the MOSFETs. It should be noted that parasitic capacitances from the board and assembly could influence the coupling capacitance.

$$C_1 = \frac{Q_g}{\Delta V} = \frac{5.2 \cdot 10^{-12}}{667} = 7.94pF \tag{6.7}$$

$$C_i = \frac{C_1}{i} \tag{6.8}$$

$$C_5 = \frac{7.94pF}{5} = 1.6pF \tag{6.9}$$

6.3. High-voltage full-bridge

A high-voltage full-bridge circuit was designed to be used in the submodule. The designed high-voltage full-bridge uses IXTH02N450HV MOSFETs. These MOSFETs can block up to 4.5 kV, but their current

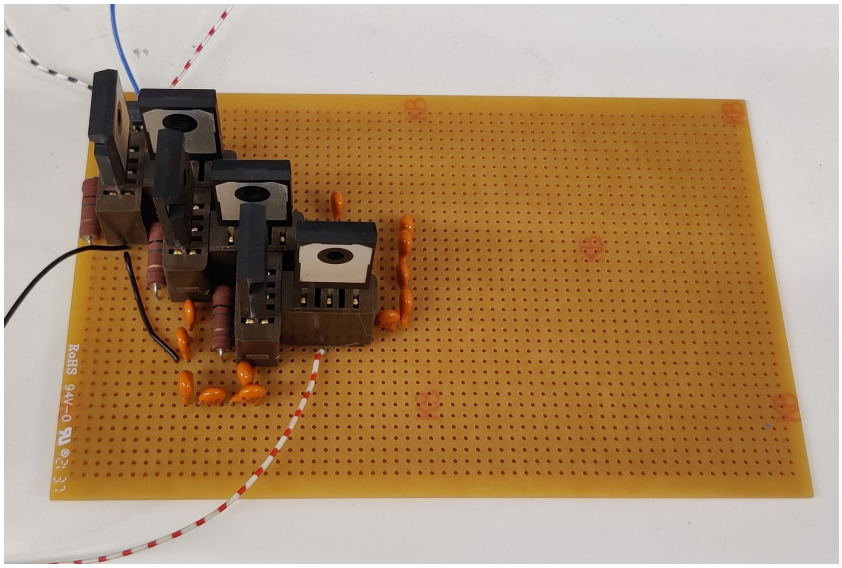


Figure 6.2: Series MOSFET switch using six individual MOSFETs

is limited to 200 mA. Their high on-resistance of 625 Ω makes this limit even harder to reach due to thermal constraints. The IXTH1N450HV is preferred since it has a lower on-resistance of 80 Ω but it was not available during this project. The resistance of these MOSFETs is very high, which should be taken into account for the thermal constraints and influence on the load of the full-bridge. Preliminary, the OPI1280-066 were used. These were used because they can block up to 15 kV and they can be powered by up to 30 V. This means that only a single power supply can be used for the gate driver and the optocoupler. During testing, it was found that these optocouplers were too slow for this application, since their rise time was several microseconds. This would distort the input signal given to the full-bridge. Since the rise and fall time were not the same, this would cause the dead time to have to be higher than several microseconds, which is not desirable. The gate drivers that were used are the IXDD630MCI. These gate drivers can be powered by up to 30 V and they can handle currents up to 30 A. These gate drivers and optocouplers are powered by a MGJ1D241905MPC-R7 isolated converter. These converters convert a 24 V input into a +19/-5 V output. This converter was chosen because it can block up to 5.7 kV and its output voltage of 19 V was higher than the required threshold voltage of 6 V to turn the MOSFET on. The -5 V can turn the MOSFET off since it is lower than the threshold voltage. These driving voltages are also within the limits of the MOSFETs gate-to-source voltage. A schematic overview of the signal path of this full-bridge can be seen in Figure 6.3. A similar structure is used to drive each of the MOSFETs in the full-bridge.

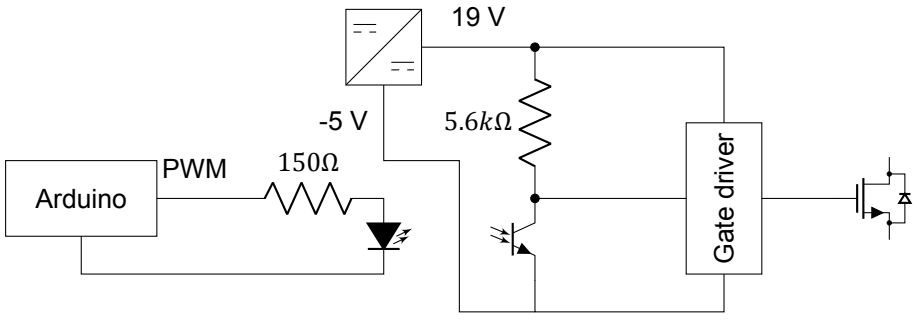


Figure 6.3: Signal path

6.4. Submodule

A submodule was designed by creating a PCB. The high-voltage full-bridge was incorporated along with an input controller, power delivery, and sensors to measure the voltage and current. After the first

PCB was designed and assembled, minor improvements were made to create a second version.

6.4.1. Gate driving

In the submodule, not all MOSFETs have their source connected to ground. As such, their gate voltage needs to be referred to the source voltage, instead of to the ground to turn on. For this, the gate driver needs to be isolated. If it is not isolated, it needs to be able to generate the threshold voltage above the source voltage of the MOSFET. Since the source voltage can be several kilovolts, this is not practical. An isolated power supply and an isolated input voltage can be used. This way, the gate driver can be referred to the source voltage of the corresponding MOSFET.

Bootstrapping can also be used, but it has a limited on-time. Bootstrapping works by connecting a capacitor between the source of the MOSFET and the positive voltage of the gate driver. By connecting a power supply to this capacitor with a diode, the capacitor can be charged when the lower MOSFET is turned on. The diode should be able to block the voltage over the lower MOSFET when it is turned off. The input voltage of the gate driver should still be isolated using an optocoupler or opto-isolator, or fiber optic cables.

6.4.2. Power delivery

This isolated power supply and input voltage need to be able to block the several kilovolts of the system. For this, an optocoupler and an isolated DC/DC converter are used. It was also opted to isolate the lower MOSFETs and not connect the grounds of the full-bridge and the control circuits together. This was done to isolate the noise that might be generated by the high dv/dt on the high voltage side. This rapidly changing voltage can introduce a voltage noise on the ground connection because of parasitic inductances. For the isolated DC/DC converters, Recom RHV2-0512D/R20 were used. These featured a high isolation voltage of 20 kV but the datasheet did not mention a working voltage. Since other converters either featured lower isolation voltages or were not in stock, it was opted to use the Recom RHV2-0512D/R20. This converter has an input voltage of 5 V and an output voltage of ±12 V. Only the +12 V was used for the gate drivers. For the signal isolation, an optocoupler was used. fiber optic transmitters and receivers are more expensive and less practical to use on a PCB since the cable needs to be a certain length. The chosen optocoupler was the OPI1268S. This optocoupler also featured an isolation voltage of 20 kV DC. The optocoupler uses a convenient through-hole package.

6.4.3. Inputs and outputs

The H-bridge is controlled using two separate inputs and an enable signal. One signal can control one half bridge, using an inverted version of itself. The non-inverted signal is connected to the top switch, while the inverted version is connected to the bottom transistor. The enable signal makes sure that all the switches can be switched off at any given moment. These signals can be connected to the board using copper cables or using fiber optic cables.

The power is delivered using a high frequency transformer. This is then rectified to create the DC bus voltage. The submodule works with a DC bus voltage of 0 kV to 4.5 kV. A large capacitor can also be connected across the DC bus to be used in conjunction with the transformer, or as a standalone unit like in an MMC.

A lower voltage winding of the high-frequency transformer is used to power the low-voltage circuitry. This is then rectified using a full-bridge diode rectifier using an RTT410 full-bridge. This lower voltage DC is then fed into the TI LMR38020F buck converter, which converts it into 5 V DC.

The output current of the submodule is measured using a hall-effect current transducer, namely the LEM HO-6P. The LEM HO-6P can measure a current from -20 A to 20 A. The output will be a voltage between 0.5 V and 4.5 V. This means that there will be 0.1 V at the output for every ampere at the input, with 0 A corresponding to 2.5 V. This signal is then converted into a digital signal using an ADC and made available for read-out using a copper cable or using a fiber optic cable. The output of the current transducer is also fed into a comparator, where it is compared to a threshold of 2.59 V, corresponding to a current of 0.9 A. When the current becomes higher than the threshold and the comparator triggers, the PLD can adjust the PWM signals of the switches to correct the current.

The DC bus voltage is also measured. The lower voltage DC (7.5 V to 67.5 V) is stepped down even further using a resistive divider consisting of a 1 kΩ resistor and a 15 kΩ resistor. This will make it into a range of 0.5 V to 4.2 V. This voltage is then digitized and made available for read-out using a

copper cable or a fiber optic cable. A comparator is also used to compare it to a threshold of 4.2 V. This is used to detect an over voltage and have the PLD alter the PWM signals to protect the switches.

6.4.4. Programmable logic input controller

A programmable logic device (PLD) is used to regulate the incoming signals to the PCB. There are three input signals. The first signal (IN1) controls if the left leg of the H-bridge is pulled high or low. The second signal (IN2) controls if the right leg of the H-bridge is pulled high or low. The third signal is an enable signal (ENA) and it turns the H-bridge off when it is pulled low. In this way, the output of the H-bridge can be positive, negative, or floating. The truth table for this operation can be seen in Table 6.1. The x symbol indicates a don't care, meaning that it does not matter what the input is, the output will always be floating when the enable signal is high.

IN1	IN2	ENA	**Output**
1	0	1	**+VDC**
0	1	1	**-VDC**
1	1	1	**0V (high)**
0	0	1	**0V (low)**
x	x	0	**floating**

Table 6.1: Truth table for the input logic

Dead time

The dead time between gate signals is implemented on the PCB. The incoming signals (IN1 and IN2) are delayed using an RC filter, where the resistance is controlled by a potentiometer. The potentiometer is a 2 gang device, meaning that there are two almost identical resistances available, so the dead time of both legs of the H-bridge can be the same. The potentiometer has a maximum resistance of 1 kΩ, meaning that with a 470 pF capacitor, the dead time can be adjusted from 0 ns to approximately 1 μs. By comparing this delayed signal with the non-delayed signal, a dead time can be implemented. The comparison is done inside the PLD.

The upper switch is driven high when the enable is high, the input is high, and the delayed input is high. The lower switch is driven high when the enable is high, and the input or the delayed input is low. This makes sure that the upper switch and the lower switch are never on at the same time, and that the switches can be enabled and disabled using an enable signal. This is done for both legs, using the two input signals.

Programming

The chosen PLD (ATF16V8C) can be programmed in the WinCupl software. The logic from Table 6.1 and the dead time were implemented, along with a shut-off function in case of a fault. If a fault occurs, the output will be set to ”floating”. An indicator LED output is also present to show that the chip is enabled and operational, as well as an LED to indicate that a fault is detected. A schematic of this circuit can be seen in Figure 6.4. The programming file can be found in Appendix B.2. This programming file is then converted into a JEDEC output by the WinCupl program. This file is then programmed into the chip using a TL866 programmer. This programmer is connected to a computer using a USB cable. Xgpro v10.80 software is used to interface with the programmer and put the JEDEC file onto the actual chip.

The programming file was also simulated in WinSim, as can be seen in Figure 6.5. It can be seen that the output is as programmed. It can also be seen that there is always a dead time between the high-switch and low-switch turning on or off. If the input is switching with the same frequency as the dead time, the output will be floating.

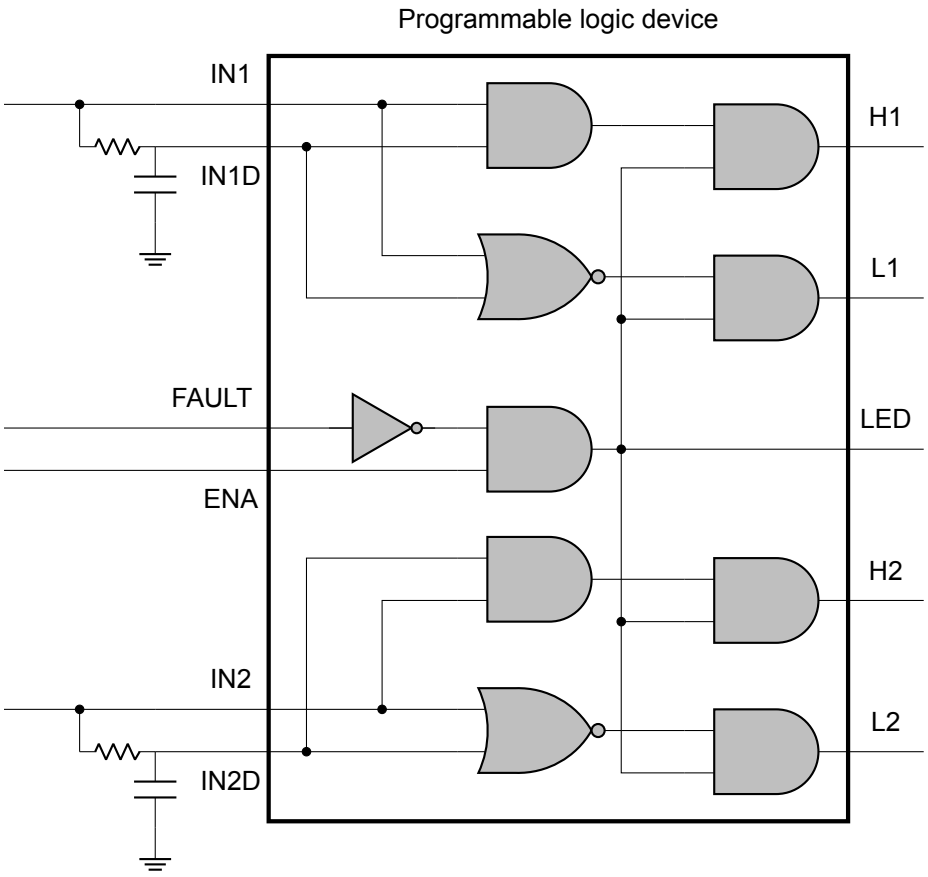


Figure 6.4: Programmed logic circuit

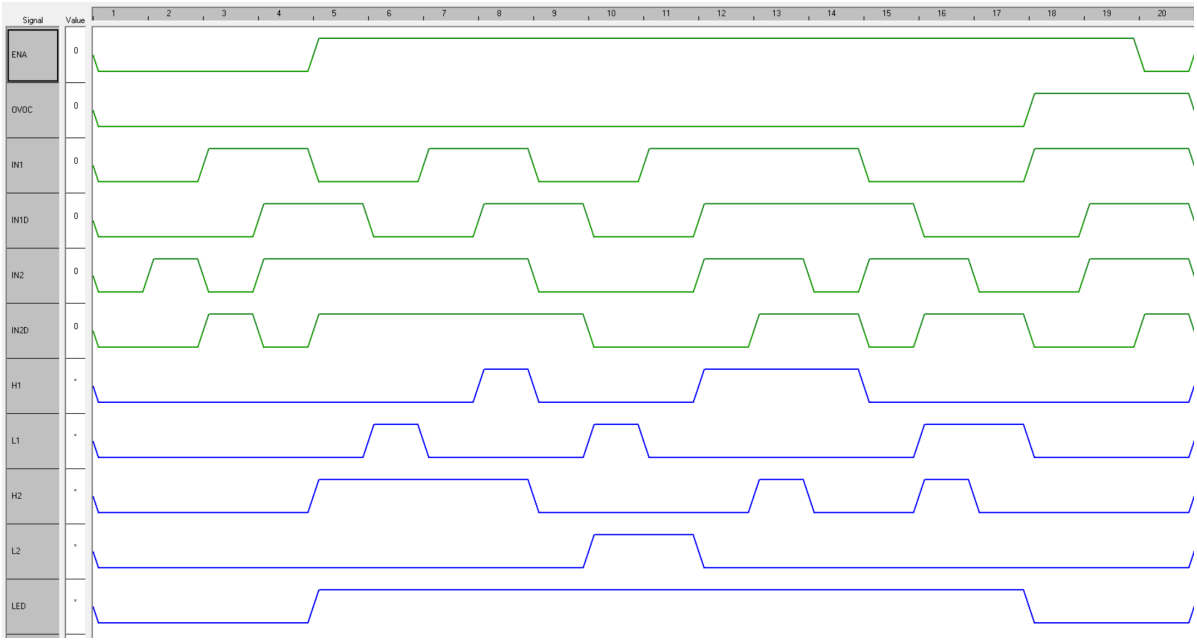


Figure 6.5: WinSim simulation of WinCupl file. Green signals are input, blue signals are resulting output

6.4.5. Current- and voltage measurement

The current and the voltage of the submodule is measured. This is done using transducers on the high-voltage side.

Voltage measurement
The voltage of the DC bus is measured using the LEM DVC-1000-P. This transducer was chosen because it can measure high DC voltages in a reasonable size. Other transducers can be much bigger and more expensive. This transducer can measure steady state voltages of 1000 V, with peaks of 1500 V. The DC bus can go up to a maximum of 4.5 kV, which is higher than the maximum range of the transducer. A resistive voltage divider is used to divide the DC bus voltage. The LEM DVC-1000-P has a primary resistance of 12.6 MΩ. Using a series resitance of 40 MΩ, the maximum voltage will be $4.5kV \cdot \frac{12.6M\Omega}{52.6M\Omega} = 1.08$ kV over the transducer. The output of the transducer is isolated and will produce a voltage between 0.5 V and 4.5 V. The output is centered around a reference voltage of 2.5 V, corresponding to 0 V on the input. An output voltage of 0.5 V corresponds to -1500 V on the input, and 4.5 V corresponds to 1500 V on the input. Since only positive voltages are used on the DC bus, only the 2.5 V to 4.5 V range of the output is utilized. A difference amplifier is used to subtract 2.5 V from this output and amplify it by 2.5x. In this way, a voltage of 0 V to 5 V will be created. This difference amplifier can be seen in Figure 6.6. Here, V_{ref} is the transducer reference voltage, and V_{TD} is the output voltage of the transducer. In equation 6.13, it can be seen that the output voltage is the difference between the inputs multiplied by a factor determined by the resistors. The resistor values were chosen to be $R_1 = R_2 = 4k\Omega$ and $R_3 = R_4 = 10k\Omega$. In this way, the desired output will be created. The load on the transducer output is also kept low because the resistance is several kiloohms.

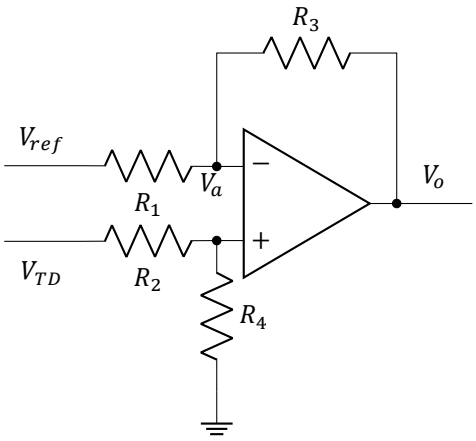


Figure 6.6: Difference amplifier

$$\frac{V_{ref} - V_a}{R_1} = \frac{V_a - V_o}{R_3} \tag{6.10}$$

$$\frac{V_{TD} - V_a}{R2} = \frac{V_a}{R_4} \tag{6.11}$$

$$V_o = -V_{ref}\frac{R_3}{R_1} + V_2\frac{R_4}{R_2 + R_4} + V_2\frac{R_3}{R_1}\frac{R_4}{R_2 + R_4} \tag{6.12}$$

$$\text{If } R_1 = R_2 \text{ and } R_3 = R_4 \Rightarrow V_o = \frac{R_3}{R_1}(V_{TD} - V_{ref}) \tag{6.13}$$

Current measurement
A current sensor needs sufficient isolation. Several options for current sensors were considered. The first option was a shunt resistor over which the voltage could be measured. This can be a cheap option, since the shunt resistors do not cost a lot of money. If this resistor is not connected to the same ground as the measuring circuit, a differential amplifier would be needed. In the case of the submodule, the current through the switches needs to be measured to prevent an overcurrent fault. The shunt resistor cannot be connected to the ground in this case because the current does not necessarily flow through the ground. In particular, if the submodule is bypassed, the current only flows through the switches and not via the ground. The current should thus be measured on the connection of the submodule ($+V_{sm}$

or $-V_{sm}$ connection if Figure 4.2). This would mean that the shunt resistor will be floating and proper isolation would be needed for the differential amplifier. Amplifiers that are capable of several kilovolts isolation are not readily available. It is possible to have the whole measurement circuit floating around the same potential as the output. This would however need a separate power supply and there would be extra electrical noise from the switching of the module. The second option was using a current probe that is often used with an oscilloscope. These are very expensive and thus not practical for the project.

The third option was using an isolated current transducer. These are current sensors that make use of the Hall effect to measure the current wirelessly. A Hall voltage will be induced in a conductor in a magnetic field. A magnetic field is made by a current flowing through a conductor. A higher current on the primary side of the current transducer will thus lead to a higher Hall voltage on the secondary side. In this way, the current can be measured while maintaining electrical isolation. It was opted to go for an isolated current transducer. These were not available with sufficient isolation however. There were several sensors that could be used using an external wire. This wire can have electrical isolation, which not necessarily impedes the magnetic fields from the current. This isolated wire can thus provide the necessary isolation for the sensor. For the first version of the prototype, the LEM HO 6-P was used. This is a fast sensor (3.5 μs 0-90% response time). Because it has a measurement range of -20 A to 20 A, it was opted to amplify the signal for a range of -1 A to 1 A. This however meant that the signal was very noisy (several 100 mA inaccuracy). This meant that the sensor could not be used to measure the low currents that would be flowing through the switches. For the second prototype, it was thus opted to go for the LEM CTSR 0.6-P. This sensor has a range of -0.85 A to 0.85 A but the response time is slower (30 μs 0-90% response time).

Sensor readout

The outputs of the current transducer and the voltage transducer also need to be sent to an external controller. To do this, the signal needs to be sent over an isolated line because of the high voltages of the submodules. Fiber optics are used for that. Fiber optics are normally used to sent digital signals, while the outputs of the transducers are analog signals. There are several options to transmit this signal to a central controller.

The first option is to use analog fiber optics. For example, a Broadcom HFBR2406 analog fiber optic receiver could be used. This receiver has a photodiode that converts the light from the fiber optic link into a current. This current is then converted into a voltage using an integrated transimpedance amplifier. By driving a fiber optic transmitter according to the voltage of the sensors, the signal can be isolated using the fiber optic link. The threshold voltage of the transmitting LED needs to be taken into account in this case. It is possible to offset the voltage of the sensor to accomplish this. The signal can be transmitted using a resistor in series with the LED to convert the voltage into a voltage. It might be more precise to utilise a transconductance amplifier to convert the voltage into a current, since an LED is a non-linear device. It should also be noted that there is no reference in the datasheet that the Broadcom HFBR2406 can be used in this way. The application notes mention that this receiver is used in combination with digital transmitters.

The second option is to use an analog to digital converter (ADC). These ADCs come in various forms. They often make use of digital protocols like I2C, SPI, or UART. These protocols use one or more data lines and a clock line to synchronise signals. In this case, multiple fiber optic links would be needed to transfer the signal. This increases the price of the prototype. One solution to this problem would be to only use the data line and filter it out on the receiving end to get the average value. This would increase the delay and it would need another ADC to make the signal available to a central controller. There are also ADCs available that use different ways of encoding the signal. For example, there is the Manchester encoding. This will encode the data signal and clock signal together, so the controller can synchronise itself using one signal. This would need a very fast controller that can decode these signals.

Another option is to use a voltage controlled oscillator (VCO). This device converts a voltage into a frequency. By reading the frequency of the signal, the input voltage can be determined by a controller. This signal can be sent over one fiber optic link since there is no clock signal needed. A suitable frequency range needs to be selected to minimise delay time and accuracy. This will depend on the speed that the controller can read out the signal.

Taking all these options into account, the voltage controlled oscillator was chosen to transfer the voltage- and currend readouts to a central controller. This way, only one fiber optic link is needed

and the load on the central controller can be minimised. The LTC6990 was chosen as the VCO. The frequency range can be changed by changing the resistors for the chip's circuit.

The sensors have a certain amount of electrical noise propagating to their output. This noise will affect the reading of the current and voltage. This noise can be filtered out using filters. This will affect the bandwidth and make the sensor slower.

6.4.6. Thermals

MOSFETs heat up due to the power that is lost in them. Power is lost because of resistive losses during conduction (conduction losses) and a overlapping period of current and voltage during the switching of the MOSFET (switching losses). The main concern with the IXTT02N450HV are the conduction losses because of its high on-resistance of 625 Ω. When it is conducting its maximum current of 0.2 A, 25 W will be lost in the MOSFET. This power loss is dissipated as heat. This heat will be conducted from the junction of the MOSFET to the air. For this, the heat needs to go through the case of the MOSFET, a thermal interface, and a heat sink. These components all have a different amount of thermal resistance. The junction-to-case thermal resistance is given in the datasheet [26] at 0.24 K/W. The thermal interface also has a relatively low thermal resistance (around 0.2 K/W) but the heat sink to ambient can have a thermal resistance of several K/W. This means that if the MOSFET should stay below 125 °C above ambient, its maximum total thermal resistance should be limited to $\frac{125}{25} = 5$ K/W. This means that the heatsink should have a lower thermal resistance than 4.5 K/W to properly cool the MOSFET with a current of 0.2 A.

6.4.7. Gate resistance

An extra resistance can be added between the gate driver output and the gate of the MOSFET to prevent unwanted oscillations. The gate resistance should also be high enough so that the gate driver stays within its current limits. For the IXDD630 there is a current limit of 30 A but the power supply of the gate driver is only capable of delivering 167 mA. This would mean that a gate resistance of at least $\frac{12V}{0.167A} = 72\Omega$ would be needed. However, this power is only provided for a very short time to provide the necessary gate charge. This means that capacitors can be used to provide this energy. This capacitors can be connected to the power supply of the gate driver to provide this energy. These capacitors need to store the charge in the gate-to-source capacitance and in the gate-to-drain capacitance.

6.4.8. Power delivery

The power is delivered from the high voltage side of the board. In the CHB mode, there is a lower voltage winding to provide the low-voltage power. This is rectified, regulated to 5 V and transferred to the low-voltage side using an isolated DC/DC converter. Here, the power can be used for the low-voltage components that handle the input from a controller. The power is also transferred to the gate drivers for each switch. These also have to be isolated from each other, since the source voltages (and thus the gate-to-source voltages) differ for each switch. The 12 V for the gate drivers is also stepped down using a Low Drop-Out regulator (LDO) to 5 V. This 5 V is used to power the optocouplers that transfer the signal. A representation of the full power regulating path can be seen in Figure 6.7.

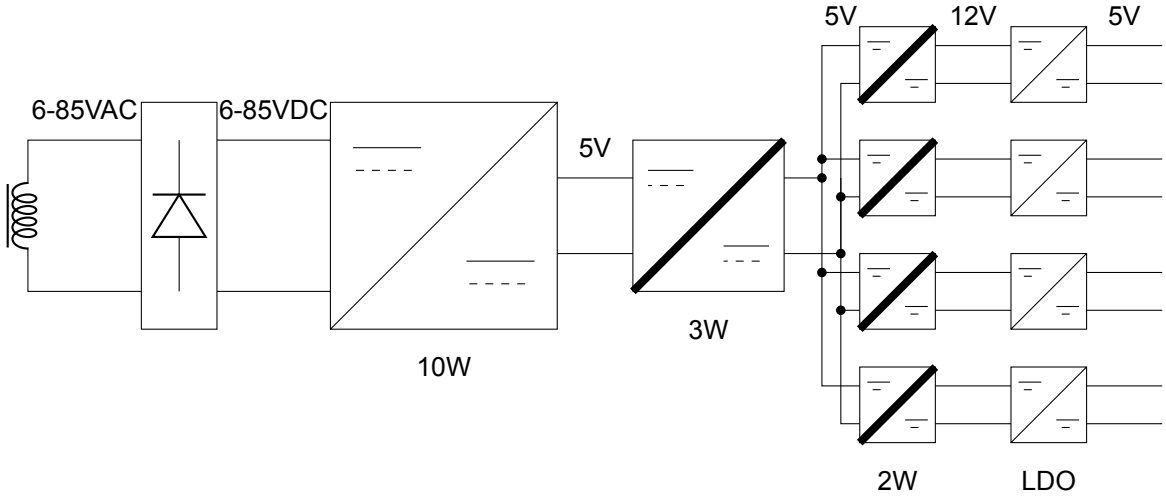


Figure 6.7: Power path, thick lines indicate 20 kV isolation

7

PCB design

A PCB was designed to create a compact design of the submodule. Care was taken for the high-voltage isolation of the signals, and the integrity of the low voltage signals. The PCB was designed in the open source software KiCad. Firstly, a schematic was created in the schematic editor with all the necessary components. Footprints of the components were assigned, and the PCB layout was designed in the PCB editor. These steps will be described in more detail in the following sections.

7.1. KiCad schematic

The full schematic can be seen in Figure 7.1. It will be broken down and explained in the later sections. The schematic was created in KiCad, using models of the component schematic models from SamacSys and UltraLibrarian.

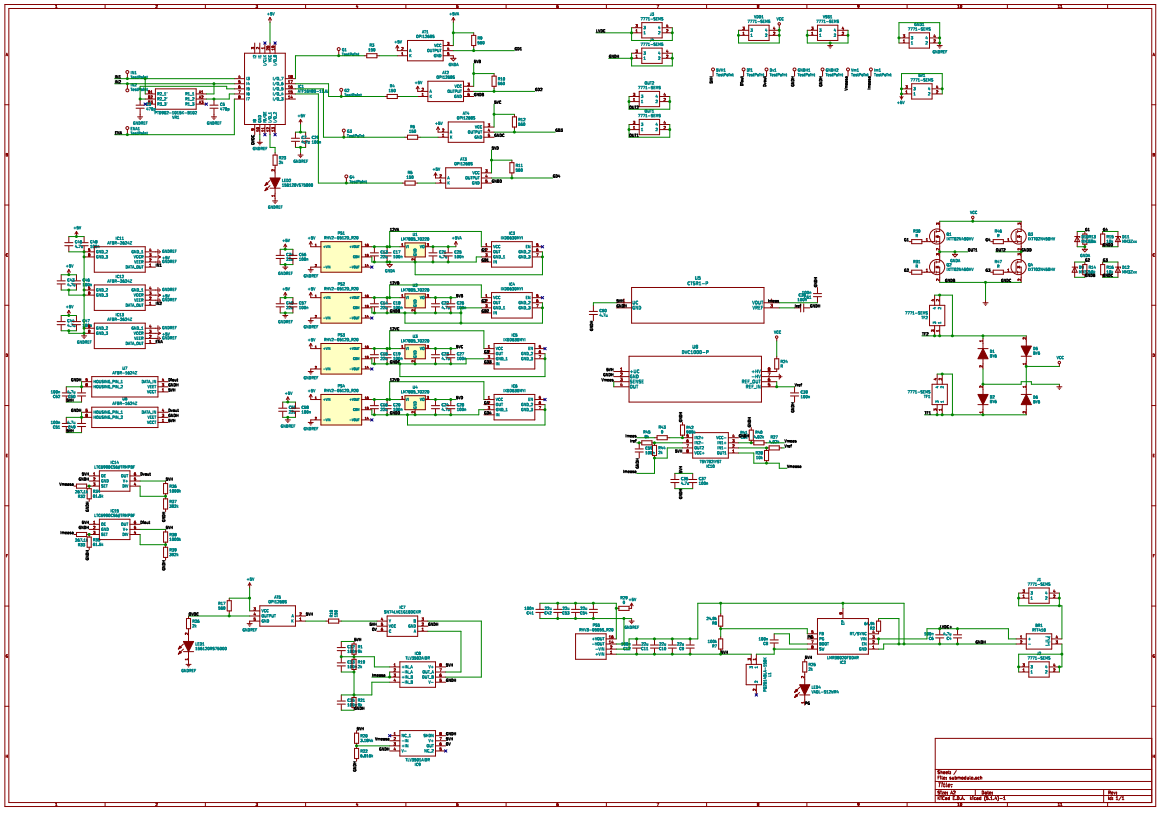


Figure 7.1: Full schematic

7.1.1. Full-bridge

The schematic for the full-bridge can be seen in Figure 7.2. The MOSFETs with gate resistors can be seen. Also the gate protecting zener diodes can be seen, along with the gate discharge resistors. The DC bus voltage is created from the full-bridge diode rectifier. This is fed by the transformer using the 7771-SEMS screw connectors.

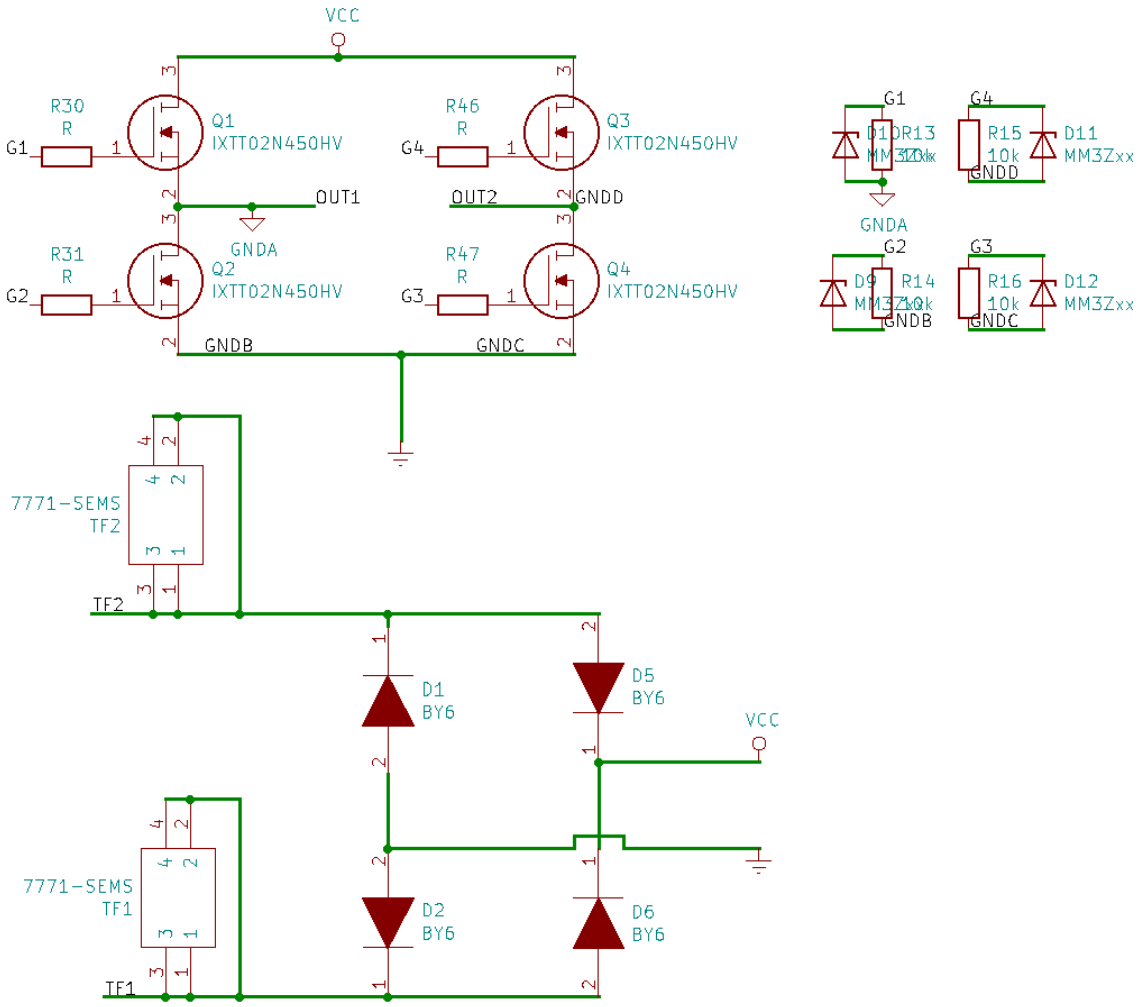


Figure 7.2: Full-bridge schematic

7.1.2. Gate drivers

The schematic for the gate drivers can be seen in Figure 7.3. The IXDD630MYI gate drivers are powered by the isolated 12 V converters. These also power the LDO regulators that are needed for the optocouplers.

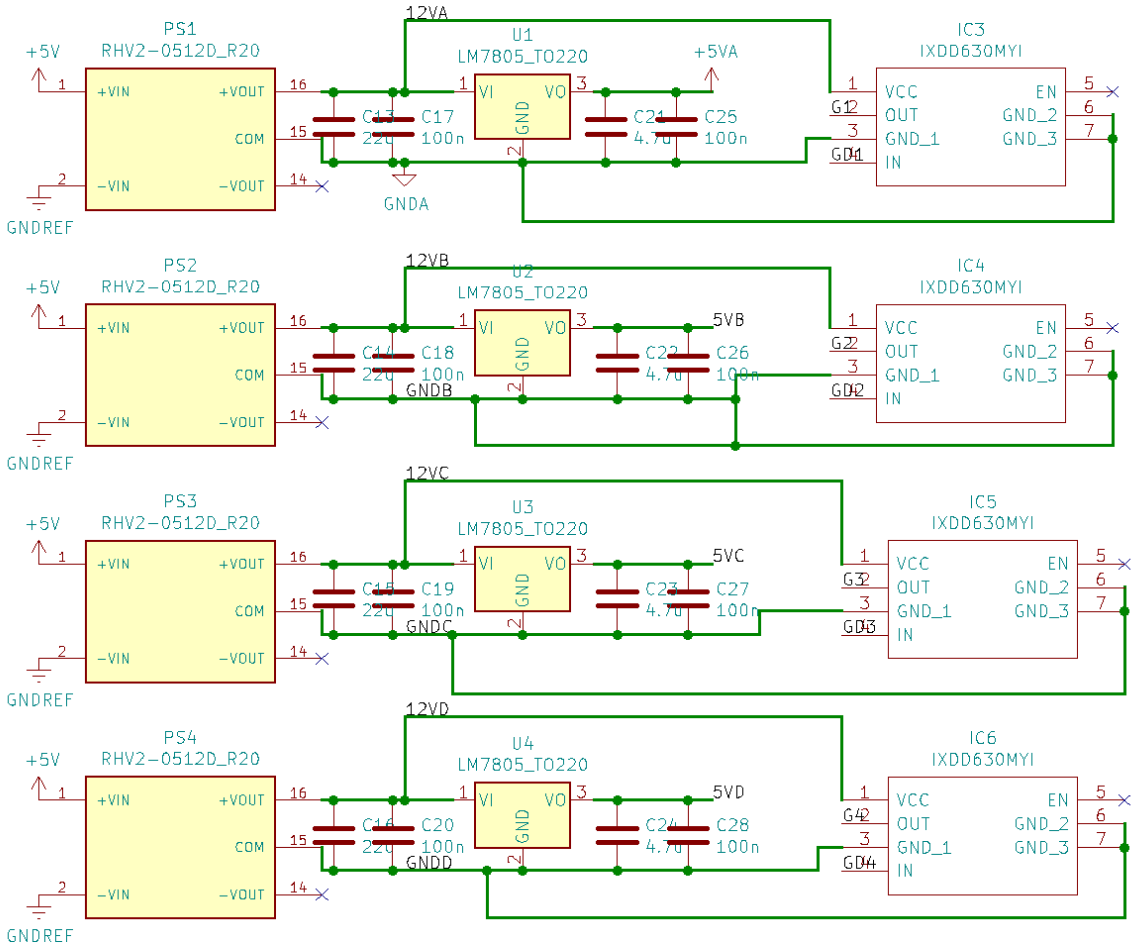


Figure 7.3: Gate drivers schematic

7.1.3. Input controller

The Programmable Logic Device (PLD) and optocouplers can be seen in Figure 7.4. The dead time is implemented using a two-gang 1 kΩ potentiometer and two 470 pF capacitors. These, delayed inputs, as well as the direct inputs are fed into the PLD. Another input is the enable signal. An LED is added to indicate that the PLD is on and enabled. The low side of the input of the optocouplers is switched because the PLD can sink more current than it can source. A current limiting resistor of 150 Ohm is then inserted to limit the current throught the LED of the optocoupler. The output of the optocoupler is pulled high using a 560 Ohm resistor. This is recommended by the manufacturer of the optocoupler.

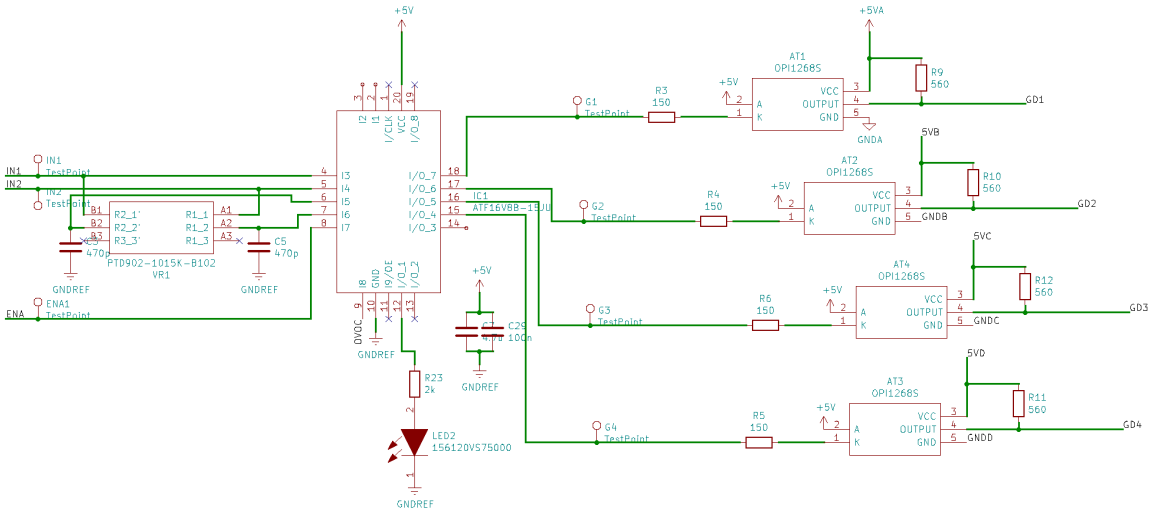


Figure 7.4: PLD schematic

7.1.4. Power delivery

A buck converter was used to create the 5 V supply that is needed to power the low voltage components on the board. An LMR38020 buck converter is used. This chip can handle input voltages from 6 V to 80 V. This means that a wide range of input voltages can be used. The board can be powered with a 6 V to 80 V DC supply, or a 6 V to 80 V AC supply that is connected to a full-bridge diode rectifier. The diode rectifier is a RTT410 that is capable of handling voltages up to 1000 V and 2 A. A 15 μH inductor is used to smooth out the output voltage, along with the capacitors. A feedback voltage divider is setup according to the datasheet of the LMR38020 to create an output voltage of 5 V [27].

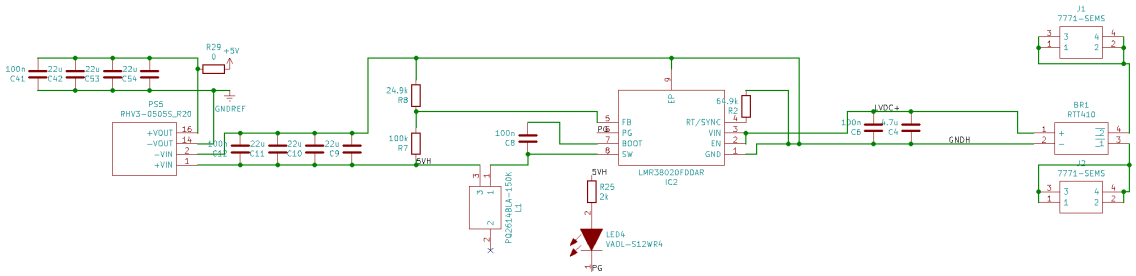


Figure 7.5: 5V generation schematic

7.1.5. Voltage and current measurement

The voltage- and current sensor circuits can be seen in Figure 7.6. The sensors were chosen based on their input range and speed. The DVC 1000-P can measure voltages from -1 kV to 1kV. The submodule is supposed to work up to 5 kV, so a voltage divider was introduced to measure the voltage. The DVC 1000-P has an internal resistance of 12.6 MΩ. A series resistor of 40 MΩ was added to reduce the voltage over the sensor by a factor of $\frac{12.6}{12.6+40} = 0.24$. This means that the sensor can now measure voltages from 0 to 4.1 kV steady state, with peaks up to 6.2 kV. Adding a series resistor could have impact on the speed of the sensor, since the input capacitance of the sensor will be charged through the high resistance.

The output of the sensor is amplified using a difference amplifier. The sensors have a reference voltage around which the signal is centered. The sensors are designed for positive and negative values of voltage and current. An output under the reference voltage indicates a negative value, and an output voltage above the reference value indicates a positive value. The reference voltage can be set

externally, or it can be kept at the internal value of 2.5 V. The output voltage range of the sensors is from 0.5 V to 4.5 V. For the voltage sensor, only positive voltages will be measured. The reference voltage was kept at the internal 2.5 V by connecting the REF_IN pin with the REF_OUT pin. The reference voltage is then subtracted and the voltage was multiplied by 2.5x using the difference amplifier. In this way, a range of 0 V to 5 V was created, indicating a input voltage range of 0 to 6.2 kV. This was done using the difference amplifier described in Figure 6.6 and Equation 6.13, with values of 4 kΩ for R_1 and R_2, and 10 kΩ for R_3 and R_4. Since there were no 4 kΩ resistors available, a 4.02 kΩ resistor was chosen instead.

For the current sensor, positive and negative currents will be measured. The internal reference voltage of 2.5 V is also kept for the current sensor. The insulation of the current sensor is not sufficient for the 4 kV working voltage of the submodule. It was thus opted to use an insulated wire through the hole of the current sensor. In this way, the insulation will take most of the voltage, so the current sensor does not break down. The CTSR 1-P has a range of -1 A to 1 A.

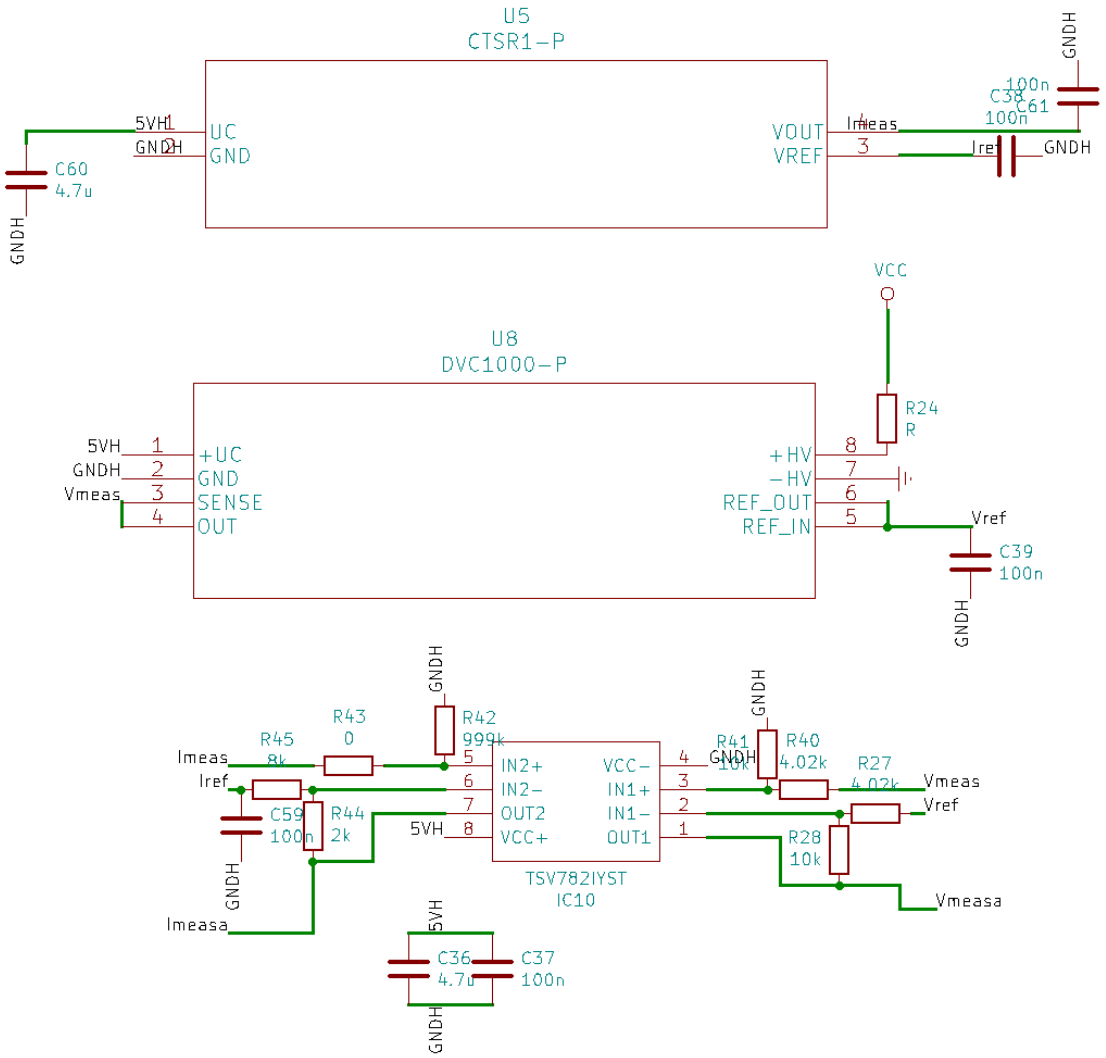


Figure 7.6: Sensors and amplifier schematic

7.1.6. Fault detection

The fault detection is comprised of comparators and a NAND gate. There is an upper limit for the voltage, and an upper limit and a lower limit for the current. Because the current can flow in both directions, a positive and a negative limit is set. The voltage limit is set to 4 kV and the current limit is set to ±0.2 A. If the voltage or current exceeds these values, the input to the NAND gate will be pulled low and the fault signal will go high. This is then sent to an indicator LED and the PLD.

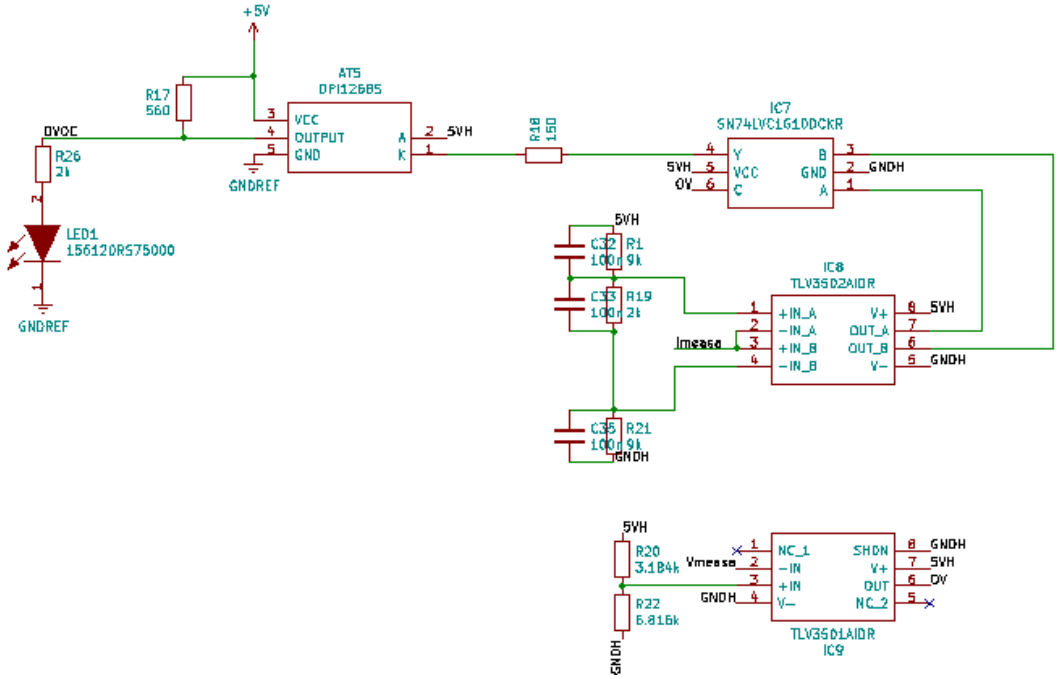


Figure 7.7: Fault detection schematic

7.1.7. Sensor readout

The sensors outputs are converted into a digital signal to be read out by an external controller. The LTC6990 voltage controlled oscillators are used for this. The output is a square wave signal, where the frequency depends on the input voltage. The frequency range is set to 3.906 kHz to 62.5 kHz using the complementary resistors. This output is made availabe via a pin and via a fiber optic output.

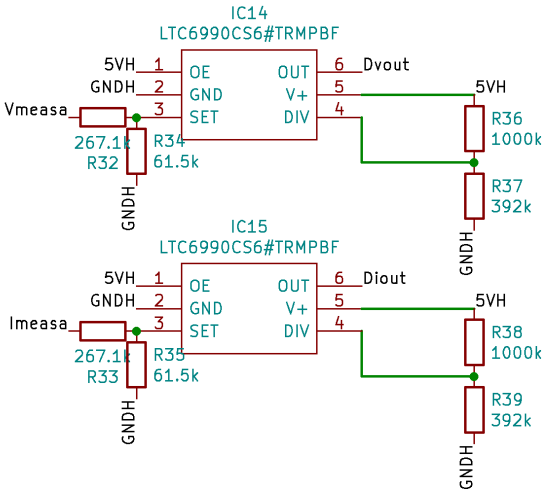


Figure 7.8: VCO schematic

7.1.8. Fiber-optic inputs and outputs

Fiber optics are used to transfer signals to and from the board. This is done to guarantee the needed voltage isolation. The input signals to drive the full-bridge and the enable are available as fiber optic input. The digitized output of the current sensor and the voltage sensor are made available as fiber optic output. For the input the AFBR-2624Z is used. This fiber optic receiver is fast and compatible with fiber optic controllers like the Typhoon HIL. The AFBR-1624Z is used for the output. This is a similarly fast fiber optic transmitter that is also compatible with the Typhoon HIL.

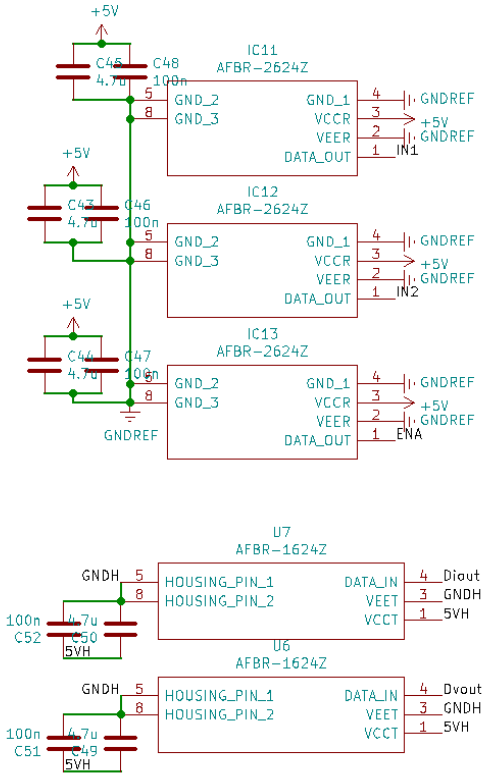
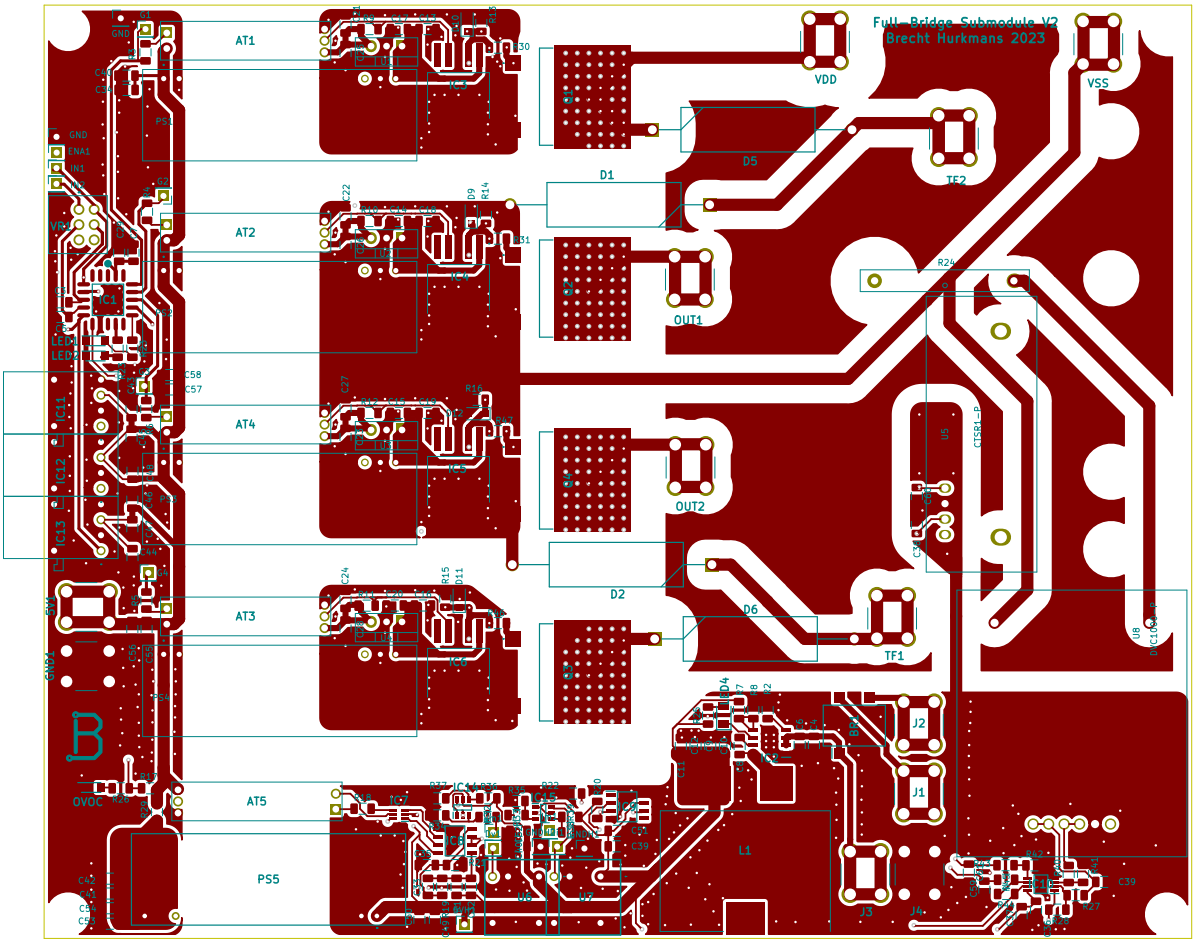


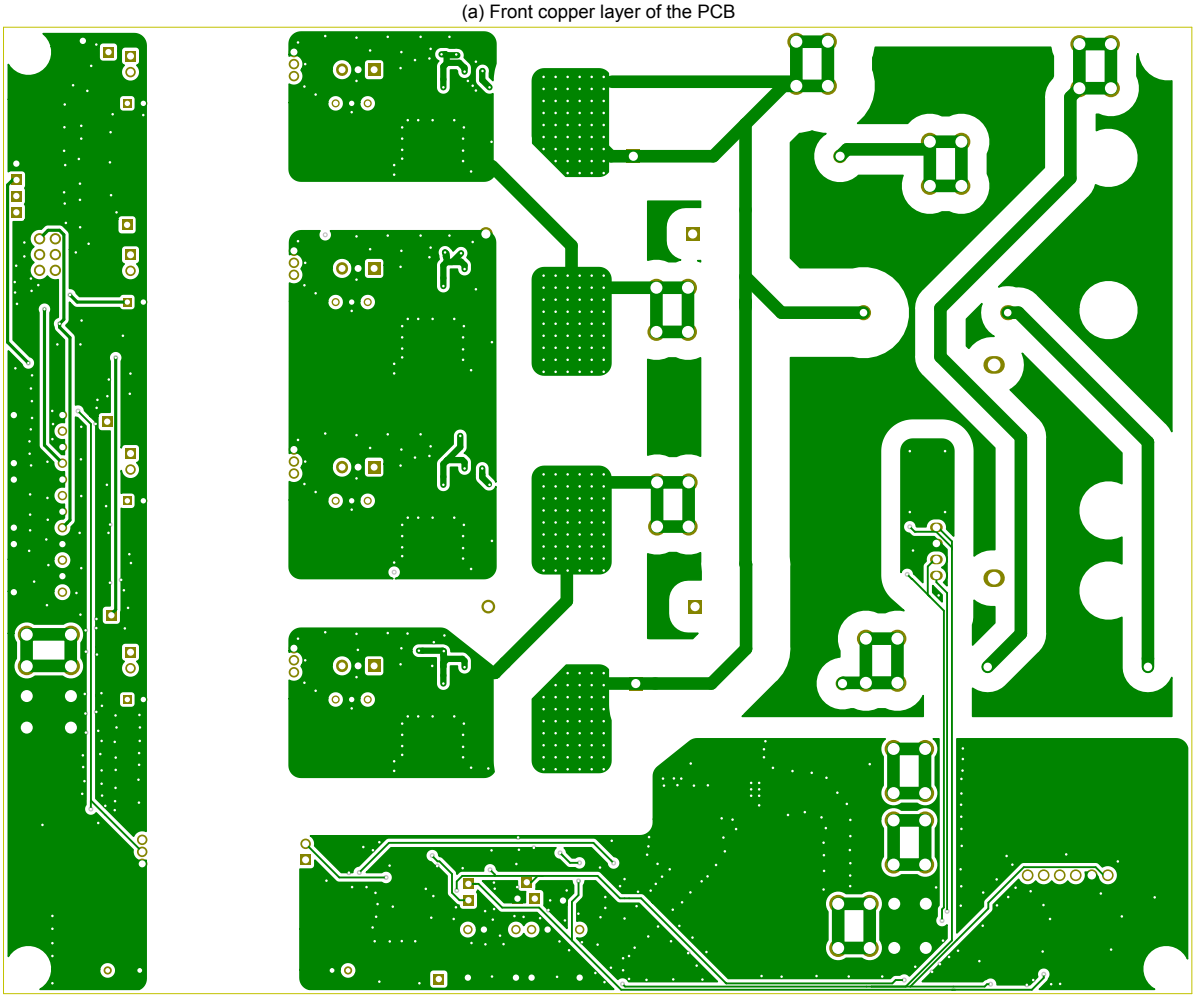
Figure 7.9: Fiber optics schematic

7.2. KiCad PCB layout

For the PCB design, several aspects were taken into account. Firstly, the clearance between the high-voltage traces should be sufficient to prevent flashover. In general, a clearance of 6 mm was maintained. This was the same clearance as the distance between the drain and the source of the MOSFETs. Between the two layers, only the thickness of the dielectric can be maintained. This should be sufficient, since the board is 1.5 mm thick. Abdelmalik et al. found that there is a partial discharge inception voltage of 12 kV for a 1 mm thick PCB [28]. Secondly, the loop inductance of the gate driving should be minimized. Inductance in the gate driving loop causes the gate voltage to oscillate. This can cause the gate voltage to become too high and destroy the MOSFET, or it can cause oscillations on the output of the MOSFET. This can be mitigated by putting the gate driver as close as possible to the MOSFET and making the tracks wide and short. The gate connecting is also put on both layers using vias to reduce the inductance even further. By increasing the thickness of the conductor, the inductance is decreased [29].



(a) Front copper layer of the PCB



(b) Back copper layer of the PCB

Figure 7.10: PCB design files

7.3. Manufacturing

During the ordering of the PCB, it was pointed out by the manufacturer that the copper on the PCB was not uniform. This can lead to problems during manufacturing, such as too much copper in an area or too little copper in an area. This can be solved by adding a copper plane between the high-voltage traces, so the copper is more uniformly spread over the PCB. The high-voltage clearance needed to be taken into account, so the copper area was kept floating and not tied to any voltage. In this way, there could be a clearance between any trace and the copper area of 3 mm, so the total clearance between two traces stays at 6 mm in total. This copper area was added in the second version, as can be seen in Figure 7.10.

7.4. PCB assembly

There were several problems that were encountered during the assembly of the first PCB. The footprint of the voltage transducer was incorrect. The downloaded model was mirrored and the pins were offset from each other. This was solved by mounting the voltage transducer on the bottom of the PCB, and skewing the sensor for the offset. One of the resistance values was also incorrect. While it should have been 1 kΩ, the ordered resistor was 10 Ω. The gate resistors could also have been placed closer to the gate driver and the MOSFET, since the components did not take up all the space in the footprint. The pin headers used to connect to external measurements and controllers were also smaller than expected. These should have been the 2.54 mm footprints instead of the 1 mm footprints. These issues were dealt with and the first PCB was assembled. Firstly, solder paste was applied to the solder pads of the SMD components. The SMD components were placed on top of the solder paste. Once all the SMD components were in place, the PCB was placed onto a hot plate and heated up until the solder melted. The PCB was removed from the hot plate and cooled down. The PCB was then inspected under a microscope. Wherever there were solder bridges, they were removed using a soldering iron and flux. The PCB was then cleaned using isopropyl alcohol. After this, the through-hole components were soldered onto the board, one by one. The voltage transducer was mounted on the bottom, so the correct pins lined up.

These problems were fixed in a second version of the PCB. The PLD was also programmed to turn the board off, not only during a fault, but also after a fault. The system can be reset by pulling the enable signal low and re-enabling the board.

8

CHB transformer

To power the cascaded H-bridge modules, isolated transformers are needed. The isolation on the transformer is created by a 3D printed bobbin mould that houses the transformer windings. It is then filled with silicone rubber to have increase the insulation of the windings. This isolation is needed since the ferrite core is conductive. A ferrite core is used to create the best magnetic coupling for the transformer. Its high magnetic permeability means that the primary side and the secondary side of the transformer have a good coupling of magnetic flux. The transformer described in this chapter was designed and built by Professor Mohamad Ghaffarian Niasar.

8.1. ZVS driver

To drive the transformer, an AC wave is needed. This wave can be generated by a function generator. However, the power that is needed to drive the transformer might be too high for function generators. It was opted to use a Zero Voltage Switching (ZVS) driver. This driver converts a DC voltage into an AC sine wave. This sine wave is of a higher amplitude than the input voltage, because it makes use of resonance between the capacitor and an inductive load. The circuit can be seen in Figure 8.1.

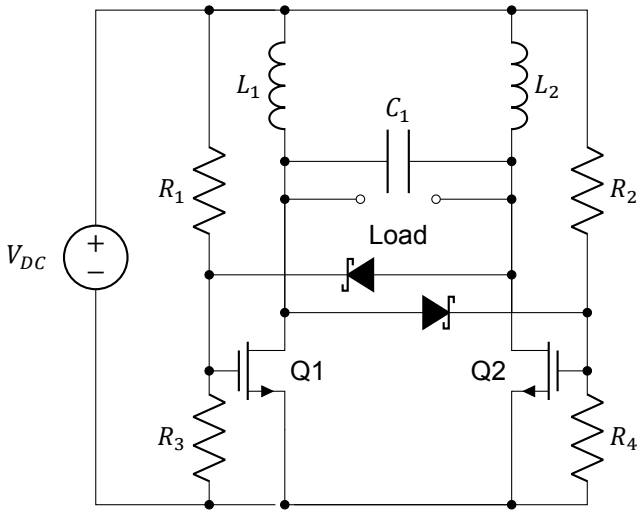


Figure 8.1: ZVS driver circuit

When the circuit starts up, one of the MOSFETs will turn on first due to dissimilar parasitic elements. When one of them is turned on, the other gate will be pulled low through the load inductor. The voltage on one side will rise and then go down because of the resonant circuit. This will cause the MOSFET to turn off, and in turn the rise in voltage over that MOSFET will turn the other MOSFET on through the diode. In this way, a sine wave is created over the inductive load, which can be used to drive the transformer and power the secondary side.

Figure 8.2: Bobbin with secondary winding of the transformer

8.2. Bobbin

The secondary winding of the transformer was made on a 3D printed bobbin. This bobbin has grooves to house the turns of the transformer and it has guides for the connecting cables. The bobbin can be filled with silicone rubber to create the desired isolation of the transformer. There is a gap between the bobbin and the core, as well as between the bobbin and the outside. The bobbin can be seen in Figure 8.2.

8.2.1. Isolation turn

An isolating turn was added in between the sections on the bobbin to create the needed isolation voltage. A close-up can be seen in Figure 8.3. This isolating turn is added to separate the sections of the secondary winding. This turn will make sure that the last turn of a segment does not touch all the other layers of the next segment. The last turn exits from the top of the first segment, whereas the second segment begins on the bottom. By wrapping the wire around the bobbin another time, this wire is separated and does not touch all the layers of the second segment. This is important for high-voltage isolation since the voltage difference between touching wires is minimized.

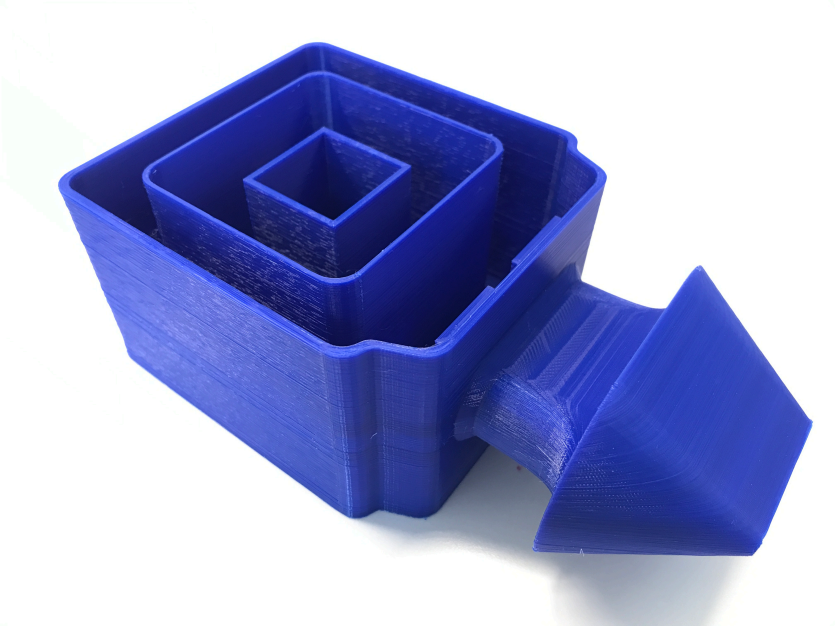


Figure 8.4: 3D printed housing of the secondary side of the transformer

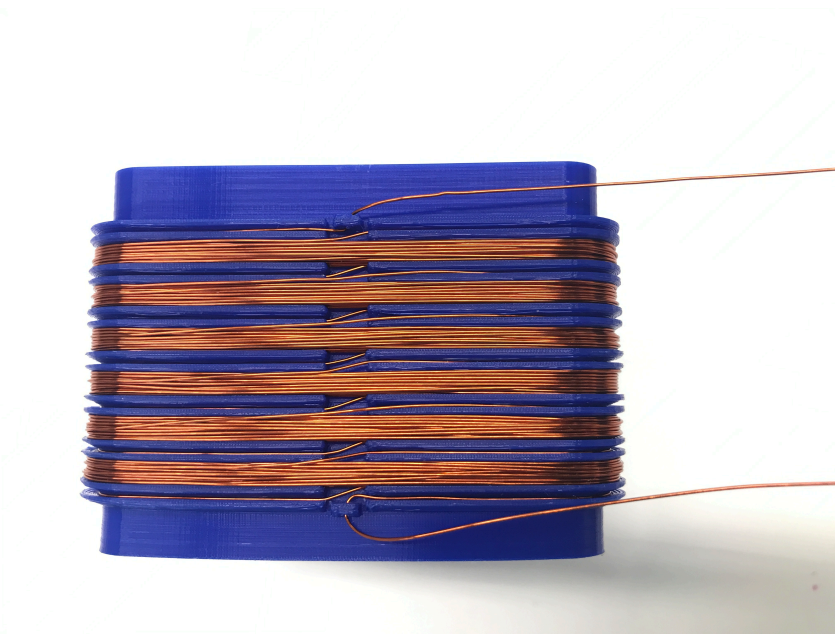


Figure 8.3: Secondary winding with isolation turn

8.3. Transformer

The housing of the secondary side of the transformer was 3D printed. In this way, it could be used as a mould for the silicone rubber, it could house the bobbin, and guide the wires to separate them. A picture of this 3D print can be seen in Figure 8.4. It can be seen that there is a space for the core to enter through. There is an air gap between the core and the main compartment. In the main compartment, the bobbin can be placed. Wires can then be attached to the winding, going out through the extended part. The extended part has a bushing shape to minimize the electric field around the exiting wires. The main compartment can then be filled with silicone rubber or other isolation materials.

4 turns were used on the primary side, with 250 turns on the secondary side. With a turns ratio of 1:62.5, a primary voltage of 64 V would be needed on the primary side to generate 4 kV on the

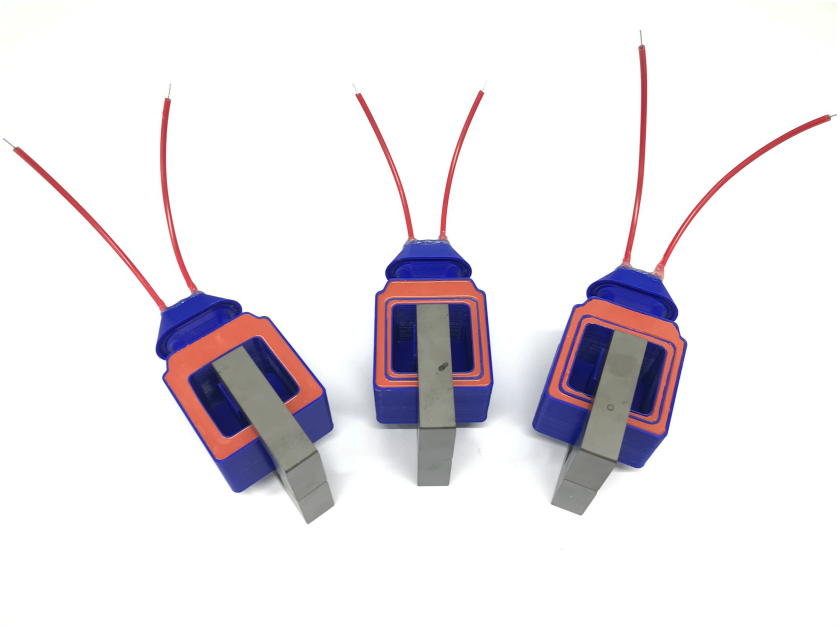


Figure 8.5: High-voltage isolating CHB transformers, filled with silicone rubber

secondary side. Since the primary voltage is multiplied by π, the driving supply voltage should be around 20 V.

For the ZVS driver, a generic commercially available device was used [30]. For the core, two Ferroxcube U100/57/25-3C90 cores were put on top of each other, with the primary and secondary winding around the legs.

The fully assembled transformers can be seen in Figure 8.5.

9 Testing

The prototypes were tested in the lab. Based on these tests, the prototypes were improved and rebuilt.

9.1. Two MOSFET switch

The prototype was tested by connecting it to a power supply. A separate power supply was used for the gate driver. The gate signal was connected to an Arduino microcontroller that provided the necessary timing. The grounds of the two power supplies and the Arduino were connected together. Two oscilloscope probes were connected to the balance resistors to measure the voltage across the lower MOSFET and the voltage across both MOSFETs. The main power supply was set to 100 V and the gate driver power supply was set to 15 V. The code that was uploaded to the Arduino can be seen in Appendix B.1. The output of the gate driver can be seen in Figure 9.1. It can be seen that it has the expected on-time of 1 μs and voltage of 15 V.

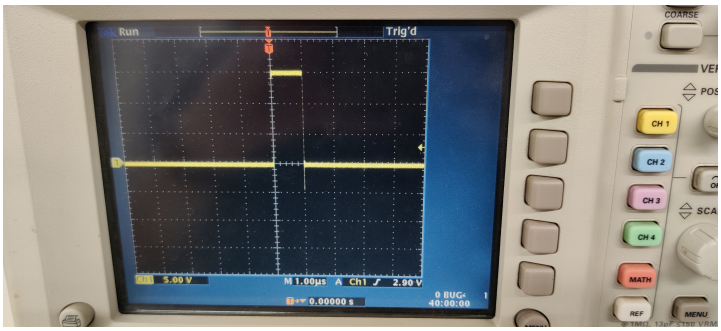


Figure 9.1: Gate driver output

The voltage across the first MOSFET was directly measured and the voltage across the second MOSFET was calculated using the math mode on the oscilloscope. To do this, the first channel (V_{ds} across the first MOSFET) was subtracted from the second channel (voltage across both MOSFETs). The result of this can be seen in Figure 9.2. It can be seen that there is a static- and dynamic voltage imbalance. This can (partly) be attributed to the influence of the oscilloscope probes. The probes have a finite resistance and a capacitance. The 10 MΩ resistance of the probe interferes with the 1 MΩ balancing resistor of the lower MOSFET, causing it to share less of the voltage. The capacitance of the probe also acts as a snubber capacitor, causing the voltage of the lower MOSFET to rise slower. This causes some dynamic voltage imbalance when turning off.

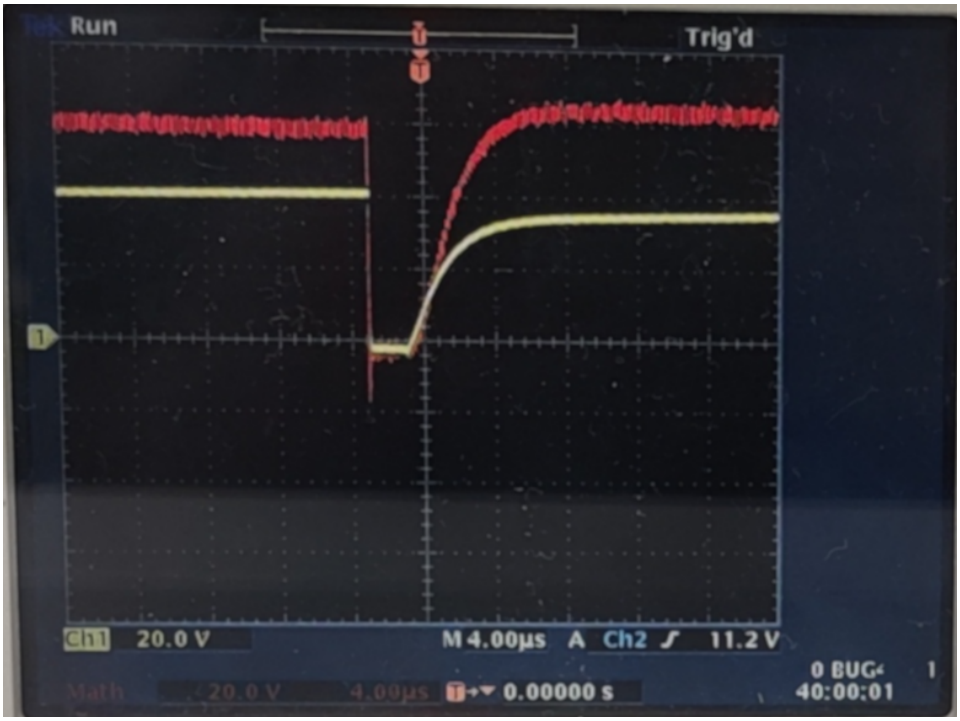


Figure 9.2: Balance of two MOSFETs

9.2. Six MOSFET switch

The six MOSFETs in series were tested in a similar way to the two MOSFETs in series. The gate driver was connected to the Arduino for the gate signals. The board and the Arduino were powered from a portable battery bank using the USB outputs. The 5 V and ground line of one of the USB ports was used to power the 12 V converter that powers the gate driver. The high-voltage supply consisted of a Spellman SL150. The oscilloscope probe was connected across the whole switch, to eliminate the aforementioned influence of the probes on the balance of the MOSFETs. The voltage was slowly raised to 4 kV. Before around 2 kV, no switching behaviour was observed. This can be attributed to the fact that the coupling capacitors were not able to hold enough charge to turn the MOSFETs on. The charge in the capacitor should be above a certain charge level to turn the MOSFET on, and since $Q = CV$, the coupled MOSFETs would not turn on below a certain supply voltage. The results from this test can be seen in Figure 9.3. It can be seen that the MOSFET does not stay on for the desired 1 μs. This is probably caused by the non-ideal components in the switch. The coupling capacitors discharge in around 250 ns, instead of the set 1 μs. There is also a stair-stepping pattern in the falling edge of the signal. It could be caused by the parasitic capacitances being higher than expected, causing the coupling capacitors to be too low. This will cause the MOSFET to turn off in steps and lower the expected on-time of the switch. The switch was able to block the 4 kV voltage.

9.3. High-voltage full-bridge

The high-voltage full-bridge was first tested separately on a proto-board. This board can be seen in Figure 9.4. The proto-board was cut in the middle to create the separation between the high-voltage side and the low-voltage side. The isolated DC converters and the optocouplers were connected across this gap to transfer the power and gate signals. The gate drivers were connected as close as possible to the switches to minimize the leakage inductance caused by long connections. This is important to minimize the oscillation in gate voltage that can occur with the fast transitions of the gate signal. The switches were also isolated between each other by removing the solder pads between them, as can be seen in Figure 9.5. The middle two switches has their sources connected since they are connected to the ground. The gate signals for switch 1 and 3 were also connected to each other for testing purposes. In this way, the full-bridge can be controlled using two input signals.

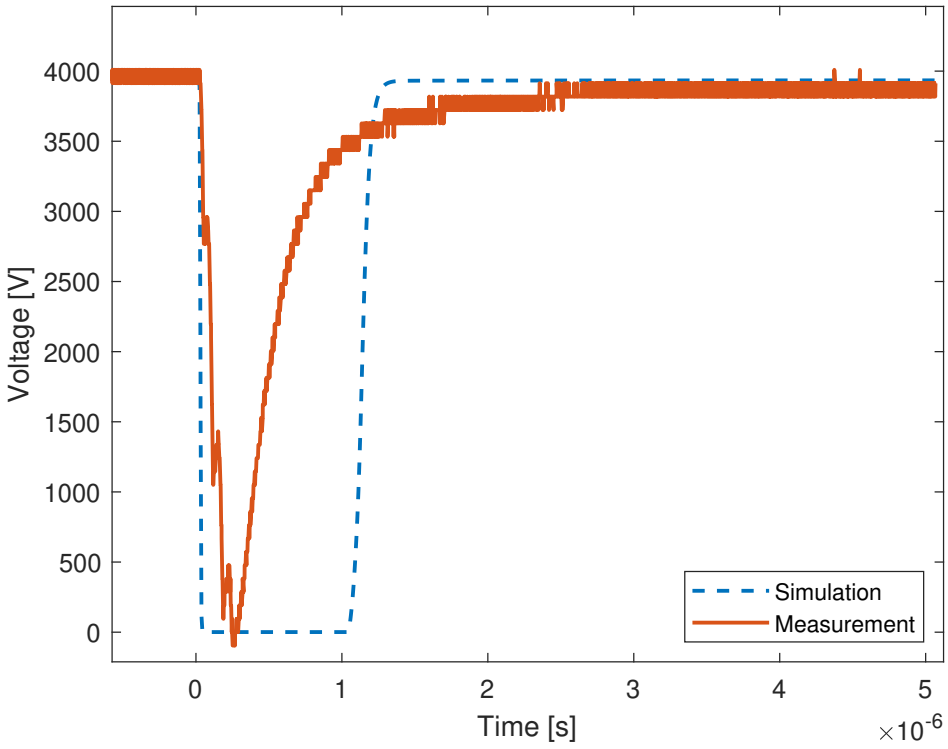


Figure 9.3: Simulated and measured voltage over the series-connected switch

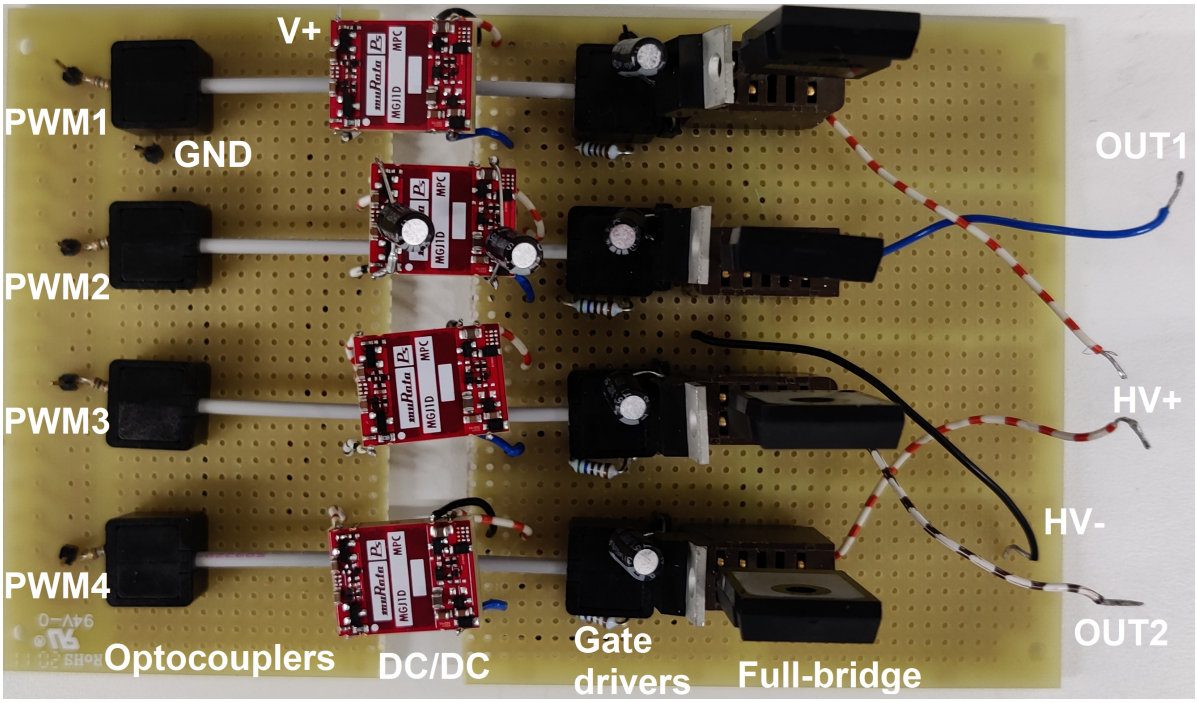


Figure 9.4: Top of full-bridge prototype board

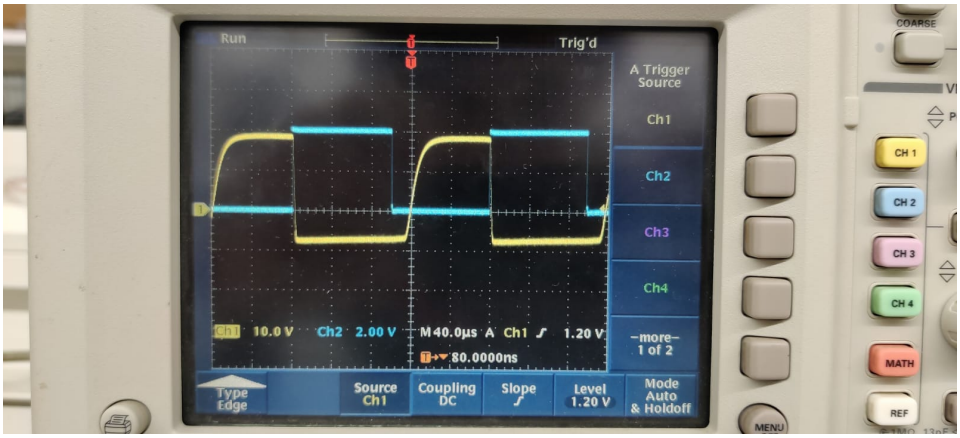


Figure 9.6: Input-to-optocoupler distortion. In blue, the input signal can be seen, with the output of the opi1280-066 optocoupler in yellow

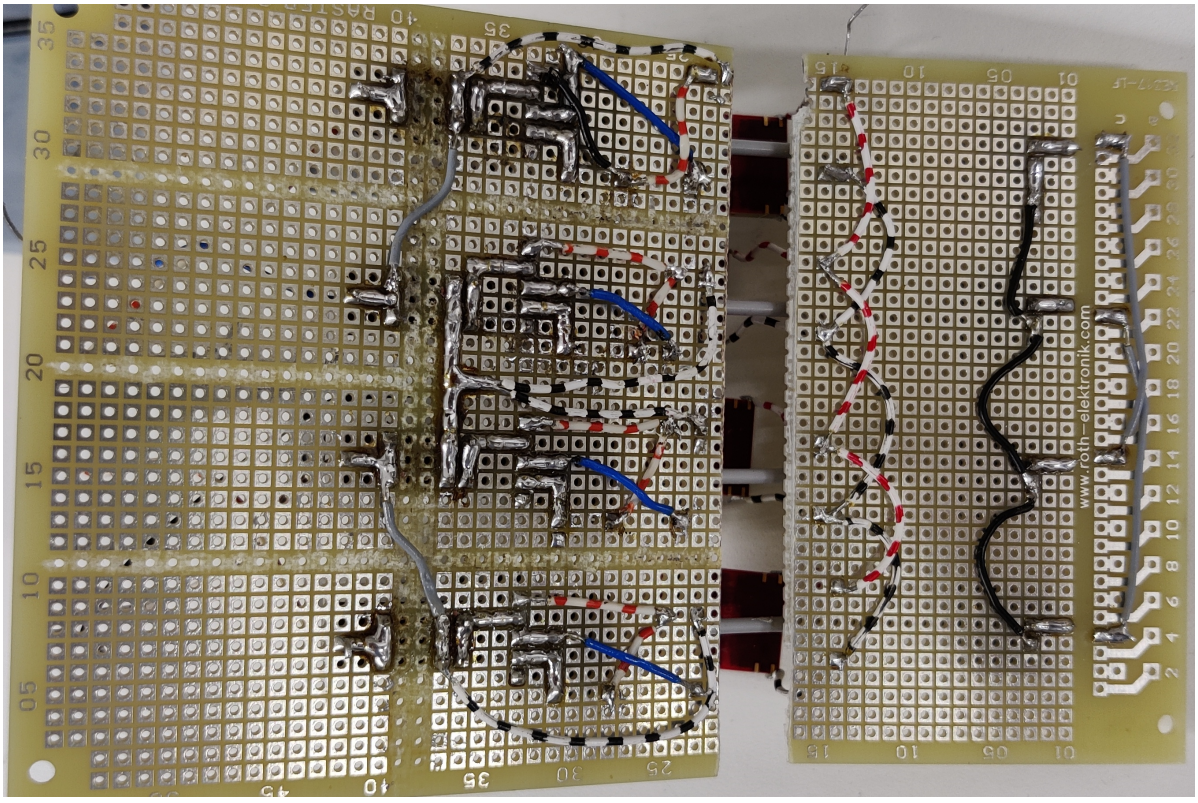


Figure 9.5: Bottom of full-bridge prototype board

The optocouplers were also separately tested. This can be seen in Figure 9.6. The cyan signal indicates the input signal for the optocoupler, the yellow signal indicates the output of the optocoupler. A slow rise time of the output can be observed. This rise time can be changed by altering the pull-up resistance. Using a lower resistance, this rise time can be decreased. The rise time being this slow is suspected to be because of a relatively high output capacitance of the optocoupler (~1 nF). This would cause distortion of the input signal which is not desired. It was decided to use a faster optocoupler for later prototypes, since this distortion was several microseconds.

The optocoupler needs a resistor to either pull-up the signal or pull-down the signal. This depends on if it is switching the high side of the power supply or the low side of the power supply. In Figure 9.7, the yellow signal indicates a resistor on the high side, and the cyan signal indicates a resistor on the low side. As can be seen, there is a slow transition when the optocoupler's parasitic capacitance

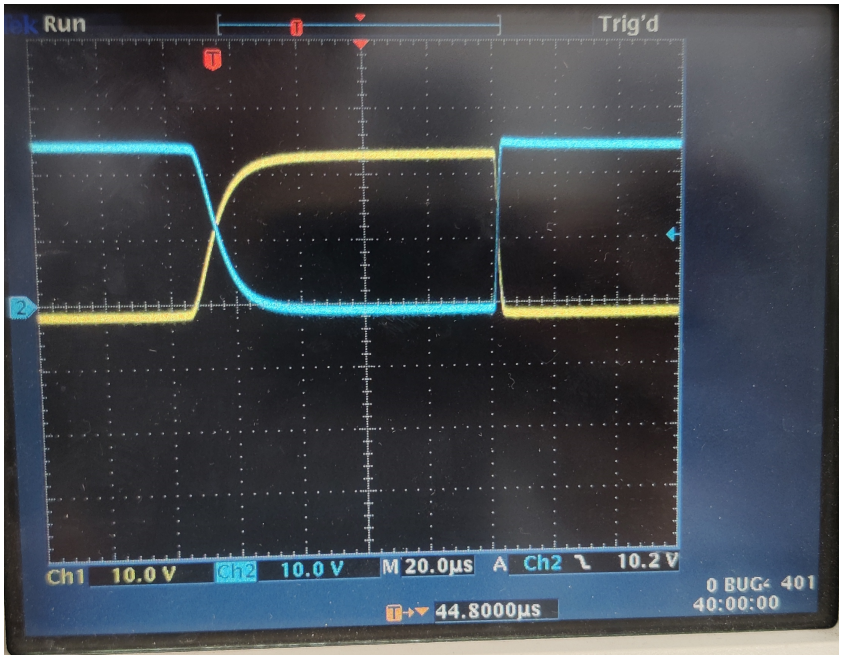


Figure 9.7: Optocoupler with inverted output (yellow) and non-inverted output (blue)

charges or discharges through the resistor when the optocoupler turns off. Because the threshold voltage of the gate driver is 0.8 V for the low transition and 3.5 V for the high transition, it was opted to used the high side resistor. In this way, the high transition would happen earlier than the low transition would happen in the low side resistor case. Because of this, the signal will be less distorted by the optocouplers. A lower resistance value can increase the speed of the optocoupler. The current limit of the optocoupler output needs to be taken into account, as well as the power supply limitations when lowering the resistance value.

The response of the faster OPI1268S optocoupler can be seen in Figure 9.8. Here, the distortion was only 30 to 45 nanoseconds (see Figure 9.9), which is an insignificant portion of the signal. Also note that the optocouplers used a different power supply. The slower optocoupler worked with the same power supply as the gate drivers (+19/-5V), while the faster optocoupler needed a separate power supply of +5V. This separate power supply was created using a Low Drop-Out (LDO) regulator. This regulator works by dropping the input voltage to a lower output voltage by dissipating power. The dissipated power is would be equal to the difference in input- and output voltage times the output current. Since the current needed for the optocoupler is low, this will not be an issue.

The following tests were conducted with the slower optocouplers and using a lower switching frequency. The prototype was connected to a high voltage supply for the output. A low voltage portable battery bank with a regulated output of 5 V was used for the gate driving circuitry. The gate signals were generated using an Arduino Uno that was also connected to the battery bank. The setup can be seen in Figure 9.12.

This setup was tested with several DC bus voltages. The resulting rise of the output voltage can be seen in Figure 9.10. The output was measured using a high voltage differential probe. No load was connected in this case. The graphs are scaled to 2 kV to compare them. The signals were also filtered using a Butterworth filter with a cutoff frequency of 10 MHz to smooth out the signals. It can be seen that there is a stepping pattern in the signal. The first step is around 350 ns and the length stays constant for each voltage. The second becomes shorter with a rising DC bus voltage, while the third step becomes longer with a rising DC bus voltage. These steps can be caused by the time difference in the optocouplers.

The optocouplers experienced some noise during the first stages of the testing. This can be seen in Figure 9.14. There is some high frequency noise present during the transition of the switching of the complementary optocoupler. This caused the gate driver to trigger multiple times, which caused noise on the output of the gate drivers as well. This can be seen in Figure 9.15. It can also be seen that

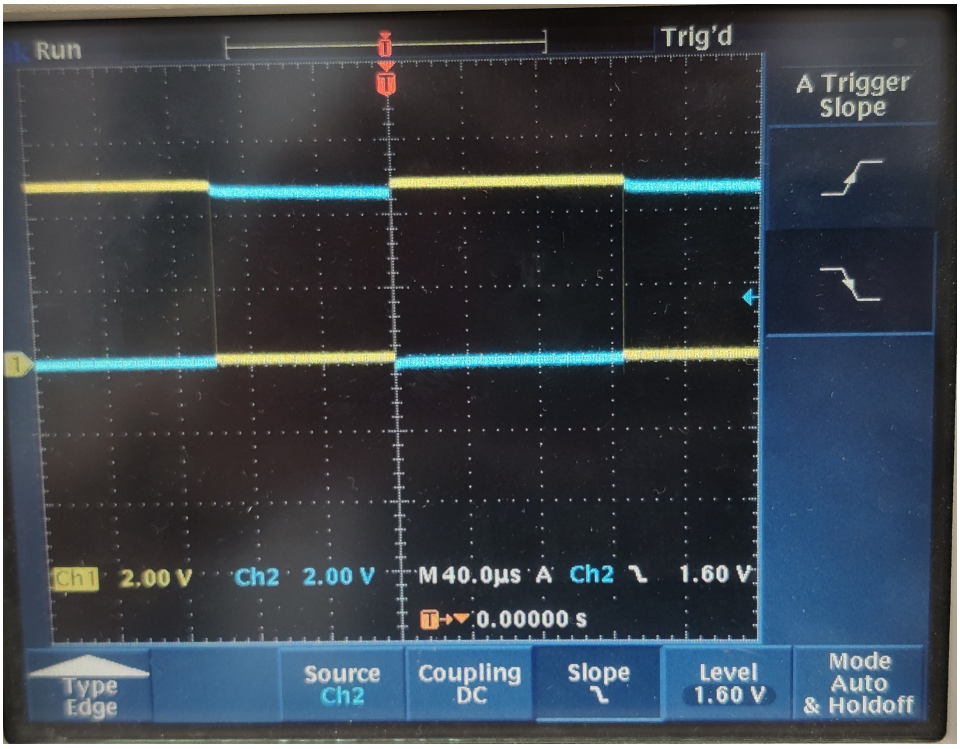
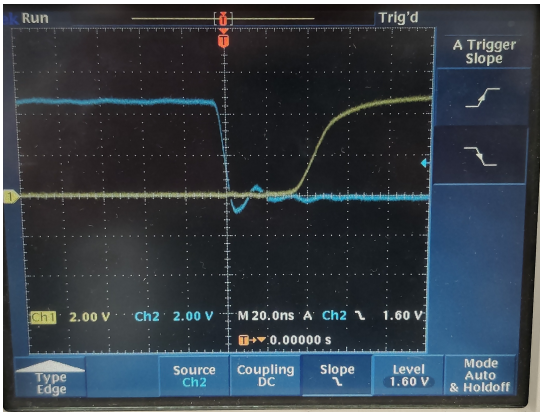
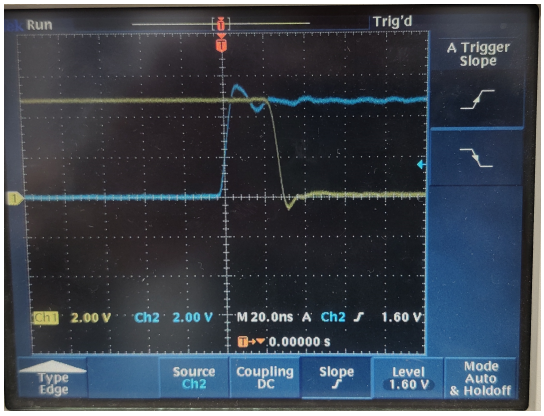


Figure 9.8: Input-to-optocoupler distortion. In blue, the input signal can be seen, with the output of the OPI1268S optocoupler in yellow



(a) Rising of the OPI1268S optocoupler output



(b) Falling of the OPI1268S optocoupler output

Figure 9.9: Rise and fall time of the OPI1268S optocoupler

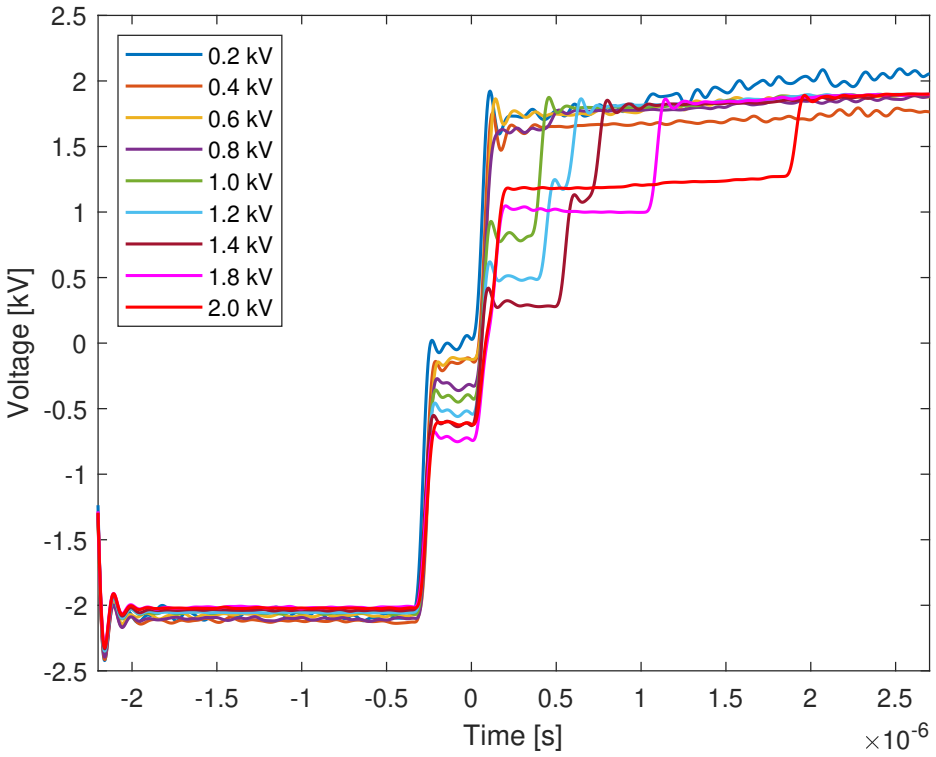


Figure 9.10: Filtered unloaded rising edge scaled to 2 kV

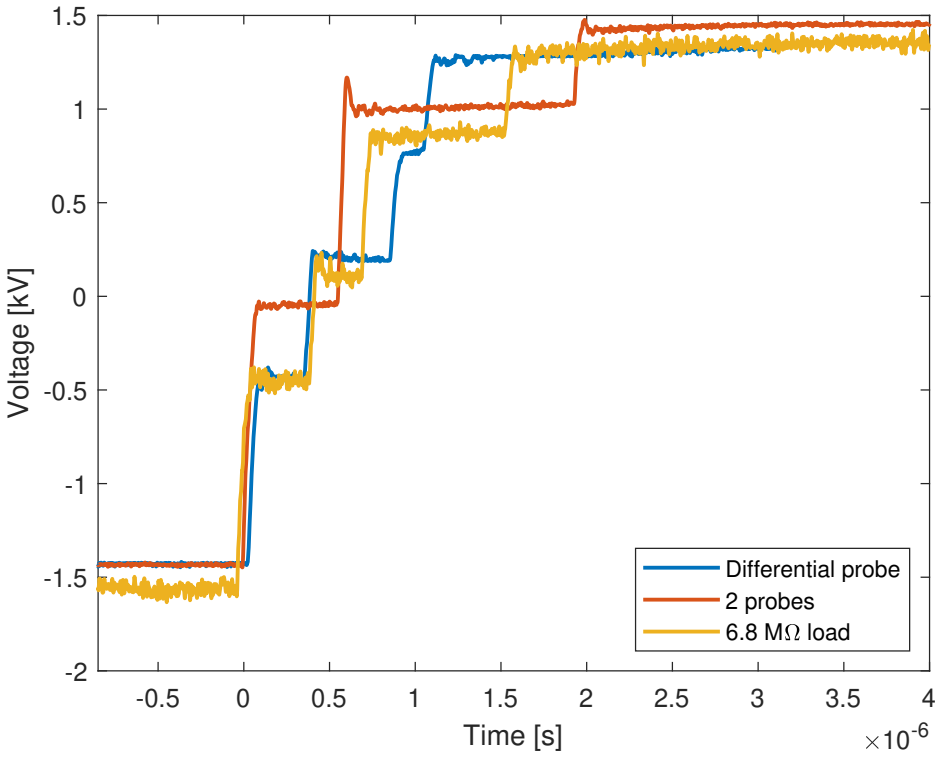


Figure 9.11: Output of full-bridge circuit with different probes and loads

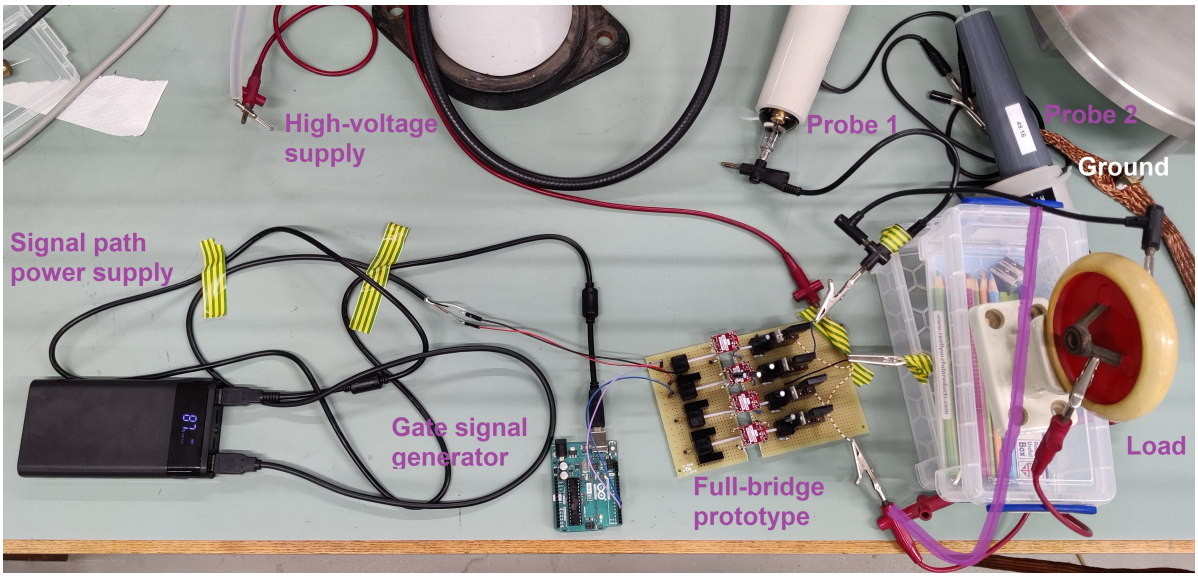
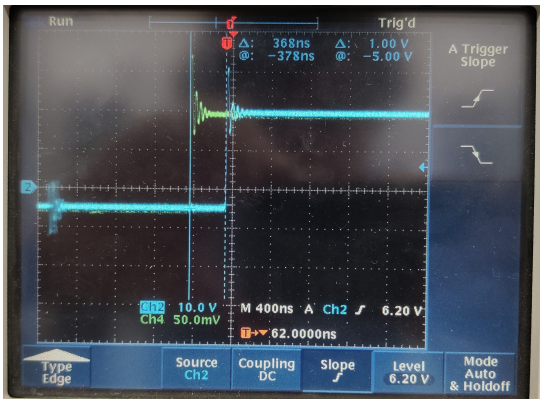
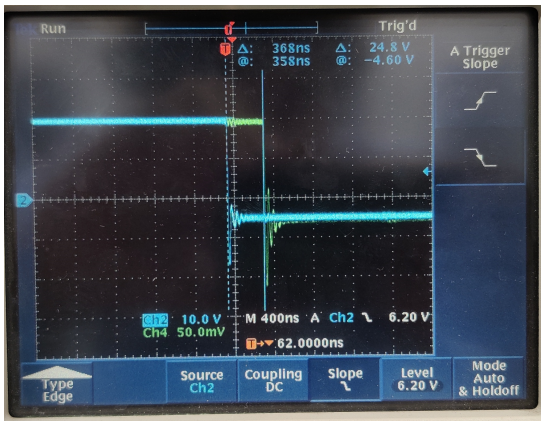


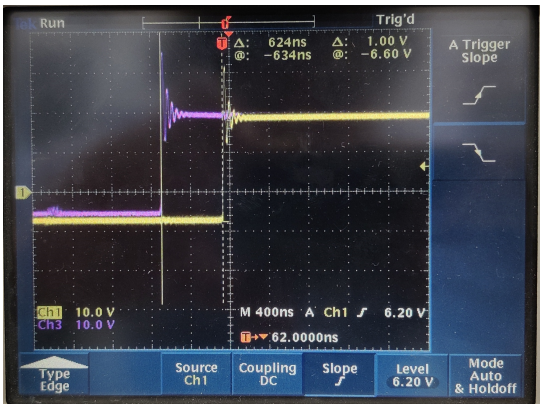
Figure 9.12: Test setup for full-bridge prototype



(a) Rising V_{GS} of switch 1 and 4



(b) Falling V_{GS} of switch 1 and 4



(c) Rising V_{GS} of switch 2 and 3

(d) Falling V_{GS} of switch 2 and 3

Figure 9.13: Gate signals for all switches

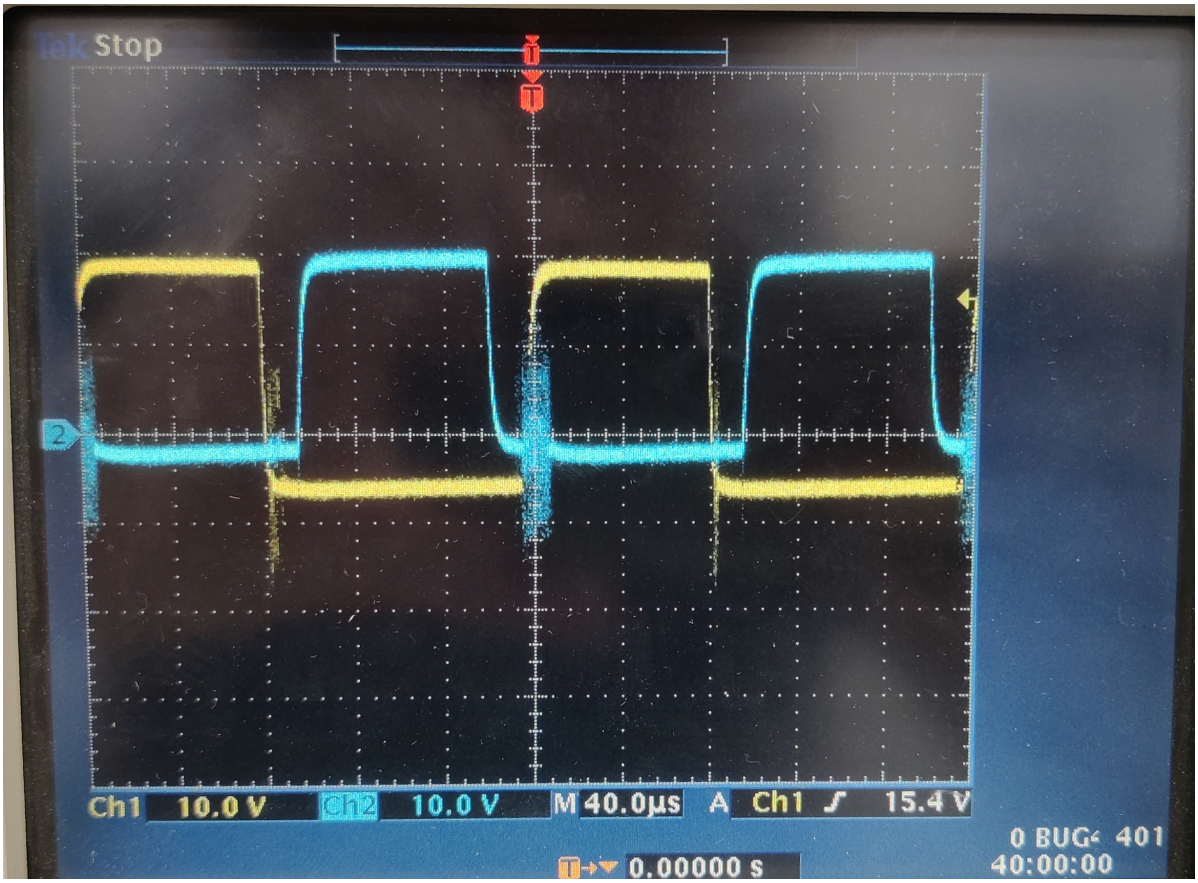


Figure 9.14: Optocoupler with noise

the gate drivers initially do no trigger at the right time, and only trigger once the noise happens. This is suspected to be caused by the power supplies being overloaded. The power supplies are rated for 42 mA, while the gate drivers and optocouplers needed more than that. The optocouplers in particular needed a lot of current to turn on with a small resistor. Once the resistor for the optocouplers was increased, the circuit worked without much noise. This can be seen in Figure 9.13. There is a bit of ringing after the transition of the gate driver but the other noise is minimised.

9.4. Submodule

After the submodule was assembled, it could be tested. The fully assembled PCB can be seen in Figure 9.16. Firstly, the separate parts of the system were tested. The buck converter was confirmed to be working, as well as all the isolated DC/DC converters. A programmed PLD was soldered onto the board. This component was also working as intended, converting the input signals into gate signals. The dead time could be set between 30 ns and 250 ns using the potentiometer. This dead time was the same for both legs. It was not symmetrical in the sense that the rising dead time would be different than the falling dead time for the same signal. It is suspected that this is caused by the threshold of the input triggering at a different time depending on if the signal is rising or falling. This will most likely not cause any problems, although the deadtime could be higher than needed if a minimum dead time on one side is required.

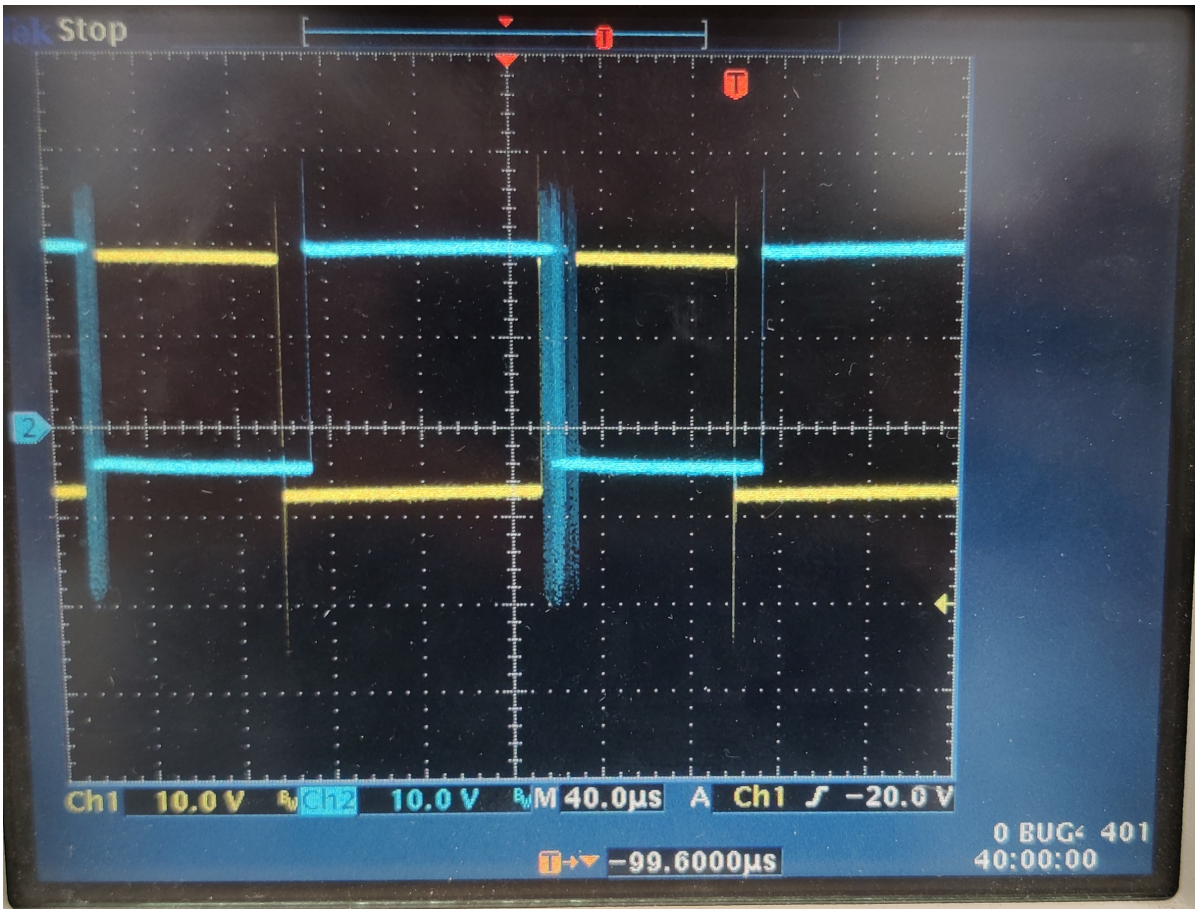


Figure 9.15: Propagated noise to gate driver

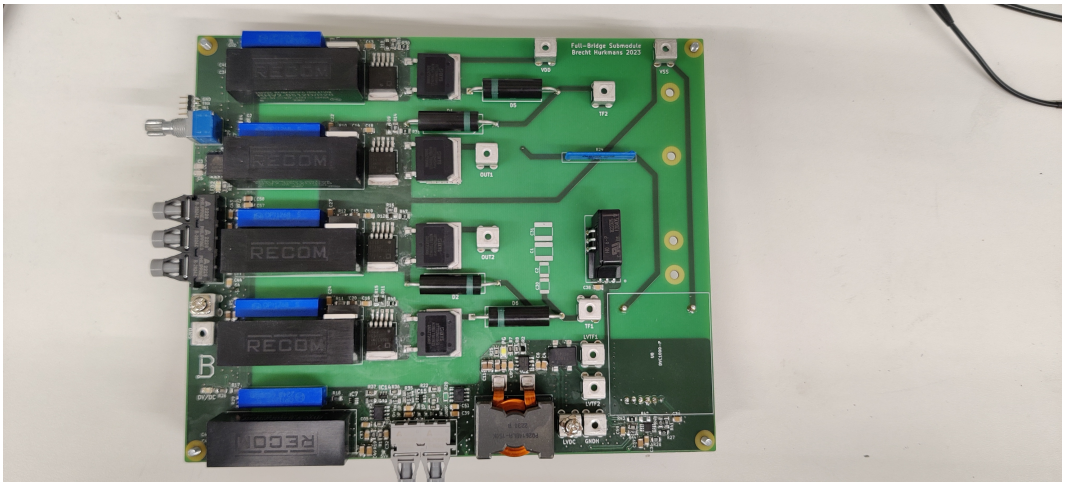


Figure 9.16: Submodule prototype

The submodule was also tested with a higher voltage applied. The high voltage was applied using a transformer with a turns ratio of . This transformer was driven by a zero-voltage switching (ZVS) driver. The low voltage side was powered using one turn extra around the core of the transformer. The output of the submodule was then measured using two high-voltage probes, referred to the ground. The difference was then calculated to get the total output. The input was set to generate a 10 kHz square wave between +VDC and -VDC. The setup can be seen in Figure 9.17. The output was measured using two high voltage probes that measured each of the legs separately. The result can be seen in Figure 9.18.

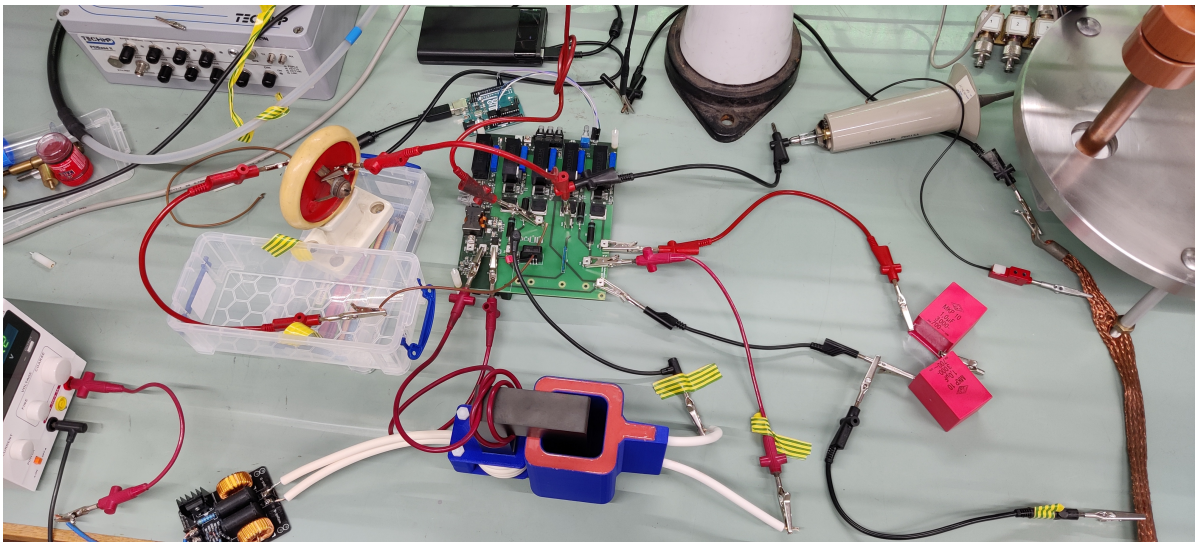


Figure 9.17: Submodule test setup

It can be seen that the submodule reacts to the input. The output is a square wave, smoothed by

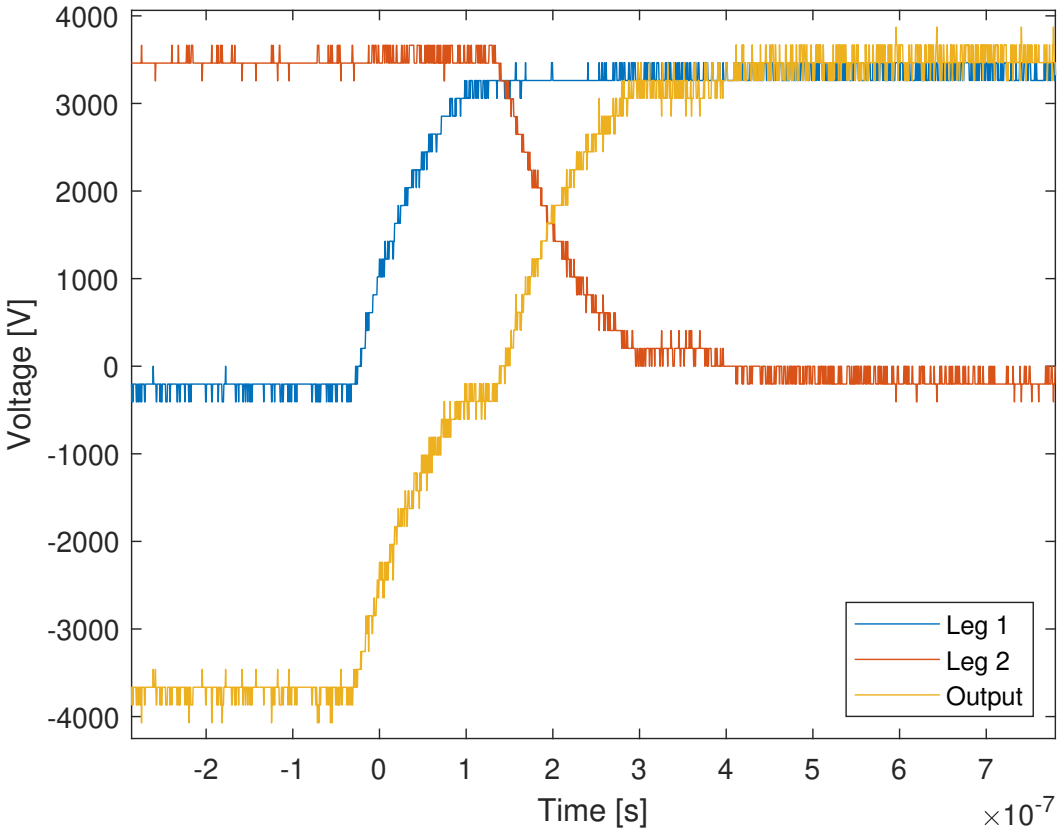


Figure 9.18: 3.5 kV no load test of the submodule. The legs were measured separately using a probe and the output was calculated using the difference.

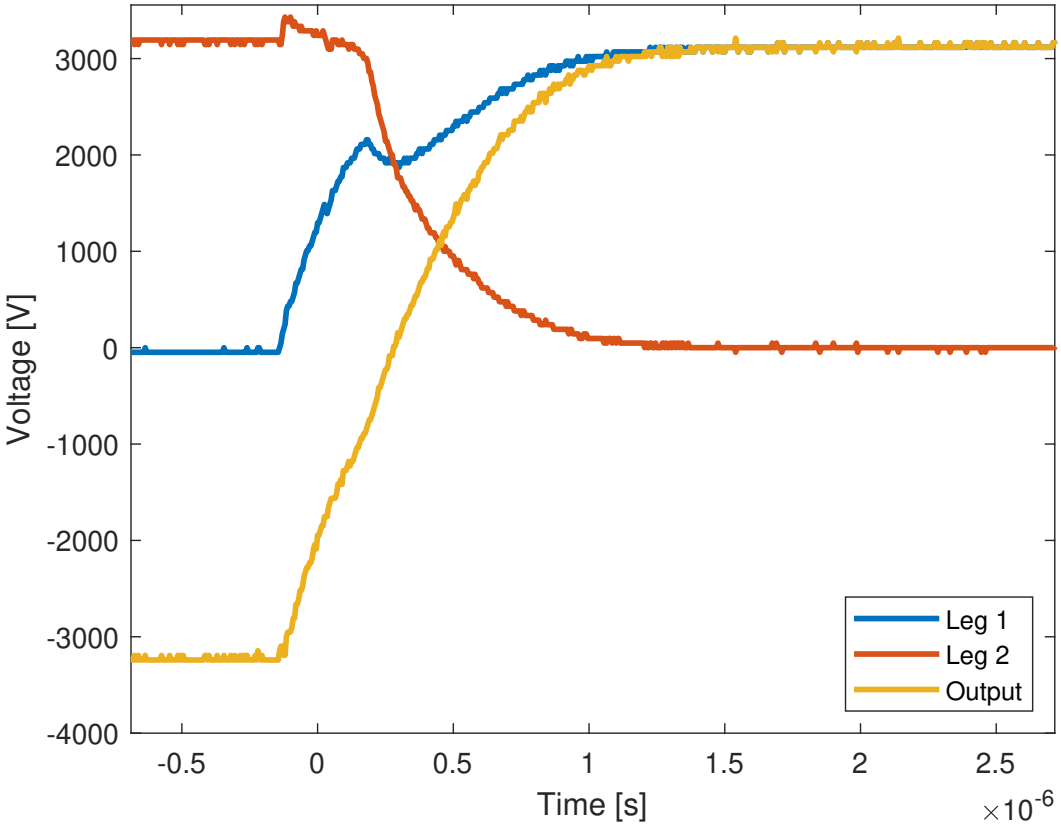


Figure 9.19: Rising transition of 3.5 kV test of the submodule with 500 pF load.

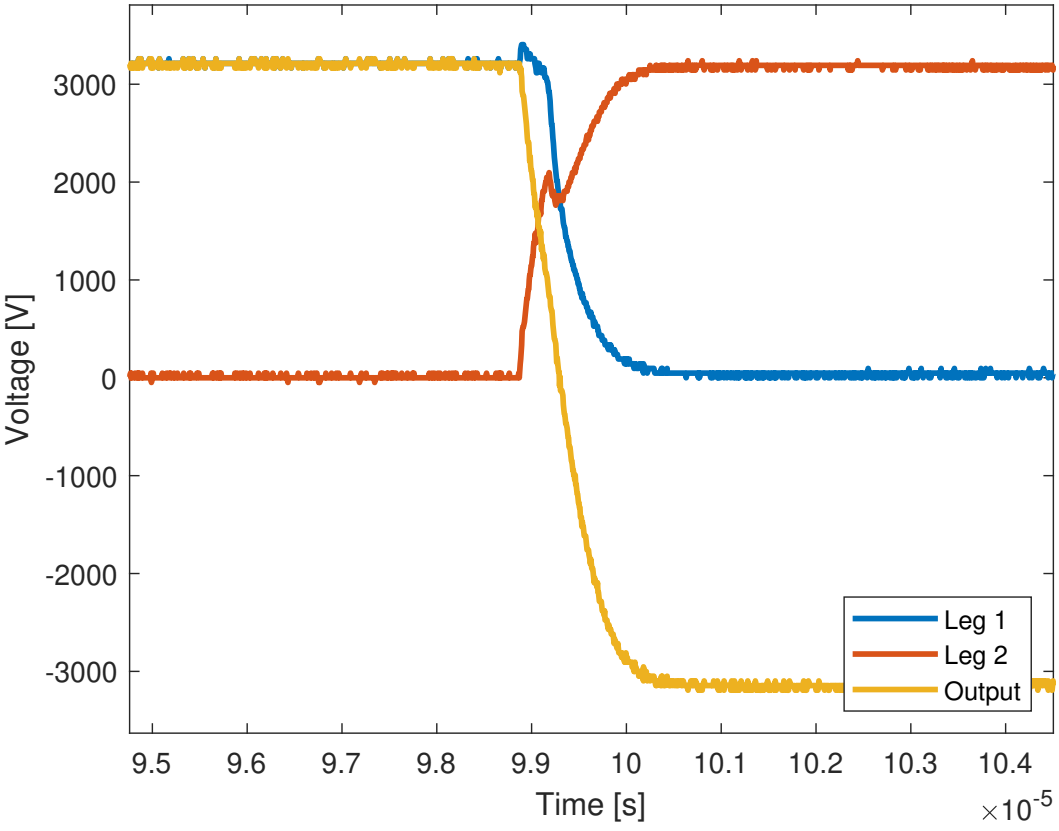


Figure 9.20: Falling transition of 3.5 kV test of the submodule with 500 pF load.

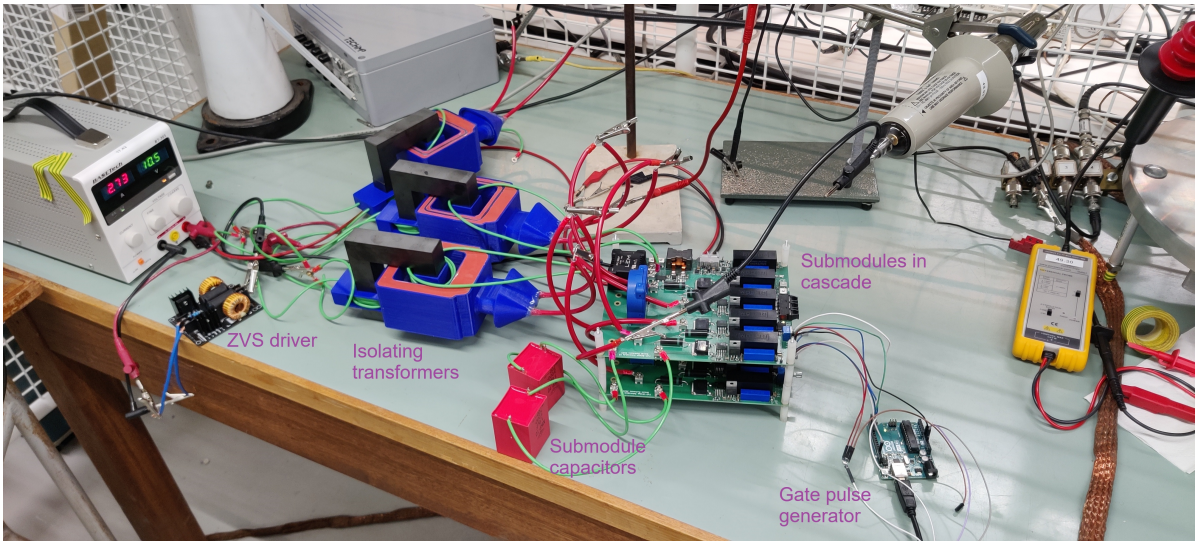


Figure 9.21: Test setup of two submodules in cascaded H-bridge configuration

the capacitive load in Figure 9.19 and 9.20. There is a slight step in the signal, caused by the dead time between the switches and legs. There is also a slight dip in the voltage, which could be caused by an increase in the load current during the transition. This causes a voltage drop over the (relatively high) on-resistance of the MOSFETs and the voltage dips.

During the loaded test, one of the MOSFETs and associated gate driver and isolated power supplies failed. This was likely caused by an overcurrent event of the MOSFET. The IXTT02N450HV can only handle 200 mA continuously, while the test was done using a 500 pF capacitor as the load. The capacitor was driven using a square wave of 4 kV peak-to-peak with a frequency of 10 kHz. The rise and fall time are approximately 500 ns, so the current during this test can be calculated by Equation 9.2.

$$i = C\frac{dV}{dt} = 500 \cdot 10^{-12} \cdot \frac{4 \cdot 10^{3}}{500 \cdot 10^{-9}} = 4A \tag{9.1}$$

$$i_{avg} = \frac{4 \cdot 500 \cdot 10^{-9}}{\frac{1}{10 \cdot 10^{3}}} = 20mA \tag{9.2}$$

While the average current is only 20 mA, the pulsed current is higher than its indicated maximum pulse current of 600 mA [26]. This caused the MOSFET to short circuit, which caused the gate driver and isolated power supply to fail as well. This problem was solved by introducing the correct current limit in the second version of the board, as well as maintaining a proper cooling setup when using higher currents.

The dip in voltage in the loaded test might be caused by the high dv/dt during switching causing a big current through the capacitor and thus a big voltage drop over the on-resistance of the MOSFETs.

9.4.1. Multiple submodules

Multiple submodules were tested together. Two submodules were assembled and tested in cascade. The test setup can be seen in Figure 9.21. A stairstepping signal was made, where one submodule is inserted. The second submodule is inserted after 12 μs. 25 μs after this, the second submodule is bypassed again. This pattern repeats itself again after 12 μs, but now the submodules are inversely inserted to create a negative voltage. The result can be seen in Figure 9.22. As can be seen, it follows the requested output waveform.

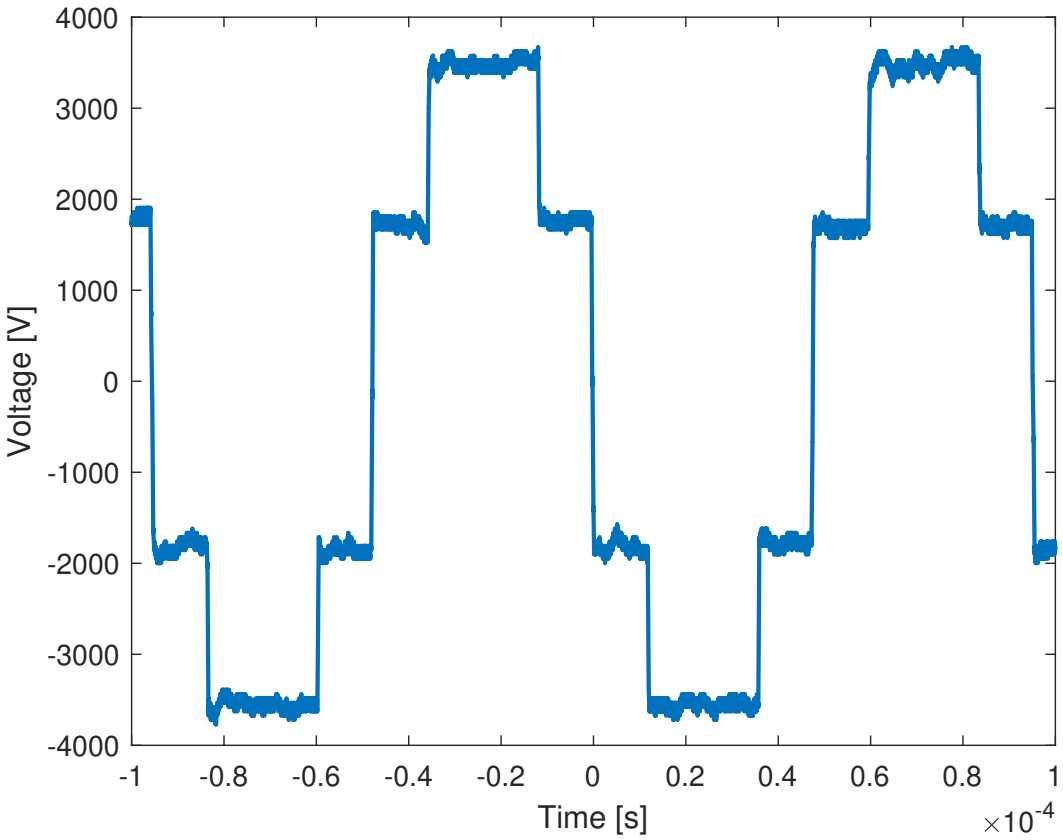


Figure 9.22: Output voltage of two cascaded submodules

10 Conclusion

The objective of this master thesis to investigate the use of series-connected MOSFETs was met. It was discovered that while it is possible to make a high-voltage switch using series-connected capacitively-coupled MOSFETs, it did not fit the requirements for a reliable switch in an MMC submodule. Mainly, the limited on-time caused by the coupling capacitors discharging made it not a good fit. To make an affordable switch using the minimum amount of components for a series connected switch, the capacitive coupling seems to be a good option. The basic configuration with coupling capacitors and balancing resistors can be enhanced using zener diodes and snubber capacitors. A method of equalizing the output capacitance of the MOSFETs was found, by adding a snubber capacitor proportional to the coupling capacitance. These circuits were simulated and behaved like expected, with a short maximum on-time.

The objective of this master thesis to implement a series connected MOSFET in an MMC submodule was not met. The capacitively-coupled series-connected MOSFETs were deemed unsuitable because of the short maximum on-time. A normal MOSFET was used instead as a high-voltage switch. This MOSFET had the downside of having an extremely high on-resistance of 625 Ω.

The objective of this master thesis to implement an MMC submodule was met. A PCB was created, on which the submodule can be controlled. The voltage over the high-voltage DC bus can be measured as well as the current through the module using sensors. These signals are made available as an output over wires, as well as over fiber optic cables. The submodule can be controlled using two input signals to control each leg, and an enable signal to enable or disable the submodule altogether. This was then successfully tested to be working although the current capabilities of the submodule are limited to around 100 mA with the current switches. To create the submodule, firstly a high-voltage full-bridge was designed and tested. During the testing, the OPI1280-066 optocouplers were deemed unsuitable and replaced by the OPI1268S optocouplers for the final design. The HO 6-P current sensor of the first iteration of the submodule design was also swapped. This current sensor had a wider range than was required. When the signal was amplified to accommodate the required range, too much noise was present in the signal. It was replaced by the slower, but more accurate CTSR 0.6-P.

The submodule was succesfully tested in CHB mode, using a custom high-voltage transformer designed by Professor Mohamad Ghaffarian Niasar. This transformer performed like expected and was able to generate the required 4 kV that was needed for each submodule.

10.1. Recommendations

The submodule could be upgraded using higher current capability switches that were not available at the time of the project. The IXTH1N450HV would be a direct replacement. This switch has an on-resistance of 80 Ω, which is a lot lower than the 625 Ω of the IXTH02N450HV that was available during the project. The PCB could also be adapted to accomodate other high-voltage MOSFETs that will become available in the future.

The capacitively-coupled series connected switch could be used in a high-voltage DC-to-DC buck converter to power the submodule from the capacitor in MMC mode. Since the duty cycle for this application would be low, the short on-time capabilities of the switch will not be an issue. This could

be investigated further by implementing the switch in such a converter, with appropriate values for the coupling capacitance.

Other methods of series connected MOSFETs could be investigated to be implemented in an MMC submodule.

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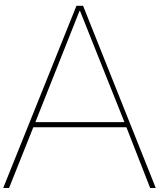

Abbreviations

A.1. List of Abbreviations

Abbreviation	Description
AC	Alternating Current
BJT	Bipolar Junction Transistor
CHB	Cascaded H-Bridge
DC	Direct Current
GaN	Gallium Nitride
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
LTspice	Linear Technology Simulation Program with Integrated Circuit Emphasis
MMC	Multilevel Modular Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PLD	Programmable Logic Device
SiC	Silicon Carbide
USB	Universal Serial Bus

B

Appendix

B.1. Arduino code

B.1.1. Square wave

```
void setup() {
  pinMode(3, OUTPUT); //Copied from Fast PWM Mode with OCRA top: https://docs.arduino.cc/tutorials/generic/secrets-of-arduino-pwm
  pinMode(11, OUTPUT); //Timers are used to make PWM output on pin 3 and 11. Pin 3 has the desired output

  TCCR2A = _BV(COM2A0) | _BV(COM2B1) | _BV(WGM21) | _BV(WGM20); //sets up non-inverted fast PWM with OCRA top
  TCCR2B = _BV(WGM22) | _BV(CS21); //Change CS21 for prescale of 8: https://circuitdigest.com/microcontroller-projects/arduino-timer-tutorial
  OCR2A = 199; //f = 16 MHz / prescale / (OCR2A+1) = 16 MHz / 8 / 200 = 10 kHz
  OCR2B = 1; // D = (OCR2B+1) / (OCR2A+1) = 2 / 200 = 1 % ~ 1 us
}

void loop() {
}
```

B.1.2. Stacked square wave for multiple modules

```
#define NOP __asm__ __volatile__ ("nop\n\t")
#define Ts round(1000/12) //Time step in microseconds (1/12 of freq)
void setup() {
  DDRD = B11111100; //set outputs 2 to 7
  pinMode(12,OUTPUT); //Enable signal
  delay(15000); //Delay to enable turn on in ms (enable on pin 12)
  noInterrupts();
}

void loop() { //12 steps for triangle wave
  digitalWrite(12,HIGH); //Enable signal high (enabled)
  while(true){
  PORTD = B00000000; //First step off
  NOP; //loop compensation
  NOP;
  NOP;
```

```
17    delayMicroseconds(Ts); //2
18    PORTD = B10000000;
19    delayMicroseconds(Ts); //3
20    PORTD = B11000000;
21    delayMicroseconds(Ts); //4
22    PORTD = B11100000;
23    delayMicroseconds(Ts); //5
24    PORTD = B01100000;
25    delayMicroseconds(Ts); //6
26    PORTD = B00100000;
27    delayMicroseconds(Ts); //7
28    PORTD = B00000000;
29    delayMicroseconds(Ts); //8
30    PORTD = B00010000;
31    delayMicroseconds(Ts); //9
32    PORTD = B00011000;
33    delayMicroseconds(Ts); //10
34    PORTD = B00011100;
35    delayMicroseconds(Ts); //11
36    PORTD = B00001100;
37    delayMicroseconds(Ts); //12
38    PORTD = B00000100;
39    delayMicroseconds(Ts);
40    }
41 }
```

B.2. Programmable logic device

B.2.1. Version 1

This version only turns off during a fault, afterwards it will immediately start again:

```
1  Name     input_control_LED ;
2  PartNo   00 ;
3  Date     2-8-2023 ;
4  Revision 01 ;
5  Designer Engineer ;
6  Company  ;
7  Assembly None ;
8  Location ;
9  Device   G16V8A;
10
11 /* *************** INPUT PINS *********************/
12 PIN   4  =   IN1                    ; /*
                                        */
13 PIN   5  =   IN2                    ; /*
                                        */
14 PIN   6  =   IN1D                   ; /*
                                        */
15 PIN   7  =   IN2D                   ; /*
                                        */
16 PIN   8  =   ENA                    ; /*
                                        */
17 PIN   9  =   OVOC                   ; /*
                                        */
18
19 /* *************** OUTPUT PINS *********************/
```

```
20 PIN    12   =    LED                          ; /*
                                                 */
21 PIN    18   =    H1                           ; /*
                                                 */
22 PIN    17   =    L1                           ; /*
                                                 */
23 PIN    16   =    L2                           ; /*
                                                 */
24 PIN    15   =    H2                           ; /*
                                                 */
25
26 /* *************** EQUATIONS ***********************/
27 H1 = IN1 & IN1D & ENA & !OVOC;
28 L1 = !(IN1 # IN1D) & ENA & !OVOC;
29 H2 = IN2 & IN2D & ENA & !OVOC;
30 L2 = !(IN2 # IN2D) & ENA & !OVOC;
31 LED = ENA & !OVOC;
```

B.2.2. Version 2

This version will have to be re-enabled after a fault before it works again:

```
1  Name     qn ;
2  PartNo   00 ;
3  Date     22-8-2023 ;
4  Revision 01 ;
5  Designer Engineer ;
6  Company  HP Inc. ;
7  Assembly None ;
8  Location  ;
9  Device   g16v8a ;
10
11
12 /* *************** INPUT PINS *********************/
13 PIN    4   =    IN1                          ; /*
                                                 */
14 PIN    5   =    IN2                          ; /*
                                                 */
15 PIN    6   =    IN1D                         ; /*
                                                 */
16 PIN    7   =    IN2D                         ; /*
                                                 */
17 PIN    8   =    ENA                          ; /*
                                                 */
18 PIN    9   =    OVOC                         ; /*
                                                 */
19
20 /* *************** OUTPUT PINS ********************/
21 PIN    12   =   LED                          ; /*
                                                 */
22 PIN    15   =   H2                           ; /*
                                                 */
23 PIN    16   =   L2                           ; /*
                                                 */
24 PIN    17   =   L1                           ; /*
                                                 */
25 PIN    18   =   H1                           ; /*
```

```
                                                    */
26 PIN     14   =     Q                               ;
27 PIN     13   =     QN                                          ;
28
29 /* EQUATIONS */
30
31 H1 = IN1 & IN1D & ENA & QN;
32 L1 = !(IN1 # IN1D) & ENA & QN;
33 H2 = IN2 & IN2D & ENA & QN;
34 L2 = !(IN2 # IN2D) & ENA & QN;
35 LED = ENA & QN;
36 Q = !(!ENA # QN);
37 QN = !(OVOC # Q);
```