IEEE Journal of Microwaves

Received 28 July 2025; revised 30 October 2025; accepted 3 November 2025. Date of publication 24 November 2025; date of current version 8 January 2026.

Digital Object Identifier 10.1109/JMW.2025.3631321

Reduction of Power Consumption in Hybrid Beamforming Integrated Circuits Using Amplitude Taper Grouping

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(Regular Paper)

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This work was supported by the National Growth Fund through the Dutch 6G flagship project "Future Network Services."

ABSTRACT A novel system design framework is proposed for hybrid beamforming receivers to reduce the power consumption withoutany loss in sensitivity or beam scanning performance. Only the amplitude taper that corresponds to the relative individual analog subarrays is applied in the analog beamforming domain, while the rest of the taper is applied using digital beamformingcoefficients. Based on a given array size, number of beams, and the desired sidelobe suppression level, the number of analog subarrays and the beamforming integrated circuit (BFIC) component characteristics are optimally selected. An improved BFIC module is recommended that has less analog pre-amplification and a smaller dynamic range of variable attenuator steps. For concept demonstration, a benchmark analog beamforming and hybrid beamforming SatCom architecture, without this improvement, are simulated using a joint signal and power consumption analysis. For a 32 × 32 element array with 2 simultaneous beams and 30 dB side lobe tapering, the analog benchmark and hybrid benchmark (with 64 subarrays) are simulated to have a power consumption of 50.1 W and 66.5 W, respectively, A similar hybrid beamforming architecture with modified BFIC modules is shown to have a total power consumption of 40.3 W, less than both benchmarks. Furthermore, a comprehensive analysis of the system is conducted to illustrate how power consumption is influenced by the chosen number of subarrays with respect to the targeted sidelobe suppression, array size, number of beams and number of ADC bits.

INDEX TERMS Amplitude tapering, beamforming integrated circuit, power consumption model, RF receiver architecture design, satellite communications, system design.

I. INTRODUCTION

Within radio frequency (RF) receiver system design, different phased array beamforming configurations are possible. Analog beamforming (ABF), which is typically seen as the most low-cost and the most energy efficient, is also the least flexible in terms of beamforming capabilities [1]. Element-level beamforming in an ABF system is usually achieved using phase shifters, variable attenuators, or vector modulators. Examples of ABF phased array architectures are given in [2], [3]. It is also possible to create clustered analog subarrays without any element-level scanning capabilities, e.g. [4], but this severely limits beam scanning capabilities. Full digital beamforming (DBF) digitizes the signal obtained by every antenna element, and performs the beamforming in the digital domain [5]. DBF systems require a separate conversion stage for every antenna element, and are therefore very costly and power-hungry. DBF systems are very flexible in terms of the number of beams and in terms of beam shaping. An example of a DBF phased array architecture is given in [6], and more examples are given in [5]. Hybrid beamforming (HBF) systems do one part of the beamforming in the analog domain and another part in the digital domain. Their performance is typically seen as a

trade-off between ABF and DBF performance, both in terms of cost and power consumption [7], [8], [9], [10]. In [11], an extensive overview of the advantages and disadvantages of ABF, DBF and HBF architectures is provided for the interested readers.

Optimal design of the beamformer for a particular application can be done in different ways. In some studies, the beamforming configuration is optimized in terms of power consumption [1], [12], [13]. In other studies, a signal-based optimization of the architecture in terms of analog- and digital beamforming weights is performed [14], [15]. Typically, for a low number of beams, the ABF configuration is deemed the most power efficient.

Analog-, hybrid-, and digital beamforming networks are used in various applications in communication and sensing, for example weather radar or 5G/6G base stations. Another important application, which is selected as the focus of this paper, is Satellite Communication (SatCom). In future communication networks, the non-terrestrial network (NTN), using satellites, will be a valuable enhancement to the terrestrial network (TN) [16]. SatCom has several advantages with respect to ground-based communications, such as coverage in remote areas where it is too expensive to set up a TN, or SatCom can provide connectivity for systems-on-the-move (SOTM) [17], [18]. SatCom can provide an additional flexible communication layer in areas that are not densely populated, to alleviate the requirements on the TN, and SatCom can serve as a back-up in areas where the TN breaks down, for example due to a natural disaster. The integration of NTN and TN is expected to increase in future network services, such as 6G [19].

Traditionally, SatCom uses geostationary (GEO) satellites [20]. These satellites are in a fixed position in the sky, with respect to the earth surface, which ensures that GEO SatCom terminals do not need any beam steering capabilities. GEO systems are particularly well suited for broadcasting the same information to a large number of users. A more recent trend is to move towards low-earth orbit (LEO), or very low-earth orbit (VLEO) SatCom systems [20], [21]. LEO satellites have a much smaller orbit altitude, which means that latency and propagation losses are reduced. However, this also means that LEO satellites move at a high velocity through the sky, and therefore LEO SatCom terminals require beam-steering capabilities. Furthermore, it is desirable for SatCom terminals to connect to the next satellite, before breaking the connection to the current satellite (make-before-break), which requires multi-beam support [22]. LEO and VLEO systems are particularly well suited for two-way user-specific communication.

Electronic phased array systems are well suited to meet the requirements for LEO communication terminals [11], [23], [24]. Phased arrays provide independent control of the amplitude and phase excitation of the antenna elements, but many electronic components, such as phase shifters, attenuators, and amplifiers, are required to achieve this. The SatCom frequency bands that are assumed in this work are centered around 20 GHz (downlink) and 30 GHz (uplink) [25], but other frequency bands such as the X- and Ku-bands are used for SatCom purposes as well [26]. To achieve large scan angles with no grating lobes, a half-wavelength array spacing is generally required, which means that antenna elements are spaced close together and very little room is available for the placement of the required components. In recent years this problem has been solved by the development of the beamforming integrated circuit (BFIC) [2], [3], [25], [26], [27], [28], [29]. These chips, implemented in IC technology, usually connect to a number of antenna channels (e.g. 8 or 16), and provide amplification and taper control. It is possible for these BFICs to be designed with multi-beam support, and to synthesize for example 2 or 4 beams, see e.g. [2], [26], or see existing commercial of-the-shelf (COTS), e.g. Renesas F6122 or Analog Devices ADAR3000.

When a SatCom terminal is designed with such a small number of beams, often an ABF system configuration is selected, since this is deemed to be the most cost-effective and power-efficient solution. Typical BFIC design reflects this approach [2], since all channels are designed to have a large range of amplitude control. A beam taper can be applied across the entire phased array, using only the BFIC amplitude control, and without the support of any digital weights. When applying a taper across the array, the taper inefficiency will reduce the receiver sensitivity, but tapering might still be necessary to reduce the sidelobes or perform nulling, such that the signal-to-interference-plus-noise ratio (SINR) in the presence of interference is acceptable.

This paper proposes a novel BFIC design guideline for hybrid beamforming, to minimize the system power consumption, without any degradation in signal performance or beamsteering capability. Furthermore, to the best of our knowledge, this is the first study that systematically explores system-level trade-offs by analyzing the power consumption dependency on side-lobe level (SLL), array size, number of beams, ADC resolution, and subarray size. These aspects extend beyond prior art and provide new insights for practical system design. The main contributions of this paper may be summarized as follows:

1) A joint signal- and power consumption analysis is performed to show how in a HBF architecture, system power consumption may be reduced by using the digital capabilities to alleviate requirements on the analog taper control, and on the required analog pre-amplification.
2) Based on this method, a design recommendation is made for a BFIC for SatCom applications that has reduced analog pre-amplification, and reduced dynamic range of the variable attenuation.
3) The dependency of HBF system power consumption on the desired sidelobe suppression level and subarray size is analyzed.

It will be shown that when following the proposed design flow, the power consumption of a HBF system can be lower than for the ABF case, even for a small number of beams.

The rest of the paper is structured as follows. In Section II, a system definition will be given of a parametrized

HBF receiver, using BFIC subsystems. In this system definition, the size of the analog subarray is parametrized, such that a comparison can be made between the ABF and HBF system architectures. All the assumed component properties will be provided, along with corresponding sources from the literature. In Section III, a detailed analysis of the signal levels, noise levels and SNR degradation across all component stages will be provided, for both the ABF and HBF architecture. These figures will clearly show the design opportunities that arise when using the HBF architecture. Furthermore, this section will explain the concept of amplitude taper grouping, and how this concept may be exploited to reduce system power consumption. Section IV shows a comparison between the ABF architecture, HBF architecture without amplitude taper grouping, and the HBF architecture with amplitude taper grouping. Section V performs a more generic analysis of the relationship and trade-offs between the optimal subarray size, and the sidelobe suppression level, array size, number of beams, and number of ADC bits. Section VI discusses the applicability of amplitude taper grouping to different component configurations. Section VII concludes the paper, and discusses directions for future work.

II. SYSTEM DEFINITION

In this section, a parametrized front-end system model for a hybrid beamforming SatCom receiver will be defined, that makes use of multi-channel multi-beam BFIC modules. The number of analog subarrays in this system definition is a parameter, which means that the extent to which beamforming is performed in the analog- or digital domain can be varied. The system is assumed to have a center frequency of f_c = 19GHz, within the commercial K-band (17.7–20.2GHz), and the instantaneous bandwidth (BW) is assumed to be 1GHz, see e.g. [30]. In this work, only a single polarization is taken into account, but the same analysis can be easily extended to dual polarization. The system definition will be given in three parts: First, the definition of the BFIC module will be given. Second, the definition of the analog subarray is given. Third, the full parametrized HBF receiver is defined.

A. DEFINITION OF THE BFIC MODULE

The definition of the BFIC module is mostly based on [2]. The SatCom BFIC configuration (Fig. 1(a)) supports two simultaneous beams, to facilitate make-before-break between satellites. It can be seen that the BFIC has several input channels, in this case $N_c = 8$. Every channel is amplified using an amplifier, and then every channel is split into two paths using a 1-to-2 Wilkinson divider, one for every beam. For each of these paths, a variable phase shifter and variable attenuator, both of which have a limited resolution, are used to be able to introduce a beam taper. Per beam, all 8 channels are combined using an 8-to-1 Wilkinson combiner, such that the total BFIC has 2 beam outputs.

All component properties, such as gain, insertion loss and power consumption, for all the components in the BFIC, are shown in Table 1. Different sources from the literature were used to obtain these values, which are also shown.

TABLE 1. Component Properties BFIC

Component	Properties	Source
Amp	Amplifier. G_{amp} = 22.4 dB, NF_{amp} = 5.6 dB. G_{amp} will be varied, and P_{amp} is determined as $G_{\text{amp}}\Delta P_{\text{amp}}$, where ΔP_{amp} = 1.5 mW/dB.	[1], [2]
wilk_div	On-chip 1-to-2 Wilkinson divider. $L_{\text{wilk\_div\_base}}$ = 0.65 dB.	[31]
PS	Variable phase shifter. $N_{\text{bits\_ps}} = 6$, $L_{\text{ps\_bit}}$ = 1 dB/bit. $L_{\text{ps}} = N_{\text{bits\_ps}} L_{\text{ps\_bit}} = 6$ dB.	[2], [32]
ATT	Variable attenuator. $N_{\text{bits\_att}} = 6$, att_min = 0 dB, att_max = 31.5 dB, step size = 0.5 dB. L_{att} = attenuation setting.	[2]
wilk_comb_1	On-chip 8-to-1 Wilkinson combiner. $L_{\text{wilk\_comb\_1}} = log_2(8) * 0.65 = 1.95$ dB.	[31]
routing_1	$L_{\text{rout\_1}}$/d = 0.5 dB/cm, where d is calculated according to (1), with $d_x = d_y = 0.5\lambda$, $N_x = 4$, and $N_y = 2$ [a].	[1]

[a]The routing on BFIC level occurs in part off-chip and in part on-chip. These routing losses are based on off-chip technology, and additional on-chip losses are included in the other components, e.g. the Wilkinson combiners / dividers.

In this table, G is the component gain, NF is the component noise figure, P is the DC power consumption, N_{bits} is the number of bits available for digital control, L is the insertion loss, and λ is the wavelength. For the amplifier, the gain may be varied, and the DC power consumption is then assumed to vary with 1.5mW per dB gain variation, as indicated by ΔP_{amp}. This is not an operational variation, but is fixed via component selection. This property will be used in Section III.

The routing losses that are required to bridge the space between different elements, are also taken into account in Table 1. These routing losses are estimated by multiplying the distance that is traversed in the combining network, with the loss per distance. The routing network is assumed to be an H-tree combining network (Fig. 2), which has an equal path length traversed to every element. This path length is calculated using the following equation:

$$d = (d_x/2)\,(N_x - 1) + \left(d_y/2\right)(N_y - 1) \tag{1}$$

where d_x and d_y are the horizontal spacing and the vertical spacing between elements, respectively. N_x is the number of horizontal elements that are combined, and N_y is the number of vertical elements that are combined.

B. DEFINITION OF THE ANALOG SUBARRAY

The analog subarray (Fig. 1(b)) is a group of analog components connected to two digital conversion chains, one per beam. Every patch antenna element is connected to a low

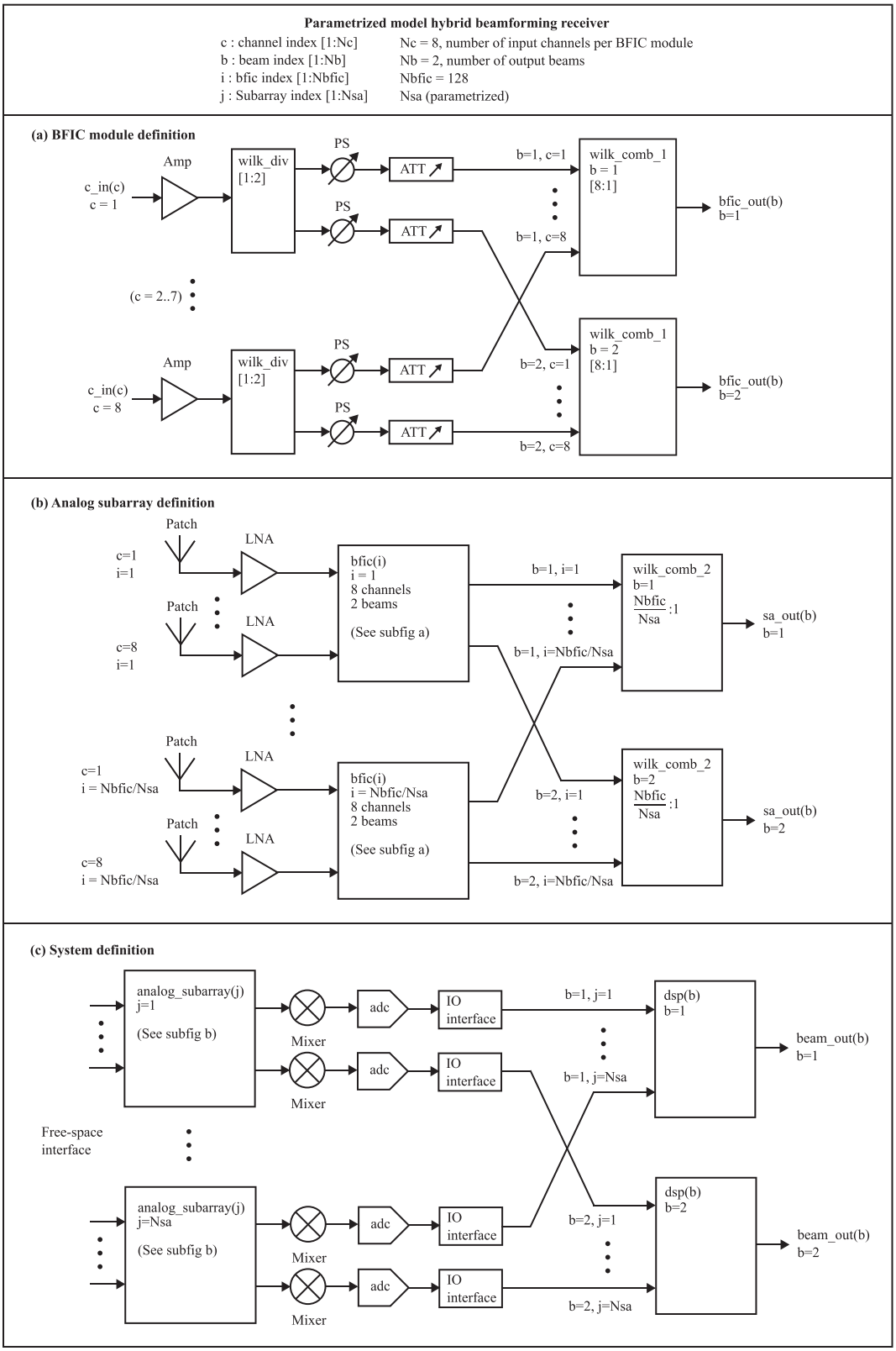

FIGURE 1. System definition of the parametrized hybrid beamforming receiver. The number of subarrays N_{sa} is parametrized, such that the extent to which beamforming is performed in the digital domain can be varied. Fig. 1(a) shows the definition of the BFIC module. Fig. 1(b) shows the definition of the analog subarray. Fig. 1(c) shows the definition of the full system.

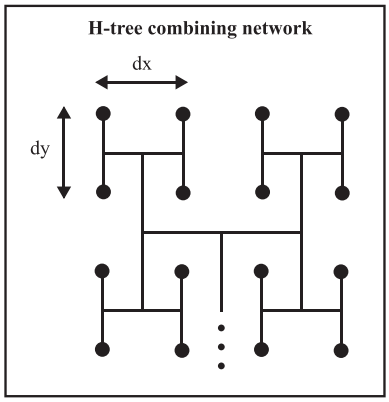

FIGURE 2. Lay-out of an H-tree combining network. For larger arrays this structure is repeated.

TABLE 2. Component Properties Analog Subarray

Component	Properties	Source
Patch	Directivity = 6 dBi, Total efficiency η = 0.9.	Typical
LNA	Low noise amplifier. G_{lna} = 19 dB, NF_{lna} = 1.45 dB, P_{lna} = 15 mW	[2]
BFIC	Beamforming integrated circuit, see Table 1.	[2]
wilk_comb_2	$N_{\mathrm{bfic}}/N_{\mathrm{sa}}$-to-1 Wilkinson combiner. L depends on selection of N_{sa} : $L_{\mathrm{wilk\_comb\_2}} = log_2(N_{\mathrm{bfic}}/N_{\mathrm{sa}}) * 0.4$ dB. Derived from CPW technology.	[33]
routing_2	$L_{\mathrm{rout\_2}}$/d = 0.5 dB/cm, where d is calculated according to (1), with $d_x = 2\lambda, d_y = \lambda$, $N_x = N_{\mathrm{bfic,sa,x}}$, and $N_y = N_{\mathrm{bfic,sa,y}}$. Derived from CPW technology.	[1]

noise amplifier (LNA), to improve system sensitivity. Groups of 8 antenna channels are then connected to a BFIC, which has 2 outputs, 1 per beam. Groups of BFIC outputs are then combined using Wilkinson combiners. The size of this Wilkinson combiner is equal to the number of BFIC modules per subarray $N_{\mathrm{bfic}}/N_{\mathrm{sa}}$, where N_{bfic} is the number of BFIC modules in the entire system, which is set to 128 (=1024/8), and N_{sa} is the total number of subarrays. The case $N_{\mathrm{sa}} = 1$ corresponds to the ABF architecture, and the case $N_{\mathrm{sa}} > 1$ corresponds to a HBF architecture. Table 2 gives the properties of components in the analog subarray.

The insertion losses of the Wilkinson combiner vary, depending on the number of combiner stages that are required, which depends on N_{sa}. Again, routing losses are taken into account, where the spacing is now based on the spacing between BFIC-modules. Here, $N_{\mathrm{bfic,sa,x}}$ is the number of BFIC modules per subarray in the horizontal direction, and $N_{\mathrm{bfic,sa,y}}$ is the number of BFIC modules per subarray in the vertical direction. More details on the array lay-out will be given in Section III.

TABLE 3. Component Properties Parametrized SatCom HBF Receiver

Component	Properties	Source
Analog subarray	Properties given in Table 2.	
Mixer	P_{mixer} = 40 mW. Only power consumption modeled for now.	[1]
ADC	Analog-to-digital converter. $N_{\mathrm{bits\_adc}}$ = 8, FOM_{W} = 20 fJ/conv-step, P_{adc} = 2.6 mW (x2 for complex), f_{s} = 1 GHz.	[1], [34]
IO interface	High-speed input-output interface. P_{io} = 10 mW / Gbps.	[1]
DSP	Digital signal processor. P_{dsp} = 1.25 mW / GMAC (x4 for complex)	[1]

C. DEFINITION OF THE HBF RECEIVER

The full HBF receiver (Fig. 1(c)) is a two-dimensional array with 1024 patch antenna elements, in a 32 × 32 configuration, see e.g. [3]. The output of every analog subarray, for both beams, is converted to baseband using a mixer, and digitized using an ADC. To transfer the data from the ADC to the digital processor, an IO interface, i.e. Serializer-Deserializer (SerDes) interface is used. This interface is used to get the high-speed ADC data to the digital processor. The DSP performs the digital part of the beamforming. For the case $N_{\mathrm{sa}} = 1$, the ABF case, the digital processor does nothing. Detailed component properties for the parametrized HBF SatCom receiver are given in Table 3. The HBF system has at least the same capabilities as the analog system in terms of beamforming and scanning. Furthermore, although this is out of the scope of this paper, the HBF system has the freedom to perform additional digital processing per subarray, for example to create additional beams or to perform spectrum equalization.

FOM_{W} is the Walden figure-of-merit for the ADC. This number is not directly used in this paper, but gives an indication of the ADC quality. More information on the FOM_{W} will be given in Section V. Both the real and imaginary parts of the signal need to be sampled, and the ADC power consumption is doubled to take this into account. Any additional circuitry required to do this is ignored in this analysis. f_{s} is the ADC sampling rate. The DSP has a power consumption expressed in mW / GMAC, which stands for mW / Giga multiply-and-accumulate, or the power required for a multiply and sum operation. The actual power consumption is multiplied by a factor 4 to take into account complex numbers.

The variable phase shifters, variable attenuators and DSP in this system are able to apply a beam taper, which may be used to suppress interferers at directions that are not in the main lobe of the beam pattern.

III. SIMULATION OF SIGNAL AND NOISE POWERS

In this section the system that was defined in Section II will be simulated for two different benchmark cases. In the first case, the number of subarrays N_{sa} is set to 1. This means that

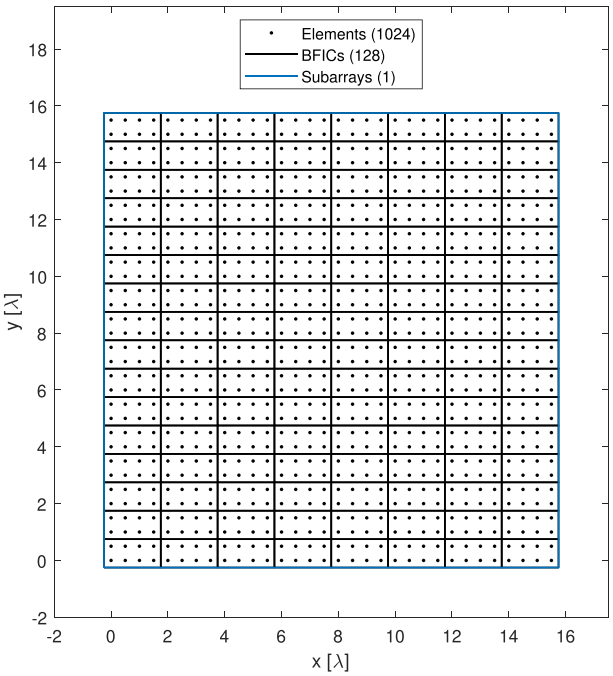

FIGURE 3. Array configuration for the case $N_{sa} = 1$. The black dots indicate the center positions of the antenna elements. The black lines indicate the BFIC mapping and the blue lines indicate the subarray mapping.

all beamforming is done in the analog domain. In the second case N_{sa} will be set to 64, so there are 64 subarrays, each of which have separate conversion stages that digitize the signal. This number of subarrays is an initial value, in Section IV the dependency on number of subarrays will be analyzed in more detail.

A. ANALOG BEAMFORMING BENCHMARK ($N_{SA} = 1$)

In the first case N_{sa} is set to 1. The array configuration that corresponds to this case is shown in Fig. 3. The black dots indicate the center positions of the antenna elements. The solid black lines indicate which elements map on a single BFIC module. The solid blue lines indicate which elements map on a single subarray. Since in this case $N_{sa} = 1$, there is only one subarray to which all elements are connected.

An overview of the simulated signal levels (red lines) and the noise levels (blue lines) at all component stages is shown in Fig. 4(a). Both the minimum and maximum levels are shown to indicate the differences between the elements due to the taper that is applied. The yellow dashed line corresponds to the system noise floor of −174.0 dBm/Hz, which is the noise spectral density at a temperature of 290 K.

The electromagnetic waves impinging upon the antenna system - both one carrying signal from a satellite and others bringing environmental electromagnetic noise - are assumed to have a signal-to-noise ratio of −10 dB, which is deemed to be a typical value for LEO SatCom applications [35]. The element-level SNR in the LEO link budget is low, even smaller than 0 dB, due to typical satellite effective isotropic radiated power (EIRP) and the path losses. The receive antenna gain is required to extract the signal from the noise floor. The effect of components on the signal can be matched with the respective component properties in Tables 1, 2, and 3. The directivity of the patch is set to 6 dBi, and the total efficiency $\eta = 0.9$, for a realized gain of 5.54 dBi. After the patch, the LNA is used to boost the signal by 19 dB, such that contributions of thermal noise in later stages have a smaller impact. After the LNA, the signals enter the BFIC modules. The BFIC module contains an additional amplifier that further boosts the signal, with respect to the noise floor. This amplifier does not require an extremely good noise figure, since it is placed after the LNA. Next, a 1-to-2 Wilkinson divider splits every channel into two channels, one for each beam. This means a 3 dB power reduction for both paths, in addition to the insertion losses of this Wilkinson divider.

After this, for every path in the BFIC, variable phase shifters and variable attenuators are used to apply the desired beam taper. The beam taper that is applied in this paper, for initial demonstration of the proposed concept, is a 30 dB sidelobe level (SLL) Taylor taper, but the same principles hold for other beam tapers. The dependency on the required level of sidelobe suppression will be studied in Section IV. The phase shifters and attenuators bring significant insertion losses. Phase shifter design often has a large insertion loss per bit [32], in this case selected to be 1 dB per bit. Variable attenuators inherently have large insertion losses, since that is their main function. For the case of a 30 dB SLL Taylor taper in a 32 × 32 array, the variable attenuators need to cover a dynamic range of 24.4 dB. The large insertion losses that are required to apply a beam taper in an analog beamforming system also explain why the large amplification of the LNA and BFIC amplifier were required. Without these the received signal would not stay above the noise floor. Although not further discussed in this paper, this large amplification also comes with significant requirements on the 1 dB compression point of the amplifiers.

Next, for the analog beamforming case, all signals for a beam are combined using two stages of Wilkinson combiners, which means that the SNR levels increase due to the beamforming gain. The routing losses and Wilkinson combiners are shown as a single stage, since in reality the routing losses and the different combiner stages are intertwined. Finally, an ADC is used to digitize the signal for every beam. In the ABF case, the DSP has no function.

Fig. 4(b) shows the total SNR degradation at all component stages. Both the cumulative SNR degradation and the contribution of individual component stages are shown. An ideal receiver would coherently integrate all energy that is incident upon the receiver, and the SNR degradation graph shows to what extent the designed receiver deviates from this ideal receiver. The efficiency of the patch is also shown as SNR degradation, since it directly affects the sensitivity of the receiver. It can be seen that the patch antenna losses (0.46 dB for $\eta = 0.9$) and the LNA noise figure (1.45 dB) together

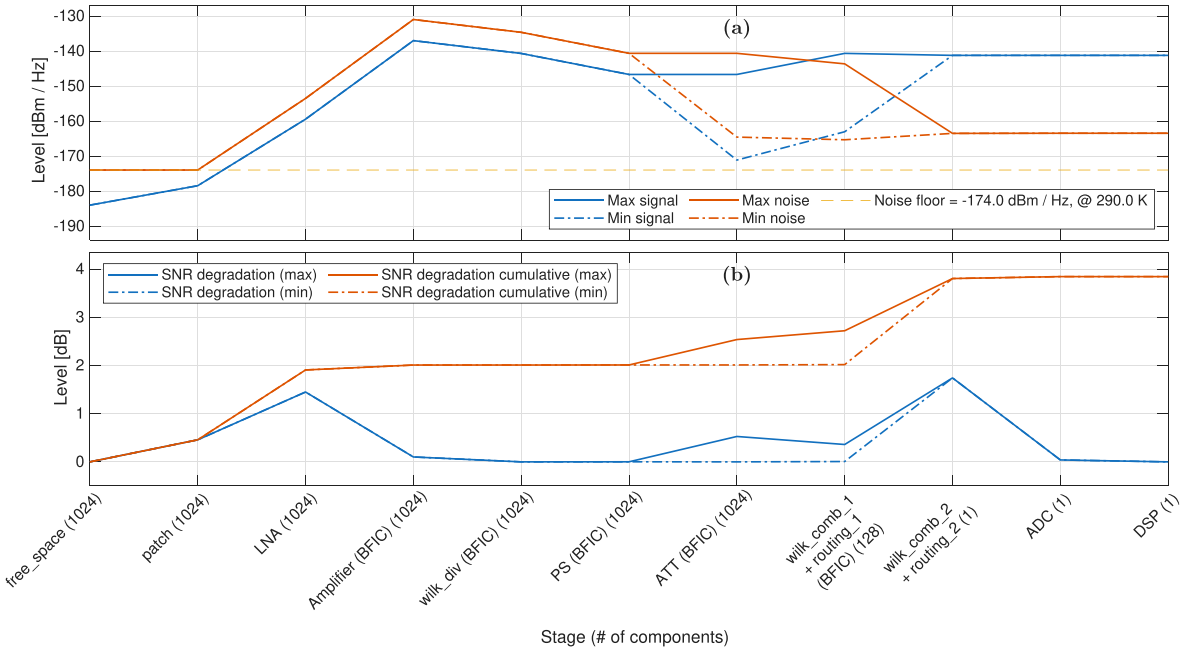

FIGURE 4. Simulation results for the analog beamforming benchmark ($N_{sa} = 1$). (a) Signal levels (blue) and noise levels (red) at all component stages. The yellow dashed line indicates the noise floor. (b) SNR degradation at all component stages. Both the cumulative SNR degradation (red) and the individual component contributions (blue) are shown.

cause 1.9 dB SNR degradation, due to their noise contributions. The rest of the SNR degradation is mostly caused by the inefficiency of the beam taper, which for a Taylor 30 dB SLL taper is 1.38 dB.

B. HYBRID BEAMFORMING BENCHMARK ($N_{SA} = 64$)

Next, the same simulation is performed for the hybrid beamforming case, where N_{sa} is set to 64. The array configuration for this case is shown in Fig. 5. It can be seen that the configuration of the antenna elements and BFIC modules is the same as for the analog case (Fig. 3), but there are now more subarrays. Every subarray connects to 2 BFIC modules, or 16 elements.

The simulation results for the hybrid configuration are given in Fig. 6. It can be seen that the number of digital conversion stages is of course much larger than for the analog beamforming case, as is indicated by the number in the labels on the horizontal axis. For the hybrid beamforming case, a part of the beamforming is done in the digital domain. For this reason, it can be seen that a part of the beamforming gain is obtained in the DSP. Because of this, the required ADC dynamic range seems to be smaller. However as is also indicated in [1], the interference suppression in the analog domain is also less, such that stronger interferers may appear at the ADC input. For this reason, the ADC resolution is not changed for the hybrid beamforming case.

Most importantly, it can be seen (Fig. 6) that the insertion losses for the variable attenuators are now much smaller. The reason for this is that a part of the amplitude tapering is now moved to the digital domain. The power levels of signal and noise are now much higher than the noise floor, as compared to the analog beamforming benchmark (Fig. 4). This is the key observation that will be exploited to design a customized BFIC module, intended for hybrid beamforming SatCom systems. This will be explained in more detail in the next section.

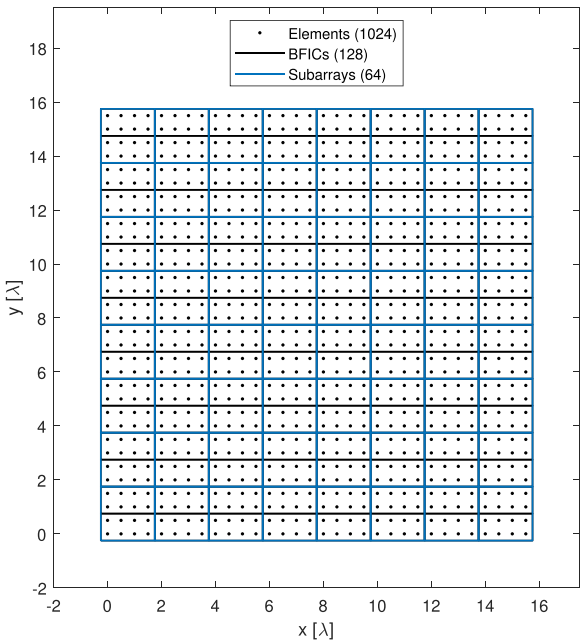

FIGURE 5. Array configuration for the case $N_{sa} = 64$.

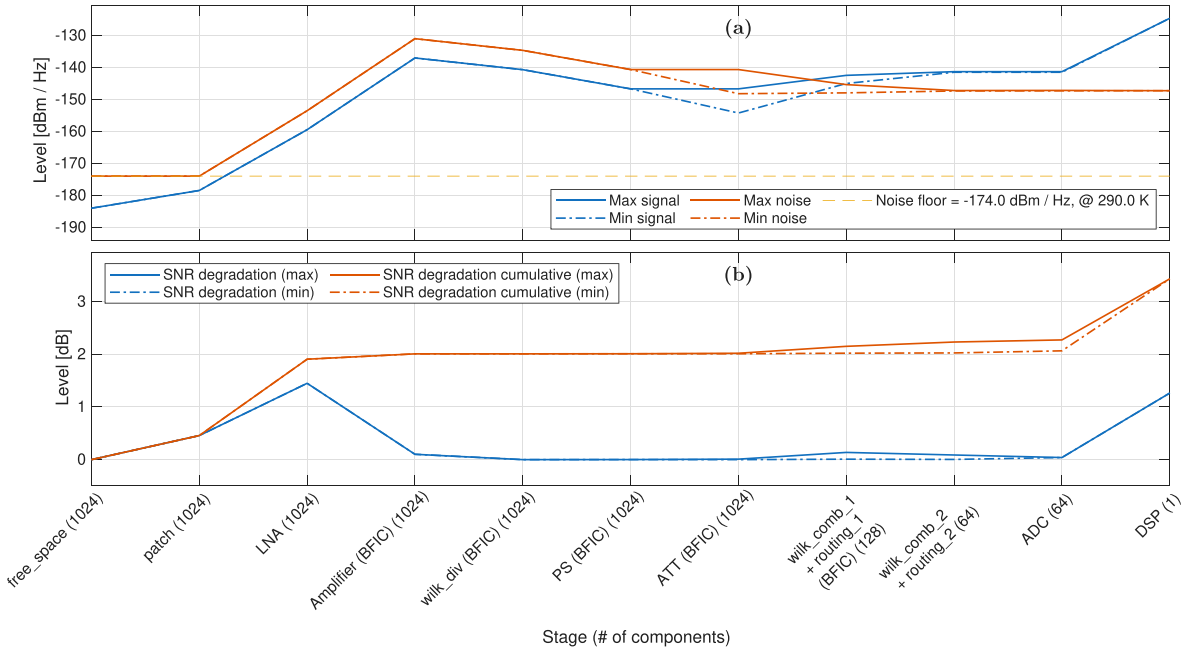

FIGURE 6. Simulation results for the hybrid beamforming benchmark ($N_{sa} = 64$). (a) Signal- and noise levels. (b) SNR degradation. Part of the amplitude taper is now performed in the digital domain, which means that there is an increased separation between signal power levels and the noise floor.

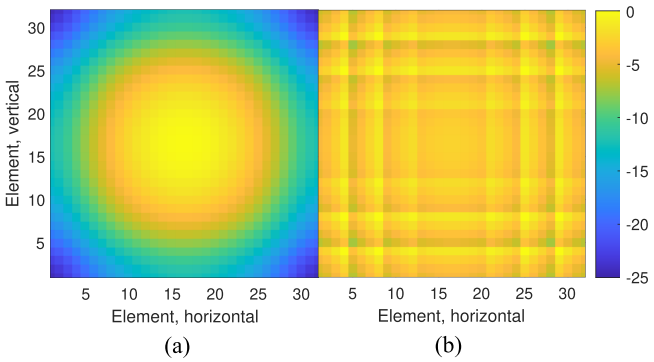

FIGURE 7. Required attenuator setting to apply the Taylor 30 dB taper. (a) shows the analog beamforming case. The required dynamic range here is 24.4 dB. (b) shows the hybrid beamforming case, which has a required dynamic range of 7.4 dB.

C. PROPOSED HYBRID BEAMFORMING ARCHITECTURE

As was observed in the last section, in case of a hybrid beamforming system, a part of the amplitude tapering may be applied in the digital domain, which reduces the requirements on the analog tapering (Fig. 7). The required settings of the variable attenuators, for the case of the analog beamforming benchmark, are shown in Fig. 7(a). Since in this case the full amplitude taper needs to be applied using these attenuators, it can be seen that the attenuators need to cover a large dynamic range, in this case 24.4 dB.

For the case of the hybrid beamforming, the attenuators only need to implement that part of the amplitude tapering, that is relative to the respective subarray. The rest of the amplitude excitation can be applied in the digital domain (Fig. 7(b)). The amplitude scaling is done separately for the 64 subarrays. In this case, the variable attenuators are only required to cover a dynamic range of 7.4 dB.

The reduced requirement in attenuator dynamic range for a hybrid beamforming system brings two main advantages. Firstly, the design complexity of the variable attenuators may be reduced, since less attenuator steps are required. This will save space in the BFIC lay-out. Second, and more importantly, to achieve a certain beam taper in a hybrid beamforming system, much less insertion loss is necessary in the front-end, as compared to an analog beamforming system, as was already visible in Fig. 6(a). This means that the amplification in the BFIC module can be much smaller than for the analog beamforming system. This provides a major advantage in terms of power consumption. An added advantage of the hybrid beamforming architecture is that the digital weights can achieve a high resolution without any insertion losses, as there would be in variable attenuators. This means that the digital weights can be used to perform calibration and tuning on subarray level.

A comparison of the required dynamic range of the taper in the analog domain and the required BFIC amplifier gain for the different systems is provided in Table 4. It can be seen that the HBF system requires 17.0 dB less dynamic range per subarray, as compared to the ABF benchmark system, because a part of the desired taper is applied in the digital domain, which was also visible in Fig. 7. This means that the required BFIC amplifier gain can also be reduced with 17.0 dB to a value of 5.4 dB. The new level information for the improved hybrid system, where this reduced gain is applied, is shown in Fig. 8.

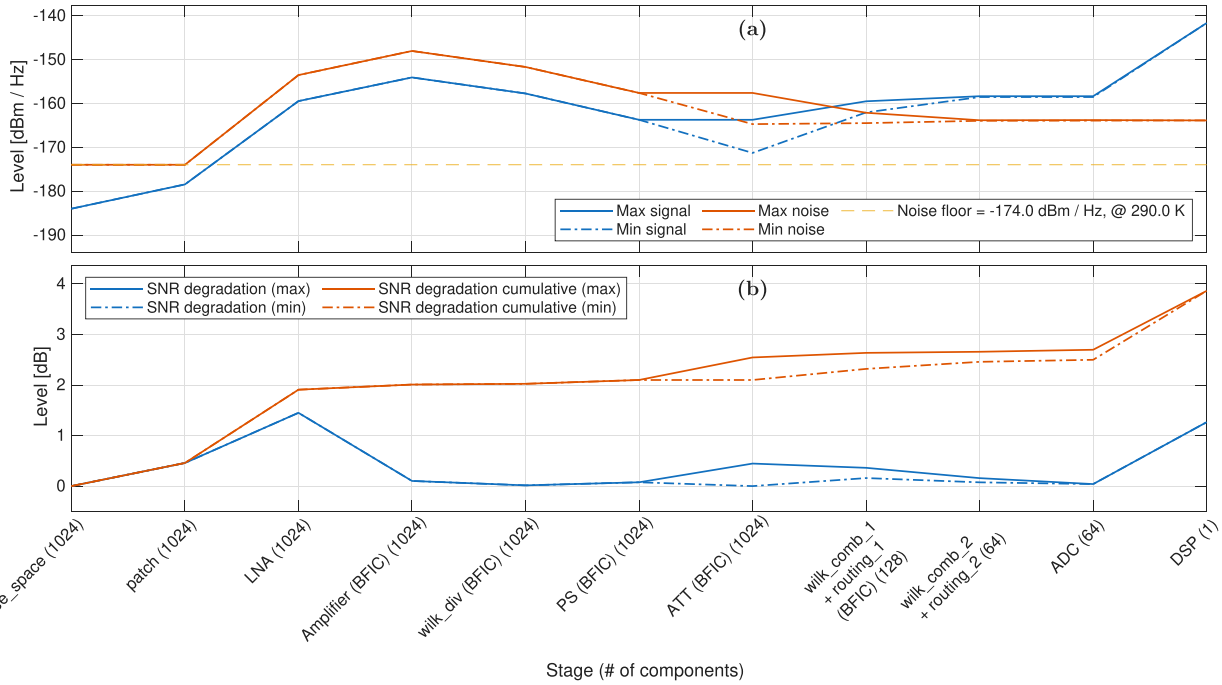

FIGURE 8. Simulation results for the hybrid beamforming system ($N_{sa} = 64$). (a) Signal- and noise levels. (b) SNR degradation. The reduced BFIC amplification makes the operational power level closer to the noise floor. However, in the SNR degradation diagram it can be seen that performance is similar to the analog beamforming benchmark and the hybrid beamforming benchmark.

TABLE 4. Differences in Dynamic Range and Required Amplifier Gain, for ABF and HBF Systems

System	Dynamic range per subarray, as in Fig. 7	Required gain BFIC amplifier
ABF benchmark	24.4 dB	22.4 dB
HBF improved BFIC	7.4 dB	5.4 dB

The results for the improved hybrid system (Fig. 8(a)) are similar to those for the hybrid beamforming benchmark (Fig. 6(a)), but now the signal power is much closer to the noise floor. With regards to SNR degradation (Fig. 8(b)), there is no reduction in sensitivity, as compared to the benchmark hybrid beamforming system (Fig. 6(b)). The reduction in BFIC amplifier gain will lead to a decrease of the amplifier power consumption, as was shown in Table 1. Another way to look at this is that the system front-end operates at lower power levels, which means that a lower linearity of front-end components is required, to obtain the same system performance. A more detailed power consumption comparison will be given in the next section.

IV. COMPARISON OF DC POWER CONSUMPTION

In this section, a comparison of DC power consumption will be done for the three systems discussed in this paper: The analog beamforming benchmark, the hybrid beamforming benchmark and the hybrid beamforming system with improved BFIC modules. The DC power consumption values are calculated based on the information in Tables 1 and 3. The result of the comparison is shown in Table 5.

It can be seen that for the analog beamforming benchmark system, the LNAs and the BFIC amplifiers have the largest contribution to the total power consumption. This is to be expected, since very little is done in the digital domain. There is only 1 digital conversion channel per beam, and no digital processing is performed. The total DC power consumption for the analog beamforming benchmark is 50.07 W.

For the hybrid beamforming benchmark, i.e. without any changes in the analog amplification gain, it can be seen that the power consumption required for analog pre-amplification is the same as for the analog beamforming benchmark. In addition to this, there are now more digital conversion channels, one for every beam and subarray, and digital processing is required. For this reason, the digital parts of the system now also have a significant power consumption contribution. For the hybrid beamforming benchmark, the total power consumption is 66.47 W. This is more than for the analog beamforming benchmark, and for a low number of beams, 2 in this case, this is in line with [1].

The last row of the table contains the power consumption information for the hybrid beamforming configuration, with improved BFIC modules. It can be seen, as is indicated in green, that there is a significant reduction in the power consumption of the BFIC amplifiers, since they require much less gain. For this system, there is more balance between the

TABLE 5. Power Consumption Comparison for the Analog Beamforming Benchmark System, the Hybrid Beamforming System, and the Hybrid Beamforming System With Improved BFIC Modules. Both the Total Power Consumption and the Contribution of Different Component Types Are Shown

	LNA	Amplifier (BFIC)	Mixer	ADC	IO interface	DSP	Total
Analog beamforming benchmark	15.36 W 30.68 %	34.45 W 68.80 %	0.08 W 0.16 %	0.01 W 0.02 %	0.16 W 0.32 %	0.01 W 0.02 %	50.07 W
Hybrid beamforming benchmark	15.36 W 23.11 %	34.45 W 51.83 %	5.12 W 7.70 %	0.66 W 0.99 %	10.24 W 15.41 %	0.64 W 0.96 %	66.47 W
Hybrid improved BFIC	15.36 W 38.11 %	8.29 W 20.56 %	5.12 W 12.70 %	0.66 W 1.63 %	10.24 W 25.41 %	0.64 W 1.59 %	40.30 W

TABLE 6. Reference System Parameters

Array size	$N_{el} = 1024$, 32x32 array
Number of subarrays	N_{sa}, parametrized
Taper	$SLL = 30$ dB Taylor window with $nbar = 4$
Number of beams	$N_b = 2$

requirements on the analog parts and the requirements on the digital parts. The digital parts have made the requirements on the analog domain less stringent. It can be seen that the total power consumption for this system is 40.30 W, which is an improvement with respect to both the analog beamforming benchmark and the hybrid beamforming benchmark.

V. TRADE-OFFS BETWEEN SUBARRAY SIZE VS. SLL, ARRAY SIZE, NUMBER OF BEAMS AND NUMBER OF ADC BITS

Now that the observation is made that the system power consumption may be reduced by selecting an appropriate subarray size, the dependency of the optimal subarray size on SLL, array size, number of beams and number of ADC bits will be investigated. The reference system configuration will be as defined in Section II, repeated in Table 6 for convenience.

Next, the general equation for the total power consumption as function of the component properties in Tables 1, 2 and 3 is given. The total system power consumption is calculated as the sum of the analog and digital power consumption:

$$P_{total} = P_{digital} + P_{analog} \tag{2}$$

The only active analog components are the LNA and amplifier, so P_{analog} is determined as follows:

$$P_{analog} = N_{el}(P_{lna} + P_{amp}) \tag{3}$$

P_{lna} is fixed, and P_{amp} is determined by the amount of required gain, as was defined in Table 1:

$$P_{amp} = G_{amp}\Delta P_{amp} \tag{4}$$

The required amount of amplifier gain is determined by the insertion losses, and the desired clearance of the noise floor:

$$G_{amp} = R - G_{lna} - NF_{lna} + L_{total} \tag{5}$$

where R is the desired clearance of the thermal noise floor for the element with the weakest taper coefficient in the array. In this case $R = 8.85$ dB, such that there is no significant SNR degradation for this element. The LNA already boosts the noise to some extent, as indicated by G_{lna} and NF_{lna}. The total insertion losses L_{total} are determined as follows:

$$L_{total} = L_{wilk\_div} + L_{att} + L_{ps} \tag{6}$$

where L_{wilk_div} are the insertion losses of the Wilkinson divider used to create multiple beams. The loss is equal to $L_{wilk\_div} = log_2(N_b)(3 + L_{wilk\_div\_base})$, with $L_{wilk\_div\_base} = 0.65$ dB, as given in Table 1. L_{att} is the required dynamic range of the variable attenuators, which depends on the selected taper and the subarray size. This value is determined as described in Section III, Section III-C. L_{ps} are the insertion losses that correspond to the phase shifter. The losses of the Wilkinson combiner network, and routing losses are not included in (6), since the element with the weakest taper will be combined with elements with a stronger taper, which will boost the combined signal. Equation (6) only takes the losses into account that need to be compensated to ensure that the margin with the noise floor R is maintained.

The digital part of the total power consumption is determined as follows:

$$P_{digital} = (P_{mixer} + 2P_{adc} + 2f_s N_{bits\_adc}P_{io} + 4f_s P_{dsp})N_b N_{sa} \tag{7}$$

where it can be seen that a digital conversion chain is required for every beam and every subarray. In this case P_{dsp} corresponds to the part of the digital beamforming for that same beam and subarray.

A special case is when $N_{el} = N_{sa}$, which corresponds to the fully digital beamforming. This means that no analog beams and analog tapering is required: $L_{total} = 0$. Furthermore, there is one digital conversion chain per element, such that (7) becomes:

$$P_{digital} = (P_{mixer} + 2P_{adc} + 2f_s N_{bits\_adc}P_{io})N_{el} + 4f_s P_{dsp}N_{el}N_b \tag{8}$$

Equations (2) up to (8) will be used to determine the dependency of the optimal subarray size on the array parameters. This dependency is still based on the component properties in Tables 1, 2 and 3, but can be applied to similar phased array systems by adapting these values.

In Fig. 9(a) the desired maximum SLL is varied. It can be seen that for stronger tapers, the benefit obtained by using

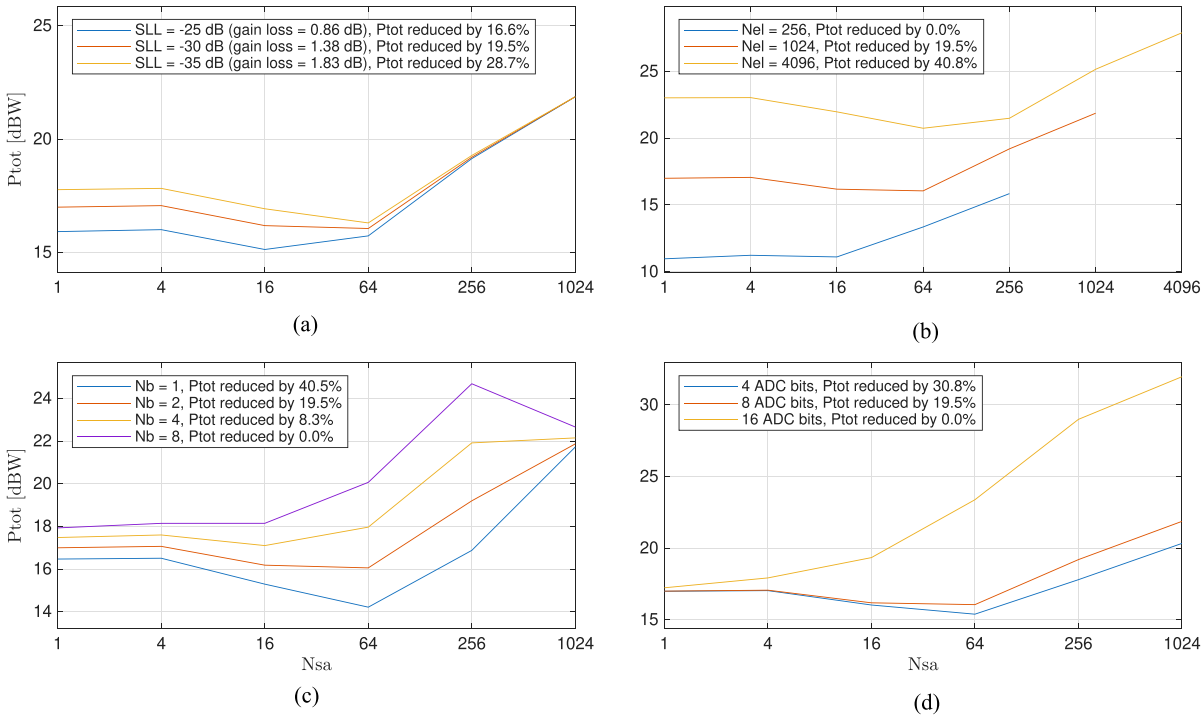

FIGURE 9. Dependency of the system power consumption for different subarray sizes and different array parameters. For each case one of the array parameters is varied with respect to the reference given in Table 6. (a) Dependency on maximum desired sidelobe suppression. (b) Dependency on array size. (c) Dependency on the number of beams. (d) Dependency on the number of ADC bits.

amplitude grouping is larger, and the optimal number of subarrays is larger. The reason is that the taper is stronger, and that therefore the reduction in required dynamic range is relatively large. In the legend the reduction in total system power consumption that may be obtained using hybrid beamforming is also given, when compared to the analog beamforming case. For a desired taper with 35 dB sidelobe suppression, a 28.7% reduction in power system consumption is achieved. For completeness, the gain loss that corresponds to a taper is also given in the legend. The gain loss that corresponds to a taper on receive is determined as follows:

$$G_{\text{loss}} = N_{\text{el}} * \sum_{e=1}^{N_{\text{el}}} |w(e)|^2 \Big/ \left(\sum_{e=1}^{N_{\text{el}}} |w(e)| \right)^2 \tag{9}$$

where w is the applied taper and e is the element index. On receive, when there is sufficient pre-amplification, there is only the SNR reduction as given by (9). There is no additional power loss as there would be on transmit, since the received noise per element is scaled by the same taper.

In Fig. 9(b) it can be seen that the benefit of amplitude taper grouping is larger for larger array sizes. The reason is that in this case many analog channels may be combined in a subarray, such that the power consumption of the digital conversion chains is relatively small. In this case for an array with 4096 elements, a system power consumption reduction of 40.8% is achieved, when hybrid beamforming is used.

Fig. 9(c) shows the dependency of the system power consumption on the desired number of beams. It can be seen that the reduction in power consumption is largest for a single beam, and becomes less for more beams. In a HBF architecture, the digital processing needs to be duplicated for every additional beam, which means that for a large number of beams this architecture quickly becomes undesirable. For a single beam, the use of hybrid beamforming provides a reduction in system power consumption of 40.5% . Furthermore, it can be seen that for the case of 8 beams, and 256 subarrays, the power consumption is even larger than for the case of fully digital beamforming. The reason is that in this case there are only 4 elements per subarray, and 8 digital conversion chains per subarray, which means that it is more efficient to just have one digital conversion chain per antenna element.

Finally, the dependency on the number of ADC bits is analyzed. The effect of the ADC number of bits on P_{adc} is determined using the Walden FOM [34]:

$$P_{\text{adc}} = 2^{ENOB} FOM_{\text{W}} f_{\text{s}} \tag{10}$$

where $ENOB$ is the ADC equivalent number of bits. In this case $ENOB$ is selected to be $N_{\text{bits\_adc}} - 1$. It can be seen (Fig. 9 d) that for more bits, the benefit obtained via amplitude taper grouping becomes smaller. The reason is that the digital power consumption for a single subarray conversion chain becomes relatively large. For an ADC with 4 bits, hybrid beamforming provides a reduction of system power consumption by 30.8% , but with more bits the benefit starts to disappear.

It can be concluded that the benefit obtained via amplitude taper grouping is the most significant for phased array systems

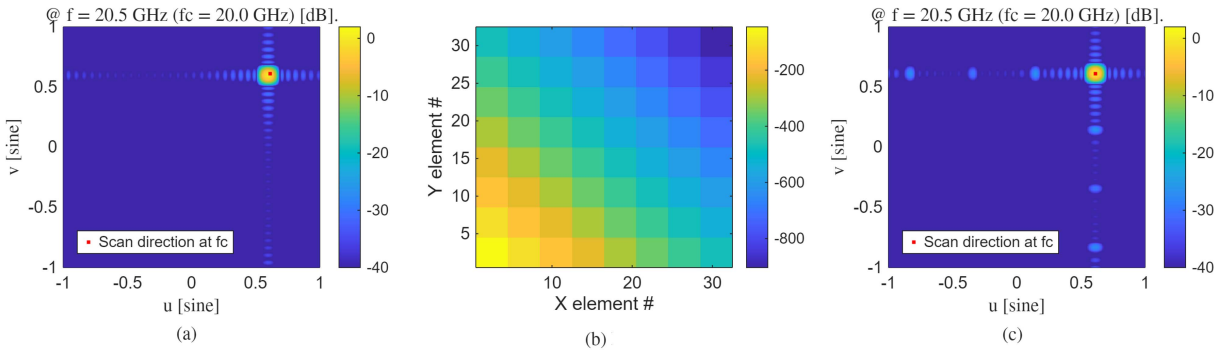

FIGURE 10. The effect of TTD correction at subarray level, for the case $N_{sa} = 64$. (a) shows the beam pattern for scan angle azimuth 45 degrees, and elevation 60 degrees, at 0.5GHz from the center frequency. In this case no TTD correction is applied yet. (b) shows the delay correction per element, when delay correction is only done per 4x4 subarray. (c) shows the same beam pattern as in (a), but now with TTD correction.

that have strong taper requirements, have a large number of elements, require a small number of beams, and require a small dynamic range. These requirements fit well with SatCom terminals, and it is expected that benefits can be achieved for this application.

VI. APPLICABILITY TO DIFFERENT BEAMFORMING ARCHITECTURES

In this section the applicability of amplitude taper grouping to other variants of beamforming architectures is discussed.

A. VARIANTS OF THE COMPONENT BUILDING BLOCKS

The BFIC module considered in this work was based mostly on [2], and uses phase shifters and variable passive attenuators. Another possibility is to use variable gain amplifiers (VGA) [32], whether this is in combination with phase shifters, or in a vector modulator (VM) configuration. The power consumption of a VGA typically does not depend on the gain setting [36], [37]. For this reason the method in this paper also applies to configurations with VGAs, to reduce the maximum required gain, and therefore the VGA power consumption.

Furthermore, in this paper a direct zero-IF conversion is assumed, where two ADCs sample the I- and Q- branches separately with a sampling rate close to the instantaneous bandwidth. Depending on system requirements, different digitization schemes, for example using multiple conversion stages, non-zero-IF sampling [38], or subsampling [39], may be desirable. The choice of digitization scheme will affect the power consumption of the digital conversion chain, as shown in Fig. 1(c), and will therefore change the optimal subarray size at which the system power consumption is minimized.

Alternatives to the digital processing are also available. For example, instead of performing the complex multiplication using 4 real multiplications and 2 additions, another method is to use 3 real multiplications and 5 additions. This choice, as well as other digital processing approaches, will affect the power consumption in the digital domain, determined in (7).

B. DELAY CORRECTION

Not yet considered in this paper is the requirement on delay correction. For wideband systems, it can be necessary to perform true time delay (TTD) correction to avoid beam squint and array-level inter-symbol interference (ISI) [40]. TTD correction may be done using analog TTD modules, but these are lossy, introduce errors in the frequency spectrum [41], and take up additional space. An additional advantage of the HBF architecture is that TTD at subarray level may be corrected in the digital domain. Fig. 10 shows the effect of performing TTD correction digitally only at subarray level, in the system defined in Section II with $N_{sa} = 64$. It can be seen that the delay correction mitigates the effect of beam squint, but some additional sidelobes are introduced, in this case at a level of -27 dB. Whether this is acceptable depends on the system requirements. The choice of analog TTD modules or digital TTD modules impacts the power consumption of the analog domain and the digital domain respectively, and will affect the optimal subarray size. To include TTD correction in the simulation approach, add the power consumption required to overcome the insertion losses of analog TTD modules, or add the power consumption required for digital TTD correction.

C. APPLICABILITY TO TRANSMITTERS

The concept of amplitude taper grouping can also be applied to the feeding network in phased array transmitters. When compared to a hybrid beamforming receiver, such as the one defined in Section II, to create the equivalent hybrid transmitter architecture the downconverter and ADC are replaced by a digital-to-analog converter (DAC) and upconverter respectively. Furthermore, the LNA and pre-amplifier are replaced by a driver amplifier and a power amplifier (PA). For smaller arrays the power consumption of a transmitter phased array is dominated by the PAs [12], [13], but for larger array sizes the digital processing, DACs and feeding network become more important. In this case the principle of amplitude taper grouping can be applied. However, in practice it is often not desirable to apply a strong taper in transmission, since this reduces the EIRP and transmitter power efficiency. When sidelobe control is desirable in a transmitter, it can be more

desirable to make use of phase-only tapering [42], with limited capabilities, or density-tapered arrays [43], [44] with a larger feeding network and calibration complexity [45].

VII. CONCLUSION

This paper presents a novel system design framework for SatCom hybrid beamforming receivers, enabling part of the desired amplitude taper to be implemented in the digital domain, thereby reducing power consumption and relaxing the constraints on the analog front-end without compromising sensitivity or beam scanning performance.

A hybrid beamforming system with parametrized subarray size was defined to create analog and hybrid benchmark systems with equal sensitivity, which were shown to have a total power consumption of 50.1 W and 66.5 W respectively. A joint signal and power consumption analysis was used to show that in the hybrid beamforming architecture a part of the amplitude taper can be moved to the digital domain, thereby reducing the required dynamic range of the variable attenuators in the analog domain. This means that insertion losses are reduced, and that therefore the amount of required pre-amplification can be reduced. Using this approach, a recommendation is made for a new BFIC module design, that has reduced attenuator dynamic range and reduced pre-amplification. A hybrid beamforming system that makes use of these modules is simulated to have a total power consumption of 40.3 W, less than both benchmarks, while achieving the same sensitivity.

Using this approach, an analysis is performed of the dependency of system power consumption on the number of subarrays, as well as the desired sidelobe suppression level, array size, number of beams and number of ADC bits. For a reference hybrid system with −30 dB SLL, 1024 elements, 2 beams, and 8 ADC bits, and with optimized subarray size, the reduction in system power consumption is simulated to be 19.5% with respect to the equivalent analog beamforming system. The reduction in the power consumption further increases for stronger sidelobe suppression levels (28.7% at −35 dB SLL), for larger array sizes (40.8% for 4096 elements), smaller number of beams (40.5% for a single beam), and a smaller number of ADC bits (30.8% for 4 bits). These properties fit well with requirements to SatCom receiver systems. The proposed power minimization approach is also applicable for similar Rx-Tx phased array systems with different component properties.

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