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CVD Delta-Doped Boron Surface Layers for Ultra-Shallow Junction Formation

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A new doping technique is presented that uses a pure boron atmospheric/low-pressure chemical vapor deposition (AP/LPCVD) in a commercially available epitaxial reactor to form less than 2-nm-thick δ-doped boron-silicide (B_xSi) layers on the silicon surface. For long exposure B segregates at the surface to form a very slow growing amorphous layer of pure B (α-B). The electrical properties of the as-deposited α-B/B_xSi stack have been studied by fabricating and measuring diodes where the B depositions are formed directly in the diode contact windows for different exposure times. It is demonstrated that the presented doping technique can be used to form high-quality δ-doped p^+n junctions. Moreover, the formed α-B/B_xSi layer is an attractive source of high-concentration B dopants for thermal annealing processes that does not induce any transient-enhanced diffusion (TED) effects.

Introduction

The future scaling of Si-based CMOS devices demands a progressive reduction of source/drain junction depths (< 10 nm), while concomitantly optimizing the sheet resistance (< 700 Ω/sq) and doping abruptness at the S/D-extension to channel junction. The most commonly used technique is ion implantation of dopants followed by activation by (rapid) thermal annealing. However, the associated implantation damage is responsible for transient-enhanced diffusion (TED) that is particularly severe for boron impurities and can lead to a significant broadening of the desired dopant profiles. As an alternative to the traditional B^+ or BF_2^+ implantations, there have been a few reports of the use of molecular layer doping (MLD) (1)-(2), and vapor-phase doping (VPD) (3)-(5). In these studies, a surface-reaction doping using B_2H_6 as gas source has been applied for implementing ultra-shallow junctions. Hereby TED was effectively avoided, since no lattice defects are created in the substrate. However, either the poor control of the high-concentration boron adsorbed layers or the process complexity have made these methods unattractive.

In this paper we present a new doping technique using a pure boron atmospheric/low-pressure chemical vapor deposition (AP/LPCVD) to form δ-doped boron surface layers. Our investigation of the deposition conditions and electrical characteristics show that B deposition has several attractive properties and these are the result of two important phenomena:

— in the first stage of the deposition, the chemical reaction of B_2H_6 with the Si surface leads to B adsorption. The B reacts with the Si to form an ultra-shallow ultra-abrupt boron-silicide (B_xSi) layer, about 2 nm thick. This layer acts as a highly doped p-type region that can either ensure low-ohmic contact to lightly doped p-regions or provide an ideal p^+n junction on n-regions;

— after a few seconds of deposition, the Si surface is completely covered with B that subsequently segregates as a very slow growing amorphous layer of pure B (α-B). This layer has semi-metallic properties with a high resistivity in the range of 10^6 Ωcm.

The as-deposited α-B/B_xSi layers have the advantages that epitaxial processes have in general: they are conformal and will give a perfect B coverage on etched surfaces, as for example in trenches, and they supply a TED-free source of B for thermal diffusion of junctions. In addition, during diffusion the presence of the α-B layer gives the extra advantage of acting as a capping layer that prevents B desorption from the B_xSi layer and also gives an abundant supply of boron that can be diffused into the Si substrate. Thus this method offers a high doping efficiency and a good control of the resulting junction depth.

B-layer material properties

Deposition and layer analysis

The boron deposition is performed in a commercially available AP/LPCVD epitaxial reactor on Si(100) wafers using B_2H_6 as the gas source diluted in H_2, for a range of deposition temperatures and pressures from 500 ºC to 700 ºC and from 36 to 760 Torr, respectively. The formation of the boron layers is slower the lower the temperature and the B_2H_6 partial pressure, and predominantly determined by the exposure time. The results presented here correspond to 1 s to 30 min depositions at 700 ºC and B partial pressure of 3.56×10^{-3} Torr in a 760 Torr ambient.

For the experiments a native-oxide-free silicon surface is ensured by HF dipping before entering the CVD reactor and using an in-situ 30 min pre-bake step at 900 ºC in H_2 atmosphere before deposition. However, a pre-processing step that allows pre-baking at 700 ºC is also commercially available and would make it possible to do the whole deposition process at this temperature. Moreover, the integration of such B-layers in a device process is facilitated by the fact that the B-layer is very robust: it does not oxidize in air and is resistant to HF etching.

If the in-situ pre-bake step is omitted, the B deposition is effectively inhibited. This is in agreement with the conclusions made elsewhere that the boron will selectively deposit on a clean Si surface. Previous studies have investigated the dependence of the B_2H_6 reaction on different underlying substrates. In particular, they have shown a negligible surface B concentration on silicon dioxide (1)-(2), and the absence of diffusion through it (6), even for temperatures higher than 700 ºC. This behavior is not physically clarified yet, but the reaction model proposed in (7) for rapid vapor-phase doping is based on the chemisorption of the BH_3 precursors, which are generated by thermal dissociation of B_2H_6, in the presence of surface Si dangling bonds. Therefore, the doping selectivity might be related to a lower surface density of sites available for formation of Si-B bonds in the SiO_2 structure, promoting migration of physisorbed species and suppressing chemisorption. For the low temperatures used in our process, it is safe to assume that the diffusion of any adsorbed B atoms through the isolation layer is prohibited even for minute long exposure.

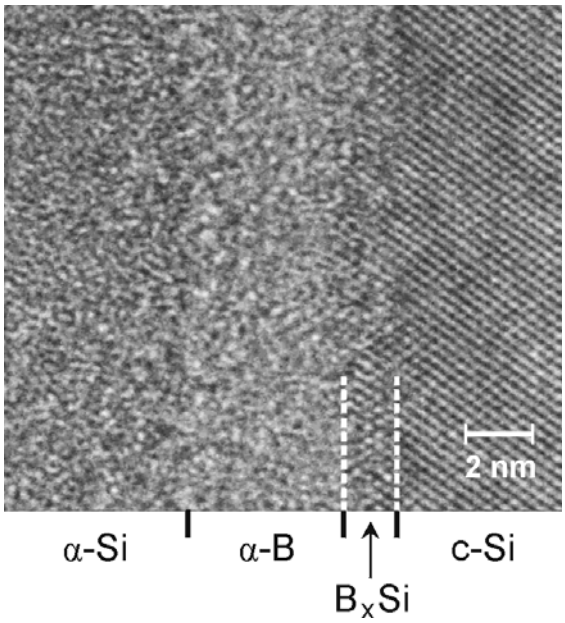

Figure 1. TEM image of the α-B/B_xSi layer stack for a 10 min boron CVD deposition at 700 ºC. The stack is covered with 100 nm PVD α-Si.

The α-B/B_xSi layer stack of a 10 min B deposition can be distinguished in the TEM image in Fig. 1. At the interface between the α-B and c-Si, a rough layer of ~ 2 nm thick is seen that can be identified as a mixture of boron and silicon atoms. Similar B_xSi layer formation has been reported in the literature under comparable deposition conditions (2). In (6) the surface morphology analysis of boron silicide layers has shown that nucleation is initiated for a small dose of B_2H_6, and grains form and merge into a rough film for increasing doses and temperatures. Above 800 ºC the reaction with Si is enhanced and the B_xSi layer thickness can reach 50 nm for a 90 min deposition. However, it is worth noting that for all the process conditions presented in (2) and (6) a boron silicide layer will form when a high boron surface density is induced, i.e. boron atoms chemically adsorb on to the surface with high sticking coefficient. In fact, Kiyota et al. (7) have demonstrated that the surface conditions for the samples doped in hydrogen atmosphere at 800-900 ºC without boron segregation were almost identical to the usual boron-doped silicon. On the other hand, in the case of nitrogen, which led to boron segregation for the same processing conditions (used also in the work of Saitoh et al. (2)), the results from x-ray photoelectron spectroscopy have been attributed to either boron that bonded with silicon or metallic boron that segregated on the surface. However, a high sticking coefficient configuration has been achieved in (8) by using hydrogen as carrier gas at 900 ºC and increasing the boron partial pressure by a factor of 10. Therefore, B segregation can prevent re-evaporation of adsorbed boron into the atmosphere and promote the reactivity of the chemisorbed species with the surface silicon atoms for the B_xSi formation. This can be achieved at higher flow rates of diborane and at lower temperatures, such as the 700 ºC that we use in the present work.

Boron SIMS profiles for various deposition times are also shown in Fig. 2. From these the integrated B surface doping densities can be estimated and the values for several of the processed δ-doped boron layers are reported in Table I. When the deposition time increases the total B concentration is seen to increase, which can be understood in terms of the following growth kinetics. First, the boron coverage increases with the B_2H_6

exposure and the adsorbed B atoms react with the Si surface to form a B_xSi region. Subsequently, dopants segregate at the surface and the coverage exceeds 1 ML (ML = mono-layer), which will be comparable to the corresponding Si(100) surface atomic density of 6.78×10^{14} cm^{-2}. This results in the α-B layer formation.

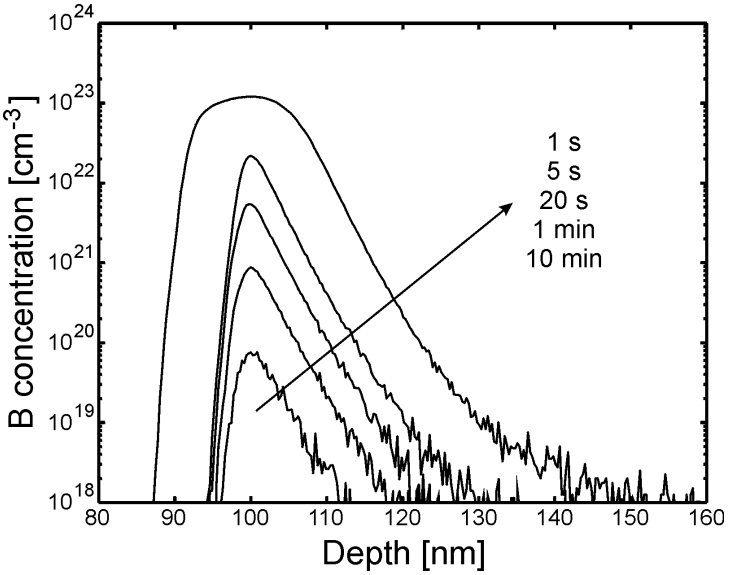

Figure 2. B SIMS profiles of the α-B/B_xSi layer stack for 1 s to 10 min boron CVD deposition at 700 ºC. The stack is covered with 100 nm PVD α-Si. The wide peak of the 10 min sample is due to the SIMS knock-on effect in the α-B layer. The point of peak B concentration is moved to 100 nm in all cases.

TABLE I. Total B SIMS concentrations for different deposition and anneal conditions, with and without α-B removal by cleaning and HF dipping.

Deposition time	Post-annealing	α-B removal	Dose [cm^{-2}]
1 s	-	-	3.84×10^{13}
5 s	-	-	4.22×10^{14}
20 s	-	-	2.47×10^{15}
1 min	-	-	9.82×10^{15}
10 min	-	-	1.55×10^{17}
10 min	-	x	9.16×10^{13}
10 min	950 ºC - 30 min	x	8.54×10^{14}
10 min	ELA 900 mJ/cm^2	x	1.59×10^{16}

Due to the very large amount of deposited B atoms in our CVD process a SIMS profile does not give sufficient depth resolution to be able to isolate whether there is B diffusion into the substrate. Therefore, the out-diffusion of the B_xSi has been monitored by an in-house CV-profiling technique that uses an abrupt n^+ buried layer to profile the tail of B-doped layers at the wafer surface (9). In Fig. 3, the measured profile of a 30 min B deposition is compared to that of a neighbouring contact without B deposition (i.e. a Schottky contact) and that of a BF_2^+ implant after a 30 min 700 ºC thermal anneal. While the latter shows an extremely large TED tail, the difference in depth between the B-deposited and Schottky contact (~ 10 nm) confirms that the diffusion of B atoms into the substrate is negligible at the processing temperature of 700 ºC and no TED effects are present even after long thermal exposure.

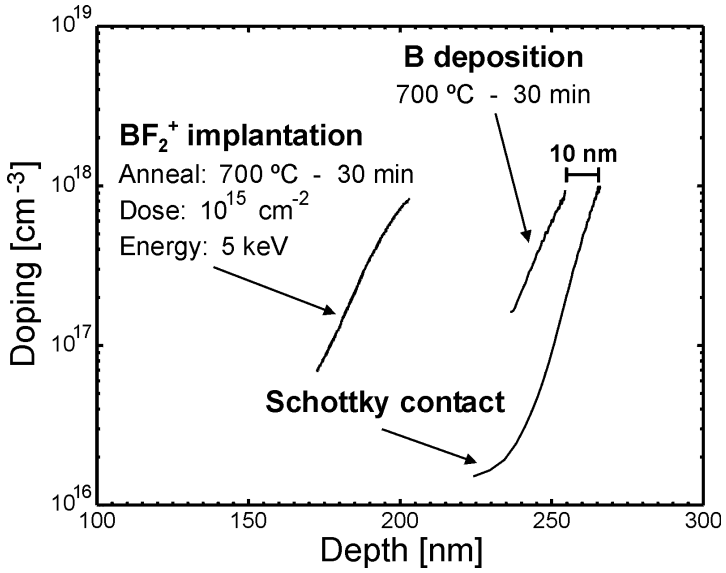

Figure 3. CV doping profiles measured from an abrupt n^+ buried layer to a Schottky contact, a 30 min B deposition at 700 ºC, and a BF_2^+ implant after a 30 min 700 ºC thermal anneal.

Deposited B as source of dopant diffusion

Two aspects may pose limitations on the use of the as-grown B_xSi layers as either S/D extensions or contacts. First, although the sheet concentration of the as-deposited B_xSi layer is much higher than 10^{14} cm^{-2} dopant atoms, the active doping concentration is limited by the B solid solubility at the deposition temperature (700 ºC) to give an active doping level of ~ 2×10^{19} cm^{-3} (10), which is more than 10 times lower than the chemical concentration. Accordingly, the sheet resistance of the layer is found to be ~ 10 kΩ/sq. A (rapid) thermal annealing step can provide a higher dopant activation and a deeper junction depth to achieve lower sheet- and contact-resistance values. However, if the B_xSi is not capped with a sufficiently thick α-B layer, the B will readily desorb, significantly reducing the dopant concentration in the Si (11). The α-B capping layer has the additional advantage of also being able to supply boron for thermal diffusion in the Si. For example, after the 950 ºC anneal shown in the SIMS profile of Fig. 4, the total number of B dopant atoms has increased and the active doping level is at ~ 10^{20} cm^{-3}. To increase the substitutional B atoms in the Si substrate even further than the solid solubility, it is possible to use the new doping method in combination with excimer laser annealing (ELA). This is demonstrated by the laser anneal result given in Fig. 4, where a junction depth similar to the thermally annealed sample is achieved but with a B incorporation that is enhanced by a factor of ~ 20.

Removal of α-B layer

The formation of the α-B layer and the associated series resistance is pattern and surface-roughness dependent, in the manner that a thicker layer forms at the contact window edge and on rough surfaces. For many applications the high series resistance through this layer will limit the device performance at high current levels. The α-B layer can be removed by standard cleaning in HNO_3 (100%) followed by a HF (0.55%) dip to remove the resulting cleaning oxide.

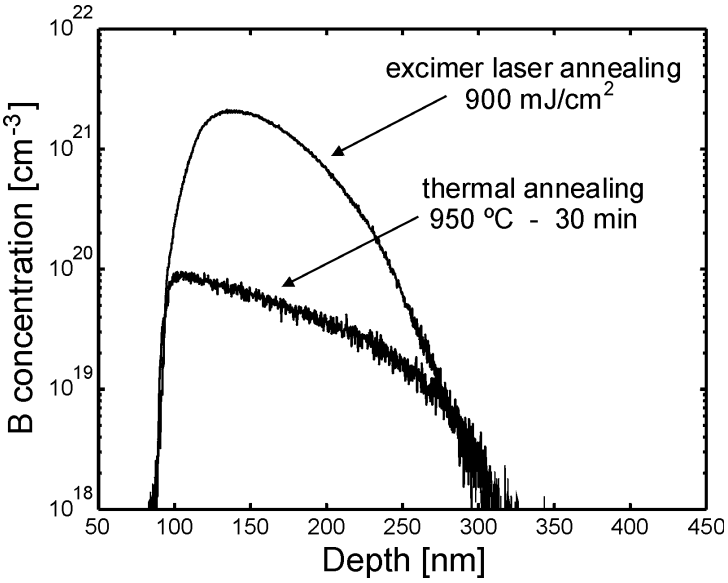

Figure 4. B SIMS profiles of a 10 min B deposition at 700 ºC after a 30 min thermal annealing at 950 ºC compared to a 900 mJ/cm^2 excimer laser annealing performed by the system described in (12). The standard cleaning in HNO_3 and the HF etching step have been performed before covering the sample with 100 nm PVD α-Si.

This process will, however, also remove a substantial part of the B_xSi layer as can seen in Table I, which has also been measured to significantly increase the B_xSi sheet resistance. On the other hand, for out-diffused junctions the removal of the α-B is no longer an issue.

Diode fabrication and characterization

Fabrication

The electrical properties of the α-B/B_xSi stack have been studied by fabricating and measuring diodes. A 0.9 μm n-doped epitaxial layer (~ 10^{16} cm^{-3}) is grown on a 2-5 Ωcm p-type Si(100) substrate with n^+ buried layer. After the growth of 30 nm thermal oxide, P^+ implantations were performed to increase the epi-doping concentration to ~ 10^{17} cm^{-3}. Kelvin test structures for measurement of the contact resistance of shallow junctions were also implemented (13) by creating a p^+ diffusion tap in the low-doped epi-layer with a deep and shallow B^+ implantations of 5×10^{15} cm^{-2} at 180 keV and 15 keV, respectively. Then a 300 nm LPCVD TEOS oxide surface isolation layer was deposited in which the contact windows to be treated with a B deposition were plasma etched with soft landing on the Si. The boron layer was deposited as described above and results are reported below for samples with different deposition times. The B-treated contact windows were directly covered by an Al/Si(1%) PVD metallization and contacts to other device regions were then opened and metallized. After metal patterning, a 400 ºC alloy step in forming gas is performed. All the different types of devices described above have been fabricated several times in different runs. It is noteworthy that even for the 1 s deposition the repeatability of the results was found to be excellent.

Electrical measurement results

Electrical measurements are summarized in Table II that also includes data for contacts processed without a deposited B-layer, i.e. a Schottky contact directly on the substrate is formed. Compared to this case, the contact resistivity first drops with B deposition time going from 1 to 5 s and then increases to reach higher values for minute long depositions. The corresponding I-V series resistance of p^+ resistors contacted via a B-deposited contact show a similar behavior. From the measured resistance and the width of the α-B layer measured by HRTEM, it can be concluded that this layer has a resistivity in the range of 10^6 Ωcm.

TABLE II. Electrical measurements results.

Deposition Time	Kelvin contact [1] ρ_c [Ωcm^2]	p^+ resistor [2] R_S [Ω]	Diode [3] R_D [Ω]	Diode [4] I_S [A]
no deposition	3.6×10^{-7}	23.8	1240	1.3×10^{-12}
1 s	1.5×10^{-7}	15.5	294	3.7×10^{-16}
5 s	1.3×10^{-7}	13.3	241	2.1×10^{-16}
20 s	(1.1×10^{-6})	16.5	214	6.3×10^{-18}
1 min	(1.1×10^{-5})	92.5	338	1.6×10^{-18}
10 min	(7.2×10^{-2})	5.2×10^5	3.5×10^5	1.3×10^{-18}
30 min	$(> 8.0 \times 10^{-2})$	1.8×10^6	2.0×10^6	1.4×10^{-18}

[1, 2] ρ_c is the contact resistivity measured by using Kelvin test structures made with p^+ diffusion taps to the contact and R_S is the corresponding total resistance measured directly through one of the p^+ taps and the B-treated contact with a size of 2×2 μm^2. The brackets indicate that measured ρ_c is not reliable, i.e. the contact resistance does not scale with the contact window size. This is due to the high resistance of the α-B layer that forces the current path away from the contact.
[3, 4] R_D is the diode high-current series resistance, that includes series resistance of n-type Si substrate, and I_S is the saturation current. The anode area is 2×1 μm^2.

In Table III the contact resistivity of the B deposition is compared to that of different types of implanted contacts as well as a low-temperature-epitaxy B-doped layer. The short-time B deposition combines a low processing temperature with the lowest contact resistivity value.

TABLE III. Contact resistivity to p^+ top layers formed with different doping techniques.

Doping technique	Process conditions	ρ_c [Ωcm^2]	Ref.
B deposition	700 ºC - 5 s (*on top of the following p^+ layer*)	1.3×10^{-7}	this work
B^+ implantation	5×10^{15} cm^{-2}, 15 keV annealing: 700 ºC - 40 min	3.6×10^{-7}	this work
	2×10^{14} cm^{-2}, 20 keV annealing: 950 ºC - 30 min	6.0×10^{-6}	(13)
	5×10^{15} cm^{-2}, 180 keV annealing: 950 ºC - 30 min	2.0×10^{-5}	(13)
	3×10^{15} cm^{-2}, 15 keV annealing: 950 ºC - 30 min	5.6×10^{-7}	(14)
BF_2^+ implantation	5×10^{15} cm^{-2}, 20 keV annealing: 700 ºC - 30 min	2.5×10^{-6}	(14)
Epitaxial growth	in-situ B^+ 2.7×10^{19} cm^{-3} 700 ºC - 2.5 min	2.1×10^{-7}	(14)

The diode I-V characteristics for different B deposition times are shown in Fig. 5, which also includes the case without any B deposition. All diodes, both large ones and the smallest ones of 1×1 μm^2, have near-ideal characteristics with ideality factors lower than about 1.02. The B deposition effectively decreases the saturation current and a transition is seen from the high-current Schottky to the low-current p^+n diode situation as the deposition time increases (15), even for small active area devices where the peripheral leakage current due to surface states at the silicon/oxide interface could be dominant. The series resistance that attenuates the current at high forward voltages decreases dramatically as the B deposition starts and a minimum is reached for the 20 s deposition as can be seen in Table II. Similar behavior was observed for the p^+ resistors, but these show an increasing resistance already for a 20 s deposition. Therefore, the benefit for the saturation current lowering in the diodes is apparently large enough to compensate the increased series resistance when the α-B layer begins to form. In fact, the p^+ resistor measurements suggest that a significant layer is already formed for the 20 s deposition. This effect may be similar to what has been reported by Connelly et al. (16) where integration of sub-nm thick nitride layers was found to decrease the contact resistance of Schottky diodes. When a significant α-B layer has formed, the series resistance starts to increase dramatically and has reached very high values for the 10 min deposition. The influence of the α-B layer is also seen in the ideal diode current that decreases by a factor 4 from the 20 s to 1 min deposition. It is plausible that this effect is due to a low surface recombination velocity at the α-B/B_xSi interface, since the extremely narrow B_xSi width would otherwise lead to a "Schottky-like" high current.

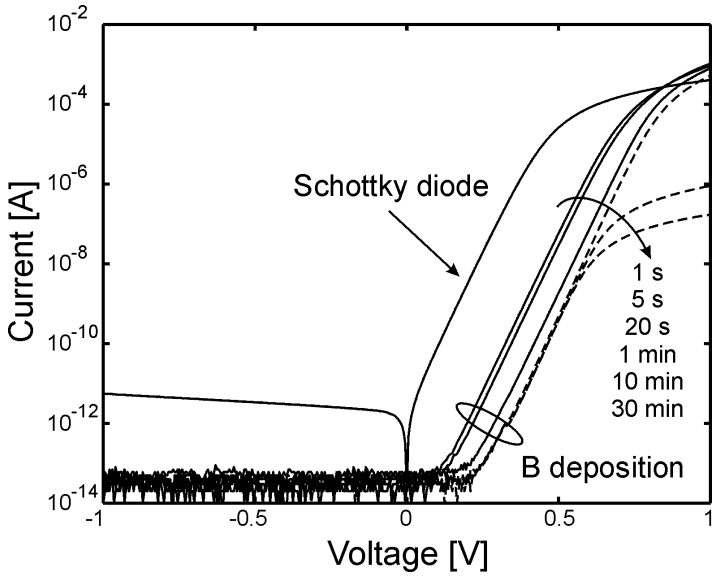

Figure 5. Diode I-V characteristics for different B deposition times. The anode area is 2×1 μm^2.

Conclusion

It has been demonstrated that CVD-deposited α-B/B_xSi stack is a reproducible, TED-free source of boron doping with which high-quality δ-doped p^+ layers with depths down to ~ 2 nm can be formed. In particular, in any subsequent rapid thermal annealing process the α-B acts as a capping layer that prevents B desorption from the B_xSi layer and also

gives an extra supply of boron that can diffuse into Si substrate. The remaining α-B layer will for a layer of nm thickness represent a high series resistance, but it can be removed by cleaning and HF etching. The non-capped, as-deposited B_xSi layers are so thin that when used to form p^+n diodes the current level will be much higher than that of deeply diffused junctions. Adding the α-B layer will very effectively suppress the saturation current but at the price of an undesirably higher series resistance. However, the results show that it is possible to get the best of both worlds by depositing a suitably thin α-B layer that both suppresses current and lowers the contact resistance to the B_xSi layer. Such an extremely shallow but efficient stack could be very interesting for use in numerous device applications. The B_xSi p^+ layers may well be a very attractive alternative to metal CMOS source/drain contacts since they have low resistance and very low reverse leakage current. The demonstrated advantages for diodes also mean that the α-B/B_xSi stack could be promising as an emitter in bipolar and heterojunction PNPs. In these applications the absence of damage that can lead to transient-enhanced diffusion, such as in the case of shallow B implants, can be of crucial importance for the overall device performance.

Acknowledgments

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