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Manufacturing of an In-Package Relative Humidity Sensor for Epoxy Molding Compound Packages

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Abstract

This study presents the design and fabrication of an in-package relative humidity sensor for epoxy molding compound (EMC) packages. The sensor comprises shielded interdigital electrodes (SIDE) for in-situ monitoring of humidity absorption/desorption in the package encapsulation layer. A novel approach is employed in the device fabrication to maximize the electrical field lines to pass through the EMC and enhance the sensitivity. The manufactured wafer includes 6x6 mm^2 dies, each containing six identical capacitive sensors with an area of 480 x 620 μm^2. SU-8 through polymer vias (TPVs) with high aspect ratio were created to locally mold the sensors by EMC. The linear capacitance change with the relative humidity level is simulated in COMSOL Multiphysics. Three designs were compared, and the calibration results show the capacitance value of 1.54 pF and 5.85 pF before and after molding, respectively. The capacitance value stays within the range of 5.85 to 5.86 pF with less than 7 aF variation under different biasing voltages, indicating the stability and robustness of the capacitance.

Keywords— In-package relative humidity sensor, epoxy molding compound, shielded interdigital electrodes, encapsulation layer, electrical field lines, through polymer vias.

1. Introduction

Electronic relative humidity (RH) sensors have been widely used in numerous applications, such as automotive reliability, quality control, and ambient control. Moreover, humidity in products such as packaged agricultural or industrial products and microelectronic devices can be a source of degradation. Therefore, the need for measuring the RH in a microelectronic system or package is of great significance in terms of reliability and quality control.

RH sensors can be implemented in resistive and capacitive configurations [1]–[4]. Resistive humidity sensors are electronic devices that measure RH by detecting changes in the electrical resistance of a sensing element. These sensors typically consist of a thin film of a hygroscopic material, such as polymer, ceramic, or metal oxide, that absorbs or releases moisture in response to changes in ambient humidity. As the humidity level changes, the sensing element's resistance changes as well. This change in resistance can be measured using a simple circuit, such as a voltage divider or Wheatstone bridge, and the resulting signal can be converted into a digital or analog output that reflects the current RH level.

Resistive humidity sensors are efficient in terms of manufacturing cost and process complexity. However, they may require periodic calibration to ensure accurate measurements due to non-linearity. Moreover, their response is limited to poor sensitivity at low humidity levels below 10%, mainly due to insufficient resistance conductivity [5].

Capacitive humidity sensors measure RH by detecting changes in the dielectric constant of a sensing element. These sensors typically consist of two metal plates separated by a thin layer of a hygroscopic material, such as a polymer. As the ambient humidity level changes, the hygroscopic material absorbs or releases moisture, which changes the dielectric constant of the sensing element. This change in the dielectric constant alters the capacitance between the two metal plates [6], [7].

In contrast to resistive RH sensors, capacitive RH sensors respond faster and perform more accurately, which makes them suitable for automotive reliability monitoring. Moreover, they are less prone to drift over time compared to resistive humidity sensors, which simplifies their readout circuits.

The capacitive sensor design methods can be divided into parallel plate (PP) and inter-digital electrodes (IDE). PP capacitive humidity sensors consist of two metal plates separated by a dielectric material, such as a polymer. These sensors are relatively simple and easy to manufacture but may be more susceptible to external interference. IDE capacitive humidity sensors use a series of interleaved metal electrodes on a substrate, typically a silicon wafer. These electrodes can be coated with a sensing material that monitors the level of humidity [8]. Compared to PP capacitive humidity sensors, IDE sensors operate with a faster response as the sensing material is directly exposed to moisture. However, only half of the electric field lines pass through the dielectric sensing material, which limits their sensitivity. Therefore, there is a trade-off between the sensitivity and the response time of the capacitive humidity sensors.

To date, extensive research has been carried out to alleviate this trade-off. For example, Zhao et al. proposed etching the sensing material in PP capacitive sensors by reactive ion etching (RIE) to increase the contact area and enhance the humidity absorption speed [9]. The response time, however, is relatively lower than conventional IDE sensors. Moreover, in 2019, Liu et al. introduced a capacitive sensor called shielded interdigital electrodes (SIDE) in which both the advantages of high sensitivity

(0.0063%) and fast response (20 s) were combined [10]. This structure, illustrated in Fig.1, was then coated with Polyimide (PI), a porous organic sensing material [11]. However, it cannot perform in-situ reliability monitoring of the packaged electronic devices coated with epoxy molding compound (EMC).

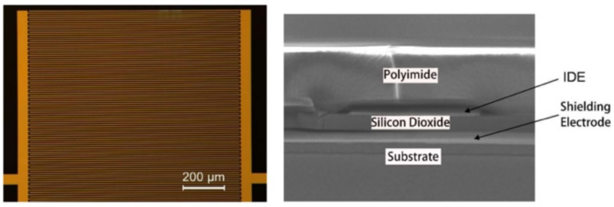
To date, the humidity-related properties of EMC have been investigated using mass measurements [12]. However, this approach is often incompatible with an industrial reliability test procedure. In this study, an in-package RH sensor is developed and manufactured to mitigate this issue. Furthermore, it can potentially monitor RF reliability and aging, and therefore contribute to EMC module development.

2. Design and Methodology

This study presents a novel SIDE capacitive structure fabricated to monitor the humidity absorption/desorption of the epoxy molding compound (EMC) or other encapsulation layers. The proposed design aims to improve the relative capacitance change under moisture exposure, i.e., sensitivity. Several designs have been tested with alternative dimensions and pitches to optimize the IDE design. The finger layouts are depicted in Fig. 2. To this end, the effect of parasitic capacitance has been minimized by dedicated sensor design and processing techniques.

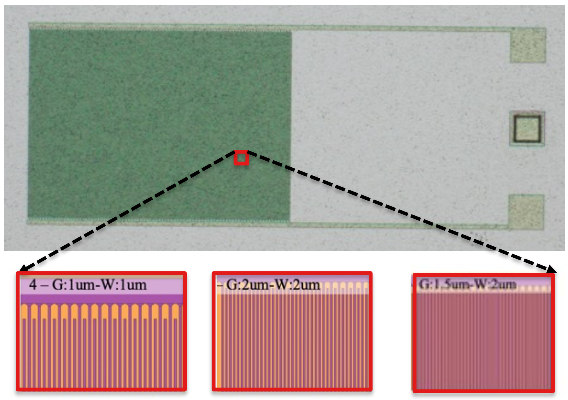
The fabrication process was initiated by cleaning and etching 120 nm deep alignment markers into the silicon wafers. Subsequently, a metal shielding layer has been deposited to enhance the sensitivity. To this end, a 500 nm thick aluminum (Al) layer was sputtered at 25 ˚C. In this case, a low deposition temperature was chosen to ensure layer uniformity rather than good step coverage. Next, 2 µm TEOS was deposited using plasma-enhanced chemical vapor deposition (PECVD). The GND contact via of the shielding layer was then opened using plasma etching. The interdigital electrodes (IDEs) were subsequently created by patterning a 2 µm thick sputtered Al layer. The photolithography process adjusts the electrodes' spacing in the range of 1 to 2 µm. The underlying TEOS layer was then etched correspondingly through the IDEs gaps to make space for the target encapsulation material. The etching area was limited to intervals between the metal fingers, which is determined by using a dedicated photo mask. The bonding pads have been protected in wafer molding by exposing a 200 µm polyimide layer and creating through polymer vias (TPV). In this design, the sensor pads were confined by SU-8 3050 layer, which is an epoxy-based negative photoresist. The SU-8 pillars, as described in Fig. 3, keep the bonding pads uncovered for wire-bonding purposes after EMC coating. The photo-sensitive SU-8 layer was manually coated and baked in two successive steps; each created 100 µm thickness. The soft baking was done at 95 ˚C for 45 min after each spin-coating step. To reach the acceptable layer uniformity (+/- 10 µm) for a successful EMC coating, the outer ring of the wafer was excluded from the exposure, which creates the most thickness non-uniformity. After ultraviolet (UV) exposure for 120 s, the post-exposure bake (PEB) was carried out at 65 ˚C for 1 min and 95 ˚C for 5 min. Therefore, the exposed parts were cross-linked, and the remaining parts were removed by propylene glycol methyl ether acetate (PGMEA) during 20 min long development. Finally, the developed layer was hard-baked at 150 ˚C for 2 hours. The SEM imaging of the SU-8 TPVs is reported in Fig. 4.

The structure is then molded by EMC as the sensing dielectric material. The in-situ reliability experiments are carried out to track the humidity absorption/desorption properties of the encapsulation layer. As a result, an in-situ humidity-monitoring device with high sensitivity is proposed to characterize the humidity uptake and provide data for further reliability investigations of semiconductor packaging materials. The proposed design can further monitor the aging properties of novel packaging materials



(a) (b)

Fig. 1. (a) Previously proposed SIDE sensor and (b) its cross-section.



1 2 3

Fig. 2. IDE capacitive sensor design layouts.

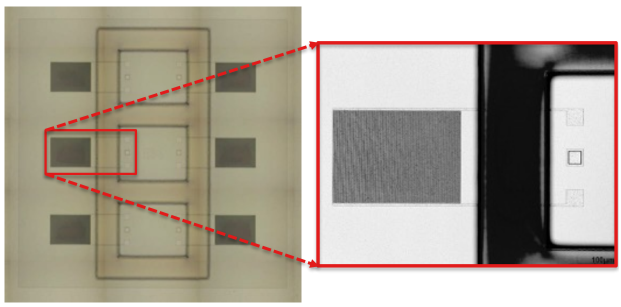


Fig. 3. The SEM imaging of the humidity sensor chip.

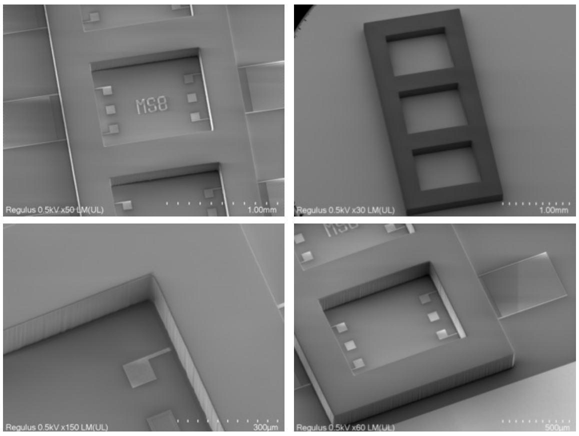


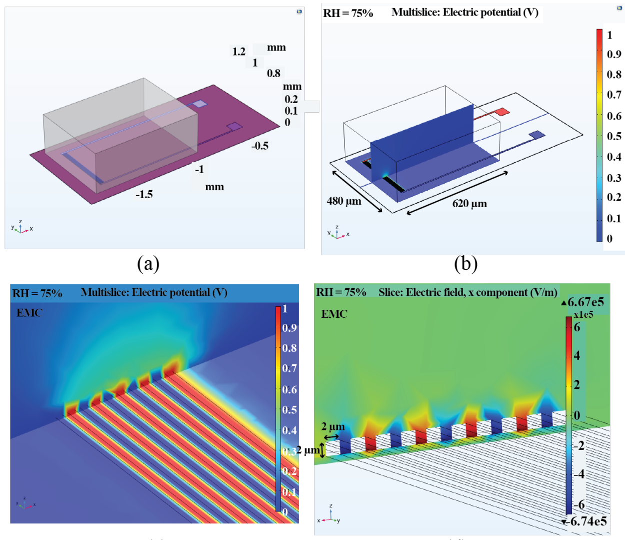
Fig. 4. The SEM imaging of the SU-8 TPVs.

in power cycling or radio frequency (RF) domain, such as 5G communication chips, where the dielectric properties of EMC play a vital role in the overall performance of the device.

3. Results and Discussion

The proposed capacitive sensor comprises interdigital metal electrodes developed on a dielectric layer and a metal shielding electrode underneath. The design employs materials and structures that are common in the back-end metallization. To further illustrate the effects of the moisture uptake, the sensor has been simulated in COMSOL Multiphysics. Fig. 5(a) shows the model in three dimensions. The maxwell capacitance and other relevant properties are calculated and plotted in Fig. 5 (b) to (d), while the shielding layer is grounded. Only five electrode pairs have been considered in the model to simplify the meshing grids and reduce the simulation time. The interdigital electrodes (IDE) are covered with EMC as the target packaging material. The dielectric constant of EMC increases linearly with moisture uptake, which is represented by an experimental equation in the simulations.

The design concerns maximizing the electrical field lines to pass through the EMC and enhancing the sensitivity. Fig. 6 shows the linear capacitance change with the relative humidity level. The manufactured wafer, including 6x6 mm^2 dies and SU-8 TPVs, is shown in Fig. 7. Each die contains six identical capacitive sensors. The IDEs cover an area of 480 x 620 µm^2. The final wafer, which is locally molded by EMC, is illustrated in Fig. 8. The nominal capacitance of the device is measured using a semi-automatic probe station which is reported In Fig. 9. The measurements were carried out in two steps before and after molding to extract the parallel capacitance and conductance. Three designs were measured and compared, and the calibration results are summarized in Fig. 10 and Table 1. An example of the capacitance value before molding is 1.54 pF. The relative dielectric constant is increased by approximately a factor of four after molding TPVs with EMC. Therefore, the final capacitance value is 5.85 pF. The proposed device provides the in-situ reliability monitoring of the encapsulation layer, in this case, the EMC. The absorbed/desorbed humidity changes the dielectric constant of the EMC, and the sensor's unique design



(a) (b)

(c) (d)

Fig. 5. (a) The device model in COMSOL Multiphysics (b),(c) The electric potential, (d) The electric field.

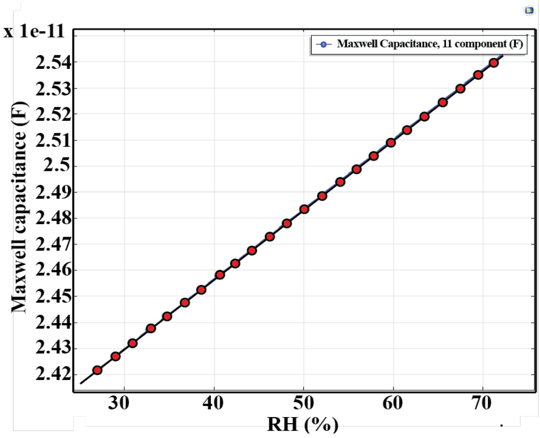
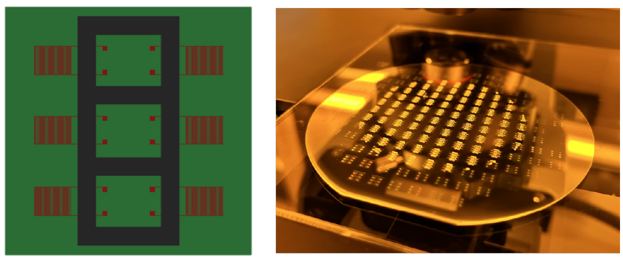
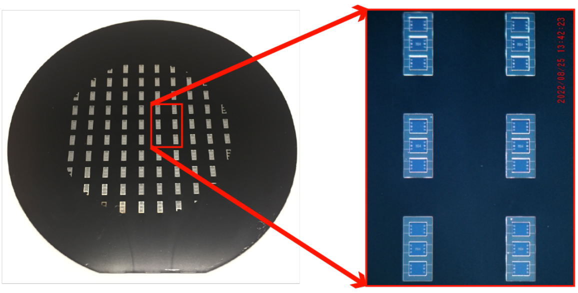


Fig. 6. The linear capacitance change vs. the relative humidity (RH).



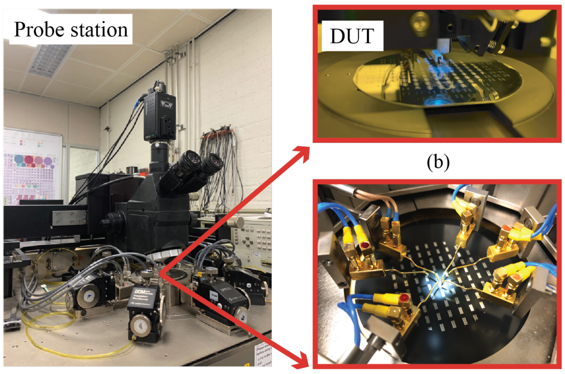
(a) (b)

Fig. 7. (a) The chip layout, (b) The processed wafer with TPVs before molding.



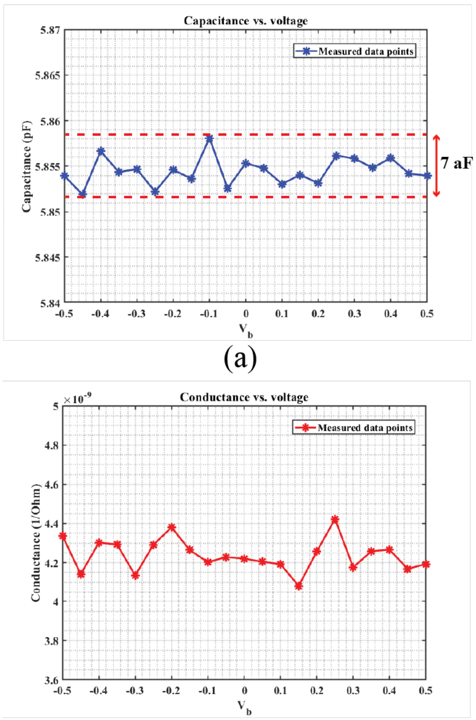
(a) (b)

Fig. 8. (a) The processed wafer after molding, (b) die images (Due to the limitations in the high aspect ratio of the photolithography, only the central part of the wafer is processed.)



(a) (b) (c)

Fig. 9. (a) The measurement setup (probe station or climate chamber), (b),(c) the device under test (DUT).



(a)

(b)

Fig. 10. The measurement results (a) parallel capacitance, (b) parallel conductance

Table 1. Sensor Calibration Results

	MS1	MS2	MS3
Capacitance before molding (pF)	1.54	0.98	3.6
Capacitance after molding (pF)	5.85	3.95	14.5
Conductance before molding Ω^{-1}	1.25 e-10	1.57 e-10	1.18 e-10
Conductance after molding Ω^{-1}	4.25 e-9	2.5 e-9	2.11 e-9
Sensor Size (μm^2)	480 x 620	480 x 620	480 x 620
Die Size (mm^2)	6 x 6	6 x 6	6 x 6
Sensors per die	6	6	6

enhances the sensitivity of the humidity sensor. The shielding layer is grounded by its dedicated contact pad, eliminating the effect of parasitic capacitances through the PECVD TEOS from both sides of the electrodes.

As shown in Fig. 10, the tolerance of the capacitance value under different biasing voltages stays within the range of 5.85 to 5.86 pF with less than 7 aF variation, indicating the stability and robustness of the capacitance.

4. Conclusions

The proposed in-package relative humidity sensor, including shielded interdigital electrodes, allows for the in-situ reliability monitoring of the epoxy molding compound (EMC) or other encapsulation layers. The novel fabrication approach maximizes the electrical field lines to pass through the EMC and enhances the sensitivity. The proposed design alleviates the trade-off between the sensitivity and response time of the capacitive sensor. The device can further monitor the aging properties of novel packaging materials in power cycling or radio frequency (RF) domain, such as 5G communication chips where the dielectric properties of EMC play a vital role in the overall performance of the device.

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