Guest Editorial Introduction to the Special Section on the 2025 IEEE International Solid-State Circuits Conference (ISSCC)

THIS Special Section of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) showcases a selection of exceptional articles presented at the 2025 IEEE International Solid-State Circuits Conference (ISSCC), held in San Francisco, CA, USA, from February 16 to 20, 2025. Under the conference theme, "The Silicon Engine Driving the AI Revolution," ISSCC reaffirmed its role as the premier global forum for innovations in solid-state circuits and systems-on-chip (SoCs), drawing together engineers and researchers at the forefront of integrated circuit (IC) design and its wide-ranging applications.

ISSCC 2025 offered a comprehensive technical program that spanned cutting-edge developments in analog, mixed-signal, digital, radio frequency (RF), and power management circuits, with applications across diverse fields. This JSSC Special Section highlights articles that delve deeper into key topics from the conference, specifically focusing on analog, power management, data converter (DC), RF, and wireless circuits.

With an acceptance rate of approximately 27%, ISSCC 2025 attracted over 2000 in-person attendees. From the rich pool of conference presentations, 30 outstanding articles were selected for this Special Section: six from the analog track, nine from power management, four from DC, seven from RF, and four from the wireless subcommittees. These articles, having undergone a rigorous peer-review process, expand on the original conference presentations and offer deeper insights into their respective fields, as detailed in the following.

The analog subcommittee selected six articles. The first article, by Cyue et al. from National Cheng Kung University, Tainan, Taiwan, reports a class-D audio amplifier achieving a 121.3-dB dynamic range and 0.0019% total harmonic distortion (THD) $+N$, based on a double-sided voltage-boosting modulation scheme. This work delivers up to 1.6 W into an 8-Ω load with a peak power efficiency of 87.2%. The second article, by Siemssen et al. from Leibniz University Hannover, Hannover, Germany, presents a three-in-one multimode, trimming-free amplifier achieving a logarithmic conformity error of 0.75% over a temperature range from -25 °C to 200 °C. The third article, by Heel et al. from the University of Twente, Enschede, The Netherlands, reports a 12.8-GS/s 4$\times$ time-interleaved track-and-hold front end implemented in 22-nm fully depleted silicon-on-insulator (FDSOI), achieving a 38-GHz signal bandwidth and an signal-to-noise-and-distortion ratio (SNDR) greater than 39 dB without skew calibration. The fourth article, by Wang et al. from Hong Kong University of Science and Technology, Hong Kong, China, presents a 32-kHz crystal oscillator employing amplitude-controlled conduction-angle class-C operation for energy-efficient intrinsic start-up, achieving 360-nW power consumption within an 820-μm^2 core area. The fifth article, by Wu et al. from Zhejiang University, Hangzhou, China, in collaboration with Vango Technologies, Hangzhou, describes a bandwidth- and power-scalable continuous-time sensor interface. This work, based on a frequency-controlled current source, allows a 225$\times$ tunable sampling-frequency range and achieves up to 85-dB SNDR. The last article, by Pan et al., is a collaboration between Tsinghua University, Beijing, China, and CoSensing, Utrecht, The Netherlands. It proposes a continuous-time capacitance-to-digital converter for floating-target displacement sensing. By processing the input capacitance in the phase domain, the converter achieves a 143-dB dynamic range and a common-mode rejection ratio exceeding 119 dB near dc.

The power management sub-committee selected nine outstanding articles this year. The first article by Shengdao et al. from Zhejiang University presents a two-stage converter featuring a regulated resonant switched-capacitor (ReSC) second-stage design, achieving a system peak efficiency of 89.3% for 12:1-V conversion with an undershoot voltage of 26 mV at 4-A/20-ns load current step. The second article by Jongbeom et al. from the University of California at Berkeley, Berkeley, CA, USA, demonstrates a supply-modulated power amplifier (PA) system architecture that utilizes a 20-ns/V transition time symbol-power-tracking (SPT) technique realized through a single-inductor multiple-output (SIMO) dc–dc converter, supporting a 400-MHz 5G FR2 64-quadratic-amplitude modulation (QAM) signal at 28 GHz. The third article by Fei et al. from the University of Macau, Macau, China, introduces a switched-capacitor (SC)-based non-isolated ac–dc power converter that combines a Sigma-SC rectifier and floating-SC dc–dc converter, obtaining a peak efficiency of 81.3% and a maximum power of 1.52 W with 739-mW/cm^3 power density. The fourth article by Yuchen et al. from Delft University of Technology, Delft, The Netherlands, presents an inductor-less, capacitor-less piezoelectric-electromagnetic (PE-EM) hybrid energy harvesting platform providing dual regulated outputs at 1.8 and 5 V, achieving a maximum output power of 2.72 mW and a peak end-to-end efficiency of 90%. The fifth article by Tian et al. from the University of Macau

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presents a 180-MHz isolated dc–dc converter using a PG downsized class-D PA that achieves a 45.3% peak efficiency and a maximum output power of 1 W, complying with the CISPR-32 class-B standard. The sixth article by Yunho et al. from Korea University, Seoul, South Korea, demonstrates an always-half-inductor current hybrid bidirectional converter (AHI-HBC) that only uses 5-V transistors for USB-to-2-cell bidirectional power transfer, obtaining peak efficiencies of 97.4% (96%) in the forward mode and 97% (96.2%) in the on-the-go mode with an inductor dc resistance of 11.5 mΩ (295 mΩ). The seventh article by Woojin et al. from Samsung Electronics, Hwaseong, South Korea, presents a dual-input bidirectional three-level battery charger that supports battery charging while supplying the wireless power sharing device at the same time, achieving a seamless bidirectional operation with a well-balanced VCF, a peak charging efficiency of 96.8%, and a maximum voltage conversion ratio of 92.9%. The eighth article by Jianqiang et al. from Iowa State University, Ames, IA, USA, introduces a small form-factor single-link multi-domain-output (SLiMDO)-isolated dc–dc converter that provides two regulated outputs in separate domains in the receiver (Rx) side with a single microtransformer demonstrating a 62.6% peak efficiency at ~600 mW, a 1.13-W maximum power, and a decent load transient response. The final article by Wenjie et al. from the University of Macau presents a high-voltage power delivery cable network, which utilizes two bidirectional dual-path boost–buck (DP-BB) converters and reuses the parasitic inductance of 2-m 28AWG cable as the power inductor, achieving a peak power conversion efficiency of 96.7% at 16.5-W output power.

In the DC subcommittee, four articles were selected, presenting recent advances in successive approximation register (SAR)-based analog-to-digital converter (ADC) architectures that deliver significant improvements in precision, bandwidth, power efficiency, and application diversity. The first article, from Peking University, presents a calibration-free pipelined-SAR ADC employing a cross-stage gain-mismatch error-shaping (CS-GMES) technique, which unifies inter-stage gain and second-stage capacitor mismatch errors through a single shaping loop. A negative-R-assisted residue integrator replaces the conventional amplifier to enable efficient residue summation and first-order error-feedback noise shaping. Fabricated in 55-nm CMOS, the prototype achieves 93.3-dB SNDR and 180.4-dB figure of merits (FoMs) within a 156.25-kHz bandwidth while consuming 307 μW, without any off-chip calibration. The second article, from Tsinghua University, introduces a filter-embedded pipelined-SAR ADC that achieves 70.1-dB SNDR over an 80-MHz filter bandwidth while consuming 4.9 mW, resulting in a 172.2-dB Schreier FoM. A progressive conversion technique overcomes the conventional speed limitation by parallelizing the filtering and SAR quantization. A floating charge transferrer (FCT) is also developed as a dynamic open-loop residue amplifier, providing high speed, low power, and strong process, voltage and temperature (PVT) robustness. Fabricated in 28-nm CMOS, the prototype demonstrates >30-dB out-of-band blocker suppression and scalable bandwidth without *RC* tuning, positioning it as a compelling alternative to continuous-time $\Delta\Sigma$ modulators in broadband wireless Rxs. The third article, from the University of Macau, reports a 72-GS/s 9-bit 64-way time-interleaved pipelined-SAR ADC implemented in 16-nm FinFET technology. The ADC features common-source-compensated source-follower buffers and split bootstrap switches for enhanced bandwidth and linearity, achieving 55.3-dB SFDR at a 20-GHz input. Using an R/R-network-embedded open-loop residue amplifier, this design extends SAR-based pipelined architectures into the multi-tens-of-GHz regime, demonstrating its suitability for optical communication front ends. The final article, from KU Leuven (ESAT-MICAS), presents a Cryo-CMOS 7-bit charge-injection SAR (CI-SAR) ADC operating with only 4-fF input capacitance that exploits the low thermal noise of cryogenic environments. Implemented in 40-nm CMOS, the ADC occupies a core area of 0.0056 mm^2 and achieves an SNDR of 40.7 dB with an effective resolution bandwidth (ERBW) of 2.5 GHz at a sampling rate of 800 MS/s and a temperature of 6.5 K. This compact and energy-efficient ADC demonstrates the feasibility of CMOS converters for quantum-computing readout and low-temperature sensing applications.

The RF sub-committee selected seven outstanding articles for this year's Special Section, seven of which were accepted. The first article, by Zhang et al. from the University of Tokyo, Tokyo, Japan, presents a cascaded fractional-*N* phase-locked loop (PLL) with an auxiliary multi-modulus divider (MMD) inserted between the first-stage integer-*N* and second-stage fractional-*N* loops, effectively suppressing both quantization noise and in-band fractional spurs caused by phase-detector nonlinearity. With an 82-MHz reference, the PLL achieves 96-fs root-mean-square (rms) jitter and −70.6-dBc worst-case in-band fractional spur while consuming 21.2 mW, corresponding to a jitter FoM$_J$ of −247.1 dB. The second article, by Livanelioglu et al. from ETH Zürich, Zürich, Switzerland, introduces an integer-*N* PLL co-designed with its crystal oscillator (XO) to achieve ultra-low-noise and power-efficient frequency synthesis through bidirectional signal interaction. The XO provides a clean reference to the PLL, while the PLL precisely times pulse injection into the XO at low impulse-sensitivity-function (ISF) regions. Fabricated in 22-nm FDSOI technology, the PLL achieves 63.3-fs rms jitter, a −255.2-dB FoM$_J$, and reference spurs below −69 dBc at 4.6 GHz. The third article, by Gallucci et al. from the Politecnico di Milano, Milano, Italy, presents a digital integer-*N* PLL featuring an adaptive common-mode resonance tuning technique for a voltage-biased digitally controlled oscillator (DCO). By detecting and nullifying the oscillator's frequency sensitivity to a dither signal, the loop continuously self-adjusts to minimize phase noise across the tuning range. Fabricated in 28-nm CMOS, the prototype achieves 45.9-fs jitter, −146.6-dBc/Hz phase noise at a 10-MHz offset from a 4.75-GHz carrier, and a −257-dB FoM$_J$. The fourth article, by Chae et al. from Seoul National University, Seoul, presents a 10.0–11.5-GHz fractional-*N* digital PLL using a quantization-error-compensating bang–bang phase detector to minimize static and dynamic delays required for removing the delta-sigma modulator's quantization error. Moreover, an orthogonal-polynomial least-mean-squares (LMS) calibration accelerates the phase detector nonlinearity compensation with minimal hardware. Fabricated in 40-nm CMOS, the 0.12-mm^2

DPLL consumes 14.4 mW, achieving 64-fs jitter, −62.8-dBc fractional spur, and a −252.2-dB FoM_J. The fifth article by Wang et al. from Nanjing Electronic Device Institute, Nanjing, China, presents a G-band PA implemented using 50-nm gallium nitride (GaN) high-electron mobility transistor (HEMT) technology. Employing multi-band large-signal impedance correction, power combining, and circuit-package co-design techniques, the PA delivers over 1-W saturated output across 216–226 GHz, with a power gain exceeding 9 dB. The sixth article, by Lv et al. from Beijing Institute of Technology, Beijing, China, presents an ultra-wideband back-off efficient switchless-class-G-Doherty-continuum PA. It combines the broadband potential of a switchless class-G PA with the efficiency of a Doherty PA through a frequency-adaptive transmission line. When driven by a 100-MHz LTE signal with a 7.5-dB peak-to-average power ratio (PAPR), the PA, fabricated in 0.25-μm GaN HEMT, achieves an average drain efficiency of 35%–49.2% across the full 1.35–7.6-GHz bandwidth, with adjacent-channel power ratios (ACPRs) of −46 dBc. The seventh work, by Zhang et al. from the Institute of Science Tokyo, Tokyo, presents a digital polar transmitter (TX) that enhances efficiency and linearity by reducing signal bit count. Multi-bit I/Q inputs are oversampled and quantized into three-level signals via delta-sigma modulators, then mapped through a nine-state lookup table to generate amplitude (AM) and phase (PM) signals. The AM drives a 1-bit linear PA, while the 3-bit PM is generated via edge selection from a 4× carrier local oscillator (LO). Fabricated in 65-nm CMOS, the TX supports 50-Msymbol/s 256-QAM signals and achieves −25.1-dB error vector magnitude (EVM) at 24.5% maximum system efficiency.

The wireless subcommittee has selected four outstanding article this year. The first article by Yang et al. from the University of Southern California, Los Angeles, CA, USA, presents a 31–34-GHz blocker-tolerant Rx that uses an N-path front end and a voltage-controlled oscillator (VCO)-based integrator in the BB implementing multi-level time approximation filtering, non-uniform sampling, and analog-to-digital conversion. The combined techniques allow for creating programmable notches in the frequency response. Implemented in a 28-nm CMOS process, this work reports 55-dB average blocker rejection across the alias band and achieves blocker 1-dB compression point (B1dB) of −3.3 to 9 dBm. The second article by Mahapatra et al. from the University of Southern California introduces a 24-GHz direct digital TX with a multi-phase sub-harmonic switching TX that targets to enhance peak and back-off efficiency at higher data rates. A phase-shifted sub-harmonic LO divider is used to mitigate sub-harmonic spurs with low implementation overhead. This work achieves 19.8-dBm peak output power and 38.3/15.2% peak/−12-dB power-added efficiency (PAE). The third article by Zhang et al. from East China Normal University, Shanghai, China, reports a 77-GHz hybrid TDMA-multi-in multi-out (MIMO) phased array radar that can cater to short-, medium-, and long-range radars using different chirp profiles to maximize detection range or range resolution. A zig-zag multiple sub-bands chirp generation technique is proposed to avoid chirp discontinuity at band edges and reduce K_VCO. Fabricated in a 55-nm CMOS process, this work achieves a maximum 186-m detection range, or can be reconfigured to provide a 3-cm range resolution. The fourth article by Abdelmagid et al. from ETH Zürich presents a 120-GHz 4×4 active reconfigurable reflective relay array with compact on-chip antennas that can enable D-band non-line-of-sight (NLOS) wireless communication links. Implemented in GlobalFoundries 22-nm FDSOI CMOS, +/−35° scan range, and 10-μs angle-of-arrival (AoA) detection latency is demonstrated, supporting a 1.3-m wireless link with 64-QAM 6-Gb/s data rate and 5% EVM.

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